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Study of Analog Compensation Techniques for Highly-Integrated Wireless Transceivers

Toshiya Mitomo

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Chapter 1

General Introduction

1.1 Introduction

Wireless applications have spread widely in recent years. As shown in Fig. 1.1, only one or two wireless systems for broadcasting services, e.g. television and radio, were used per user 15-20 years ago. Personal cellular phone terminals have become widely used and the number of wireless transceivers (TRXs) in a cellular phone has increased in the last decade. Various wireless systems for data transfer, authentication, radio frequency identification (RFID) tag and wireless sensors for health care, smart houses and so on are expected to become widespread in the ubiquitous network society. Of course, such wireless systems should be very small, low cost and also have small power consumption for incognizant usage by users.

In addition, as shown in Fig. 1.2, the data rate of the wireless system is increasing. In this situation, very high carrier frequency (f_C) and/or multi input and multi output (MIMO) systems [1] are adopted to obtain fast data rate. Therefore, reduction in size, cost and power consumption of high-frequency circuits is also very important for realizing ubiquitous networking society.

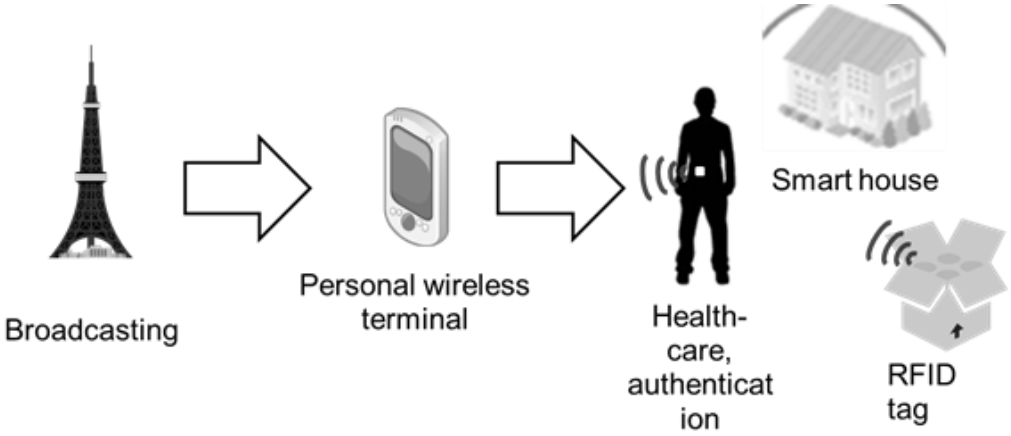


Figure 1.1: Transition of wireless applications.

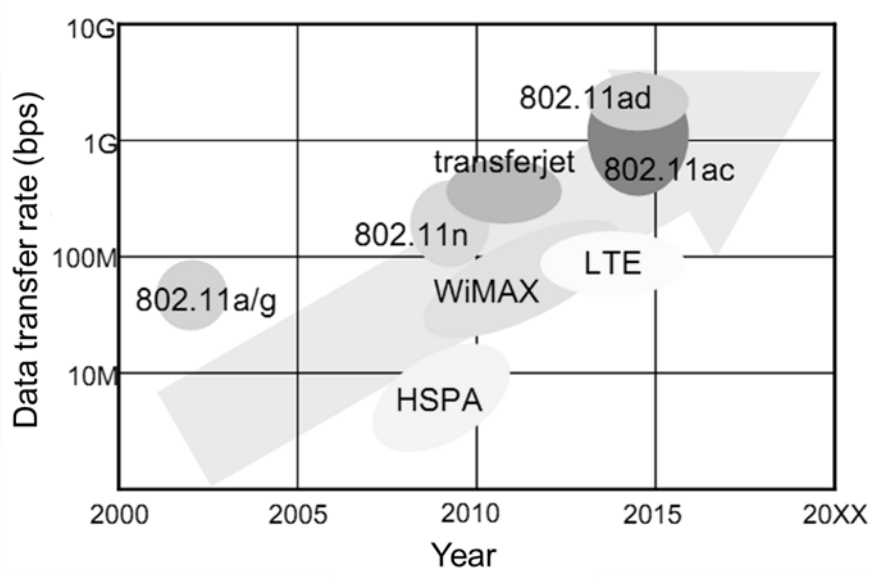


Figure 1.2: Advance of wireless data transfer.

Fig. 1.3 shows an example of a block diagram of a wireless system. In a transmitter (TX) part, a digital baseband (BB) signal in a digital baseband block (DBB) is converted to an analog signal by digital-to-analog converter (DAC). The converted analog signal is filtered and up-converted to high-frequency by a filter circuit and a quadrature modulator (QMOD), respectively. For frequency conversion, local oscillation (LO) signal is required. The up-converted signal is amplified to the desired transmitting signal level by a TX variable gain amplifier (VGA) and a power amplifier (PA). In order to transmit the signal efficiently, power matching between a PA and an antenna is required.

In a receiver (RX) part, high-frequency input signal from an antenna is amplified with a low-noise amplifier (LNA). In order to optimize gain and noise figure (NF) of the LNA, a matching circuit is required between the antenna and the LNA. The amplified high-frequency signal is down-converted to baseband by using a quadrature demodulator (QDEMOD). The same as for the TX part, an LO signal is required for the down-converting function. Undesired adjacent channel signal in the down-converted signal is filtered by BB low-pass filter and the filtered signal is amplified to the required input level of the analog-to-digital converter (ADC) by an RX VGA. Finally, the converted signal is demodulated by the DBB block.

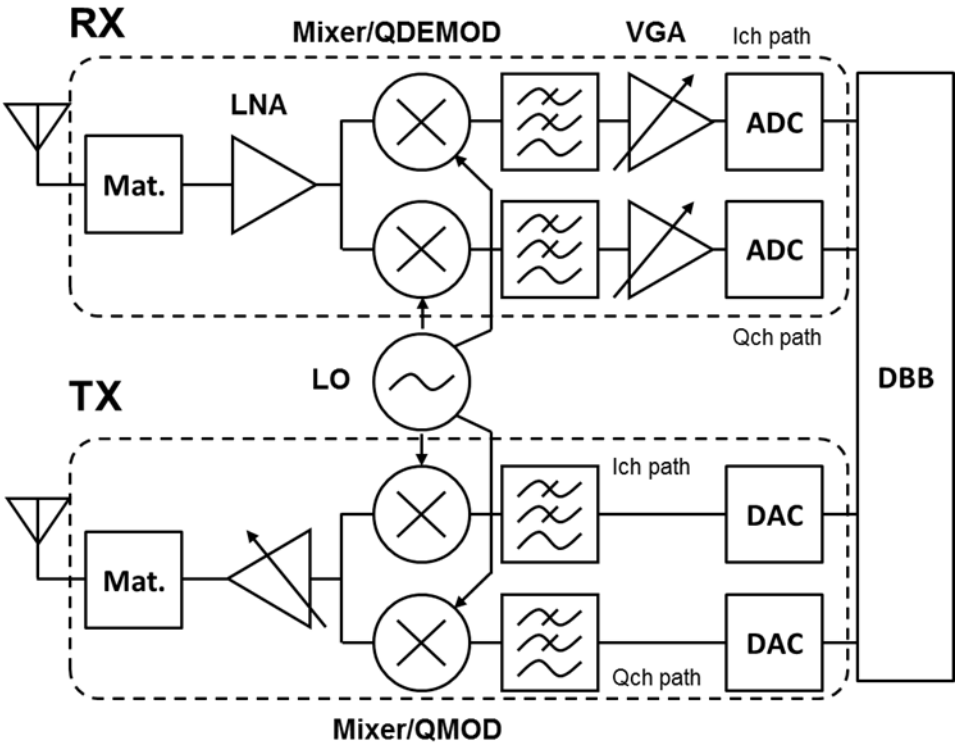


Figure 1.3: Block diagram of a wireless system.

In order to realize the widespread use of consumer wireless applications, a small and low-cost solution is strongly desired. One of the effective solutions is to reduce the number of components of a wireless TRX. A TRX system using individual components for each function is not allowable. Integrating the TRX function blocks to the silicon IC as shown in Fig. 1.4 is an effective solution for a small and low-cost wireless system. It means realizing a TRX by integrating as many components as possible and the integration is particularly effective when employing many wireless TRXs in consumer products. The number of components can be drastically reduced by integrating these wireless systems to one or a few ICs. However, some serious problems arise if the TRX is integrated with approaches which are same as that of the TRX based on discrete components.

An objective of this dissertation is leading correct selections of proper solution for issues concerning integration of wireless systems. In order to assist designers who are trying to integrate wireless TRXs, major issues and solutions concerning the integration of high-frequency analog circuits are explained in the following sections.

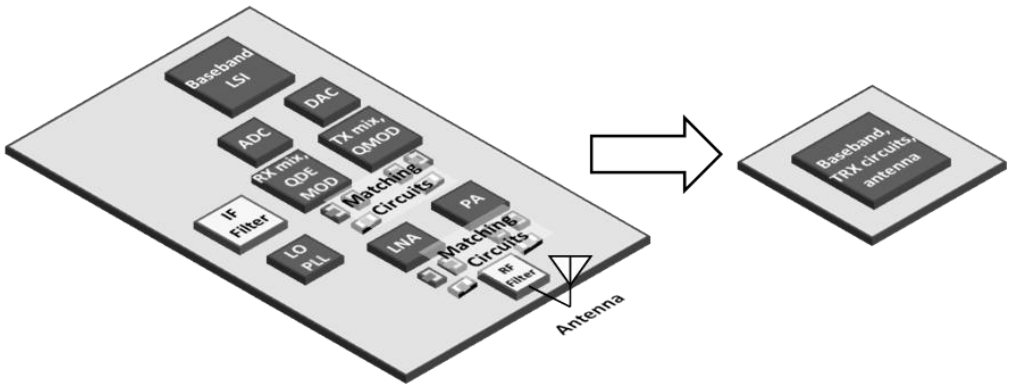


Figure 1.4: Integration of components for wireless system.

1.2 Issues Concerning Integration of High-frequency Analog Circuits

The major issues concerning integration of high-frequency analog circuits are, PVT variation, high-frequency signal leakage and insufficient performance of integrated devices. In the following subsections, these problems are described in detail.

1.2.1 PVT Variation

Process, supply voltage and temperature (PVT) variation is one of the major issues concerning integration of high-frequency circuits. In the case of active devices in silicon process, NMOS transistor for example, the drain current I_D of the saturation region is basically given by the following equation [2].

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\,(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \qquad (1.1)$$

In the equation, the geometry L and W, threshold voltage V_{th}, gate oxide capacitance C_{ox}, carrier mobility μ and channel length modulation coefficient λ have variations due to process variation caused mainly by geometry/thickness error and impurity doping density error. Supply voltage variation corresponding to drain-to-source voltage V_{DS} variation changes the operating point of the active devices. Temperature change makes drain current drift owing to V_{th} and μ variation. Such an operating point variation causes degradation of high-frequency performances of active devices, e. g. gain, NF and linearity. Furthermore, the parasitic capacitance and resistance of a transistor, which have impacts on high-frequency performance, change under process variation. Transition frequency (f_T) and maximum oscillation frequency (f_{max}) of a transistor are shown in the following equation [2], [3] and the value depends on the value of parasitic elements in a high-frequency equivalent circuit of a transistor as shown in Fig. 1.5.

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}},\ f_{\max} = \frac{g_m}{4\pi}\sqrt{\frac{R_o}{(C_{gs}+C_{gd})(\sqrt{2}g_m R_o C_{gd}+C_{gs}+C_{gd})R_g}} \qquad (1.2)$$

Where g_m is transconductance of the transistor, R_o is output resistance, C_{gs} is parasitic capacitance between gate and source, C_{gd} is also parasitic capacitance between gate and drain, and R_g is parasitic resistance of gate. As mentioned above, PVT variation changes DC and AC characteristic of the active devices and it has a particularly large impact for active devices adopted for high-frequency operation. Characteristics of passive devices on a Si die, resistor, capacitor and inductor, are also influenced by process and temperature variation. Resistivity of the polysilicon and thickness of metal layer vary under process variation. And the resistance of polysilicon and metal layer vary under temperature change in accordance with their temperature coefficients. These variations result in resistance, impedance and quality-factor variation or degradation. Furthermore, the performance mismatch within multi-devices causes other problems.

Such PVT variation causes various performance degradations in integrated wireless TRXs. Figure 1.6 shows an example in a wireless RX. Gain, noise performance and linearity are varied and degraded in whole analog circuits in the RX owing to variation of the operating point of the active devices, load resistance and so on. Parameter mismatch causes offset and even order distortion between pair devices, e.g. differential pair circuit. Additionally, quadrature accuracy in the output of the QDEMOD, filtering performance of the channel selecting filter, gain control linearity in the variable gain amplifier, resolution in the ADC and oscillation margin of the LO generator are degraded by PVT variation.

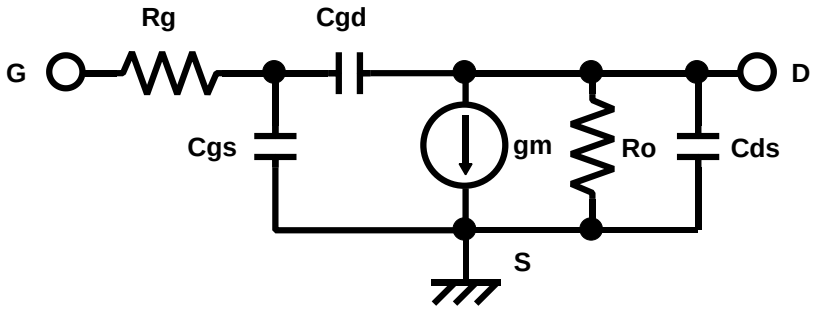


Figure 1.5: Simplified transistor equivalent circuit for estimating f_T and f_{max}.

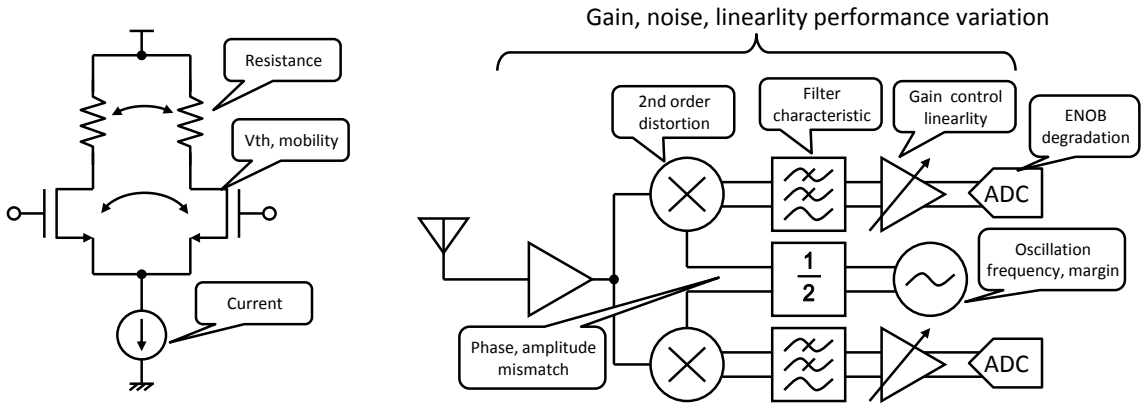


Figure 1.6: Performance degradation caused by PVT variation.

1.2.2 High-frequency Signal Leakage

High-frequency signal leakage in a highly integrated wireless system on a silicon die is also a serious problem. In the case of integration of the multiple high-frequency circuits for integrating an RX and a TX, a multi wireless platform wireless TRX and a phased array/MIMO system, several high-frequency circuits operate at the same time. In such a case, the high-frequency leakage appears and the leaked signal degrades the performance of other high-frequency circuits operating simultaneously. That is because the silicon substrate doped to P or N type does not have enough isolation for high-frequency signals [4], [5]. The substrate is modeled as resistive and capacitive networks as shown in Fig. 1.7. The resistance is not as large as that in the compound semiconductor process. Therefore, a high-frequency signal leaks to various circuits. The signal leakage is larger in the case of a highly integrated wireless TRX because of the smaller substrate resistance due to small distance, only tens to hundreds of micrometers, between high-frequency circuits and strong capacitive coupling with such a high-frequency signal. Such a high-frequency leakage signal causes several problems as explained in the following.

Assuming a direct-conversion RX IC that includes an LO generator and a QDEMOD, the input RF signal is converted to a quadrature baseband signal directly by using the QDEMOD. Since the LO frequency is the same as the carrier frequency of the RF signal, no image signal appears in the BB signal and the image rejection filter for filtering an unwanted signal at image frequency can be removed [6]. The IF band-pass filter for channel selection is replaced by a low pass-filter (LPF) for channel selection in BB. Such an LPF can be integrated in the same die. There are some issues inherent to the adoption of direct-conversion architecture. The LO signal is leaks to the RF signal path via electromagnetic and substrate coupling. The signal is mixed by a mixer circuit and DC offset appears at the output of the mixer. The DC offset causes voltage saturation for the following high-gain VGA. This issue is known as “self-mixing” [6], [7]. Sometimes the LO signal emission by an antenna is also poses a problem with regard to satisfying a legal specification.

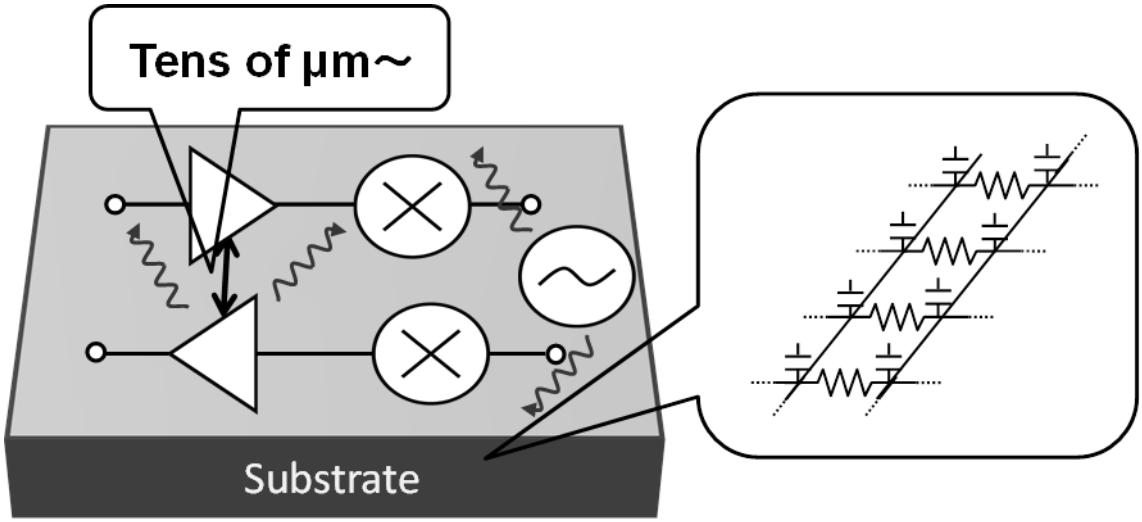


Figure 1.7: High-frequency signal leak via silicon substrate.

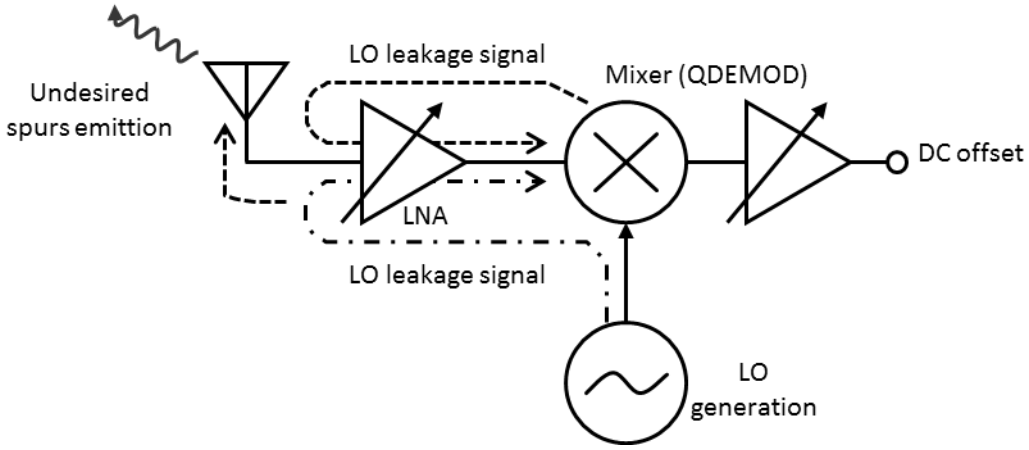


Figure 1.8: LO signal leakage and self mixing.

In order to achieve a TRX with fewer components, integrating a TX and an RX or multiple TX/RX circuits in the same die is one of the effective solutions. In such a case, a serious issue arises concerning the FDD TRXs, MIMO and phased array systems. For example, in a WCDMA system, the carrier frequency of 2140 MHz is allocated for the RX and the 1950 MHz band is allocated for TX. As specified by 3GPP [8], the output power at the antenna is 24 dBm as shown in Fig. 1.9. A duplexer is used for obtaining isolation from the PA output to the LNA input and typical isolation is about 50 dB [9]. Thus -25 to -20 dBm of TX signal leaks to LNA. Such a TX leakage signal has larger power than that of input signal and it degrades the LNA noise performance.

The TX signal also leaks to the RX mixer circuit. The TX signal leaks mainly via substrate resistive/capacitive coupling and electromagnetic coupling. Thus, the leaked signal is a common-mode signal as shown in Fig. 1.9. If the mixer is sensitive to the common-mode TX signal, the TX leakage signal causes unwanted DC voltage drop by even-order distortion because the down-conversion mixer circuit often has resistive load for low-frequency output signal. Such a voltage drop degrades the high-frequency performance of the mixer when using low-voltage supply. In order to integrate the TX and the RX, high isolation is required. A simple and effective approach involves careful floor planning of the TX and the RX and implementation of wide guard ring. A TRX of [10] shows estimated isolation calculated by electro-magnetic simulation is more than 60 dB. On the other hand, a research result of substrate coupling [4], [5] shows the highest isolation is up to 40 dB at 50 μm distance from 50 μm square of noise signal source at 2 GHz. As explained in the references, the isolation is strongly dependent on the actual environment including device parameters of the silicon substrate and layout of circuits and lines. Therefore, it is difficult to estimate isolation with enough accuracy before test chip fabrication.

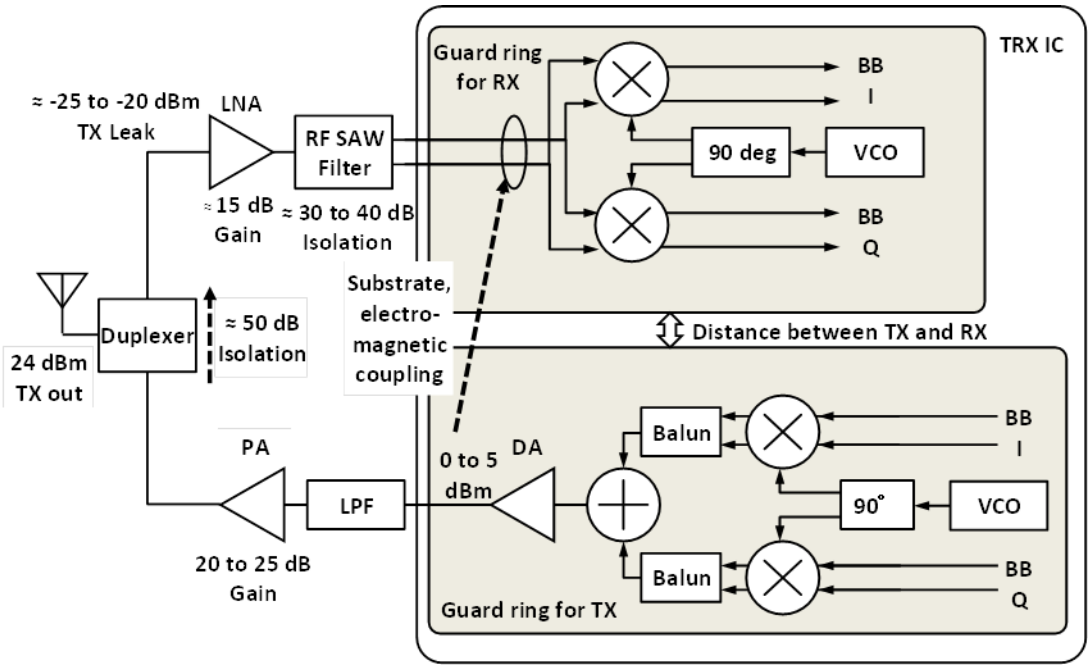


Figure 1.9: Performance degradation caused by TX leakage.

1.2.3 Insufficient Performance of Integrated Devices

Another problem concerning realization of a highly integrated wireless TRX is insufficient high-frequency performance of integrated active and passive devices in silicon. The carrier frequency, f_C of wireless TRXs is increasing every year. Figure 1.10 shows publication numbers of wireless TRX for each carrier frequency from 1995 to 2012 reported in the IEEE Journal of Solid-State Circuits. The peak of each carrier frequency moves to a higher frequency range, year by year. The frequency shift presumably corresponds to trends of high-data-rate wireless or ranging/sensing systems. Of course, the applicable maximum operating frequency of the silicon transistor on a silicon die also has also progressed. Figure 1.11 shows the transition frequency f_T of the transistors in BiCMOS and CMOS processes [11]. f_T of the transistors is proportional to the transconductance of the transistor and inversely proportional to the parasitic capacitance between base/gate and emitter/source terminals. Therefore, recent fine process can make a transistor device with smaller parasitic capacitances and more than 100 GHz f_T has been achieved.

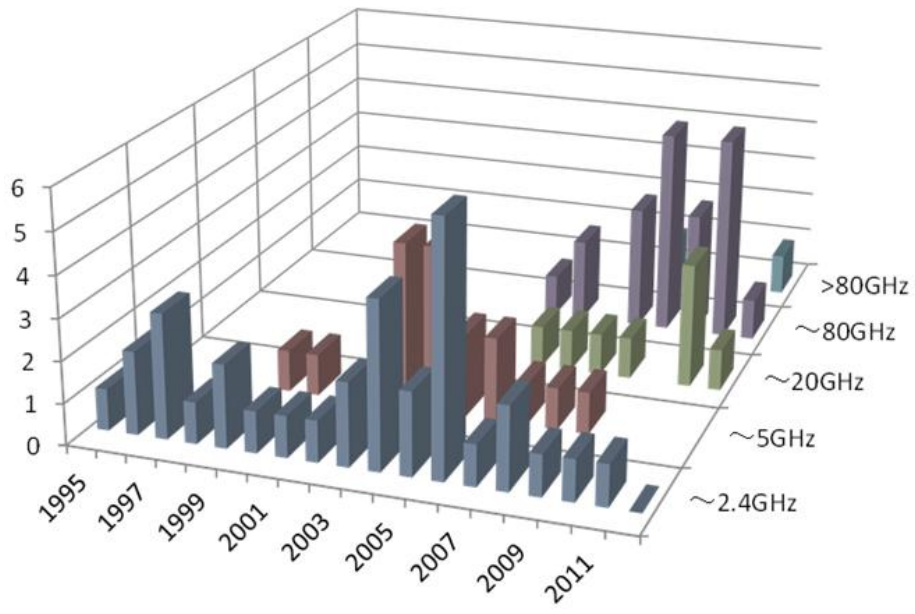


Figure 1.10: Transition of carrier frequency of wireless system.

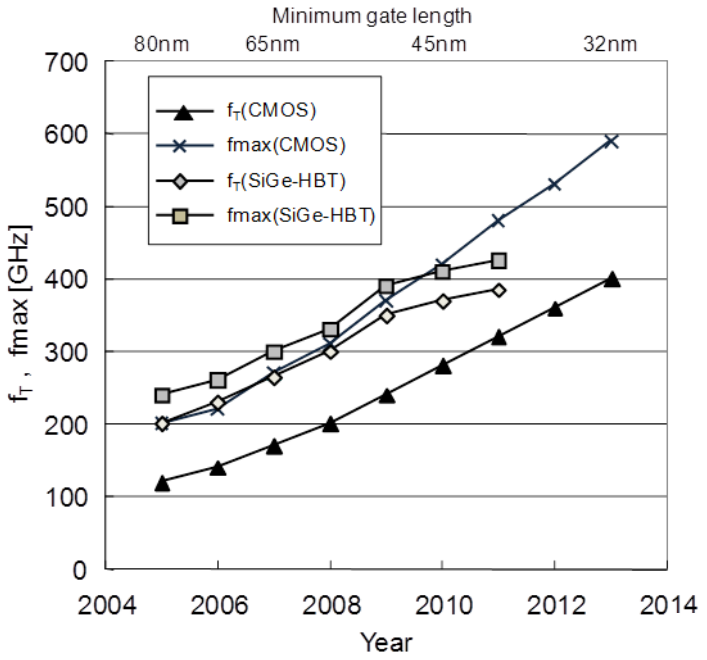


Figure 1.11: Roadmap of transistor operating frequency.

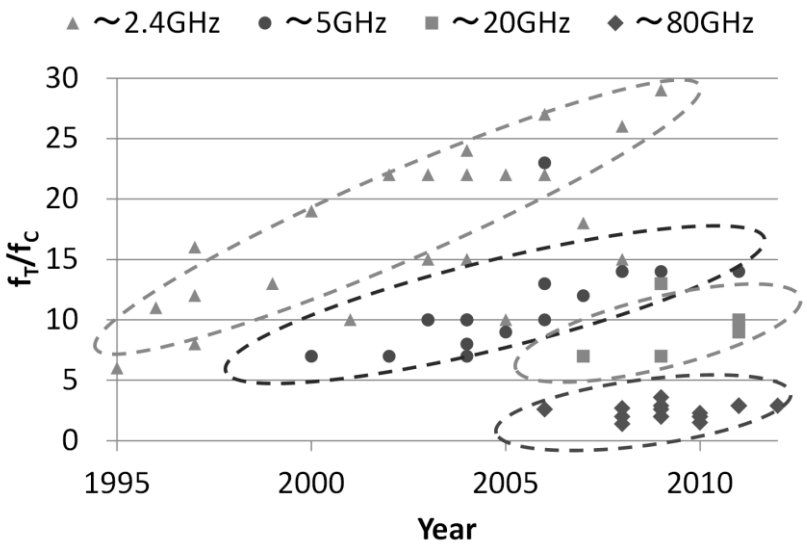


Figure 1.12: f_T and f_C ratio of wireless TRXs.

The ratio of carrier frequency f_C which is shown in Fig. 1.10 and transition frequency f_T is shown in Fig. 1.12. As shown in the plot, the f_T/f_C ratio is low (<10) in beginning years of research in all frequency ranges. The ratio becomes lower for the higher f_C that is larger than 20 GHz and the value is less than 5. In the case of such a low f_T /f_C ratio, the performance of the high-frequency circuit is degraded compared to the case of high f_T /f_C ratio that is larger than 20 for the following reasons.

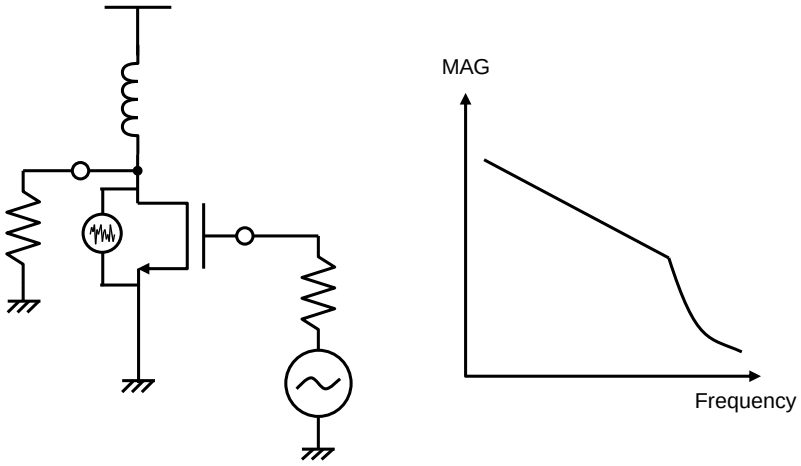


Figure 1.13: High-frequency performance of active devices.

Since the maximum available gain (MAG) is inverse proportional to the frequency as shown in Fig. 1.13 [12], the gain performance is degraded in higher frequency range. In order to obtain maximum gain, the input power source is impedance-matched to the transistor in high-frequency circuits. The gate resistance (base resistance in bipolar) and capacitance reduce the voltage swing between base/gate and emitter/source terminal. Noise performance is also degraded in this case because the desired signal amplitude is reduced. In addition, a similar problem appears even in a relatively low-frequency TRX for very low-power wireless system such as a sensor network [13]. In order to achieve low power consumption, supply voltage and current consumption of the active devices are reduced and the f_T is degraded.

Performances of the passive devices in integrated circuits are also degraded compared to those of the individual discrete devices. For example, an on-chip spiral inductor as shown in Fig. 1.14 has parasitic resistance. The resistance depends on the thickness of the metal layer which is as thin as several micrometers, and substrate resistance, which is relatively low [12]. Therefore the quality factor of the inductor is much less than those of discrete inductor chip devices.

For example, a performance of a high-frequency matching circuit using on-chip inductors is considered. Small transistors are selected for high-frequency circuits to reduce parasitic capacitors for better gain and noise performance. Thus the input impedance of such transistors is typically much higher than characteristic impedance of 50 ohms. The impedance-matching circuit works as an impedance transformer and it is generally composed of inductive and capacitive devices as shown in Fig. 1.15. In the case of impedance matching at the input of the amplifier or mixer, the input resistance of the transistor, R_{tr} is converted to R_{in}, which is equal to the signal source impedance. The efficiency of the matching circuit is approximated by using the following equation [15].

$$\eta = \frac{1}{\frac{r}{Q_{ind}^2}+1} \tag{1.3}$$

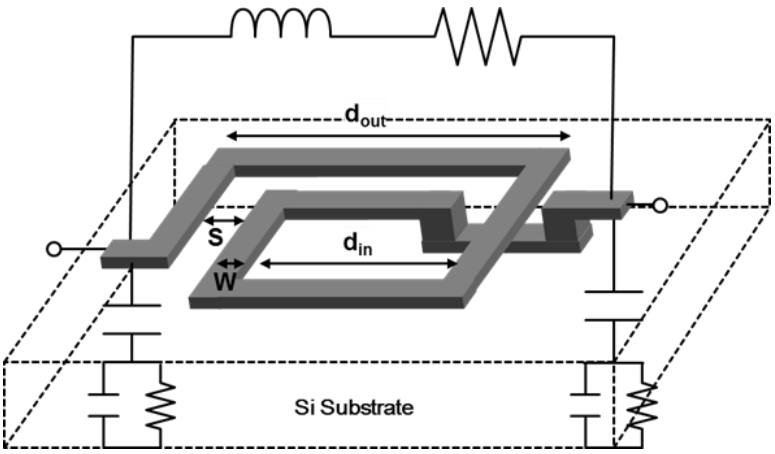


Figure 1.14: Planar on-chip spiral inductor.

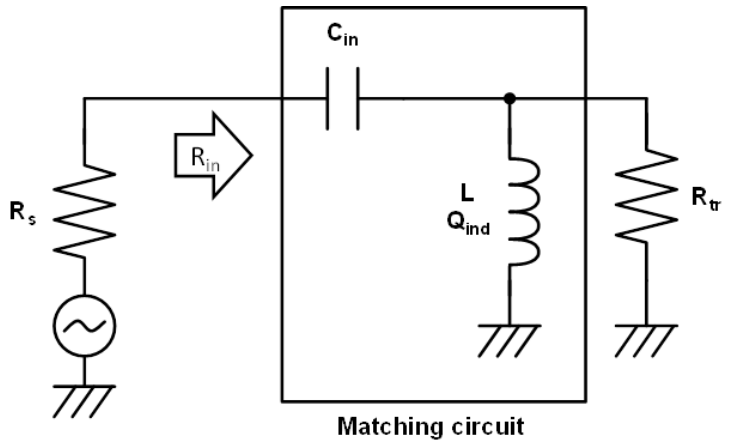


Figure 1.15: Matching circuit using inductive and capacitive devices.

Note that η is the efficiency, r is the impedance-transforming ratio and Q_{ind} is the quality factor of the inductor used in the matching circuit. As shown in the equation, higher Q_{ind} is required for higher impedance-transforming ratio. However, the spiral planar inductor shown in Fig. 1.14 has a small quality factor due to the larger serial parasitic resistance and substrate loss. Thus the efficiency of the matching circuit is degraded compared to the case of using off-chip passive components.

1.3 Solutions for Issues

In order to integrate the high-frequency circuits, the problems explained above should be ameliorated. Some solutions are applied for the problems as shown in the following.

- Applying finer and faster silicon process.
- Applying large devices and circuits.
- Increasing current consumption of the high-frequency circuits.
- Compensation of high-frequency circuit by using digital circuits.
- Compensation of high-frequency circuit by using analog circuits.

1.3.1 Applying finer and faster silicon process

A smaller or thinner transistor structure with smaller parasitic capacitances can be adopted by using advanced process and the f_T can be increased and higher MAG can be obtained. Thus, the gain and noise performance of transistors are improved. On the other hand, more advanced process means higher cost. And if the process with enough f_T is not available, time to market of the desired wireless TRX will be longer.

1.3.2 Applying large devices and circuits

The parameter mismatch between pair devices is inversely proportional to area of the devices [2]. Thus, using larger devices ameliorates the mismatch problem. And the leak problem is ameliorated by using high-frequency circuits with large interdistance on the same silicon die. However, the large devices have large parasitic capacitances and the f_T of such device is reduced. In addition, a large IC chip area increases the cost of the IC chip and package.

1.3.3 Increasing current consumption of the high-frequency circuits

Figure 1.16 shows the relationship between the current density of the MOS transistor and f_T [16]. The MAG of the transistor is also boosted. Thus, the higher gain performance is achieved by increasing current consumption. As shown in the figure, the improvement has a limit because the DC characteristic is saturated. As the power consumption of the high-frequency circuit increases, the internal temperature of the IC chips also rises. This degrades the performance of active and passive devices. This problem is particularly important when several wireless systems operate simultaneously. Furthermore, the power consumption sometimes exceeds the desired specification. Therefore, this method causes problems and it should only be applied in cases where it is unavoidable.

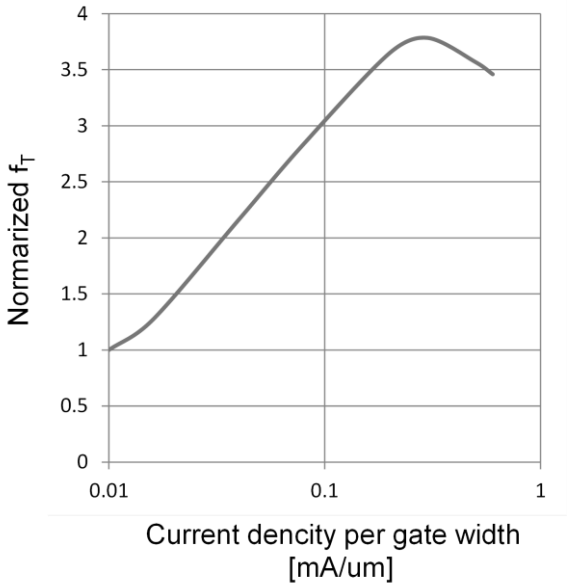


Figure 1.16: Relationship between f_T and current consumption of active devices.

As explained in 1.3.1 to 1.3.3, these methods can improve degraded performances directly. However, adoption of these methods has various drawbacks. On the other hand, compensation techniques for high-frequency analog circuits involving the use of digital or analog circuits, which are mentioned in the following subsections, are expected to have fewer drawbacks than the above-mentioned methods.

1.3.4 Compensation by Using Digital Circuits

Figure 1.17 shows a simplified block diagram of the compensation by using digital circuits [17], [18]. The high-frequency analog circuit that is the target of the compensation has a tuning mechanism for performance variation/degradation. A part of the output signal from the high-frequency analog circuits is monitored by ADCs. The monitored signal is compared to a reference signal that is defined as a digital amount. The digital compensation algorithm outputs a value to compensate the high-frequency circuits. In this way, the varied performance can be compensated. For example, quadrature signal accuracy is compensated by monitoring the baseband signal and controlling the oscillator circuits that generate the quadrature LO signal [19]. In another approach, the cut-off frequency of the channel selection filter is compensated [20].

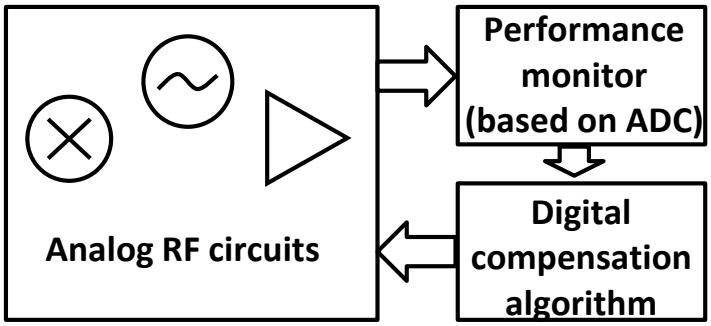


Figure 1.17: Typical structure of the compensating method the performance of high-frequency analog circuits by using digital circuits.

Figure 1.18 shows an example of performance compensation by using a digital circuit for a high-frequency analog circuit [18]. Output amplitude of a VCO at the GHz band is compensated in the example. The output voltage is monitored by a peak detector based on a rectifier circuit and the output is compared to the reference voltage corresponding to the desired VCO output amplitude. The compared result is input to a digital signal processor and it outputs a control signal to tune the current source of the VCO to control the VCO output voltage to desired amplitude. This method is effective for output voltage variation/degradation caused by PVT variation.

This compensation is an effective for dealing with performance degradation by PVT variation. And the ADC for monitor and digital signal processing circuit can be implemented in a small area by finer silicon process. In recent research attempts have been made to realize digital high-frequency circuit blocks including a PLL or TX circuits [21]. In these circuits the signal information is converted from magnitude to time and the sensitivity of high-frequency circuits to the PVT variation can be lowered.

Next, a case of compensation by using digital circuits for problems due to high-frequency signal leakage or insufficient high-frequency device performances is considered. As explained above, analog signal monitoring is required for the compensation technique. In the case of compensation for a performance degradation of a high-frequency analog circuit by high-frequency leak signal, leak signal or degradation of the high-frequency circuit should be monitored.

For example, a situation of monitoring the leakage signal at a frequency of several GHz band, which is very low power and exists with the desired high-frequency signal, is considered. Since it is necessary to distinguish the leakage signal from the desired one, detection of the average power using a simple power detector based on a rectifier is no longer applied. In this case, a high-sampling-rate and high-resolution ADC is required to sense such a high-frequency signal. Recent ADC sampling frequency and resolution are plotted in Figure 1.19 [22]. As shown in the plot, a flash ADC can operate at up to several GHz of sampling clock. However, the resolution of such a

high-sampling-rate ADC is only up to several bits. Such a resolution is insufficient to detect leak signal that is included with the desired signal. In order to improve the resolution in such a high-frequency band, a large-scale circuit and high power consumption are required for the ADC. In addition, the high-frequency analog core circuit should be controlled by a digital compensation algorism and it is also difficult in this case. The leak signal should be cancelled by using the result of detecting the leakage signal or performance degradation of the high-frequency analog circuit. This is because it is difficult to realize a signal generator that outputs high-frequency signals for cancelling the unwanted leakage signals.

In the case of compensation using digital circuits, the performance is compensated by a tuning mechanism based on a parameter switching circuit. The DC operating point or a combination of the passive components is typically controlled. Although the performance degradation by PVT variation can be compensated, compensating/enhancing intrinsic high-frequency device performance is difficult. Thus, other approaches without a high-frequency ADC and a signal generator are required to compensate the issues.

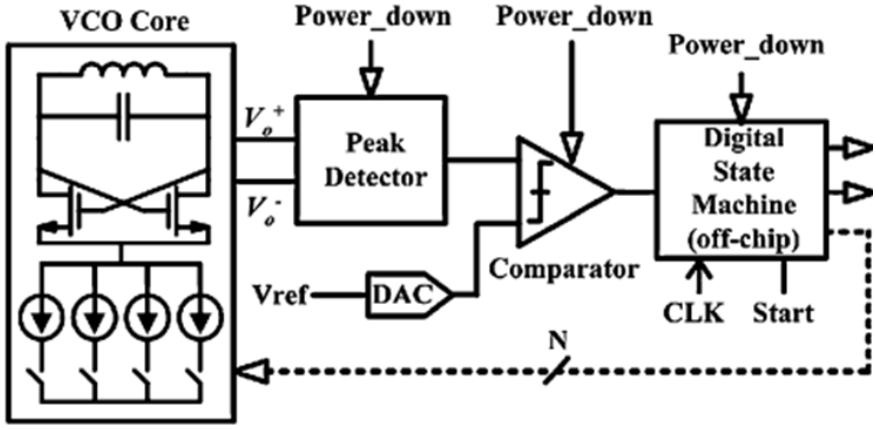


Figure 1.18: Compensation technique using digital circuits for high-frequency VCO [18]. ©IEEE 2005

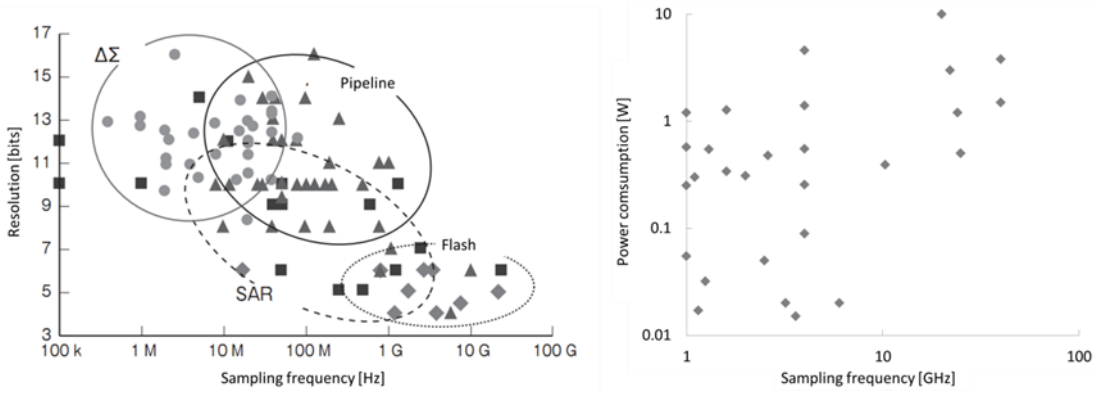


Figure 1.19: The Relationship between sampling frequency and resolution and the relationship between sampling frequency and power consumption of the ADC [22].

1.3.5 Compensation by Using Analog Circuits

The concept of a compensation method by using analog circuits for high-frequency circuits is defined as shown in Fig. Figure 1.20. The compensation method applies additional analog circuits for high-frequency core circuits and sometimes these circuits are merged to the core circuits. The additional analog circuits can operate at DC and/or in the high-frequency range according to compensation targets because such an analog circuit can share signals treated in the core high-frequency circuits. In order to suppress drawbacks of the compensation, the core analog high-frequency circuit after compensation should be the same as that before compensation. In other words, power consumption and occupied area of the core circuit should not be increased. Of course the minimum area and power consumption increase are desired for the additional/merging analog circuit for compensation.

A well-known example of the compensation method is a common-mode feedback circuit [2]. The circuit is added to the core analog circuit for compensating the DC operating point. The circuit is effective in a frequency range from DC to relatively low frequency. Adoption of high-frequency performance compensation is difficult because the compensation is based on a feedback system. This is similar to the case of a compensation technique using a digital circuit. On the other hand, the additional analog circuit is not only for the feedback system and it can also share the high-frequency signal depending on the additional or merging manner. Thus, the method is expected to enhance the basic performance of active and passive devices at the situation of low f_T and f_C ratio. And the compensation method is expected to ameliorate some problems caused by high-frequency signal leakage by improving immunity of the high-frequency analog circuits. Therefore, a compensation technique using analog circuits is expected to manage the issues that are difficult to handle with a compensation method using digital circuit. The circuit scale and power consumption of the analog circuit for compensation should be smaller or same compared to that of compensation using digital circuits. For example, the additional analog circuit should be implemented with several active or passive devices and additional power consumption should be much less than that of high-frequency analog core circuits, e.g. less than 1/10. In addition, PVT variation affects both the high-frequency core circuits and analog circuits for compensation. Thus, the operation of the additional/merging analog circuit sometimes cannot be effective for PVT variation.

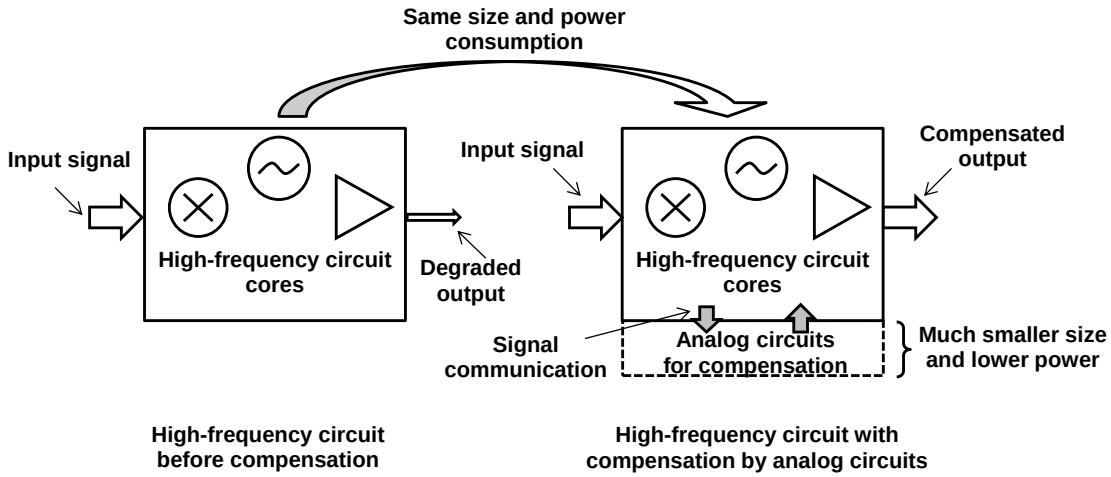


Figure 1.20: Concept of compensation method for the performance of high-frequency analog circuits by using analog circuits.

1.4 Objective of Dissertation

As described above, compensation technique for high-frequency analog circuits using digital or analog circuits improves performance with minimum drawbacks. However, each of these methods has a different effective region concerning the problems explained above. Therefore, if a designer of high-frequency circuits encounters these problems, the designer should select a compensation method using digital or analog circuits. If the selection is incorrect, there is a risk of impossibility/insufficiency of compensation and unacceptable circuit area/scale/design time arise. Selecting a correct compensation method is one of the most important factors at the beginning of the design of a high-frequency integrated circuit. Therefore, the objective of this dissertation is to clarify the effective regions of digital and analog compensation methods in order to assist designers who are trying to realize a highly integrated TRX.

In this dissertation the effective region is estimated based on actual substantiation and the result is very important for the designer who must resolve the issues. In order to obtain accurate estimation of the effective region of both digital and analog compensation methods, almost all situations should be substantiated. However, this requires much time and many integrated ICs for various motifs. On the other hand, problems caused by PVT variation can be compensated with the compensation method using digital circuits. The PVT variation causes various problems in whole integrated high-frequency wireless circuits. Thus, the effective region of compensation by using analog circuits is assumed to be smaller than that by using digital circuits as shown in Figure 1.21. Therefore, a smaller area should be substantiated at first to save time and the research in this dissertation is focuses on compensation method using analog circuits.

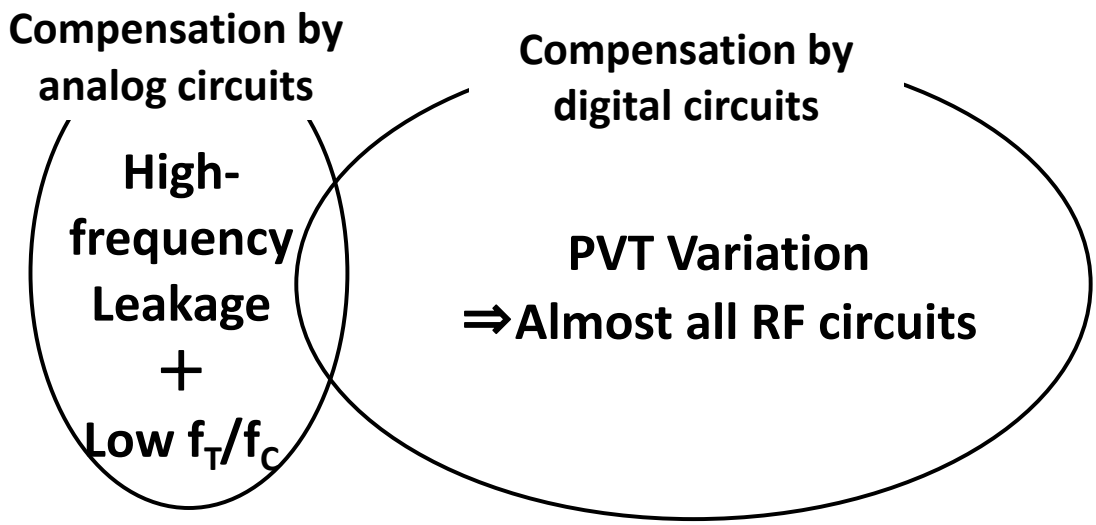


Figure 1.21: Predicted issues for which the compensation technique using digital and analog circuits is effective.

1.5 Organization of This Dissertation

In this chapter, the motivation for integrating wireless systems and some critical issues are introduced. These issues are expected to be resolved by adopting the digital or the analog compensation method for high-frequency analog circuits. The purpose of this dissertation is to clarify the effective regions of both methods by substantiation of the compensation method using analog circuits. In order to substantiate the compensation methods using analog circuits, this dissertation is organized as follows (Fig. 1.22). As explained in the previous subsection, there are three critical issues concerning the integration of high-frequency analog circuits as shown in the figure. The first issue is performance degradation by high-frequency signal leakage. Solutions for this issue are introduced in Chapters 2 and 3.

Chapter 2 focuses on the issue of LO signal leakage. A QDEMOD circuit for direct conversion RX is a motif of the problem. A compensation technique using analog circuits is applied to the LO buffering amplifier to suppress DC offset that causes LO leakage. A compensation technique with small area and lower current consumption is proposed and the LO leakage is suppressed. An example of the signal leakage problem of RX performance degradation caused by TX circuits that are integrated on the same die is shown in Chapter 3. A QDEMOD circuit for an FDD system is a motif of the problem. A compensation technique using analog circuits is applied to the QDEMOD. The noise performance degradation caused by TX leakage signal is suppressed by using the proposed compensation method and the input matching circuit can also be integrated by using the proposed solution.

Chapters 4 to 6 show solutions for very high-frequency wireless systems. These chapters treat problems corresponding to the issues caused by insufficient performance of silicon devices. A 60 GHz RX circuit with a mixer that operates with low-voltage LO signal and fully differential high-frequency circuits to avoid undesired performance degradation in very high-frequency band is described in Chapter 4. Chapter 5 contains a 60 GHz TRX with high-frequency circuits that are compensated by analog circuits with minimum additional power consumption and area. An LNA and a mixer circuit that operate with lower power consumption are shown in the chapter. In Chapter 6, a 77 GHz band radar TRX is a motif of a much higher-frequency TRX. Accurate 77 GHz frequency modulated signal is achieved with a PLL-based signal generator and a compensation technique by using analog circuits. Finally, the impact of the compensation techniques by using analog circuits are summarized and the adoptable regions of compensation techniques using digital and analog circuits are allocated for designers of high-frequency analog circuits in Chapter 7. A vision of the future wireless system adopting the results presented in the dissertation is also discussed in the chapter.

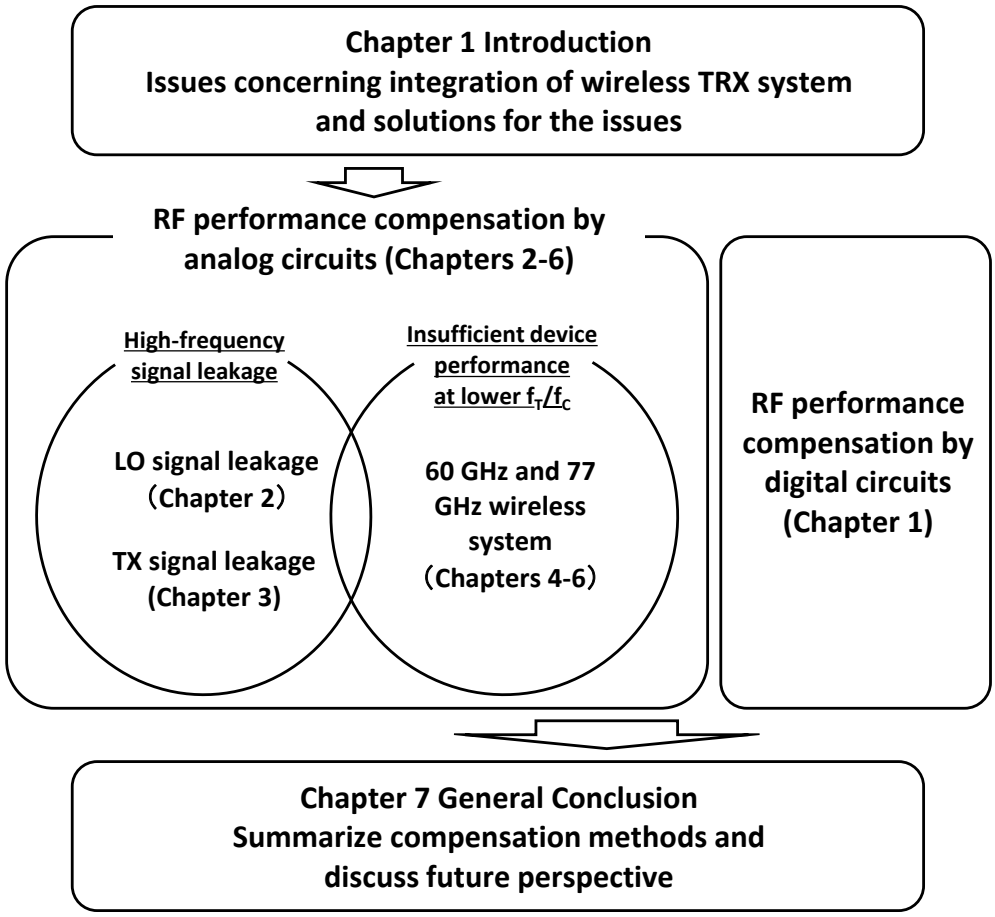


Figure 1.22: Organization of this dissertation.

Chapter 2

A Low LO Leakage and Low power QDEMOD

In this chapter, an issue of LO signal leakage in cellular phone system which is a case of high-frequency signal leakage problem explained in chapter 1 is substantiated. The LO leakage is a serious problem for direct-conversion RXs. LO leakage via QDEMOD must be suppressed in order to achieve a low DC offset and spurs emission form the antenna.

2.1 Introduction

2.1.1 Super heterodyne TRX for Cellular System

Super heterodyne (SH) TRX is widely adopted to various wireless applications especially in early phase in development [23], [24]. Figure 2.1 shows an example of a SH TRX architecture. In the RX chain, the input RF signal from an antenna is filtered by a preselect filter and the signal is input to LNA to be amplified with low noise. The output signal is input to the first mixer with LO signal generated by a VCO3 to intermediate frequency (IF) signal. There is serious problem at the downconversion, image problem. If the carrier frequency of the desired signal, f_C is lower than LO as IF frequency f_{IF}, $f_C = f_{LO} - f_{IF}$ as shown in Fig. 2.2, image frequency f_{IMG} is $f_{LO} + f_{IF}$. Undesired signal at the image frequency is also downconveted to IF frequency and the signal to noise ratio is considerably degraded. In order to reject the image signal, band pass filter is typically adopted. As explained below, the typical IF frequency is up to a few hundreds MHz for channel selection. The image frequency is close to desired carrier frequency. Thus bulky off-chip filter is required to obtain enough image rejection ratios. After first downconversion, the IF signal is input to a surface acoustic wave (SAW) device based channel selection filter. In order to obtain very high out-band suppression, off-chip SAW filter is typically used. Out of band interference signal and image signal from an antenna and TX, in the case of adopting frequency division duplex (FDD) system as like wideband code division multiple access (WCDMA) cellular application, is filtered by band pass filters. Then the signal is amplified and demodulated by a quadrature demodulator with quadrature LO signal generated by VCO1. Thanks to these filters, relatively low linearity RX specification is allowed.

In the TX chain, the input baseband signal is up-converted to RF band and modulated by using a

QMOD. The QMOD is derived by quadrature LO signal generated by using a frequency multiplayer with output signals from VCO2 and VCO3. Then the signal is filtered by the LPF to suppress low frequency noise and output to the antenna via power amplifier.

As explained above, a lot of number of filters and VCOs are required for the SH TRX. Off-chip filters are required especially for IF band. Individual VCO especially for lower oscillation frequency typically less than 300 MHz for VCO1 and VCO2 and PLL synthesizer ICs are required to avoid unexpected spurs caused by signal coupling between the VCOs and performance degradation such a lower frequency. And LNA and PA is typically individual IC to obtain low noise and high power performance. Of course off-chip matching circuits are required for the interface of the VCO, LNA, PA ICs and TRX ICs. Through the SH TRX has some advantages as explained above, it is not suitable for low cost TRX because of requirements of many off-chip components.

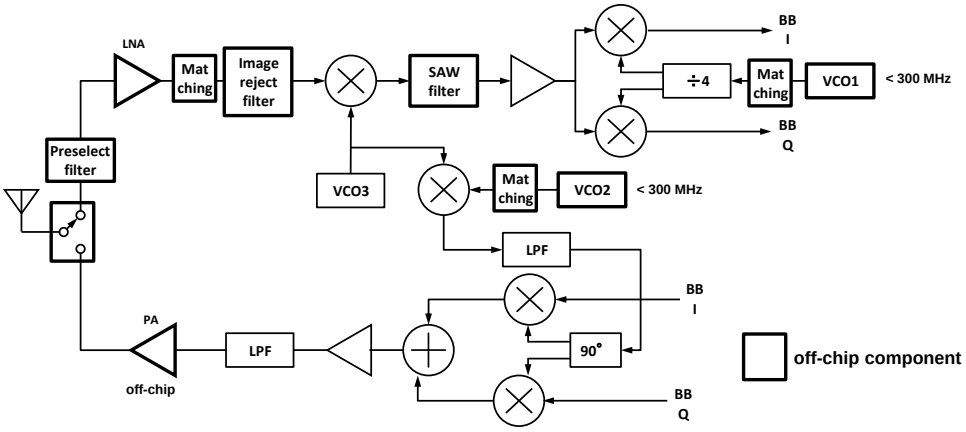


Figure 2.1: Typical Super-Heterodyne TRX.

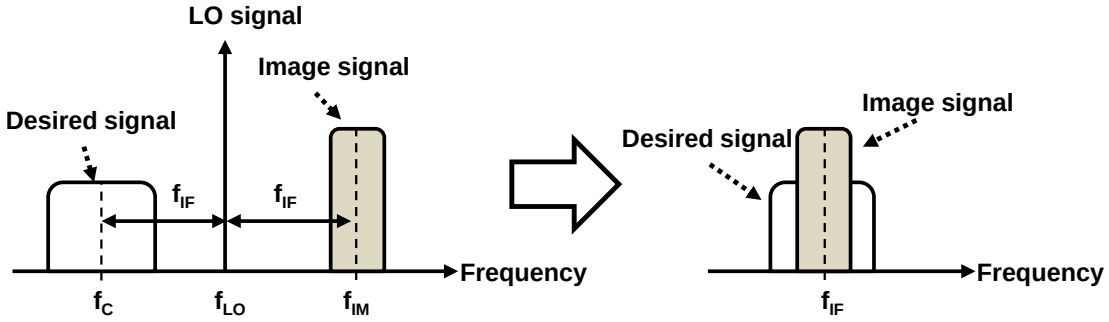


Figure 2.2: Problem of image signal.

2.1.2 Direct Conversion TRX for Cellular System

One of the solutions for integrating analog functional blocks such as a PLL synthesizer IC and off-chip filter is applying a direct conversion architecture ([6], [7]). An RF TRX using the architecture applies an LO signal whose frequency is same to carrier frequency of the desired RF signal. In a RX IC, the RF signal is converted to quadrature baseband signal directly by using a QDEMOD. By using the architecture, only one PLL synthesizer is used because the frequency conversion is only once. Thus a PLL synthesizer can be integrated the RX IC without coupling problems with other PLL synthesizers. Furthermore, bulky off-chip filters, an image rejection filter and an IF SAW filter, can be removed or integrated in the same die of the RX. Since the LO frequency is same as the carrier frequency of the RF signal, no image signal appears in BB signal and the image rejection filter can be removed. The IF band pass filter for channel selection is replaced to a low pass filter (LPF) for channel selection in baseband. Such a LPF can be integrated in same RF RX IC. Therefore,

There are some inherent issues by adopting direct conversion architecture. One of major issues of a direct conversion is DC offset. The LO signal which is generated in the same IC leaks to RF signal path via electro-magnetic and substrate resistive coupling. Then the signal is mixed by mixer circuit as shown in Fig. 2.5. The mixed signal is down-converted to DC as shown in Fig. 2.4 and the DC offset causes voltage saturation for following high gain VGA. This issue is known as “self-mixing” [6], [7]. In order to suppress the DC offset, the PLL generates multiple frequency signal of the carrier frequency. The signal is divided and quadrature LO signals are also generated in the case of using a master-slave flip-flop divider [25]. And a DC offset canceller with low frequency low-pass feedback is also adopted for baseband VGA circuit [26]. Second issue is channel select filter performance for the integrated low pass filter. Since the down-converted signal from the QDEMOD is not filtered, high order channel selection filter for suppressing the adjacent channel signal is required. And the VGA should have enough linearity against large adjacent channel signal. Some RX IC employ a linearized transconductor based VGA and filter, Gm-C filter, to obtain high dynamic range and high order low pass characteristic [25], [27].

Distortion and noise performance degradation is also the major issues. Higher power undesired signal input to the QDEMOD than SH architecture because there are no channel selecting filter before QDEMOD. It causes serious second order distortion problem. If there are undesired signals whose frequency difference is less than the bandwidth of the desired signal as shown in Fig. 2.6, the second order distortion product appears at the in-band of the downwconverted baseband signal. In order to improve the problem, differential balanced circuit with careful layout is required. Some researches have other approach to cancel the distortion caused by imbalance of the circuit [25]. Noise performance degradation is caused by low frequency flicker noise especially using CMOS process.

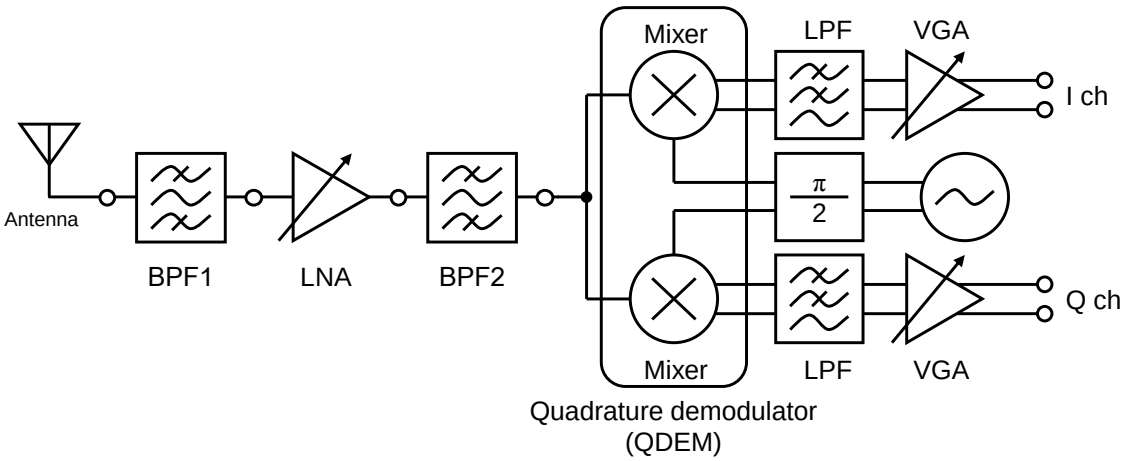


Figure 2.3: Direct conversion architecture (RX).

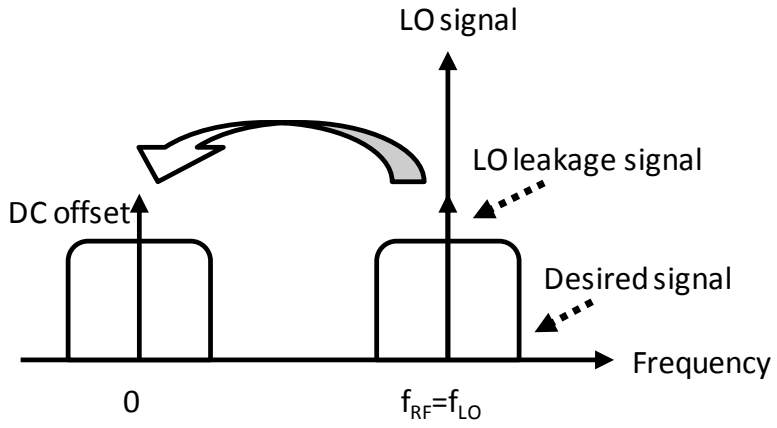


Figure 2.4: DC offset caused by LO leakage.

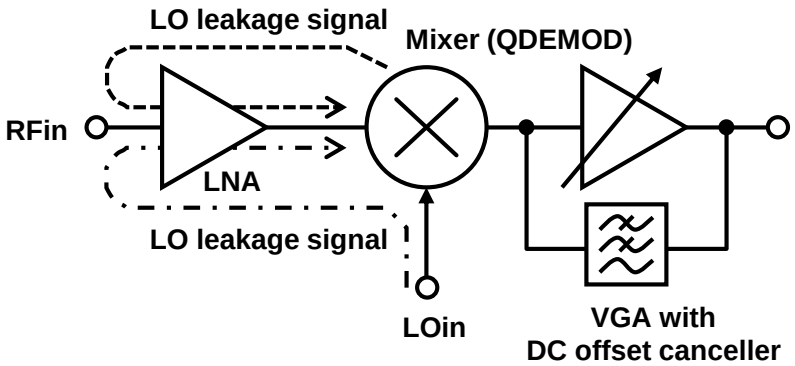


Figure 2.5: LO leakage and self mixing.

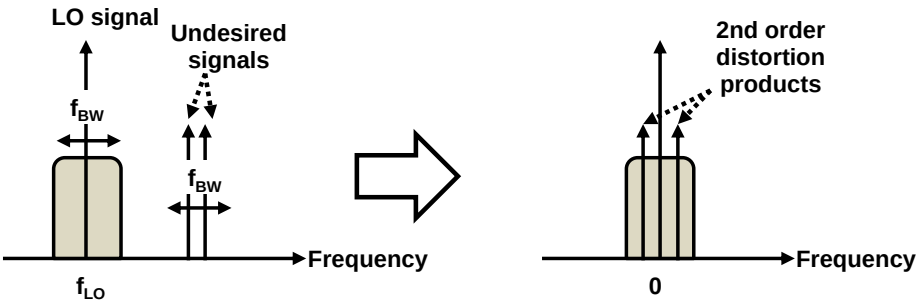


Figure 2.6: 2nd order distortion problem.

2.2 DC Offset Caused by LO Leakage in Double Balanced Mixer

2.2.1 DC Offset Caused by Self-Mixing

Figure 2.7 shows a block diagram of a direct conversion RX. The QDEMOD is composed of the double balanced mixers, the LO buffers, and the dividers. The double balanced mixer is suitable for the direct conversion RX because the ideal double balanced mixer does not leak LO signal [28]. The oscillation frequency of VCO is doubled frequency $2f_{LO}$ of the center frequency of the RF f_{RF}, and the f_{LO} signal is provided from the divider. So, output signal caused by mixing between the direct leakage $2f_{LO}$ signal from the VCO and f_{LO} signal does not have DC component. Thus, a serious self-mixing problem is caused by leakage of the f_{LO} signal after division.

In the case that LO signal leaks to the input of the single-ended low-noise amplifier (LNA), this leakage signal is amplified by the LNA and converted to differential signal by the balun shown in Fig. 2.7. This differential LO leakage signal is input to the QDEMOD again and induces DC offset caused by self-mixing. Since this DC offset is caused by differential LO leakage signal, it cannot be suppressed by using the double balanced mixer.

To suppress the DC offset, a DC offset canceller is implemented in BB analog block as shown in Fig. 2.7. This DC offset canceller requires a certain convergence time to complete DC offset cancel. When the gain of the LNA is changed by automatic gain control, the LO leakage input to the QDEMOD varies rapidly, so rapid variation of the DC offset occurs. However, the DC offset canceller cannot respond to a rapid variation of DC offset as shown in Fig. 2.8 [26]. To minimize rapid DC offset variation, it is important to suppress the LO leakage.

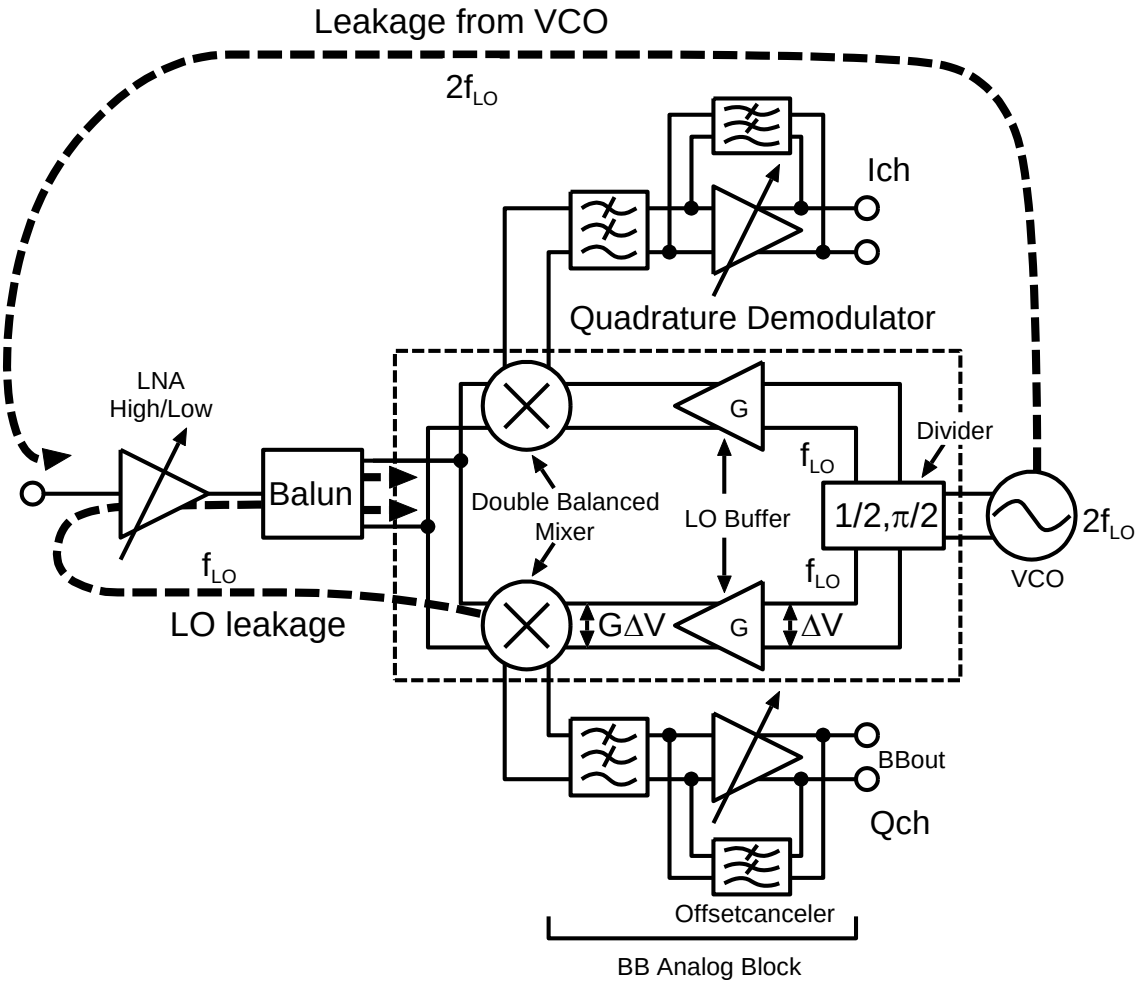


Figure 2.7: Self-mixing at RF front end.

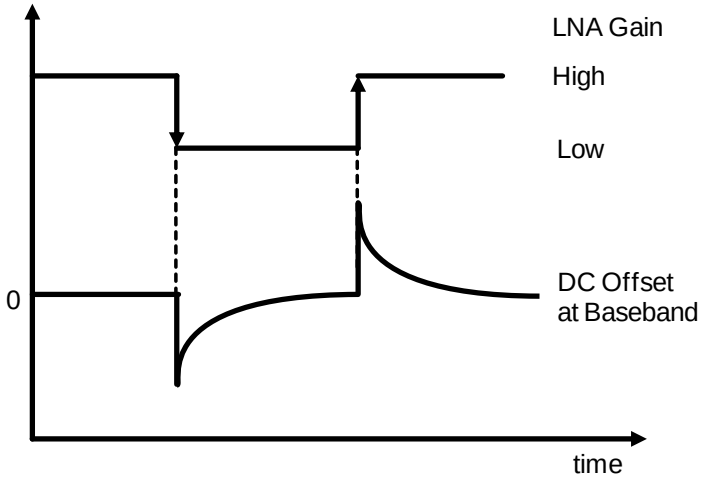


Figure 2.8: Rapid variation of DC offset.

2.2.2 LO Leakage caused by Double Balanced Mixer

Figure 2.9 shows the double balanced mixer circuit. In this circuit, differential pair Q_1, Q_2 with emitter degeneration inductor L_1 and L_2 is used as the transconductors and $Q_3 – Q_6$ are the switching transistors.

Figure 2.10 shows the half circuit of a double balanced mixer. In ideal balanced switching transistors, the signal at the node A has the $2f_{LO}$ component as shown in Fig. 2.10(a). Though this signal leaks outside the mixer via parasitic capacitance C_μ of Q_1, this signal does not causes self-mixing because the frequency of the leakage signal is $2f_{LO}$ frequency.

In a practical case, the switching transistors pair does not balance. So the signal at node A has $2f_{LO}$ and f_{LO} component as shown in Fig. 2.10(b). This signal which has f_{LO} component leaks outside the QDEMOD via Q_1 and reaches the input of the LNA. And this signal is amplified and converted to differential mode. Then this differential signal causes a DC offset.

The imbalance of the switching transistor pair is caused by a device mismatch of switching transistors and a DC offset generated by the LO buffer. When the LO buffer has a resistive load and DC gain G as shown in Fig. 2.11, the input offset voltage ΔV_{DC} caused a large offset G ΔV_{DC} at the output. This offset dominates the imbalance of the switching transistors. Thus, the DC offset caused by the LO buffer must be suppressed. For this purpose, it is necessary to suppress the DC gain of the LO buffer.

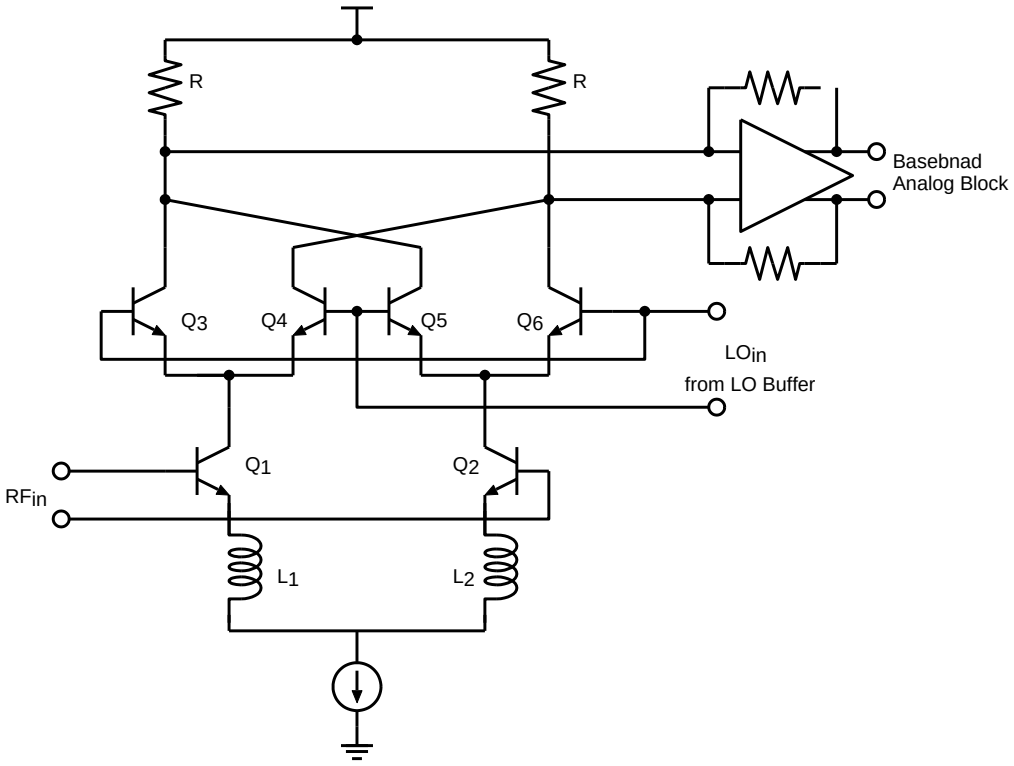


Figure 2.9: Double balanced mixer.

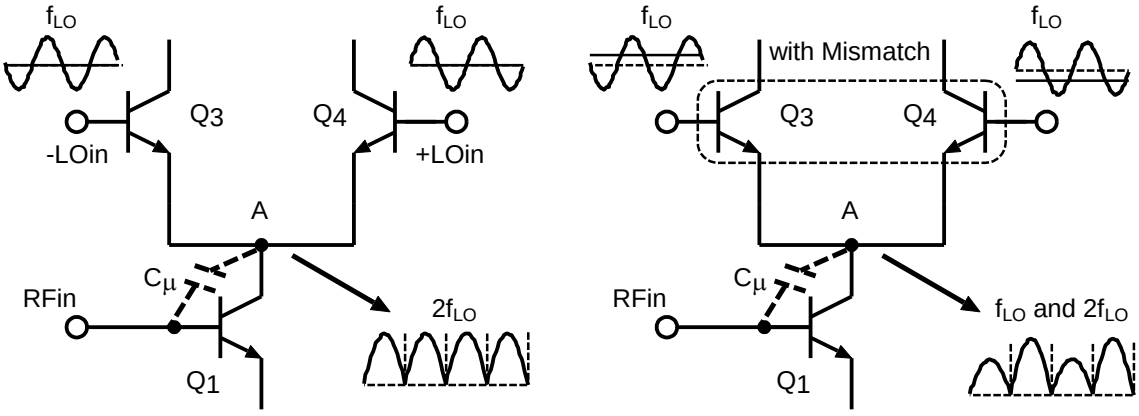


Figure 2.10: LO leakage caused by LO buffer DC offset.

2.3 Design of the LO Buffer

2.3.1 Conventional LO Buffers without DC Gain

There are some conventional LO buffers which have low DC gain. One is an LO buffer which has a band-pass characteristic such as in the case using a tank circuit as a load. The other is an LO buffer which has a high-pass characteristic such as in the case using DC blocking capacitors between LO buffer and mixer.

The LO buffer with a tank circuit load is shown in Fig. 2.12. This LO buffer has band-pass frequency response because the tank circuit has a band-pass characteristic. However, this circuit requires a large chip area for inductors to achieve a sufficient AC gain for switching mixer. According to a rough estimation for the 2 GHz application, the inductor is about 240 μm^2. Since there are two LO buffers for I and Q channels, respectively, 4 inductors are required for the QDEMOD. Thus, the total area of the QDEMOD with these inductors is 18 % larger than that of the QDEMOD without inductors.

The LO buffer with DC blocking capacitors between the LO buffer and the mixer is shown in Fig. 2.13. An additional DC bias circuit is required for the mixer to supply DC bias voltage V_{bias}. According to our estimation, the required I_{bias} is 150 μA, considering process and temperature variation of base current I_b of switching transistors. Since there are two LO buffers in the QDEMOD, the total additional bias current consumption is 300 μA. The DC blocking capacitors have parasitic elements which depend on the capacitance indicated by dashed line in Fig. 2.13. The output voltage of the LO buffer is reduced due to the parasitic elements. Even if the optimum DC blocking capacitance is selected, additional current is required for the LO buffer to obtain the desired AC gain. According to our estimation, an additional current of about 740 μA is required for two LO buffers.

Then the total additional current required for the LO buffer with DC blocking capacitors is approximately 1 mA. The current consumption of the QDEMOD with this LO buffer results in an increase of 13% as compared with that of the QDEMOD without DC blocking capacitors.

As discussed above, conventional LO buffers which suppress DC offset require a large chip area or a large additional current consumption.

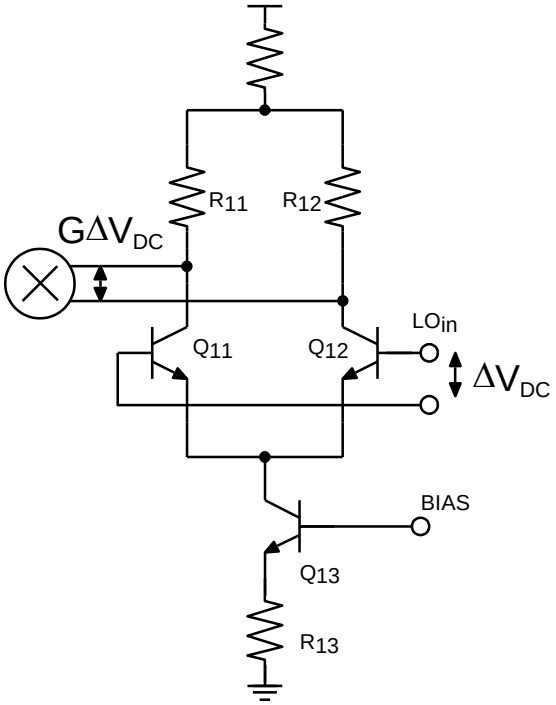


Figure 2.11: LO buffer with resistive Load.

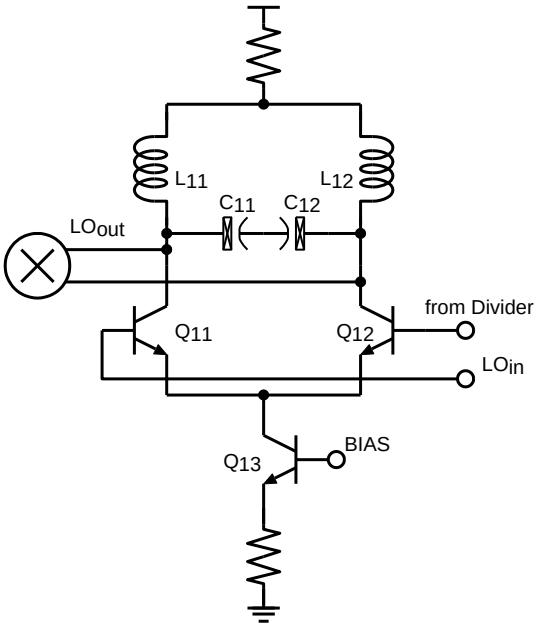


Figure 2.12: LO buffer with tank circuit load.

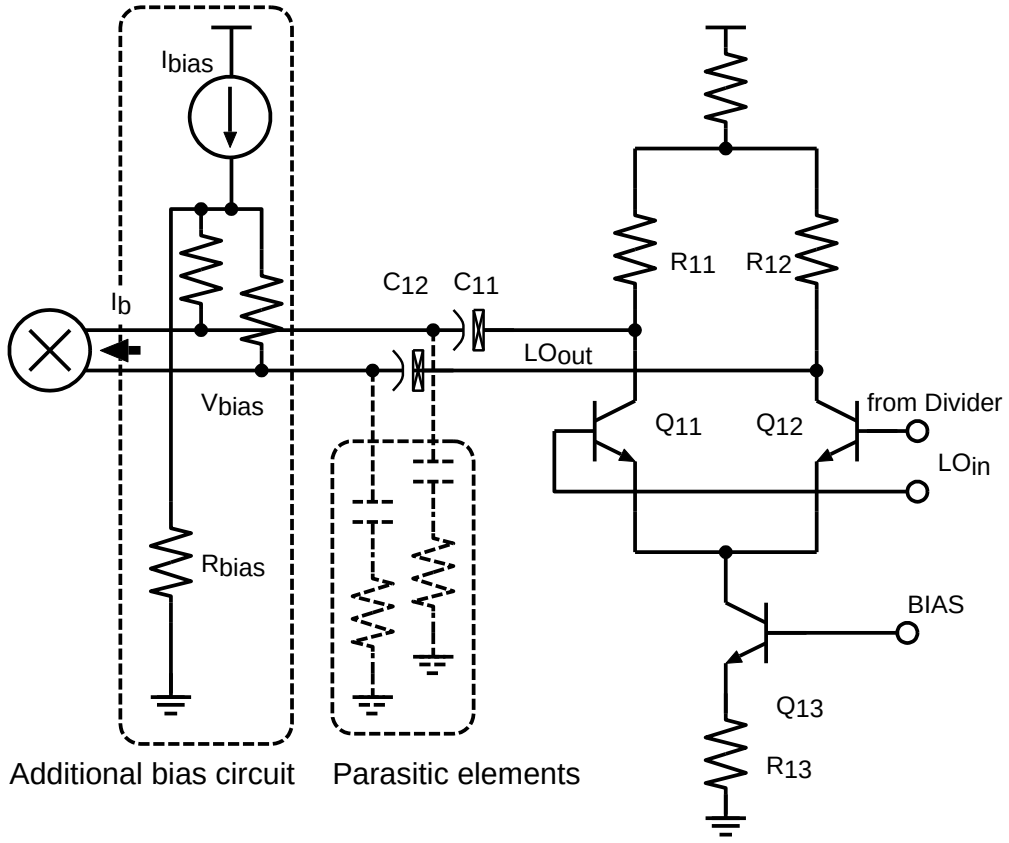


Figure 2.13: LO buffer with DC-cut capacitor.

2.3.2 Proposed LO Buffer

We proposed the LO buffer circuit shown in Fig. 2.14. This LO buffer has capacitors between emitters of the differential pair transistors Q_{11} and Q_{12}. The DC offset at the input of the LO buffer is eliminated at the LO buffer output because the capacitors work as a large attenuator at DC, supposing that offset current between the current source Q_{13} and Q_{14} is small owing to emitter degenerating resistor of R_{13}, R_{14}. In contrast, for the desired high-frequency signal, this circuit works as a differential amplifier because the capacitors exhibit small impedance. Thus, the LO buffer has high-pass frequency response and does not output DC offset to mixer. The cut-off frequency of the proposed LO buffer is roughly estimated by a product of the gm of Q_{11} and C_{e1}, C_{e2} in series capacitance. Selecting small degeneration capacitances which achieve sufficiently high cut-off frequency, the small chip area is occupied by the degeneration capacitances. Though these series capacitors also have parasitic elements as shown in Fig. 2.13, these parasitic elements do not degrade AC gain because the parasitic elements of C_{1e} and C_{2e} exist at AC ground. In addition, the current mirror transistors Q_{13}, Q_{14} and resistors R_{13}, R_{14} are in a common centroid layout in order to suppress DC offset at the LO buffer output.

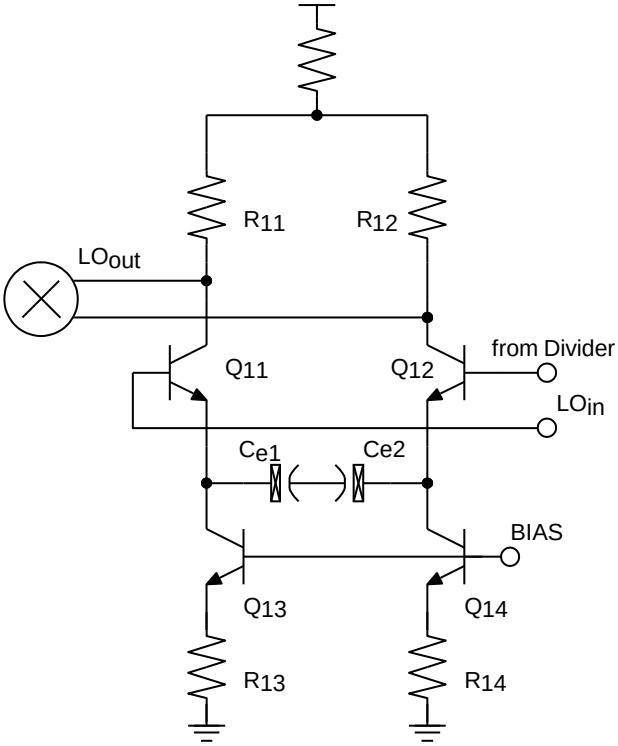


Figure 2.14: Proposed LO buffer.

Unlike the LO buffer using a tank circuit, this circuit does not require a large chip area, and unlike the LO buffer circuit using DC blocking capacitors, it does not consume additional current for AC gain compensation. Thus, the proposed LO buffer achieves small DC offset without increasing the chip area or the current consumption.

2.3.3 Simulated Results

Figure 2.15 shows the simulated results of the frequency response of the proposed LO buffer, the LO buffer without emitter degeneration capacitors shown in Fig. 2.11 and the LO buffer with a tank circuit shown in Fig. 2.12. These results show that the proposed LO buffer has high-pass frequency response and the same gain at the desired frequency as the LO buffer without high-pass characteristic.

Simulated results of the LO leakage are shown in Fig. 2.16. A DC offset voltage was added at the LO buffer input and common-mode LO leakage power level at the input of the QDEMOD was simulated. In Fig. 2.16, the horizontal axis shows the offset voltage at the LO buffer input and the vertical axis shows the LO leakage power at the QDEMOD input, respectively. According to these results, in the case that the DC offset at the LO buffer input is 1 mV, LO leakage suppression of 20 dB is achieved by using the proposed LO buffer and this is close to the result in the case of using LO buffer with a tank circuit. Though there is a mismatch of the switching transistors, the advantage of

using the proposed LO buffer does not disappear because the impact of the DC offset caused by the LO buffer is much greater than that of the mismatch of the switching transistors.

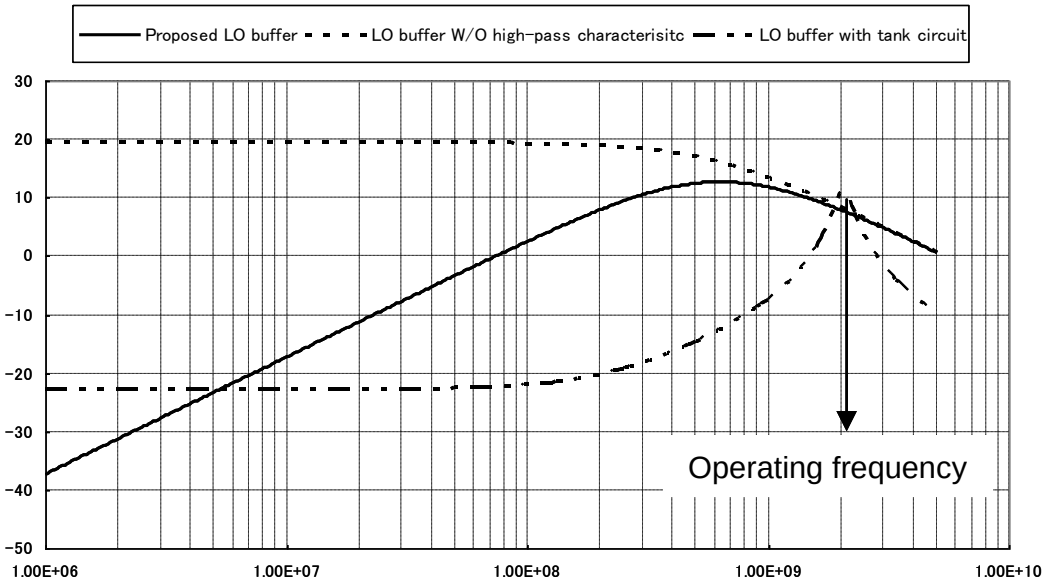


Figure 2.15: Frequency response of LO buffer.

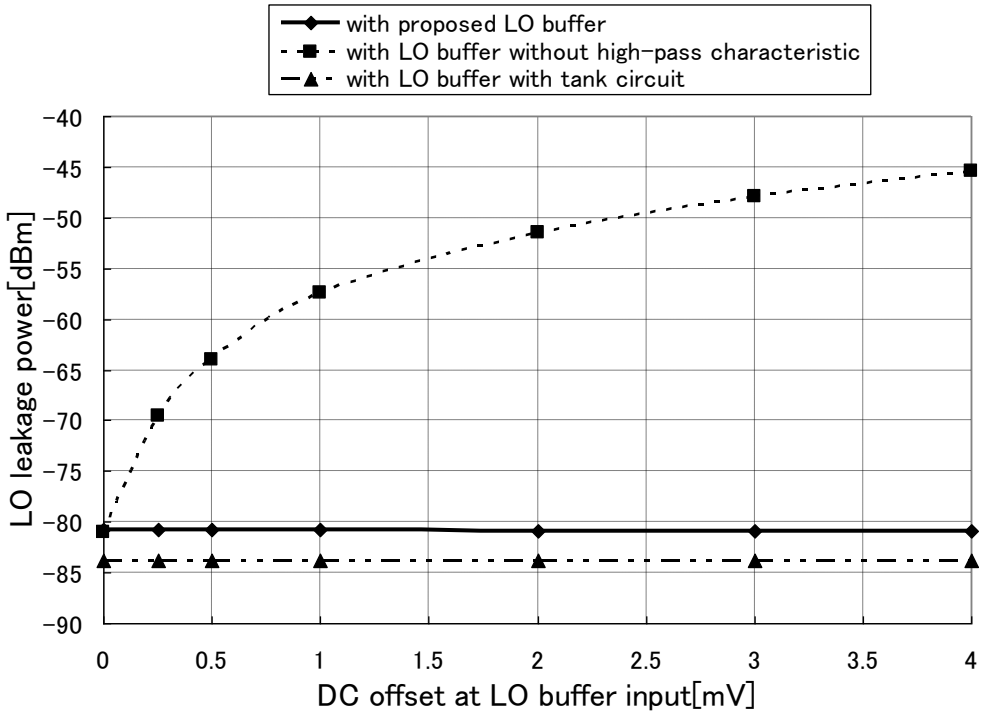


Figure 2.16: Frequency response of LO buffer.

2.4 Measured Results

The QDEMOD with the proposed LO buffer was fabricated using an f_T = 45 GHz Si-Ge BiCMOS process. Figure 2.17 shows the die photograph of the QDEMOD using the LO buffers with a tank circuit. In the fabrication of the QDEMOD using the proposed LO buffer, only Al wiring was changed. The inductors indicated in the dashed area occupy large chip area. This area can be reduced by adopting the proposed LO buffer. The summation area of the inductors is about 0.23mm^2 and the total area is about 1.3mm^2. So, compared to the case of adopting inductors, the die area can be reduced by about 18%.

The QDEMOD ICs in a package were mounted on an evaluation board. Table 1 shows the measured results for voltage gain, NF, IIP_2, IIP_3 and current consumption. In this table, "Proposed" is the QDEMOD with the proposed LO buffer, "W/O HP" is the QDEMOD with the LO buffer without a high-pass characteristic and "with tank" is the QDEMOD with the LO buffer with a tank circuit. These results show there are no significant differences between the circuits.

For twenty samples of each IC picked out randomly, LO leakage power at the input of the QDEMOD was measured. Figure 2.18 shows the measurement setup. The VCO which is integrated in the IC oscillates at 4280 MHz and the LO leakage signal is measured at 2140 MHz using a spectrum analyzer. Since the LO leakage occurs as common-mode signal dominantly, the LO leakage was measured at each input terminal of the QDEMOD. We also measured LO leakage in differential mode. The measured results were 30 dB less than those for common-mode.

Figure 2.19 shows the relative frequencies and the Gaussian fitting curves of the LO leakage power measured for the ICs. These results show LO leakage power of the QDEMOD with the proposed LO buffer is distributed from -75 dBm to -65 dBm and the peak of the Gaussian fitting is about -70 dBm.

On the other hand, the results of the QDEMOD with LO buffer without high-pass characteristic are distributed from -65 dBm to -50 dBm and the peak of the Gaussian fitting is about -58 dBm. This LO leakage power is more than 10 dB larger than that in the case of using the proposed LO buffer. We think that this increase of the LO leakage is due to the large DC offset caused by the conventional LO buffer shown in Fig. 2.11, considering the simulation results in Fig. 2.16. And this distribution is wider than in the case of the proposed LO buffer. Because the offset at the switching transistors consists of the DC output from the LO buffer and mismatch of the switching transistors, the total offset has wider variation. As a result of the wider DC offset variation, the LO leakage distribution is wider than the distribution of the results for the QDEMOD with the proposed LO buffer.

In addition, the LO leakage from the QDEMOD using the LO buffer with a tank circuit is about -53 dBm and it is larger than in the 2 cases described above. The distribution of the LO leakage

using a tank circuit is narrower than that due to device mismatch shown in Fig. 2.19, so the LO leakage is not mainly caused by the device mismatch. In the case of using a tank circuit, the LO leakage from another terminal such as Vcc is large, so we think the high LO leakage shown in Fig. 2.19 is caused by the electromagnetic radiation induced by the inductors used in the LO buffer. And the simulation result shown in Fig. 2.16 is much smaller than the measured result because the simulation result does not include the effects due to the radiation induced by the inductors. In addition, though the measured result for the distortion shown in Table 1 is less than that for other QDEMOD ICs, we think this degradation is associated with variation caused by LO leakage at Vcc and so on. The QDEMOD with the proposed LO buffer suppresses LO leakage by more than 10dB compared with the conventional circuits. This suppression is nearly equivalent to suppressing DC offset caused by self-mixing to 1/3.

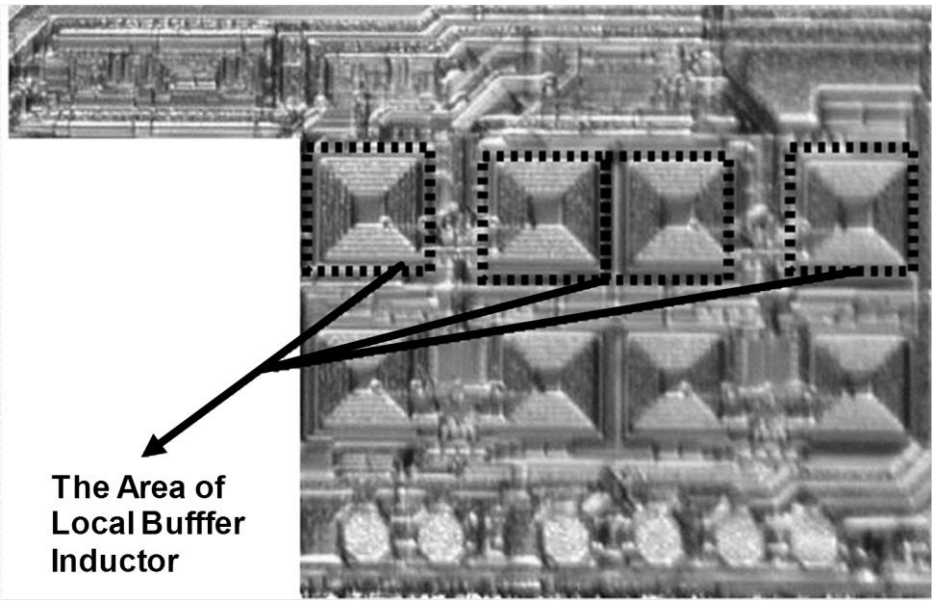


Figure 2.17: Die photograph of the QDEMOD.

Table 2.1: Measured characteristics of QDEMOD.

	VolgateGain [dB]	NF(DSB) [dB]	IIP2 [dBm]	IIP3 [dBm]	Current [mA]
Proposed	12.0	9.7	34	−1.2	8.2
W/O HP	11.8	10.1	35	−1.3	8.2
with tank	11.6	10.2	28	−2.5	7.8

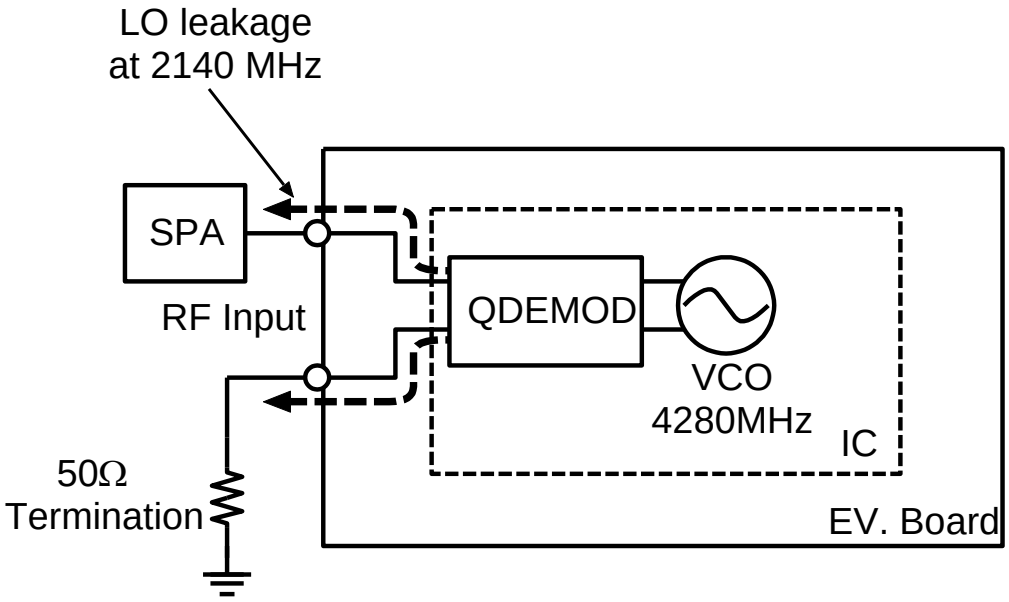


Figure 2.18: Measurement instruments of LO leakage power.

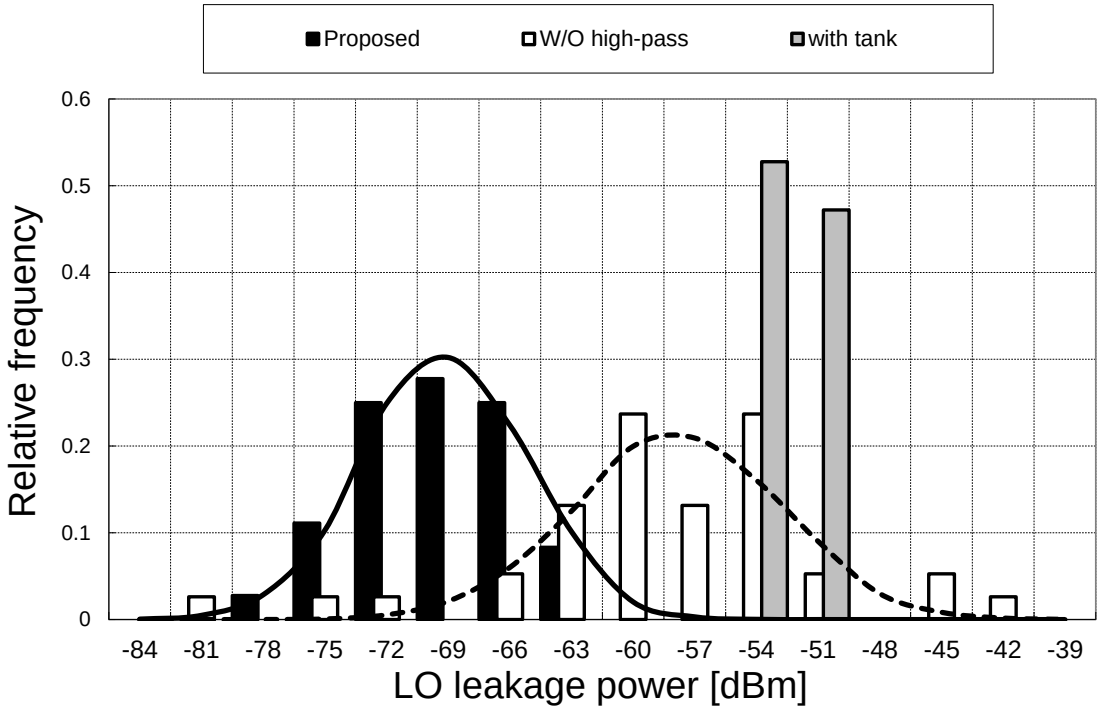


Figure 2.19: Relative frequency of LO leakage power.

2.5 Comparison and Summary

Figure 2.20 shows a performance comparison of the LO signal leakage. In order to comparison, the measured differential LO leakage power is adopted the result shows the leakage power is same level with the state of the art. This measured result indicates that the proposed compensating technique using analog circuit is suitable for high-frequency signal leakage.

An LO buffer is proposed that achieves small DC offset output to mixer with high-pass frequency response and without large area and additional current consumption [29]-[36]. The measured results show that the QDEMOD with the proposed LO buffer improves LO leakage more than 10dB compared with the QDEMOD without the proposed LO buffer. It is equivalent to the suppression of the DC offset to less than 1/3. Thus, the proposed LO buffer is suitable for direct-conversion RXs. Finally, the QDEMOD was a commercialized in a part of dual-band WCDMA RX IC.

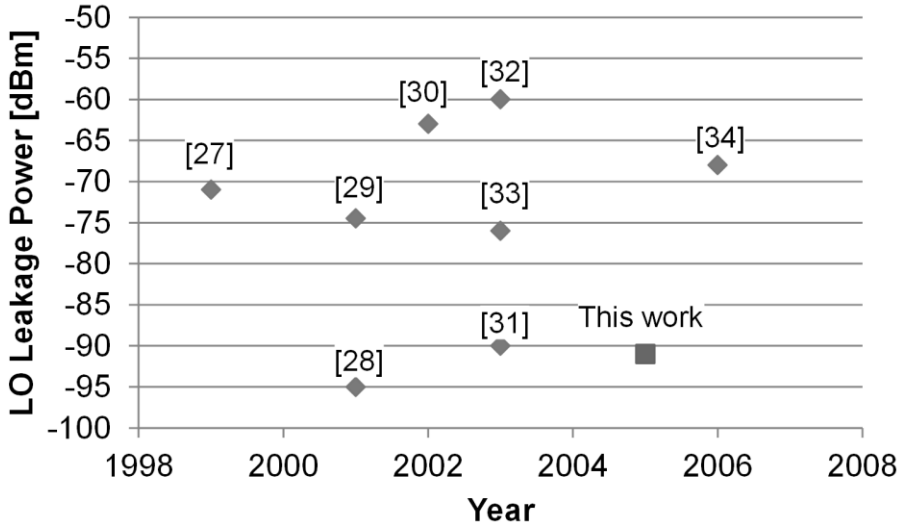


Figure 2.20: Performance comparison of LO leakage power.

Chapter 3

A QDEMOD with Integrated Matching Circuits and Robustness to TX Leakage

In this chapter, an issue of performance degradation of RX QDEMOD caused by TX signal leakage in cellular phone system which is a case of high-frequency signal leakage problem explained in chapter 1 is introduced. A mixer circuit for QDEMOD using common-base input stage is robust to parasitic elements is substantiated for integrating on-chip matching circuits to realize small and low-cost wireless system.

3.1 Introduction

The integration of off-chip components in ICs is desired in order to realize a small and low-cost RF front-end module. Generally, an input impedance of a common-emitter circuit with an on-chip matching circuit is sensitive to parasitic elements that are difficult to estimate in simulations. On the other hand, a QDEMOD, Fig. 3.2 (a), using a common-base input stage, Fig. 3.2(b), is suitable for an on-chip matching circuit because its low input impedance is robust to parasitic elements [37], [40].

In a WCDMA terminal, the TX block works simultaneously with the RX block. So, the common-mode TX signal leaks to RF input of QDEMOD while the RX block is active. In the case that the TX block and the RX block are on the same chip, this leakage causes serious problems. One of the problems is RX noise figure degradation due to the TX leakage signal [41],[42].

In this work, we propose a QDEMOD using a common-base input stage with an on-chip matching circuit that is capable of suppressing the common-mode TX signal input. The outline of this paper is as follows. Section 2 discusses the pros and cons of a general common-base input stage. Section 3 presents the proposed common-base mixer. Measured results are shown in Section 4 and Section 5 concludes this paper.

3.2 Mixer Using Common-Base Input Stage

3.2.1 On-chip Matching Schemes

Figure 3.1 shows matching circuit architects for lower or moderate impedance transformation ratio. The simplest matching circuit is using a termination resistor as shown in (a). The termination resistance is selected to have same resistance of the signal source, 50 ohms in typical, and the input impedance of the transistor is much higher than the terminal resistance. However, such a termination causes 3 dB of insertion loss. An architecture using resistive feedback is shown in (b). The input impedance is determined by the open-loop gain of the amplifier and the feedback resistance [39], [43]. Thus the input impedance can be controlled to have lower impedance transformation ratio and the input impedance has broadband characteristic. The topology sometimes requires larger power consumption for higher loop gain. As shown in (c) is architecture using inductive degeneration. The architecture is widely adopted for RF amplifier and mixer circuits [44]. Input impedance of the transistor with degeneration inductor is approximated by product of transconductance of the transistor and the inductance of the degeneration inductor. Series inductor is used for resonating with the parasitic capacitances between base or gate terminal and emitter or source node. Because of using the resonator, the matching architecture cannot be adopted for wideband operation. Common-base or common-gate circuit also can be used as matching circuit as shown in (d). The input impedance of such a circuits is approximated as invers of the transconductance. Impedance matching is obtained by tuning the transconductance to have same input resistance of signal source. Choke inductance is connected between emitter or source terminal and ground to supply DC bias current without changing the input impedance at desired frequency band. Additionally, a bonding wire is used as an inductor with high quality factor, such a inductor can be adopted for degeneration inductor between emitter or source node and ground pin of IC package via a bonding wire [41].

In the case using on-chip or in-package passive components, the parameters of such components cannot be changed as off-chip components. Thus the characteristic of the on-chip inductor and the transmission line should be estimated by calculation or electro-magnetic simulation or measured results of single on-chip components. However, it is difficult to accurate prediction including parasitic devices due to actual peripheral environment, coupling with other line or devices, of the target device and non-uniform permittivity of dielectrics in the die. The capacitance of the on-chip capacitor typically has 10-20% of process variation due to metal width and dielectric thickness variation. In order to integrate the matching components, impedance matching should be kept including estimation error and variation. Common-base or common-gate circuitry can be applied for robust impedance matching.

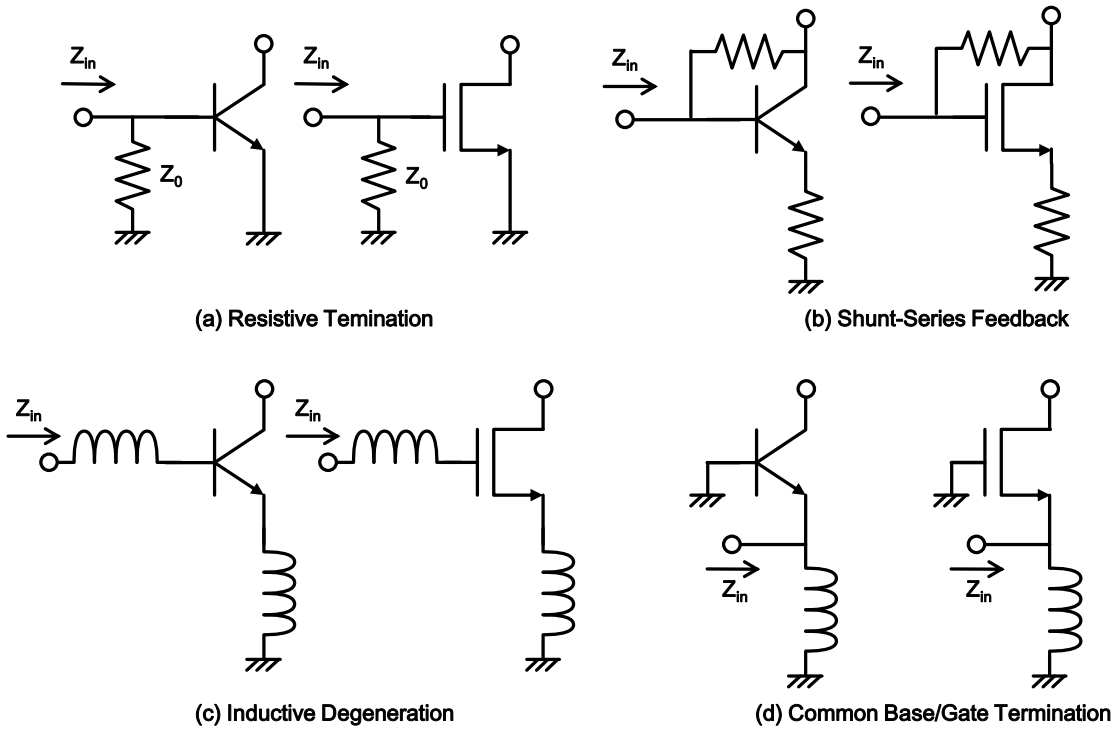


Figure 3.1: Matching circuit architectures.

3.2.2 General Common-Base Input Stage

Figure 3.2 shows a double-balanced mixer circuit using a common-base input stage. The input impedance of the common-base circuit is 1/gm and in most cases much smaller than that of base-emitter capacitance $C\pi$ and parasitic capacitances of passive devices and metal lines Cp at a few GHz signal frequency. In order to supply bias current to transistors, choke inductors Lc are connected between the emitter of the common-base transistors and ground. The impedance of the choke inductors is designed to be sufficiently larger than that of the common-base circuit. Therefore, the input impedance is mainly determined by 1/gm and is robust to parasitic capacitance of transistors, passive devices and metal lines.

Figure 3.3(a) and Fig. 3.3(b) show the common-base circuit of the mixer input-stage for a differential signal source, e.g. desired RX signal, and for a common-mode signal source, e.g. TX leakage signal, respectively. The source impedance for the differential-mode is twice the single source impedance Z_0, whereas the common-mode input source impedance is half of the Z_0. Thus, the S_{11}, reflection coefficient, is the same value for both modes as shown in Fig. 3.3. So, the general common-base input stage has the same sensitivity for both the common-mode signal and the differential-mode signal.

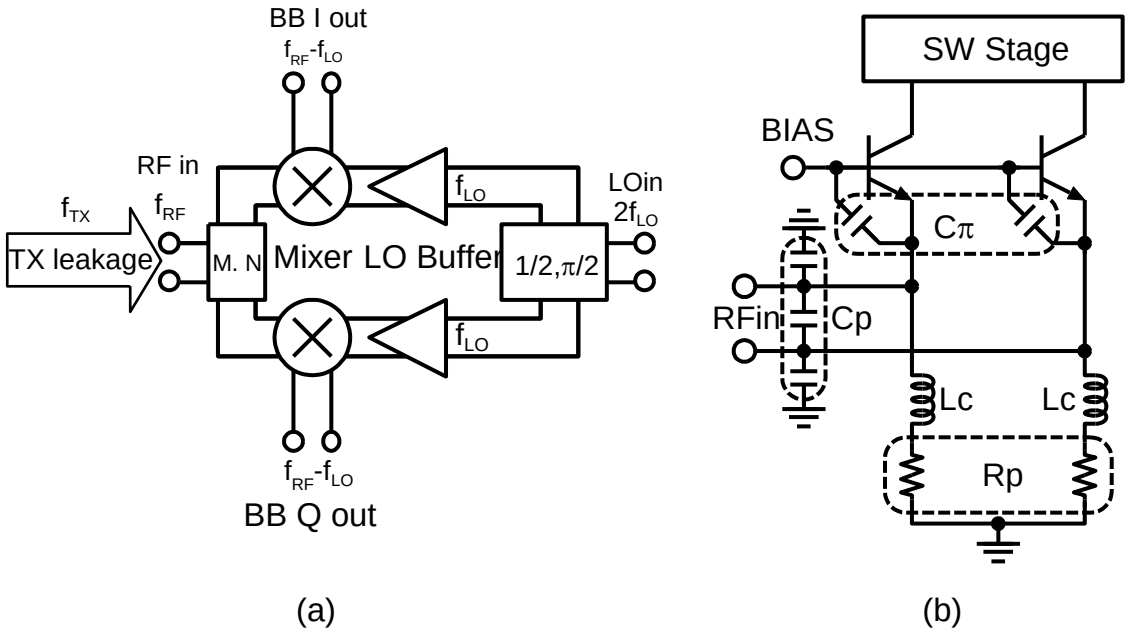


Figure 3.2: QDEMOD and mixer with common-base input stage.

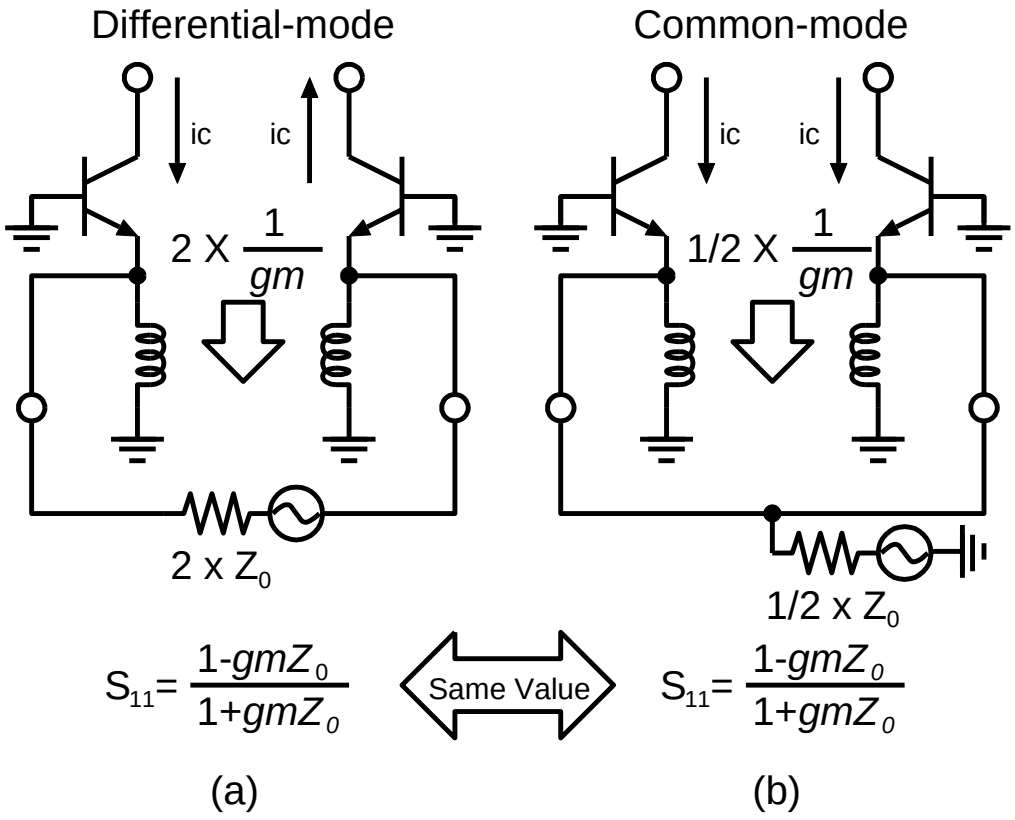


Figure 3.3: Reflection coefficients of the common-base input stage for the differential-mode and for the common-mode.

3.2.3 Noise Degradation Due to TX Leakage Signal

A large blocker such as the TX leakage signal causes noise performance degradation of a mixer [41], [42]. In a highly integrated TRX IC for a WCDMA terminal, the RX block and the TX block are integrated on the same chip. In this case, a large common-mode TX signal leaks into the input of the mixer.

This leakage signal causes additional base-band (BB) output noise due to two factors.

The first factor is additional DC current generation by even-order distortion from common-base input transistors. When a large common-mode TX signal is input to the mixer, the input transistors generate even-order distortion. Since this distortion signal contains DC element, the shot noise of the input transistors is increased. In addition, the switching transistors in the mixer do not work correctly and the voltage gain is compressed because the output DC voltage and the Vce of the switching transistors become lower.

The second factor is a frequency conversion of noise with a TX signal. The noise comes from two kinds of noise sources. The former is noise of the common-base input stage. When the TX leakage signal is input to the mixer input stage, low-frequency, around f_{LO} - f_{TX}, noise at the mixer input stage is mixed with TX signal (f_{TX}) and upconverted to the LO frequency (f_{LO}) due to second-order intermodulation at the input stage as shown in Fig. 3.4(a). This upconverted noise around f_{LO} is injected to the switching stage and then it is mixed with the LO signal (f_{LO}) and downconverted to f_{BB} around DC as also shown in Fig. 3.4(a). The latter noise is noise of the switching stage originating from the frequency divider/phase-shifter and the LO buffer, which are shown in Fig. 3.2(a), and the switching transistors. When the TX signal is input to the mixer input stage, this TX signal is amplified at the common-base input stage and goes to the following switching stage. Then, at the switching stage, the noise mentioned above at around the TX frequency (f_{TX}) is mixed with the amplified TX signal and downconverted to f_{BB} as shown in Fig. 3.4(b). If the switching stage consists of ideal matching transistors, the BB noise downconverted from the LO buffer and divider is cancelled. However, the cancellation is incomplete due to device mismatch of the switching transistors and the noise of the switching transistors does not have correlation. So, downconverted noise appears to be the BB output.

Therefore, a large common-mode TX signal must be suppressed at the input stage of the mixer sufficiently in order to avoid noise performance degradation. However as mentioned in section 2.1, the sensitivity of the general common-base input stage for the common-mode TX leakage is the same as that of the differential-mode desired RX signal.

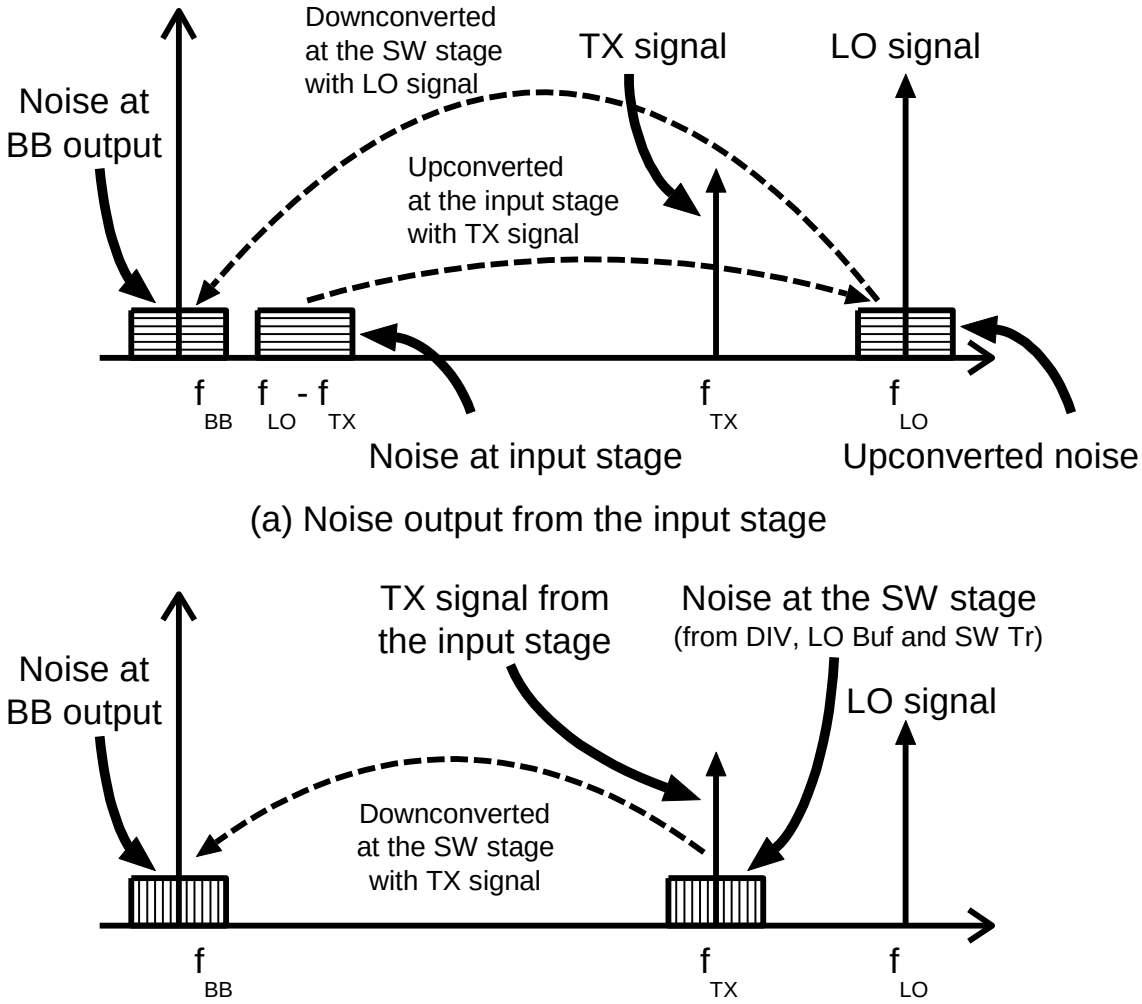


Figure 3.4: Noise downconversion and upconversion to BB frequency.

3.2.4 Temperature Dependence of on-Chip Inductors

There are parasitic resistances in the on-chip choke inductors. In the typical BiCMOS process, on-chip inductors are made of aluminum lines and their resistivity temperature coefficient is 0.44%/°C [45]. So, the inductor's parasitic resistance varies 46.2% when temperature varies from -20 °C to 85 °C. This resistance causes the bias current variation of the common-base circuit with temperature and then the gain varies with temperature.

3.3 Proposed Common Base Mixer Design

3.3.1 Choke using Symmetrical Inductors

The mixer with a common-mode input stage is suitable for an on-chip matching circuit, but the problems described above arise when it is used for a WCDMA direct-conversion RX. To overcome these problems, the common-mode sensitivity and the gain variation with temperature in a common-base input stage must be suppressed.

Figure 3.5(a) shows the proposed mixer circuit. This is a double-balanced mixer composed of a common-base input stage and a symmetrical inductor for choke whose coupling factor is k. The center-tap of the choke inductor is connected to ground via capacitor *Ce* and resistor *Re*.

The inductance of the symmetrical inductor shows different values for the differential-mode and the common-mode, respectively [46]. When the individual inductance of the symmetrical inductor is *L*, the differential-mode inductance L_{diff} is

$$L_{diff} = (1+k)L \qquad (3.1)$$

and the common-mode inductance L_{com} is

$$L_{com} = (1-k)L \qquad (3.2)$$

This inductor has large inductance for a differential-mode signal and small inductance for a common-mode signal. Using the symmetric inductors for the common-base input stage, this inductor works as choke for a differential-mode signal and as a shunt device to ground via capacitor for a common-mode signal. So, the differential-mode signal is input to a common-base input stage, and the common-mode signal is reflected. The calculated coupling factor and the individual inductance of the symmetrical inductor by using the geometric parameters of the inductor [46] are 0.8 and 4.9 nH. In this case an inductance ratio of differential-mode versus common-mode is 9. A common-base input stage using a symmetrical inductor can achieve both impedance matching for differential-mode and large reflection for common-mode simultaneously.

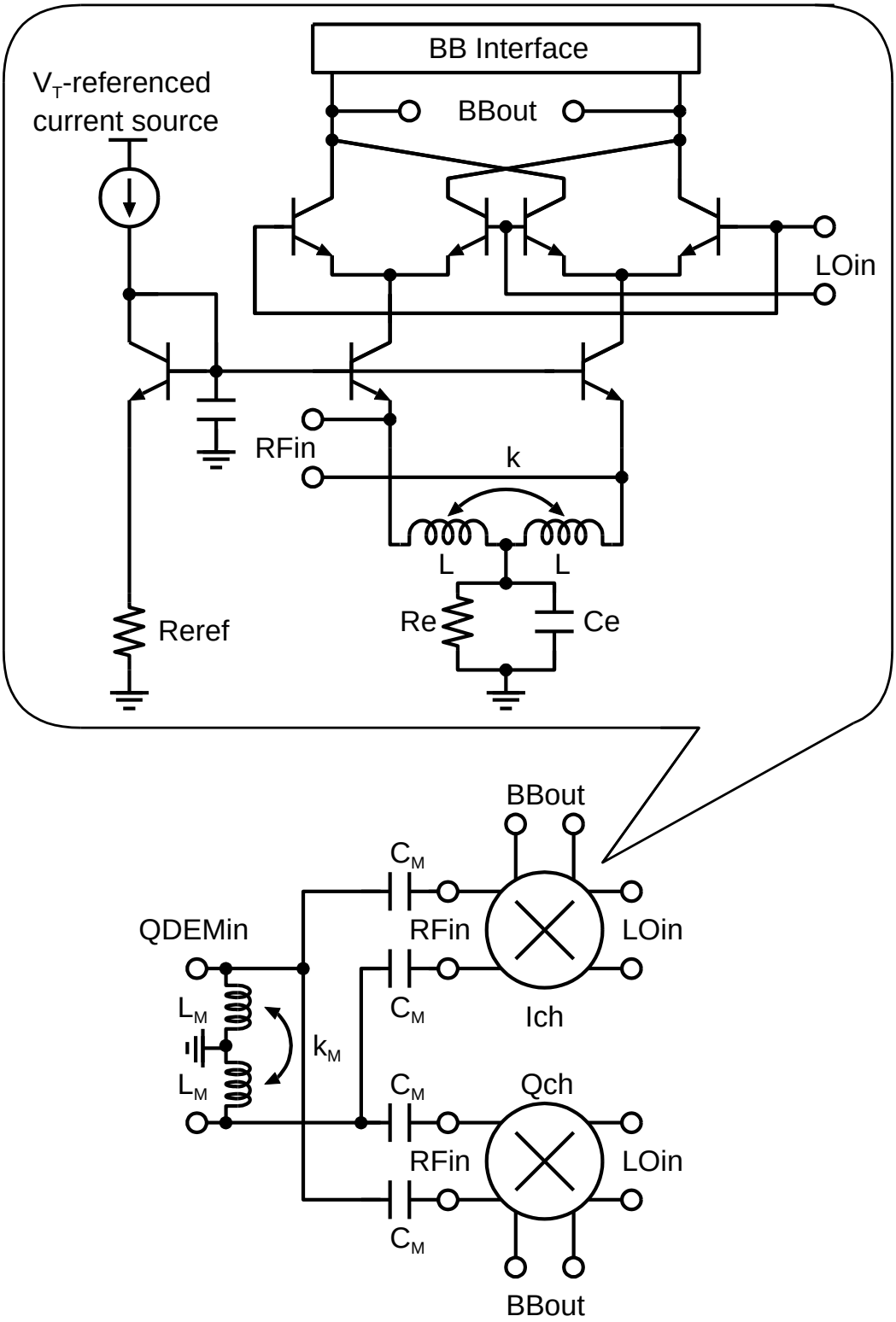


Figure 3.5: Proposed mixer circuit with common-base input stage and input matching circuit.

3.3.2 Input Matching Circuit Using Symmetrical Inductors

Figure 3.5(b) shows the input matching circuit for the proposed mixers. The input impedance of the QDEMOD was tuned to 200 Ω in order to match the off-chip SAW filter's output impedance. A symmetrical inductor is also used in the matching circuit to increase the reflection of the common-mode input signal. Capacitors C_M used in this circuit work as DC-block and matching circuit. These capacitors also suppress noise coming from Ich mixer to Qch and vice versa.

3.3.3 Gain Compensation Technique

To compensate for the gain variation with temperature caused by inductor parasitic resistance, a degeneration resistor *Re* and that of current mirror *Reref* made of polysilicon are placed on the center-tap of the inductor and on the emitter of the current mirror transistor, respectively, as shown in Fig. 3.5(a). The resistance is sufficiently, about 10 times, higher than that of inductor parasitic resistor. Thus, the variation of the current mirror ratio is suppressed because the resistance variation of the choke inductor is much smaller than the degeneration resistance of the *Re*. In addition, a shunt capacitor *Ce* is also connected parallel to the degeneration resistor *Re* in order not to increase common-mode impedance.

3.4 Measured Results

The QDEMOD is fabricated using a f_T = 75 GHz SiGe BiCMOS process. The QDEMOD consists of a matching circuit, I/Q common-base input mixers, I/Q LO buffers, a divider/phase-shifter and a bias circuit as shown in Fig. 3.2. A photograph of this chip is shown in Fig. 3.6. The die area of the QDEMOD is 0.76 mm × 1.15 mm. The two inductors located in the center of Fig. 3.6 are chokes for the mixer circuit and the inductor located on the left-hand side is for the matching circuit. By using the symmetrical inductors, the number of inductors is reduced to half.

We measured the proposed QDEMOD performance with the measurement setups shown in Fig. 3.7. Fig. 3.7 (a) is a setup to measure performances for desired differential RF input without common-mode TX input. The RF input signal is given from the signal generator via an onboard balun in order to convert the impedance of the signal source from 50 Ω to 200 Ω because the input impedance of QDEMOD is tuned to 200 Ω. And LO signal, which is double the frequency of the RF signal, is supplied from an external signal generator.

Figure 6(b) shows a setup to measure the input S-parameters. The reference plane of the network analyzer is adjusted at RF input pin of the QDEMOD IC. 2 port S-parameter was measured and converted to differential-mode S-parameter and that of common-mode [47].

Figure 3.7(c) shows a setup for measuring QDEMOD performances with common-mode TX signal. The differential input nodes of the QDEMOD IC are connected to each other on the evaluation board

in order to input common-mode TX signal. The common-mode sine wave signal at TX frequency (1950MHz) was injected from the signal generator. Variation of DC current consumption and degradation of noise characteristic caused by the common-mode TX signal was measured by ammeter and spectrum analyzer.

The measured summary of QDEMOD performance for differential mode RF input by using the setup shown in Fig. 3.7(a) is shown in table 1.

Figure 3.8 shows the measured S-parameters of the QDEMOD with 1 GHz to 3GHz range. S_{dd} is the S-parameter for the differential-mode signal and S_{cc} is for the common-mode signal. At RF center frequency of 2140MHz, S_{dd} is -14 dB. In contrast, S_{cc} is -1.7 dB at TX center frequency of 1950MHz. It means common-mode TX leakage signal is attenuated by 15dB. Thus, the proposed QDEMOD achieves matching for differential-mode signal and large reflection for common-mode signal, simultaneously.

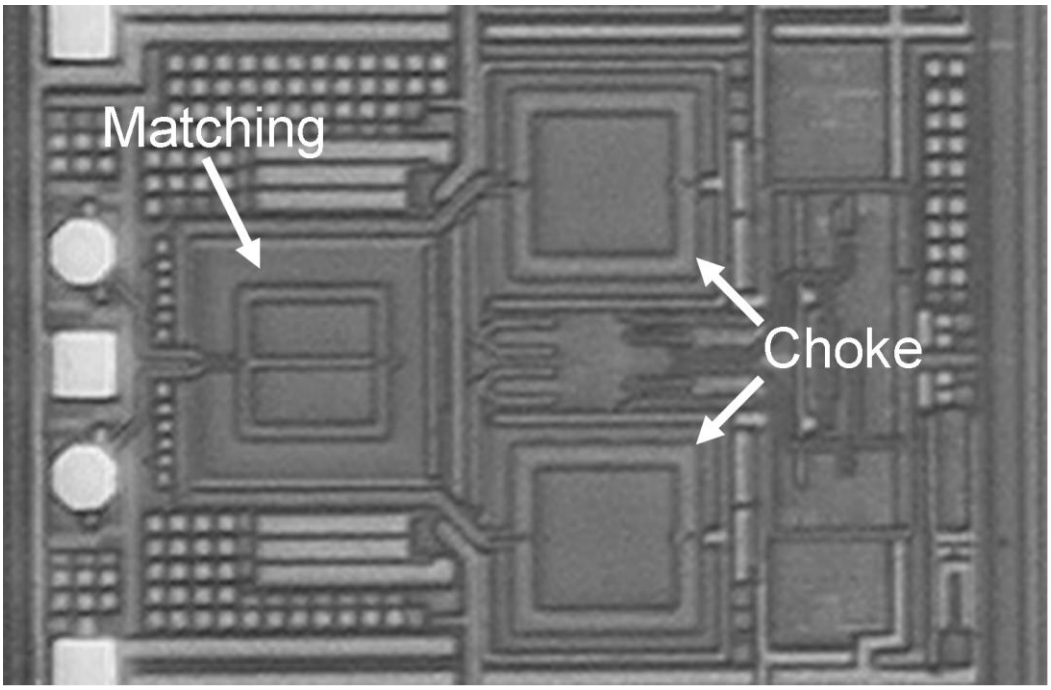
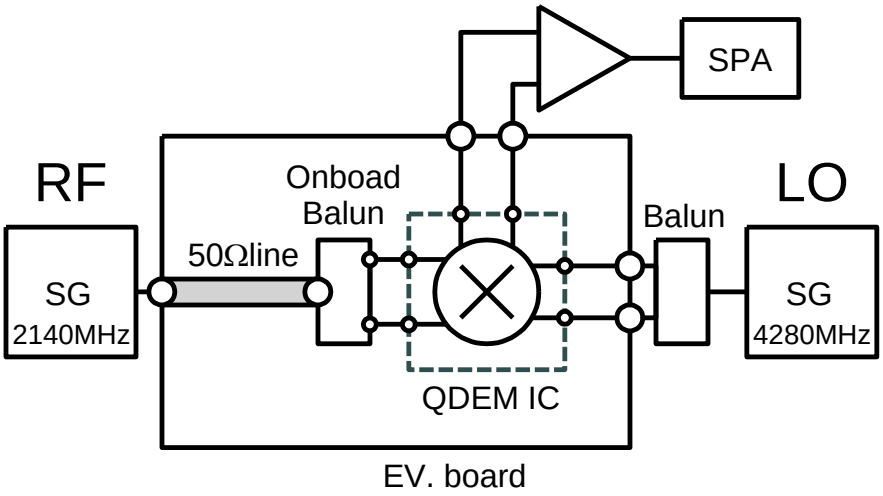
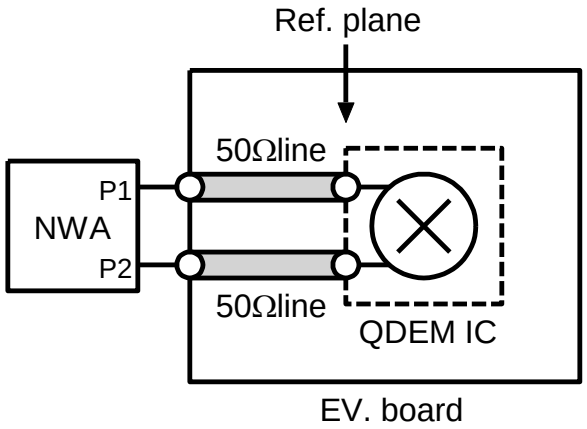


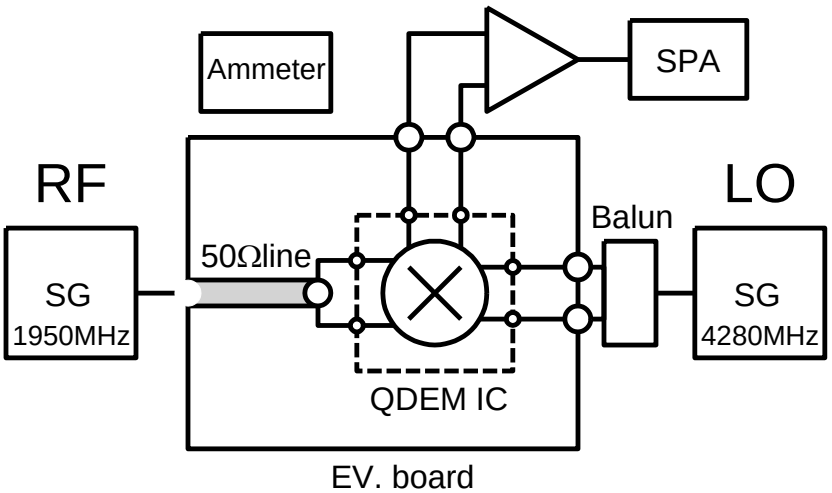
Figure 3.6: Chip micrograph.



(a)Differential measurement (w/o TX signal)



(b)S-parameter measurement



(c)Current and noise variation w/ common-mode TX

Figure 3.7: Measurement setup for differential-mode and common-mode signal.

Table 3.1: Summary of the measured QDMEOD performances for differential mode RX input.

RF input frequncy	2110-2170 MHz
LO input frequency	4220-4340 MHz
LO input level	-18 dBm
S11 (2140MHz)	-14 dB
Voltage gain	13.2 dB
Noise figure(DSB)	8.5 dB
IIP3	1 dBm
IIP2	45 dBm
Supply voltage	2.9 V
Current consumption	6.7 mA
Die area	0.76 x 1.15 mm2

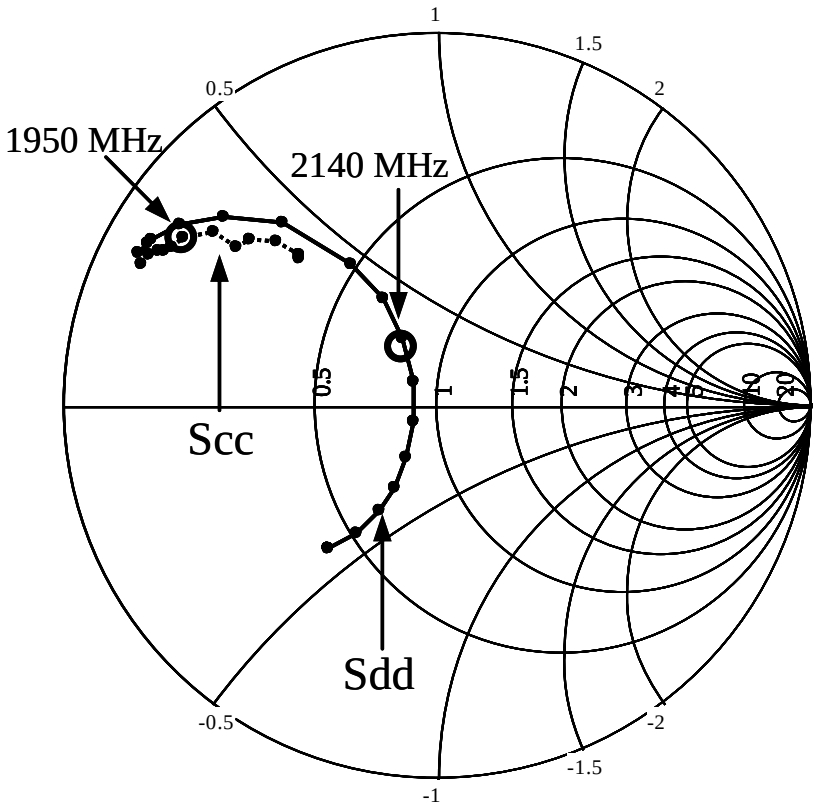


Figure 3.8: Measured input impedance of differential-mode (S_{dd}) and common-mode (S_{cc}).

Figure 3.9 shows the measured results of DC current increase caused by the TX signal. The measured result shows very small DC current increase because the TX input signal is not input to the input transistors by large reflection. On the other hand, the simulated result in the case of using a conventional common-base mixer shown in Fig. 3.7(b) shows much larger DC current increase caused by the even-order distortion of the input common-base transistors with the TX input signal as mentioned in section 2.2.

Figure 3.10 shows the measured results of the BB output noise increase versus TX input power. The result shows that noise degradation does not occur until the TX input power reaches -10dBm. Typically, the maximum output power of the on-chip TX driver amplifier is estimated to be about 4 dBm because the maximum output power specified by 3GPP [8] is 24 dBm and typical gain of the power amplifier is about 20-25 dB [48], [49]. Thus, in the case of the proposed mixer, the required isolation between TX output and RF input is 14 dB in order not to degrade the noise figure. This isolation is easily achievable even in the case of a one-chip TRX.

The simulated result in the case of using a conventional input stage shows that noise degradation occurs when the TX input power is -30dBm. Then the required isolation is 34dB and this value is 20dB higher than that of the proposed QDEMOD.

Figure 3.11 shows the conversion voltage gain for differential RF input measured at certain temperatures. The gain variation is less than 0.2 dB from -20 ℃ to 85 ℃ by using the proposed QDEMOD.

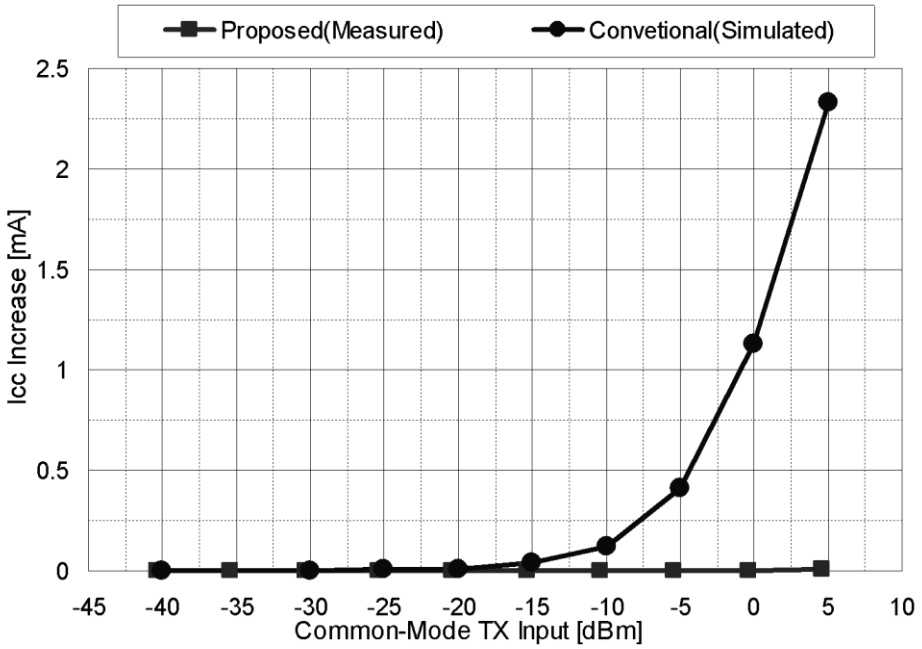


Figure 3.9: Measured and simulated DC current variation caused by the common-mode TX input signal.

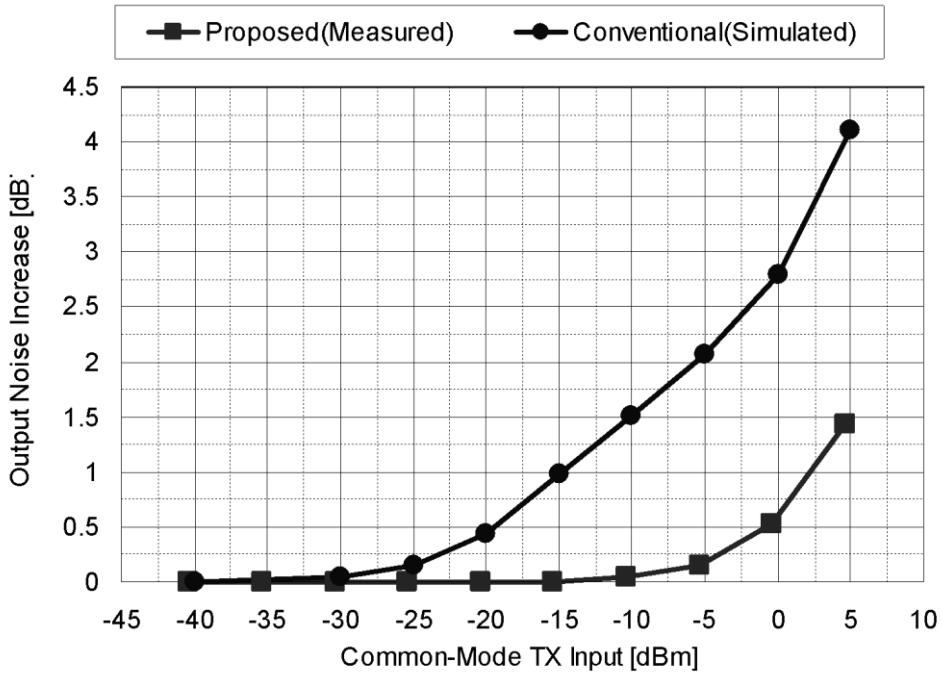


Figure 3.10: Measured output noise variation caused by the common-mode TX input signal.

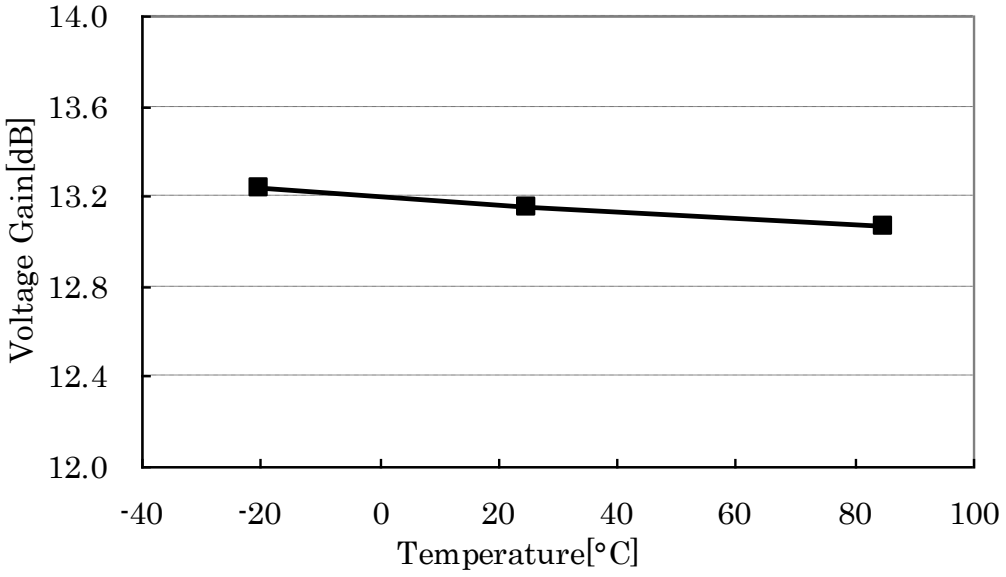


Figure 3.11: Gain variation with temperature.

3.5 Comparison and Summary

Figure 3.12 shows development of integration in recent years for WCDMA application. Horizontal axis means year and vertical axis means circuit block [50]-[60]. The rectangular means integrated circuits in references. The approach of chapter 3 is mapped as the figure and the approach is the first example which has capability of TX and RX circuits in the same die. The QDEMOD with proposed compensating technique using analog circuit is suitable for small and low-cost RF front-end modules and for TRX IC for WCDMA application.

A QDEMOD for a WCDMA direct conversion RX capable of suppressing the common-mode sensitivity has been presented. The proposed circuit employs symmetrical inductors in order to match for differential-mode desired RF signal and to reflect for common-mode TX signal. Simulated and measured results show that the proposed QDEMOD achieves robustness to TX leakage signal. This technique relaxes the isolation specification between TX and RX. The QDEMOD also achieves low gain variation with temperature. The QDEMOD is suitable for small and low-cost RF front-end modules and for TRX IC for WCDMA application. Finally, the QDEMOD was a commercialized in a part of tri-band WCDMA TRX IC.

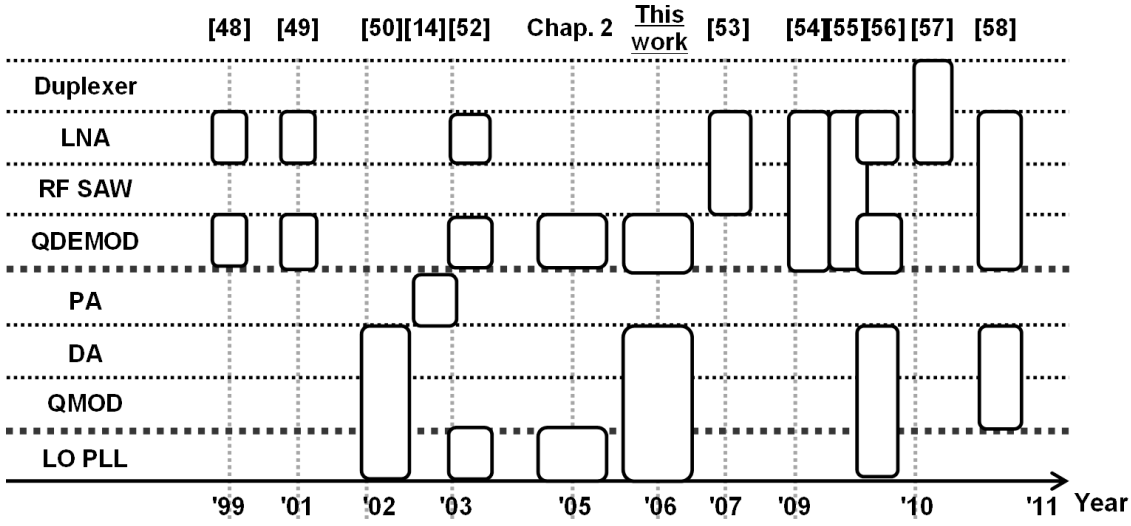


Figure 3.12: Comparison of Integration for WCDMA TRX.

Chapter 4

A 60-GHz RX Front-End With Frequency Synthesizer

This chapter 5 describes a 60-GHz RX front-end chip to substantiate an effectiveness of compensation method by using analog circuits for the issue of performance degradation by insufficient high-frequency performance of integrated silicon devices. The RX chip consists of an LNA, a down conversion mixer and a phase-locked loop synthesizer. The components of the RX chip employ fully differential architecture to avoid influences of parasitic components and the down conversion mixer with compensating technique for lower voltage LO signal for operation.

4.1 Introduction

Millimeter wave application is recently developing for commercial applications such as very high speed wireless data transfer and automotive radar. Millimeter wave is an electromagnetic wave whose wavelength is 1 mm to 10 mm and it is corresponding to 30 GHz to 300 GHz of frequency as shown in Fig. 4.1. Figure 4.2 shows a frequency allocation of millimeter wave band for commercial applications. Very wide, 7 to 9 GHz of frequency band is allocated around 60 GHz and the band is attracting attention for very high speed wireless data transfer using such a wideband. On the other hand, the 60 GHz band signal is attenuated by oxygen in atmosphere as shown in Fig. 4.3 [61] and it is difficult for long range communication as like cellular application. Thus, the 60 GHz band is suitable for high-speed, short-range personal area network at home or office. The other allocated frequency band in Fig. 4.2 is 77 GHz band and it is used for ranging application for automotive radar. Unlike the 60 GHz band signal, the attenuation by atmosphere is much less than that of the 60 GHz band signal. Thus, the signal can be used for ranging more than 100 m distance using high-directivity antenna.

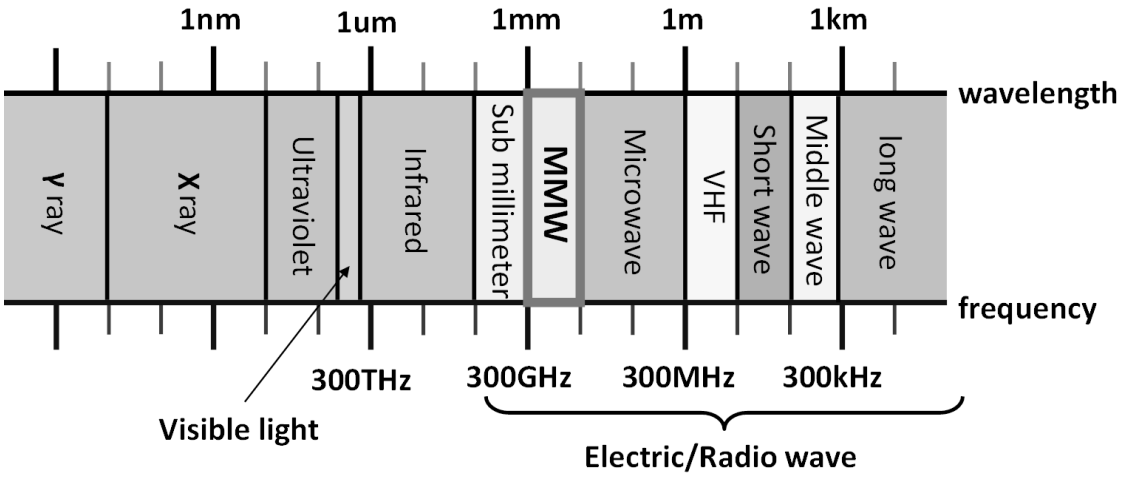


Figure 4.1: Electromagnetic wave with wavelength/frequency.

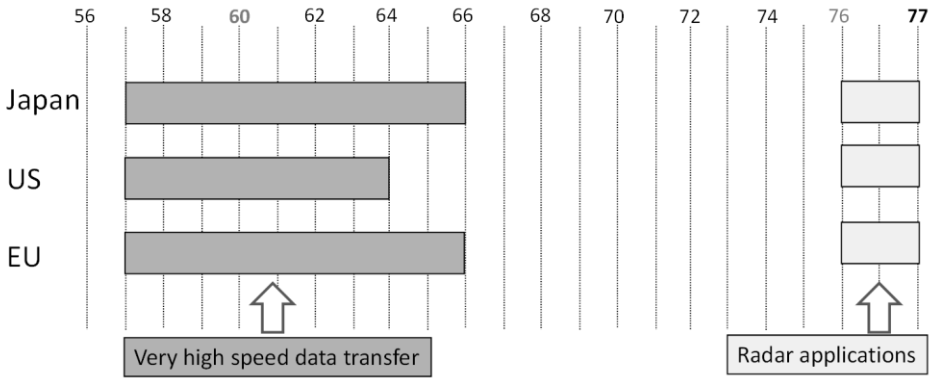


Figure 4.2: Frequency allocation of the commercial millimeter wave applications.

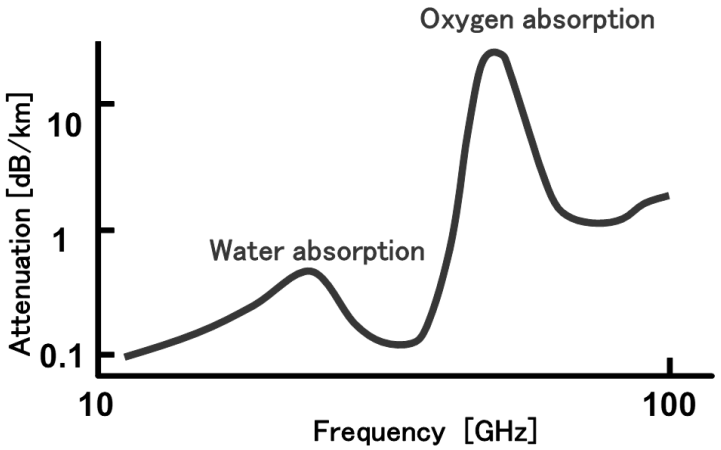


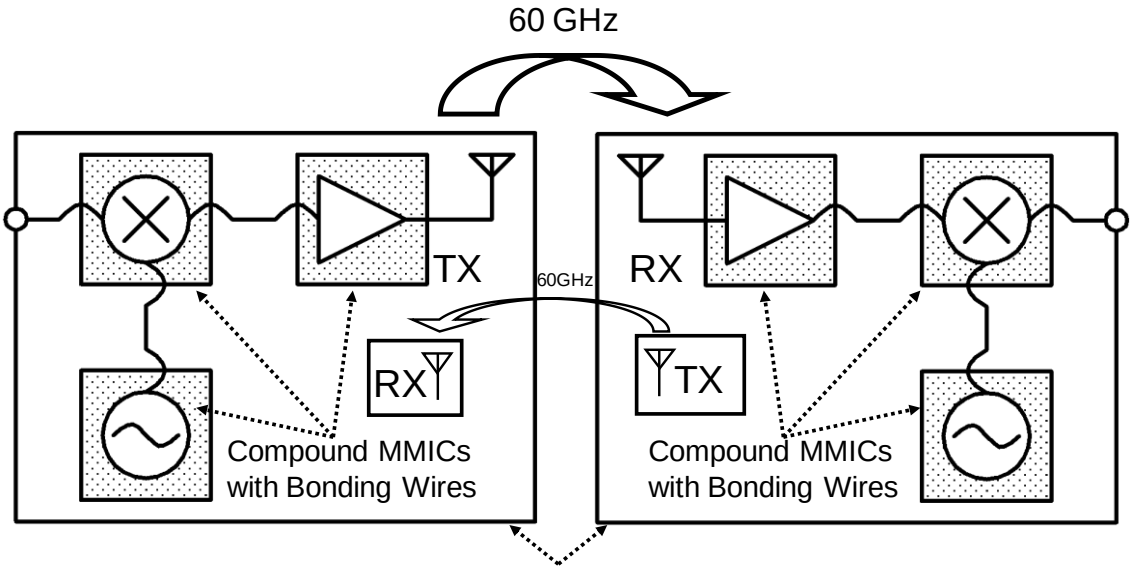
Figure 4.3: Propagation attenuation characteristic for atmosphere [61].

Figure 4.4(a) shows a conventional TRX module for 60-GHz signal using compound semiconductor MMICs. Many MMICs are required in order to increase the yield of the modules because low process yield of the compound semiconductor prevents high integration of MMICs. The MMICs are mounted on a ceramic board and require bonding wire of accurate length to propagate 60-GHz signal outside the MMICs. This is because the ceramic board enables use of low loss transmission lines and the accurate length of the bonding wire enables adjustment of the length of stubs on the ceramic board and connection of the MMICs to the ceramic board. Thus, the module with compound semiconductor MMICs requires many devices and the cost is high.

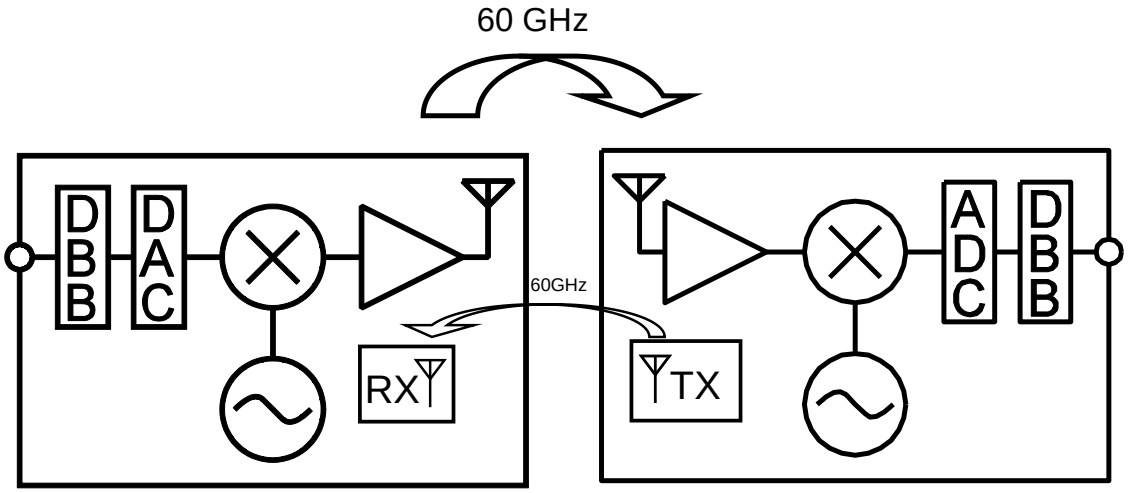
On the other hand, in terms of process development, the challenge of realizing 60-GHz TRX using silicon process is attracting attention [62]. The silicon process ICs such as Si-Ge BiCMOS and CMOS process are much lower in cost than the compound semiconductor process ICs. Since the yield of silicon processes is much higher than that of the compound semiconductor process, highly integrated TRX is achieved. In the case of using an on-chip antenna on RF IC, the ceramic board and the accurate bonding wire mentioned above are not required and the ceramic board can be replaced by an inexpensive resin board because there are no off-chip 60-GHz interfaces. In particular, in the case of using CMOS process, a complete one-chip TRX with RF front-end and A/D or D/A converter and digital baseband processor as shown in Fig. 4.4(b) can be realized.

Recently, 60-GHz RF front-end using Si-Ge bipolar process and RF building blocks using the advanced CMOS process have been reported [63], [64]. In this work, a 60-GHz RX front-end IC is demonstrated. The RX IC consists of an LNA, a downconversion mixer (Dmix) and a PLL synthesizer using 90 nm CMOS process. This is the first report of the RX IC including PLL synthesizer for 60-GHz signal. This RF front-end IC can be applied for BPSK demodulator by using synchronized detection. And the 60-GHz LNA, mixer and synthesizer can be developed to the direct conversion RX front-end by achieving accurate I/Q signal generator and low DC offset mixers.

This paper is organized as follows. Section II identifies design issues concerning realization of CMOS 60-GHz RX circuits. The design of the developed RX and each building block is presented in Section III, which is followed by the presentation of RX measured results in Section IV. Conclusions are presented in Section V, the final section of this paper.



(a) MMICs on Ceramic Board



(b) CMOS IC with On-Chip Antenna

Figure 4.4: 60 GHz TRXs using compound semiconductor MMICs (a) and CMOS ICs (b).

4.2 Design Issues for CMOS 60-GHz RX Front-End

There are many design issues concerning realization of CMOS 60-GHz RX RF front-end. We pay attention to the following two issues in order to reduce design time and power consumption of the RX IC.

The first issue is the effect of parasitic elements. Figure 4.5(a) shows a single-ended amplifier, Fig. 4.5(b), is described in the Sec. III.C). This amplifier is composed of an NMOS device and short stubs for input matching and output load / matching circuit. These short stubs work as inductors and their impedance Z_{stb} is controlled by the length of the stub as shown in equation (4.1),

$$Zstb = jZ_0 \tan\left(\frac{d}{\lambda} \times 2\pi\right) \tag{4.1}$$

where Z_0 is characteristic impedance of the transmission line of the stub, d is physical length of the stub and λ is the wavelength of the signal frequency in the silicon substrate. As there are parasitic elements on the ground, voltage supply and bias node, the input and output impedances are not equal to those in the case of using Z_{stb} only. Therefore, the parameter of the parasitic elements must be estimated accurately using, for example, electromagnetic simulator or must be measured and modeled by using test devices. However, in any case, the layout of the ground pattern is like perforated “cheese” owing to strict design rule of the layout pattern and the ground and supply have many connections on the ICs. Therefore, the simulation or measurement should be done with the whole pattern of these nodes. And the bonding wires also should be simulated or measured in the case of using packaged RF ICs. Thus, the estimation with simulation or measurement is time-consuming. Furthermore, when the failures of the fabricated ICs caused by unpredicted parasitic elements are detected, the ICs must be redesigned to tune the Z_{stb} by adjusting the length of the short stubs and be fabricated again.

The second issue is the need for large LO signal for mixer. Figure 4.6 shows the mixer and the VCO with output buffer and matching circuits for these circuits. Transmission lines are used as stub or phase rotator for impedance matching. Since the input or output impedance of these circuits is tuned to the characteristic impedance of the transmission line, the interconnection of these circuits is achieved by simple connection of transmission line. Thus, the impedance matching between these circuits is preferable for flexibility of the placement of these circuits on the same die. However these transmission lines have resistive loss due to the sheet resistance of the metal. And the LO signal amplitude should be large to drive the mixer. So, the VCO output buffer capable of outputting large LO signal, compensating the loss of the transmission lines, is required. Such LO output buffer requires large current consumption and causes unwanted large LO signal emission.

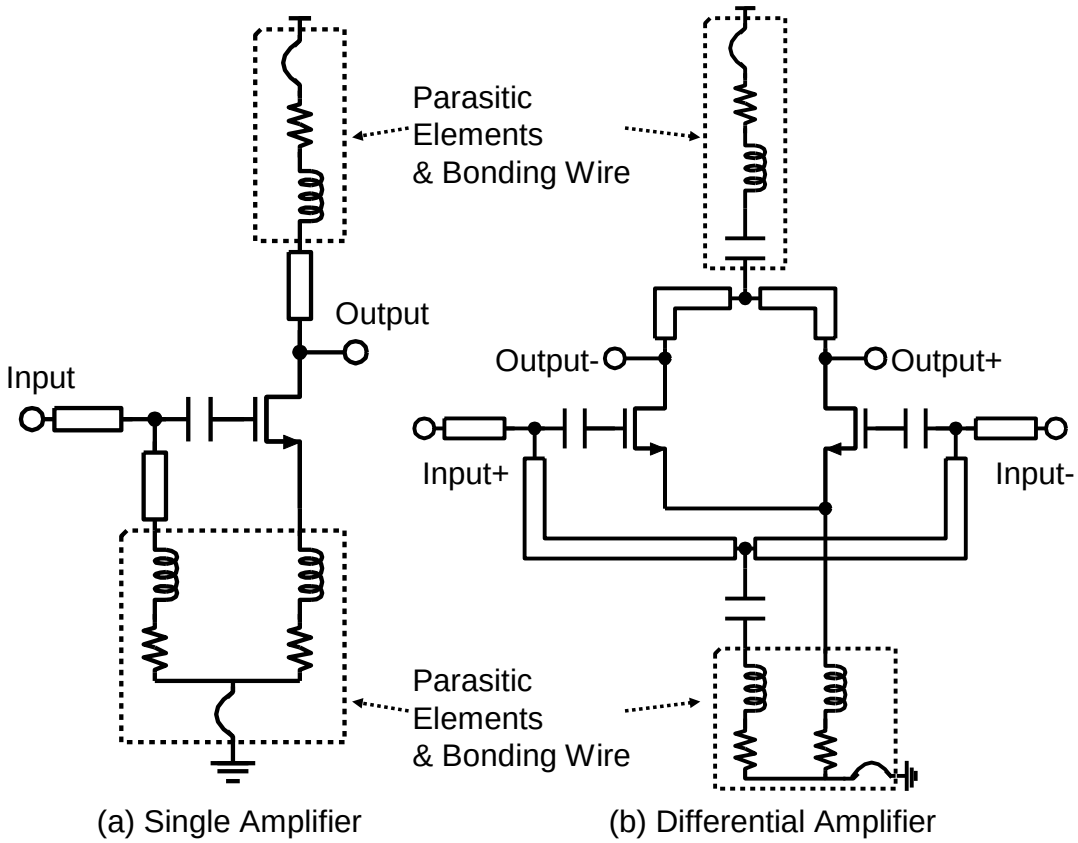


Figure 4.5: Single-ended amplifier (a) and differential amplifier (b) with short stubs and parasitic elements.

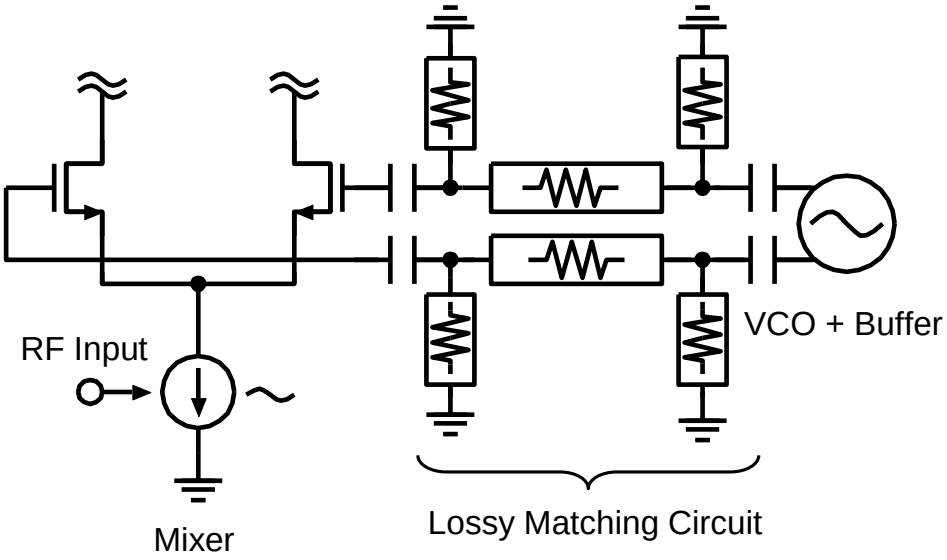


Figure 4.6: VCO and mixer circuit with input interface circuit.

4.3 60-GHz RX Circuits

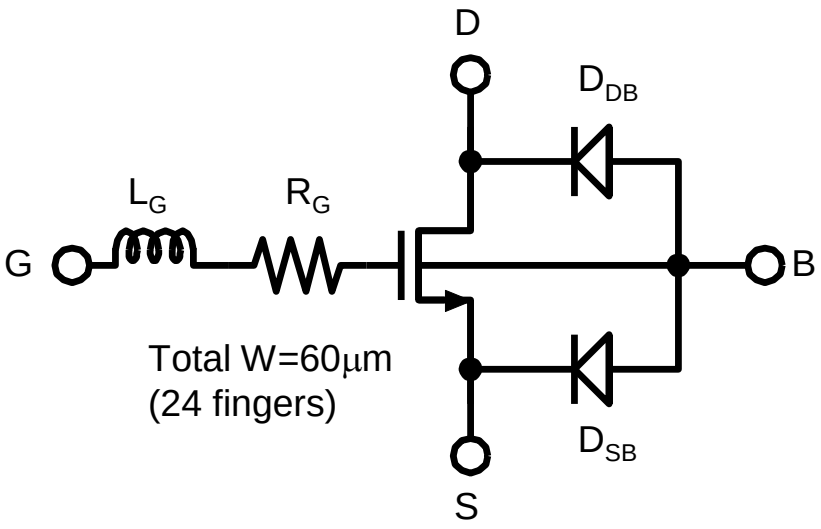
4.3.1 Transistor Model and Transmission Line

Accurate device models are required to achieve desired RX IC operation. In particular, MOS transistor and transmission line are key devices of 60-GHz circuit. So, the test devices were fabricated before designing the RX IC and the device parameters of these devices were extracted. Figure 4.7(a) shows a schematic of the device model of an NMOS transistor. The model consists of BSIM3 transistor, drain-bulk/source-bulk diodes, gate inductor and gate resistor [65], [66]. Since BSIM3 transistor does not have the gate resistance and bulk to drain/source resistance, the external gate resistor and the parasitic resistor in the diodes represent the loss at high-frequency. Note that source and drain resistance are included in BSIM3. The parameters of the NMOS, diodes, R_g and L_g are extracted by measurement and optimization at fixed gate length and width, 90 nm and 2.5 μm. The finger number is the design parameter and the device parameters of diodes, R_g and L_g, are scaled with the number of the gate fingers.

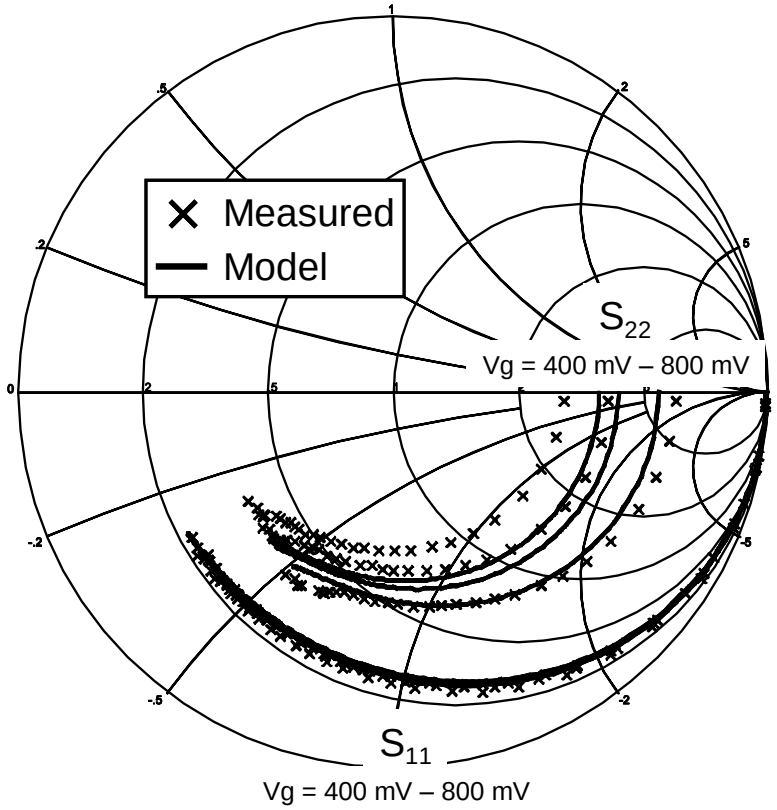
Figs. 4.7(b) and 4.7(c) show the S-parameters of the measured and simulated results of the extracted model from 0.5 to 65 GHz. The total gate width is 60 μm with 24 fingers. Model parameters were optimized for especially high-frequency around 60 GHz. Thus, the measured results of S_{11}, S_{22} and S_{21} correspond to those simulated around 60 GHz. The measured maximum available gain (MAG) at 60 GHz is 8.1 dB with at 0.25 mA per 1 μm gate width of drain current.

A grounded coplanar line is used as the transmission line of RX IC [67]. Figure 4.8(a) shows the cross-sectional view of the transmission line. The side grounded wall is composed of stacked metal and the lower end of the stacked metal is connected to the bottom grounded metal plate. This structure is able to avoid silicon substrate loss owing to the bottom grounded plate and able to isolate signal from other components owing to stacked side grounded metal. The transmission line is designed by using 3-dimensional electromagnetic simulator to estimate a fringe effect of each metal layer. The characteristic impedance of the transmission line is designed to be 50 Ω

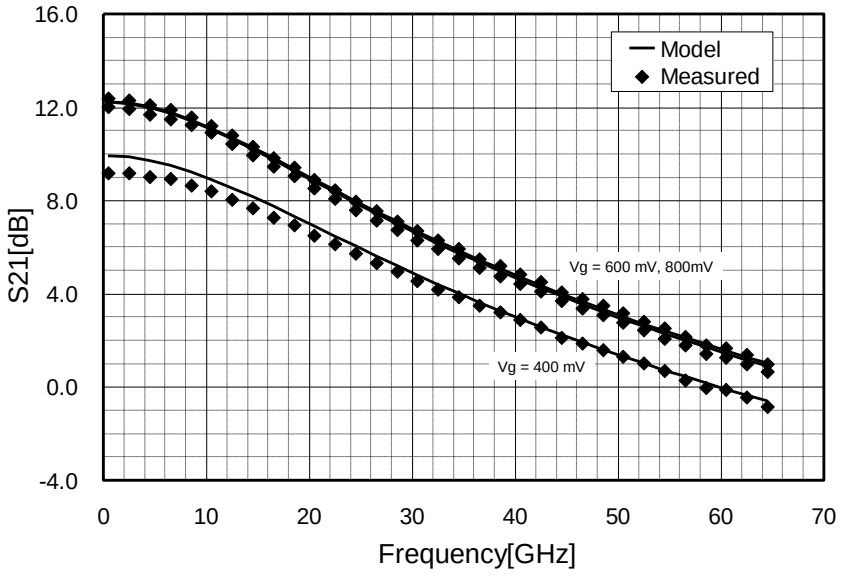
Figs. 4.8(b) and 4.8(c) show measured S_{11} and S_{21} of the 200 μm-length transmission line from 0.5 to 65 GHz. This shows the characteristic impedance Z_0 is about 45 Ω which matches the design target. And the loss coefficient α is 120 Np /m or 0.52 dB/mm, phase coefficient β is 2400 rad/m or 137.5 deg/mm and Q as β/α is 20 at 60 GHz.



(a) NMOS transistor model circuit

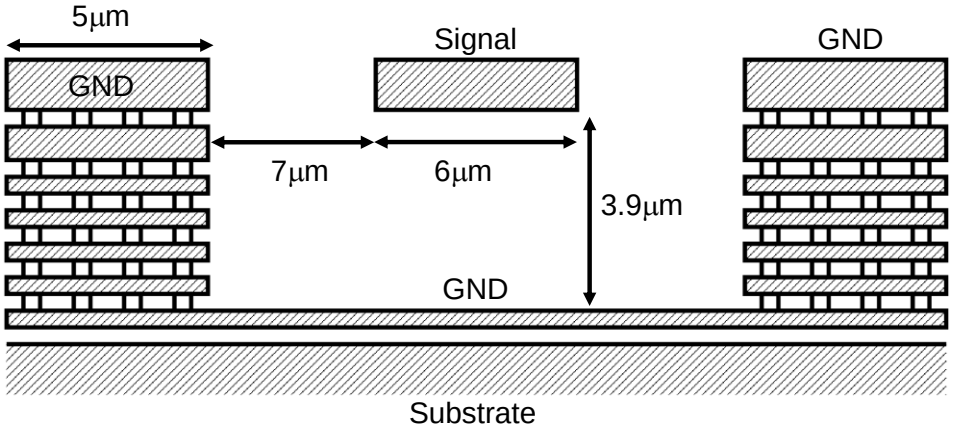


(b) Measured and simulated results using a model of S_{11} and S_{22}.

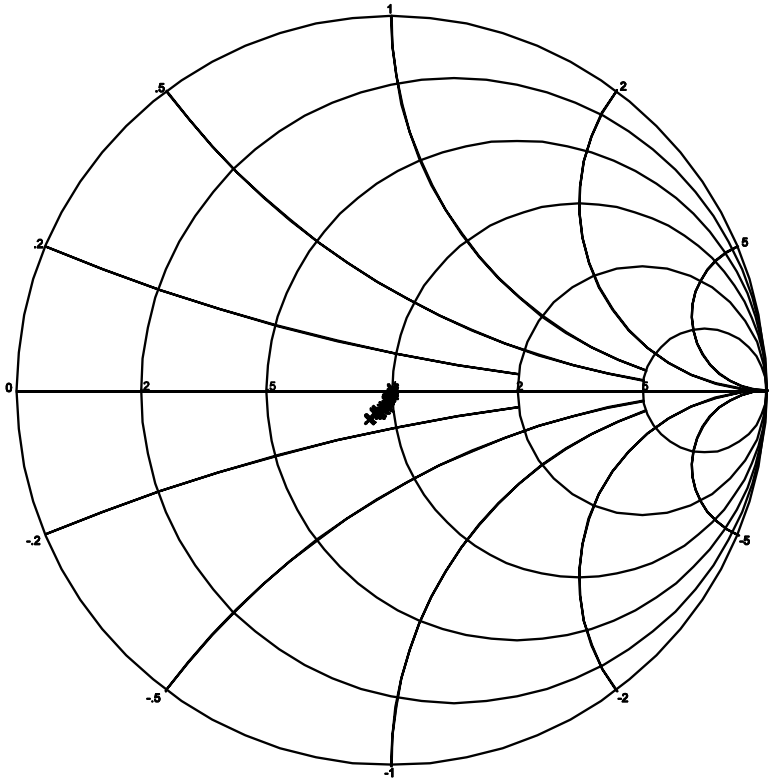


(c) Measured and simulated results using a model of S_{21}

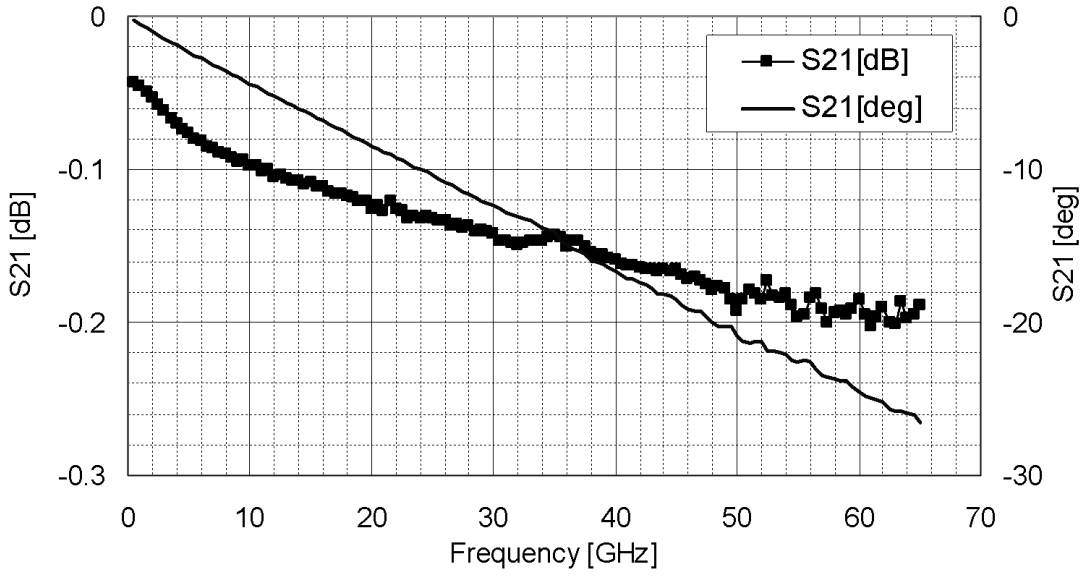
Figure 4.7: Transistor model circuit (a) and measured and simulated S-parameter of MOS transistor (b), (c).



(a) Cross-sectional view of the transmission line.



(b) Measured S_{11}



(c) Measured S_{21}

Figure 4.8: Transmission line structure (a) and the measured result of S_{11} (b), S_{21} (c).

4.3.2 Fully Differential RX

Figure 4.9 shows a 60-GHz RX block diagram. The RX employs fully differential structure, including differential on-chip dipole antenna. The on-chip antenna length is half the length of the wavelength at 60 GHz with wavelength compression on the silicon substrate. Since the antenna is divided in two at its center and these divided ends are connected to the input node of the LNA, it generates differential signal from input radio wave and the differential signal is input to LNA. Figure 4.5(b) shows an example of a differential amplifier. The short stubs between plus and minus terminals of the amplifier's input and output are connected to each other. So, the first design issue mentioned above is solved because these short stubs are connected to the common node and the parasitic elements are neglected for differential signal.

Each block in Fig. 4.9 has input and output impedance of 100 Ω for differential signal to make use of on-chip 50 Ω transmission lines for inter-stage connection. Each building block is discussed in detail as follows.

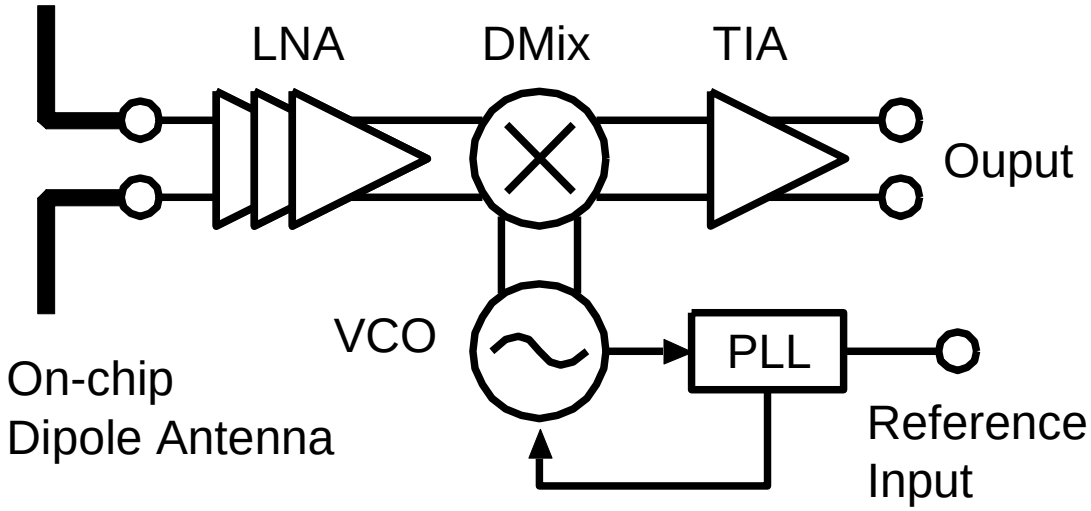


Figure 4.9: RX front-end.

4.3.3 Low Noise Amplifier (LNA) and On-Chip Antenna

As mentioned above, the maximum gain of the NMOS transistor is 8 dB at 60 GHz. So, the LNA has 3-stage amplifiers in order to achieve the gain of larger than 10 dB, including the loss of the passive components. Each amplifier employs a fully differential and cascode structure as shown in Fig. 4.10. Short stubs, which consist of transmission lines and whose nodes are connected, are used for the load and the matching circuits. The bias current of each stage is about 12 mA to give the operating point that allows maximum gain of the transistor as mentioned above. These three amplifiers of the LNA are identical circuits as shown in Fig. 4.10 and the input and output impedance of the amplifier is designed to be 100 Ω in order to connect each circuit via 50 Ω transmission line.

The individual LNA test circuit is fabricated and the RF performance of the LNA is measured by using a 4-port vector network analyzer to measure differential signal. Figure 4.11 shows the measured S-parameters. The input and output differential-mode S-parameter (S_{dd11}, S_{dd22}) is lower than -10 dB from 60 GHz to 66 GHz and from 58 GHz to 66 GHz, respectively. The measured differential gain S_{dd21} is 13.7dB at 60 GHz and peak gain is 16.3 dB at 63 GHz as shown in Fig. 4.11 with 35.7mA current consumption. On the other hand, the common-mode gain S_{cc21} is 10 dB or more lower than that of the differential-mode. Unlike the case of differential-mode, common-mode gain is degraded by the parasitic elements as shown in Fig. 4.5(a). The noise figure (NF) of the LNA is an important performance but the measurement is difficult. Therefore, the LNA NF was measured indirectly by using the LNA gain, the whole RX NF and the NF of the downconversion mixer. The calculated LNA NF is 7.8 dB at 61.5 GHz.

Figure 4.12 shows on-chip dipole antenna structure and the simulated result of differential-mode S_{11} by using 3-dimensional electromagnetic simulator. The antenna is half of the wavelength and includes pads. Input impedance is adjusted around 100 Ω by adjusting the length from pad, antenna width and length from antenna to the edge of the chip. Simulated directive gain is 3.4 dBi and whole gain is -9 dB because the RF signal is injected to the low impedance silicon substrate.

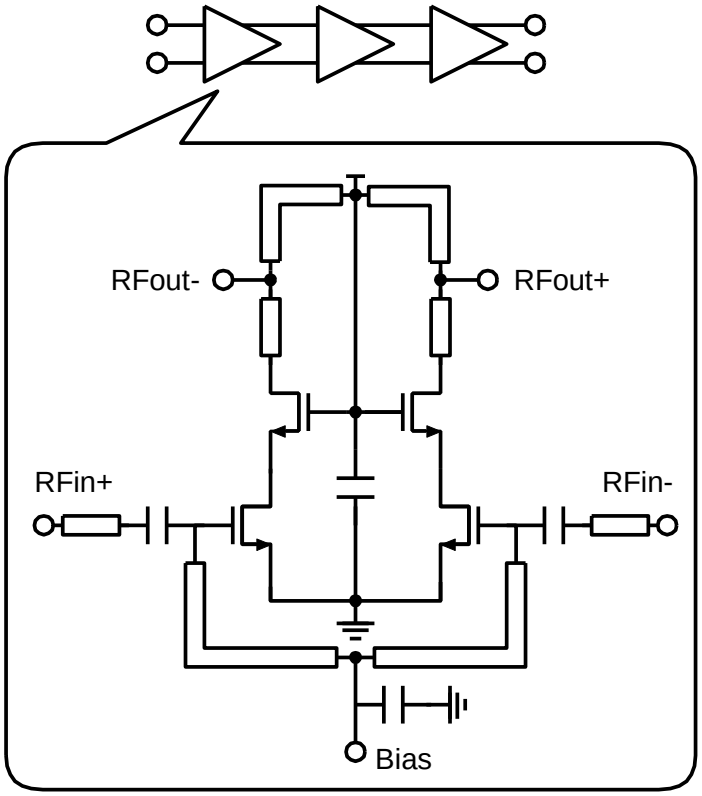


Figure 4.10: LNA and its individual stage.

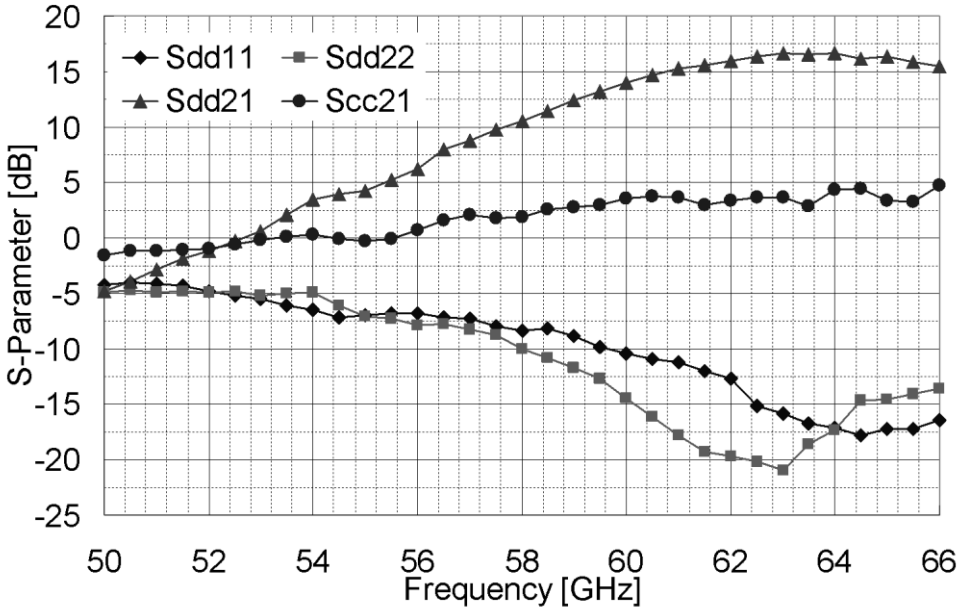


Figure 4.11: LNA measured result.

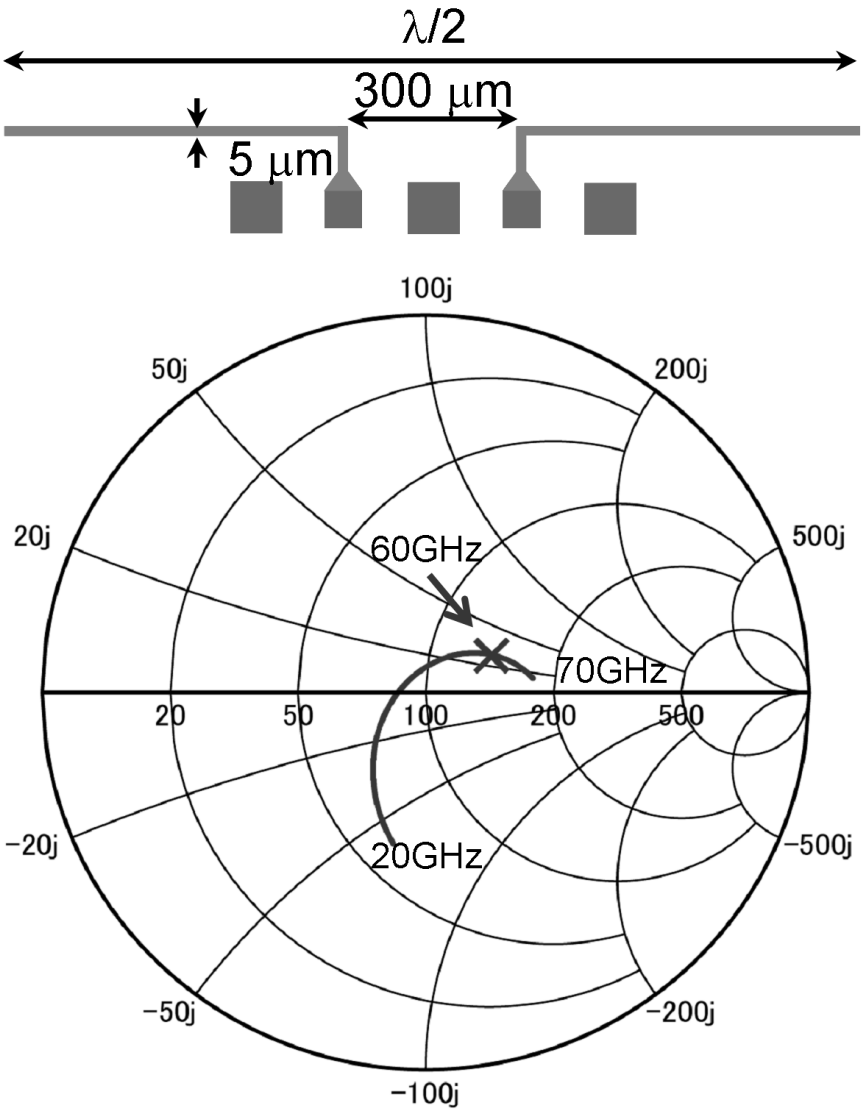


Figure 4.12: On-chip antenna and simulated S_{11}.

4.3.4 Downconversion Mixer (Dmix)

The Dmix consists of a mixer core circuit and a trans-impedance amplifier (TIA). The mixer core is a double balanced structure as shown in Fig. 4.13. To solve the second design issue mentioned above, the bias current of switching transistor is shunted by current source of I_{shunt} in order to reduce required LO signal amplitude. The instantaneous drain current of the switching transistors, I_{switch}, varies with LO signal amplitude V_{LO}. In the case of using shunt current source, the I_{switch} is expressed as

$$I_{switch} = (I_{tail} - I_{shunt}) - k\frac{W}{4L}V_{LO}\sqrt{\frac{4(I_{tail} - I_{shunt})}{kW/L} - V_{LO}{}^2} \tag{4.2}$$

where k, W, L is a device parameter of the switching NMOS transistors and I_{tail} is a tail current of the switching pair. In order to achieve maximum conversion gain of the switching mixer, the switching transistors must be switched completely by LO signal. In other words, the I_{switch} must reach to $I_{tail} - I_{shunt}$. The required V_{LO}, V_{LOSAT}, is calculated from equation (4.3):

$$V_{LOSAT} = \sqrt{\frac{(I_{tail} - I_{shunt})}{2kW/L}} \tag{4.3}$$

This shows lower V_{LOSAT} can be obtained by I_{shunt}. So, the required LO amplitude at the mixer LO input port becomes smaller than in the case without shunt current source. And the required output power for the VCO output buffer is decreased and the current consumption of the buffer can be reduced. We designed the I_{shunt} = 3/4 I_{tail} and the V_{LOSAT} is decreased by half.

The input transconductor (Gm) stage is composed of a common-gate circuit that enables wideband operation. However, much of the output current of the Gm stage is shunted to ground via parasitic capacitances at the common source node of the switching transistors because the input resistance of the switching transistor is large owing to the use of shunt current source mentioned above. So, short stubs are connected between the source node of the switching transistors and ground node to resonate at 60 GHz with the parasitic capacitors. Then the current flow into parasitic elements is suppressed and high conversion gain can be obtained [67].

The performance of the fabricated individual mixer test circuit was measured with the measurement setup as shown in Fig. 4.14. The RF input signal and the LO signal are supplied from external signal generator via external balun consisting of phase rotator and coupler. The differential signal level and the phase at the output of the probe are adjusted by using variable attenuator and phase rotator. The low-frequency output signal is measured by spectrum analyzer with low-frequency external balun. The frequency response of these external components is measured and the loss is calibrated for performance measurement of the mixer. And the noise figure is calculated with conversion gain and output noise level. The conversion gain versus output frequency with fixed 60-GHz LO signal is shown in Fig. 4.15(a). 7.8 dB conversion gain is obtained and the DSB NF is 14 dB at 100 MHz output frequency. Figure 4.15(b) shows the conversion gain and the NF versus

LO input power. This shows the gain and the NF saturated at around -7 to -5 dBm LO input power. This power can be generated from on-chip VCO and output buffer with moderate current consumption.

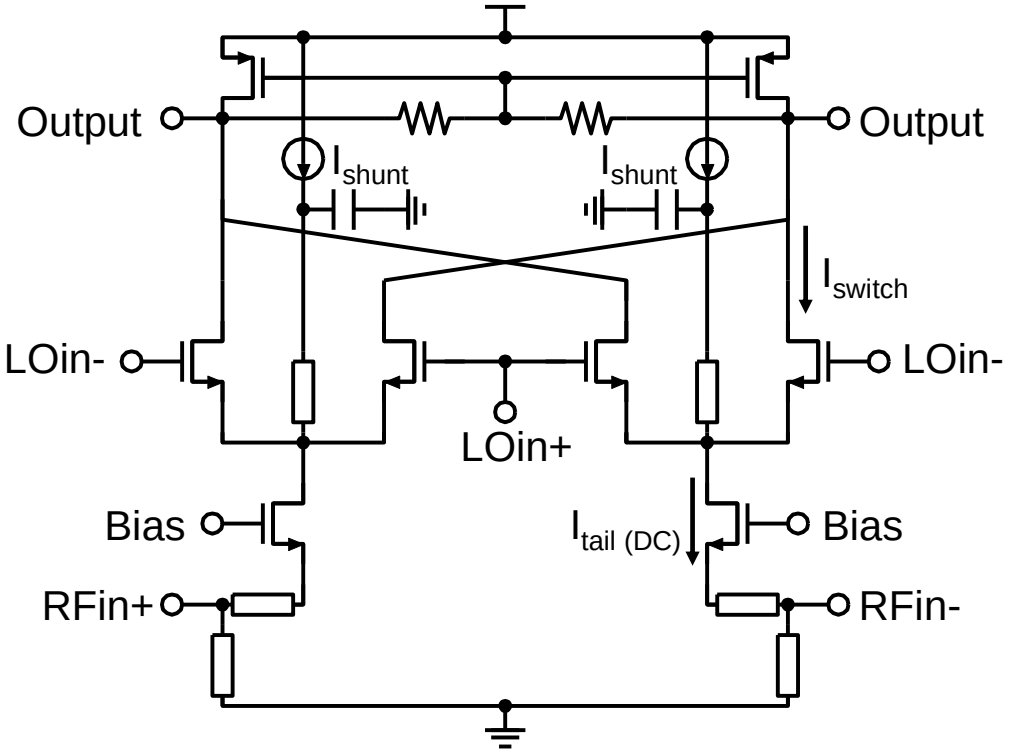


Figure 4.13: Mixer circuit.

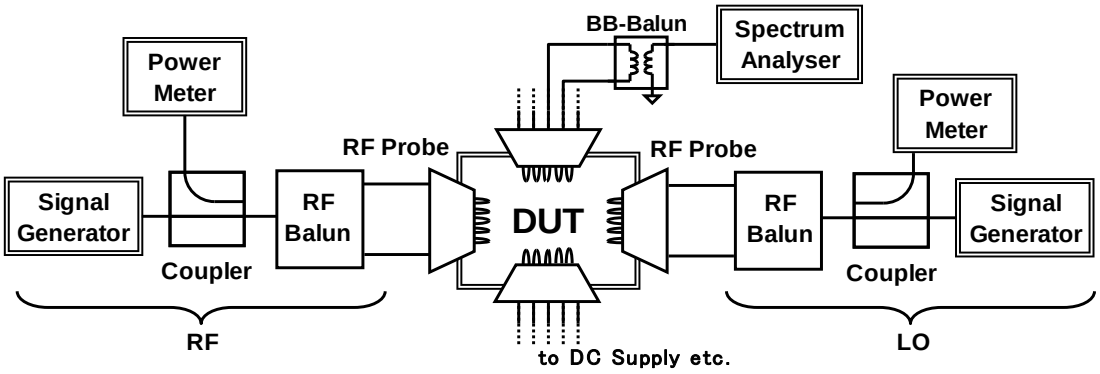
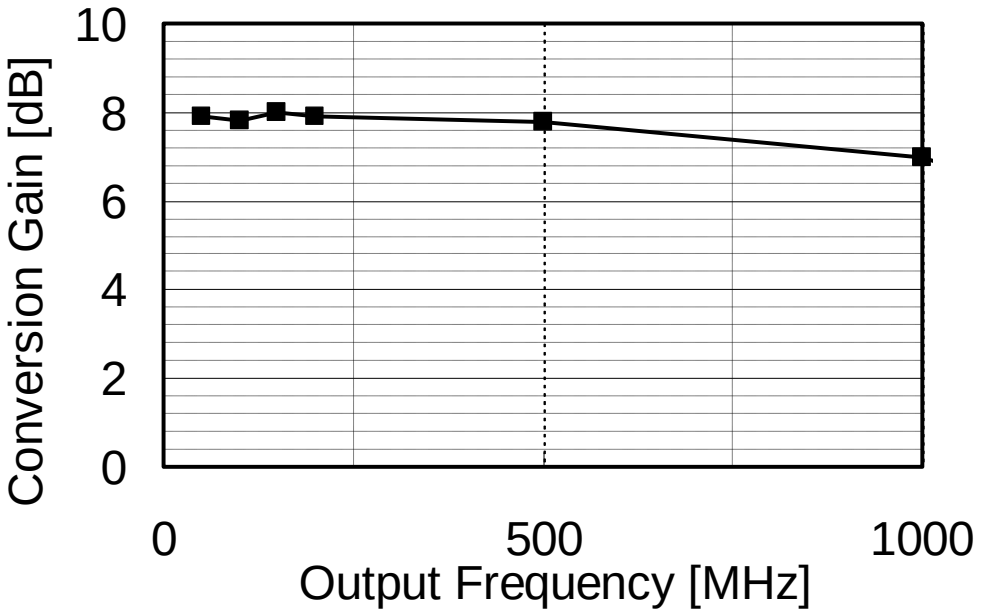
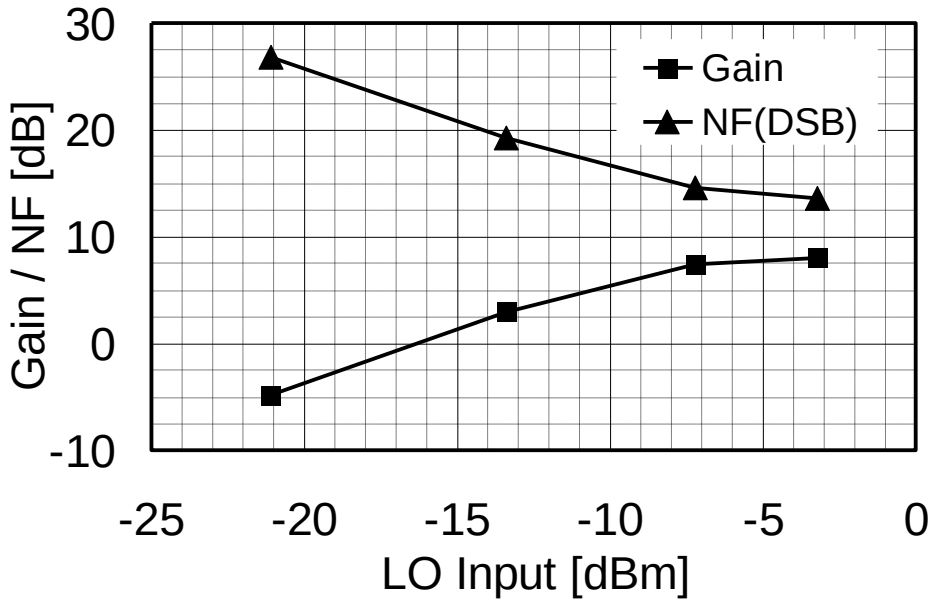


Figure 4.14: Measurement setup for mixer.



(a) Measured mixer gain versus output frequency.



(b) Measured mixer gain and NF versus LO input power.

Figure 4.15: Mixer gain (a) and NF variation with LO input power (b).

4.3.5 Phase-Locked Synthesizer

The synthesizer is an integer PLL and consists of a 60-GHz VCO, a prescaler, an integer divider, a phase detector and a charge pump with a loop filter. The VCO is a cross-coupled LC tank oscillator whose tank circuit is composed of an inductor consisting of transmission line and accumulation MOS varactor. Measured VCO oscillation range was from 61.2 GHz to 64.4 GHz with more than -7 dBm output power [68], which is enough to drive the mixer as shown in Fig. 4.15(b). The phase noise was measured with external balun, external harmonic mixer, external divider and VCO signal analyzer. The phase noise was -90 dBc/Hz at 1 MHz offset with 61-GHz oscillating frequency [68].

A prescaler shown in Fig. 4.16 is a ring oscillator type injection locked 1/4 divider. The load of the divider is not an inductor as in [69], [70], but a PMOS active load. Thus, the prescaler is small and it can be located close to the VCO. The 15-GHz divided signal is further divided by 256 by the integer divider and then input to the phase detector. The division ratio is fixed at 1024 in this PLL and the reference frequency is around 60 MHz. The output signal frequency of the synthesizer is controlled by changing reference signal frequency. The measured locking range of the individual PLL synthesizer was 1.7 GHz without changing the bias condition of the prescaler. And the phase noise of the PLL is -80 dBc/Hz dB at 1 MHz offset with 61.4 GHz oscillating frequency [69]. The phase noise is higher than that of the VCO due to the noise of reference and PLL because the loop bandwidth is a few hundred kHz.

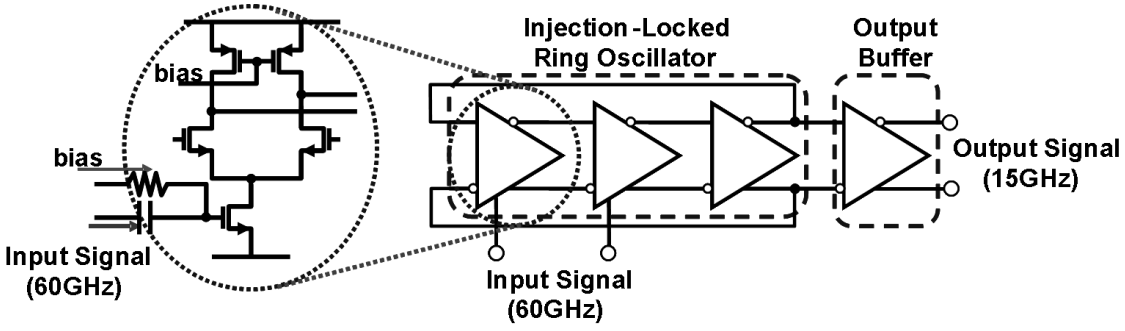


Figure 4.16: Injection locked frequency divider for 60 GHz prescaler.

4.4 RX Measured Results

Figure 4.17 shows a chip micrograph of the RX chip. This chip was fabricated in 90 nm CMOS process and the die area is 2.4 mm × 1.1 mm without pads. The on-chip antenna was connected to LNA.

The measurement setup of the RX chip is similar to the case of the mixer circuit as shown in Fig. 4.14, but there is no external LO signal generator. In order to measure RX performance accurately, the on-chip antenna was not connected and pads are connected directly to the LNA and the 60-GHz signal is input from external signal generator. The differential RF input signal was input to LNA via external balun and RF probe and the low-frequency output signal was measured by spectrum analyzer.

Figure 4.18 shows a measured gain of the RX IC versus RF input frequency with fixed output frequency of 100 MHz. The input RF frequency was changed by external signal generator and the internal LO frequency was changed by PLL reference frequency of around 60 MHz from external signal generator. The measured gain was 21.8 dB to 22.5 dB from 61.34 GHz to 63.40 GHz. Note that measured PLL locking range of the RX chip was about 500 MHz with fixed bias condition and it is narrower than that of individual PLL test circuit because the prescaler input signal from the VCO is single-ended unlike the case of the individual PLL and the input signal is smaller than the case of individual PLL. Thus, the frequency response shown in Fig. 4.18 was measured by adjusting the operating point of the prescaler. The measured DSB NF was found to be 8.4dB at 61.5 GHz of RF frequency by calculating the output S/N with the spectrum analyzer. The current consumption of the whole RX is 120 mA with 1.2 V supply.

RX chip with on-chip dipole antennas was also measured. A photograph of the measurement setup is shown in Fig. 4.19. The RX chip was mounted on an evaluation board made of resin. The RF input signal was injected by using an external horn antenna placed at a distance of several centimeters from the on-chip antenna and the output signal was measured. The measured output signal was about -15 dBm at 100 MHz. The result is consistent with our expectation which is calculated from the estimated gain of the on-chip antenna from electromagnetic simulation as described in section III C, the gain of the RF chip as shown in Fig. 4.18, the output power from the external horn antenna measured by using two opposed horn antennas and the distance from horn antenna to RX IC. Therefore, it was confirmed that the RX chip functions with the on-chip antenna.

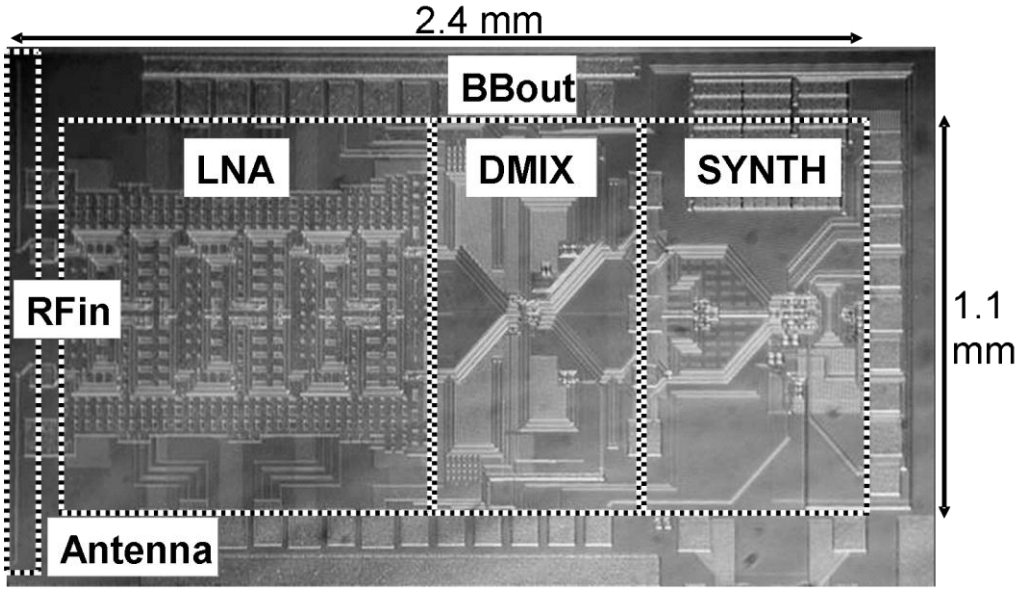


Figure 4.17: Chip photograph of the RX IC.

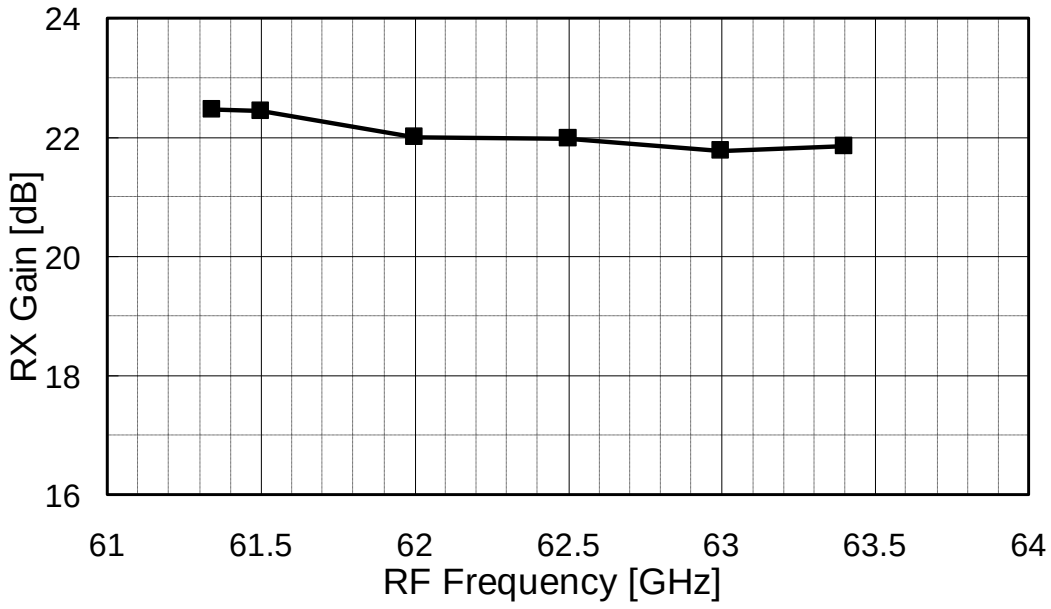


Figure 4.18: Measured RX gain with RX input frequency.

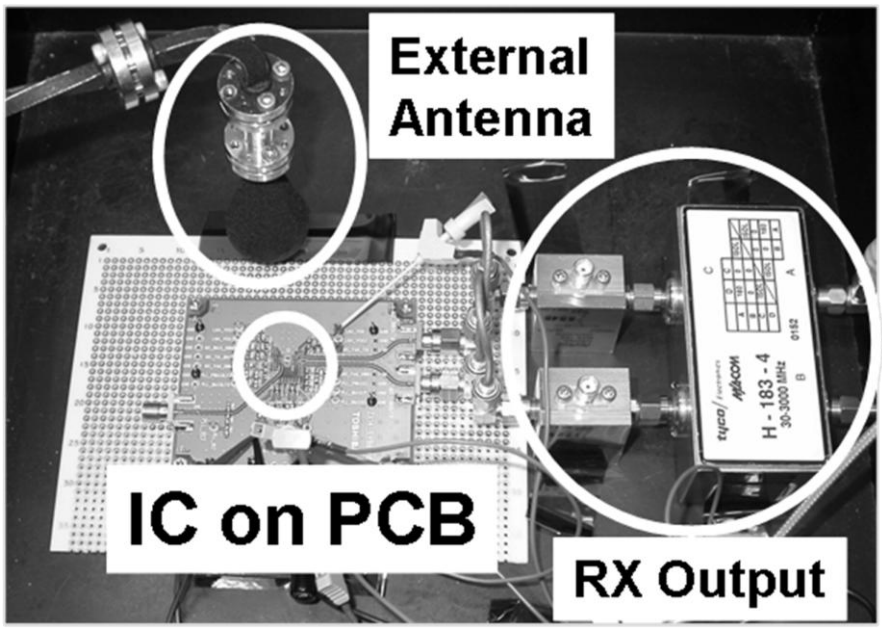


Figure 4.19: Measurement setup for RX IC with the on-chip antenna.

Table 4.1 Performance Summary.

LNA	
Gain	13.7 dB @ 60 GHz, 16.2 dB @ 63 GHz
VSWR	1.62 @ 60 GHz, 1.38 @ 63 GHz
NF	7.8 dB @ 61.5 GHz (Calculated by using RX and Mixer NF)
Current Consumption	37.5 mA @ Vdd = 1.2 V

Downconverter	
Gain	8.2 dB @ 60 GHz
NF	14 dB @ 60 GHz
Current Consumption	18 mA @ Vdd = 1.2 V

Synthesizer	
Operating Frequency	61.35 GHz-63.09 GHz
VCO Phase Noise	-90 dBc/Hz @1 MHz offset, fc = 61 GHz
Current Consumption	70 mA @ Vdd = 1.2 V

RX	
Gain	21.8 dB-22.5 dB @ 61.34 GHz - 63.4 GHz
NF	8.4 dB @ 61.5 GHz
Current Consumption	120 mA @ Vdd = 1.2 V

4.5 Comparison and Summary

Fig. 4.20 shows a comparison of the required LO input power for down conversion mixers [71]-[77]. The proposed mixer has the lowest required power than other approaches. These results indicate that the proposed compensating technique using analog circuit can be applied very high-frequency wireless system.

A 60-GHz CMOS RX chip was presented in this paper. The design issues were solved with fully differential RX front-end and the Dmix operating with low LO amplitude. The fabricated RX IC consisting of the LNA, Dmix and synthesizer works from 61.34 GHz to 63.40 GHz and 22 dB gain and 8.4 dB DSB NF at 61.5 GHz were achieved. And the RX chip receives radio signal with on-chip dipole antenna. These results indicate the possibility of realization of low-cost CMOS single-chip 60-GHz TRX.

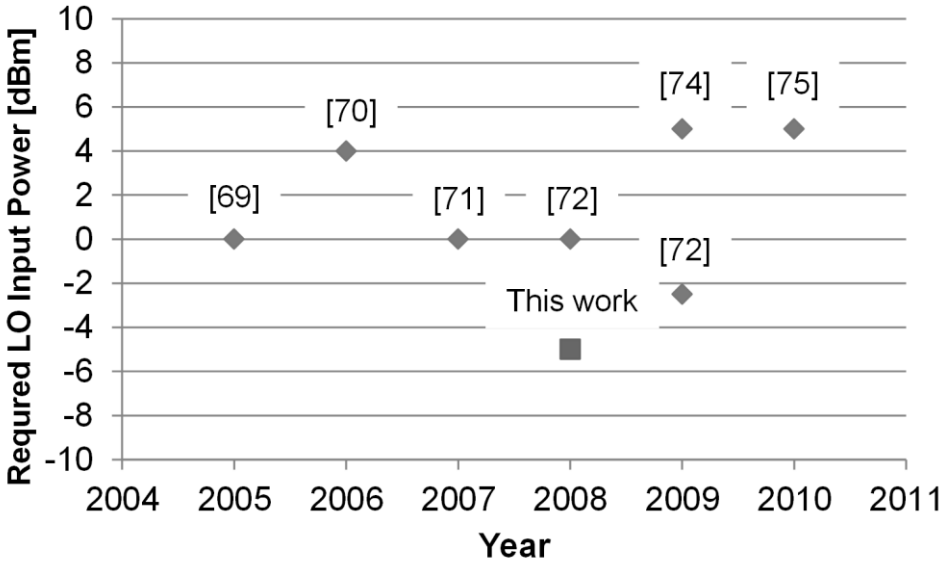


Figure 4.20: Comparison of required LO input power for 60 GHz downconverter.

Chapter 5

A 60-GHz TRX Chipset for Short-Range Wireless Communication

This chapter 6 describes a fully-integrated 60GHz TRX chip for substantiating much highly integrated system. In order to realize TRX in the same die, low loss TRX selecting switch and lower power high-frequency circuit is required. A proposed TRX switch and low power LNA/Mixer circuit adopting a compensation technique using analog circuits is substantiated.

5.1 Introduction

High-speed and energy-efficient wireless communication using 60 GHz band is attracting attention and recent works have realized a highly integrated CMOS TRX [78]-[80]. This chapter presents a first fully integrated chipset for short-range/one-to-one wireless communication. The chipset is composed of 2 chips, an RF chip with in-package antenna and a BB chip including physical (PHY)/media access control (MAC) layer. The chipset achieves 2.62 Gb/s PHY data rate and 2.07 Gb/s MAC throughput. The MAC is designed to have a high efficiency feature due to short interval DATA/Acknowledgement (ACK) frame exchange. It is realized by an RF technique of fast TX/RX switching. As a result, an energy consumption of 651pJ/bit is achieved.

Figure 5.1 shows a proposed RF and BB chipset. Short range, which is less than 5 cm, and high speed one-to-one wireless communication using 60 GHz band is suitable to secure file transfer application especially mobile devices. In order to realize such an application, small size, capability of a data retransmission and high power efficiency are required. The proposed chipset realizes data retransmission and low energy consumption by including a high efficient MAC with fast TX/RX switching. And the chipset is composed of easy mountable standard plastic BGA packages of approximately 1 mm thickness by adopting a bonding-wire-based in-package antenna [81].

Since the TX and the RX share the antenna as shown in Fig. 5.2, a TX/RX switch is integrated in the RF IC for frame exchange. The switching can be settled in a short time to realize high speed frame exchange. The RX of the RF IC consists of an LNA, an RX mixer with 40 GHz band LO, a QDEMOD at 20 GHz band IF and an LPF/VGA. The TX is composed of a quadrature modulator (QMOD), a TX mixer and a PA. An LO PLL adopting a 20 GHz quadrature VCO and a frequency

doubler is also integrated [80]. Differential circuitry is used in all circuit blocks including the antenna.

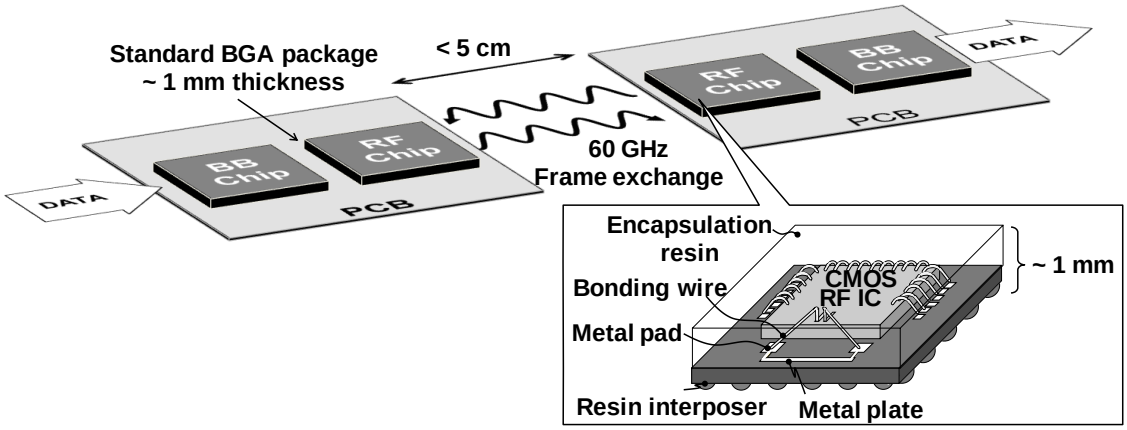


Figure 5.1: Short-range 60 GHz TRX chipset.

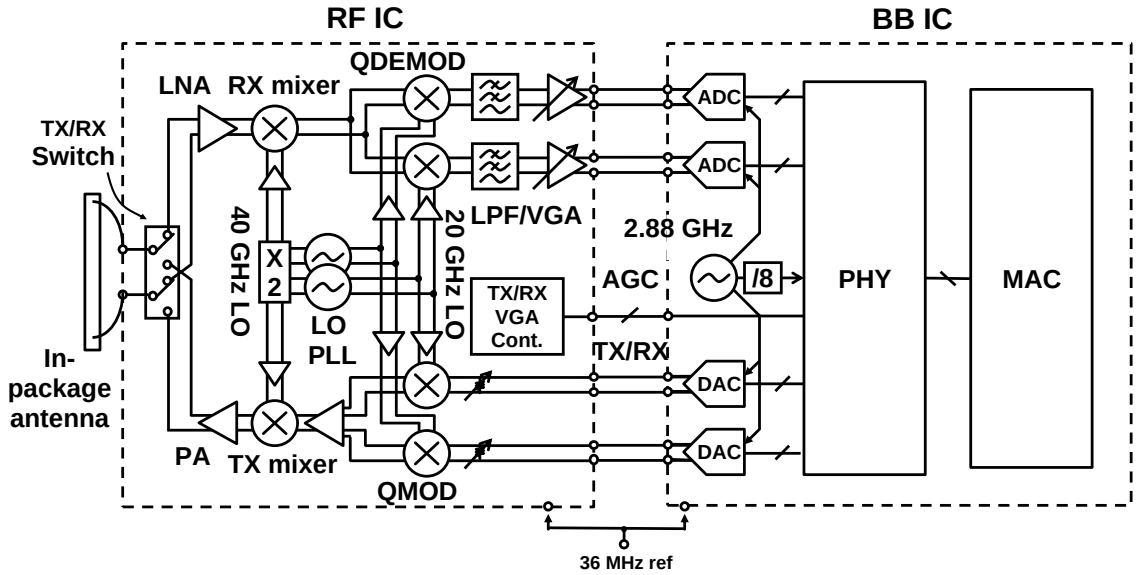


Figure 5.2: Chipset block diagram.

5.2 BB IC and Required RF IC Performance

Figure 5.3 shows a block diagram of the BB IC. The PHY layer employs OFDM-QPSK modulation, considering scalability to QAM under multipath fading channel. In addition, convolutional code and Reed-Solomon code are adopted for non-flatness of the RF IC and channel. The ADC/DAC sampling rate is 2.88 GHz and guard interval (GI) is set to 2.78 ns. In order to achieve maximum data rate of 2.67 Gb/s, 48 of 64 sub-carriers are assigned as data sub-carriers and none are assigned as pilot sub-carriers. The TX pre-emphasizes the 2.15 GHz band edge in the frequency domain to compensate frequency response of analog circuits. The RX applies an RSSI based AGC and a blind demodulation technique for the data symbols. Summary of the PHY block is shown in Table 5.1. The MAC layer employs Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA)-based protocol with retransmission mechanism using ACK as shown in a timing diagram of Fig. 5.4. According to the plot of a throughput against a Short Inter Frame Space (SIFS) between DATA and ACK frame as shown in Fig. 5.5, less than 3 μs SIFS is required to achieve 2 Gb/s throughput with approximately 80 % MAC efficiency. This means fast TX/RX switching of the RF IC is required. The ADC is based on a 5 bit flash architecture [82]. The DAC employs a 6 bit current steering circuit with the same delay buffer layout for high speed operation. The 2.88 GHz clock generator integrated in the same die is based on a sub-sampling PLL with ring oscillator.

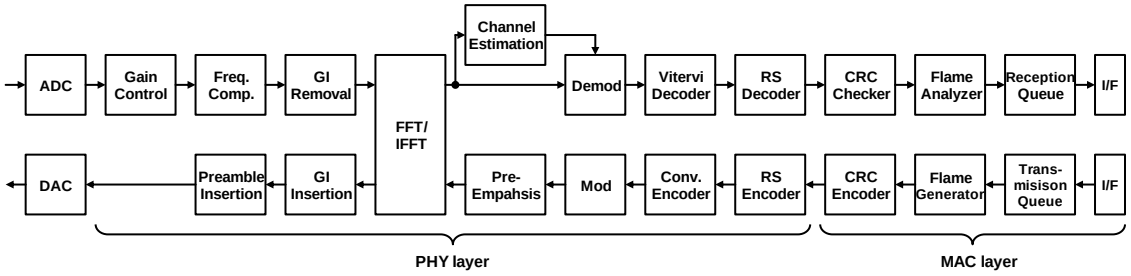


Figure 5.3: Digital block diagram.

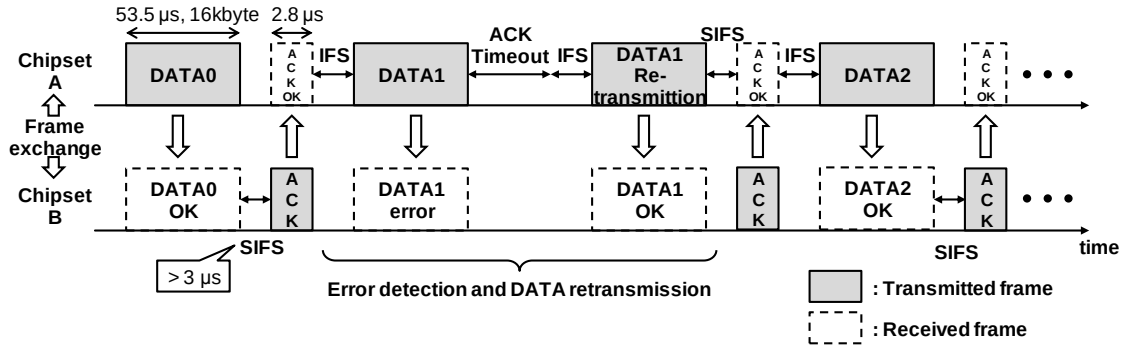


Figure 5.4: MAC sequence.

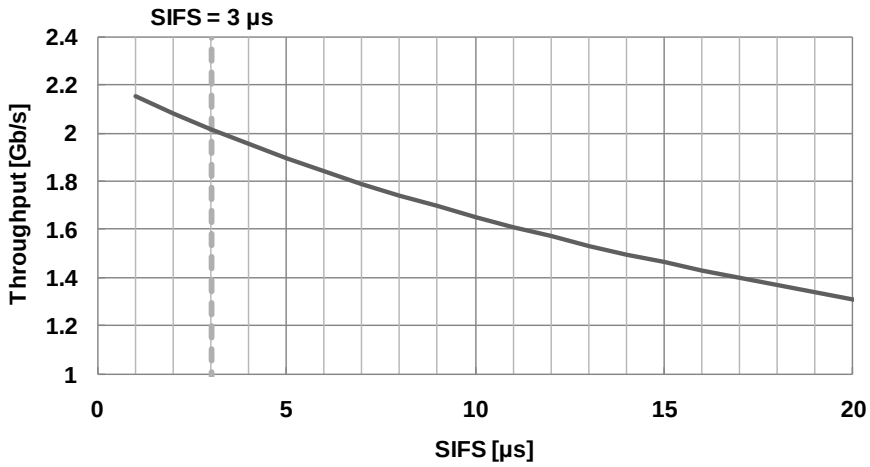


Figure 5.5: Relationship of short inter-frame space (SIFS) and throughput.

Table 5.1: Summary of the PHY.

Parameter	Value or Descrption
Carrier Modulation	OFDM
Data Modulation	QPSK
Outer FEC	Reed-Solomon Code (240,224)
Inner FEC	Convolutional Code R=3/4
ADC/DAC Sampling	2.88 [GHz]
FFT/IFFT points	64
Number of data subcarriers	48
Number of null subcarriers	16 (incl. one DC carrier)
Subcarrier Spacing	43.875 [MHz]
Guard Interval (GI)	2.78 [nsec] (8 points)

5.3 Design of RF Building Blocks

5.3.1 TX/RX Switch Circuit

As explained in the previous sections, TX/RX switching within 3 μs is required for achieving 2 Gb/s throughput with frame exchanging function. Therefore the RF IC employs RX/TX switch at 60 GHz band and fast settling PLL and analog base band circuit. Figure 5.6 Shows the TX/RX switch circuit. A transformer-based TX/RX switch is adopted for small area and low insertion loss compared to a conventional switch with λ/4 transmission line [83]. In the TX active mode, the NMOS switch and the PA turn on and the LNA turns off. Then the PA output nodes are coupled to antenna nodes. The transformer also works as a matching circuit for the PA and antenna. In addition, parasitic capacitance of the LNA input stage works as a compensation capacitance for leakage

inductance of the transformer. However the gate resistance of the LNA input transistor causes losses of the PA output signal, then a negative resistance is applied as shown in the Fig. 5.6. A common source transistor with capacitive degeneration is used for the negative resistance. At the RX mode, the PA and the NMOS switch turn off. The transformer is decoupled to the LNA by the NMOS switch. Then the LNA does not couple to the parasitic resistance which is included in the parasitic diode existing in the large transistor of the PA circuit which degrades noise figure. And the noise optimum matching is achieved by tuning the inductive matching circuit using the transformer. The transformer laid out in 45 μm diameter. The estimated TX loss including a reflection and an insertion/ohmic losses of the switch is 2.4 dB larger than that of the PA with individual output matching circuits at 60 GHz as shown in Fig. 5.7. And the estimated NF degradation compared to the LNA with an individual matching circuit to obtain is 1.5 dB as shown in Fig. 5.7.

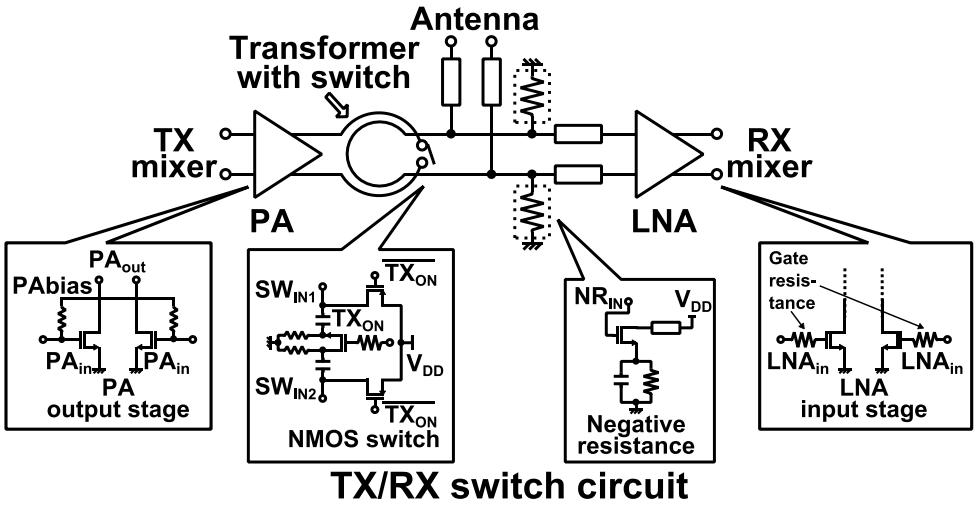


Figure 5.6: TX/RX switch circuit.

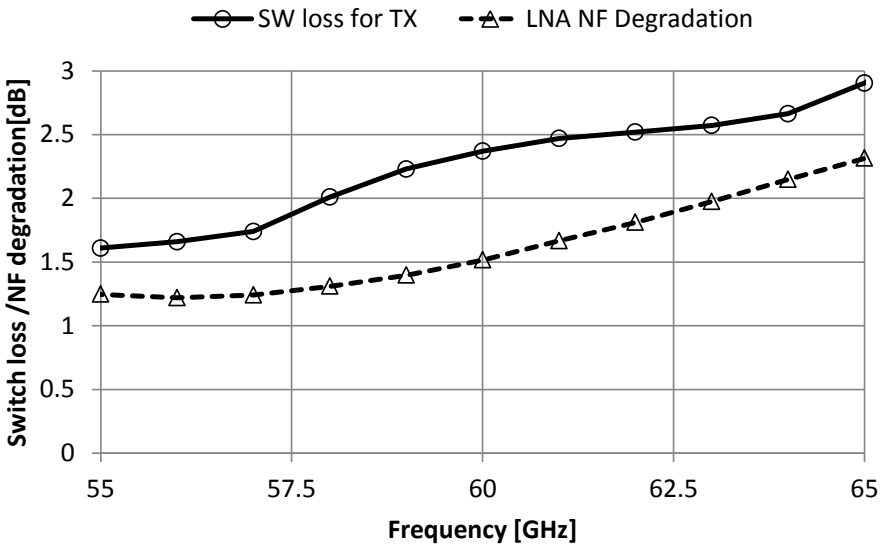


Figure 5.7: Simulated results of the TX/RX switch circuit.

5.3.2 Fast Settling PLL and LO distribution

Frequency fluctuation of the LO PLL at TX/RX switching operation degrades error vector magnitude of both transmitted and received signal. However, longer SIFS for waiting the TX/RX switching settling degrades the throughput as shown in Fig. 5.5. The frequency fluctuation is mainly caused by two reasons. The first reason is the rapid variation of the load of the VCO core circuit. Since the VCO output (LO) signal is connected to both the TX and RX mixer circuit, the load impedance of the VCO, which consists of parasitic gate capacitances of the mixer driving buffer circuit, is fluctuated by Miller capacitance and depletion capacitance variation when the TX/RX switching because these circuits turns on and off. The second reason is the supply voltage variation. Since the current consumption of the RF TX and RX is more than 100 mA, the supply voltage is fluctuated and also the voltage fluctuation couples to other supply line or circuit. In order to avoid these problems, the VCO of the PLL is isolated from fluctuating input capacitance of the TX/RX LO driver circuits by adopting a cascode isolation buffer that does not turn off at TX/RX switching. And a dedicated voltage supply is used for the PLL. The supply line is laid out far from the other supply line in order not to couple to the PLL power supply. The loop gain of the PLL can be tuned for optimizing for settling and phase noise, and fast locking mode is applied for fast channel change and power on.

A quadrature VCO (QVCO) is applied to generate a quadrature LO signal for quadrature modulation/demodulation. The output quadrature LO signal from the output buffer described above is distributed to the TX and RX QMOD and demodulator. About 700 μm of Equal length of transmission lines are applied to transmit the quadrature LO signal in order to suppress phase and amplitude mismatch. 40 GHz LO signal for upconversion and downconversion mixers is generated by a frequency doubler circuit based on a drain coupled circuitry. Although the 40 GHz LO signal is distributed by transmission line similar as quadrature LO signal, the line length is less than 1/5 of that of the 20 GHz LO distribution to avoid insertion loss of higher frequency LO signal.

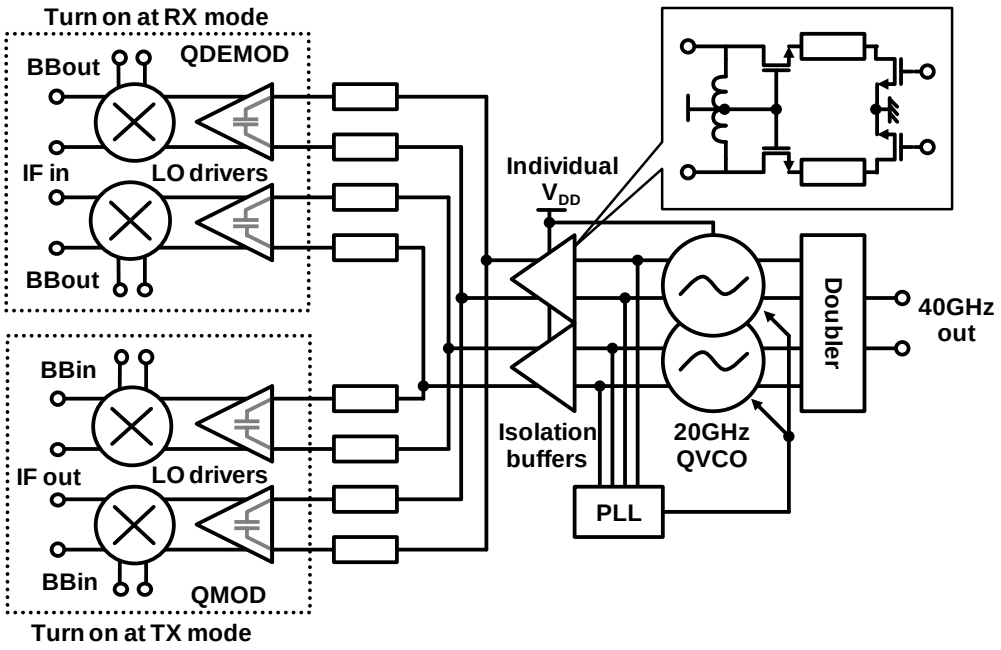


Figure 5.8: LO distribution.

5.3.3 LNA, Mixer and Other Circuits

The LNA is based on current reuse 3-stage amplifier [84] with gate to drain capacitance neutralization in order to achieve higher gain and to obtain optimum inter-stage matching. The RX mixer circuit for the RX is based on the double balanced topology, which uses 40 GHz band LO signal to output 20 GHz band IF signal. The mixer switching circuit applies the current boosting technique as shown in previous chapter to obtain the mixing function with lower LO swing voltage. However, the additional current bleeding source is required to achieve the function and the bled current degrades the efficiency of the mixer circuit. Figure 5.9: RX LNA and mixer circuit shows the LNA and the mixer circuit. An input stage of the mixer circuit is shared with the 3rd stage of the current-reuse LNA circuit. The bias current of the mixer switching stage which is controlled by common-mode feedback circuit with a replica of the LNA first stage is much less than that of mixer input/LNA 3rd stage. And the LNA first stage amplifier also works as a current bleeding source for the mixer switching stage. Therefore, there is no current waist because the bled current is used for amplification function. Measured individual LNA gain and NF are 16.5 dB and 5.3 dB at 60 GHz. A double balanced passive mixer is adopted to the QDEMOD circuit in order to save the current consumption of the RF IC.

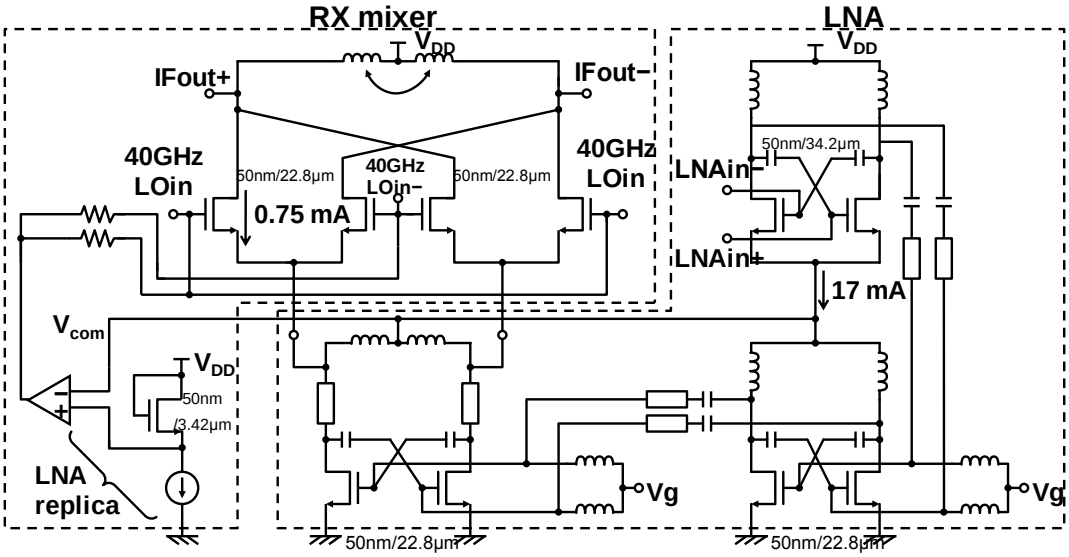


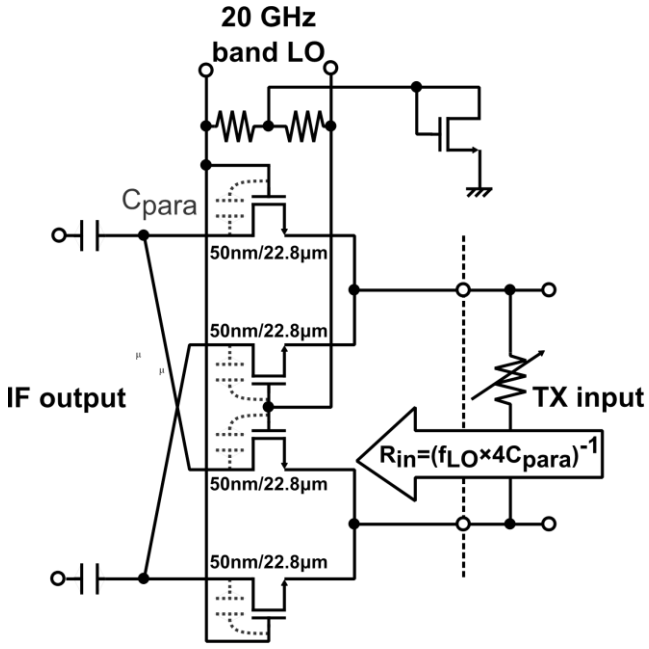
Figure 5.9: RX LNA and mixer circuit.

TX mixer chain as shown in Fig. 5.10 is similar to that of the RX. Passive mixer is applied to the QMOD to generate 20 GHz IF signal. The passive mixer and its parasitic capacitances work as a switched capacitor circuit to the BB input node as shown in Fig. 5.10(a). The input resistance (R_{in}) of the passive mixer is calculated as below

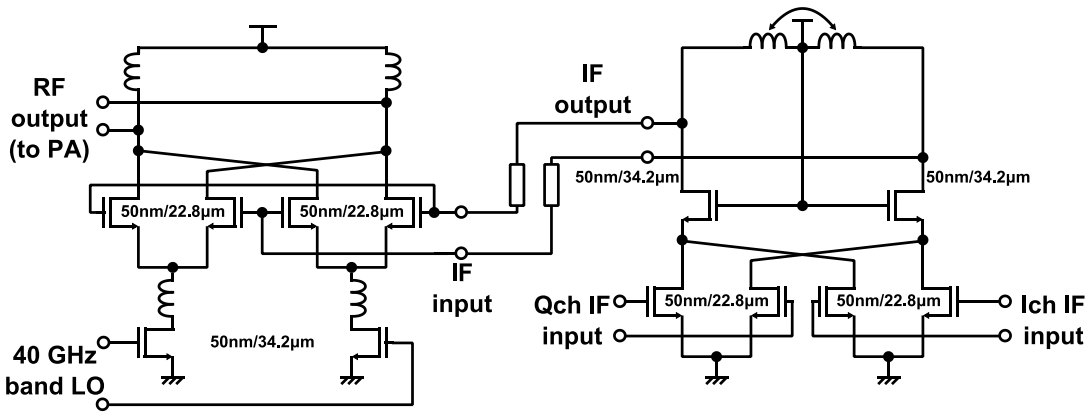
$$R_{in} = \left(f_{LO} \times 4C_{para}\right)^{-1}$$

f_{LO} is a LO frequency for the QMOD and C_{para} is whole parasitic capacitance of the passive mixer circuit viewed from BB input terminal. The value of the R_{in} is a few hundred ohms that is comparable to the desired TX input impedance of 100 Ω. Furthermore, the R_{in} varies with f_{LO} and C_{para} by channel switching and process variation. A variable resistance is applied at the input of the QMOD for keeping the input resistance under frequency and process variation to suppress an unexpected reflection and filter frequency characteristic variation. The quadrature output signal from the QMOD are combined by IF amplifier and up-converted to 60 GHz band by an active double-balanced mixer as shown in Fig. 5.10(b).

The RX LPF/VGA has 30 dB gain control range with 1 dB gain step [85] and 1.04 GHz cut off frequency adopting 3rd order Butterworth filter. DC offset cancellation with a fast settling mode is adopted for less than 2 μs AGC requirement. The PA is 3-stage current reuse amplifier and common source output stage with 10 dBm maximum output and 13.1 % PAE [84].



(a) Mixer circuit for QMOD.



(b) TX IF amplifier and RF mixer.

Figure 5.10: TX mixer circuit.

5.4 Measured Results

The RF and BB IC are fabricated in 65nm digital CMOS process. Figure 5.11 shows a chip micrograph of the RF IC. The RF IC's active area is 2.2 mm × 1.3 mm and the BB IC's whole die area is 3.4 mm × 3.9 mm as shown in Fig. 5.12. These ICs and antenna are packaged in 9 mm x 9mm, 201 pin standard BGA package. The in-package antenna is integrated in the RF IC's package as shown in Fig. 5.13.

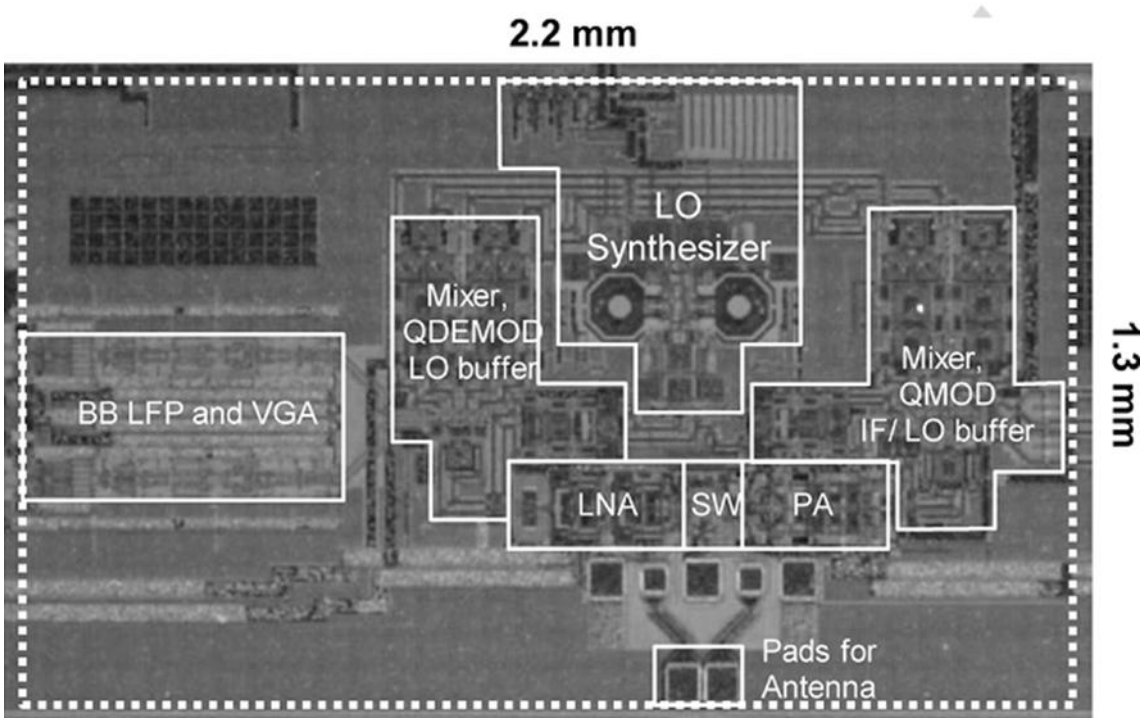


Figure 5.11: RF chip micrograph.

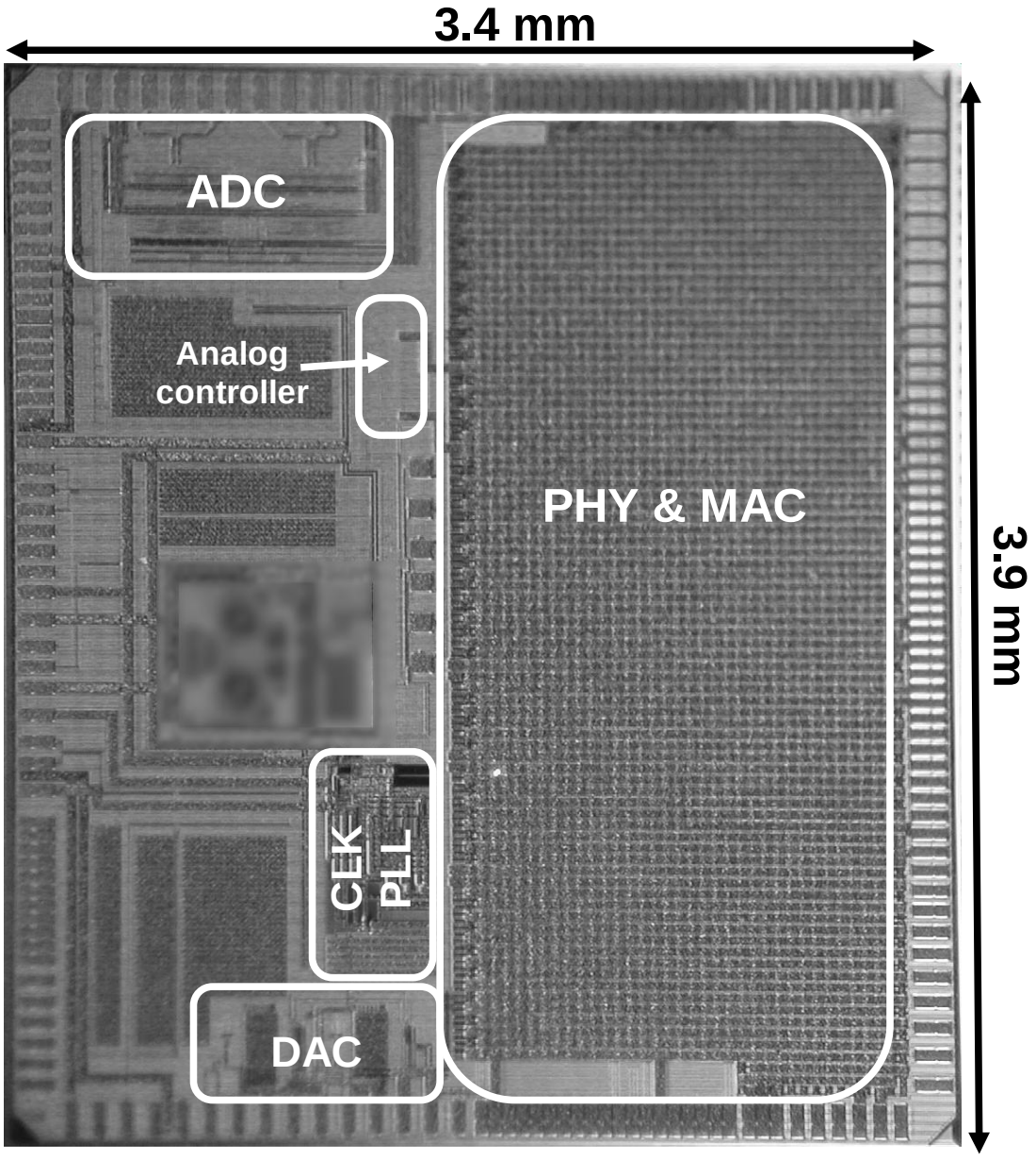


Figure 5.12: BB chip micrograph.

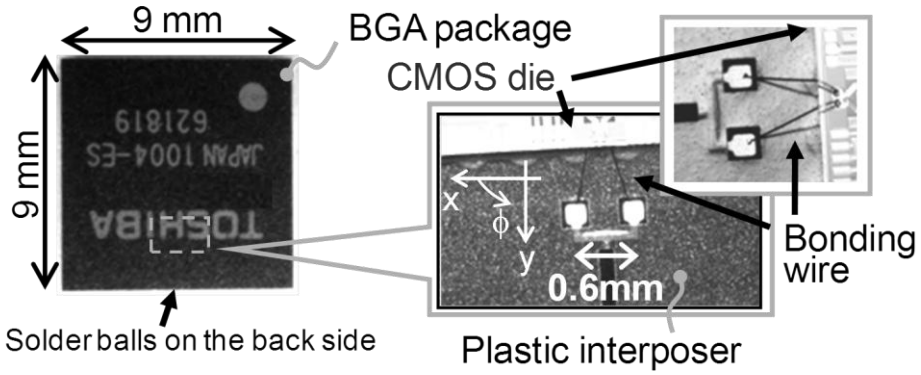


Figure 5.13: In-package antenna.

5.4.1 Measured Results of the RF IC

The performance of the RF IC is measured by using on-wafer probe for 60 GHz RF signal input/output without antenna. Figure 5.14 shows an RX gain characteristic at maximum baseband VGA gain. The RX operates from CH1 (58.32 GHz) to CH4 (64.8 GHz) and the maximum RX gain at CH1 and CH2 (60.48 GHz) is larger than 35 dB. The gain deviation excluding a baseband LPF in CH1 and CH2 is 2 dB and the lowest noise figure is 14 dB, which allow a signal to noise ratio for digital data demodulation. In addition, the frequency characteristic is able to be compensated by tuning matching circuits of RF blocks. Input 1 dB completion is -33 to -30 dBm for 4 channels and the average quadrature phase and amplitude error of 39 samples is 2.8 degree and 0.8 dB. Measured power consumption of the whole RX with an LO PLL is 233 mW at 1.2V supply including a 50 Ω output buffer (48 mW).

The measured TX output power and gain/frequency performance are shown as Fig. 5.15 and Fig. 5.16. The maximum output power of TX at CH2 is 6 dBm and output referred 1 dB gain suppression point is 2.6 dBm with quadrature sinusoidal signal input. And the small signal gain is 15 dB. TX quadrature error measured by using median image rejection ratio is 29 dB and the estimated phase and gain error, which is measured by manual quadrature I/Q tuning to the BB input signal, is 1.9 degree and 0.3 dB, respectively. Power consumption of the TX including the LO PLL with 1.2 V supply is 160 mW.

From the measured phase noise of the 20 GHz PLL, the estimated phase noise of the RF IC is -89 dBc at 1 MHz offset. Measured performance of the RF IC is summarized in

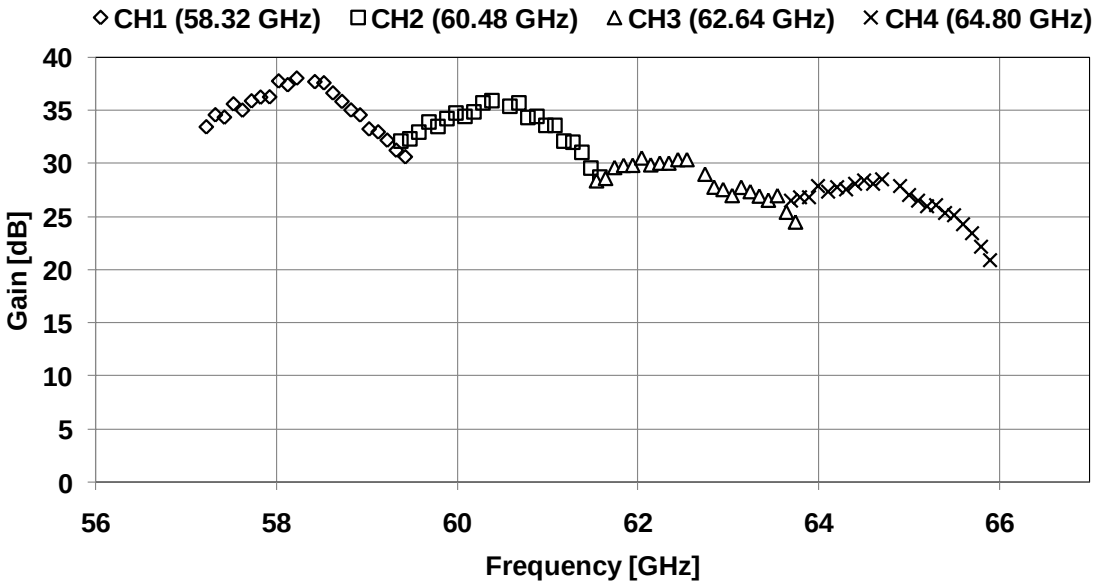


Figure 5.14: RX gain characteristic.

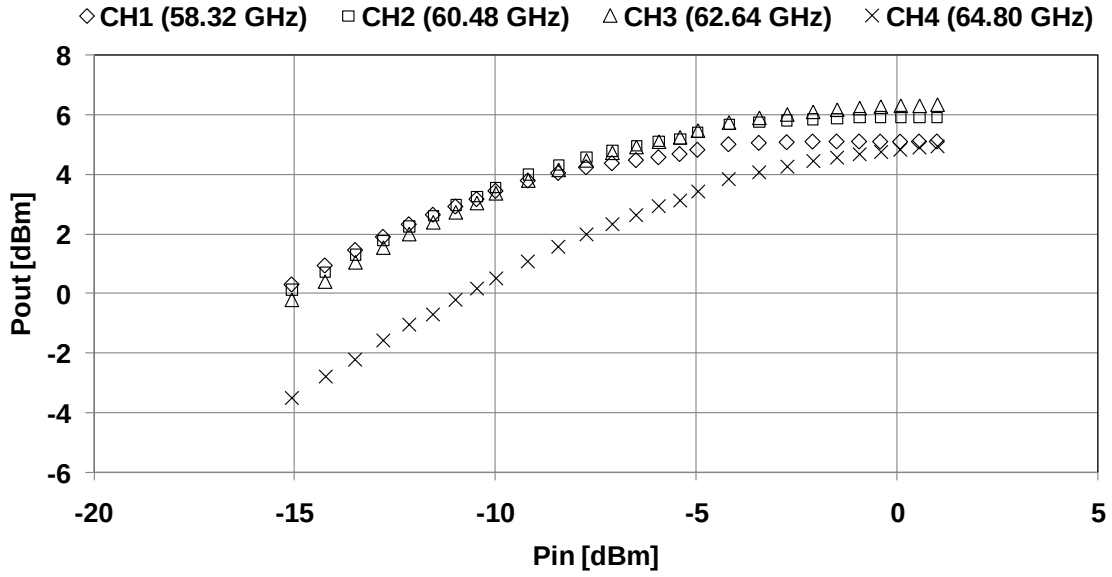


Figure 5.15: TX output power

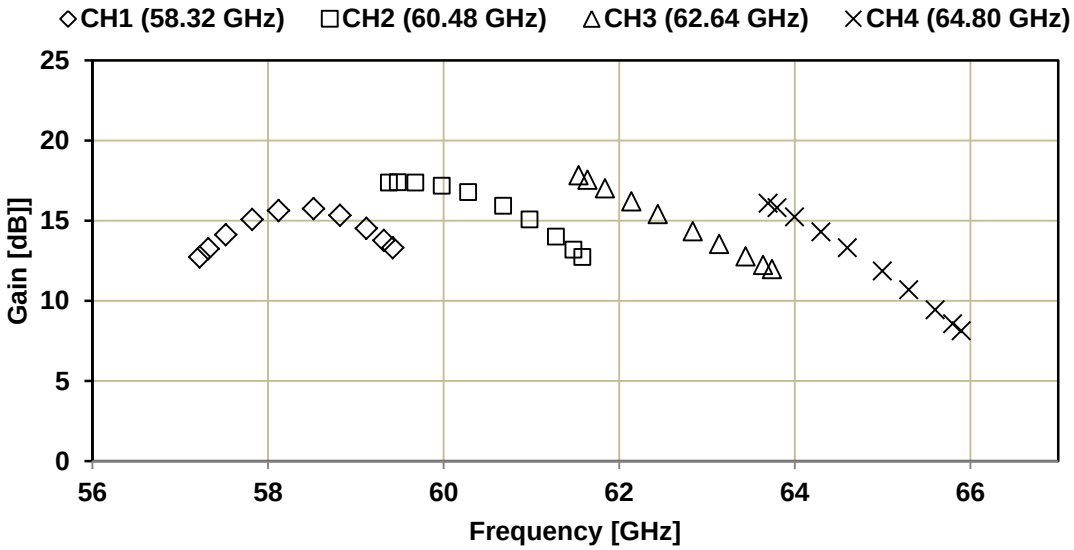


Figure 5.16: TX gain characteristic.

5.4.2 Throughput Measurement

Figure 5.17 shows a measurement setup for data transfer. The RF chip and BB chip are mounted on PCBs and connected via baseband I/Q input/output signals and control signals of AGC and TX/RX switching. 2 chipsets are used for data TX (chipset A) and RX (chipset B) respectively. The RF chips are placed several cm apart and CH2 is used for the measurement.

The PHY data rate is measured in one-way mode without TX/RX switching. The measured data rate is 2.62 Gb/s up to 4 cm distance including packet error. Throughput with MAC and DATA/ACK frame exchange using RF TX/RX switching was also measured. In order to measure frame exchange between both chipsets, a part of 60 GHz transmitted DATA and ACK frame is detected by external horn antenna. The picked-up signal is amplified and mixed down to lower frequency by external components, and then input to an oscilloscope to measure time-domain signal. Fig. 5 shows a measured waveform of frame exchange. DATA frames from chipset A and an ACK frame from chipset B appear in the expanded plot. After the DATA frame from chipset A, an ACK frame transmitted from chipset B appears with 2.45 μs of SIFS. And the IFS from an ACK frame to a next DATA frame is 3.40 μs. These results are achieved by fast switching of RF TRXs. 503 packet (8 Mbyte) data transfer is completed with 3 times retransmission by MAC layer with Cyclic Redundancy Check (CRC) in 31.6ms. The result shows 2.07 Gb/s throughput is achieved by the chipsets.

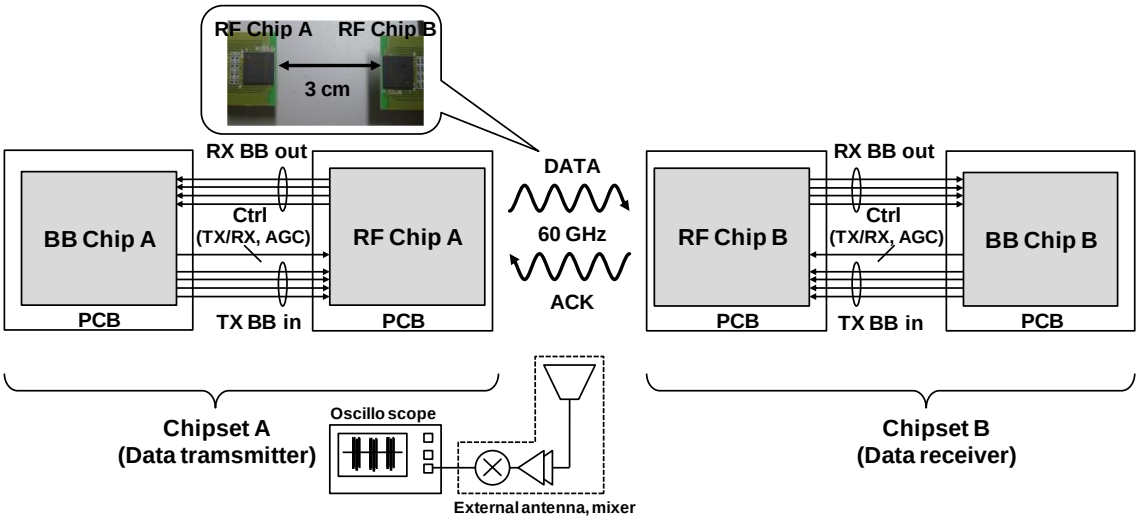


Figure 5.17: Data rate/throughput measurement setup.

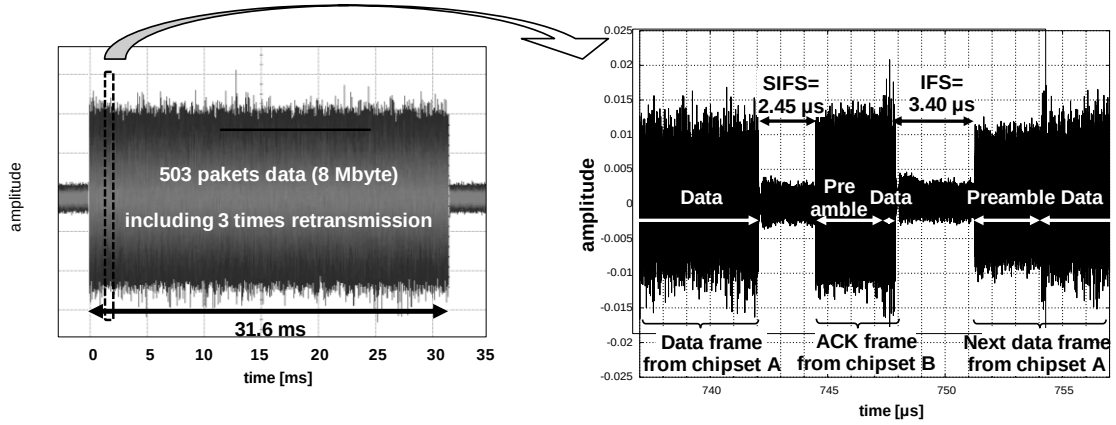


Figure 5.18: Measured result of throughput.

5.5 Comparison and Summary

Table 5.2 is a comparison of the power consumption of the LNA and mixer circuit of 60 GHz band [79], [80], [89], [78]. The smallest power consumption can be achieved the proposed circuit based on compensation method using analog circuits. The chipset achieves 2.62Gb/s data rate, 2.07Gb/s throughput and energy consumption of 651pJ/bit by high efficiency MAC using short interval frame exchange with fast RF TX/RX switching. The proposed high-frequency circuits using analog circuit are suitable for small and low-cost RF front-end modules.

Table 5.3 shows a performance summary of the chipset and comparison. The energy consumption of the TRX is calculated by throughput divided by whole power consumption of the chipset, which is the summation of data TX and data RX. The proposed chipset achieves an energy consumption of

729 pJ/bit. This value is much less than those of other previous TRXs including MAC layer [86]-[88], as shown in Table 5.4. Such a value is achieved by the fast throughput by using 60 GHz and lower power consumption by using a short range wireless system, respectively. And the chipset is the first solution of 60 GHz TRX including from an antenna to MAC layer in standard BGA packages.

Table 5.2: Power consumption of the LNA and mixer circuit of 60 GHz band.

Referece	LNA [mW]	MIX [mW]	Total [mW]
JSSC'09 [74]	18	51.6	69.6
JSSC'11 [78]	74		74
JSSC'11 [87]	18	33	51
JSSC'12 [76]	20.7	60.8	81.5
This work	19.4	20.9	40.3

Table 5.3: Summary of measured results.

RX RF at CH2		
Voltage gain	[dB]	35
Minimum DSB NF	[dB]	14
I/Q phase error	[deg]	3
I/Q amplitude error	[dB]	0.7
Power consumption	[mW]	233
Input 1 dB compression (@Max Gain)	[dBm]	-33
TX RF at CH2		
Power gain	[dB]	15
P1dB output	[dBm]	2.6
Saturation output	[dBm]	6
Image rejection ratio	[dB]	28
Power consumption	[mW]	160
Phase noise (1MHz offset)	[dBc]	-89

RF IC power consumption		
LNA	[mW]	19.3
Mixer/QDEMOD/LO Buf.	[mW]	23.5
LPF/VGA	[mW]	72.8
BB output buffer	[mW]	48.0
QMOD/Mixer/LO Buf.	[mW]	34.2
PA/TRX switch	[mW]	68.4
LO PLL	[mW]	63.4

Table 5.3 (Cont' d): Summary of measured results.

BB Block		
Clock PLL Power (TRX)	[mW]	66
ADC Power (RX)	[mW]	137
PHY+MAC Pow. (RX)	[mW]	320
DAC Power (TX)	[mW]	83
PHY+MAC Pow. (TX)	[mW]	283

Chipset power counsumption		
Total Power (RX)	[mW]	756
Total Power (TX)	[mW]	592

Data transfer performance		
Max distance	[cm]	4
PHY data rate	[Gb/s]	2.62
Throughput w/ MAC	[Gb/s]	2.07

*Data rate and throughput was measured at 3 cm.

Table 5.4: Comparison with other wireless applications.

Comparison of TRX including MAC layer				
	System	TRX Total Power [mW]	Throughput [Mb/s]	Energy/bit [pJ/bit]*
[94]	802.11n	1312	311	4220
[95], [96]	UWB	747	378	1976
[97]	UWB	290	27.2	10636
This work	60 GHz	1348	2070	651
Comparison of 60 GHz TRX in CMOS				
	Package	Antenna	RF	BB Digital
[86]	BGA with Waveguide	Waveguide Antenna	TRX	PHY
[67]	N/A	N/A	TRX	N/A*
[88]	HTCC Package	Dipole Antenna on HTCC	TRX	N/A
This work	Standard BGA	Bonding Wire Antenna	TRX	PHY/MAC

Chapter 6

A 77-GHz TRX for FMCW Radar Applications

In this chapter, a 77 GHz frequency modulated continuous wave (FMCW) radar TRX IC with an FMCW chirp signal generator has been presented for a case of very high-frequency TRX with insufficient performance of the integrated devices. In the case of FMCW radar system in such a high-frequency oscillation, chirp nonlinearity of the frequency chirping generator based on DDFS degrades the performance of the whole radar system. A proposed FMCW signal generator at 77 GHz band adopting a compensation technique using analog circuits is substantiated.

6.1 Introduction

A 77 GHz radar application is suitable for measuring distance for various purposes owing to its narrow beam radius. In order to realize consumer radar/ranging applications for Intelligent Transportation System (ITS), a low-cost 77 GHz TRX is desired. A TRX using low-cost standard CMOS process instead of compound semiconductor or Si-Ge BiCMOS process is expected to be one of solutions capable of satisfying this demand in view of its suitability for high integration such as system-on-a-chip and the possibility of 77 GHz TRX in CMOS technologies is shown in recent research [90]−[92].

There are several ranging methods such as a pulse-radar, UWB radar and a frequency modulated continuous-wave (FMCW) radar [93], [94], [95]. Pulse radar and UWB radar require high peak-to-average power ratio (PAPR) or wideband operation to output short pulse signal or wideband spread spectrum signal. It is serious issue to manage with CMOS technology because the CMOS, unlike a compound semiconductor or a Si-Ge BiCMOS process, cannot be applied high supply voltage for obtaining high-power output signal and also it has lower maximum available gain (MAG) at millimeter-wave band for achieving wideband operation. On the other hand, the FMCW radars, that use only frequency modulation, require lower PAPR and moderate bandwidth than those required by other ranging methods. Therefore, the FMCW radar is a possible candidate for realizing a CMOS radar IC.

Figure 6.1 shows an FMCW radar TRX. An FMCW signal whose frequency is modulated in a triangular shape with time is generated by an FMCW signal generator. A TX amplifies the FMCW signal and radiates the signal via a TX antenna. Then, the radiated signal reaches the target located at a distance *R* from the TRX and the target reflects a portion of the signal back to the radar TRX. The reflected signal is input to the RX via an RX antenna. The received signal is amplified and mixed with a local oscillation (LO) signal generated from the same FMCW generator used for the TX. Since the round-trip time of flight (TOF) of the signal is 2*R*/c, where c is the speed of light, the frequency difference between the received signal and the LO signal, which results in the frequency of the mixer output (f_{beat}), is related to the TOF (Fig. 6.1). Then, the distance can be obtained by frequency detection such as a fast Fourier transform (fft). Since the frequency difference is determined by a frequency chirp ratio of the FMCW signal, a highly linear frequency chirp is required to avoid degradation of ranging accuracy [94].

The first 77 GHz FMCW radar TRX IC fabricated in 90 nm CMOS process that applies a phase-locked-loop (PLL)-based linear FMCW generator is presented. This paper is organized as follows. Section II identifies design issues concerning realization of linear FMCW signal in CMOS IC and shows a proposed low-cost and low-power-consumption FMCW generator and results of numerical analysis. The design of the developed 77 GHz RX and TX is presented in Section III, which is followed by the presentation of TRX measured results in Section IV. Conclusions are presented in Section V, the final section of this paper.

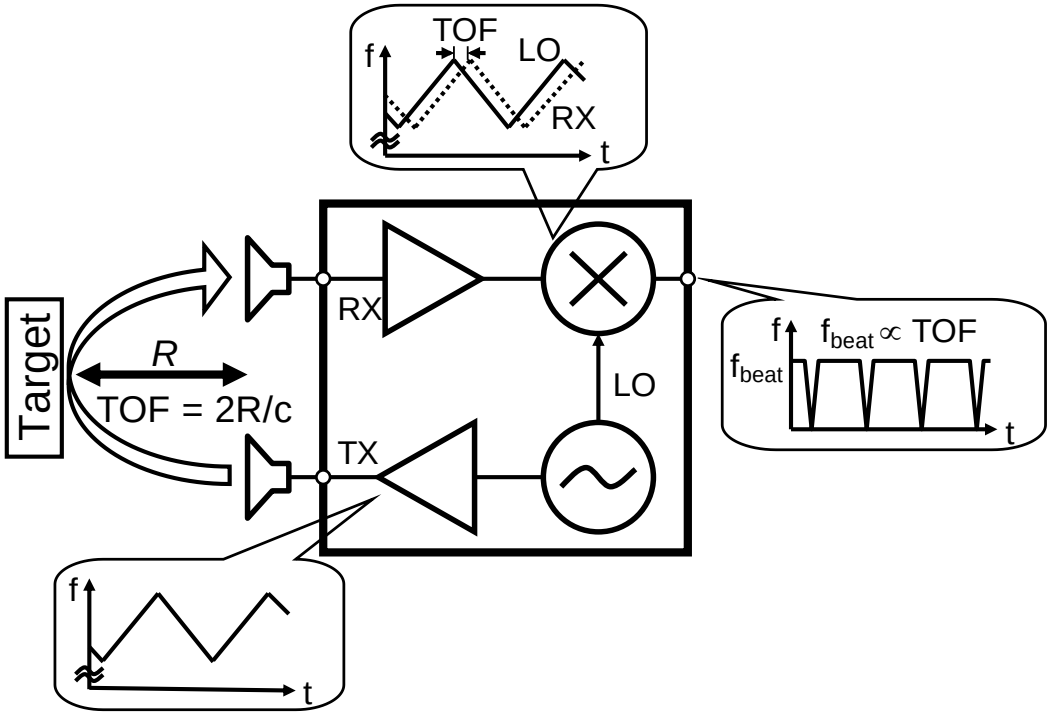


Figure 6.1: FMCW radar TRX.

6.2 77-GHz FMCW Signal Generator

6.2.1 Issues concerning a CMOS IC for FMCW TRXs

In general, a 77 GHz voltage-controlled-oscillator (VCO) in CMOS is nonlinear with respect to the input frequency control signal owing to nonlinear devices such as a varactor diode of the VCO. A look-up table-based nonlinearity compensator for the VCO achieves linear frequency sweep. However the look-up table should be refreshed for the frequency drift with a temperature variation or other disturbance and the method cannot compensate fast frequency variation caused by unwanted load variation or disturbance. Delay line-based compensator generates linear frequency sweep by picking up the frequency variation ratio using a delay line and a mixer [96]. However, long delay line, which is hard to integrate in CMOS IC, is needed.

In the CMOS 77 GHz radar TRX, the PLL-based FMCW signal generator is used because a PLL can compensate the VCO nonlinearity by its feedback manner. A PLL using low frequency and accurate chirp FMCW reference signal generated by a direct digital frequency synthesizer (DDFS) is suitable for CMOS because the DDFS can be integrated in CMOS IC [97], [98]. Figure 6.2 shows the block diagram of the PLL-based FMCW generator. Phase frequency detector (PFD) detects the phase/frequency difference between the output signal and reference signal, charge pump (CP) outputs source and drain current according to the polarity of the output of the PFD, the loop filter (LF) filters out the high-frequency components and divider (DIV) output the frequency divided signal of the VCO output. The nonlinearity of the CMOS VCO is compensated by locking with an accurate frequency reference signal from the DDFS.

The frequency chirp of the reference signal has discrete stair-like shape. Required performances of the DDFS, such as clock frequency (f_{clk}) and frequency control word length (W) corresponding to the phase resolution, can be determined by the refresh time of the frequency variation and the minimum frequency step. Fiure 6.3 shows a specification of the FMCW frequency chirp. In the case that the required ranging accuracy is 1 m, which corresponds to the TOF of 6.7 ns, the output frequency should change in 6.7 ns and the frequency variation in this time is 16 kHz. With regard to the reference signal, the DDFS should also change the output frequency in 6.7 ns. Hence, the minimum f_{clk} should be higher than 150 MHz. And this means the maximum output frequency of the DDFS is 75 MHz, which is equal to the Nyquist frequency of the f_{clk}. In order to divide the 77 GHz output signal into 75 MHz reference frequency, the division number of the PLL is assumed to be 1024. This results in the required frequency resolution for the DDFS of less than 16 Hz.

Since the frequency resolution of the DDFS is determined by $f_{clk}/2^W$, both 150 MHz f_{clk} and 24 bit W are needed for the FMCW frequency reference signal for the PLL. Such a high-speed and high-resolution DDFS requires high-power consumption over 100 mW and 1 mm^2 area including

DAC for DDFS output [99], [100]. Thus, a PLL that generates a linear FMCW signal even using a rough and low-resolution discrete stair-like frequency reference signal generated from low-spec DDFS that can be easily achieved in CMOS is desired to realize low-cost FMCW TRX for commercial radar applications.

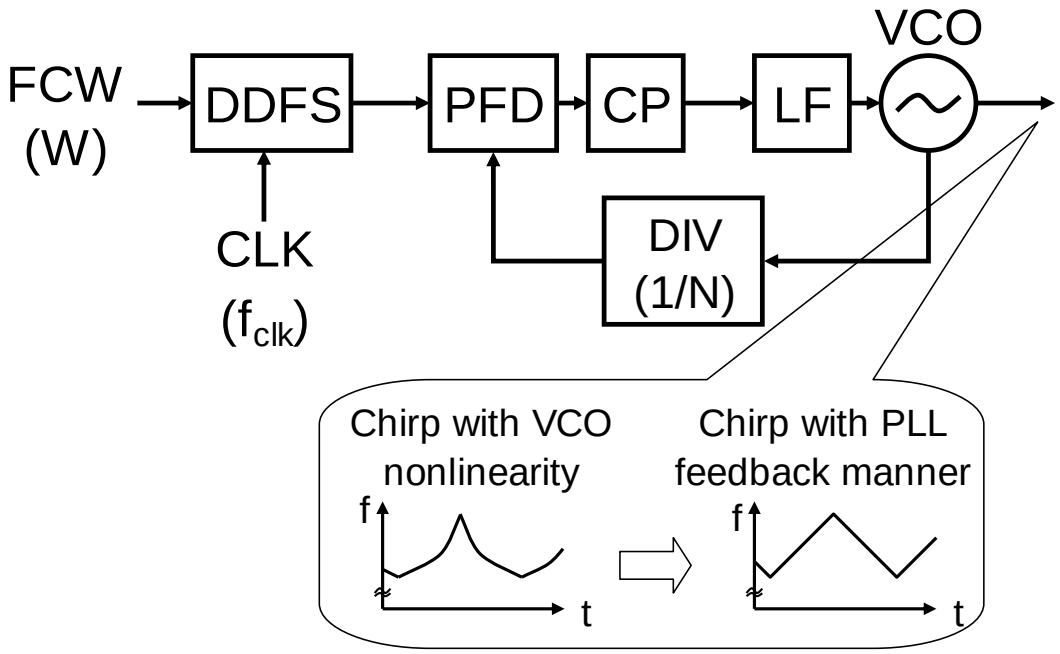


Figure 6.2: Chirp linearization using a PLL with DDFS frequency reference.

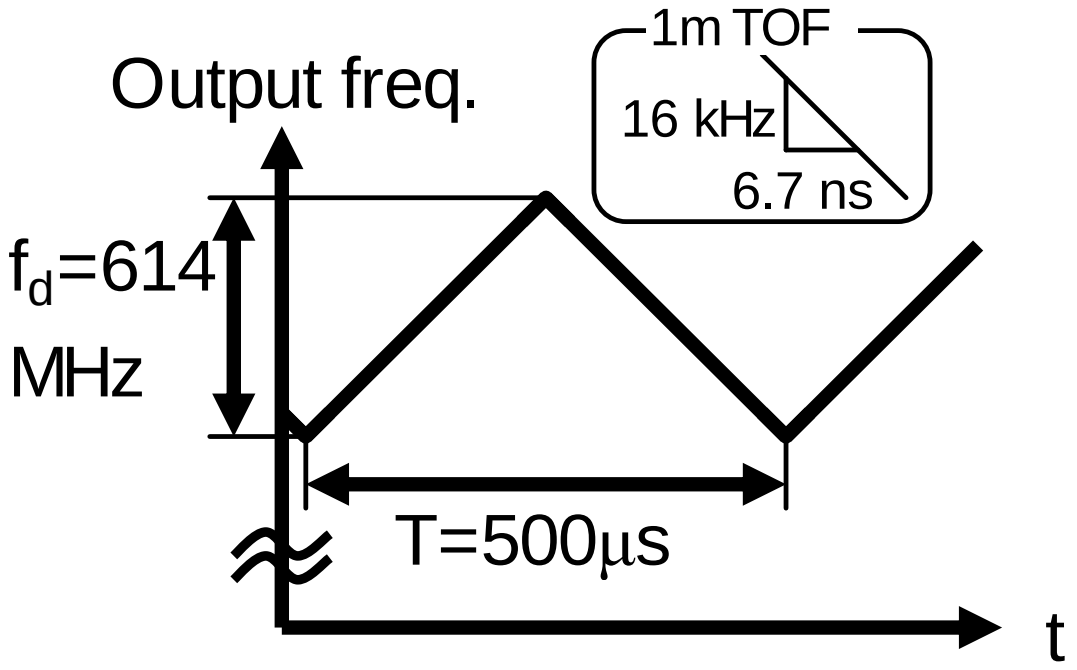


Figure 6.3: Specification of an FMCW output frequency.

6.2.2 Design of a CMOS FMCW gGenerator

Figure 6.4 shows the proposed PLL for the FMCW radar. Rough stair-like time-domain frequency variation from the low-spec DDFS is converted to the time-domain voltage variation at the output of the charge pump of the PLL. Therefore, the low-pass loop filter (LF) can smooth the stair-like voltage variation, and the non-stair-like voltage signal is supplied to the VCO. Then, the output frequency variation of the PLL is smoothed into linear chirp. As shown in Fig. 6.4, a cut-off frequency of the PLL transfer function (f_{PLL}) should be lower than $1/\Delta t$, which is the refresh rate of the low-spec DDFS, to suppress the spurs at $1/\Delta t$ that cause sinusoidal nonlinear frequency chirp at the output. The f_{PLL} should also be much higher than $1/T$ to create a triangular shape for FMCW signal. Therefore, a linear FMCW chirp signal can be generated by satisfying the inequality, $1/T << f_{PLL} < 1/\Delta t$. For further relaxation of f_{clk} and W of the DDFS, the reference signal is generated from a single-sideband mixer and a CW signal generator (crystal oscillator) as shown in Fig. 6.4.

The output chirp linearity of the proposed PLL with low-spec DDFS for the frequency reference signal is estimated by using the parameters shown in Table I. Such a low-speed (1.2 MHz) and low-resolution (8bit) DDFS consumes less than 1/10 power than that shown in section II-A. The transfer function of the actual designed PLL calculated from parameters of VCO gain, LF characteristics, CP current and division number of DIV is shown in Fig. 6.5. The frequency component corresponding to the $1/\Delta t$ is suppressed by 30 dB and the $1/T$ is not suppressed by the PLL. The calculated output chirp of the PLL is shown in Fig. 6.6. Though the chirp overshoots at the turning point of the triangular shape, the transition time is not long and the time can be neglected at the received signal processing. The output frequency error of the chirp is shown in Fig. 6.7. The chirp has sinusoidal nonlinearity whose error amplitude is 40 kHz at 77 GHz output. An FMCW radar output signal that has sinusoidal nonlinearity is:

$$s_b(t) = c_0 \cos 2\pi \left[\begin{array}{l} \left(f_c + \frac{f_d}{2} \right) TOF + \frac{f_d}{2T} (TOF)^2 - \frac{f_d}{T} TOFt \\ + \frac{A_n \Delta t}{2\pi} \left\{ \cos 2\pi \Delta t^{-1} (t - TOF) - \cos 2\pi \Delta t^{-1} t \right\} \end{array} \right] \tag{6.1}$$

where c_0 is the amplitude of beat signal, f_c is the carrier frequency of the FMCW signal, f_d is the frequency deviation of the chirp and A_n is the magnitude of the sinusoidal nonlinearity which equals to the peak value of the spurs at $1/\Delta t$ [94]. Figure 6.8(a) shows the calculated radar output signal using equation (5.1) for a target at 10 m. The spurs that appear at $f_{beat} \pm 1/\Delta t$ are suppressed to 40 dB lower than desired beat signal at f_{beat}. The ranging resolution, standard deviation ($\sigma_{\delta R}$), is also calculated from sinusoidal nonlinearity magnitude as [101]:

$$\sigma_{\delta R} \approx \frac{\sqrt{2} A_n 1/\Delta t}{f_d / T \cdot c} R \tag{6.2}$$

The result shows 46 cm resolution can be obtained for R = 100 m. If the PLL does not have a smoothing function, the output chirp has very large, 3 MHz, error magnitude and the radar output signal for the same target becomes as shown in Fig. 6.8(b). The spurs are 30 dB larger than the previous case and the resolution is much more degraded.

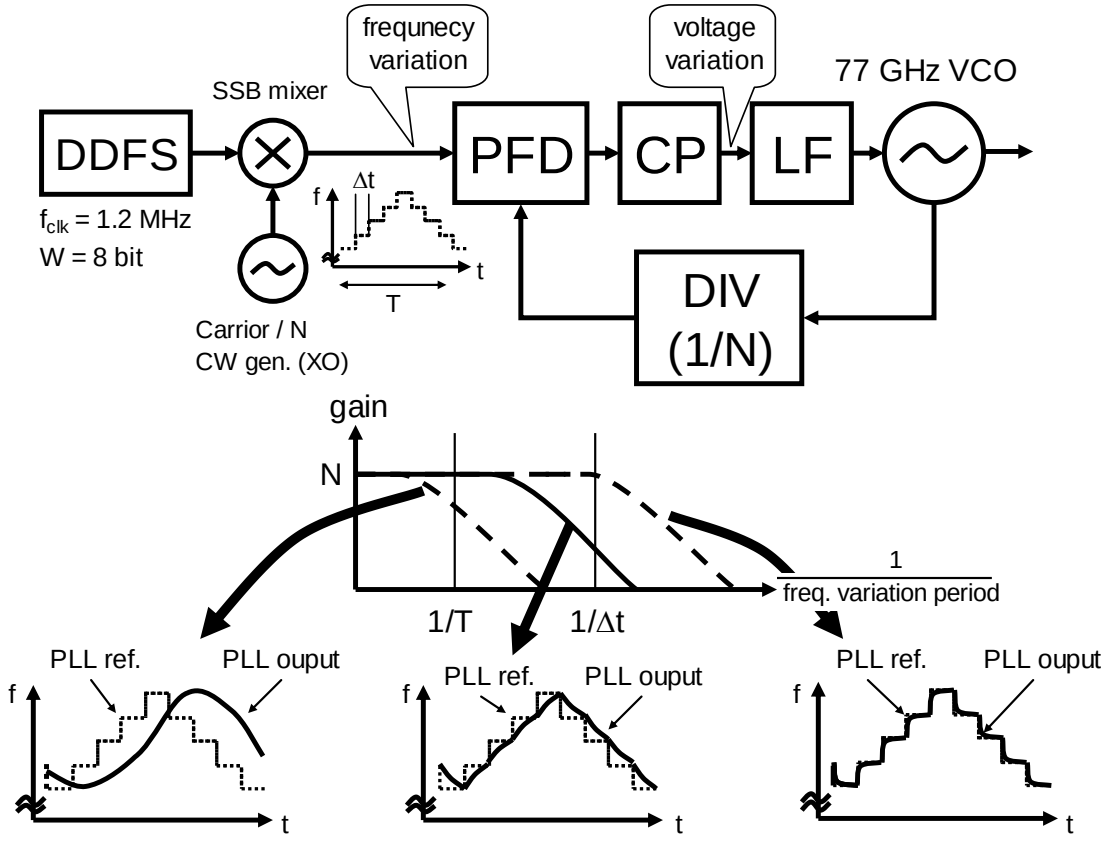
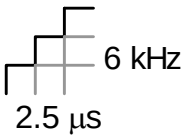


Figure 6.4: Block diagram of the proposed PLL-based FMCW generator.

Table 6.1

DDFS specification			
fclk	W	Δt	Freq. variation in Δt
1.2 MHz	8 bit	2.5 μs	6 kHz



PLL specification					
LF type	LF capacitance	LF resistance	CP current	VCO Kv	N
Rag-filter	200 pF	15 kΩ	160 μA	1 GHz/V	1024

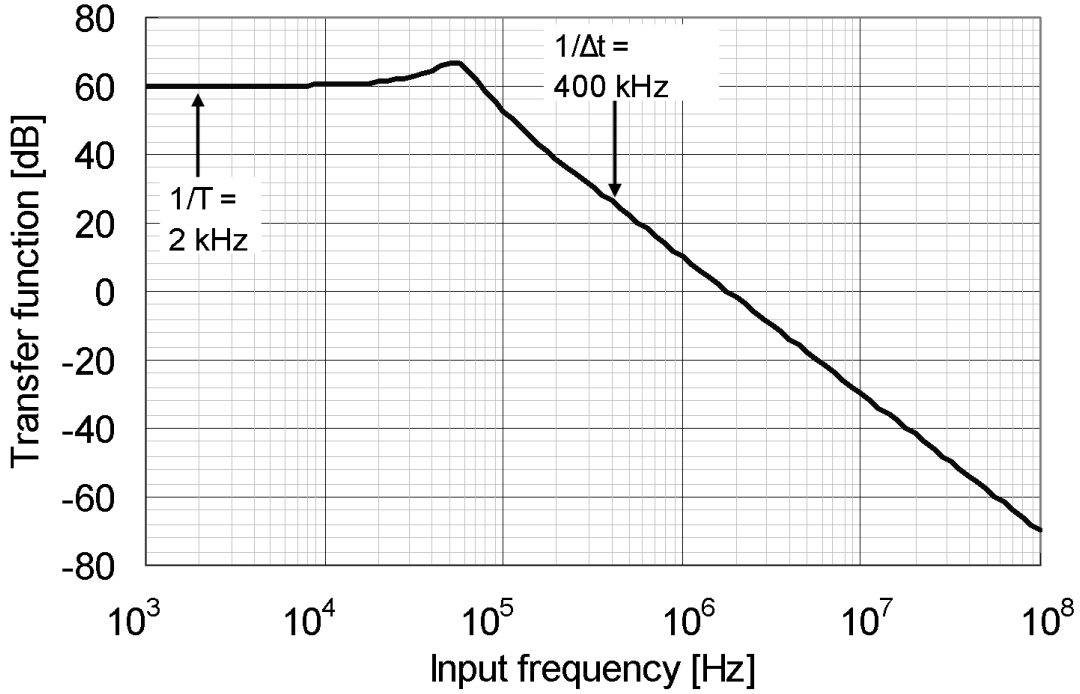


Figure 6.5: Calculated transfer function of the PLL.

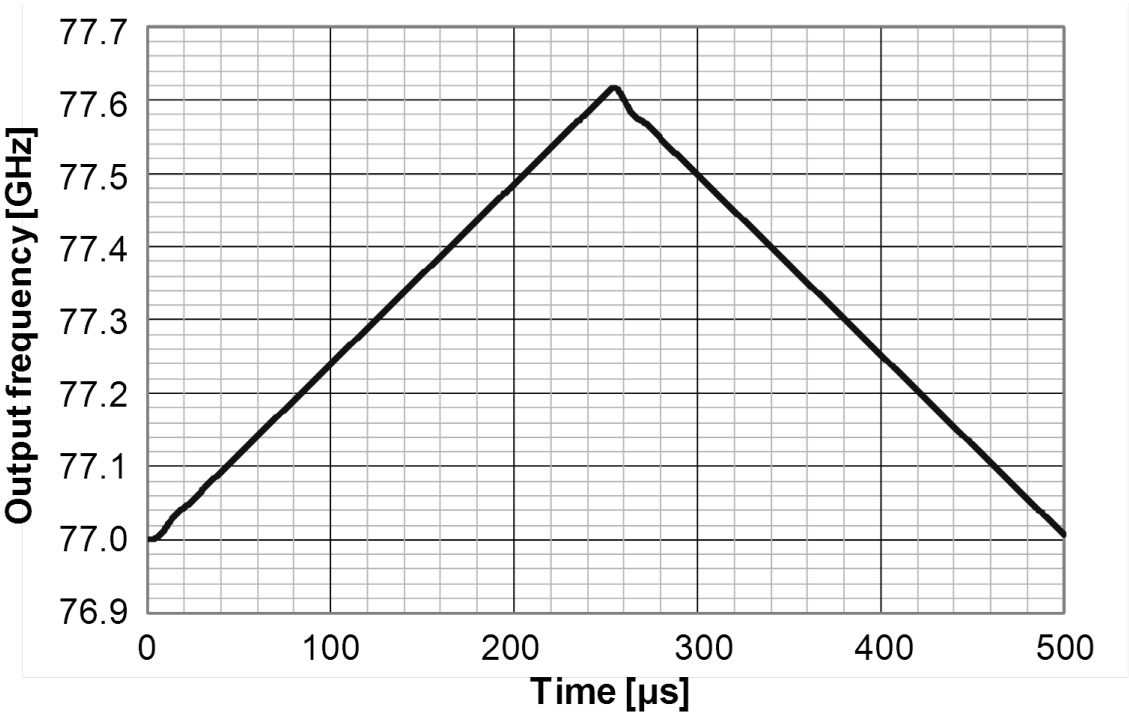


Figure 6.6: Calculated FMCW output chirp of the proposed FMCW generator with low-spec DDFS.

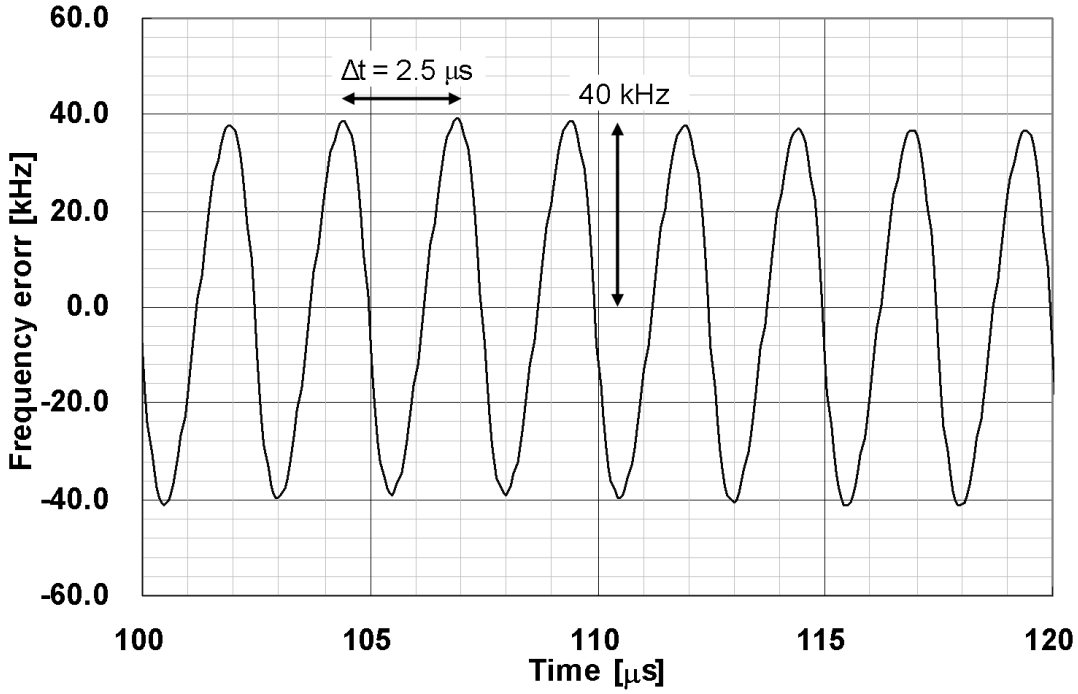
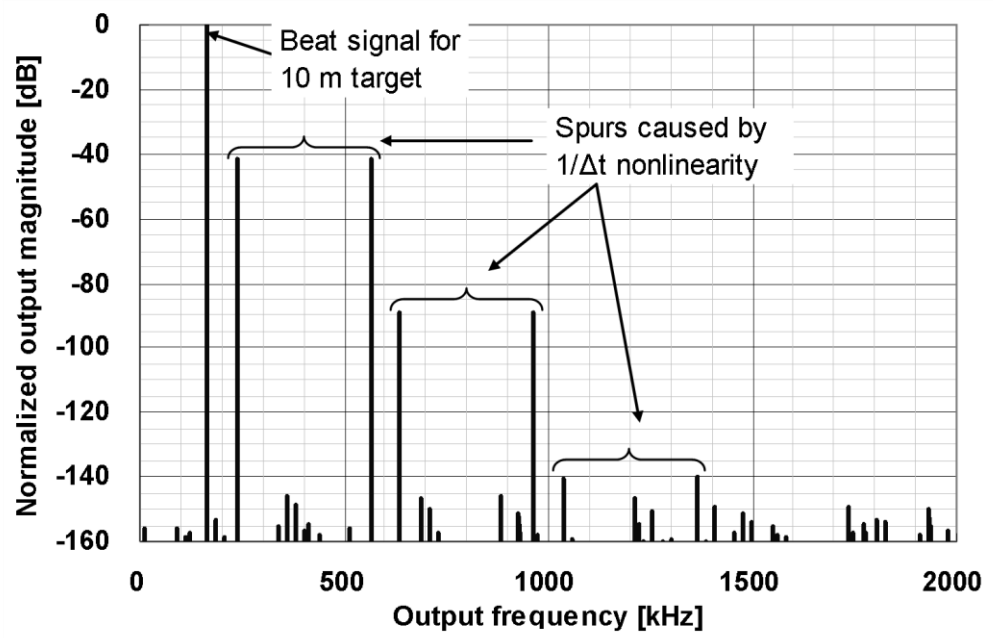
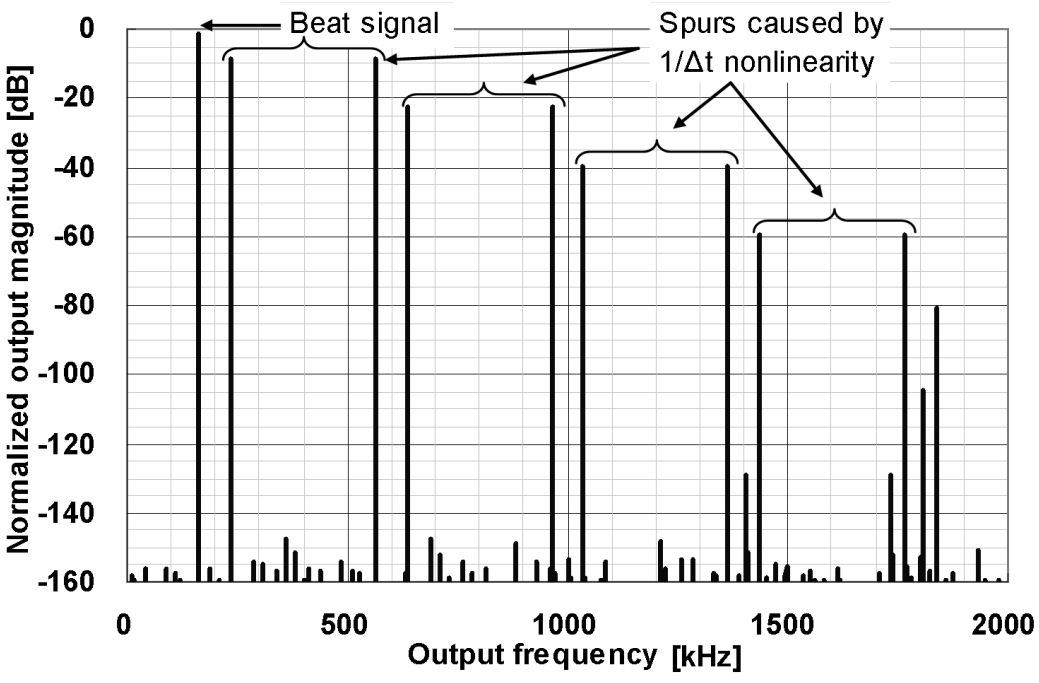


Figure 6.7: Calculated frequency error of the proposed FMCW generator with 1.2 MHz, 8bit DDFS for the frequency reference.



(a)



(b)

Figure 6.8: Calculated radar output spectrum for a target located 10m using the proposed FMCW generator with smoothing function (a) and that of without smoothing function (b).

6.3 TRX Building Blocks

The RX consists of an LNA, a down-conversion mixer and an output transimpedance and buffer amplifier as shown in Fig. 6.9.

An LNA is needed to have sufficient gain for the RX. However, NMOS transistors which we used have MAG of about 4 to 5 dB at 77 GHz, which is not sufficient to achieve desired gain with single stage amplifier. Furthermore, insertion loss of the passive components such as transmission lines (TLs) degrades the amplifiers gain. Thus, the LNA has five cascade amplifiers to achieve sufficient gain as shown in 6.10(a). Each cascade amplifier has grounded coplanar TLs used as matching and load circuits both to avoid influences of lossy substrate and to suppress leakage signals from the TX circuit on the same die. As explained before, the IC is fabricated by using a standard CMOS process which does not have special thick copper layer. Therefore, a top aluminum layer for pads is used for the signal line to achieve lower insertion loss and 50 Ω characteristic impedance (Z_0). The insertion loss of the TL at 77 GHz is about 1.4 dB / mm in our design.

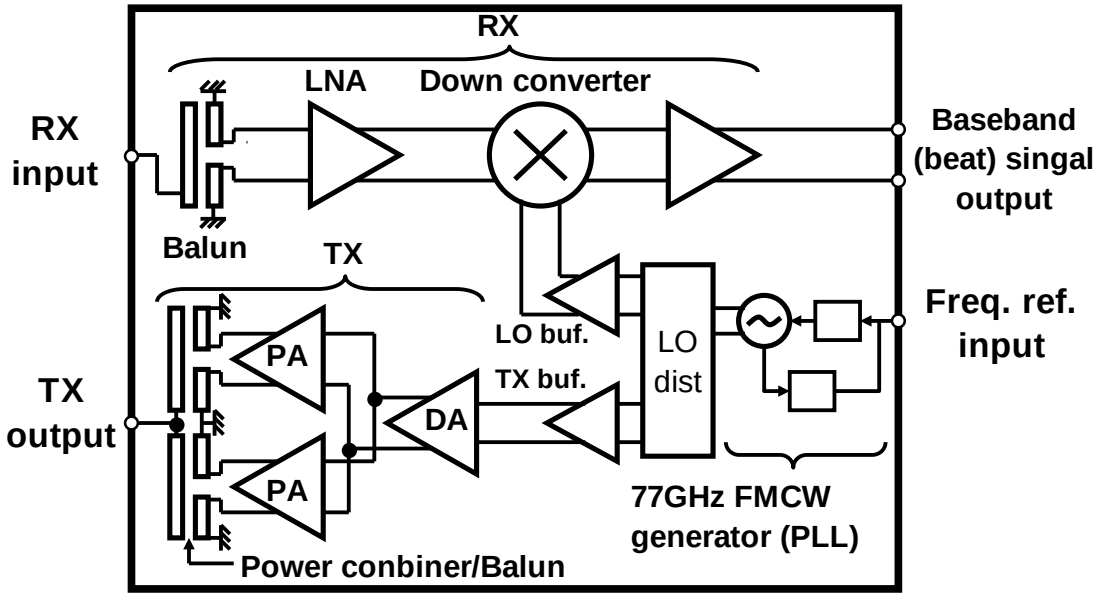


Figure 6.9: Block diagram of the fabricated TRX IC.

The LNA employs differential circuitry to avoid the influence of the complicated parasitic element networks at the ground and common nodes such as a power/bias supply and each amplifier's input and output differential impedance is matched to 100 Ω. In order to obtain higher gain with lower current consumptions, a bias current density per gate width of the transistors is selected to 250 μA/μm which can obtain highest MAG of the NMOS transistors from the measured results. Since a general high gain / narrow beam antenna for radar applications is a single-ended input and output terminal, an on-chip TL-based Marchand balun is used at the input of the LNA to convert a single-ended signal from the 50 Ω output impedance of antenna to a differential signal of 100 ΩFigure LNA input. The measured gains of the LNA with and without balun are 14 dB and 16.3 dB, respectively. The current consumption of the LNA is 45 mA.

A down-conversion mixer consists of a double-balanced mixer using a common-gate circuit for the input stage to obtain wider bandwidth as shown in Fig. 6.11. The common source node of the switching pair of the mixer is connected to a current source to drive the switching pairs easily with small LO signal amplitude. The output power of the synthesizer is estimated about -12 dBm from the measured result and the power gain of the LO distribution circuit with two-stage common-source buffer amplifier is 2 dB from the simulation result. Thus, the LO input power for the down-conversion mixer, including a single stage LO buffer amplifier, is assumed to be around -10 dBm. Figure 6.11 shows the simulated results of the normalized conversion gain variation with LO input power. The conversion gain with boosting current source is saturated around -10 dBm LO input power which is much lower than the case without boost. Inductors using TLs are connected between the common-source of the switching pair and the current source in order to cancel the parasitic capacitances to achieve higher conversion gain.

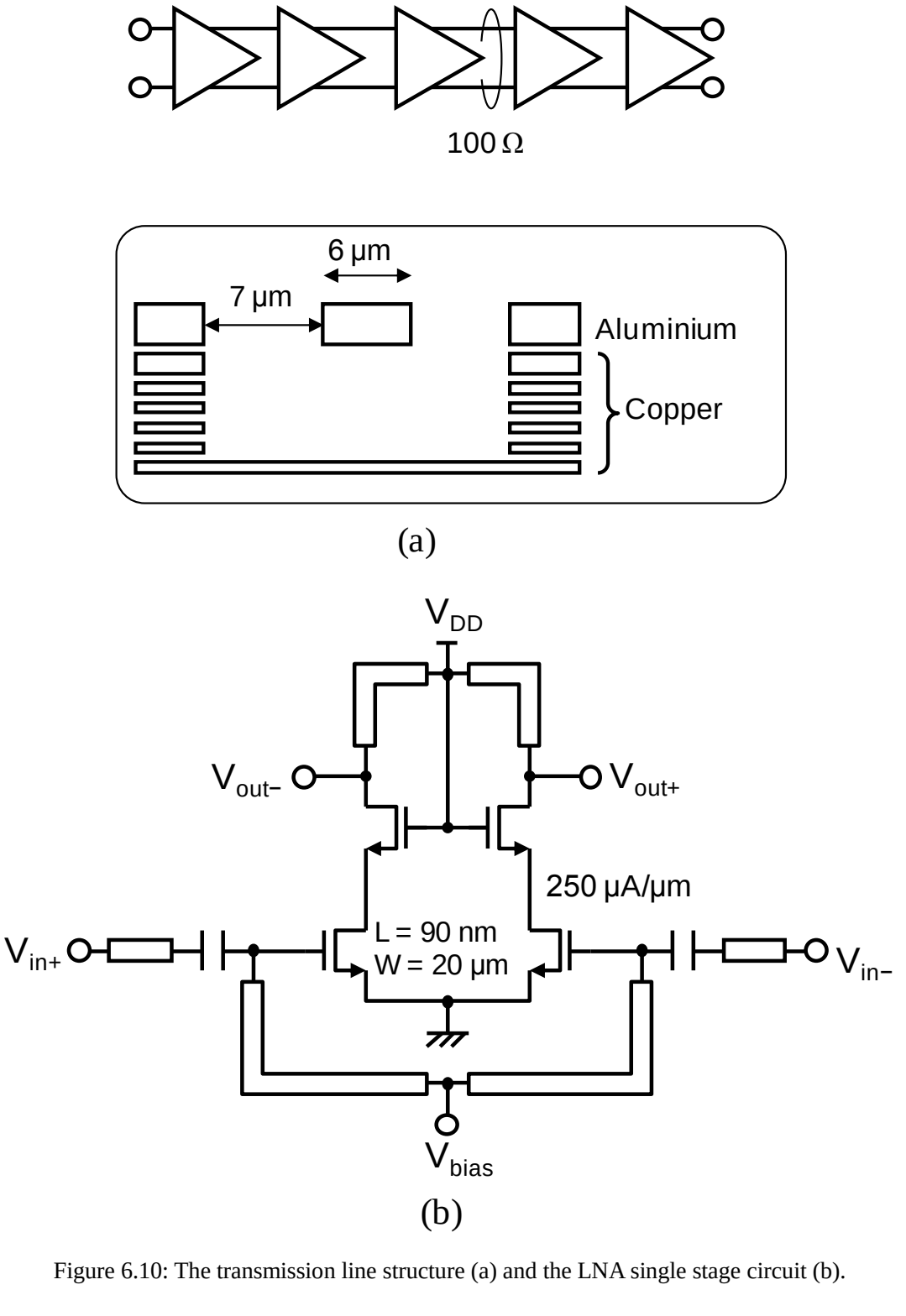


Figure 6.10: The transmission line structure (a) and the LNA single stage circuit (b).

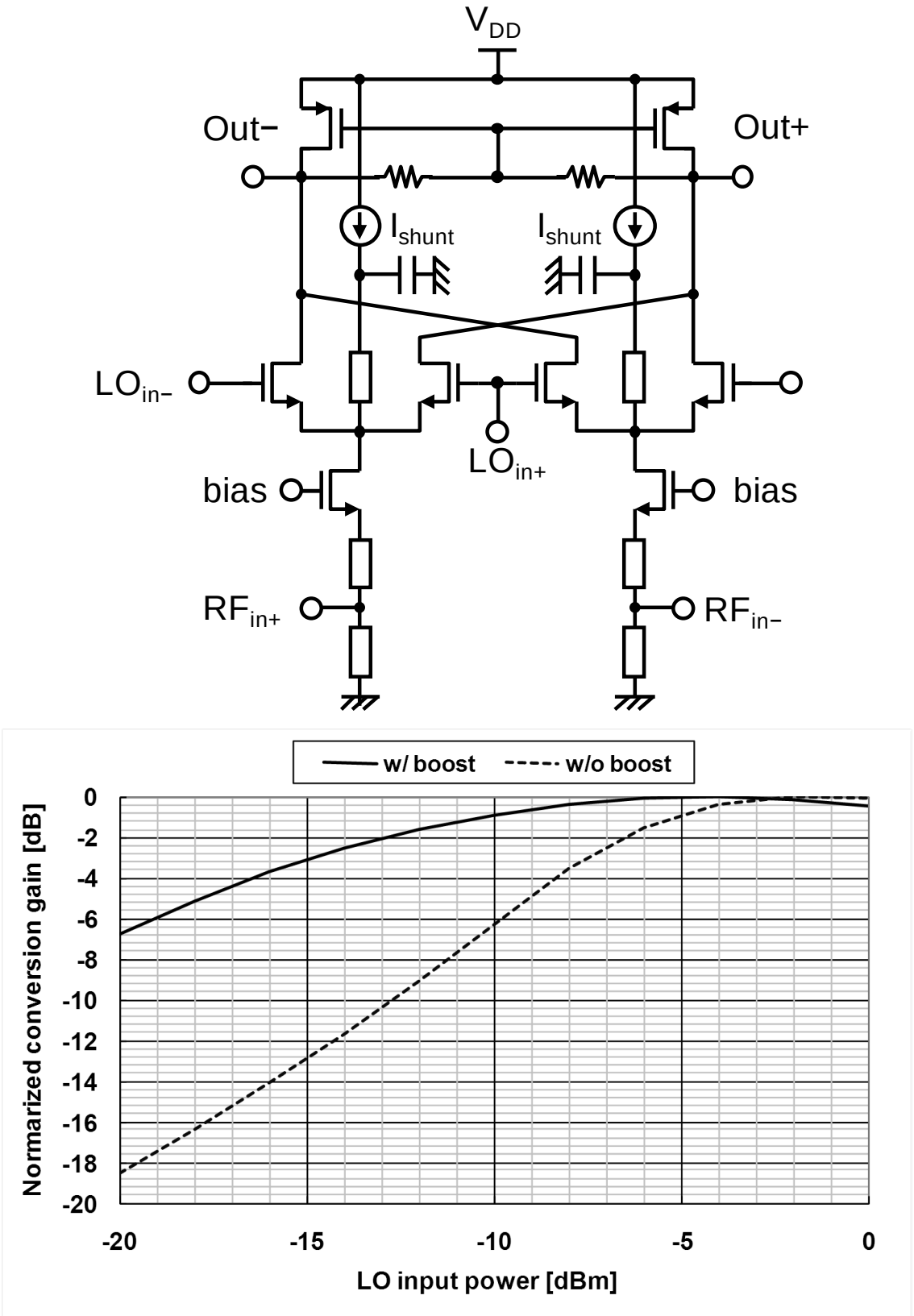
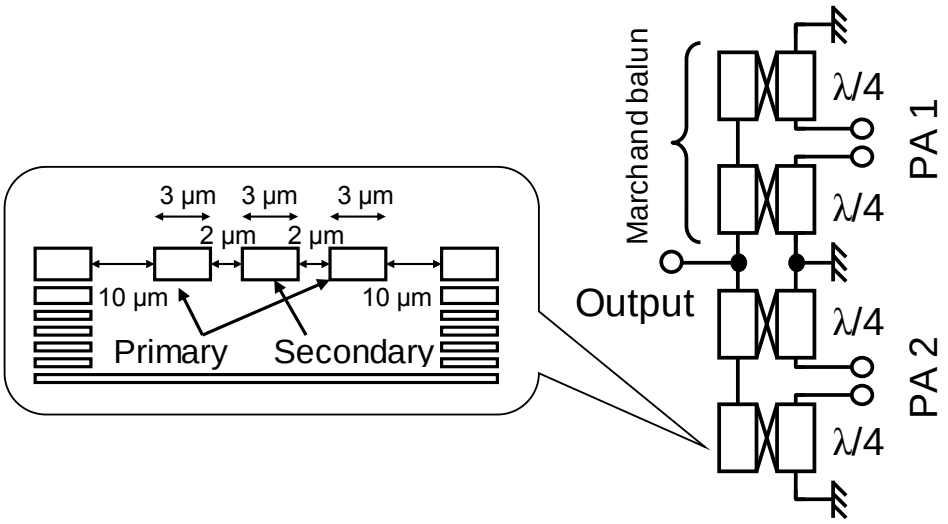


Figure 6.11: Mixer circuit and conversion gain variation with LO input power.

The TX block has a power amplifier (PA) and a driver amplifier (DA) as shown in Fig. 6.9. Figure 6.12 shows the PA consists of 2 differential common-source amplifiers and a power combiner. The Marchand balun based power combiner, which consists of λ/4 of the 77 GHz signal length TL based coupling line, is used to achieve differential to single-ended transformation, power combining of two amplifiers output and impedance transformation from the PA output impedance to 50 Ω for external antenna input impedance [102]. Figure 6.12 shows the structure of the Marchand balun based power combiner. The output of the single-ended signal of each balun is in-phase. As a result, the output power of the combiner is ideally equals to twice the power of each PA. In order to obtain required coupling factor for the balun, the secondary line is placed between two primary lines as shown in Fig. 6.12. The architecture of the DA is the same as that of the LNA circuit to achieve sufficient gain from the synthesizer output and LO distribution circuitry.



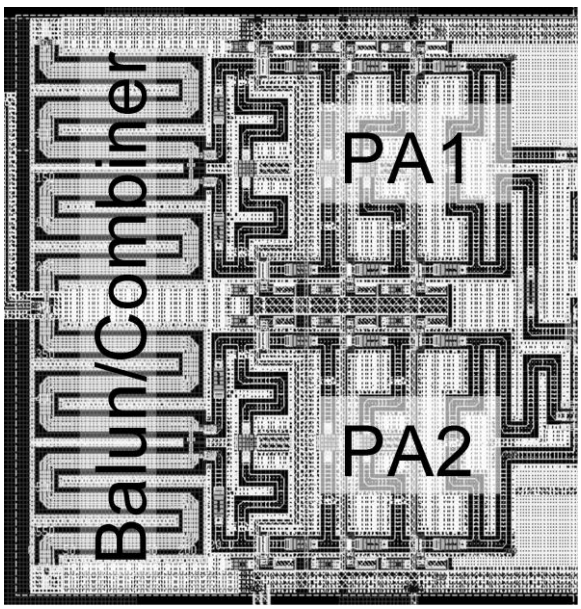


Figure 6.12: The PA block diagram and layout image using a Marchand balun-based power

combiner.

A 77 GHz VCO consists of an NMOS cross-coupled pair with a resonator using a TL and accumulation-mode varactors. As shown in Fig. 6.13, wider metal compared to the 50 Ω TL used for other circuit blocks is applied to reduce insertion loss and to achieve higher Q. The TL has 38 Ω Z_0, 120 μm length. Since the TL is connected between the differential output nodes, the TL works as an inductor whose inductance is about 30 pH. The resonating capacitance including the parasitic capacitances at the output nodes is designed to have the value from 135 fF to 145 fF and the resonance frequency is designed to have around 77 GHz with 1 GHz variation under the control voltage from 0.2 V to 1.0 V. A prescaler for 77 GHz is an injection-locked frequency divider [103]. Measured PLL locking range is about 800 MHz around 78 GHz and the phase noise is –85 dBc/Hz at 1 MHz offset as shown in Fig. 6.13. Since the transfer function of the PLL is designed to validate the smoothing function for stair-like reference signal, order of the PLL transfer function is 1st order by using parallel RC low pass filter for LF. It means that the PLL phase noise can be improved by adopting higher order transfer function to extend the loop bandwidth of the PLL. By using higher order transfer function, sufficient spurs suppression of the stair-like reference signal can be obtained even if the loop bandwidth is extended.

The output signal from the PLL is distributed to both the RX LO buffer connected to the mixer and the TX buffer amplifier connected to the DA. Figure 6.14 shows the distribution network. The buffer amplifiers are connected to the PLL simply via TLs with $Z_0 = 50$ Ω to reduce chip area and insertion losses. Since the RX and TX buffer circuits are the same architecture, the impedance matching and accurate power distribution are achieved simultaneously using the same matching circuit and distribution TLs.

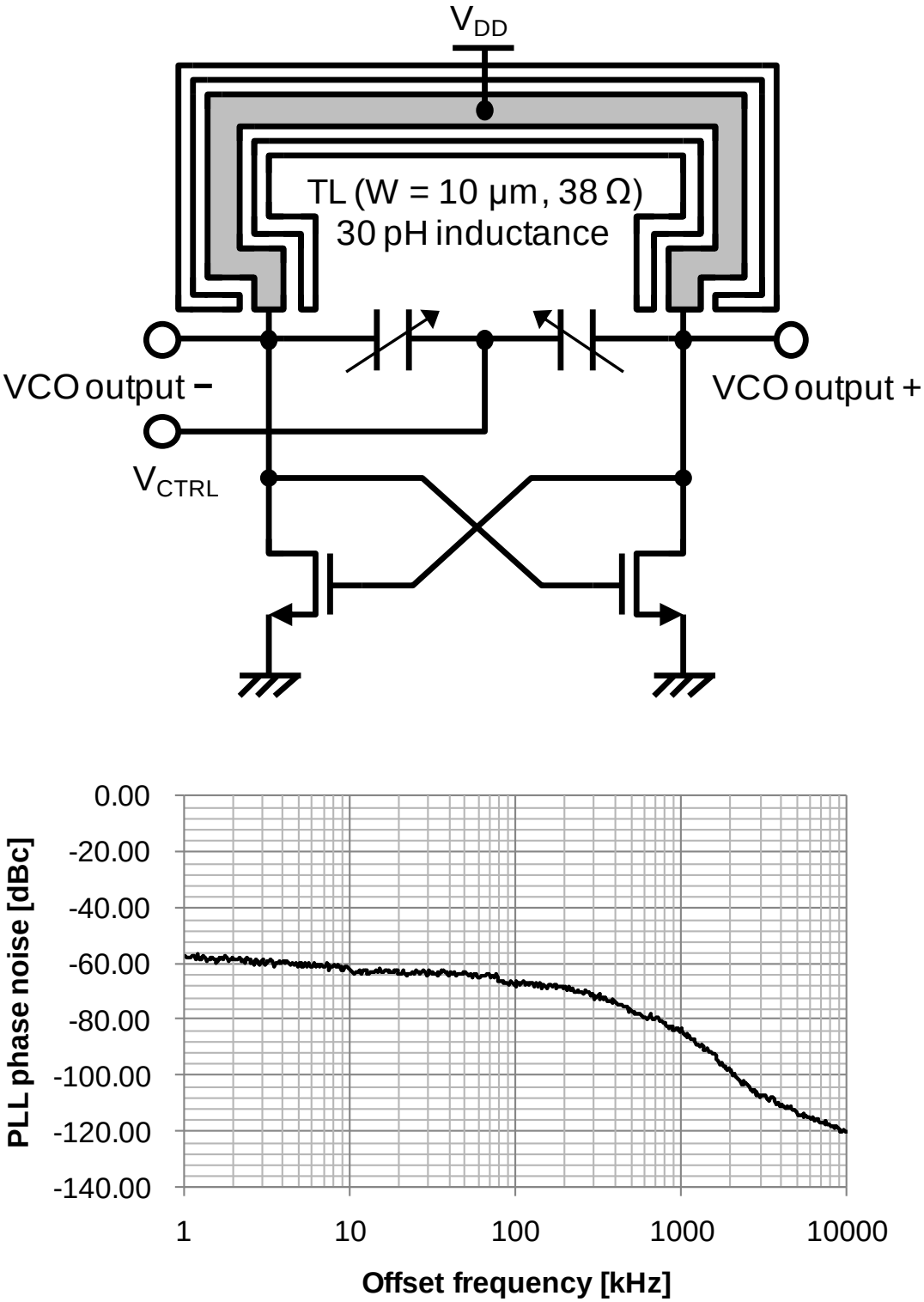


Figure 6.13: The VCO circuit and the measured PLL phase noise.

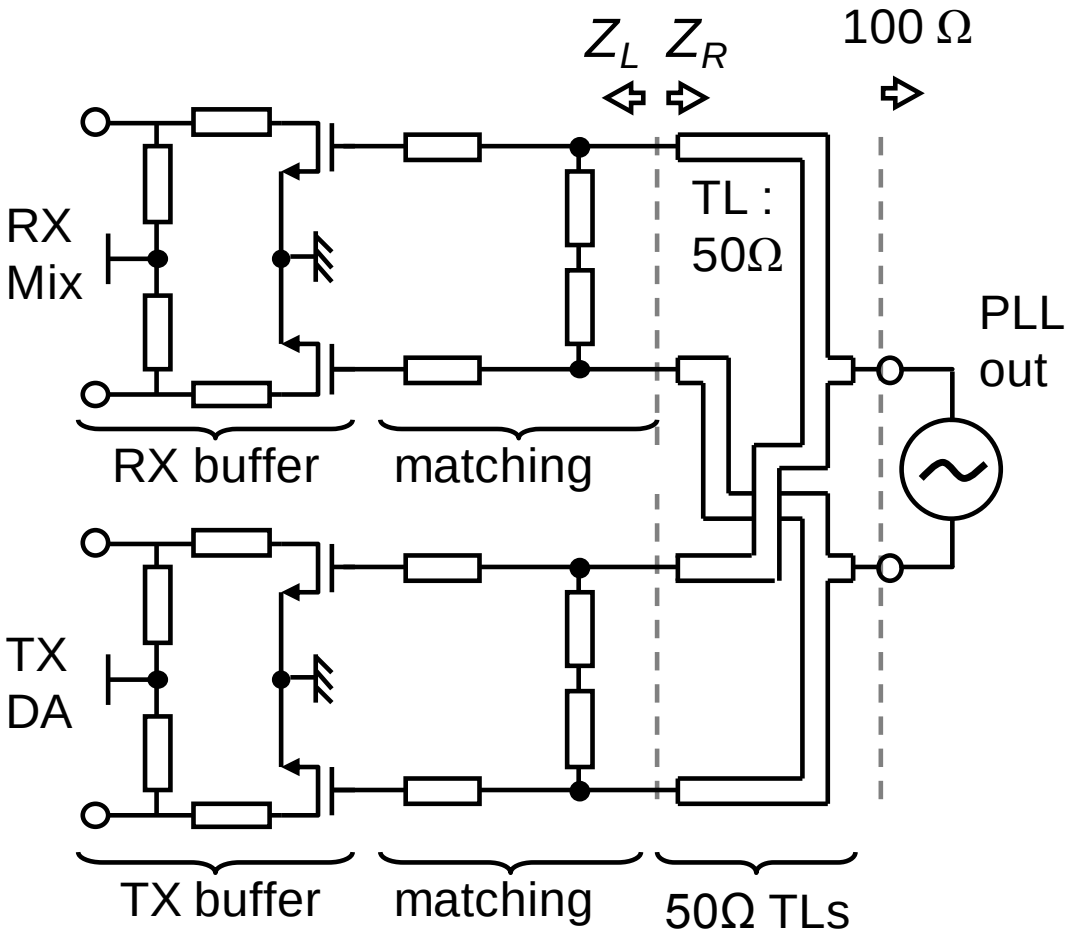


Figure 6.14: Signal distribution for the TX and the RX buffers using simple power divider and distributor bsed-on transmission lines.

6.4 Measured Results

Figure 6.15 shows a die photograph of the fabricated radar TRX IC using 90 nm CMOS process. The chip size including pads is 3.50×1.95 mm^2. The fabricated IC is measured on a probe station and the frequency reference signal for the on-chip PLL is generated by using an arbitrary waveform generator as shown in Fig. 6.16. The frequency reference signal that is assumed to be an 8 bit / 1.2 MHz DDFS is generated and the signal is converted to analog signal by 8 bit DAC. The output signal of the DAC is up-converted to 77 MHz carrier signal using SSB mixer and 77 MHz CW signal. The measured output spectrum of the TX is shown in Fig. 6.17. The spectrum that has 614 MHz bandwidth is achieved from a 600 kHz bandwidth frequency reference signal and N=1024 division PLL. Note that the Fig. 6.17 is a photograph of the display of the spectrum analyzer. Although the measurement was done by 20 ms sweep time that is shorter than FMCW chirp period, the image of previous sweeps is remained. Therefore, the spacing of the spectrums in Fig. 6.17 is not uniform.

Frequency chirp is also measured by using an external down-conversion mixer and a signal source analyzer. Figure 6.18 shows a measured time-domain frequency chirp of the TX output. The result shows a linear frequency chirp is achieved even using a low-spec rough stair-like frequency reference signal. The FMCW frequency error, sinusoidal nonlinearity, is extracted by subtraction of an ideal FMCW frequency chirp from measured FMCW frequency chirp. The time-domain frequency error is shown in Fig. 6.18, indicating that the standard deviation of the error magnitude of 1.05 MHz appears at any time. In order to extract sinusoidal nonlinearity from the measured results, the time domain frequency error variation is converted to frequency domain by using fft. Figure 6.19 (a) shows the output frequency error at the reference signal in frequency domain. Large spur appears at 400 kHz, which is equal to $1/\Delta t$, caused by stair-like frequency chirp from low-spec DDFS. Since the phase noise of the arbitrary waveform generator is not sufficiently low, the frequency reference signal has flat frequency error like white noise. This results in large frequency error at the transmitted signal as shown in Fig. 6.18. The noise can be reduced by using more accurate low-frequency DAC for the DDFS output and low phase noise CW generator such as a crystal oscillator. Figure 6.19(b) shows the frequency domain error magnitude of the transmitted signal. Even though the white noise in the reference signal is multiplied 1024 times, the spur at $1/\Delta t$ is suppressed by using the proposed PLL. The sinusoidal error magnitude that corresponds to the magnitude of the spur at $1/\Delta t$ is 93 kHz. According to equation (5.2), the ranging resolution is about 1 m for a target located at 100 m distance. Note that the cut-off frequency and the peaking property of the PLL transfer function of the fabricated IC is not same to the estimated result as shown in Fig. 6.5 due to variation of the loop filter components, resistance and capacitance, and the CP current.

Ranging performance of the fabricated TRX IC is measured by using external 20 dBi horn

antennas. Ranging measurement for the fixed target is done with the set-up as shown in Fig. 6.20. The output signal of the TRX is radiated to the ceiling at 2.8 m distance and the reflected signal is input to the RX antenna. Figure 6.21 shows a spectrum of the received signal. The peak of the spectrum is located at 46 kHz, which corresponds to 2.8 m for the fabricated FMCW radar. Spurs at 46 kHz ± 400 kHz ($1/\Delta t$) arise owing to the nonlinearity of the FMCW frequency chirp is less than 30 dB which is the same level as the floor noise. Note that the spectrum around 86 kHz is double-reflected signal by the probe station. The distance for 86 kHz is shorter than 2.8 m × 2 because the path does not include the cable between the antenna and the IC in the first reflection path.

The radar performance is also measured using a small metal reflector target with various distances and the measured distance is shown in Fig. 6.22. The standard deviation of the error for each measurement is less than 1 % for a target at from 1 m to 8 m. Note that we have no velocity data because we do not have a moving target.

The performance of the 77 GHz TRX is summarized in Table II. A ranging distance with a certain detection probability and false alarm ratio can be estimated by signal-to-noise ratio (SNR) of the received signal [104]. The received power is estimated from the radar equation [104]:

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{6.3}$$

where P_t is the output power of the TX, G_t and G_r is the antenna gain for input and output, λ is the wavelength of the 77 GHz signal and σ is the reflection cross-section of target. The SNR is calculated from the received power at the RX input, noise figure of the RX and the resolution of the fft at baseband DSP. The RX SNR (SN_{RX}) in ideal environment is calculated by

$$SN_{RX} = \frac{P_r}{\kappa T \cdot NF \cdot f_{fft} / p_{fft}} . \tag{6.4}$$

For achieving the detection probability of 99 % and the false alarm ratio of 10^{-10}, 16 dB of SN_{RX} is required [104]. In order to estimate the SN_{RX} of the fabricated TRX IC, the parameters in Table 6.3: Estimated link-budget of the fabricated IC are used for the variables in equation (5.3) and (5.4) and σ of 10 m^2 is used assuming a small car target [105], [106]. The calculated result shows 16 dB SN_{RX} is obtained for R = 107m. Note that the fft period is longer than that of FMCW chirp (4096 points for 2 MHz Nyquist frequency) in order not to degrade the SN_{RX} from fft resolution.

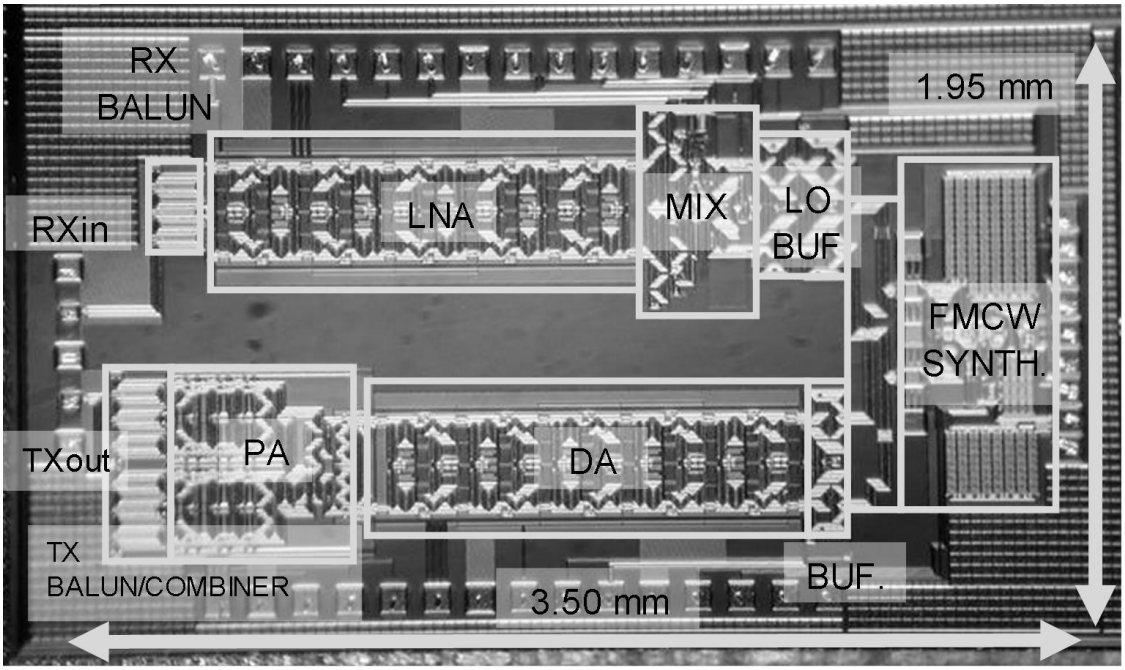


Figure 6.15: Micro-photograph of the fablicated radar TRX IC in a 90nm CMOS process.

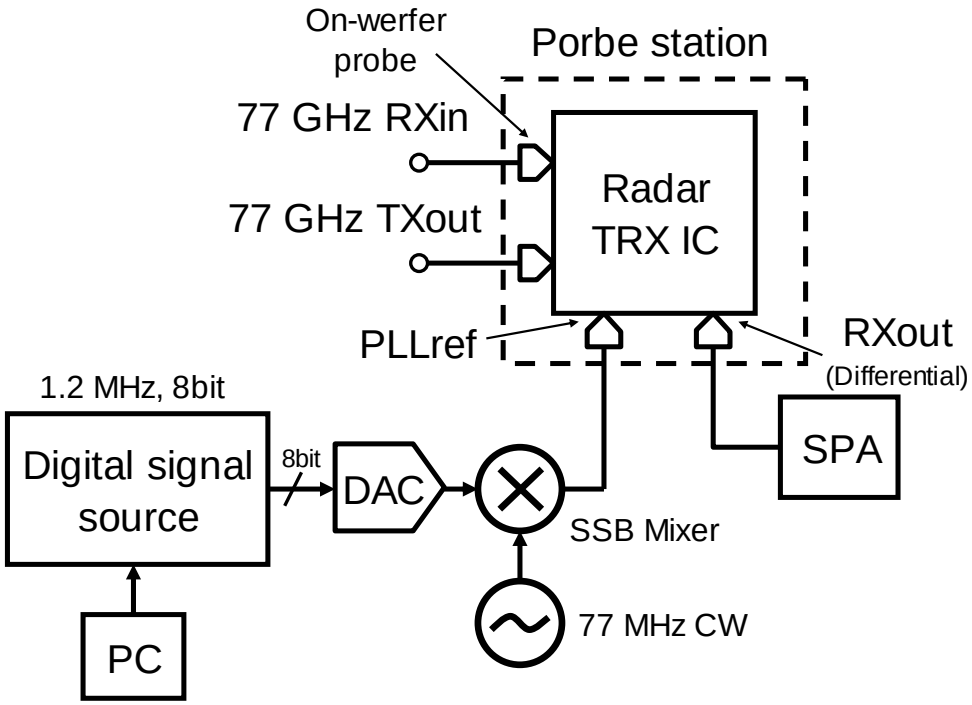


Figure 6.16: Measurement set-up of the radar TRX IC.

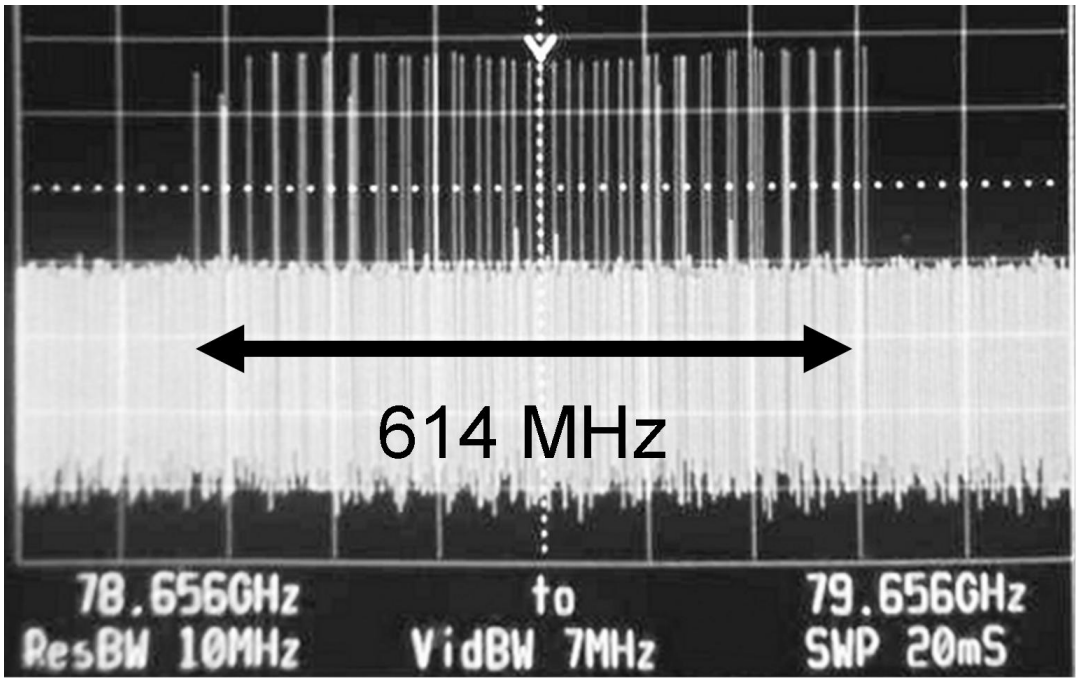


Figure 6.17: Radar measurement using a external antenna and fabricated radar TRX IC.

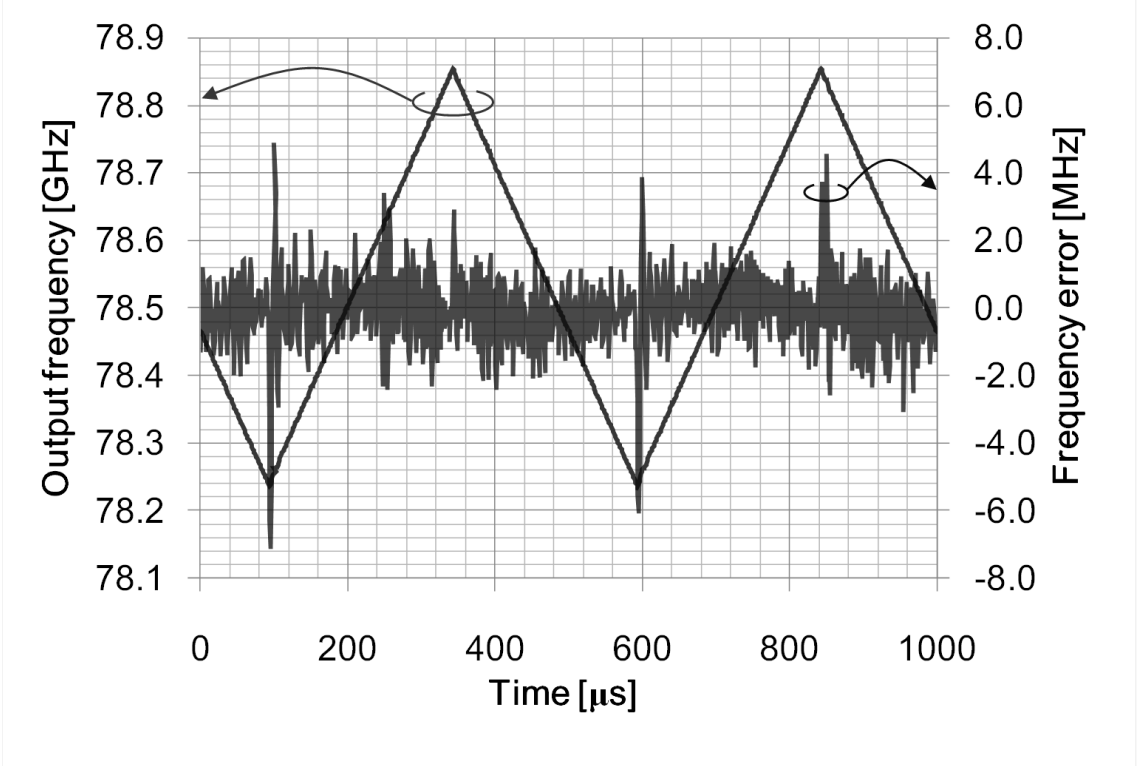
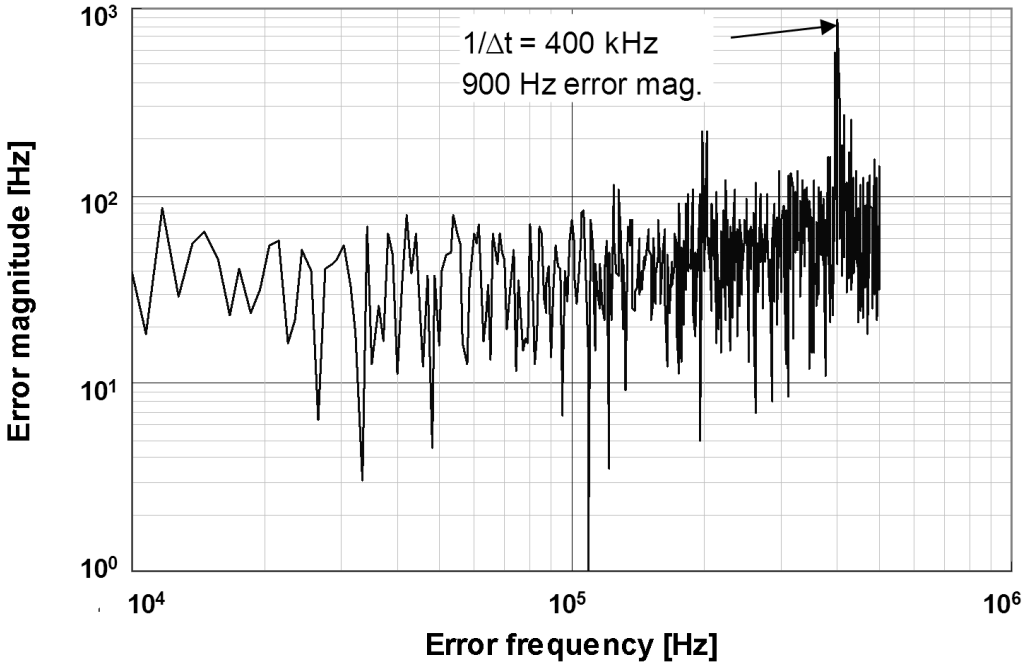
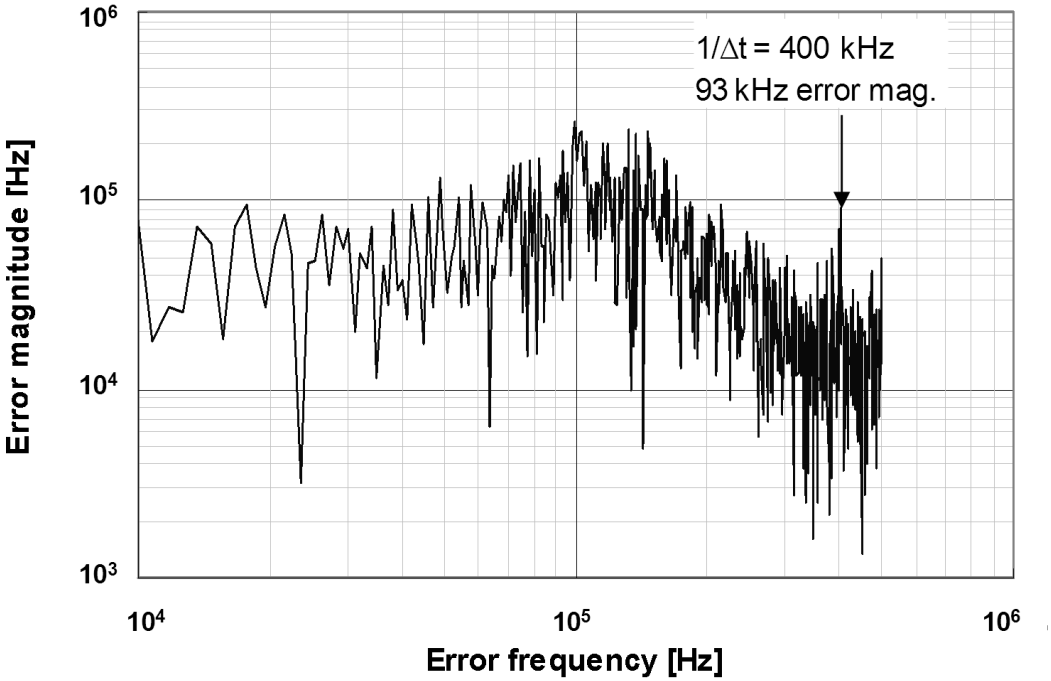


Figure 6.18: Measured output frequency chirp and time-domain frequency error to an ideal FMCW chirp.



(a)



(b)

Figure 6.19: Measured frequency domain frequency chirp error against an ideal FMCW signal of the frequency reference (a) and that of the output signal (b).

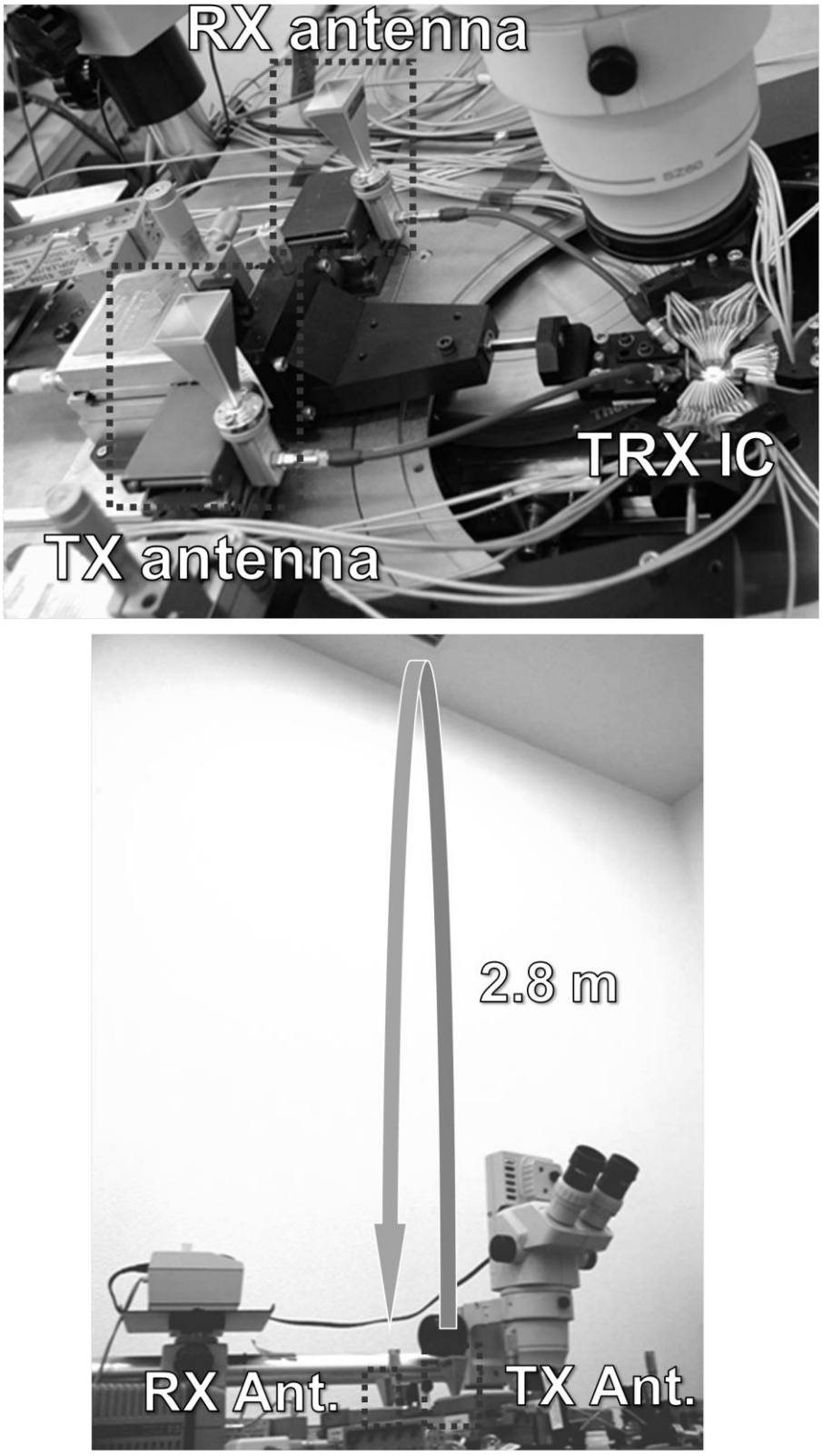


Figure 6.20: Radar measurement using an external antenna and fabricated radar TRX IC.

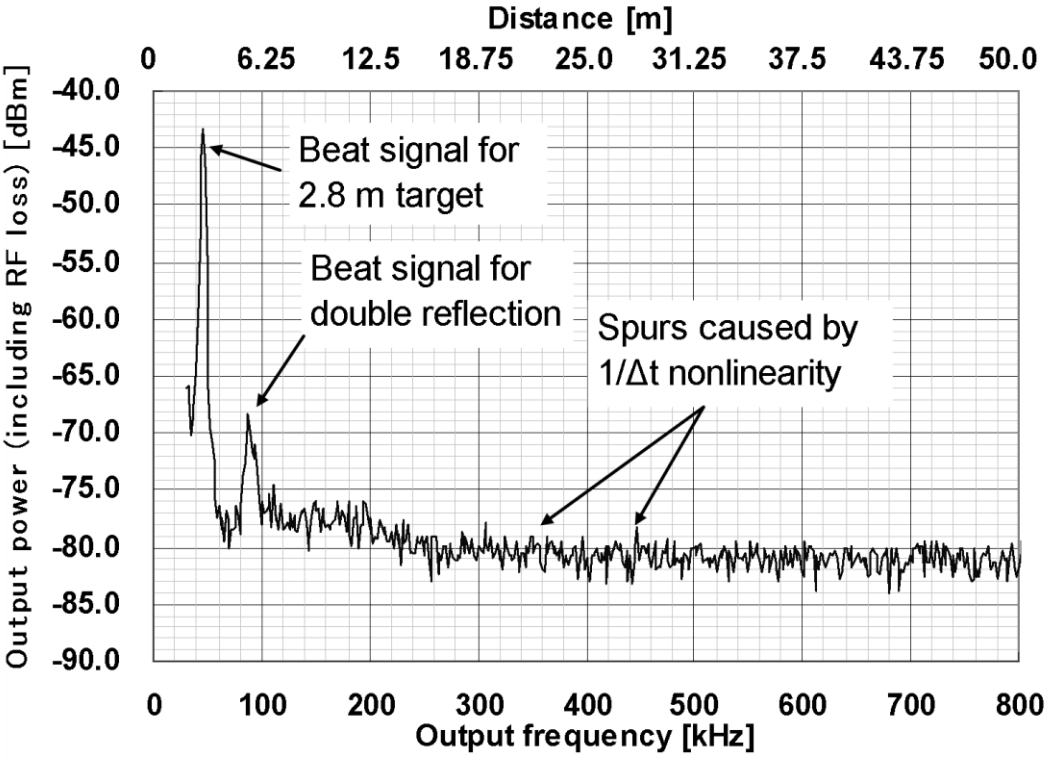


Figure 6.21: Measured output spectrum that is corresponding to the target distance for the target located at 2.8 m.

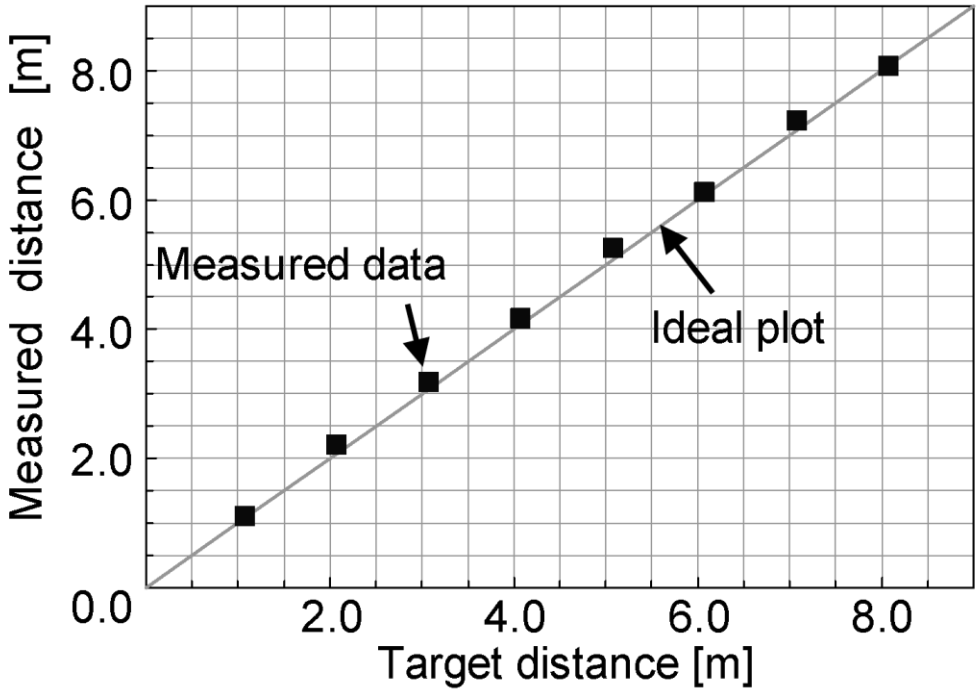


Figure 6.22: Measured distance for a target located 1 m to 8 m distance.

Table 6.2: Performances of the radar TRX IC.

Synthesizer operating frequency	[GHz]	78.1-78.8
Synthesizer output power	[dBm]	-13
Synthersizer phase noise (1MHz offset)	[dBc/Hz]	-85
Synthesizer power consumption (1.2V Supply)	[mW]	101
TX ouput power	[dBm]	-2.8
TX power gain	[dB]	14
TX power consumption (1.2V Supply)	[mW]	305
RX power gain	[dB]	23.1
RX noise figure (single side band)	[dB]	15.6
RX power consumption (1.2V Supply)	[mW]	111

Table 6.3: Estimated link-budget of the fabricated IC.

PA output power	P_t	[dBm]	-2.8
TX antenna gain	G_t	[dBi]	20
RX antenna gain	G_r	[dBi]	20
Wave length	λ	[mm]	3.9
Reflection cross section	σ	[m^2]	10
Distance	R	[m]	107
Receiver NF	NF	[dB]	15.6
fft Nyquist freq.	f_{fft}	[MHz]	2.0
fft points	p_{fft}		4096
RX Input noise	κT	[dBm/Hz]	-173.8
RX Input power	P_r	[dBm]	-115.1
RX S/N	SN_{RX}	[dB]	16.17

6.5 Comparison and Summary

The comparison of the required DDFS specification is shown in Table 6.4 [98], [107]. This means the proposed FMCW generator circuits can operate even using a reference signal with chirp nonlinearly.

The first CMOS radar TRX IC using a PLL capable of generating linear FMCW frequency chirp with low-spec DDFS is presented. The TRX employs a PLL capable of smoothing nonlinear stair-like reference frequency signal generated by low-spec DDFS. The measured results show that the chirp nonlinearity of the output signal from the TX is 93 kHz for 614 MHz bandwidth with 77 GHz band carrier. The fabricated IC shows less than 1 % ranging error for 1 m to 8 m ranging measurement and the estimated maximum ranging distance for 10 m^2, small car, reflection cross-section target in ideal condition is 107 m. These measured results show the TRX IC achieves fundamental performance for FMCW radar applications.

Table 6.4: Estimated link-budget of the fabricated IC.

Reference	Clock [MHz]	Control Word Length [bits]
ISSCC2007 [96]	150	28
EuMC2007 [105]	320	17
This work	1.2	8

Chapter 7

General Conclusions

7.1 Summary of the Compensation Technique

Highly integrated RF ICs are desired for a small and low-cost wireless solution to realize the future ubiquitous network society. This dissertation describes the method of compensation of performance degradation for highly integrated high-frequency analog wireless circuits by using analog circuits. The results of the approaches can assist designers of high-frequency circuits or wireless systems select an appropriate compensation method.

In Chapter 1, the motivation for integrating of wireless systems and some critical issues are introduced. These issues are expected to be resolved by adopting a digital or analog compensation method for high-frequency analog circuits. The purpose of this dissertation is introduced, namely, clarification of the adoptable regions of both methods by substantiation of the compensation method using analog circuits.

In the Chapter 2, the issue of LO signal leakage in a cellular phone system, which is a case of the high-frequency signal leakage problem explained in Chapter 1, is discussed. This is a serious problem for direct-conversion RXs. LO leakage via QDEMOD must be suppressed in order to achieve a low DC offset and spurs emission from the antenna. An LO buffering circuit that drives QDEMOD is the main cause of the LO leakage. An LO buffer with a compensation method using analog circuits that has a high-pass frequency response with small occupied area and low current consumption is proposed. A QDEMOD using the proposed LO buffer is fabricated in a SiGe BiCMOS process. Measured low LO leakage of -70dBm is achieved, which is 10dB lower than that of a QDEMOD with a conventional LO buffer. It is equivalent to the suppression of the DC offset to less than 1/3. A performance comparison of the LO signal leakage shows the leakage power is the same level as the state of the art. This measured result indicates that the proposed compensation technique using analog circuits is suitable for high-frequency signal leakage.

In the Chapter 3, an issue of performance degradation of RX QDEMOD caused by TX signal leakage in a cellular phone system is introduced, which is a case of the high-frequency signal leakage problem explained in Chapter 1. A mixer circuit for QDEMOD using a common-base input stage is robust to parasitic elements and is suitable for integrating on-chip matching circuits to realize a small and low-cost wireless system. However, a common-mode blocker signal, such as the

TX leakage signal, degrades the noise performance due to DC current increase and intermodulation distortion of the TX leakage signal and noise. We propose a QDEMOD with a common-base input stage capable of suppressing the TX leakage signal using symmetrical inductors. The measured results show that the NF degradation does not occur until the TX leakage signal input is larger than -10 dBm. This technique relaxes the isolation specification between TX and RX. The required isolation with a typical TX driver amplifier in the same die including various leakage paths is 20 dB and the isolation has a margin against typical isolation of silicon substrate of 40 dB. The approach described in Chapter 3 is applicable to TX and RX circuits in the same die. The QDEMOD with the proposed compensation technique using analog circuits is suitable for small and low-cost RF front-end modules and for TRX ICs for WCDMA application.

Chapter 4 describes a 60-GHz RX front-end chip to substantiate the effectiveness of the compensation method using analog circuits for the issue of performance degradation due to insufficient high-frequency performance of integrated silicon devices. The RX chip consists of an LNA, a down-conversion mixer and a phase-locked loop synthesizer. The components of the RX chip employ fully differential architecture to avoid influences of parasitic components. Since the down-conversion mixer requires a high voltage LO signal for saturating operation, a number of buffering amplifiers and power consumptions are required. To resolve the issue, a mixer circuit with a current bleeding technique was adopted. By using the proposed mixer the required LO input power could be reduced. A comparison of the required LO input power for down-conversion mixers shows that the required LO signal power for the proposed mixer circuit is the lowest among all the approaches. These results indicate that the proposed compensation technique using analog circuits can be applied to very high-frequency wireless systems.

Chapter 5 describes a fully-integrated 60 GHz TRX chip for substantiating a very highly integrated system. In order to realize a TRX in the same die, a TX/RX selecting switch with an insertion loss compensation technique using analog circuits is applied. And in order to compensate the gain performance degradation due to insufficient high-frequency performance of the integrated devices with minimum drawbacks, an LNA and mixer combination circuit with a current reuse structure including a current bleeding structure for a mixer circuit is proposed. A comparison of the power consumption of the LNA and mixer circuit of 60 GHz band shows that the smallest power consumption can be achieved with the proposed circuit based on the compensation method using analog circuits. The chipset achieves 2.62 Gb/s data rate, 2.07 Gb/s throughput and energy consumption of 651 pJ/bit by high efficiency MAC using short interval frame exchange with fast RF TX/RX switching. The proposed high-frequency circuits using analog circuits are suitable for small and low-cost RF front-end modules.

In the Chapter 6, a 77 GHz FMCW radar TRX IC with an FMCW chirp signal generator is presented for a case of a very high-frequency TRX with insufficient performance of the integrated

devices. In the case of an FMCW radar system in such a high-frequency oscillation, chirp nonlinearity of the frequency chirping generator based on DDFS degrades the performance of the whole radar system. A PLL synthesizer adopting chirp smoothing technique that is able to output linear FMCW frequency chirp using a nonlinear reference chirp signal is proposed. The comparison for a 77 GHz FMCW signal generator of the required DDFS specification shows that the proposed FMCW generator circuit can operate using a reference signal without very high accuracy in order to compensate the chirp nonlinearity of the FMCW generator. And the same techniques introduced in Chapter 5 are adopted for the whole high-frequency circuits and a mixer circuit that are operating at 77 GHz band. The estimated ranging capability based on measured performance is up to 100 m. These results indicate that the proposed compensation technique using analog circuits can be applied to very high-frequency wireless systems.

As reported in Chapters 2 to 6, compensating high-frequency analog circuits by using analog circuits is effective for two of the issues explained in Chapter 1, as shown in Fig. 7.1. The first issue is high-frequency signal leakage and the effectiveness of the compensation technique is substantiated in Chapters 2 and 3. The second issue is insufficient silicon device performance for high-frequency operation and it is substantiated in Chapters 4 to 6. Therefore, the compensation technique using analog circuits covers a region that is unsuitable for compensation by using digital circuits. The relationship of the two compensation techniques using analog and digital circuits is summarized in Fig. 7.2. The vertical axis of the plot shows an integrating scale or number of the high-frequency circuits and the horizontal axis shows f_C/f_T of the wireless TRX. The larger the value of the vertical axis, the greater the number of the high-frequency circuits/systems integrated into the same IC die and the higher the risk of ta signal leakage problem. The smaller the value of the horizontal axis, the higher the carrier frequency and the higher the risk of performance degradation caused by insufficient high-frequency characteristics. As explained in Chapter 1, a compensation technique for high-frequency circuits by using digital circuits is highly effective for issues caused by PVT variation because it can monitor performance variation. This compensation technique is effective mainly in a low to relatively high carrier frequency region for large-scale integration and a medium frequency region for relatively small-scale integration. This is because the performance monitor circuit for the compensation can pick up DC to relatively low-frequency signal. On the other hand, the compensation technique using analog circuits is effective for the remaining upper right region where the compensation technique using digital circuits is ineffective. This is because the analog circuit for compensation can influence a part of the high-frequency signal of the core high-frequency circuit.

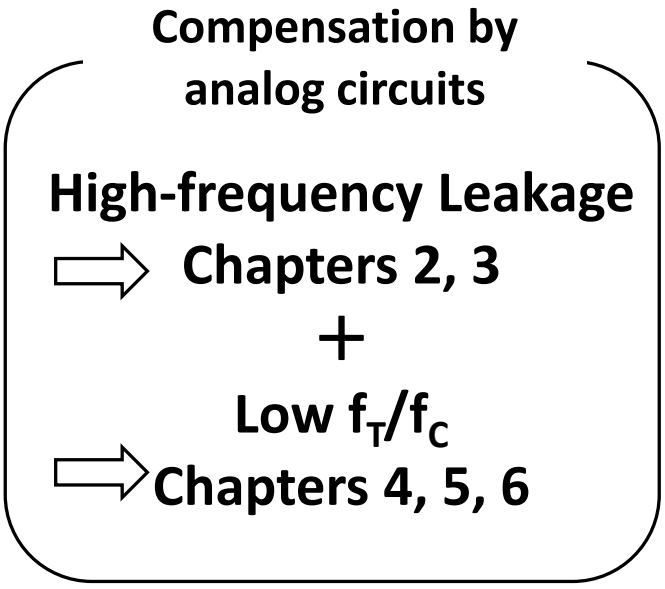


Figure 7.1: Summary of the substantiation of compensation technique for high-frequency circuits using analog circuits.

Therefore, a complementary relationship can be considered to issues for integrating high-frequency circuits. When issues concerning integration of high-frequency circuits arise, a designer of the high-frequency analog circuits and wireless systems can select an appropriate solution For example, if carrier frequency of the desired wireless system is much lower, about 20 to 30 times, than f_T of the silicon process applied and the main issue is performance degradation of high-frequency circuits due to PVT variation, the designer can select an appropriate solution on the basis of the Fig. 7.2, namely, a compensation technique using digital circuits. On the other hand, in the case of high-frequency performance degradation due to high-frequency signal leak from circuit blocks in the same die and the f_T having small margin against the f_C, the region in the plot corresponding to the issue is at upper right which means the designer should select the compensation using analog circuits. In addition, some situations concerning the issues are not substantiated in this dissertation. An important example of such an issue is a PVT variation of a high-frequency circuits including compensating analog circuits. The nominal performance of the high-frequency circuit is improved by the compensation techniques as explained in previous chapters. However, sometimes the improved performances are degraded by the PVT variation. In such a situation, the compensation method using digital circuits is applicable.

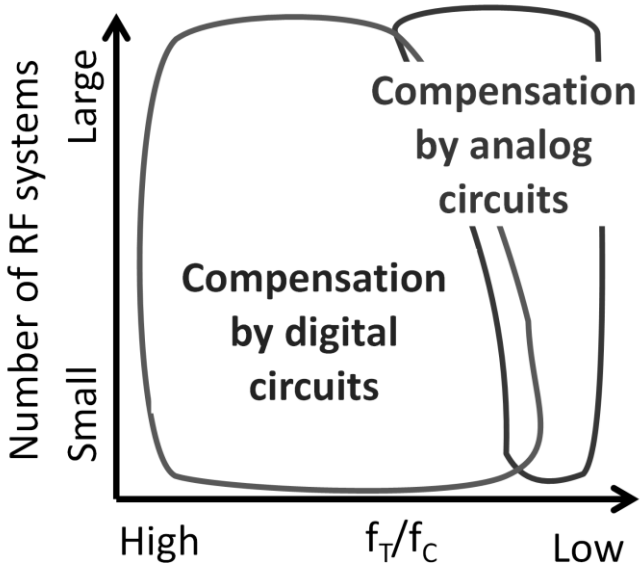


Figure 7.2: Effective region for compensating technique for high-frequency circuit using digital and analog circuits.

7.2 Future perspective

In this subsection, the perspective concerning future wireless systems and the effectiveness of the results of the research report in this dissertation are discussed. Finer Si semiconductor process and increase of f_T are expected to enable further advances in terms of the area occupied by digital circuits and the maximum operation frequency of the digital and ADC circuits. The effective region of the compensation technique using digital circuits extends to the upper and upper right regions as shown in Fig. 7.3. The expanded scope of the compensation method using digital circuits seems to overlap the effective region of the compensation technique using analog circuits. However, this will not result in the disappearance of the effective region of the compensation technique using analog circuits. The reason is described as below.

Wireless sensor/images for healthcare and safety are one of the future trends of wireless applications. As shown in Fig. 7.4 [108], the population ratio of people aged over 65 years in advanced countries is increasing. The change in the demographic profile means that the cost of medical care for the elderly will increase significantly in the future. Therefore, with a view to reducing medical costs, simplified medical tests at medical facilities and self-administered medical checks using personal testing systems are attracting attentions. Applications to secure safety and security to address threats posed by crime and terrorism are also attracting attention. As solutions for these needs, high-frequency, millimeter wave to terahertz, signal imaging technology has been proposed in recent researches [109]-[111]. In order to detect a signal generated by black-body

radiation or to improve ranging resolution of the target, such a very high-frequency signal is required. Furthermore, a phased array TRX is required for detecting angular information of the target in two-dimensional sensing. Furthermore, wireless systems capable of much higher data rates are expected; more than 100 GHz TRX is a challenge for over 10 Gb/s data transfer [112], [113].

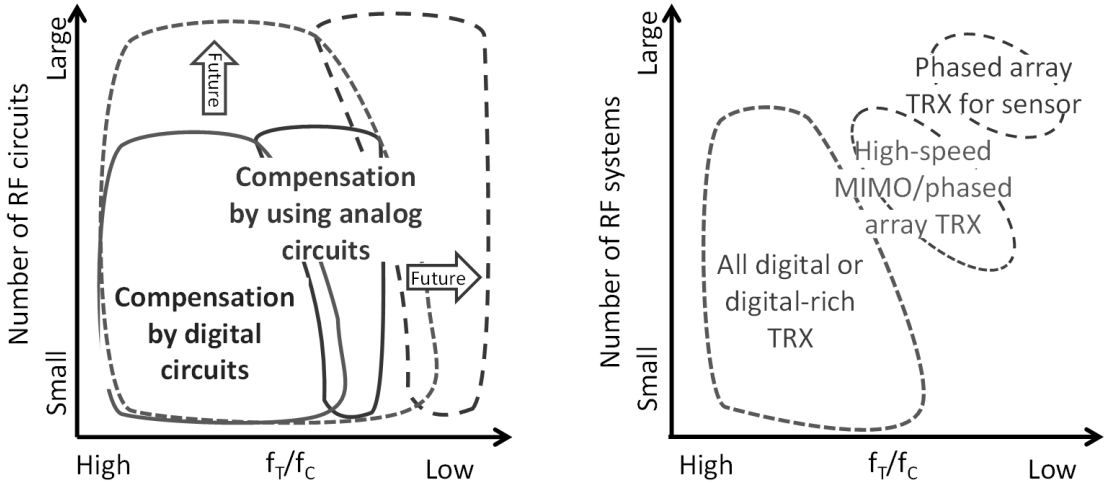


Figure 7.3: Prediction of future transition of effective region for compensating technique for high-frequency circuit using digital and analog circuit and trend of wireless systems.

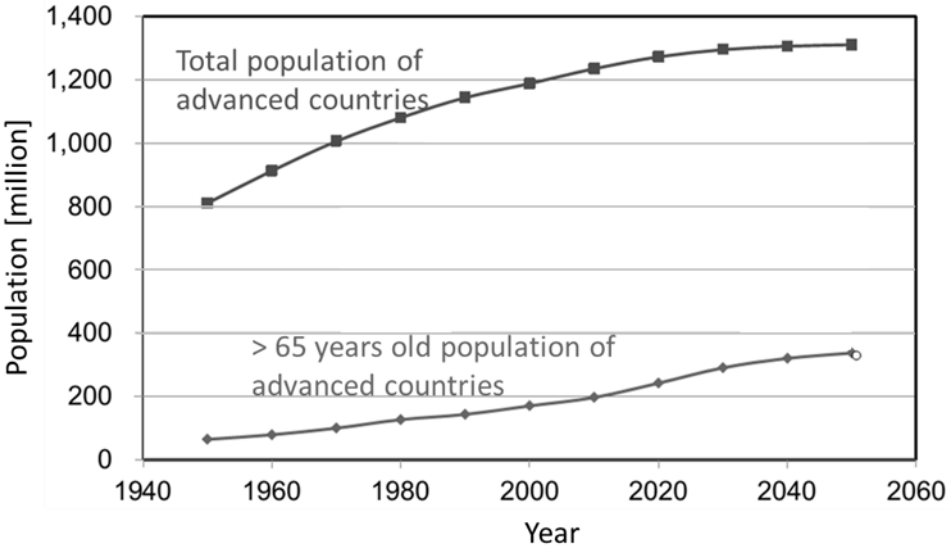


Figure 7.4: The changing demographic profiles of advanced countries [108].

The carrier frequency will increase and the number of high-frequency wireless circuits integrated will also be increase. These changes mean the region suitable for the adoption of the compensation technique using analog circuits will expand to upper right as shown in Fig. 7.3. Therefore, the effective region of compensation using digital or analog circuits will shift in accordance with process and frequency scaling. The relationship of the two compensation methods will be persist.

In addition, improvement of high-frequency circuit performance through a combination of compensation techniques using analog and digital circuits also will be effective. For example, a 60 GHz TRX with MIMO or phased array technology as shown in Fig. 7.6 [114] is currently in the effective region of the compensation method using analog circuits. However, even in such a region, a combination of compensation technique using analog and digital circuits is effective. This is because the basic performance of gain and NF can be compensated by using analog circuits and degradations due to PVT variation can be compensated by using digital circuits. Circuits with relatively low frequency range in the wireless system can be compensated by using digital circuits. Such a combination technique will also be effective for a future digital-rich TRX as shown in fig. 7.7 [21]. Even in such a digital-rich TRX, some high-frequency analog circuits will sometimes be effective for those circuits.

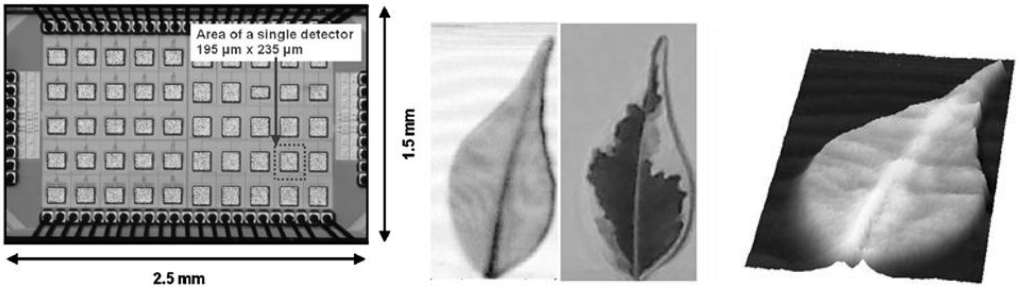


Figure 7.5: Terahertz wireless imager array [111]. ©IEEE 2011

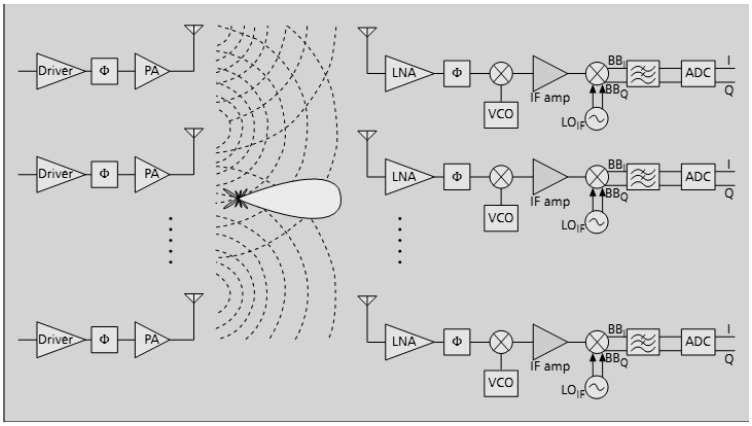


Figure 7.6: Future millimeter-wave wireless data transfer adopting MIMO or phased array system [114]. ©IEEE 2004

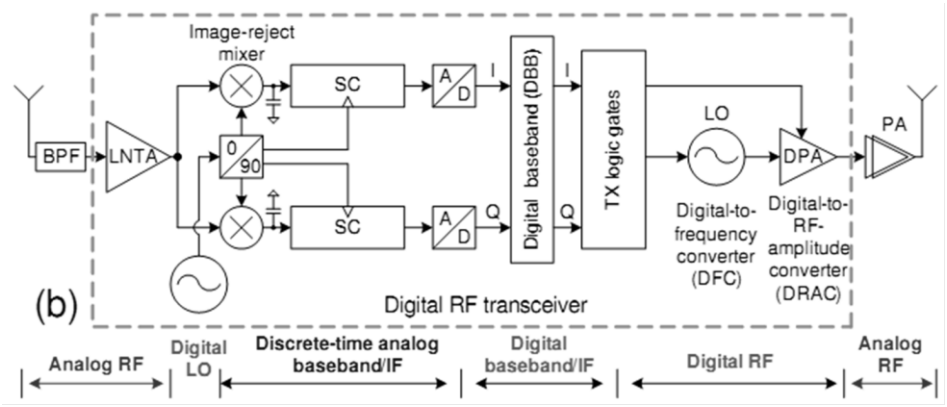


Figure 7.7: Future digital TRX [21]. ©IEEE 2012

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Publications and Presentations

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