

論文 / 著書情報
Article / Book Information

題目(和文)	アクティブマトリクス型液晶ディスプレイのための高性能多結晶Si薄膜トランジスタに関する研究 / 三村秋男
Title(English)	Study of high performance poly-silicon thin film transistors for active-matrix liquid-crystal displays
著者(和文)	三村秋男
Author(English)	
出典(和文)	学位:博士(工学), 学位授与機関:東京工業大学, 報告番号:乙第3467号, 授与年月日:2000年9月30日, 学位の種別:論文博士, 審査員:松村 正清
Citation(English)	Degree:Doctor (Engineering), Conferring organization: Tokyo Institute of Technology, Report number:乙第3467号, Conferred date:2000/9/30, Degree Type:Thesis doctor, Examiner:
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

DOCTORAL THESIS

STUDY OF HIGH PERFORMANCE
POLY-SILICON THIN FILM TRANSISTORS
FOR ACTIVE-MATRIX LIQUID-CRYSTAL DISPLAYS

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March, 2000

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PREFACE

In today's electronics industries, LSI chips and LCDs are key mass products which have become known as "rice" and "paper", respectively.

Capacity of LSI memories is increasing on a technical trend, with the mass production of 64 M bit DRAMs and the development of 128-256 M bit DRAMs. The progress in LSI chips has realized many kinds of electronic information devices and created the necessity of high performance man-machine interfaces, i.e. displays.

In LCD technologies, the main stream is made up of active-matrix (AM) LCDs which use a-Si TFTs and the main applications are for PCs. Panel size and resolution are increasing from 10.4" VGA to 15" SXGA. Viewing angle which has been a weak point of LCDs is being dramatically improved. So, monitor and TV applications to replace CRTs is a new trend and 15-30" type XGA-QUXGA panels have been successfully developed. Mother glass size has been expanded to 650x830 mm². Substrate thickness has decreased from 1.1mm to 0.7 mm to reduce panel weight. Namely, TFT technology and image quality of a-Si TFT LCDs are beginning to mature. But, a third new market of middle size panels for portable (mobile) information terminals is growing.

Thus, continuous demands for lighter, thinner, compacter, and more reliable LCDs point out the necessity of TFT technology innovation. Driver integration on higher resolution middle size LCD panels is one of the important concepts which suggests Giant-Electronics. Poly-Si TFTs have high driving ability which allows driver integration. High-performance poly-Si TFTs also create a possibility for intelligent system integration on LCD panels. Driver or system integration is indispensable in the near future not only for LCDs of mobile terminals but also for super high resolution LCDs of PCs and monitors.

In this thesis, fabrication technologies of high-performance TFTs and their applications to AM-LCDs are presented. Two major concepts of crystallization of Si films are examined experimentally. The first solid phase crystallization (SPC) is one fundamental technology. Low (600°C), middle (900°C) and high (1000°C) temperature SPC TFTs are investigated. The second technique is a melt and regrowth method. High-temperature RF zone-melting-recrystallization and 3 μ m LSI processes are utilized to realize ultimate c-TFTs and a very fine SOI-TFT-LCD for the first time. Then, low-temperature excimer laser crystallization is studied. In addition to the crystallization technologies, low energy high speed ion doping and laser activation are developed for CMOS TFTs. For gate insulator preparation, thermal oxidation (600°C), photo-CVD, and PECVD are also investigated. Then, the world's largest 18.2" TFT-LCD is fabricated. A new multi-processor is proposed for innovative continuous processes of CVD and laser crystallization. The machine offers various crystallization techniques and contributes to realize flat and large grains for future c-TFTs.

From these results, this thesis overviews the key technologies to realize the high-performance poly-Si TFTs on large glass substrates and concludes that excimer laser crystallization is a promising technology to realize high-performance low-temperature CMOS poly-Si TFTs and also ultimate c-TFTs for future system integration on panels.

ABRIVIATION

AC: Alternative Current	LCD: Liquid Crystal Display
AFM: Atomic Force Microscope	LED: Light Emitting Diode
AM: Active-Matrix	LEP: Light Emitting Polymer
APCVD: Atmospheric Pressure Chemical Vapor Deposition	LDD: Lightly Doped Drain
a-Si: Amorphous-Si	LPCVD: Low Pressure CVD
CDT: Color Display Tube	LSI: Large Scale Integration
CMOS: Complimentary Metal-Oxide-Semiconductor	MOS: Metal-Oxide-Semiconductor
COG: Chip on Glass	MBD: Molecular Beam Deposition
CPU: Computer	MBP: Mechanical Booster Pump
CRT: Cathode Ray Tube	MFC: Mass Flow Controller
CVD: Chemical Vapor Deposition	MP: Melting Point
c-Si: (Single) Crystal-Si	PALC: Plasma Addressed LC
c-TFT: Crystalline-TFT	PC: Personal Computer
CW: Continuous Wave	PDP: Plasma Display Panel
DC: Direct Current	PECVD: Plasma Enhanced CVD
DMD: Diffraction Mirror Display	p-Si: Polycrystalline-Si
DP: Dry Pump, Diffusion Pump	PSG: Phospho-Silicate-Glass
DRAM: Dynamic Random Access Memory	RF: Radio Frequency
EB: Electron Beam	PJ: Projection (Display)
EBD: Electron Beam Deposition Electron Beam Diffraction	RF-ZMR: RF-Zone Melting Recrystallization
E-E: Enhancement-Enhancement	RT: Room Temperature
ELD: Electro-Luminescent Display	RTA: Rapid Thermal Annealing
EVF: Electric View Finder	SED: Surface Conduction Electron Emission Display
FA: Furnace Annealing	SEM: Scanning Electron Microscope
FED: Field Emission Display	SIMOX: Separation by Implanted Oxide
FET: Field Effect Transistor	SIMS: Secondary Ion Mass Spectroscopy
FPD: Flat Panel Display	SIPOS: Semi-Insulating Polycrystalline Si
FT-IR: Fourier Transform Infrared Spectroscopy	SOG: Spin on Glass
GB: Grain Boundary	SOI: Silicon on Insulator
GOLDD: Gate Overlapped LDD	SOP: System on Panel
HJBT: Hetero-Junction Bipolar Transistor	SPC: Solid Phase Crystallization
HMD: Head Mount Display Helmet Mounted Display	TAB: Tape Automated Bonding
IC: Integrated Circuit	TDS: Thermal Desorption Spectroscopy
I/D: Ion Doping	TEM: Transmission Electron Microscopy
I/I: Ion Implantation	TEOS: Tetra-Ethoxy-Silane
IPS: Inductively Coupled Plasma	TFT: Thin Film Transistor
IR: Infrared	TMP: Turbo Molecular Pump
ITO: Indium Tin Oxide	TN: Twisted Nematic
LA: Laser Annealing	XRD: X-Ray Diffraction
	XPS: X-ray Photoelectron Spectroscopy
	YAG: Yttrium Aluminum Garnet

SYMBOLS (Unit)

Cadd: Additional Capacitance (pF)	NT: Trap Density ($\text{cm}^{-3} \text{eV}^{-1}$)
Cgs: Gate-Source Capacitance (pF)	s: Threshold Factor (A/decay)
Cox: Gate Oxide Capacitance (pF)	t: Time (s)
Cstg: Storage Capacitance (pF)	tp: Poly-Si Thickness (nm)
Dit: Interface Trap Density ($\text{cm}^{-2} \text{eV}^{-1}$)	T: Temperature ($^{\circ}\text{C}$)
Ea: Activation Laser Energy (mJ/cm^2)	Ta: Anode Electrode Temperature ($^{\circ}\text{C}$)
Ec: Crystallization Laser Energy (mJ/cm^2)	Tc: Cathode Electrode Temperature ($^{\circ}\text{C}$)
Id: Drain Current (A)	VDD: Supply Voltage (V)
IDD: Driving Current (A)	VFB: Flat Band Voltage (V)
IOFF: Off-Current (A)	VG: Gate Voltage (V)
ION: On-Current (A)	VIN: Input Voltage (V)
L: Channel Length (μm)	VOUT: Output Voltage (V)
μFE : Field-Effect Mobility (cm^2/Vs)	VTH: Threshold Voltage (V)
NFB: Flat Band Concentration (cm^{-2})	W: Channel Width (μm)

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Introduction

In this chapter, first, the importance of single crystal MOS LSI devices and thin film transistor liquid-crystal displays (TFT-LCDs) is introduced. Then, application fields of poly-Si films to active and passive devices are overviewed. Next, structures and operation principles of LCDs, structures of TFTs, operation characteristics of TFTs, and demands for low-temperature poly-Si TFTs, are summarized. Finally, purposes and an outline of this thesis are presented.

1.1 Outline of applications of poly-Si films and TFTs to electronic devices

1.1.1 LSI chips and displays

It is noteworthy that the present commercially successful MOS LSI technologies have originated from trial and error development of polycrystalline TFT fabrication [1]. The principle structures of the TFT were patented by Lilienfeld in 1925 and Heil in 1935. Basic operations of TFTs were observed by Shockley and Pearson using evaporated Ge film in 1948. Improved CdS TFTs were studied by Weimer in 1962, and then applications of TFTs to memories and image sensors were proposed. These studies of TFTs led to the inventions of the point contact transistor and bipolar transistor. Later, the planar technology which uses the native oxide of Si substrate promoted development of MOS transistors. These surface engineering applications have also contributed to the improved TFT performance of today.

Nowadays, MOS LSI chips fabricated on single crystal Si wafers are typical electronic products. 64 M bit DRAMs (0.25 μm device) are mass produced and 128-256 M bit devices (0.18 μm) have been developed. Possibility of fabrication of very fine n-MOS FETs with gate length of 0.1-0.014 μm has already been confirmed [2]. Si wafer size is now 8" and technologies for next generation 12" wafers have been developed as a standard. Progress with these LSI devices continues.

The evolution of MOS LSI devices has dramatically contributed to miniaturization, improvement of operation speed and reliability, and cost reduction of electronic equipment. Huge amounts of information are now treated by electronic equipment which requires high-performance man-

machine interfaces. Of the human's five senses, eyesight is the most useful means to understand supplied information, assisted by hearing, and other senses. Therefore, the most effective man-machine interface is a visual display.

1.1.2 Poly-Si devices

Poly-Si has long been a raw material for single crystal Si wafers. But recently, it is also being widely applied to active and passive electronic devices.

Fig. 1.1 relates the fabrication methods of poly-Si films, temperature classification of device processes, and applications of poly-Si films. Example typical applications of poly-Si films to electronic devices are shown in Fig. 1.2. As passive applications, typical ones are as gate electrodes and resistors of MOS LSI devices ((a)). In the dielectric isolation of high voltage power ICs, thick poly-Si films are used for substrates ((b)) [3]-[6]. Semi-insulating poly-Si film (SIPOS) with high resistivity is applied to very high voltage planar devices for highly reliable passivation films ((c)) [7]-[10] and low leakage current poly-Si TFTs [11]. Poly-Si films are also applied as the emitter of a heterojunction bipolar transistor (HJBT) [12], emitter of a field emission display (FED) [13], resistors of sensors [14], and micro-machines [15], etc.

As active applications, typical ones are TFTs for LCDs as discussed in this thesis. TFT arrays are also used to drive ELDs. Low temperature poly-Si TFTs are fabricated by laser crystallization. High temperature poly-Si TFTs are produced by solid-phase crystallization (SPC) on quartz substrates. Single crystal Si film (c-Si) for SOI TFTs is converted from poly-Si by zone-melting. The load MOSFET of an SRAM uses a poly-Si active layer ((a)) [16]. Poly-Si type solar cells will be indispensable in the near future from the viewpoint of the environment ((d)). The line image sensor [17], plane X-ray sensor, and light shutter array for printers [18] all use poly-Si TFT drivers on transparent insulating substrates.

Thus, poly-Si films and TFTs take very important roles in today's electronic industries. In this thesis, development of high-performance poly-Si TFTs and SOI TFTs (c-TFTs) for AM-LCDs is presented.

1.2 State of the art and technical trends of AM-LCDs

1.2.1 Overview of flat panel displays

A digital multi-media era is coming for which high-performance displays are indispensable as man-machine interfaces. The cathode ray tube (CRT) which was invented by Braun 100 years ago, is continuing to evolve for high resolution color data display tubes (CDTs), high definition television (HDTV), and large size, wide TVs. Conventional color picture tubes (CPTs) will continue to be the most important display for daily use in developing countries.

Flat panel displays (FPDs) are recent innovative products and various kinds of them are being developed across application fields.

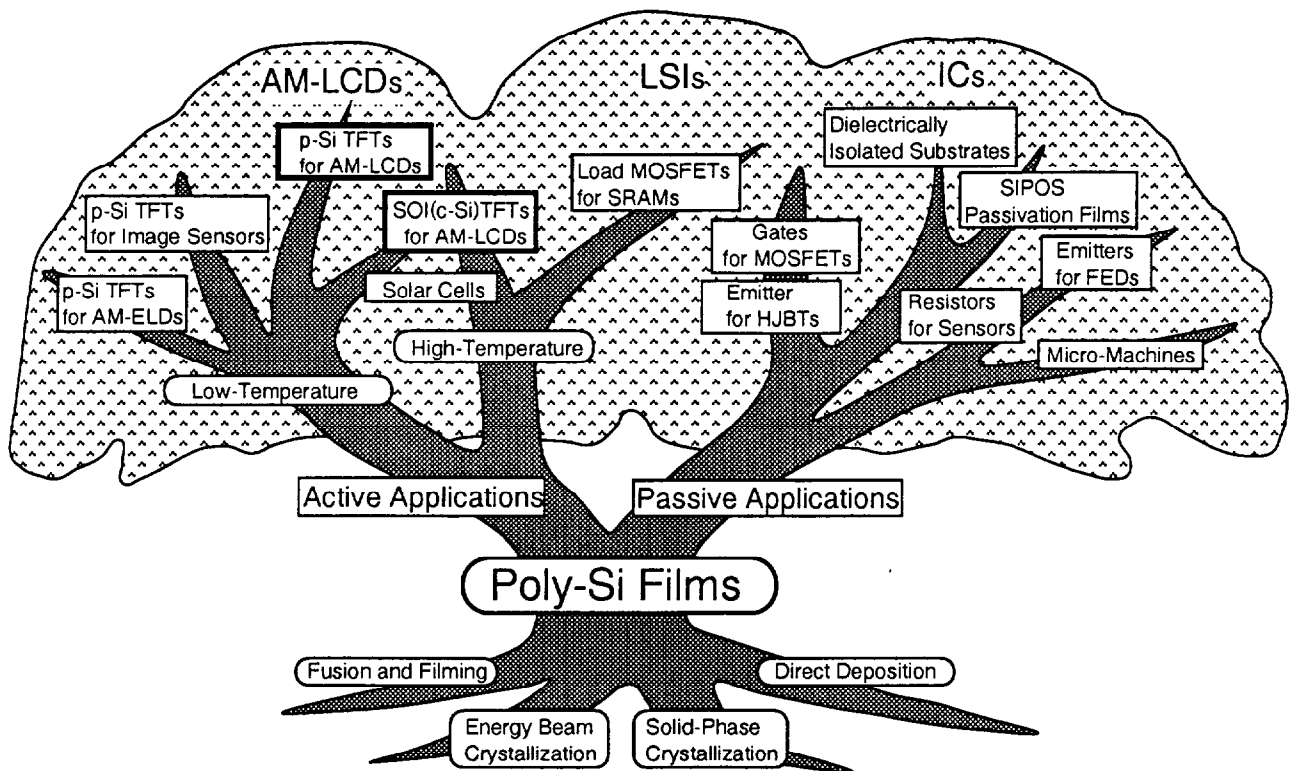


Fig. 1.1. Poly-Si tree.

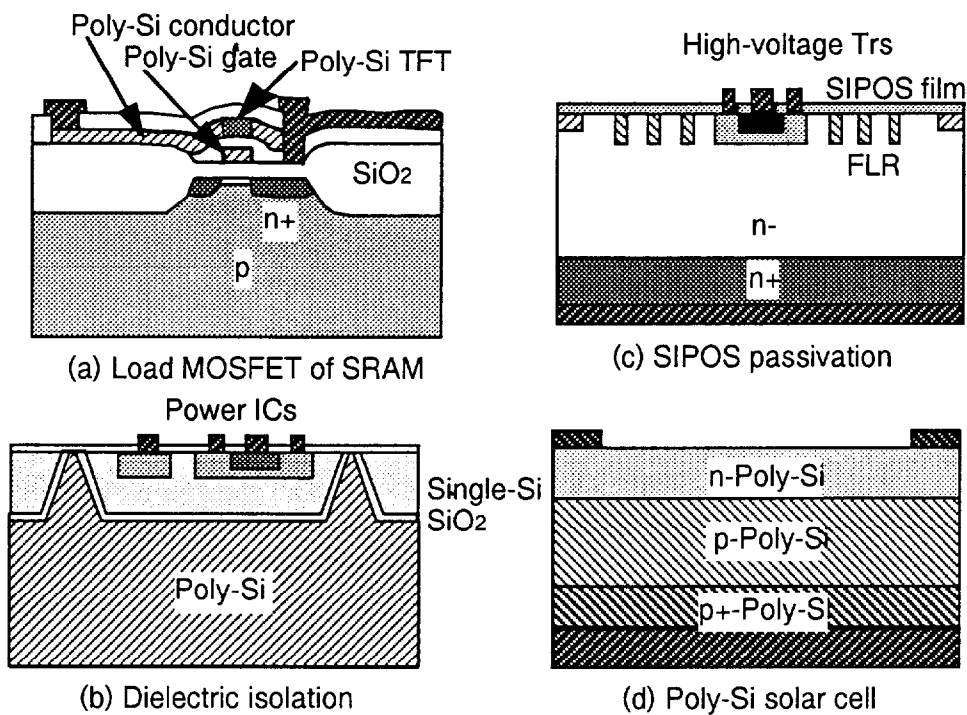


Fig. 1.2. Example applications of poly-Si to electronic devices.

Plasma display panels (PDPs) are a self-emissive type with possibilities of full color and wide viewing angle presentation. But they need a high driving power, such as 300W and 400W for AC and DC discharge types in a 42" panel, respectively. They are produced by a simple thick film printing process. Large area (25-60") PDPs have been developed for monitors and wall TVs.

Field emission displays (FEDs) are also self-emissive and they have a wide viewing angle. Cone emitter types need fine processing. Among them, the surface conduction electron emitter (SED) type has a planar structure and a 10-30" panel has been fabricated. A carbon nanotube emitter is expected to reduce extraction voltage from 5-6kV to 1kV.

Plasma addressed LC (PALC) displays are constructed by the combination of an LC cell for a light shutter and a plasma discharge matrix which supplies the driving voltage of the LC cell. The plasma discharge matrix is made by the same thick film printing method as the PDP. A large panel (42") has been developed.

Electroluminescent displays (ELDs) are all solid state displays. Middle size panels are used for factory and office machines. Recently, a light emitting polymer (LEP) was developed and a 10" panel was fabricated. An application to light and flexible displays is expected. Combination of the LPE and poly-Si TFT array is a new technology trend.

Light emitting diode (LED) arrays are being applied to outdoor traffic signals and public large area (100") displays since bright blue and green LEDs are now available in addition to conventional red, yellow green and yellow LEDs.

AM-LCDs have a history of 25 years and are typical FPDs of today because of their thin, compact, and low power consumption features. Recently, AM-LCDs have made great progress in resolution and image quality. The combination of a low-temperature poly-Si TFT array and reflective mode LC is a new approach for mobile equipment with very low power consumption. The LCD market size is expected to be comparable to that of CRTs within the next few years.

1.2.2 Principle of LC cell operation

General materials have three phases, solid, liquid, and gas. A LC material is an organic rod-like molecule which has an intermediate state between a solid and a liquid. It shows both crystal-like and liquid-like properties simultaneously in the proper temperature range. The basic behavior was discovered in 1888 by Reinitzer in specific ether compounds. The behavior originated from the orientated arrangement of the molecules. Therefore, the LC material is dielectric anisotropic which gives rise to its electro-optical characteristics. The twisted nematic (TN) mode is a fundamental presentation of this.

Fig. 1.3 illustrates the operation principle of the TN mode normally-on (-white) type liquid crystal cell. The cell consists of one set of glass substrates coated with polarizers, transparent electrodes and alignment

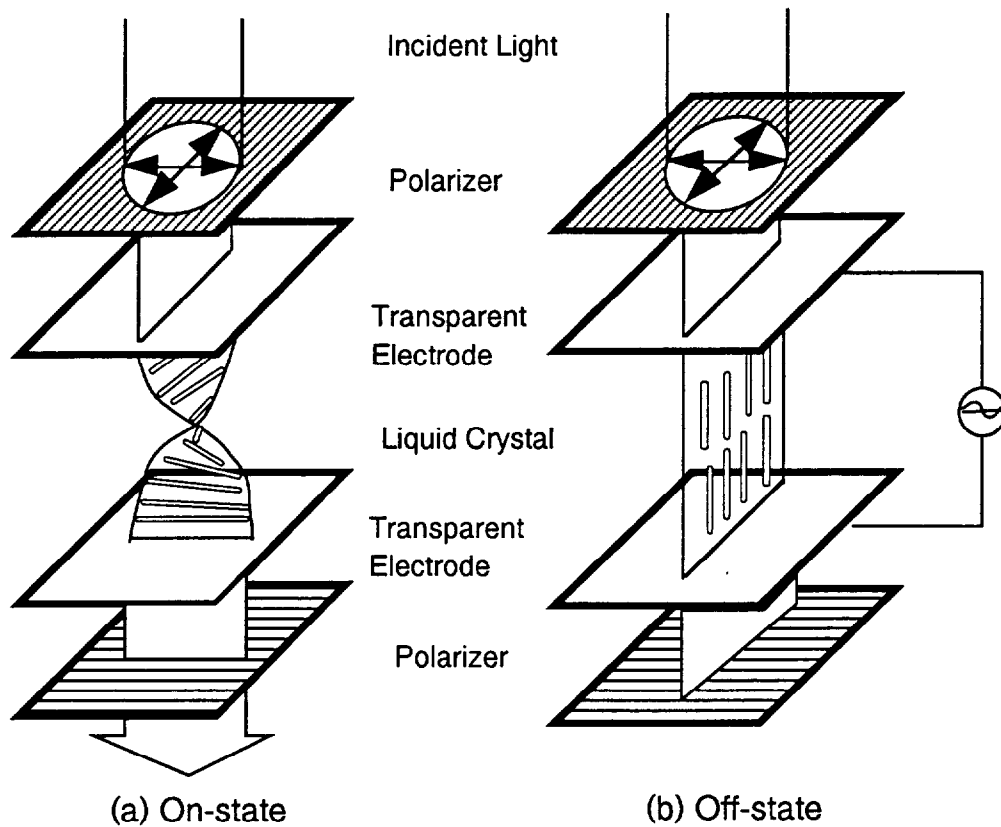


Fig. 1.3. Operation principle of normally-on type TN-cell.

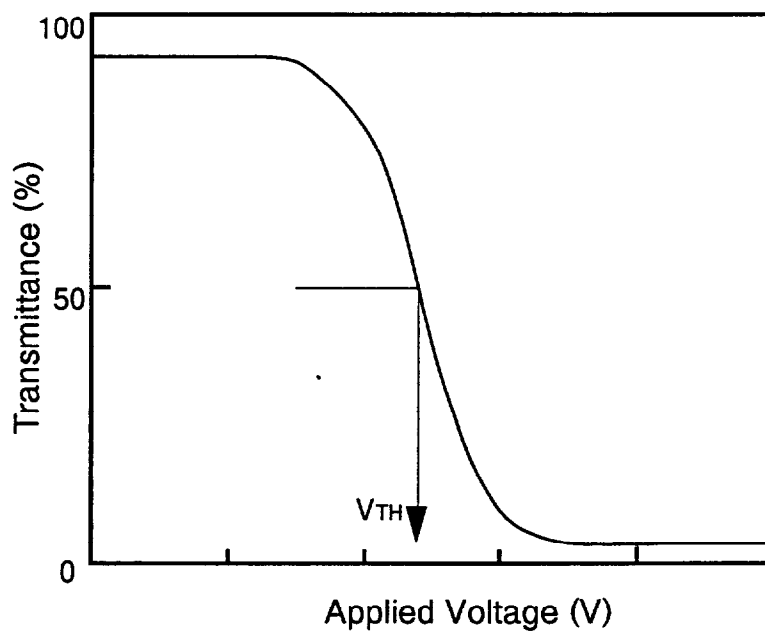


Fig. 1.4. Transmittance-voltage characteristics of TN-LCD with normally-on mode.

layers. TN LC materials are filled between the layers to a thickness of several microns. Two polarizer orientations and alignment directions are set perpendicular to each other. In the on-state of Fig.1.3(a), voltage is not applied between the two transparent electrodes and the LC is twisted 90 degrees between the two alignment layers. Therefore, polarized light is rotated 90 degrees in the LC layer and transmitted from the opposite side polarizer. In the off-state (Fig. 1.3(b)), AC voltage is applied between the two transparent electrodes and LC molecules are oriented parallel to the applied electric field, perpendicular to the polarizer. The polarized light is not rotated in the LC layer and it is cut off at opposite side polarizer. The normally-off (-black) type LC cells can be obtained by setting a pair of polarizers and alignment layers parallel to each other.

Fig. 1.4 illustrates the transmittance-voltage characteristics of TN-LCD with the normally-on mode. By increasing applied voltage, the LC cell shift from on-state to off-state as shown in Fig. 1.3, and transmittance decreases. Applied voltage at 50 % transmittance is defined as threshold voltage (V_{TH}) of LC cell. Ratio of transmittances of on-state and off-state is defined as contrast ratio.

1.2.3 Principle of simple matrix LCD

There are two fundamental cell structures, segment and matrix types. Segment types are used for small capacity displays such as electric calculators and watches. Matrix types are widely used for much larger capacity displays such as data displays and TVs. The matrix LCDs are also classified into two types, simple matrix (passive matrix) and active matrix types.

Figs. 1.5 and 1.6 show a the side view and an electrical circuit model for a simple matrix LCD. A pair of glass substrates with striped transparent electrodes and alignment layers are assembled face to face and TN liquid crystals are used between them. In the image presentation, the horizontal (row: X axis) electrodes are scanned from the top to the bottom and selected successively. For example, when the dots (2,1) and (3,2) are selected, first, the first row line and the second vertical (column: Y axis) electrode are selected simultaneously, then the second row electrode and third column electrode are selected simultaneously, and so on. When color presentation is necessary, color filters are attached on the inside of one glass substrate. This display structure is simple and production cost is moderate. But there is a serious problem in image quality, which is a low contrast ratio due to cross-talk. When the number of row lines is increased in a high resolution display, selection time is decreased and an insufficient voltage is applied to the selected dot. All electrodes are connected together and a small voltage is added to the non-selected dot. There are improvements for LC materials and driving methods. But this structure is applied only to super twisted nematic (STN) and ferro-electric LC displays.

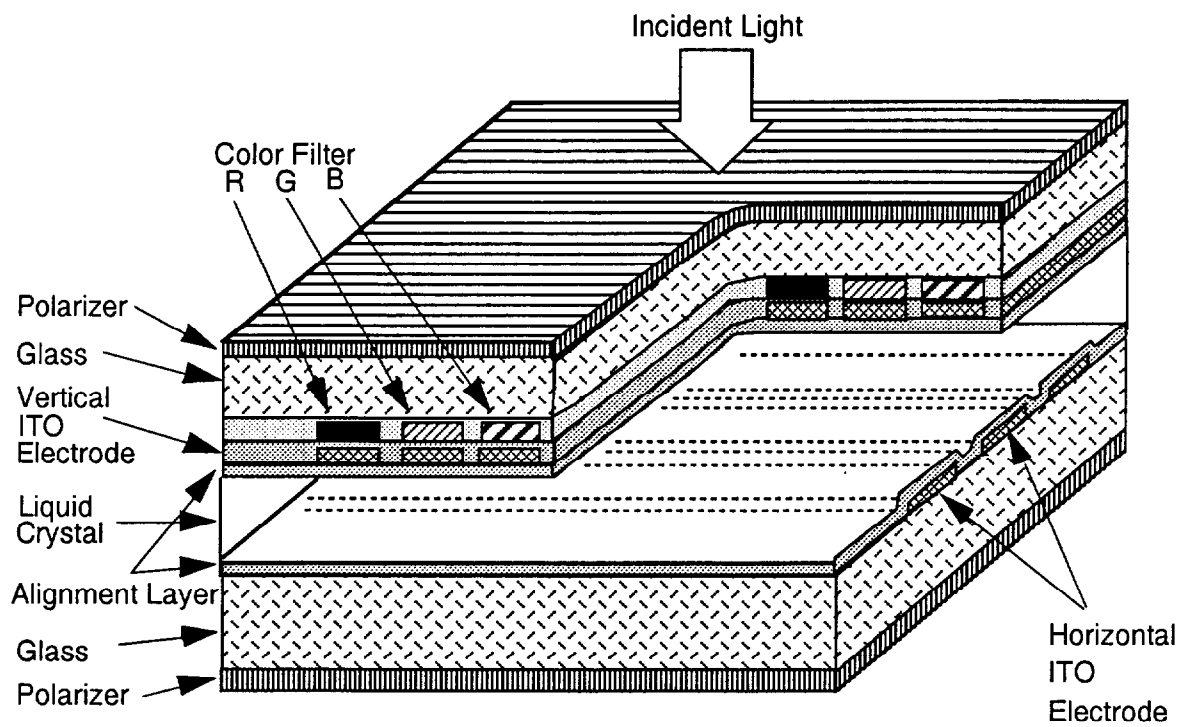


Fig. 1.5. Side view of simple matrix LCD.

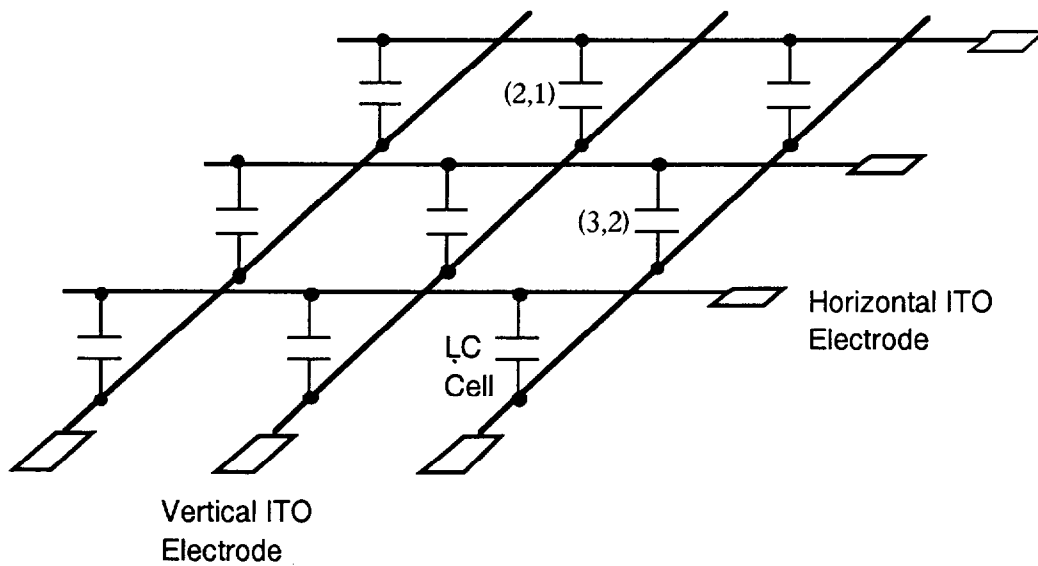


Fig. 1.6. Electrical circuit model for simple matrix LCD.

1.2.4 Principle of AM-LCD

The main LCD structure in use today is the active matrix type which has active devices at every pixel to switch the applied voltage independently and completely. Figs. 1.7 and 1.8 show a schematic side view and a circuit model of the TFT type AM-LCD. The upper glass substrate is coated with a polarizer. There are a color filter, common transparent electrode (indium tin oxide: ITO), and alignment layer. On the lower substrate, there are a polarizer, TFTs with gate line and drain line, pixel ITO, and alignment layer. TN-LC material is filled between the two substrates. Polarizer axes are perpendicular to each other. Each pixel TFT is switched independently by scanning the gate line and applying a signal voltage from a finite data line. Without a signal voltage, the pixel is in the on-state as shown in Fig. 1.3(a). When a signal voltage is applied between the pixel electrode and common ITO, the pixel is in the off-state (Fig. 1.3(b)). Applied signal voltage is kept until the next frame by switching off the TFT by removing the gate voltage.

Therefore, the image quality depends on performance of TFTs. If an ideal transistor with a very high on-current and very low off-current is available, short time charge-up of the pixel and long time holding of signal voltage become possible. Thus, a very large scale AM-LCD with super high resolution could be realized.

1.2.5 History of AM-LCDs

An application of TFTs to LCDs was proposed in 1971 by Lechner et al. [19], after various studies of TFTs having the goal of realizing semiconductor ICs. The first AM-LCD was experimentally studied by Brody et al. [20] in 1973 using CdSe TFTs and TN LCs. This compound semiconductor film is easily made by evaporation and mobility is large [21]. But its poor stability and toxicity obstructed future development. Plasma enhanced chemical vapor deposition (PECVD) technology which was developed for thin film solar cells, could be used for film deposition of semiconductor Si and insulator. Then, epoch making technologies, substitutional impurity doping to a-Si by Spear and LeComber [22] and fabrication of a-Si TFTs by LeComber et al. [23], build the foundation of a-Si TFT AM-LCDs of today.

Generally, a-Si TFTs are fabricated by continuous plasma CVD of SiN, intrinsic a-Si, and doped a-Si films at about 300°C, which is sufficiently low to use mass-produced glass substrates. Such a simple and low temperature fabrication process promoted the mass production of a-Si TFT-LCDs. Recently in 1997, substrate size was expanded to 650mm x 830mm with a thickness of 0.7 mm. Maximum panel size and resolution reached 30" (UXGA) and QUXGA (20"), respectively.

The first poly-Si TFTs were fabricated on an oxide of Si-wafers and quartz substrates by using LSI high-temperature processes above 900°C [24], [25]. A 1.51" TFT-LCD with scan and data driver integration was fabricated by SPC [26] and a 3" TFT-LCD was also fabricated by laser

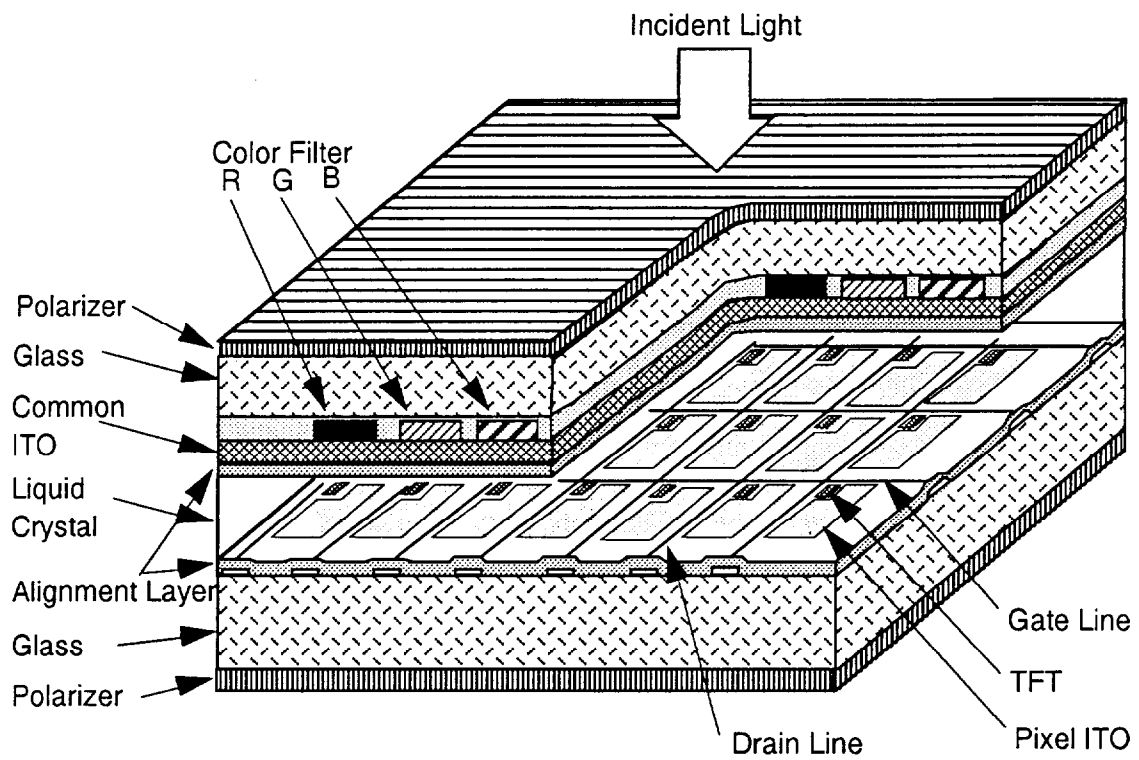


Fig. 1.7. Side view of AM-LCD.

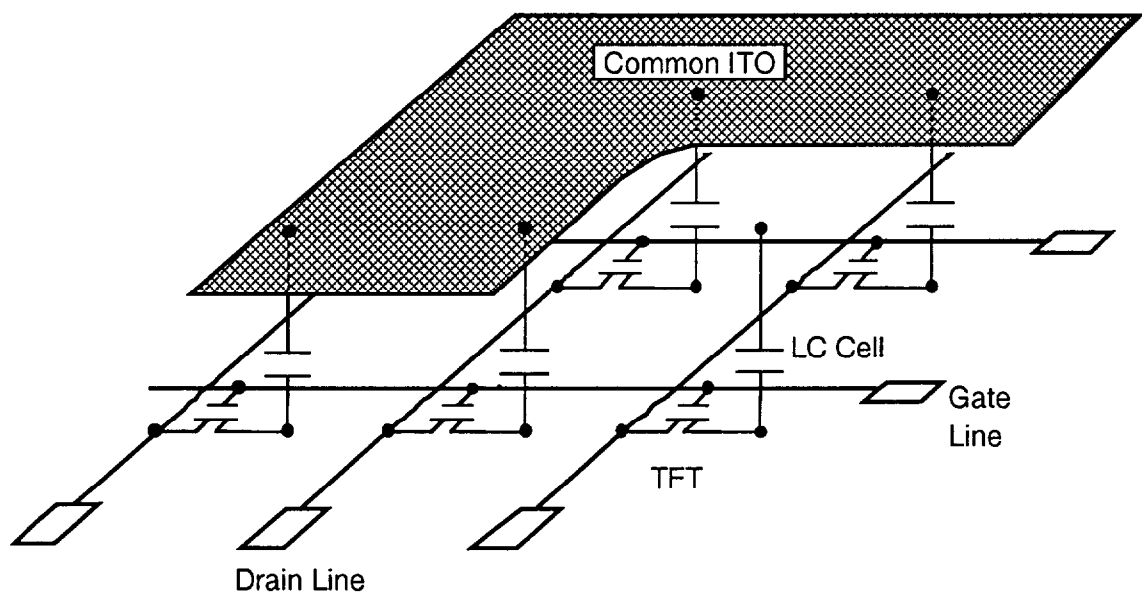


Fig. 1.8. Electrical circuit model for AM-LCD.

crystallization [27]. These fabrications have become the foundation for very fine high-temperature poly-Si TFT-LCDs for electronic view finders (EVF), projector (PJ) engines and head mount displays (HMDs).

The first poly-Si TFTs on glass substrates were fabricated by Matsui et al. [28] in 1980 using a low-temperature process below 600°C and molecular beam deposition (MBD) of Si film. Then, a 10x10 matrix TFT-LCD was fabricated [29]. Small size TFT-LCDs were reported by using low temperature SPC [26] and electron-gun-evaporated Si films [30]. Low temperature poly-Si TFT technology has moved on to high quality SPC and laser crystallization.

To simplify the fabrication process of switching devices, bi-terminal devices such as the diode [31], diode ring [32], metal-insulator-metal (MIM) [33] have also been proposed. They are applied to middle size LCDs. From the viewpoint of super fine LCDs, reflective panels with driver integration on the Si substrate by the LSI process are proposed such as NCAP MOS [34], digital mirror display (DMD) [35], and Si chip based LCD [36] or liquid crystal on silicon (LCOS). The minimum size is 0.24" and these miniature LCDs should be indispensable for watch TVs, HMDs and wearable CPUs in the future.

1.2.6 Application fields of TFT-LCDs

Fig.1.9 shows application fields of TFT-LCDs. Main products of a-Si TFTs are large panels for portable PCs. Panel size and resolution are increasing from 10.4" to 14.1" and from VGA to SXGA, respectively. Larger size monitors are a recent new application. Panel size and resolution are 15-30" and XGA-QUXGA, respectively. There will be a limitation of size of TFT-LCDs. A tile TFT-LCD is one means to realize larger size TFT-LCDs than 30" diagonal. A 40" TFT-LCD was fabricated successfully by connecting two 29" panels [37]. Middle size panels (2-8") are applied to portable (mobile) communicators such as digital video cameras, personal data assistants (PDAs) and car navigators. Reflective mode is expected to be suited to mobile use because of its very low power consumption. Very small size panels (0.5-1.4") are applied to PJ engines, EVFs and HMDs.

Small size panels are produced by high-temperature poly-Si TFTs on 6-8" quartz wafers. Some middle size TFT-LCDs (2-10") are produced using low-temperature poly-Si TFTs [38], [39]. Low-temperature poly-Si TFTs are now expected to realize compacter, thinner, and lower cost displays for high resolution panels for PCs and monitors by driver integration [40] as well as middle size LCDs for mobile communicators.

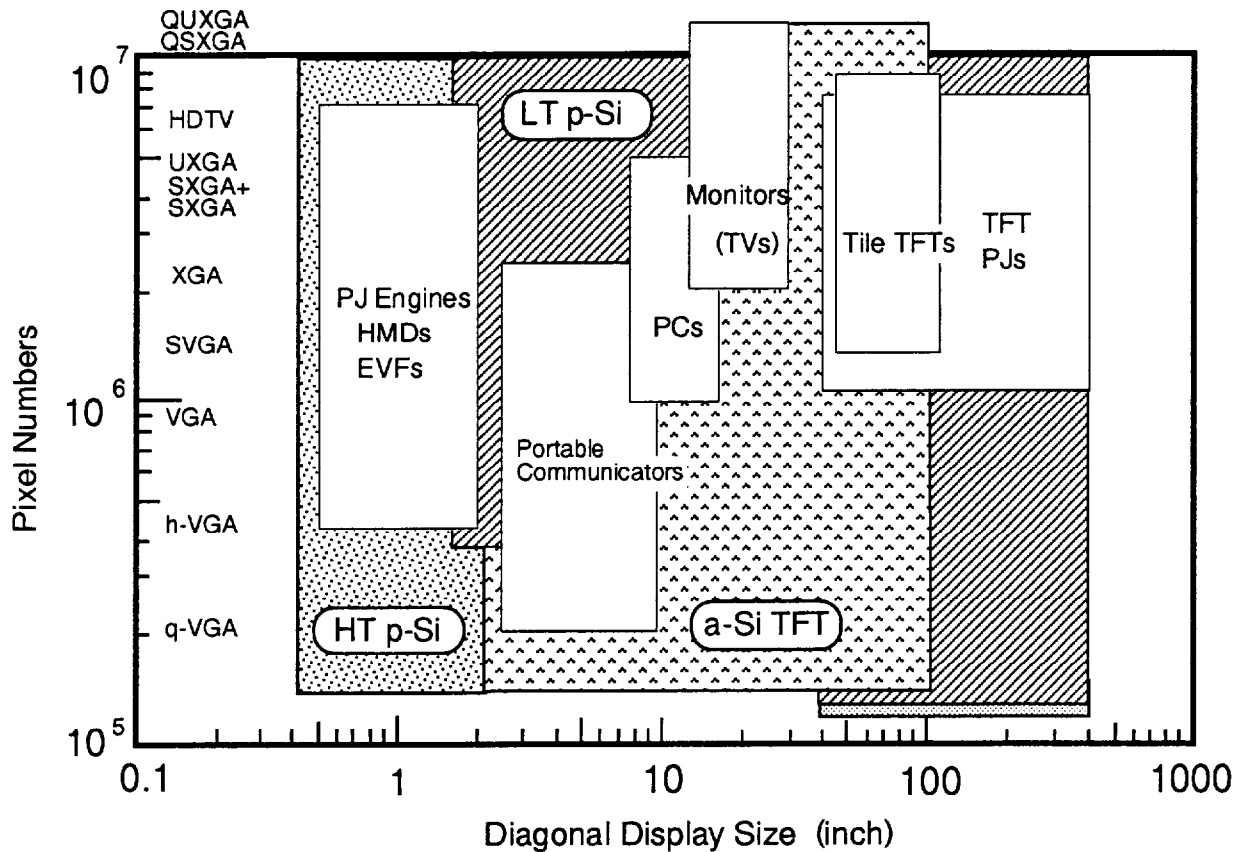


Fig. 1.9. Application fields of TFT-LCDs.

1.3 TFT technologies in AM-LCDs

1.3.1 Structures and operation characteristics of TFTs

Fig.1.10 illustrates typical structures of TFT-LCDs. Fig.1.10(a) is a typical a-Si TFT-LCD. Fig.1.10(b) is a recent a-Si TFT-LCD with in-plane switching (IPS) mode for wide viewing angle [41]. A common electrode is placed on the TFT substrate to apply a horizontal electric field between the source and common electrodes. Fig.1.10(c) is a coplanar type TFT-LCD like high-temperature and low-temperature poly-Si TFTs. Fig.1.10(d) is an example of a reflective mode AM-LCD with metal reflector.

Fig. 1.11 shows various TFT structures developed for AM-LCDs. Reversed stagger type (a) is a fundamental a-Si TFT structure which is fabricated by continuous CVD of gate insulator SiN, active layer intrinsic a-Si, and doped n-type a-Si. This structure is also used in recent low-temperature poly-Si TFT-LCDs [38], [39]. Stagger type (b) is also used for both a-Si and poly-Si TFTs. This basic structure can be fabricated by a two-step patterning process using an ITO for drain and pixel electrodes and it is applied to small size TFT-LCDs [42]. The vertical type TFT (c) realizes a short channel a-Si TFT [43]. Coplanar type (d) come from the MOS FET on bulk Si and is fundamental for low-temperature and high-temperature poly-Si TFTs. It is suitable for fabricating high performance CMOS TFTs.

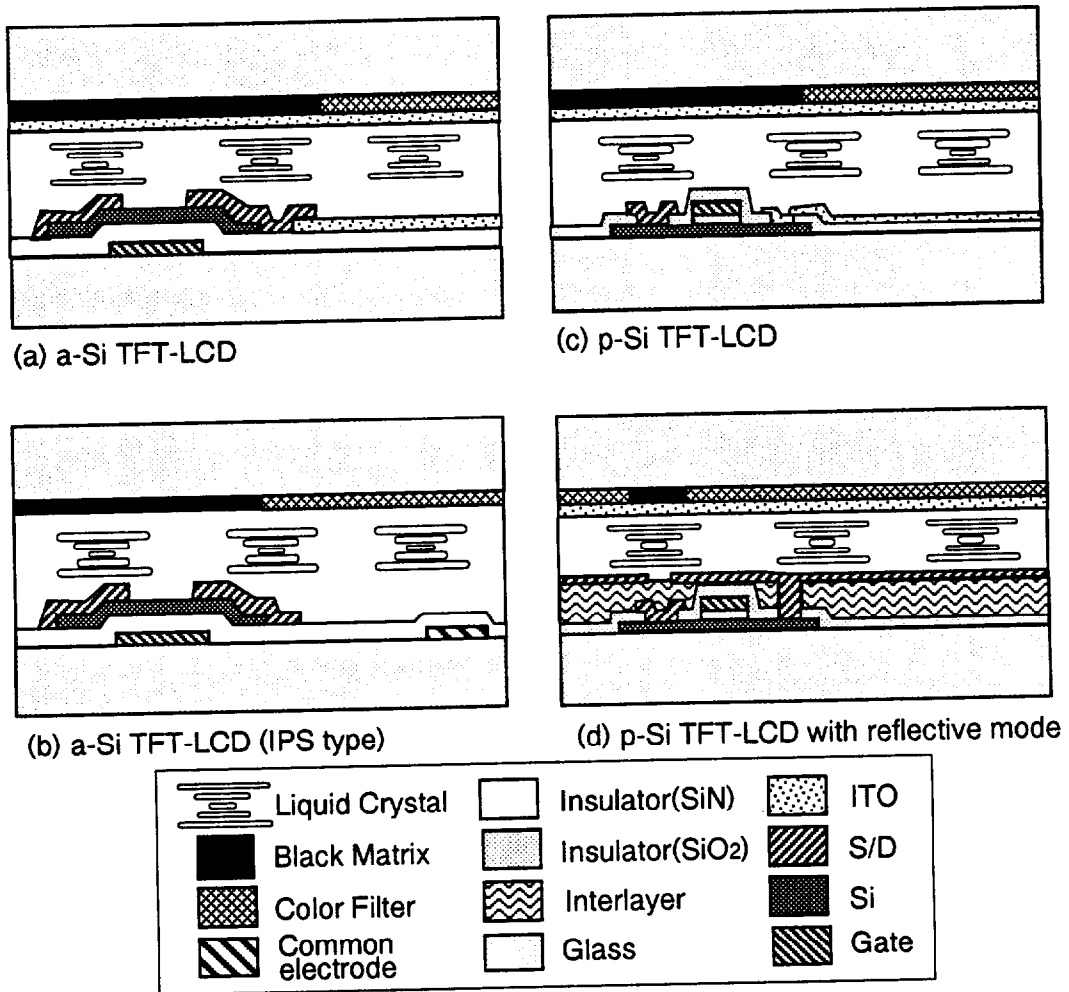


Fig.1.10. Typical structures of TFT-LCDs.

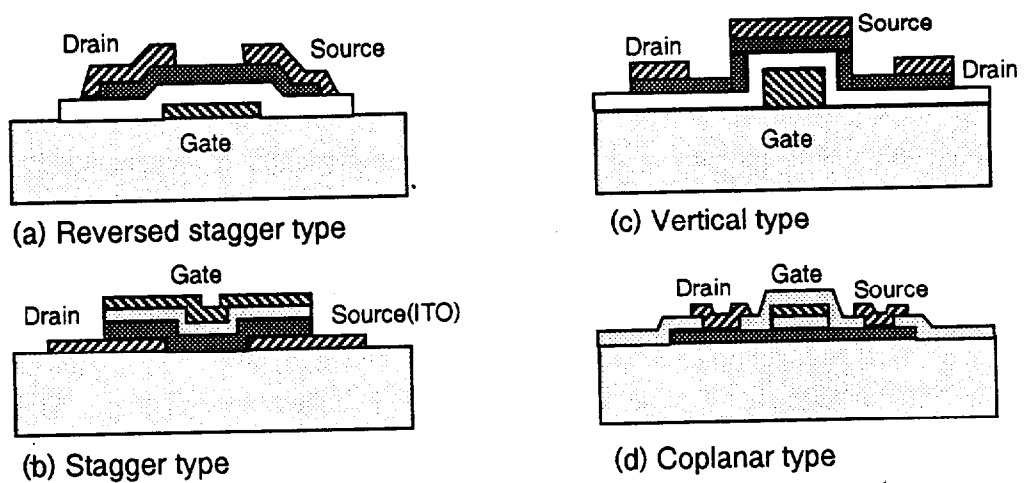


Fig. 1.11. Typical structures of TFTs.

Fig.1.12(a) illustrates typical operation characteristics, gate voltage (V_G)-drain current (I_D) curves of a-Si, poly-Si and SOI (c-Si) TFTs. These TFTs operate according to MOS theory. Important basic performance characteristics of TFTs are on-current, sub-threshold characteristics such as V_{TH} , and off-current. An a-Si TFT fabricated by glow discharge CVD has low carrier mobility and low on-current. But it has steep sub-threshold characteristics because of low localized gap states in the bulk a-Si and low surface states at the interface of a-Si and insulator SiN. It also has low off-current because of the serial intrinsic a-Si off-set structure in the drain. If an SOI TFT is fabricated by a high-temperature LSI process using the pn junction, it should show ideal characteristics with high on-current, low V_{TH} , and low off-current. Poly-Si film has higher crystallinity than a-Si film, but also a high density of states at grain boundaries. Therefore, it shows high on-current and also high V_{TH} and high off-current which originates from the field emission current through deep level states. Thus, performance of poly-Si TFT critically depends on the film quality of gate insulator and poly-Si. Fig. 1.12(b) shows example curves of p-channel and n-channel TFTs for CMOS configuration. Balance of each V_{TH} is important for ideal operation of inverters.

1.3.2 TFT technology trend

Fig.1.13 relates the field effect mobility and process temperature for various TFTs. The a-Si TFT is the main stream device of today's AM-LCDs. The maximum process temperature is about 300 °C and field effect mobility is improving [44]. Solid-phase crystallization (SPC) is a fundamental technology to obtain high quality poly-Si films. High-temperature (HT)-SPC using quartz substrate is already applied to the production of very fine poly-Si TFT-LCDs (0.5"-1.4") using the LSI process. Mobility of HT-SPC is improved by using Si_2H_6 CVD and two-step temperature SPC [45], and combination of SPC and laser recrystallization [46].

Low-temperature SPC using glass substrates is a new stage of development. To realize high performance poly-Si TFTs on large glass substrate, SPC at 600°C is studied in this thesis as presented in Chapter 2. Middle temperature (MT) SPC (900°C) is a possible process to use with the large size quartz substrate which was developed for photolithographic mask substrates larger than 300mm x 300mm. The MT-SPC process also refers to basic LT-SPC technologies and it is proposed in Chapter 3. Thus, the basic concept of LT-SPC is applied to both MT-SPC and HT-SPC to improve performances of TFTs.

Melt and regrowth method is another promising technique to achieve very high performance TFTs. Floating zone (FZ)-melting is a conventional crystallization method to produce a single crystal rod for LSI devices. The film zone-melting method is applied to crystallize poly-Si films into single crystal Si (c-Si) films on the insulating substrates. The high quality SOI has high mobility comparable to bulk Si and sufficient

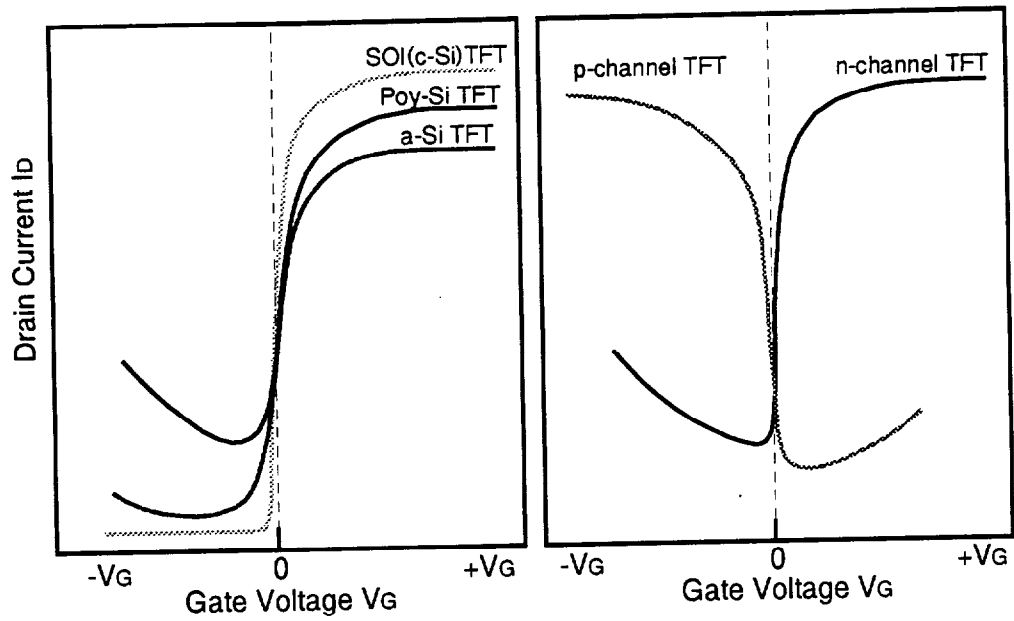


Fig.1.12. Typical gate voltage-drain current characteristics of TFTs.

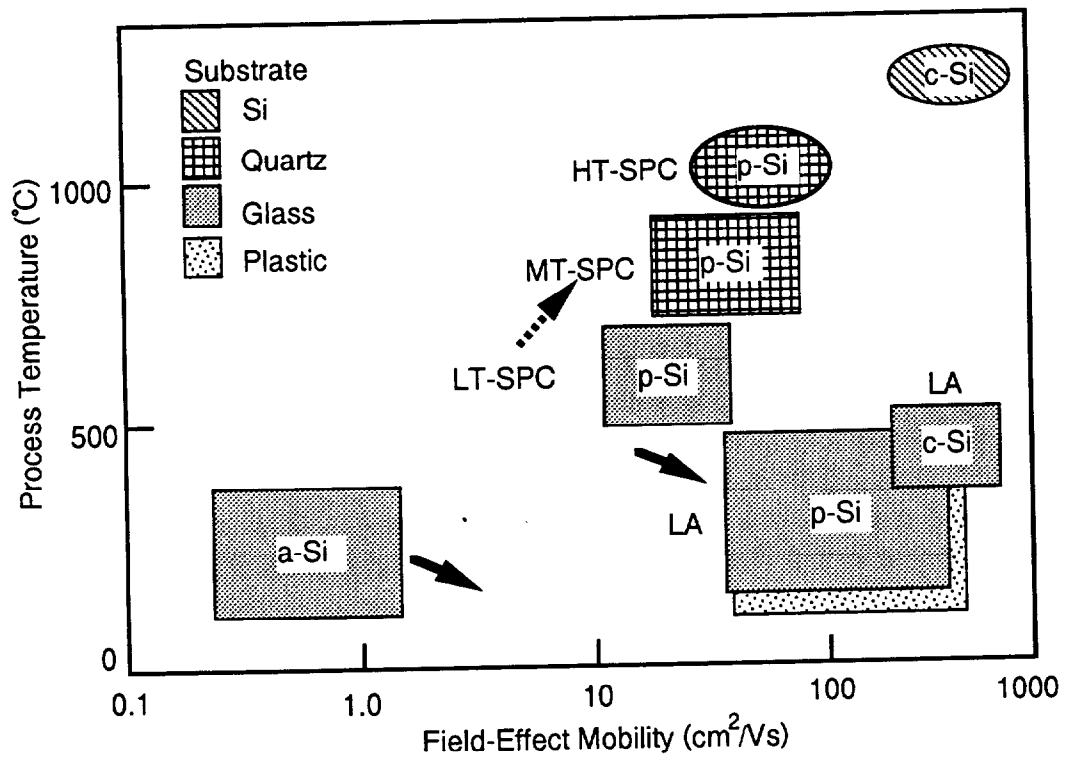


Fig. 1.13. Process temperature and field-effect mobility of TFTs

potential to realize very fine SOI-TFT LCDs with driver integration using the LSI process as shown in Chapter 4.

Laser crystallization is another technique of melt and regrowth and recent current technologies are shown in Chapters 5, 7 and 8. High performance TFTs are fabricated at temperatures of 350-450 °C which are almost comparable to those of a-Si TFTs. Laser crystallization technology should have a potential to realize c-Si TFTs on plastic substrates as well as on glass substrates [47].

1.4 Demands for poly-Si TFTs

1.4.1 Operation of pixel TFT

Demands for poly-Si TFTs are examined considering the fundamental operation of pixel TFTs in high resolution AM-LCDs, and inverters which are basic components of integrated peripheral drivers.

Fig.1.14 illustrates the equivalent circuit model of one pixel of a TFT-LCD. A pixel consists of TFT, LC cell, and additional capacitance C_{add} . The LC cell is shown as a equivalent circuit with parallelly combined capacitance of LC and resistance of LC. To achieve high contrast images, a sufficient signal voltage V_S must be kept. Additional capacitance C_{add} supports holding the applied V_S , which is reduced by leakage current through R_{TFT} and R_{LC} . In TFT switching, the V_S is affected by gate-source capacitance C_{GS} .

Fig. 1.15 shows a driving timing chart for one frame and waveforms of pixel voltage V_S . Subscripts H and L indicate maximum and minimum voltages of V_D and V_G , respectively. t_L , f_L and V_{sig} are address time, frame frequency, and signal voltage for LC cell, respectively. In the waveform of V_S , there are transient voltage changes V_{GS1} and V_{GS2} at switching timing of V_g . V_{GS1} and V_{GS2} depend on C_{GS} and give rise to unbalance of V_{sig} and image sticking in LCDs. V_{GS1} or V_{GS2} are reduced by C_{add} as follows,

$$V_{SG1} = V_{SG2} = C_{GS} / (C_{GS} + C_{LC} + C_{add})(V_{GH} - V_{GL}).$$

Thus, low C_{GS} is also indispensable to reduce V_{GS} and area of C_{add} . For pixel TFTs in high resolution AM-LCDs, high on-current is necessary for charging in a short address time, and low off-current is also necessary for keeping signal voltage in one frame time t_f . A small size TFT is suitable to obtain a high aperture ratio. Therefore, a high performance self-aligned coplanar TFT of small size is reasonable.

1.4.2 Operation of inverters for driver circuits

Fig.1.16 shows example inverters and basic operation characteristics. Primitive enhancement and enhancement (E-E) inverters consist of a set of the same polar TFTs such as n-channel TFTs. Output voltage is controlled by the ratio of channel resistances of two TFTs. Therefore, the

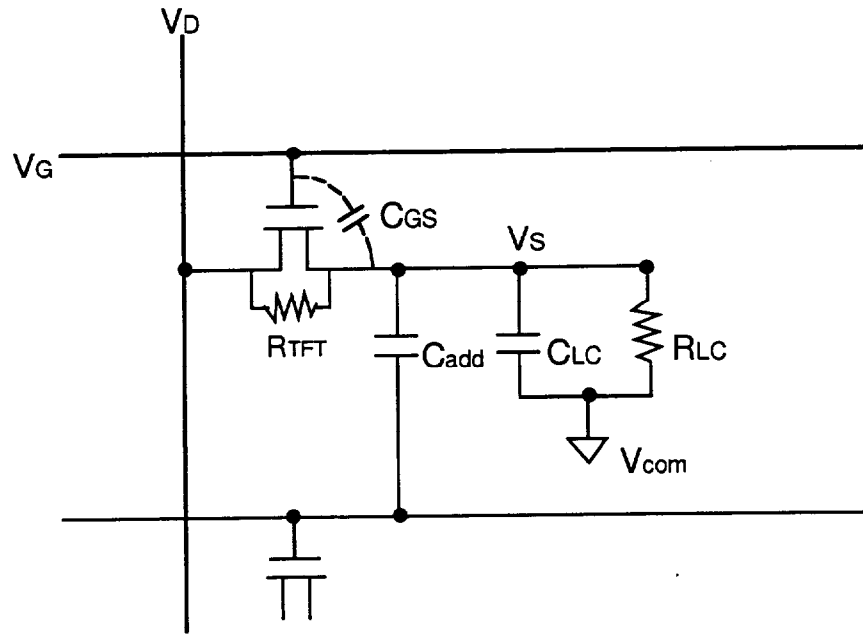
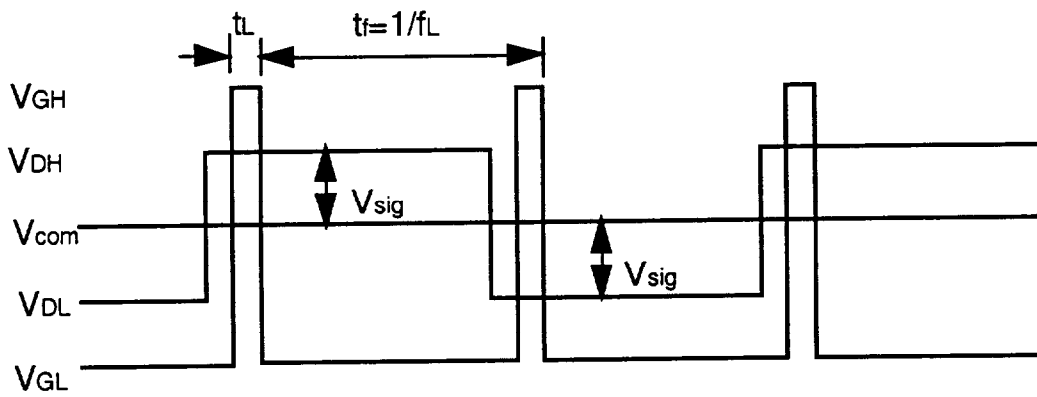
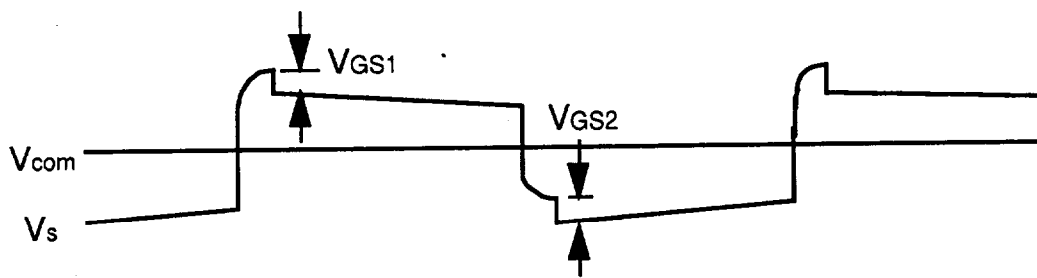


Fig. 1.14. Equivalent circuit model of one pixel.

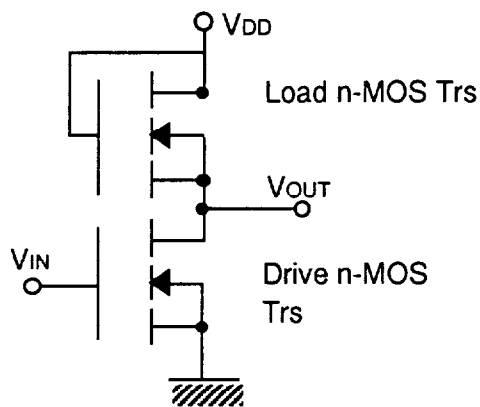


(a) Driving waveform

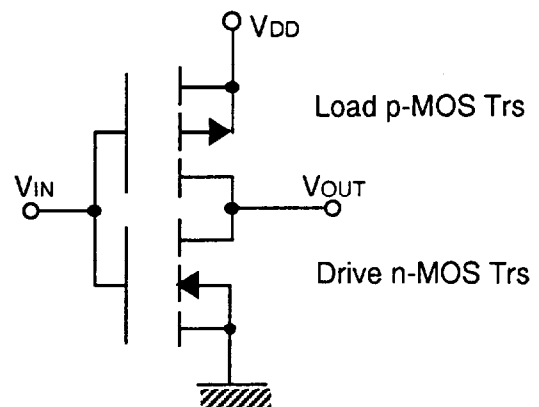


(b) Waveform of V_s

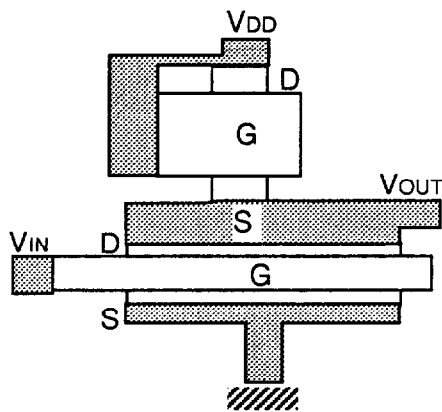
Fig. 1.15. Driving timing chart and waveform of V_s



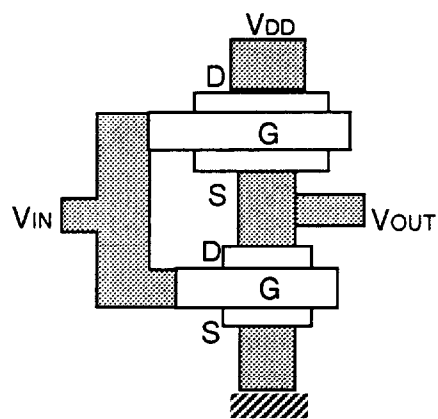
(a-1) Circuit model



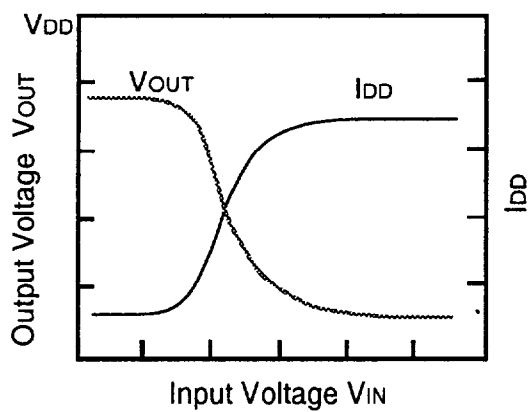
(b-1) Circuit model



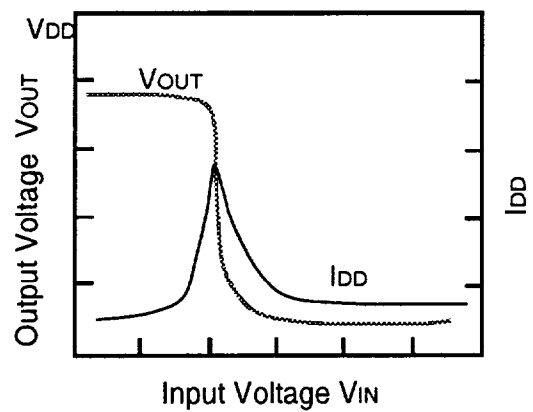
(a-2) Plane structure



(b-2) Plane structure



(a-3) Switching characteristics



(b-3) Switching characteristics

(a) E-E type inverter

(b) CMOS type inverter

Fig. 1.16. Examples of inverters.

fabrication process is simple, but TFT size of the drive TFT is large and power consumption becomes large. CMOS inverters consist of load p-MOS TFT and drive n-MOS TFT. In these inverters, load TFT and drive TFT are in the off-state in low and high modes, respectively. Therefore drive current I_{DD} flows only in the switching period and low power consumption is achieved. High inverter ratio is obtained by using small size TFTs and high switching speed is also realized. Thus, in CMOS TFT inverters, high on-current, and balance of V_{TH} of n-channel and p-channel TFTs are important. Low C_{GS} and reduction of channel length are also effective to increase switching speed (proportional to $1/(L^2)$).

Generally, TFTs are fabricated on glass substrates in which thermal conductance is very low compared to that of bulk silicon. Therefore, CMOS TFTs with low C_{GS} , short channel, and low power consumption are indispensable for driver integration in AM-LCDs.

1.4.3 System integration

If very fine and high performance TFTs (c-TFTs) comparable to bulk devices are realized, there is a possibility of further intelligent system integration on display panels. Fig.1.17 shows the steps to system integration. Today, main current a-Si TFT-LCDs use tape-automated-bonding (TAB) or chip-on-glass (COG) to mount driver LSI chips. For the XGA panel, 12 signal driver chips and 4 scan driver chips are mounted by bonding 4000 terminals (Fig.1.17(a)). There is one step to integrate a full scan driver and reduce the number of chips of data drivers by using the switch matrix of n-channel TFTs ((b)) [48]. When a high speed CMOS TFT driver is possible, full integration of scan and data drivers is possible ((c)) [26]. This technology should contribute to realizing very thin PC systems by lowering thickness of driver chips and using thinner (0.5 mm thick) glass substrates or plastic plates. The final goal is system integration on reflective display for personal data communication systems ((d)) [49]. To integrate the interface, CPU, and memories, very high performance and sub-micron TFTs comparable to LSI devices on bulk Si are necessary on display panels. These TFTs will be realized by c-Si (SOI) TFTs. Solar cells, micro-camera, flat speaker and microphone can all be mounted on a display by discrete chips.

1.4.4 Key technologies for high-performance poly-Si TFTs

Fig.1.18 illustrates key technologies for high performance poly-Si TFTs considering the discussions above. Coplaner self-aligned structure is essential to achieve low C_{GS} and fine CMOS circuits. Field-effect mobility (or on-current) critically depends on silicon film quality. Therefore, crystallization and termination of atomic defects are very important key technologies. Flat and large grains are indispensable to realize c-TFT. The location controlled grains with $1 \mu m^2$ will be sufficient to realize sub-micron TFTs for system integration.

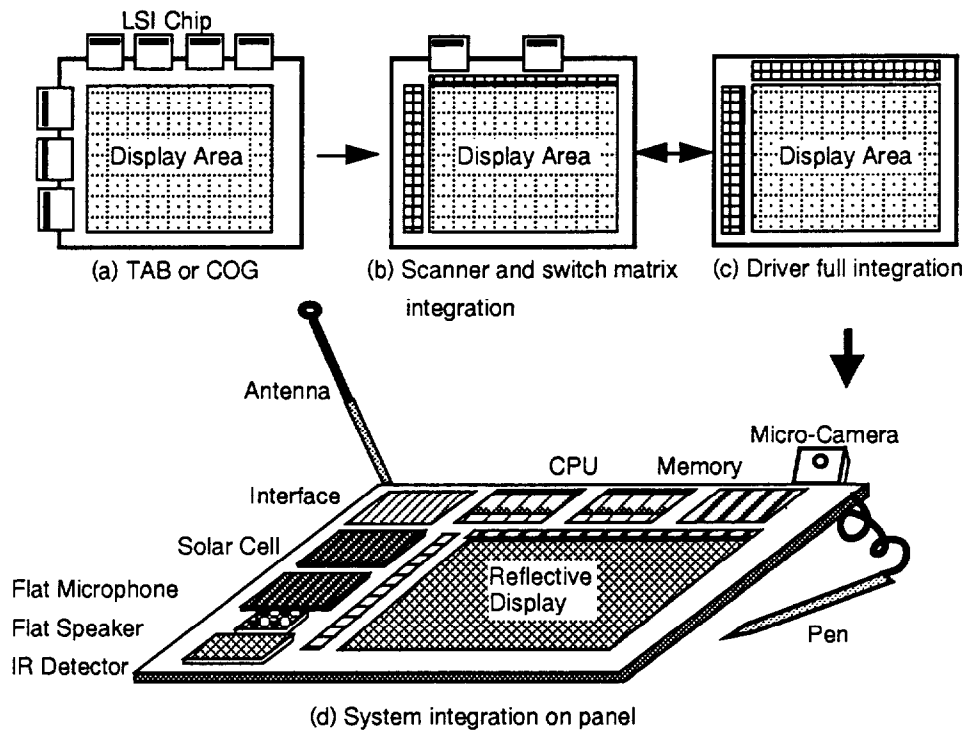


Fig. 1.17. Driver and system integration on display panel.

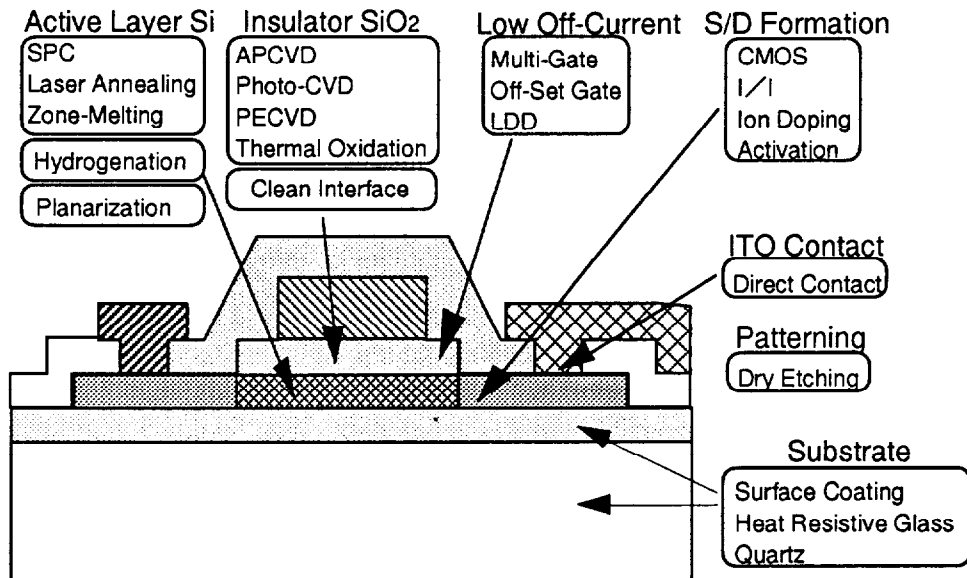


Fig. 1.18. Key technologies for high performance poly-Si TFTs.

Generally, a-Si TFT uses SiN for an insulator. But in poly-Si TFTs, high quality SiO₂ is necessary as gate insulator and passivation films. Reduction of interface states between gate oxide and poly-Si film is necessary to realize steep sub-threshold characteristics (low V_{TH}). Drain engineering is also important to realize CMOS TFTs by large area ion doping and activation, and reduce off-current. High quality poly-Si with low density of states is also essential to reduce field emission off-current. As general issues, pixel ITO contact to source poly-Si, fine patterning of thin films, and selection of glass substrate with low shrinkage are also indispensable to realize high performance low-temperature poly-Si TFT LCDs on large glass substrates.

1.5 Purposes and outline of this thesis

The application fields of low-temperature poly-Si TFTs on glass substrates will be for small and middle size, high resolution TFT-LCDs as shown in Fig. 1.9. The TFT-LCDs have made great progress in production technologies and image quality, but there are continuing demands for lighter, thinner and more compact structures. Driver and system integration by high performance poly-Si TFTs is a promising way to realize these TFT-LCDs. This thesis studies key technologies such as crystallization and doping for high performance poly-Si TFTs on large glass substrates. The accompanying peripheral technologies, large area LPCVD of Si film and dry etching are also studied.

Fig.1.19 illustrates the flow of this thesis. According to the analysis of technology trends in **Chapter 1**, first, crystallization technologies which are most important in poly-Si TFTs are studied. These technologies are classified into two major technologies, SPC, and melt and regrowth methods such as zone-melting and laser crystallization.

In **Chapter 2**, low temperature SPC at 600°C, which is the maximum process temperature to use mass-produced glass substrate, is studied. Deposition conditions under LPCVD of Si films are optimized to obtain high crystallinity in SPC. Performance of TFTs is improved to use these Si films and a 3.3" TFT-LCD is fabricated for the first time which has integration of scan and data drivers on glass substrates. Peripheral technologies such as hydrogenation, gate insulator formation by APCVD, photo-CVD and thermal oxidation are also reported.

In **Chapter 3**, the application of SPC to high-temperature TFTs is reviewed referring to the SPC results in Chapter 1. Then, middle-temperature poly-Si TFTs are proposed to use large quartz substrates. Using Si₂H₆ for source gas of LPCVD of Si film, two-step temperature SPC at 600°C and 900°C are studied experimentally and high performance TFTs are fabricated on quartz substrates. Ion doping (Chapter 6) and CVD gate oxide which are applicable to large substrates are incorporated.

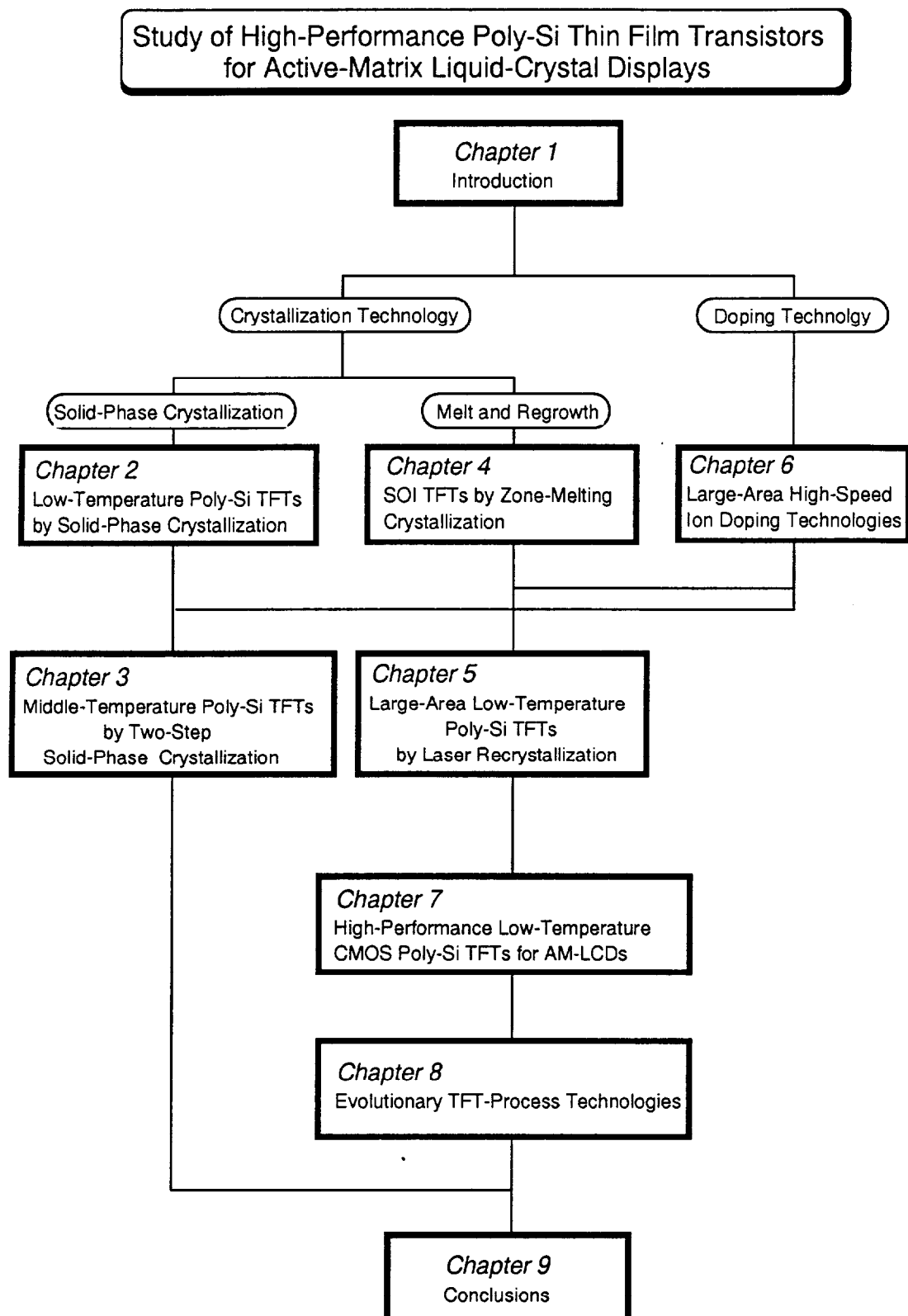


Fig. 1.19. Outline of this thesis.

As the melt and regrowth technologies, zone-melting recrystallization on quartz substrates and laser crystallization on large glass substrates are studied in the next two chapters.

In **Chapter 4**, RF heated zone-melting crystallization for high performance SOI TFTs is studied to confirm the ultimate performance of c-TFT. Quality of SOI is analyzed by TEM and EBD. Then, n-channel and p-channel TFTs are fabricated independently on 3" quartz wafers by the 3 μm LSI process. Performances of TFTs for low-voltage drive (3-5V) and operation characteristics of fundamental circuits are investigated. A very fine 1.15" p-channel SOI TFT LCD is successfully fabricated for the first time.

In **Chapter 5**, low-temperature laser crystallization technology is studied for very large glass substrates. Excimer laser crystallization is applied to 350mm x 450mm substrates. Gate SiO_2 formation by PECVD and ion doping is also used for TFT fabrication. Characteristics of n-channel TFTs are presented, using a multi-gate structure to reduce off-current. The world's largest 18.2" TFT-LCD is trial manufactured to show the possibility of poly-Si TFT-LCD fabrication on very large glass substrates.

In **Chapter 6**, large-area high-speed ion doping technology is reported. A bucket type ion source with high ion density and non-mass-separation is proposed instead of conventional ion implantation for LSI devices. First, a fundamental study by a small size ion source is presented to show the possibility of 10 s doping. And excimer laser activation is also studied for a low-temperature activation method. A large-area ion doping machine is developed for large 350mm x 450mm glass substrates. The doping mechanism for low energy doping and laser activation is proposed.

In **Chapter 7**, high-performance low-temperature CMOS poly-Si TFTs for AM-LCDs are shown. Fabrication process of CMOS TFTs using ion doping is studied. To realize TFT-LCDs with full integration of driver circuits with CMOS configuration, better uniformity of laser crystallization, higher quality of CVD gate insulator SiO_2 , and reduction of off-current are studied. A well balanced CMOS shift resistor shows 18 MHz operation. Finally, the 3.8" poly-Si TFT-LCD with driver integration is fabricated to show the practical performance of low-temperature poly-Si TFTs.

In **Chapter 8**, evolutionary process technologies for simple and super high performance poly-Si TFTs are explored. One-mask CMOS doping to eliminate a process step is proposed by using ion doping and laser activation. The novel multi-processor for continuous process of SiO_2 and a-Si depositions and laser annealing is developed to reveal great practicability and possibility. Direct laser crystallization for PECVD a-Si on SiO_2 is carried out to obtain very flat and large poly-Si grains. Continuous process of laser crystallization and gate SiO_2 deposition to

realize a clean interface, and location control of flat and large grains are also explored.

In **Chapter 9**, results are summarized and conclusions of this thesis are presented.

As **Appendices**, applications of thick poly-Si film to dielectric isolation, SIPOS passivation, a preliminary study for low-temperature SPC, large-area LPCVD of a-Si film, dry etching of ITO to realize an all-dry etching process on large glass substrates (350mm x 450mm), and repair technology by cut and deposition are presented.

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Low-Temperature Poly-Si TFTs by Solid-Phase Crystallization

In this chapter, a simple and basic technique, solid-phase crystallization (SPC) at 600°C, which is the maximum temperature to use mass-produced glass substrates, is studied to make high quality poly-Si film. Conditions for LPCVD of precursor Si film are optimized to get a high quality poly-Si film after SPC. Hydrogenation and TFT gate structures are also investigated. High performance n-channel TFTs are realized by using these process technologies and a 3.3" TFT-LCD with scan and data driver integration is successfully fabricated for the first time. The fabrication process and driving characteristics of a transparent storage capacitor are studied for grey scale presentation. In addition, new trial fabrications of SiO₂ gate insulator by photo-CVD at 300°C and thermal oxidation at 600°C are also reported.

2.1 Introduction

2.1.1 Background of low-temperature SPC of Si film

The first poly-Si TFTs were obtained by using a HT-SPC process on an oxidized Si-wafer or quartz substrate. The TFT fabrication process was based on a high-temperature process above 900 °C and an LSI process [1], [2]. A 1.51" TFT-LCD with scan and data driver integration was fabricated by SPC [3] and a 3" TFT-LCD was also fabricated by laser crystallization [4]. These technologies are the foundation of very fine high-temperature poly-Si TFT-LCDs used today in EVFs, PJ engines and HMDs.

A high-temperature process is not applicable to realizing low cost large area TFT-LCDs on glass substrates. The first low temperature poly-Si TFTs fabricated on glass substrates (below 600°C) were studied by Matsui et al. [5] in 1980 and the operation of a 10x10 matrix TFT-LCD was reported [6]. Molecular beam deposition (MBD) was used for Si film preparation. Then LT-SPC [3] and electron gun evaporation [7] were used for small size TFT-LCD fabrication. But MBD or electron gun

evaporation used a very high vacuum system which was not economical for treating large area glass substrates.

The LT- and HT-SPC have been studied by many authors [1]-[3], [8]-[16]. In these experiments, Si films were deposited by LPCVD using a simple thermal decomposition reaction. But the relationships between poly-Si film characteristics and low-temperature TFT characteristics have not been studied in detail to realize high-performance poly-Si TFTs.

2.1.2 Glass substrate and maximum process temperature

The maximum process temperature is limited by heat resistive characteristic of glass. Because poly-Si TFTs are basically MOS FETs and use SiO₂ gate insulator, mobile ions, such as sodium, and heavy metal ions, such as iron, must be eliminated to achieve high performance and stability of TFTs. Soda lime glass which is a typical mass-produced structural material contains a large amount of alkaline oxide and the heat resistivity is about 400°C. Therefore, a suitable glass material must be selected for poly-Si TFT fabrication.

Table 2.1 lists characteristics of a few kinds of glasses used by electronics industries. Fig. 2.1 shows the dependence of shrinkage on annealing time at 600 °C. Corning 7059 is a typical material but its strain point (an indicator of heat resistivity) is low and shrinkage is very large. The other glasses have strain points higher than 600 °C. Corning 1733 is mass-produced by a fusion method [17] but shrinkage is large. The amount of shrinkage saturates with increasing annealing time. Therefore, pre-annealing is a practical way to reduce glass shrinkage in the TFT fabrication process. For Asahi AN, after a 100 h pre-annealing at 600 °C, the shrinkage is 10 ppm (1 µm/10 cm) in a 10 h heating process in TFT fabrication at 600 °C.

Considering heat resistivity and shrinkage, Asahi AN was selected for the present experiments and the maximum process temperature was set at 600 °C.

2.1.3 Review of low-temperature SPC technologies

Review of previous experimental studies was carried out to clarify the key technologies to realize high-performance TFTs as indicated in Fig. 1.18. The results of preliminary experiments are presented in Appendix 3.

To identify the important factors for the active layer Si film and gate SiO₂, a few preparation methods of Si films and SiO₂ films were considered for TFT fabrication. Quartz substrates and 3 µm LSI process were used. As Si film preparations, MBD [5], PECVD, and LPCVD at 580°C or 640°C were demonstrated. Gate SiO₂ was fabricated by APCVD, PECVD and high temperature thermal oxidation. Among these experiments, none of these processes could achieve sufficient TFT characteristics. But the TFTs fabricated by MBD Si and APCVD SiO₂ were the best. The grain size of PECVD Si films after SPC at 580°C was

Table 2.1 Characteristics of glasses for electronic industries

		Corning #7059	Corning #1733	Asahi AN	HOYA NA-40
Components	SiO ₂	49	57	55.5	55
	Al ₂ O ₃	11	16	15	14
	Ba ₂ O ₃	15	11	2	-
	RO	25	14	28	31
	R ₂ O	0.1	0.1	0.05	0.1
Strain Point (°C)		472	640	655	656
Transition Point(°C)		718	928	910	904
Thermal Expansion Coefficient(ppm)		4.6	3.9	4.4	4.6
Production Method		Fusion	Fusion	Block Slicing	Block Slicing
Application		a-Si TFT		Photo-mask	Photo-mask

R: Refractory Metal

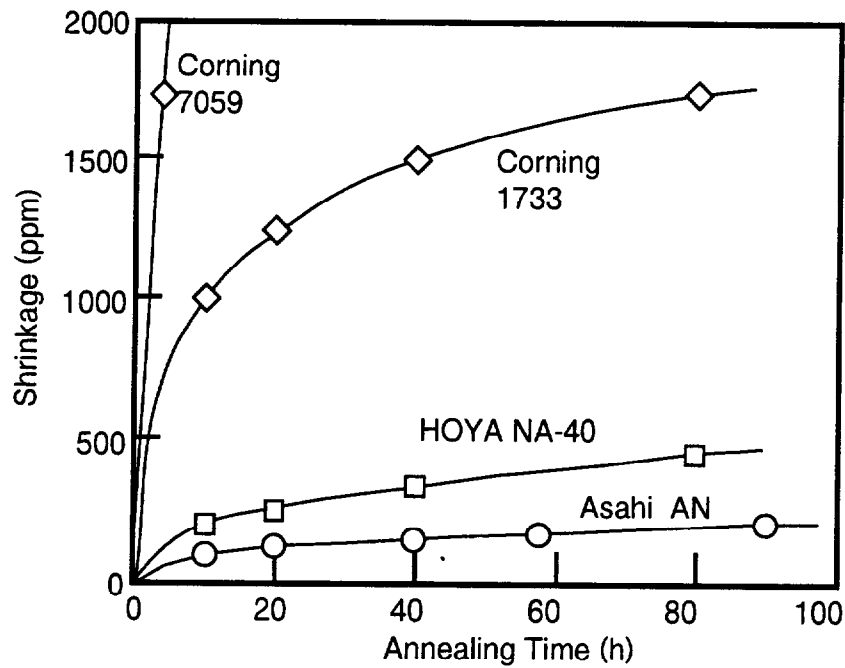


Fig. 2.1 Shrinkage of glass substrates by annealing at 600°C.

not drastically increased [18]. The TFTs with LPCVD Si obtained by somewhat high-temperature deposition showed low threshold voltages. Mobility of TFTs with thermal gate oxide was very low, contrary to expectation. The TFTs with APCVD and PECVD gate SiO_2 showed almost the same mobility.

Therefore, these results indicate that optimization of the SPC process of LPCVD Si films and combination of gate oxide of APCVD SiO_2 would improve TFT characteristics. In general, the quality of Si films and the gate insulator is very important, as indicated in Fig. 1.18.

2.1.4 Purposes of this study

First, process conditions of SPC at 600 °C were studied. Deposition conditions of Si films by LPCVD were optimized to obtain high quality poly-Si films after SPC. Effective hydrogenation was also investigated by improving TFT structures. The developed high-performance n-channel TFTs were applied to a 3.3" TFT-LCD with integration of scan and data drivers on glass substrates, for the first time, to test the TFT ability. The fabrication process and driving characteristics of a transparent storage capacitor were studied for grey scale presentation. As new approaches to obtain novel gate oxides at low temperature, photo-CVD at 300 °C and thermal oxidation at 600 °C were also studied.

2.2 High-performance poly-Si TFTs by solid-phase crystallization

2.2.1 Optimization of solid-phase crystallization of LPCVD Si films at 600°C

(1) Si film preparation and evaluation

Fig. 2.2 illustrates the apparatus for LPCVD of precursor Si films. Glass substrates (Asahi AN, 1.1 mm thick), coated with APCVD SiO_2 , were set in the LPCVD tube. Source gas was 20% SiH_4 diluted with helium. Substrate temperature and gas pressure were varied from 500 to 620 °C and 40 to 100 Pa, respectively. Pressure was controlled by operating a variable conduction valve. Temperature was controlled within ± 1 °C over 300 mm region to realize good uniformity of film thickness. Film thickness was typically 150 nm and measured by ellipsometry. The deposited films were annealed to crystallize in the diffusion process tube under an N_2 atmosphere at 600 °C. The crystallinity of the films was evaluated by measuring the intensity of thin film x-ray diffraction (XRD) intensities. The beam was fixed by 2° from the Si film surface. The sample size and film thickness were also fixed at 20 mm x 20 mm and 150 nm, respectively. Microstructures of a cross section of the films were observed by transmission electron microscopy (TEM) at an acceleration voltage of 200 kV. The hydrogen content was analyzed by secondary ion mass spectrometry (SIMS), using cesium ion bombardment.

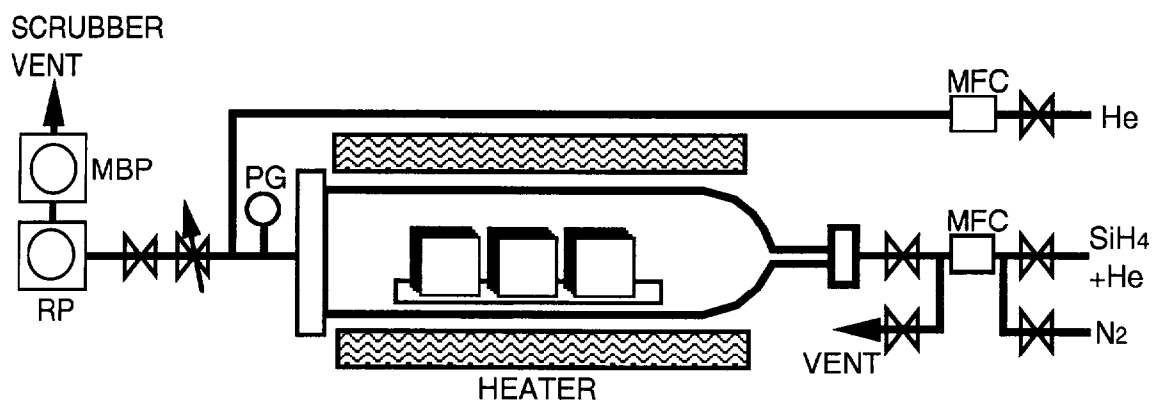


Fig. 2.2 Apparatus for LPCVD of Si films.

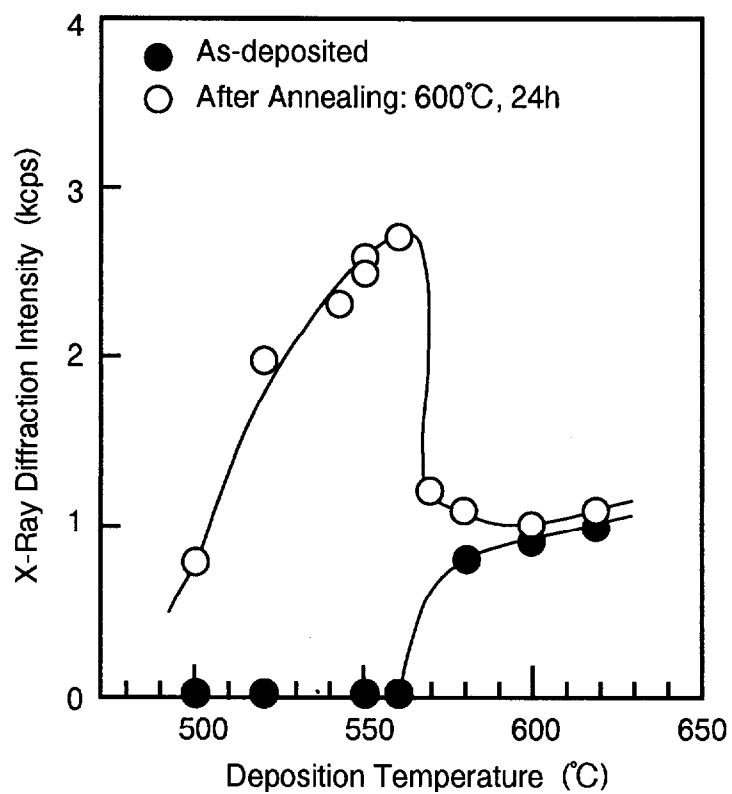


Fig. 2.3 Dependence of X-ray diffraction intensity of (111) surface on Si film deposition temperature.

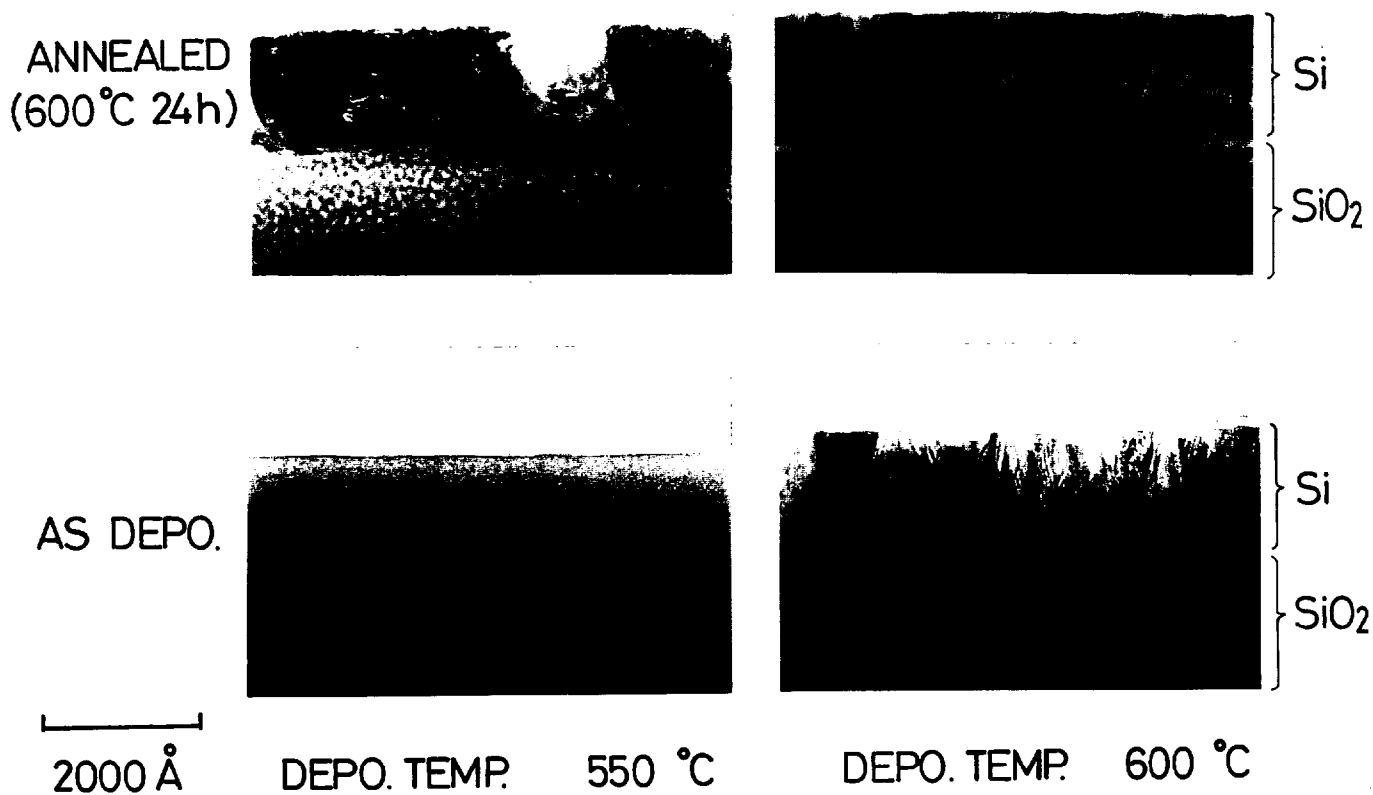


Fig. 2.4 TEM observations of poly-Si film cross sections.

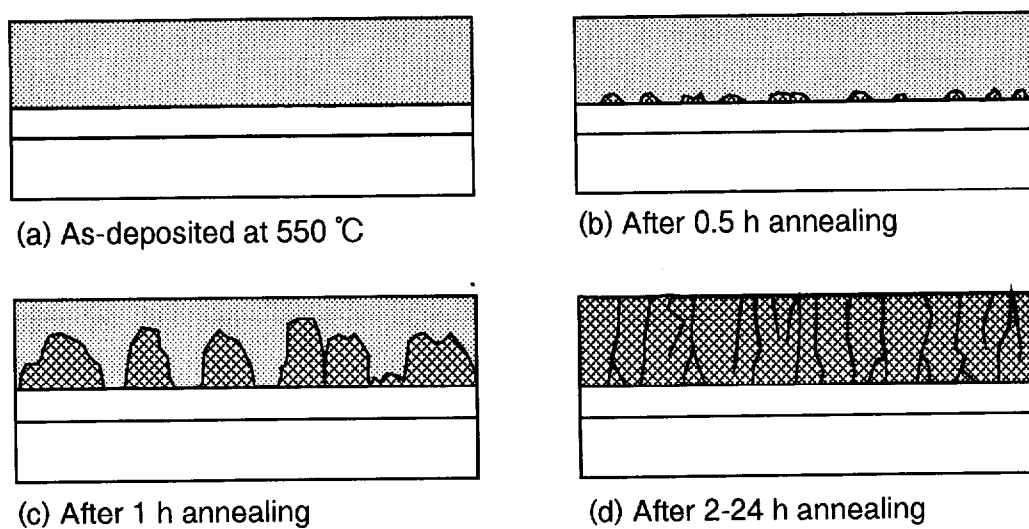


Fig. 2.5 Crystallization progression of LPCVD Si film for 600 °C SPC [22].

(2) Crystal quality of poly-Si films

Fig. 2.3 plots dependence of X-ray diffraction intensity of (111) surface on poly-Si deposition temperature. The diffractions from (111), (220), and (311) surfaces were observed, but that of (111) was the strongest for the powder x-ray diffraction. Therefore, the intensity of (111) was used as an indicator for crystallinity of the poly-Si layer. For the as-deposited films above 580°C, a crystal component (x-ray intensity) was observed which increased by raising deposition temperature. But there was almost no increase in crystallinity (grain size) after annealing. The films deposited below 560°C were amorphous because the diffraction spectrum had no peaks. After annealing at 600°C, the Si film deposited at 550-560°C showed the highest intensity indicating that it had the highest crystallinity. The mean grain size calculated by Sherrer's equation [19] also showed a maximum and was about 20 nm for that temperature range.

Table 2.2 shows the ratio of XRD intensities of (111), (220), (311) surfaces.

Table 2.2 Ratio of XRD intensities of (111), (220), (311) surfaces

Powder XRD (Standard)	I(111) : I(220) : I(311) = 100:55:30
550°C Deposition	I(111) : I(220) : I(311) = 100:35:20
620°C Deposition	I(111) : I(220) : I(311) = 100:40:25

The Si film deposited at 550°C had a higher intensity ratio of $I_{(111)}$ than that of powder XRD [20] which has no preferred orientation. Therefore, the Si film deposited at 550°C had the largest grain size and also the (111) preferred orientation.

Fig. 2.4 shows TEM photographs for Si film cross sections. The Si film deposited at 600°C had needle-like poly-Si grains that indicated that crystalline growth started at the interface of Si film and SiO₂. But grain growth was not advanced by a following 600°C thermal annealing. The Si film deposited at 550°C was amorphous, but large cube-like grains were observed after annealing. For the poly-Si deposited at 520°C, large grains were also observed though they were somewhat smaller than the 550°C deposited poly-Si.

(3) Mechanism of large grain growth

From the results of x-ray diffraction and TEM observations, it was concluded that the Si film deposited at 600°C was already poly-Si, but it had no amorphous phase to promote grain growth during annealing. On the other hand, precursor Si film deposited at 550°C was almost entirely amorphous, but it had an optimum number of nuclei and optimum volume of amorphous phase to induce remarkable grain growth in annealing.

More detailed considerations on the crystallization have been reported by Aoyama et al. [21] and Adachi et al. [22]. Fig. 2.5 shows a schematic of crystallization progression for 600°C SPC [22]. After 0.5 h annealing, crystallization started at the interface of Si film and underlayer SiO₂. Stress in the Si film at the interface was considered to be the motive force of nuclei generation. Grain growth continued with increasing annealing time and saturated after 2 h when the whole amorphous region was consumed for grain growth. Fig. 2.6 plots the effect of the deposition temperature on the average grain (crystallite) size [21] calculated by Scherrer's method [19]. A maximum size of 20 nm was obtained at the deposition temperature of 550°C. TEM observation of poly-Si film surface also showed the same tendencies as the cross section of Fig. 2.4 and the maximum grain size was about 500 nm at 550°C deposition. This apparent grain size was much larger than the film thickness and the mean grain size of x-ray diffraction in which crystallites were observed. This result showed that lateral grain growth occurred occasionally and dendrite-like grains were observed. High-resolution TEM observation (lattice pattern) showed that the apparent grains had small angle grain boundaries and twins, and were composed of several crystallites. The electron beam diffraction (EBD) analysis showed that Si film deposited at 550°C had almost halo pattern indicating it was almost amorphous. But after annealing, irregular spots were observed showing it had oriented grains. Fig. 2.7 shows the effect of the deposition temperature on electron spin density of Si films [21]. A maximum spin density was observed for the as-deposited film at 550°C and a minimum spin density was observed for that film after annealing. The results implied that the spin density (dangling bond density) significantly contributed to promote SPC. Increasing deposition pressure was also effective in increasing the x-ray diffraction intensity. But, too high a pressure (high deposition rate) induced surface roughness.

2.2.2 TFT fabrication process

Figs. 2.8 and 2.9 show a cross-sectional view of TFT and the typical fabrication process of the poly-Si TFT with the conventional n-channel MOS FET structure, respectively. The substrate was Asahi AN glass (100 mm by 100 mm, 1.1 mm thick). An underlayer of SiO₂ (400 nm) was deposited by APCVD. Poly-Si (150 nm thick) was deposited at 550 or 580°C to give the active layer poly-Si. The poly-Si was annealed at 600°C for 20 h in N₂ to recrystallize and then patterned into islands. After chemical cleaning, the gate oxide (100 nm) was deposited by APCVD at 480°C. The gate poly-Si (50-350 nm) was deposited by LPCVD at 550°C. After gate patterning, phosphorous ions were implanted at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ and 30 kV to form the source, drain and gate regions by self-alignment structure. After deposition of phospho-silicate glass (PSG) for passivation, thermal annealing was carried out at 600°C for 20 h in N₂ to

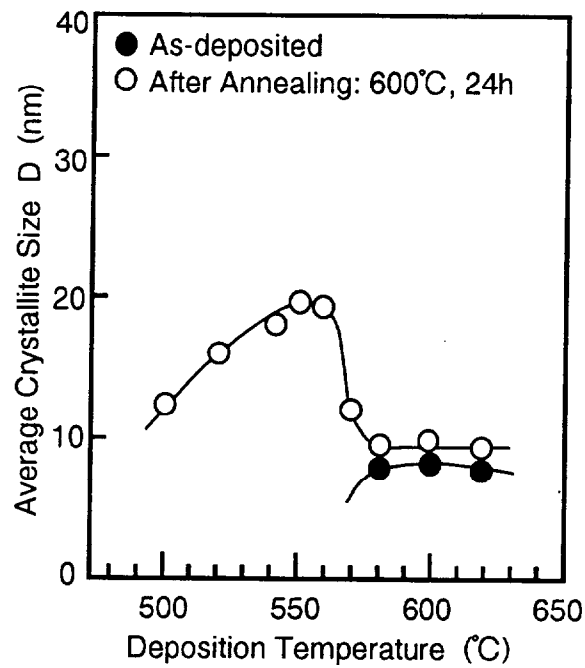


Fig. 2.6 Dependence of average crystallite size on deposition temperature. After Aoyama et al.[21].

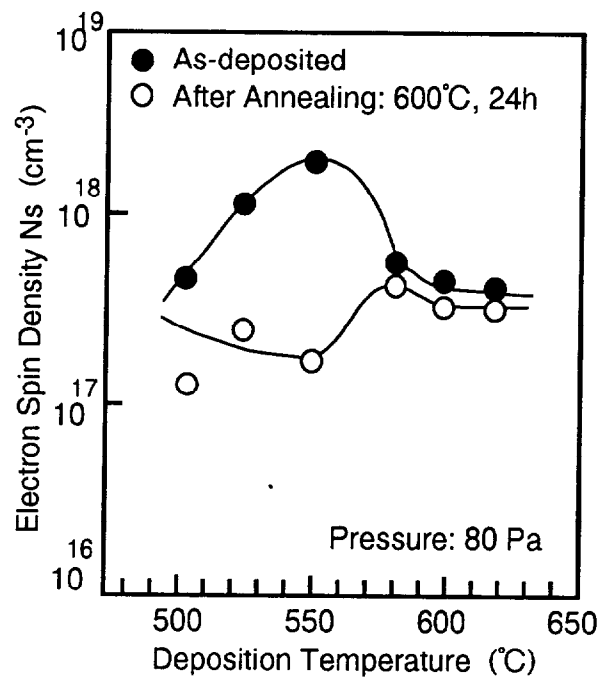


Fig. 2.7 Dependence of electron spin density on Si film deposition temperature. After Aoyama et al.[21].

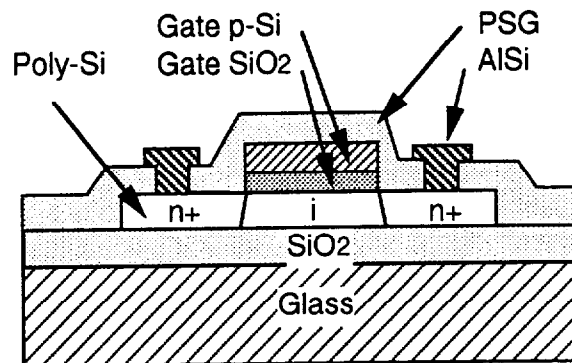


Fig. 2.8 Cross-sectional structure of TFT.

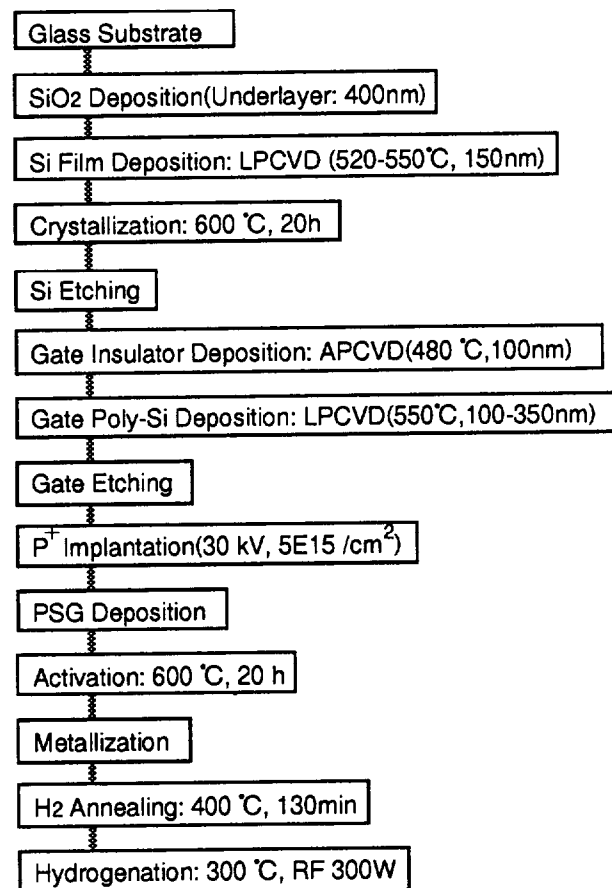


Fig. 2.9 TFT fabrication process.

activate implanted ions. After metallization by sputtered AlSi (2 %), the substrate was annealed at 400°C for 30 min in the forming gas. Finally, hydrogenation was carried out in a plasma reactor with parallel electrodes (13.56 MHz) at 300°C and 300 W in pure H₂ atmosphere. Indium tin oxide (ITO) was deposited and wet etched as the transparent electrodes when the TFTs were applied to LCD use.

The basic characteristics of TFTs were measured. The field-effect mobility, μ_{FE} , is defined as the maximum value calculated from the following equation (2-1) for $V_D = 0.1$ V. And the threshold voltage, V_{TH} , is derived from the square root of I_D versus V_G curve at saturated region of $V_D = 5$ V, according to equation (2-2).

$$\mu_{FE} = \frac{L}{W} \cdot \frac{1}{V_D \cdot C_{OX}} \cdot \frac{\partial I_D}{\partial V_G} \quad \text{----- (2-1)}$$

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_{FE} \cdot C_{OX} \cdot (V_G - V_{TH})^2 \quad \text{----- (2-2)}$$

Here, L , W , and C_{OX} are the channel length, channel width and the gate capacitance, respectively.

2.2.3 Improvement of TFT characteristics by optimization of solid-phase crystallization

It was shown in section 2.2.1 that poly-Si quality was drastically improved when LPCVD conditions of precursor Si were optimized.

Fig. 2.10 plots the dependence of field-effect mobility and threshold voltage on the deposition temperature of LPCVD Si. Field-effect mobility and threshold voltage were calculated by equations (2-1) and (2-2). In this experiment, hydrogenation was not used because it was ineffective for the thick poly-Si gate (350 nm) TFTs as described in section 2.2.4. Significant results were that the field-effect mobility became a maximum (30 cm²/V·s) and the threshold voltage became a minimum (12 V) at a deposition temperature of about 550°C. These results agreed with those of Figs. 2.3 and 2.4. The field-effect mobility increased from 2 to 30 cm²/V·s when deposition temperature was controlled from 580°C to 550°C.

High crystallinity revealed another important role for the TFT process. Fig. 2.11 shows the dependence of sheet resistance of active layer (source and drain), and gate poly-Si layers. Phosphorous ions were implanted in the active layer and gate, with and without pre-crystallization (20 h), respectively. Activation time was 20 h in N₂. Sheet resistance of source and drain layer were a minimum at deposition temperature of 550°C. This indicated that the poly-Si with the highest crystallinity had a minimum sheet resistance corresponding with Fig. 2.3. This was because high crystallinity assisted the activation of impurities

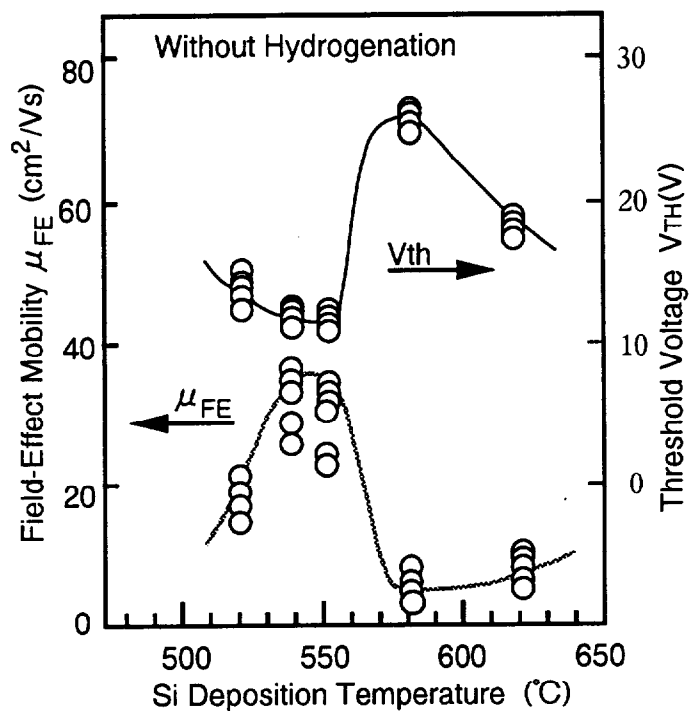


Fig. 2.10 Dependence of field-effect mobility on Si film deposition temperature.

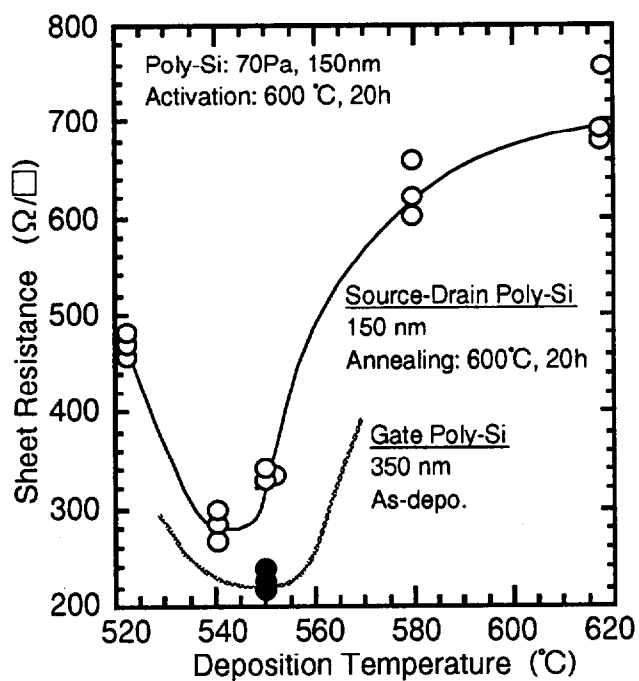


Fig. 2.11 Dependence of sheet resistance on poly-Si deposition temperature.

and carrier conduction. Also the thick gate (350 nm) had a lower sheet resistance than the active layer (150 nm) at 550°C deposition. Therefore, gate poly-Si was also deposited at 550°C in TFT fabrication.

Fig. 2.12 plots the dependence of field-effect mobility on XRD intensity of (111) surface obtained from Figs. 2.6 and 2.10. Field-effect mobility was almost proportional to the XRD intensity (crystallinity). Therefore, it was concluded that there was noticeable improvement of TFT characteristics as realized by increasing crystallinity (grain size).

Fig. 2.13 plots the dependence of leakage current on XRD intensity of (111) surface. The leakage current increased with increasing XRD intensity, namely increasing poly-Si crystallinity. This was because carrier mobility was increased though localized state density (trap density) was decreased. Reduction of leakage current is indispensable to TFT use for pixels. So optimization of TFT structure and drain engineering are necessary. Some considerations about leakage current are presented in section 2.2.5.

2.2.4 Improvement of TFT characteristics by hydrogenation

To realize high performance poly-Si TFTs, first, high-quality poly-Si must be obtained. This was achieved by optimizing Si deposition conditions as discussed in section 2.2.1. Second, atomic defects (dangling bonds) must be reduced. Hydrogenation [23]-[25] is an effective technique for this purpose, and it can be done by hydrogen plasma [26]-[27], plasma-deposited silicon-nitride film [28]-[31], and implanted hydrogen [32]-[34]. In the next experiment, hydrogenation using only a conventional plasma reactor and pure H₂ gas was employed for atomic defect passivation. The conspicuous effects of hydrogenation on multi-gate (1-10 division) and thin poly-Si gate TFTs were studied.

(1) Hydrogenation for TFTs with thick and thin poly-Si gates

It is important to understand the hydrogen content profiles in gate poly-Si films for effective hydrogenation using pure hydrogen plasma.

Fig. 2.14 shows hydrogenation temperature and time dependence on the hydrogen content profile in poly-Si films as measured by SIMS. Under practical conditions for effective hydrogenation to improve TFT characteristics, for example, 60 min at 270°C, thickness of the hydrogenated area was estimated to be about 100 nm. Hydrogen has a very large diffusion coefficient [35] and it can penetrate PSG (600 nm) and gate oxide (100 nm) easily. These indicate that a thick gate poly-Si prevents hydrogenation of the active layer poly-Si and thinning the poly-Si gate below 100 nm is necessary to realize effective hydrogenation for the channel region which is under the gate poly-Si and gate oxide.

Fig. 2.15 plots the threshold voltage dependence on RF power for TFTs with various gate thicknesses in hydrogenation. The TFT with 350 nm gate showed no improvement in threshold voltage. This was because

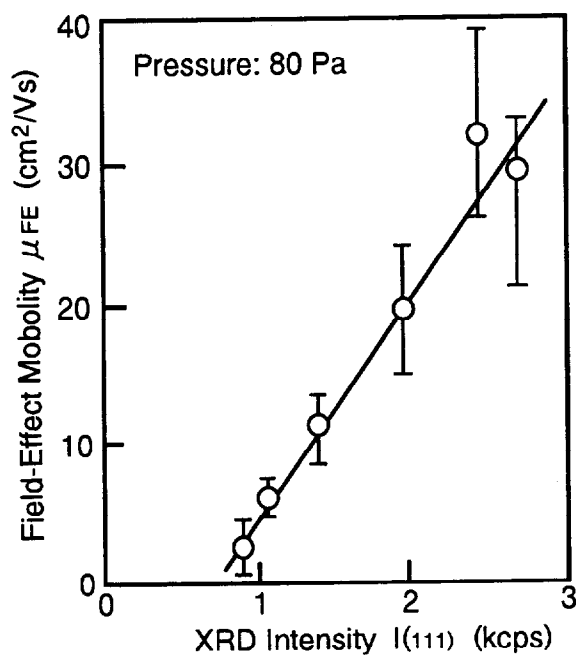


Fig. 2.12 Dependence of field-effect mobility on XRD intensity of (111) surface.

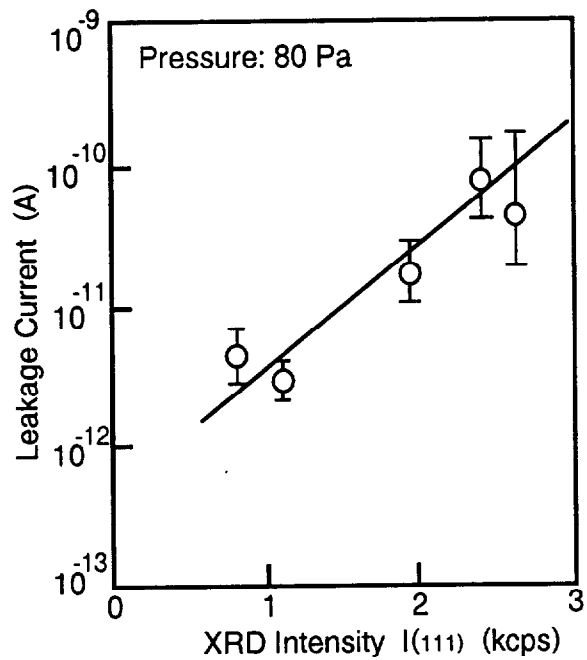


Fig. 2.13 Dependence of leakage current on XRD intensity of (111) surface.

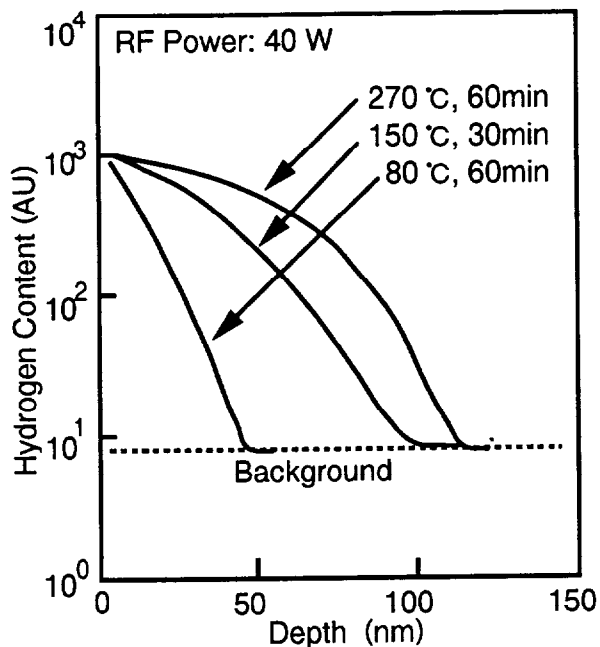


Fig. 2.14 Dependence of hydrogen content profile on substrate temperature during hydrogenation.

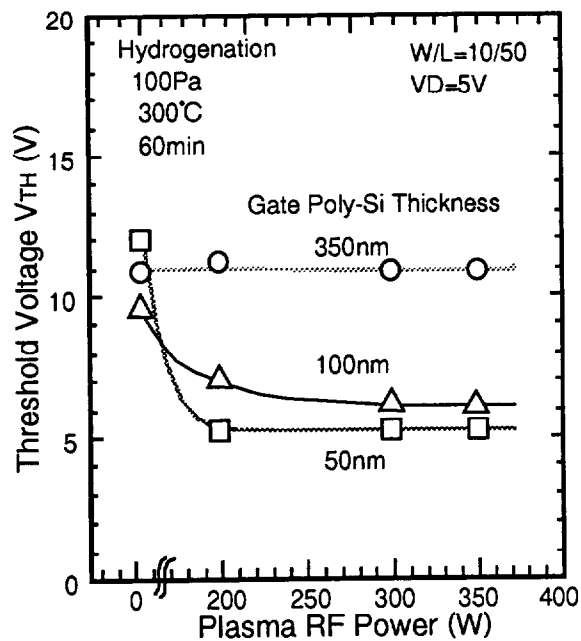


Fig. 2.15 Effect of RF power on threshold voltage of TFTs.

hydrogen did not reach the bottom of the gate poly-Si as implied in Fig. 2.14. The TFTs with thinner gate poly-Si showed a lower threshold voltage which saturated at lower RF power.

Hydrogenation for TFTs also closely depends on the TFT structure. In the first stage of this research, a multi-gate structure with a conventional thick poly-Si gate (350 nm) was studied. The gate thickness of 350 nm is standard for 3 μ m CMOS LSI devices.

Fig. 2.16 shows photographs of the fabricated single- and multi-gate TFTs which were used in this study.

Fig. 2.17 describes the expected diffusion route of hydrogen into active layer poly-Si. If the diffusion rate of hydrogen in oxide is very large, lateral diffusion of hydrogen in gate oxide will have an important role in hydrogenation.

Fig. 2.18 illustrates hydrogenation models for the thick poly-Si single-gate TFTs. It was assumed that, in the thick poly-Si gate TFTs, only the side of the long gate was laterally hydrogenated. On the other hand, in a short multi-gate TFT, all of the channel areas were hydrogenated laterally to improve TFT characteristics. Fig. 2.19 shows hydrogenation models for the thin poly-Si gate structure TFTs. It was expected that all single- and multi-gate TFTs were effectively hydrogenated through thin gates.

Fig. 2.20 shows the hydrogenation effect on threshold voltage versus gate poly-Si thickness characteristics. Before hydrogenation, threshold voltage was independent of gate poly-Si thickness. But, thinning of gate poly-Si was remarkably effective in reducing the threshold voltage after hydrogenation. The reduction ratio was about 50 % at a gate poly-Si thickness of 100 nm.

Fig. 2.21 shows the hydrogenation effect on field-effect mobility versus gate poly-Si thickness characteristics. The field-effect mobility also increased in the thin poly-Si gate TFTs.

Thus, further thinning of the gate (below 50 nm) may be more effective to improve static performance, however, sheet resistance of gate poly-Si increased. Therefore the gate poly-Si thickness of 100 nm was adopted in TFT fabrication.

(2) Hydrogenation of single- and multi-gate TFTs

Fig. 2.22 shows the hydrogenation effect on threshold voltage V_{TH} in thick poly-Si gate (350 nm) TFTs. N was the number of divisions, and total channel length of all TFTs was 30 μ m to normalize the electric field strength in the channel. The effect of hydrogenation was very small for single and long gate (30 μ m) TFTs. But, reduction of unit channel length was very effective to reduce V_{TH} , which supported the model shown in Fig. 2.18. At a unit channel length of 3 μ m and a division number of 10, a V_{TH} of 6 V was obtained. From this result, the lateral penetration length of hydrogen in the gate oxide was estimated to be about 2-3 μ m under this hydrogenation condition. A short-channel multi-gate was effective for reducing V_{TH} , even if the poly-Si was thick.

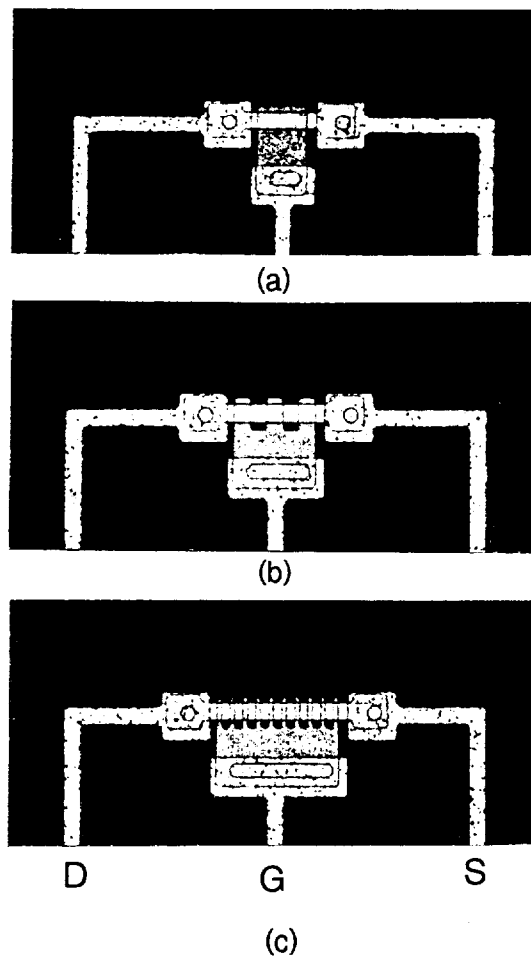


Fig. 2.16 Photographs of fabricated single and multi-gate TFTs. Division numbers are (a) one (single), (b) three, and (c) ten. Total channel length $L=30\ \mu\text{m}$, $W=10\ \mu\text{m}$.

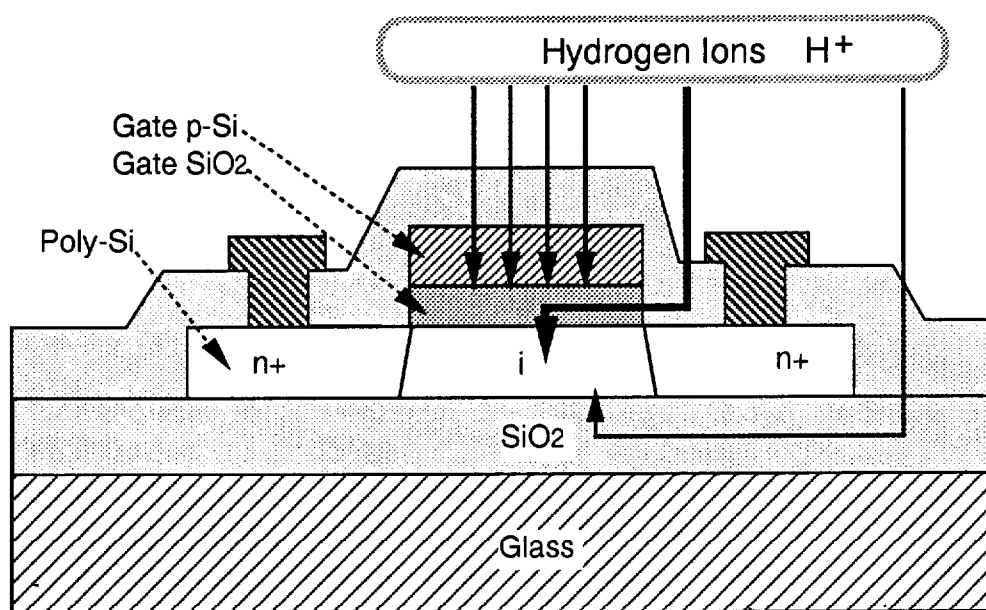


Fig. 2.17 Diffusion route for hydrogenation.

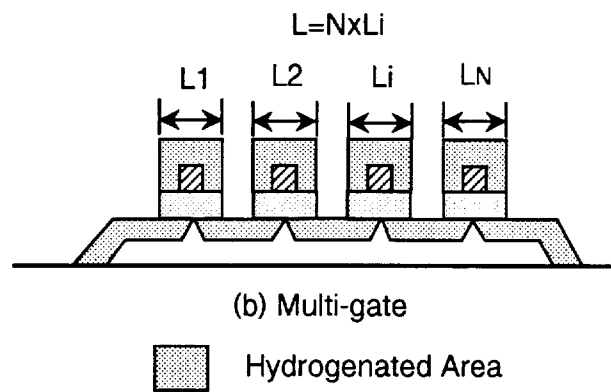
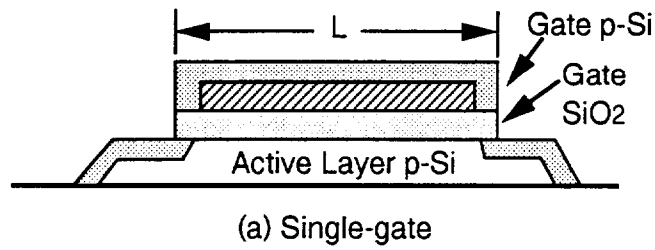


Fig. 2.18 Hydrogenation models for thick poly-Si gate TFTs.

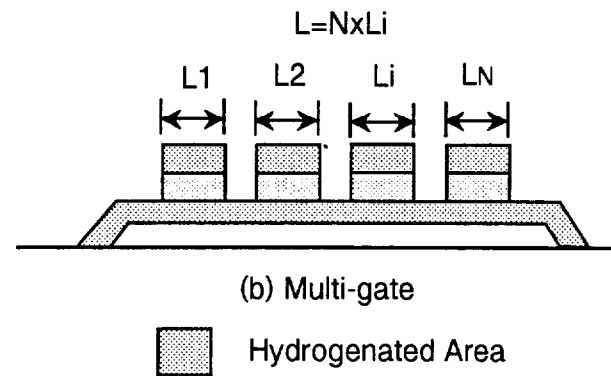
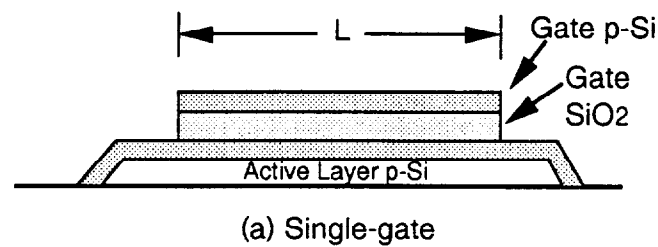


Fig. 2.19 Hydrogenation models for thin poly-Si gate TFTs.

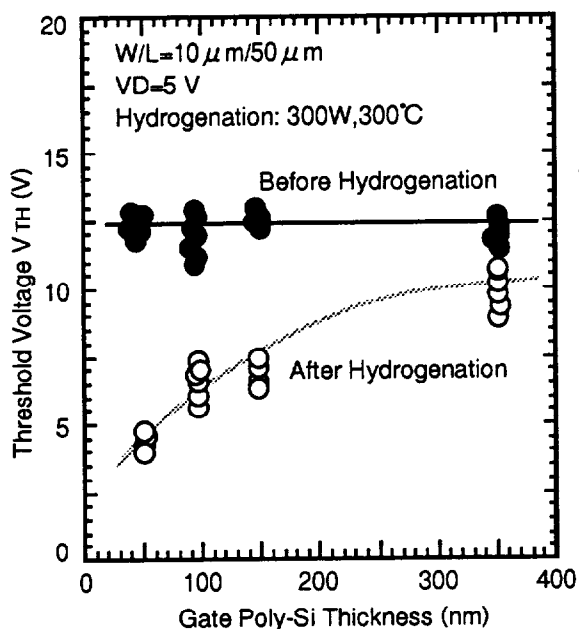


Fig. 2.20 Hydrogenation effect on threshold voltage versus gate-poly Si thickness characteristics.

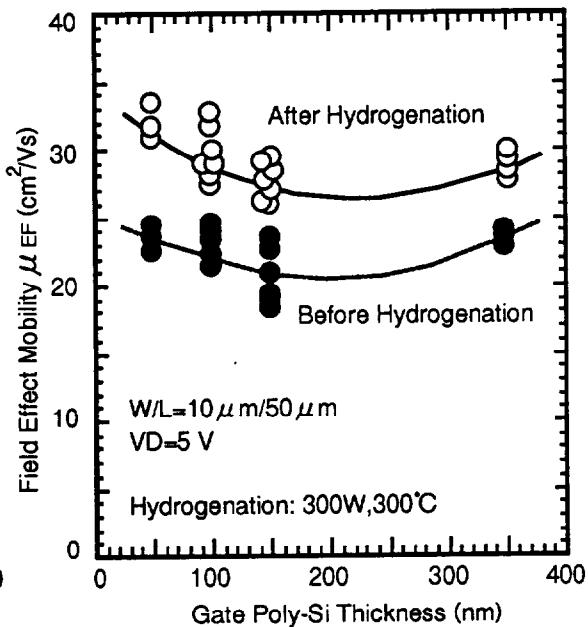


Fig. 2.21 Hydrogenation effect on field-effect mobility versus gate-poly Si thickness characteristics.

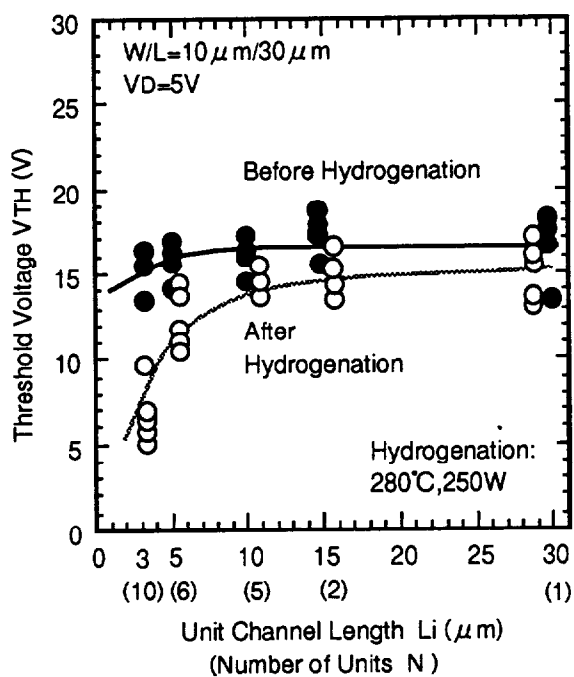


Fig. 2.22 Hydrogenation effect on threshold voltage of thick poly-Si multi-gate TFTs.

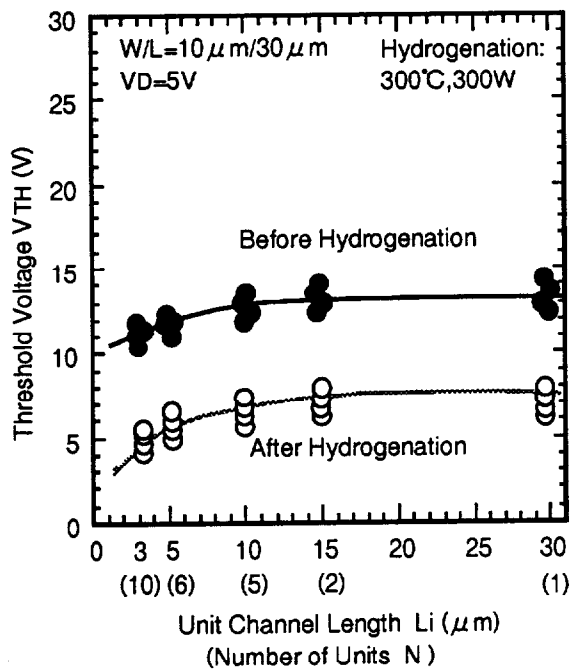


Fig. 2.23 Hydrogenation effect on threshold voltage of multi-gate TFTs with 100 nm poly-Si gate.

Reduction of the unit channel length was also effective to increase μ_{FE} . The value increased from 15 to 22 $\text{cm}^2/\text{V}\cdot\text{s}$ after hydrogenation at a channel length of 3 μm .

However, long-channel TFTs with low V_{TH} are necessary to fabricate simple E-E-type drive circuits. From this consideration, it was concluded that hydrogenation from the gate surface was indispensable and thinning of the gate should be pursued.

Fig. 2.23 plots the hydrogenation effect on threshold voltage in multi-gate TFTs with a 100 nm poly-Si gate. Total channel length was 30 μm , the same as in Fig. 2.22. The effect of hydrogenation was very large for all TFTs and independent of the unit channel length. The V_{TH} of single-gate TFTs with a channel length of 30 μm was reduced to about 7 V, one half of the initial value and practical for logic circuits. At a unit channel length of 3 μm and division number of 10, a V_{TH} of about 4 V was obtained. A thin poly-Si gate was also effective for changing μ_{FE} , which increased from 23 to 30 $\text{cm}^2/\text{V}\cdot\text{s}$ for TFTs with a channel length of 30 μm .

(3) Dehydrogenation of thin poly-Si gate TFTs

Dehydrogenation occurs when TFTs are treated at high-temperature [23], [36], [37]. Dehydrogenation induces the degradation of TFT characteristics. The process temperature after hydrogenation must be controlled to avoid dehydrogenation. The dehydrogenation effect on TFTs was studied for multi-gate TFTs with 100-nm poly-Si gate.

Fig. 2.24 shows the annealing temperature dependence on V_{TH} versus the unit channel length characteristics. Initial values refer to V_{TH} just after hydrogenation at 300 °C and 300 W. Annealing was carried out in $\text{N}_2\text{-H}_2$ atmosphere. Significant degradation of characteristics was not observed for the TFTs annealed at 350 °C, though some dehydrogenation occurred at this temperature [36], [37]. But, by raising the annealing temperature from 375 to 450 °C, V_{TH} increased noticeably. The V_{TH} of TFTs annealed at 450 °C was almost the same as that of TFTs before hydrogenation as shown in Fig. 2.23. The increasing ratio of V_{TH} of short unit channel TFTs was slightly larger than that of long unit channel ones. This showed that short-channel TFTs were both hydrogenated and dehydrogenated rapidly. The TFTs with higher temperature hydrogenation showed slower dehydrogenation at thermal annealing [36]. The hydrogenation temperature of 300 °C that was used in this experiment was deemed practical, considering these results.

The TFT fabrication process shown in Fig. 2.9 did not include any higher temperature step than 350 °C after hydrogenation. Therefore, the hydrogenation effect was not lost in the developed TFTs.

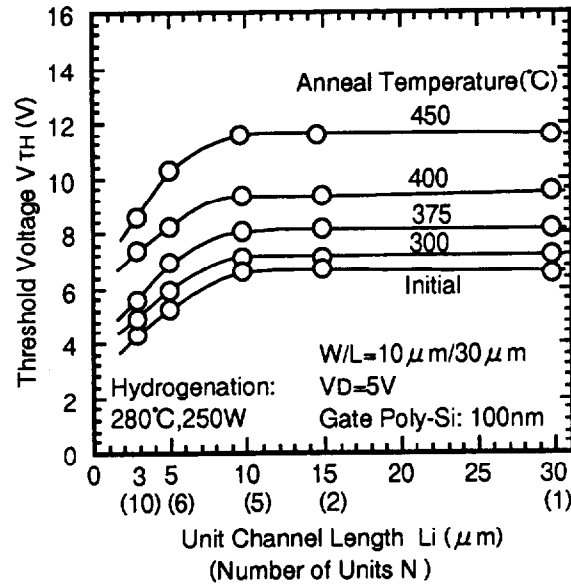


Fig. 2.24 Dehydrogenation annealing effect on V_{TH} versus unit channel length characteristics.

Table 2.3 Characteristics of the developed TFTs with optimized temperature deposited poly-Si and thin gate

Device			A	B	C	D	E
Poly-Si Deposition	Temperature ($^\circ C$)		550	520	580	550	550
	Pressure (Pa)		80	80	80	133	133
	Thickness (nm)		150	150	150	150	60
Gate-Poly Si	Temperature ($^\circ C$)		550	550	550	550	550
	Pressure (Pa)		133	133	133	133	133
	Thickness (nm)		100	100	100	100	100
Threshold Voltage V_{TH}			(V)				
Field-Effect Mobility μ_{FE}			(cm^2/Vs)				
On-Off Ratio (Log(I_{on}/I_{off}))							
Off-Current			(pA)				
Gate Breakdown Voltage BV_G			(V)				
Ion: $V_D=5V, V_G=20V$							
VTH: $V_D=5V,$							
Ioff: $V_D=5V, V_G=0V$							
$\mu_{FE}: V_D=0.1V$							

2.2.5 High-performance TFTs with optimized poly-Si deposition and hydrogenation

(1) TFT characteristics

Table 2.3 and Figs. 2.25 to 2.28 summarize the characteristics of the developed TFTs with 100 nm poly-Si gate and active layer poly-Si deposited at various conditions. TFT-A was the developed standard with poly-Si deposited at 550°C according to the results of Fig. 2.10. TFT-B and TFT-C were reference devices with poly-Si deposited at 520 and 580°C, respectively. TFT-D was the best TFT with poly-Si deposited at 550°C and 133 Pa. Increasing deposition pressure is another effective way to improve crystallinity, but a higher pressure than 133 Pa causes a gas phase reaction and particle generation (rough surface). Characteristics of the optimized TFT-A and TFT-D were remarkably improved compared to TFT-B and TFT-C. TFT-E had a thin active layer 60 nm thick to reduce off-current [38], [39]. But on-current was saturated because of high resistivity of source and drain. In the TFT fabrications, ion implantation was carried out at 30 kV which is a minimum operation value for an ordinary implanter. The projection range (about 40 nm for P⁺) was too deep for 60 nm poly-Si film. To optimize the projection range, novel shallow doping technologies are indispensable, such as controlling the projection range by using a cap SiO₂ layer, using a lower energy implanter with an acceleration voltage below 10 kV, or using new ion doping technologies (cf. Chapter 6).

(2) A consideration for on- and off-current of TFTs

Poly-Si TFT operation was provisionally considered using the device model of a bulk MOS FET. But in a more detailed study to improve poly-Si TFT characteristics or simulate a device, further theoretical consideration is necessary. This is because poly-Si has an imperfect crystal structure as shown in Fig. 2.29. Poly-Si ((b)) has a long range order compared with amorphous Si ((a)). But, it has crystal disorders such as grain boundaries (macro defects) and dangling bonds (atomic defects) which degrade the carrier conduction and become the site of leakage current generation. Hydrogenation is effective to eliminate dangling bonds, resulting in increased mobility and reduced threshold voltage. In this section, a previously proposed theoretical consideration is reviewed and an approach to improve TFT characteristics is discussed.

Fig. 2.30 illustrates the energy band structure in a grain boundary trapping model which was first proposed to explain the carrier conduction in poly-Si [40], [41]. It is understood that lowering barrier height and reducing the number of grain boundaries are effective to increase carrier conductivity.

A peculiar characteristic of poly-Si TFT is increase of the leakage current at negative gate voltage application as was shown in Figs. 2.25 to 2.28. The leakage current characteristic has been discussed using the

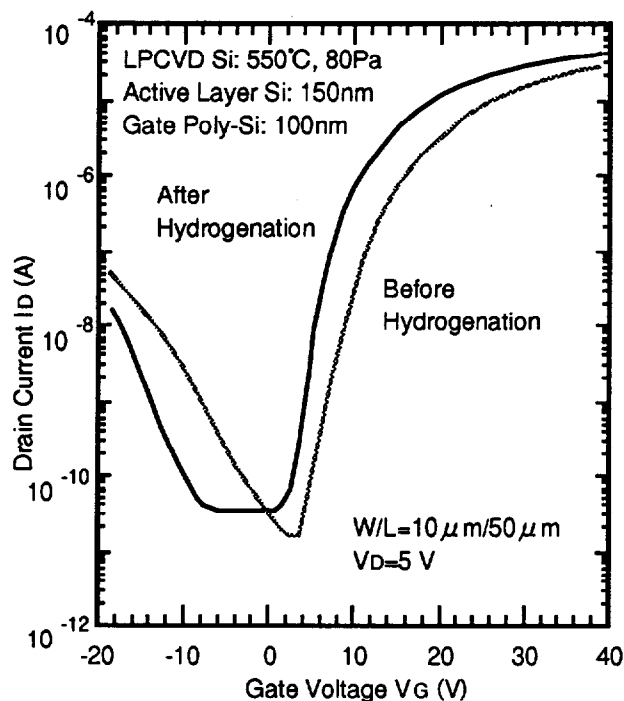


Fig. 2.25 Drain current-gate voltage characteristics of TFT-A.

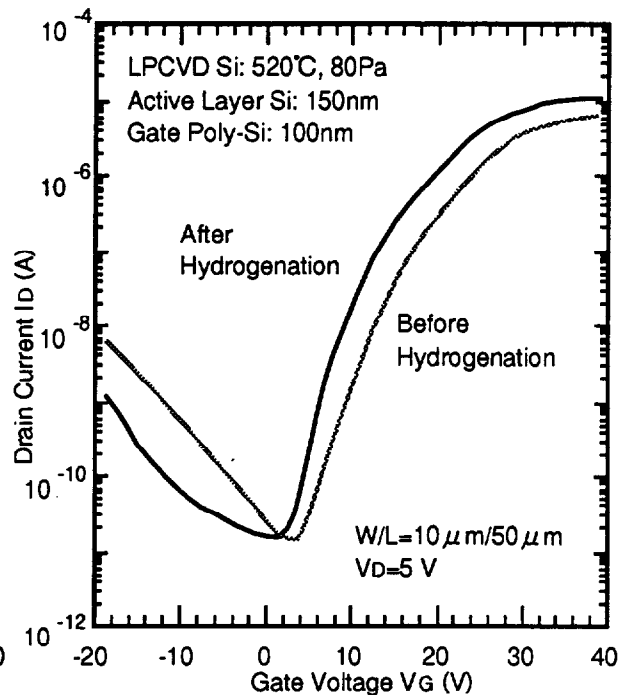


Fig. 2.26 Drain current-gate voltage characteristics of TFT-B.

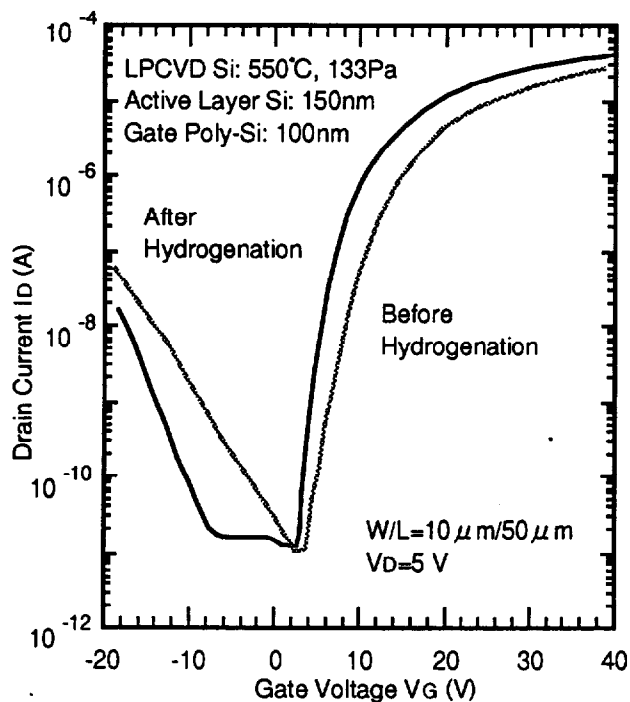


Fig. 2.27 Drain current-gate voltage characteristics of TFT-D.

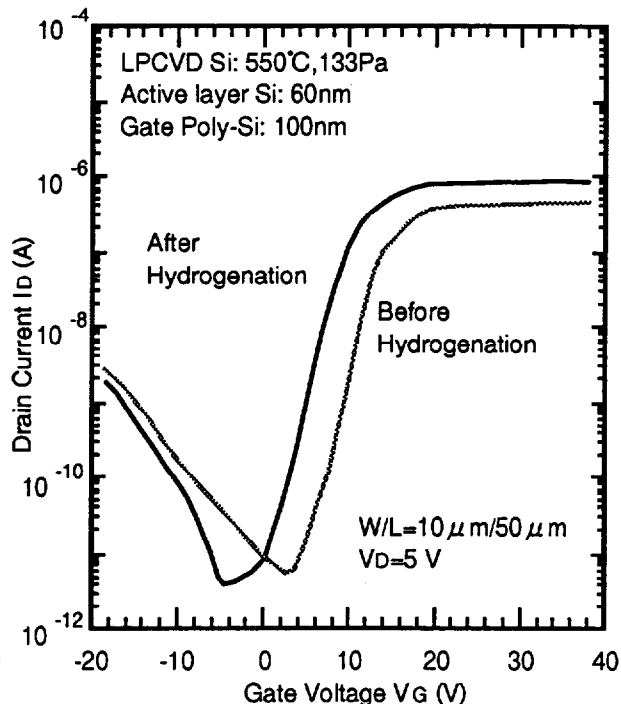


Fig. 2.28 Drain current-gate voltage characteristics of TFT-E.

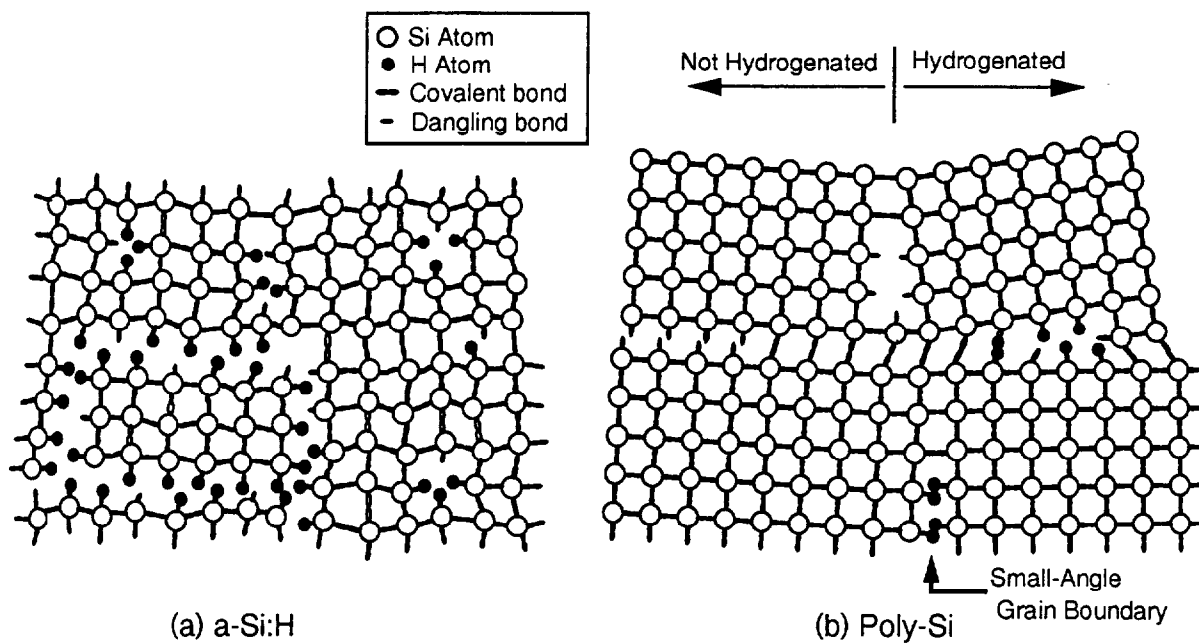


Fig. 2.29 Two-dimensional structure models of a-Si and poly-Si .

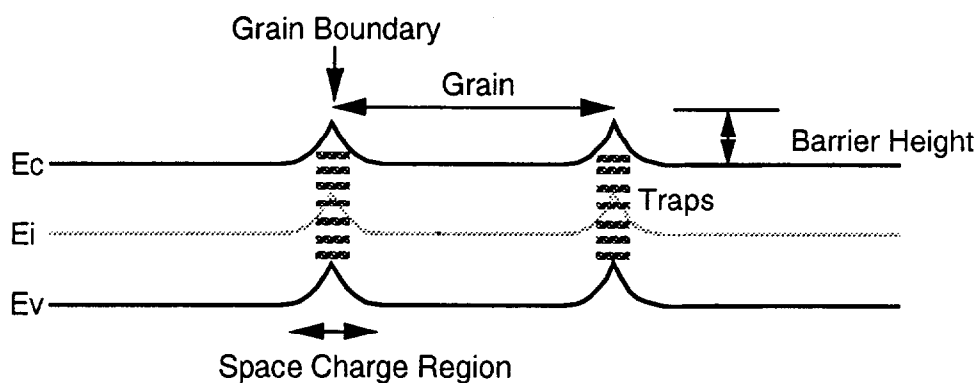


Fig. 2.30 Energy band structure of poly-Si grain boundary.

effective medium model [42]-[46]. Effects of TFT structure and fabrication process on on- and off-currents were discussed by Ono et al. [46]. Figs. 2.31 and 2.32 plot temperature dependence of V_G - I_D characteristics and activation energy of carriers at various V_G , respectively. There are four typical components in leakage current. Component A is the thermoionic field emission current [44]-[45] which has the activation energy of 0.1-0.2 eV and is thermally generated through the traps. Component B (minimum current) which has the activation energy of 0.55 eV (half band gap of Si) is limited by film resistivity. Component C is field emission (tunneling) current with very low activation energy. Component D is generation current through the deep level traps because it is V_G -independent and has a value of 0.53 eV (about half the band gap). From the experiments, estimated N_T is shown in Fig. 2.33 [46]. Hydrogenation effectively reduces the deep level trap states to reduce the leakage current. On-state current is improved by reducing band tail states, improving crystal quality by optimizing SPC conditions or using laser crystallization [46].

According to the model proposed by Fossum et al. [43], an anomalous leakage current at negative gate voltage in an n-channel TFT is described as follows. Figs. 2.34 and 2.35 are a cross section of the drain region and an electron band diagram along the surface between the p+ inversion layer and the n+ drain, respectively. Here, simply assuming that $E_C - E_T = E_T - E_V$, field emission current I_{fe} and generation current I_g [47] are shown as equations (2-3) and (2-6), respectively.

$$I_{fe} = \frac{1}{2} q W X_e N_T \frac{1}{\tau} \left(\frac{V_D}{\epsilon_y} \right) \quad \text{----- (2-3)}$$

$$\tau = \tau_0 \exp \left[\frac{4(2m^*)^{1/2} \{(E_V - E_C)/2\}^{3/2}}{3q \hbar \epsilon_y} \right] \quad \text{----- (2-4)}$$

$$\epsilon_y = \epsilon_1 + \alpha \epsilon_S^D + (-\beta \epsilon_S^I) \quad \text{----- (2-5)}$$

$$I_g = q W t_p |U| W_D \quad \text{----- (2-6)}$$

$$U = -\frac{1}{2} \sigma V_T N_T n_i \quad \text{----- (2-7)}$$

$$W_D = \left[\frac{q}{2\epsilon_S} N_T N_D / (N_T + N_D) V_D \right]^{-1/2} \quad \text{----- (2-8)}$$

where

- W: channel width
- X_e : effective depth of the junction
- N_T : trap density
- τ : time constant for tunneling

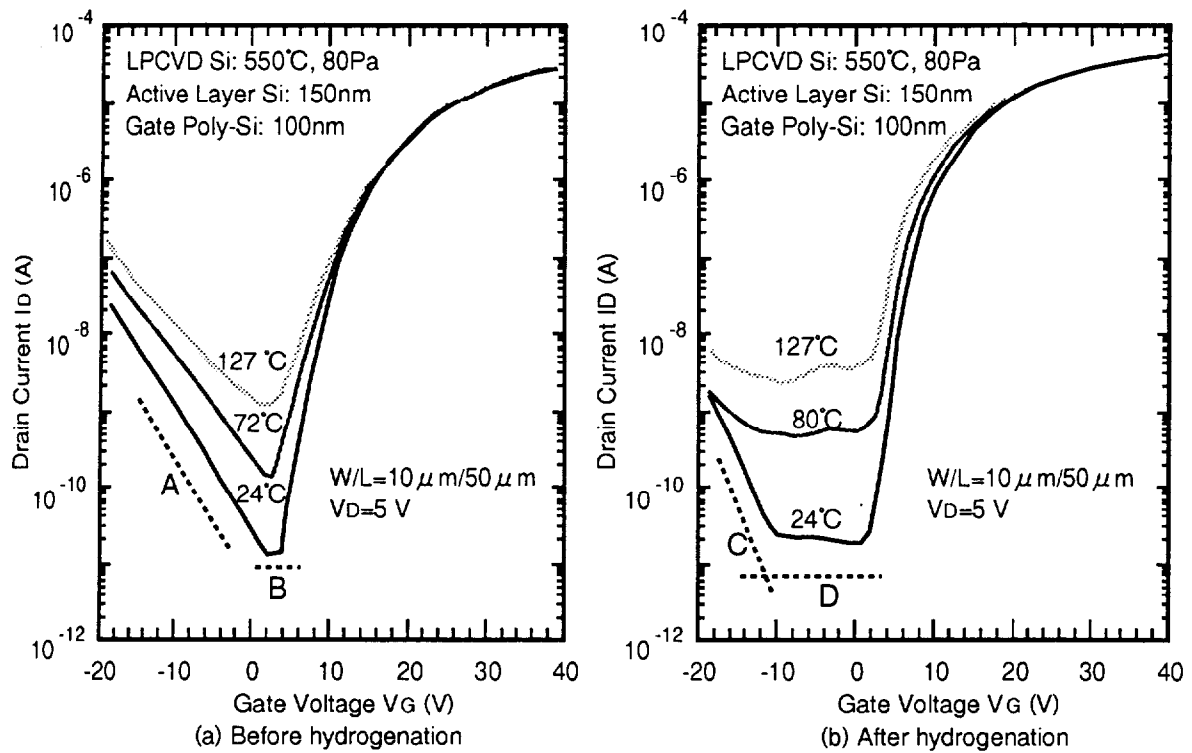


Fig. 2.31 Temperature dependence of drain current-gate voltage characteristics before and after hydrogenation. After Ono et al.[46].

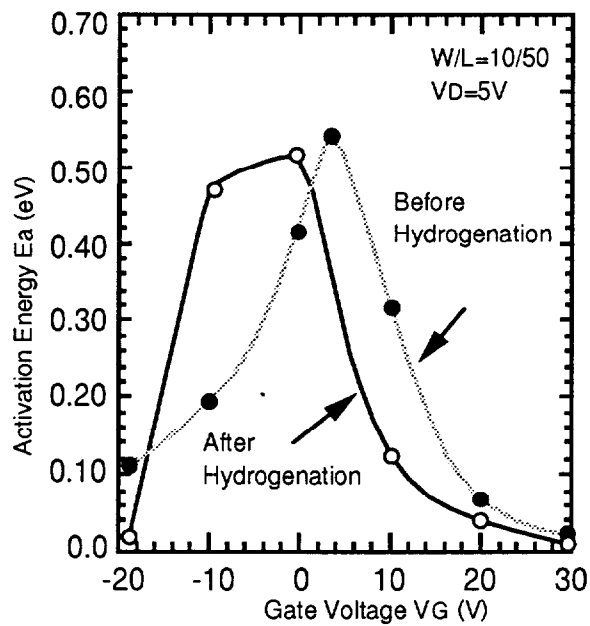


Fig. 2.32 Dependence of activation energy E_a of I_D on gate voltage. After Ono et al.[46].

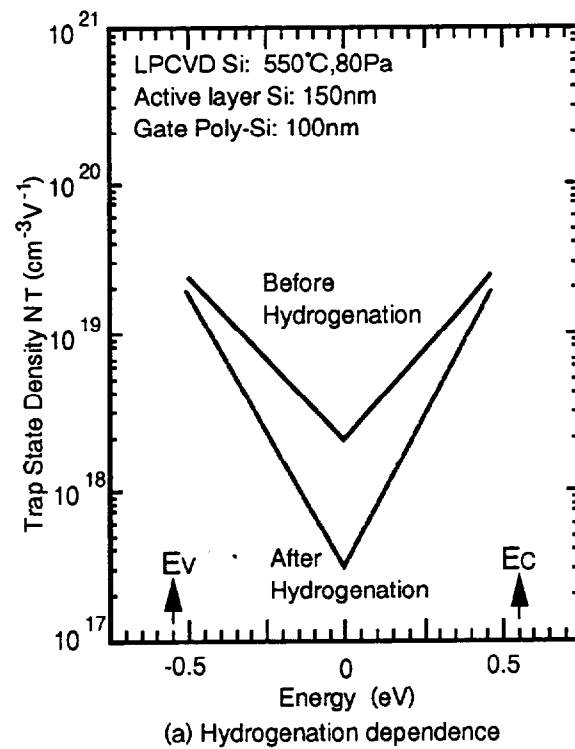
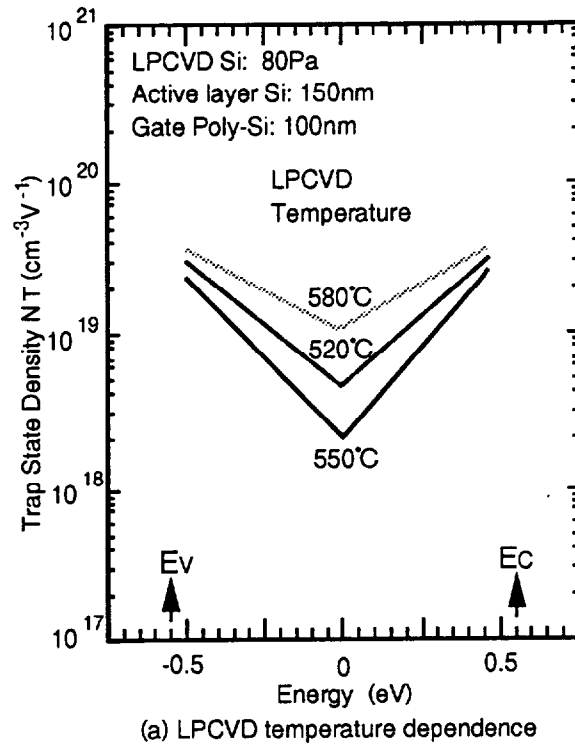


Fig. 2.33 Estimated trap state density profiles before and after hydrogenation. After Ono et al.[46].

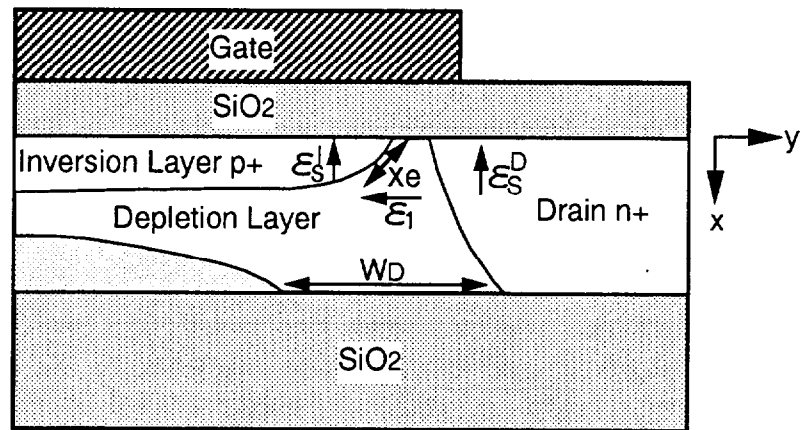


Fig. 2.34 Critical depletion region between p+ inversion layer and n+ drain [43].

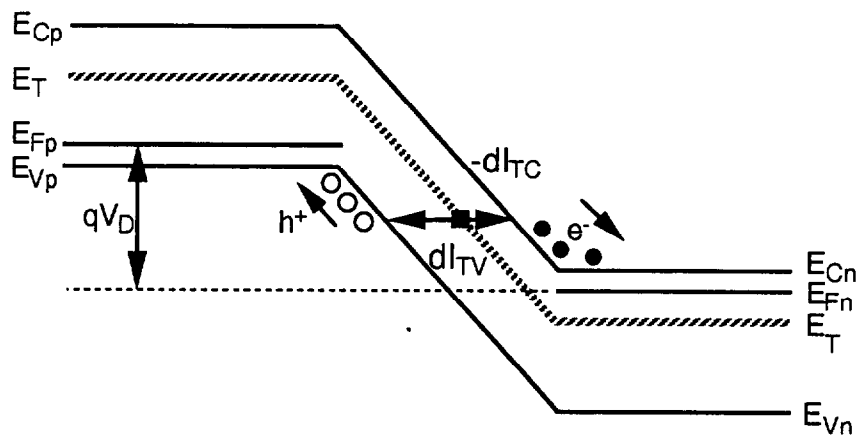


Fig. 2.35 Electron energy band diagram along the surface between the p+ inversion layer and n+ drain [43].

W_D : depletion layer thickness
 σ : carrier capture cross section
 V_t : carrier thermal velocity
 n_i : intrinsic carrier density
 t_p : p-Si film thickness
 ϵ_s : dielectric constant of Si
 N_D : drain carrier concentration .

From these data and equations, reduction of N_T , namely better crystal quality is effective to improve on-characteristics (Figs. 2.31 and 2.33). The tail state governs on-state current [46]. Also, general means to reduce leakage current are implied. Component C of field emission current I_{fe} is proportionally reduced by reducing N_T as shown in equation (2-3). And reduction of drain concentration also reduces I_{fe} resulting in reduction of electric field and increasing carrier tunneling time. Generation current I_g is proportional to film thickness and is reduced by reducing N_T , though depletion layer thickness W_D increases.

Therefore, field emission current I_{fe} is suppressed by reducing deep level N_T by hydrogenation and reducing electric field by using low drain concentration. Generation current I_g is also reduced by reducing deep level N_T and poly-Si film thickness.

Fig. 2.36 plots the drain current dependence on poly-Si film thickness in actual TFTs with and without hydrogenation. The on-current is proportional to film thickness because field-effect mobility (film quality) increases with film thickness. The off-current before hydrogenation is proportional to film thickness verifying that off-current is governed by film resistivity or generation current [46] as shown by equation (2-6). But after hydrogenation, at film thicknesses below 60 nm, the slope of I_D becomes larger than 1. This may be caused by the decrease of drain concentration and drain field strength because of miss control of implantation projection range for very thin films, though N_T is increased from 1.5×10^{17} to 3×10^{17} at film thicknesses of 150 and 40 nm, respectively.

In application of TFTs to LCDs in which TFTs are illuminated by back light, increase of leakage current (photo-generation) must be considered. Fig. 2.37 shows the effect of illumination on V_G - I_D characteristics. TFT was illuminated from the gate side by a halogen lamp. Mobility, V_{TH} and on-current are not changed by illumination. When light strength was increased, the off-current increases and shows a flat bottomed trough shape like Fig. 2.31 when temperature was raised. There are two typical points in the off-current curves. Point A is in a flat region and point B is in the minimum region. At point A where the channel is formed and the drain field is applied, the off-current does not depend on L , but depends slightly on V_D . The photo-generated carriers are extracted instantly by the drain field and conducted through the inversion layer and drain. At point B where the channel is not formed (flat band status), the off-current

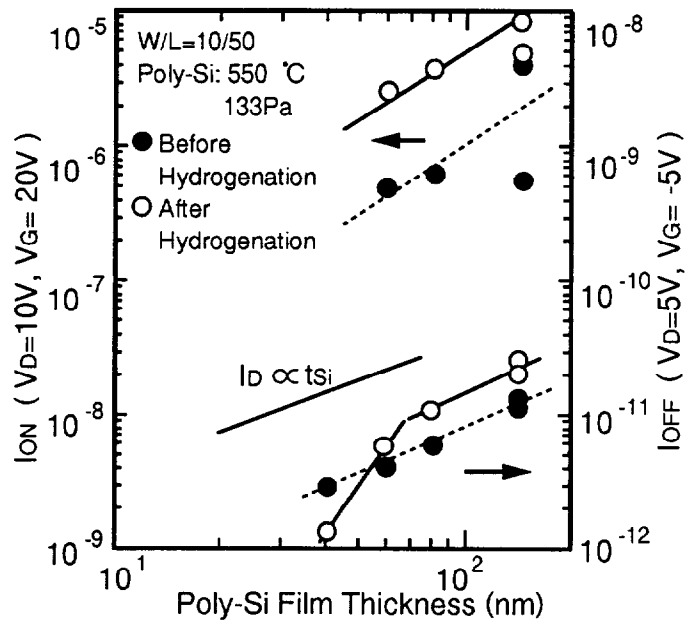


Fig. 2.36 On- and off-current dependence on poly-Si Film thickness.

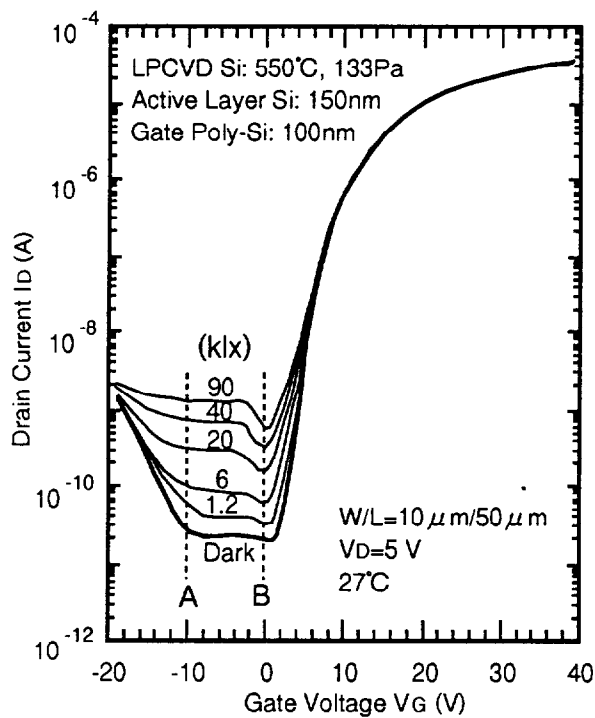


Fig. 2.37 Effect of light illumination on V_G - I_D characteristics after hydrogenation.

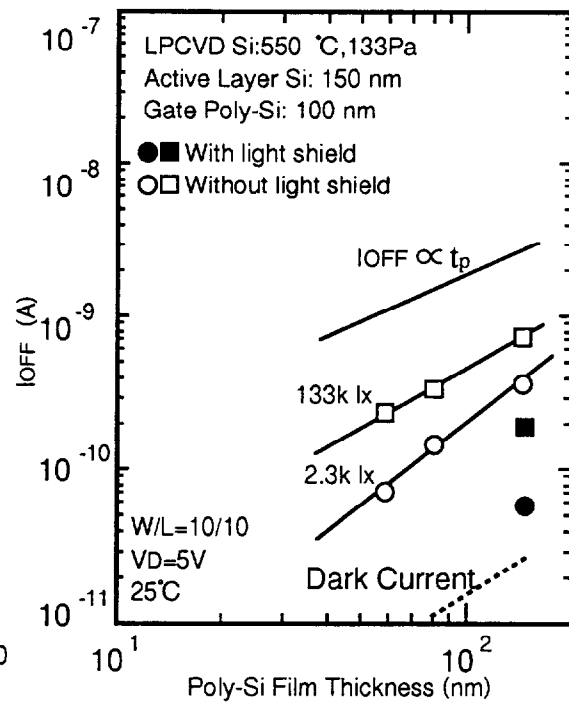


Fig. 2.38 Dependence of off-current on poly-Si film thickness after hydrogenation.

depends on L and V_D . Therefore, it is supposed that photo-generated carriers are conducted by diffusion which is limited by intrinsic poly-Si resistance.

Fig. 2.38 plots the off-current dependence on poly-Si thickness under illumination. From equation (2-6), the slope of 1 is expected. But in an actual TFT, the value is 1.3 to 2. In a projection type display, a very strong light source (over 10^5 lx) is used. Thinning of poly-Si [10], [27], [38], [39] and using a light shield (cover for drain junction) are very effective to reduce photo-generated current.

2.2.6 Application of poly-Si TFTs to driver integrated LCDs

(1) Characteristics of logic circuit operations

In this section, as the optimized fabrication process, device D (Fig. 2.26 and Table 2.3) was used for the TFT-LCD with driver integration. As the component of logic circuits, a primitive and simple E-E type inverter was selected because it is composed of only n-channel TFTs.

A particular concern of TFTs on glass substrates for which thermal conductivity is about two orders of magnitude lower than that of Si wafer, is thermal breakdown by self-heating. In the off-state of an E-E type inverter (Fig. 1.16), most of V_{DD} is applied to load TFT ($V_G = V_D \leq V_{DD}$) and a penetration current flows. Power consumption is about $V_{DD} \times I_D$. Under these conditions, safe operation conditions without thermal breakdown were studied experimentally. Fig. 2.39 is an example photo showing breakdown of load TFT in a level shifter. Fig. 2.40 shows the safe operation area of load MOS TFTs with different dimensions of E-E type inverters. From these results, TFTs with $W/L = 60/35$, $60/40$, and $30/60$ (μm) were used in logic circuit design.

Table 2.4 lists the characteristics of 51-stage ring oscillators. Fig. 2.41 is a photograph of a ring oscillator. The inverter is an E-E type. Type A with a drive TFT channel length of $10 \mu\text{m}$ operates at 75 ns/stage, and type B with a drive TFT channel length of $5 \mu\text{m}$ operates at 11 ns/stage at V_{DD} of 30 V. Power dissipations are 2.1 and 4.7 mW, respectively. This high speed operation is good enough to make logic circuits with the developed n-channel TFTs. Considering the power dissipations, a channel length of $10 \mu\text{m}$ (Type A) has been adopted for drive TFTs.

(2) Fabrication of Poly-Si TFT-LCDs with driver integration

In this section, a 10" VGA-level VDT (video display terminal) with 640×400 pixels was assumed as a goal to prove the driving ability of the developed TFTs and driving circuits.

Fig. 2.42 is a schematic diagram of the drive circuit integrated display which has a display area with 3.3" diagonal ($59.4 \text{ mm} \times 59.85 \text{ mm}$) and $396(132 \times 3, \text{H}) \times 133(\text{V})$ dots. Fig. 2.43 is a schematic cross section of

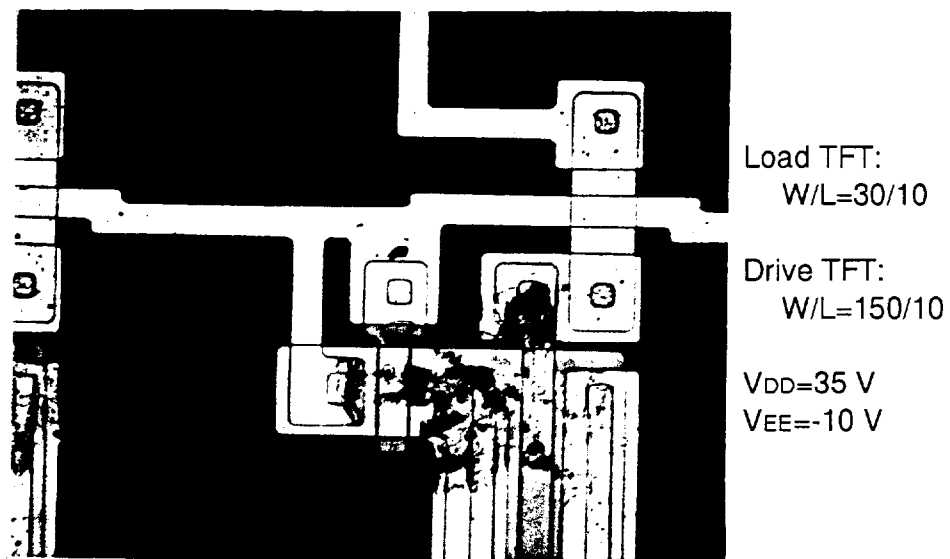


Fig. 2.39 Example photo showing thermal breakdown of E-E type inverter.

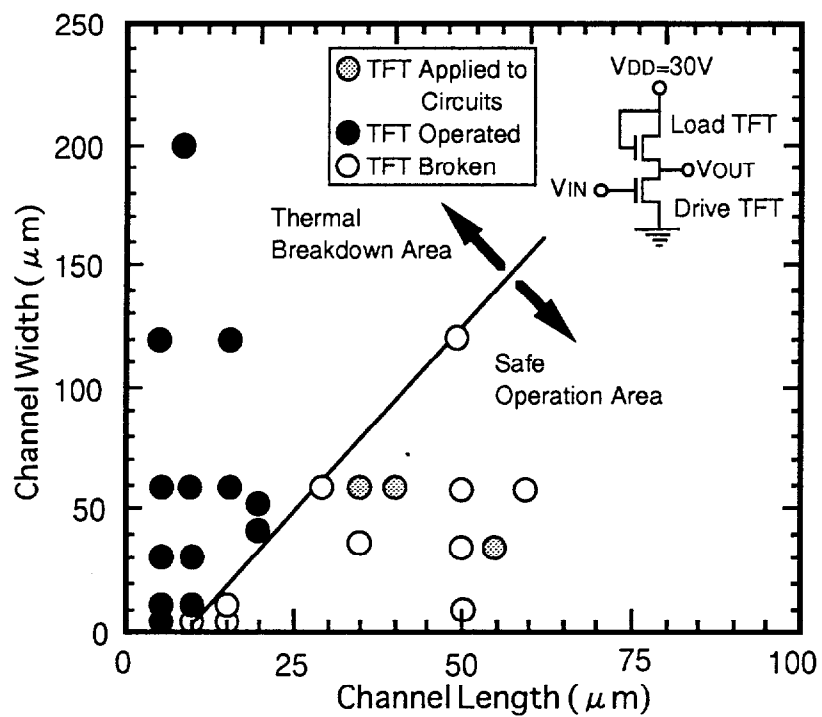


Fig. 2.40 Safe operation area of Load MOS TFTs in E-E type inverters.

Table 2.4 Characteristics of E-E type 51-stage ring oscillators

Circuit Type	A	B
Load TFT W/L	30 μ m / 60 μ m	30 μ m / 30 μ m
Drive TFT W/L	50 μ m / 10 μ m	50 μ m / 50 μ m
Delay Time / Stage (V _{DD} =30V)	75 ns	11 ns
Power Consumption / Stage (V _{DD} =30V)	2.1 mW	4.7 mW

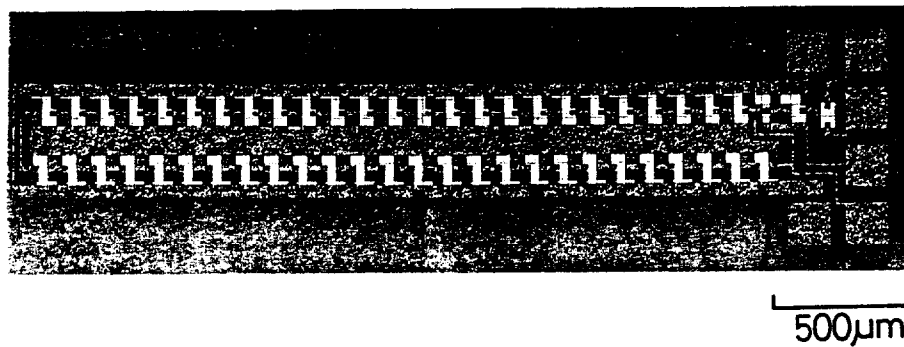


Fig. 2.41 Photograph of 51-stage ring oscillator.

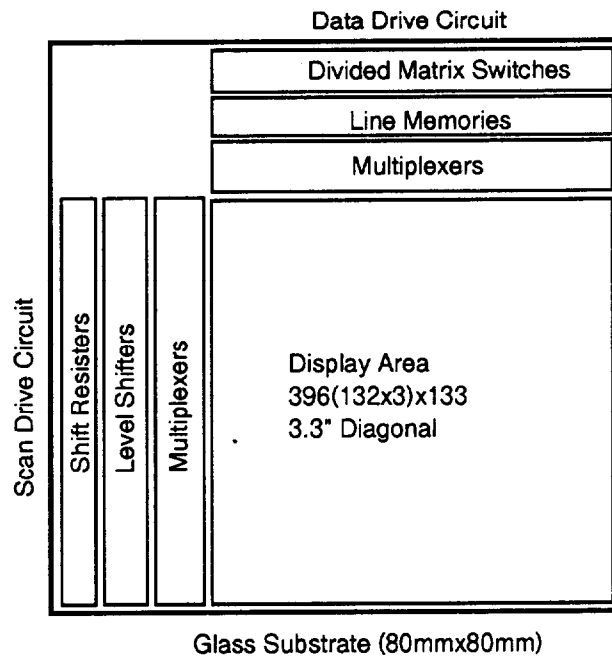


Fig. 2.42 Schematic diagram of drive circuit integrated display.

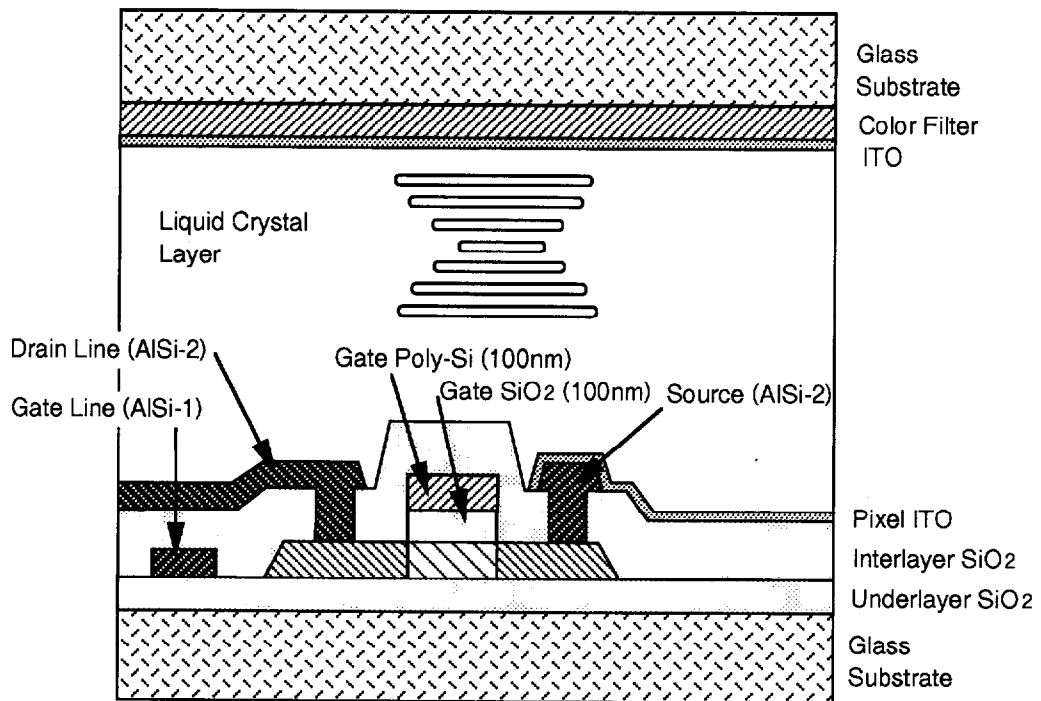
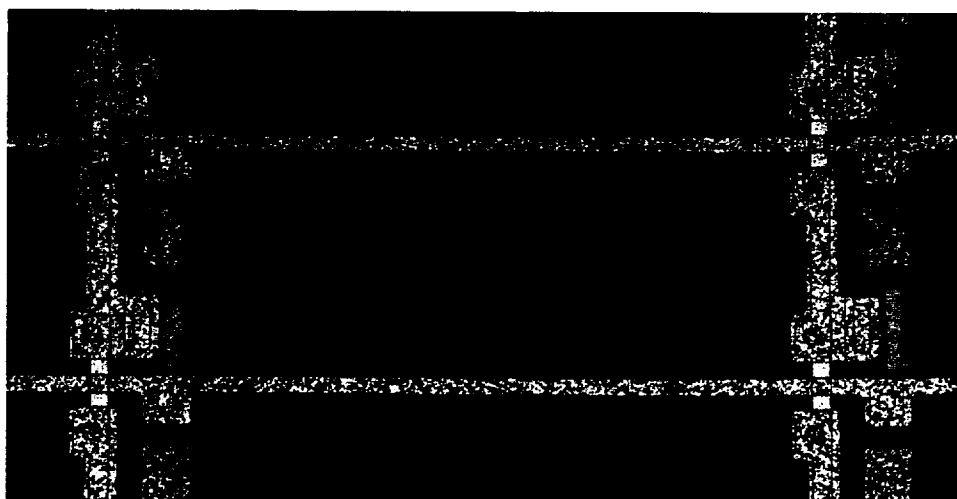


Fig. 2.43 Schematic cross section of poly-Si TFT-LCD with driver integration.



100 μm

Fig. 2.44 Photograph of pixel.

poly-Si TFT-LCD with driver integration. The pixel ITO was fabricated on the Al electrode of the TFT source. Thickness of TN liquid crystal was 5.5 μm . Fig. 2.44 shows a photograph of the pixel. The pixel size was 150 μm $\times$ 450 μm . L and W of pixel TFTs were 50 and 10 μm , respectively. Aperture ratio was 67 %. Two-layer aluminum metallization was used for drain (300 nm thick) and scan (600 nm thick) lines.

Fig. 2.45 shows a photograph of the integrated drive circuits in the active matrix substrate. The scan drive circuits and data drive circuits were integrated on the left and upper right sides of the display area (DP), respectively. Fig. 2.46 shows a photograph of a multi-color (8 color) display image of a poly-Si TFT LCD with fully integrated drive circuits. The whole display area was driven with a frame frequency of 60 Hz and a maximum supply voltage of 30 V. The scan drive circuits were composed of two-phase clock dynamic shift resistors (SRs) and buffers (BFs), level shifters (LSs) with three step inverters, and multiplexers (MPs) that had very large TFTs with $W=1830\ \mu\text{m}$ and $L=10\ \mu\text{m}$ to drive a large scan line load. These scan circuits operated at 200 Hz - 100 kHz with a maximum supply voltage of 30 V and a load capacitance of 350 pF, which was equal to the load of the scan line with 640 $\times$ 3 cells (Fig. 2.47).

The data drive circuit was composed of divided matrix switches (DMSs) [48], line memories (LMs) using inverters, and MPs. A set of 12 data lines was driven by block scanning in the DMSs. This data drive circuit operated at 6 MHz (effective data scan speed of 72 MHz) with a maximum supply voltage of 30 V and the load capacitance of 22 pF, which was equal to the load of the data line with 400 cells (Fig. 2.48).

Therefore, these scan and data drive circuits would be able to drive LCDs with 640($\times$ 3) by 400 dots. The numbers of outer connections for scan and drive circuits were 14 and 49, respectively, about one tenth of the connections for an LCD without circuit integration. The number of outer driver LSLs also would be reduced to one tenth for a 640 ($\times$ 3) 400 dot LCD.

Table 2.5 summarizes the operation characteristics of the 3.3" poly-Si TFT-LCD with driver integration. Tentative specifications for the 10" LCD (640 $\times$ 400) are also listed for comparison. Both scan and data drivers had sufficient ability to drive 10"-level TFT-LCDs. More detail of operation characteristics are in the literature [49].

In this section, primitive E-E type inverters using only n-channel TFTs were used to compose the shift resistors in driving circuits to confirm the driving ability of the developed TFTs. Considering the application of TFTs to practical driving circuits of recent high resolution TFT-LCDs, increasing operation speed and reduction of power consumption were studied with CMOS configuration [50]. Figs. 2.49 and 2.50 show the frequency characteristics of output voltage and power consumption of shift resistors, respectively. It was confirmed that the maximum operation speed and power consumption of CMOS shift resistors at V_{DD} of 20 V were noticeably improved from 25 kHz to 1.25

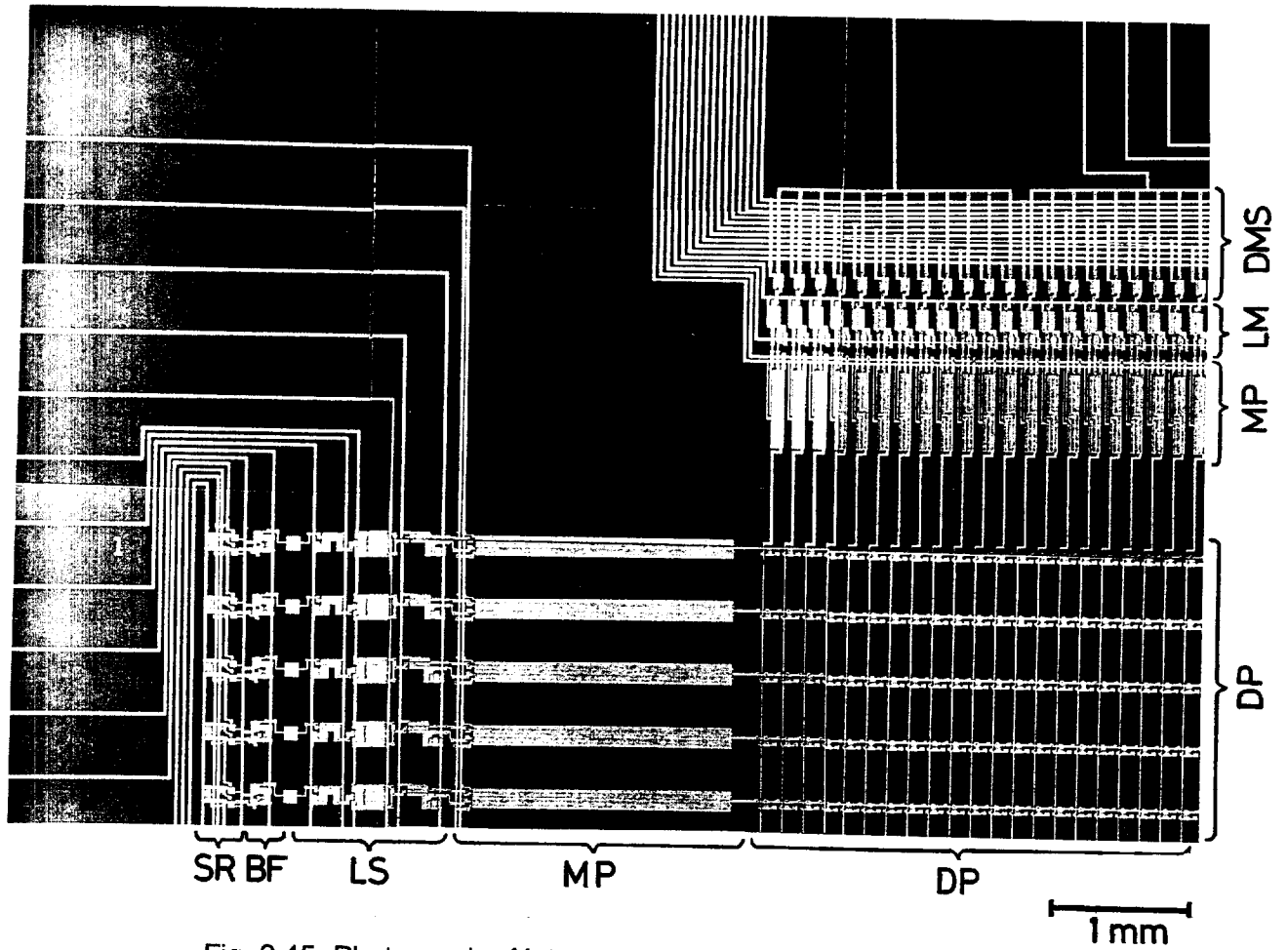


Fig. 2.45 Photograph of integrated drive circuits.
 Left side: scan drive circuits. Upper side: data drive circuits.

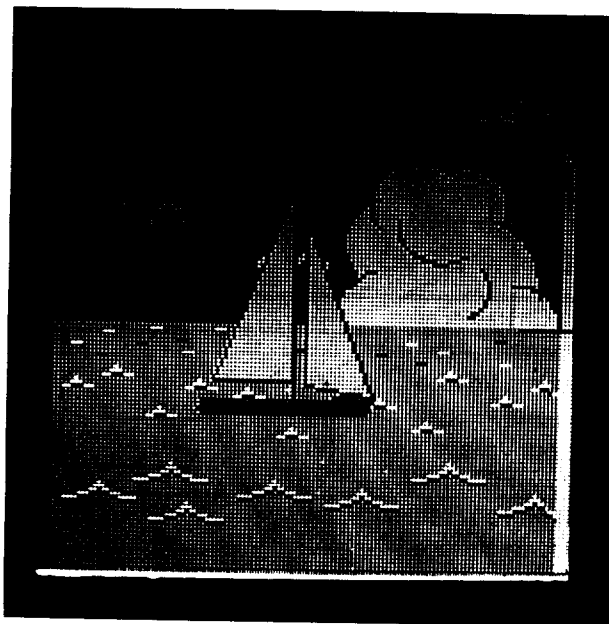


Fig. 2.46 An example multi-color display image
 of 3.3" diagonal poly-Si TFT-LCD with fully integrated
 drive circuits and 132(×3) × 133 dots.

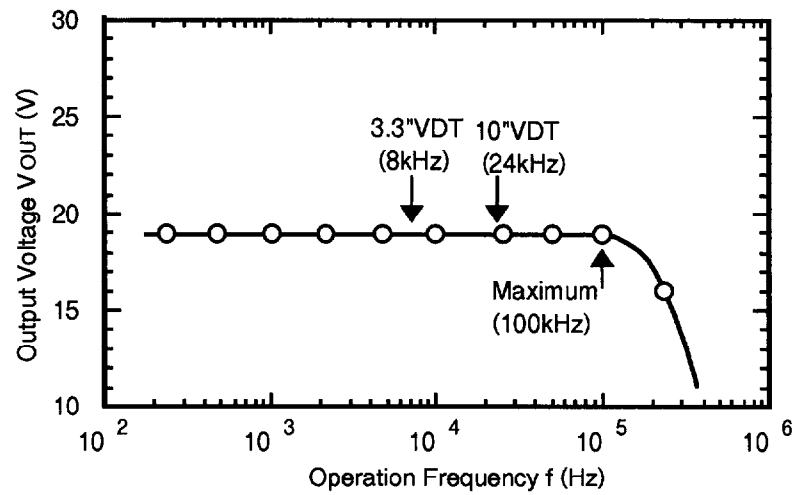


Fig. 2.47 Frequency characteristics of scan drive circuits.

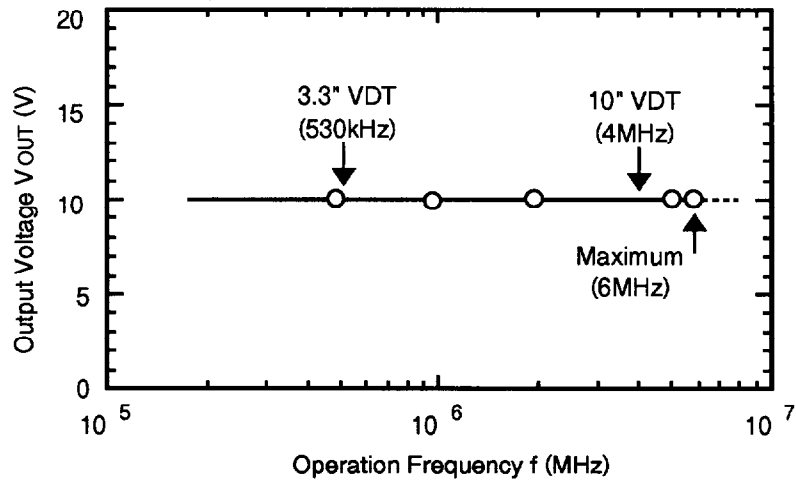


Fig. 2.48 Frequency characteristics of data drive circuits.

Table 2.5 Comparison of operation characteristics of the 3.3" Poly-Si TFT-LCD with driver integration and the 10" VDT

Circuits	Characteristics	10" VDT	3.3" LCD
Scan Driver	Operation Frequency (kHz)	24	100-250
	Source Voltage (V)	30	30
	Output voltage (V)	≥ 18	19
	Input Voltage (V)	≤ 20	12
	Power Consumption (W)	-	0.68
Data Driver	Operation Frequency (MHz)	4	6
	Source Voltage (V)	30	30
	Output voltage (V)	≥ 10	14
	Input Voltage (V)	≤ 20	16
	Power Consumption (W)	-	0.3
Display Area	Drive Voltage (V)	≤ 20	18
	TFT Off Current (pA)	≤ 30	30
	Power Consumption (μ W)	-	3

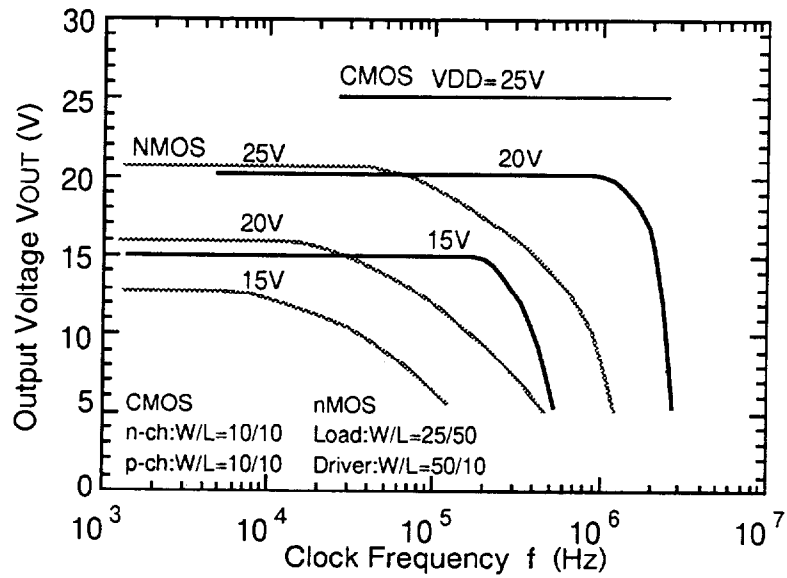


Fig. 2.49 Output voltage versus clock frequency characteristics of CMOS and nMOS shift registers. After Takabatake et al.[50].

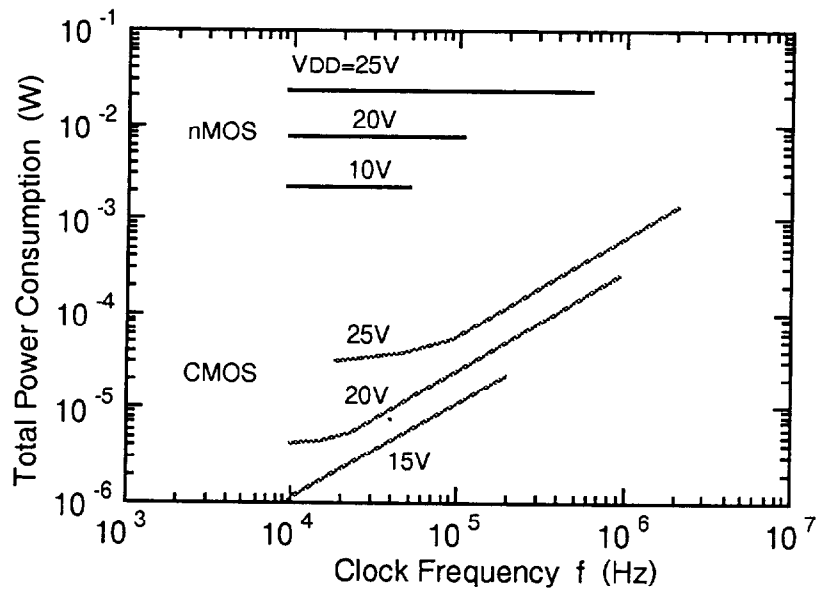


Fig. 2.50 Power consumption versus clock frequency characteristics of CMOS and nMOS 10-stage shift registers. After Takabatake et al.[50].

MHz, and 8 mW to 0.16 mW, respectively [50]. The CMOS shift resistors were considered to be promising candidates for integrated peripheral circuits of poly-Si TFT-LCDs with 1120 (x3) x 780 (VGA) dots. Additional research showed that the developed high-performance TFTs had sufficient ability to integrate peripheral circuits for TFT-LCDs in the CMOS configuration also.

2.2.7 Summary

High-performance low-temperature n-channel poly-Si TFTs were developed by a 600°C process on a hard glass substrate. Poly-Si films were deposited by LPCVD and crystallized by thermal annealing at 600°C. The X-ray diffraction intensity (an indicator of crystallinity) of poly-Si (111) depended closely on poly-Si deposition temperature and showed a maximum at 550-560°C. The V_{TH} and μ_{FE} of TFTs showed a minimum and a maximum at this deposition temperature, respectively. Multi-gate TFTs were used to study effective hydrogenation by pure H_2 plasma. Shortening of the unit channel length reduced the V_{TH} of TFTs with thick poly-Si gate. Thinning of the gate was remarkably effective to reduce V_{TH} , independently of channel length.

The developed TFTs with poly-Si deposited at 550°C and the thin gate of 100 nm had a V_{TH} of 6.2 V, μ_{FE} of 37 cm²/V·s, and on/off ratio of 6×10^6 . High-speed operation of E-E-type ring oscillators showed application ability for logic circuits. A 3.3" diagonal TFT-LCD with fully integrated drive circuits was operated. These results showed the possibility of large area LCDs with driver integration using hard glass substrates. The improvements of TFT structure for low off-current and CMOS configuration for logic circuits should contribute to realization of practical devices for TFT-LCDs.

2.3 Transparent storage capacitor structure for AM-LCDs

2.3.1 Poly-Si TFT-LCD and storage capacitor

Fig. 2.51 illustrates two auxiliary capacitor structures for AM-LCDs. The additional capacitance (C_{add}) structure which makes a capacitance with a previous gate line, is common for amorphous-Si (a-Si) TFT LCDs. This structure has a large capacitance load for the gate line. The storage capacitor structure (C_{STG}) is used for high resolution LCDs with high density gate line. In this structure, load for the gate line is reduced and reverse gate scanning becomes possible. But, generally, the auxiliary capacitance structure decreases aperture ratio.

The fabrication of storage capacitors that are combined in parallel with a liquid crystal capacitance began with the introduction of TFT-addressed LCDs [51]. In the early period of LCD development, CdSe TFTs were used with storage capacitors to solve the problem that CdSe TFTs had a large leakage current [52], [53].

LCD image characteristics depend greatly on the liquid-crystal drive voltage, which is influenced by both the liquid crystal resistance and the off-resistance of the TFTs. Recent a-Si TFT LCDs have brought noticeable advances not only in display size, but also in definition. Therefore the pixel size has decreased, resulting in a decrease in the liquid crystal cell capacitance. The specifications for the holding characteristics have become more severe. The amorphous-Si TFT must have a sufficiently low off-current in the dark. However, an increase in the off-current because of back lighting and higher temperature, and a decrease in the resistivity of the liquid crystal itself because of this severe environment, are fundamental concerns in the production of auxiliary capacitors for realizing high-stability TFT LCDs. The auxiliary capacitor also has the advantage of reducing the residual DC voltage component which causes image sticking in TFT LCDs.

The first low-temperature poly-Si TFT LCD was reported in 1983 [6]; at that time, storage capacitors were necessary to compensate for the large off-current [7]. Newer low-temperature poly-Si TFTs have realized a sufficient low off-current for large LCDs by the use of a thin poly-Si active layer [39], and drain engineering such as an off set gate [54] or dual gate [3]. However, as mentioned above, the holding characteristics also depend on the liquid-crystal resistance, and the residual DC component depends on the TFT structure (C_{gs}). Therefore, auxiliary capacitors are still necessary for poly-Si TFT LCDs so that high stability of the image quality is realized.

The basic and ideal structure of a large-capacity storage capacitor is ITO (pixel electrode)-insulator-ITO (buried common electrode) structure. It is a transparent structure with hardly any aperture ratio reduction. Low-temperature poly-Si TFTs generally use hydrogenation to improve the TFT characteristics, especially the on-characteristics as

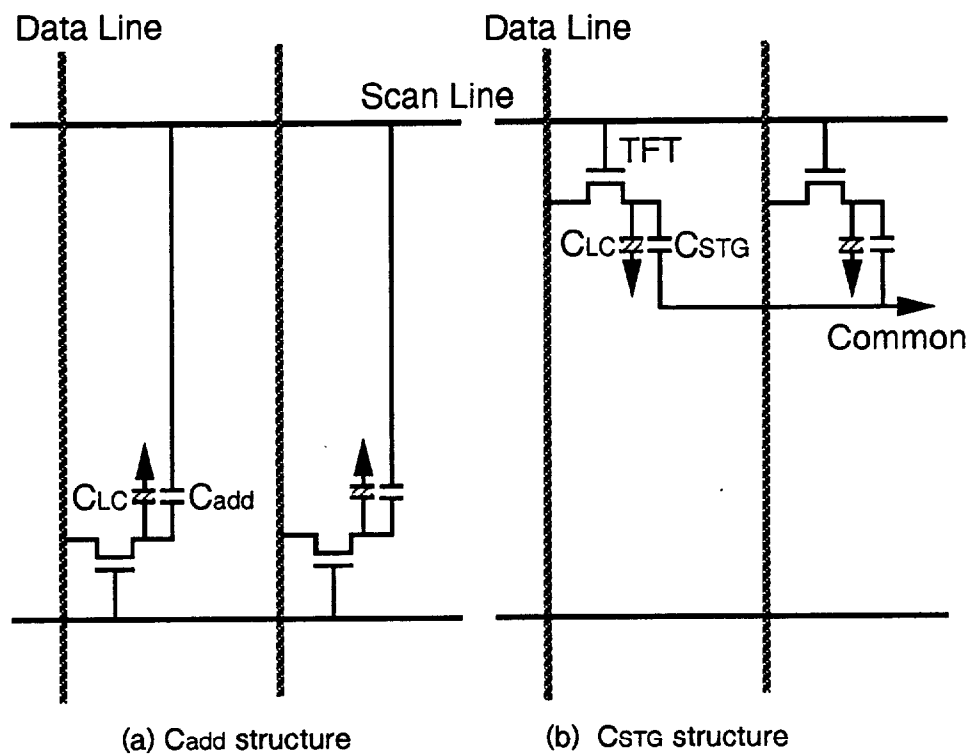


Fig. 2.51 Equivalent circuit of liquid-crystal cell with auxiliary capacitors.

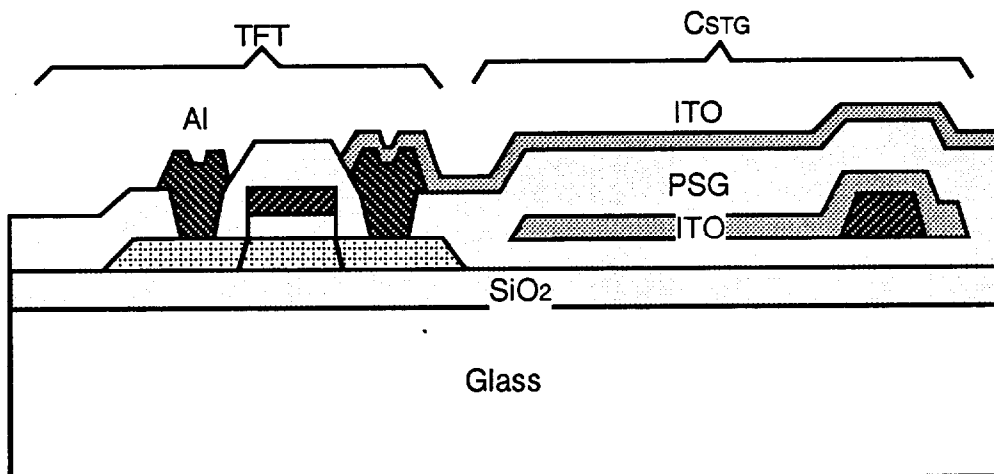


Fig. 2.52 Cross-sectional view of poly-Si TFT with storage capacitor.

discussed in section 2.2.4. The ITO characteristics change with heat treatment and effect of hydrogenation must be considered.

In this section, a storage capacitor fabrication process for low-temperature poly-Si TFT was studied. Compatibility with hydrogenation using pure hydrogen plasma was required. The changes in characteristics of bare ITO and buried ITO during heat treatment and hydrogenation were investigated. The storage capacitor with the ITO(pixel)-SiO₂-ITO(buried) structure was fabricated as the equivalent circuit shown in Fig. 2.51(b). To confirm the function of the storage capacitor, the hold and drive characteristics of the TFT were evaluated.

2.3.2 Characterization of ITO in heat treatment process

(1) Bare ITO Characteristics

Fig. 2.52 shows a cross-sectional view of the poly-Si TFT with a storage capacitor. The common electrode line was fabricated in the same step as the gate layer and placed in parallel with the gate line. Only one photo-mask to pattern the buried ITO was added to fabricate the storage capacitor.

An ITO film (100 nm) was deposited by DC sputtering using In₂O₃-SnO₂(5%) target and Ar plasma. Transmission was observed at wavelengths of 400-600 nm, and the sheet resistance was measured by a 4-probe method. The crystallinity was inspected by XRD, EBD and TEM.

In storage capacitor fabrication, the ITO must be buried in the insulator. APCVD SiO₂ was used as insulator and ITO was heat-treated in O₂ and H₂/N₂ ambient. In this section, the effects of these treatments on ITO were studied.

Fig. 2.53 plots the ITO-sheet resistance against annealing temperature in various atmospheres. In N₂ annealing, the sheet resistance decreased sharply in the temperature range 150-250°C. The sheet resistance was almost constant for the high-temperature region, and it had the same value as that in forming-gas (H₂/N₂) annealing. However, in O₂, the sheet resistance increased with increasing annealing temperature. This is caused by the decreased number of oxygen vacancies to contribute to carrier generation [55].

Fig. 2.54 shows the dependence of the X-ray diffraction intensity of In₂O₃ (222) on the annealing temperature in various atmospheres. The X-ray intensity increased sharply at 200-250°C in N₂, showing that crystallization started at this temperature. The XRD intensity was saturated at higher temperature, and did not depend on the gas atmosphere. However, the intensity was remarkably decreased by hydrogen-plasma treatment, showing that the ITO was reduced to indium metal in the hydrogen plasma, as has also been reported for tin oxide [56].

From these results, it was concluded that the crystallization of the ITO started at about 200 °C in N₂, as has been reported in relation to reactive evaporated ITO [57], [58]. And crystallinity was improved at temperatures over 300°C in every atmosphere. The sheet resistance

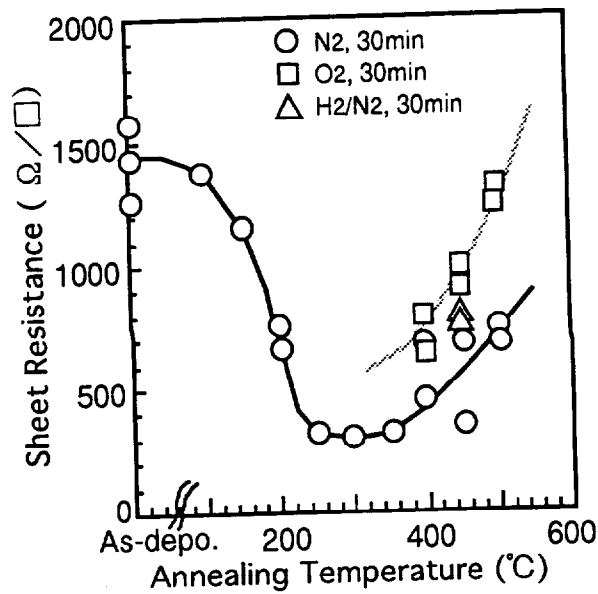


Fig. 2.53 ITO-sheet resistance dependence on annealing temperature in various atmospheres.

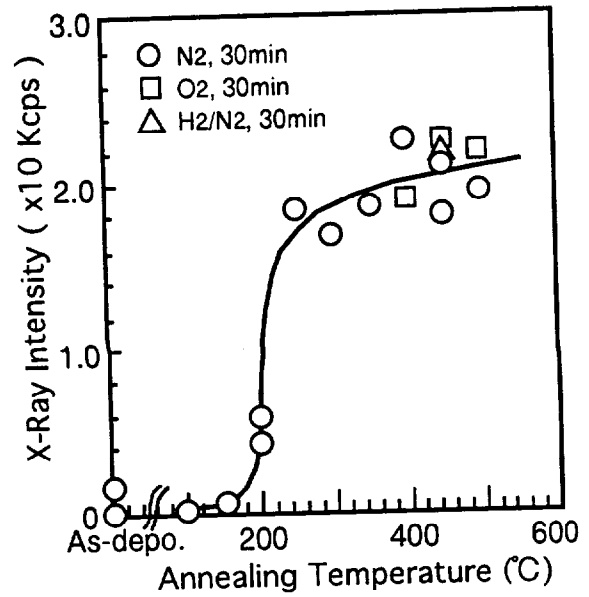


Fig. 2.54 Dependence of X-ray diffraction intensity of In₂O₃ (222) on annealing temperature.

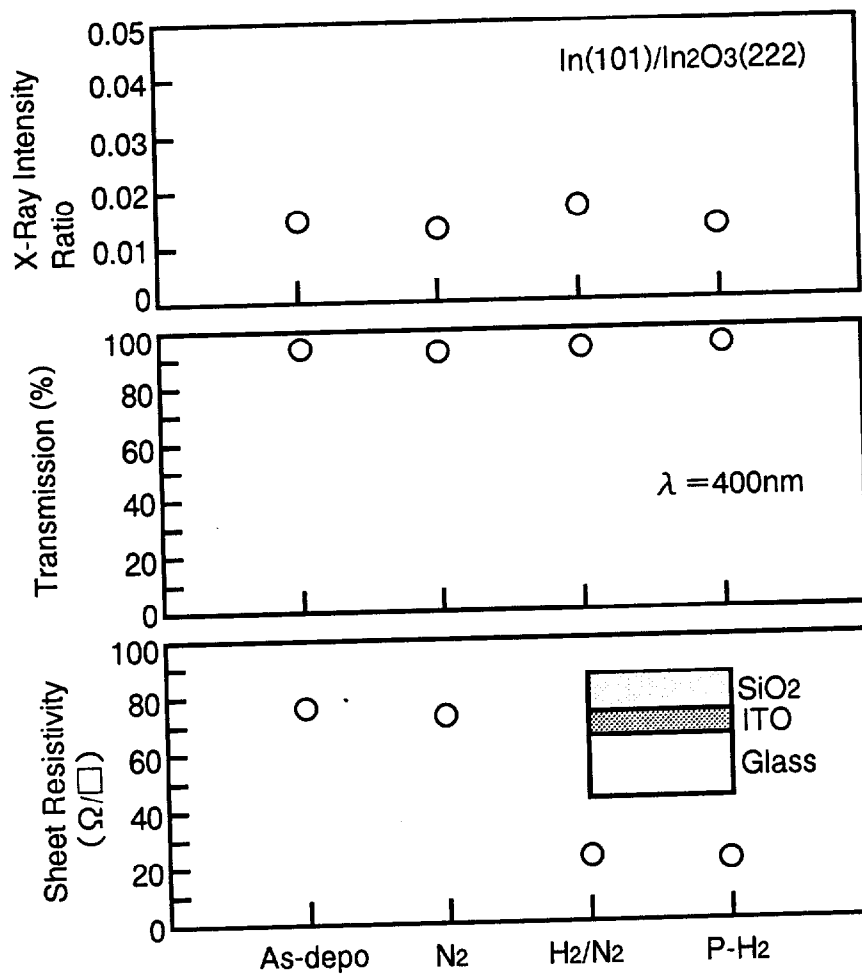


Fig. 2.55 Dependence of buried-ITO characteristics on annealing atmospheres.

decreased on crystallization. However, the sheet resistance was increased by annealing in O_2 at 400-500°C. It was assumed that the numbers of oxygen vacancies to act as donors decreased with O_2 annealing. Pure hydrogen plasma strongly reduced ITO to indium powder. It is necessary to protect ITO during the hydrogenation process in the fabrication of storage capacitors.

(2) Buried-ITO characteristics

Fig. 2.55 shows the dependence of buried-ITO characteristics on annealing atmosphere. The ITO coated with APCVD SiO_2 (300 nm) was heat-treated at 450°C for 30 min, and characterized after SiO_2 was removed by hydrofluoric acid. The X-ray intensity ratio and transmission were almost constant for every treatment. The sheet resistance decreased after treatment in forming gas and hydrogen plasma. The results of TEM and EBD observations for the cross section of the ITO covered with SiO_2 showed polycrystalline grains of ITO and their diffraction spots, even after hydrogenation.

These results indicated that the APCVD SiO_2 protected the ITO from reduction, even in hydrogen plasma. However, as explained in Fig. 2.56, hydrogen plasma improved the TFT characteristics, although the TFT used 400 nm thick PSG. Hydrogen would be able to penetrate 1-2 μm PSG (passivation film) and 100 nm SiO_2 (gate oxide) as shown in Fig. 2.17. Therefore, it was assumed that only the reduction ability for the ITO was decreased by APCVD SiO_2 cap. The PSG (SiO_2 with 4 mol% P_2O_5) also protected the ITO, as shown in the final device in Fig. 2.52. Thus, carrying out hydrogenation after the deposition of SiO_2 (PSG) on the ITO was reasonable for fabrication of the storage capacitor.

2.3.3 Pixel structure and its fabrication process

Hydrogenation is a useful means of improving the characteristics of low-temperature poly-Si TFTs. Pure hydrogen plasma and a thin poly-Si gate mentioned in section 2.2.4 were used in this experiment to obtain effective hydrogenation.

The TFT had a conventional n-channel MOSFET structure as shown in Fig. 2.52. The substrate was Asahi AN glass (100 mm x 100 mm, 1.1 mm thick). An underlayer of SiO_2 (400 nm) was deposited by APCVD. Active layer poly-Si (60-80 nm) was deposited at 550°C according to the results of section 2.2.5. The poly-Si was annealed at 600 °C for 20 h in N_2 to crystallize it, and it was then patterned into islands. After chemical cleaning, a gate oxide (100 nm) was deposited by APCVD at 480°C. Gate poly-Si (100 nm) was deposited by LPCVD at 550°C. After gate patterning, phosphorous ions were implanted at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ and 30 kV (minimum operation voltage of implantor) to form the source, drain and gate regions by a self-alignment structure. Projection range was controlled by using cap SiO_2 . After deposition of PSG for passivation, thermal annealing was carried out at 600°C for 20 h in N_2 to activate the

implanted ions. After the first metallization and patterning of AlSi (2%) for the crossover lower electrode, the first ITO layer (100 nm) was sputtered on for the storage common electrode. Then, PSG was deposited by APCVD for the crossover insulator and the storage capacitor insulator. After the second AlSi (2%) metallization for the source and drain electrode, the substrate was annealed at 400 °C for 30 min in forming gas. Hydrogenation was carried out in a plasma reactor (13.56 MHz) at 300°C for 1 h in pure hydrogen. Finally, ITO was deposited as a transparent pixel electrode.

2.3.4 Driving ability of poly-Si TFT for storage capacitor

(1) Writing characteristics

Fig. 2.56 shows the typical characteristics of the TFT before and after hydrogenation. Both the on and off characteristics were remarkably improved by hydrogenation. The off-current was successfully reduced by the use of thin poly-Si (60-80 nm), in comparison with the conventional 150 nm TFT shown in section 2.2.4. Table 2.6 summarizes the typical characteristics of the TFT before and after hydrogenation. This TFT has sufficient ability to be used in peripheral drive circuits for grey scale presentation [59].

Table 2.6 Typical TFT characteristics before and after hydrogenation

Hydrogenation	Before	After
Threshold Voltage (V)	12.0	7.5
Field-Effect Mobility (cm ² /Vs)	21.0	26.2
On-Current (mA)	8.0	30.0
Off-Current (pA)	20.0	9.0

Fig. 2.57 shows the discrete TFT with a storage capacitor that was used to study driving ability. The channel width W, channel length L, and storage capacitance C_{STG} were 50 μm, 10 μm, and 3 pF, respectively. This TFT was scaled up, and W was five times larger than that for an actual pixel TFT (Fig. 2.60) to reduce measurement noise.

Fig. 2.58 shows driving waveforms for the storage capacitor produced using the poly-Si TFT shown in Fig. 2.57. More than 95 % of the drain voltage of 8 V (- 3V to 5 V) was written in about 2 μs and more than 95 % of the drain voltage of 8 V(5 to -3 V) was erased in about 2 μs as shown in Figs. 2.58(a) and (b), respectively.

To achieve complete TFT-LCD operation, the address time T_A must satisfy the relationship

$$T_A = 1/(F_f N) \geq T_D + T_{IN} \text{ -----(2-9)}$$

where T_D, T_{IN}, F_f and N are the gate delay time, the writing time, the frame frequency (60 Hz), and the gate line number, respectively. When

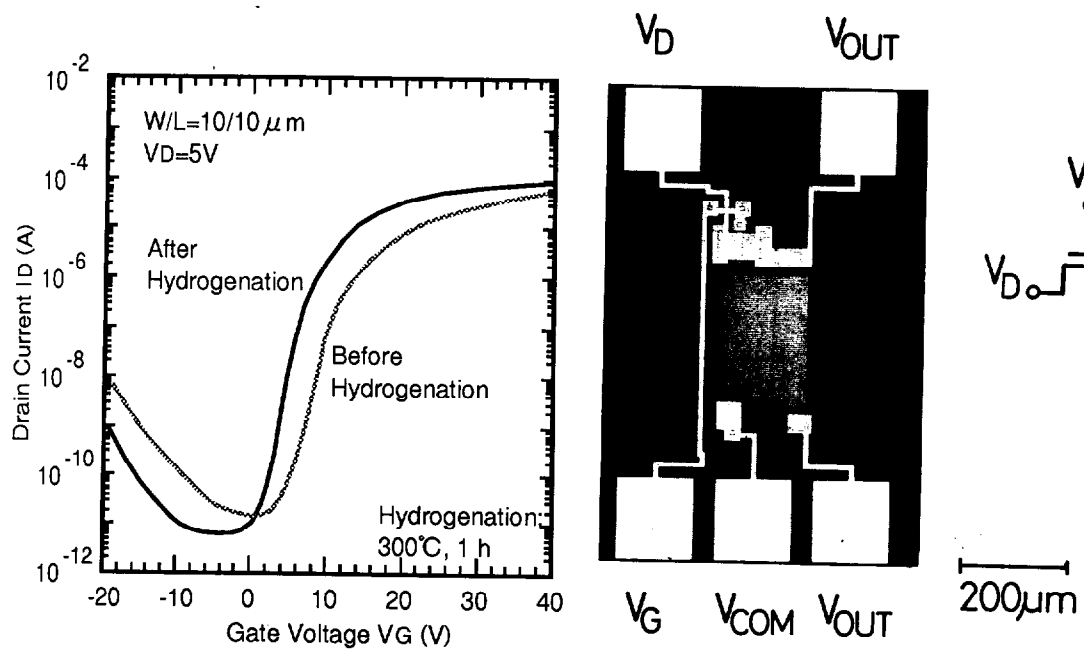


Fig. 2.56 Drain current-gate voltage characteristics of poly-Si TFT before and after hydrogenation.

Fig. 2.57 Discrete TFT with storage capacitor.

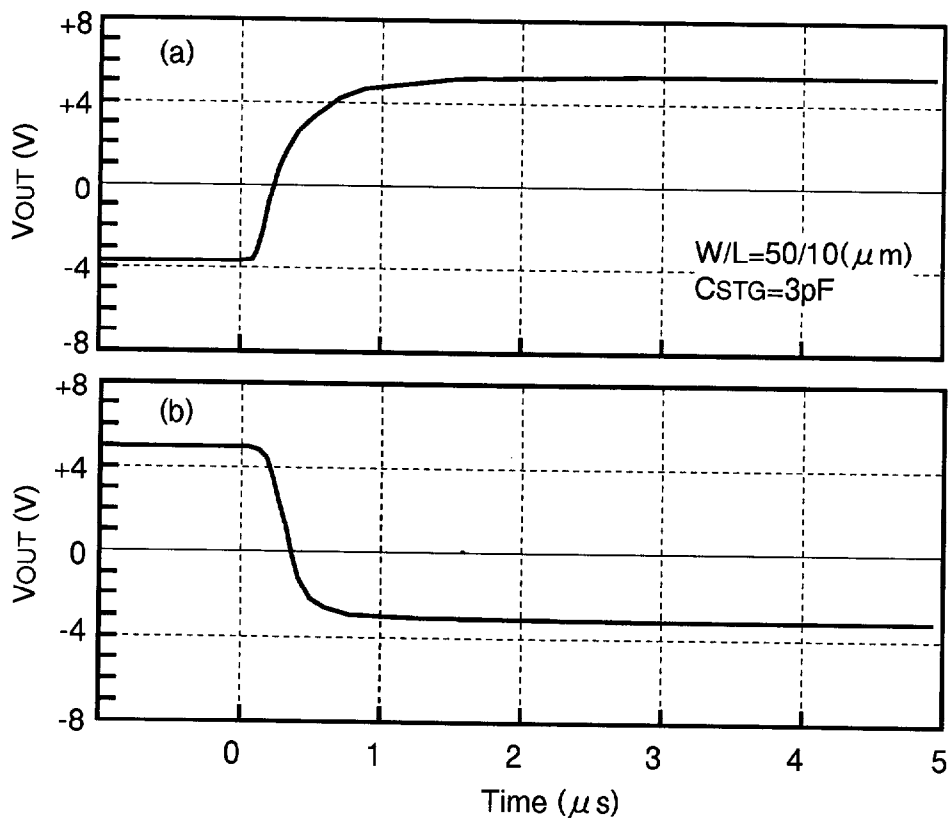


Fig. 2.58 Driving waveforms for storage capacitor by poly-Si TFT.
(a) $V_G = -4V$ to $16V$, (b) $V_G = 10V$ to $-4V$.

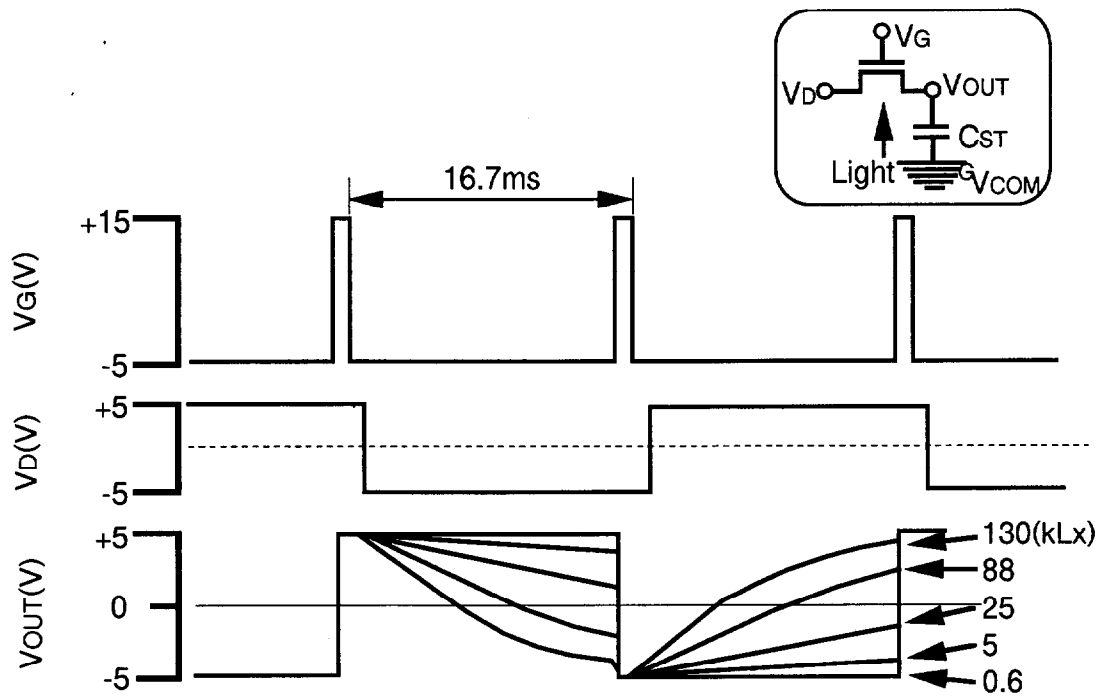


Fig. 2.59 Hold characteristics of TFT with storage capacitor under illumination.
 $W/L=10/10$, $C_{STG}=2.8\text{pF}$.

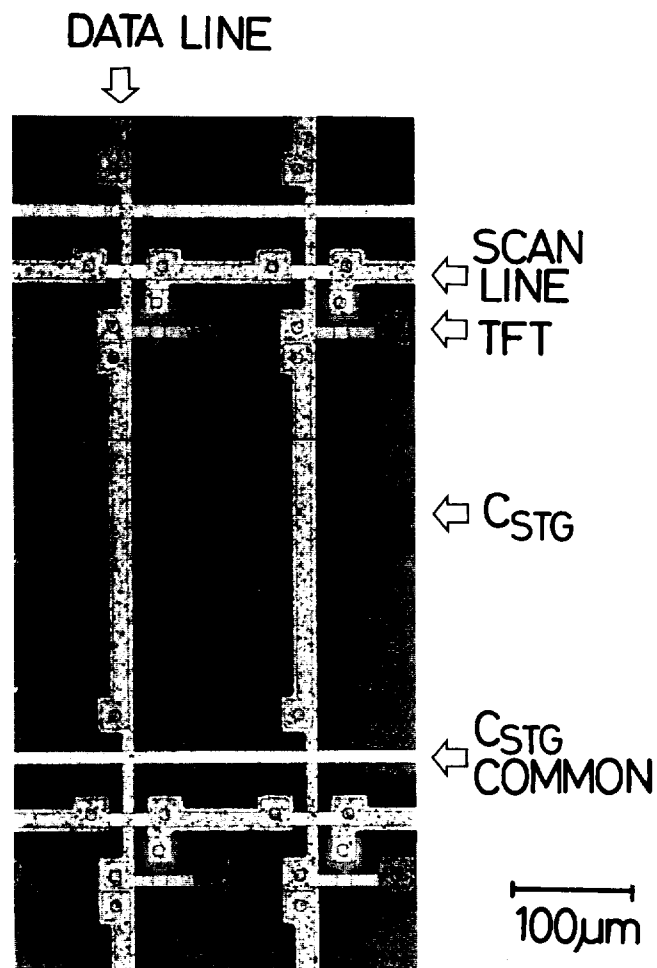


Fig. 2.60 Pixel with storage capacitor applied to 3.3" poly-Si TFT-LCD with monolithically integrated peripheral circuits for grey scale presentation.

T_{IN} is estimated to be 2 μ s, as shown in Fig. 2.58, and N is 1000 assuming high resolution LCD, T_A becomes 16.7 μ s. Therefore,

$$T_D \leq T_A - T_{IN} = 14.7 \mu s. \text{ -----(2-10)}$$

This relationship will be realized when self-aligned small-size poly-Si TFTs and conventional low resistive Al or Cu alloy are used for the pixel TFTs and the gate line, as predicted for large and high resolution LCDs [60].

(2) Hold characteristics

Fig. 2.59 shows the hold characteristics of the discrete TFT with $W=10 \mu m$, $L=10 \mu m$ and $C_{STG}=2.8 pF$ ($C_{STG}/C_{LC}=6$). This TFT has the same structure as that shown in Fig. 2.57. To inspect the effect of illumination on the holding characteristics, the back of the bare channel region was illuminated by a halogen lamp. Drain voltages of +5 V and -5 V were applied alternately to the capacitor for each frame period. The output voltage decreased when the back light strength increased because the TFT leakage current increased as shown in Fig. 2.37. However, a sufficiently large V_{OUT} was maintained at an illumination of 5000 lx. In actual LCD panel as in Fig. 1.7, the back light is absorbed by a polarizer, liquid crystal layer and alignment layer, and so the hold characteristics are much better. From this result, it was assumed that the storage capacitor had an ability to compensate for the TFT leakage current. As advanced technologies to reduce base leakage current in TFTs, dual-gate [3], off-set gate [54], and lightly doped drain LDD [61] structures are more practical.

Fig. 2.60 shows a pixel that is used in the 3.3" poly-Si TFT LCD with monolithically integrated peripheral circuits and 132(x3)x133 dots. The picture cell size was $150 \mu m \times 450 \mu m$. With this storage capacitor, grey scale representation with 64 colors was successfully achieved [59].

The low-temperature poly-Si TFT has the ability to drive large storage capacitors. Therefore, the poly-Si TFT should realize not only peripheral circuit integration, but also allow the addition of a storage capacitor to compensate leakage currents in TFTs and LCs, and to reduce the residual DC voltage component, resulting in the production of high-quality images in large-area high resolution LCDs.

2.3.5 Summary

The storage capacitor fabrication process was studied for low-temperature poly-Si TFTs, and compatibility with a hydrogenation treatment was focused upon. Bare ITO was reduced to indium metal by pure hydrogen plasma. The ITO buried under APCVD SiO_2 was protected from reduction. The transparent storage capacitor, ITO- SiO_2 -ITO (buried) structure was successfully fabricated. The poly-Si TFT with $W=50 \mu m$ and $L=10 \mu m$ drove 3 pF storage capacitance in 2 μ s. The TFT

with a storage capacitor showed sufficiently good holding characteristics under illumination to make grey scale representation possible. The low-temperature poly-Si TFT should have the ability not only to integrate peripheral driver circuits, but also to drive large storage capacitors to realize high-quality large-area TFT-LCDs.

2.4 Poly-Si TFTs with two-layer gate oxide with photo-CVD and APCVD

2.4.1 Approach to lower CVD temperature

The maximum process temperature must be below 600°C when hard glass substrates are used. Under this limitation, high-quality oxide and active layer poly-Si are indispensable components to realizing high-performance low-temperature poly-Si TFTs as studied in section 2.2. Generally, thermally annealed LPCVD poly-Si and APCVD SiO₂ have been used [10], [62]. Poly-Si and gate SiO₂ are discontinuously deposited in individual reactors. The poly-Si film is patterned into islands by photolithography and dry etching. In this case, the interface of gate SiO₂-poly-Si is on the initial poly-Si surface. On the other hand, it is inside the initial surface in the thermal oxidation method used in IC fabrication. Therefore, in the TFT process, special treatment or cleaning of the poly-Si surface before gate SiO₂ deposition is very important for keeping a clean interface and realizing low threshold voltage and high field-effect mobility.

Photochemical-assisted vapor deposition (photo-CVD) is advantageous for deposition of SiO₂ at very low temperatures below 300 °C [63], [64]. A photochemical reaction using UV light and ozone is very effective for poly-Si surface cleaning when strong oxidation ability is desired. The photo-CVD SiO₂ has been tentatively applied to the gate SiO₂ in the high temperature bulk-silicon MOSFET [64].

In this section, the photo-CVD was adopted for interface cleaning and surface protection of poly-Si in addition to the deposition of SiO₂ for low-temperature TFTs.

Table 2.7 summarizes preparation methods of various SiO₂ films. Photo-CVD is expected to be a favorable very low temperature CVD technology though its deposition rate is moderate.

2.4.2 Fabrication and characteristics of photo-CVD SiO₂

(1) Preparation of photo-CVD SiO₂

Fig. 2.61 is a schematic of the photo-CVD apparatus. The silicon source was TEOS (tetra-ethoxy-silane: Si(OC₂H₅)₄). TEOS and sensitizer were evaporated by carrier gases of N₂ (500 sccm) and O₂ (200 sccm), respectively, and the source gases were introduced into the reactor. The reactor was equipped with a heater, fused quartz window and low-pressure mercury lamp. The heater temperature was 300°C and wave lengths and emission power of UV lamp were 185nm, 254 nm and 80

Table 2.7 Preparation methods of various SiO₂ films

Method	Temperature	Conditions		Pressure	Deposition Rate
Photo-CVD	300 °C	TEOS/N ₂ O ₂ (carrier)	500sccm 200sccm	1064 Pa	4-5 nm/min
APCVD	480 °C	SiH ₄ /N ₂ O ₂ N ₂	16000 sccm 600 sccm 800 sccm	1 atm	50-60 nm/min
PECVD	320 °C	SiH ₄ /He N ₂ O He	40 sccm 50 sccm 50 sccm	27 Pa	25-30 nm/min
LT Oxidation	600 °C	wet O ₂	3000 sccm	1 atm	0.014 nm/min
HT Oxidation	1000 °C	Dry O ₂	3000 sccm	1 atm	0.1 nm/min

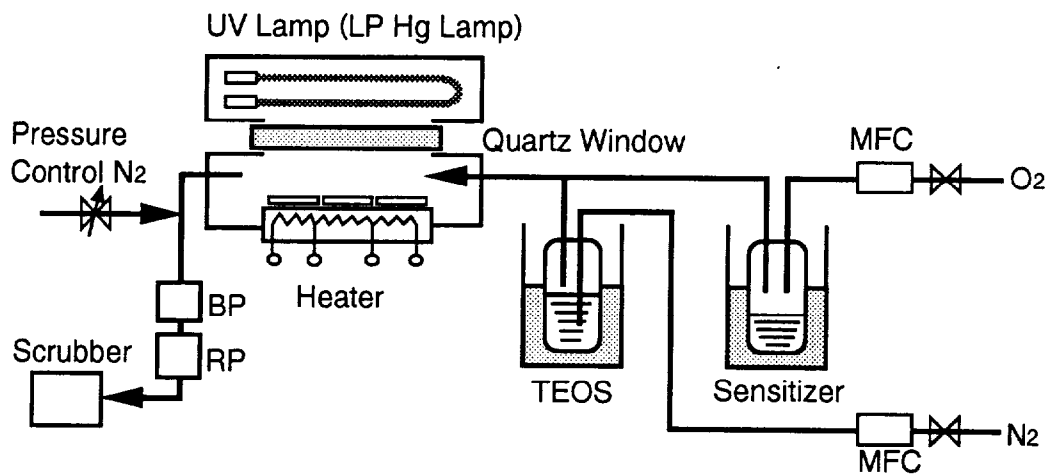


Fig. 2.61 Schematic of photo-CVD apparatus.

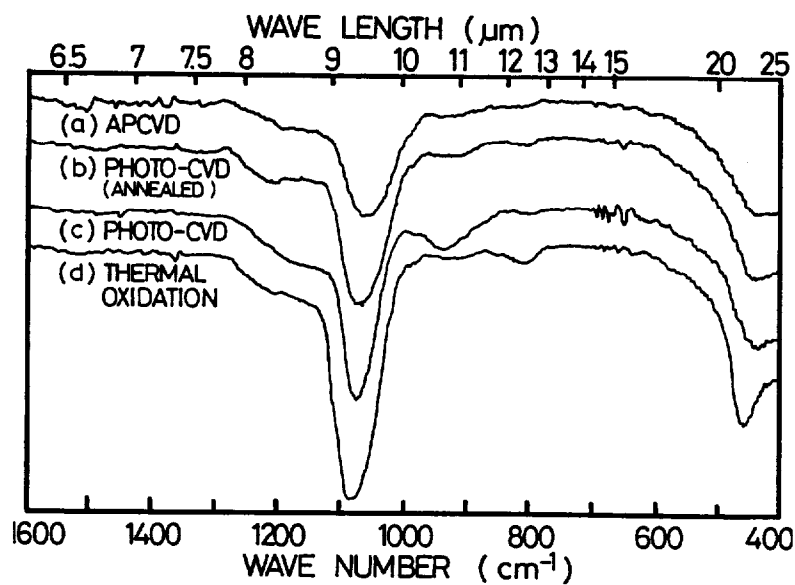
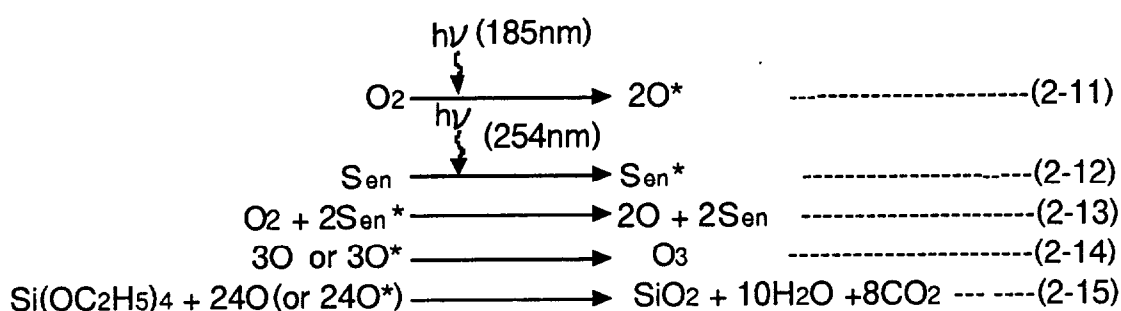


Fig. 2.62 Infrared absorption spectra of various SiO₂ films.

mW, respectively. Uniformity and deposition rate on 3" Si wafer were 5 % and 4-5 nm/min, respectively. When ozone cleaning was applied before film deposition, only O₂ was introduced and UV was irradiated at 1064 Pa for 5 min.

Hall and Peters [64] considered the reactions in photo-CVD for the SiH₄ + N₂O system. There are two basic reaction mechanisms: photolysis via sensitizer and direct photolysis. In the sensitizing reaction, sensitizer absorbs UV radiation and transfers energy to the reactant gases catalytically. In direct photolysis, UV radiation with high enough energy splits reactant gases directly and the reaction proceeds through collisional relaxation of excited atoms.

From these considerations, the following basic reactions were expected in this experiment for TEOS and O₂ system:



where S_{en} stands for catalyzer. The atomic oxygen in an excited state O* is produced by direct photolysis as equation (2-11). Atomic oxygen in the ground state O is generated by sensitizing reaction equations (2-12) and (2-13). Ozone is generated by equation (2-14). These reactions promote the deposition of SiO₂ in equation (2-15) at lower temperature.

(2) Characterization of photo-CVD SiO₂

Fig. 2.62 shows the infrared absorption spectra of various SiO₂ films. APCVD SiO₂ and thermal SiO₂ are presented for comparison with typical examples of CVD SiO₂ and standard SiO₂, respectively. The photo-CVD SiO₂ had the same structure as these films because absorptions of the Si-O bond stretching mode were observed at 9.6 and 12.6 μm. The peak position of Si-O near the 9.6 μm peak of photo-CVD SiO₂ film was shifted to the long wavelength region compared to that of thermal SiO₂. The shift of photo-CVD SiO₂ was smaller than that of APCVD SiO₂. The absorption at 10.7 μm corresponded to Si-OH bonding in as-deposited photo-CVD SiO₂. The Si-OH bonding was thought to be formed using H₂O released in the decomposition of TEOS. But this absorption disappeared after annealing at 580°C for 1 h in N₂.

Fig. 2.63 plots the dependence of etching rate of SiO₂ on annealing temperature. The etching rate was significantly reduced by heat treatment showing that the films were densified.

Fig. 2.64 shows the dependence of leakage current of MOS diodes on annealing temperature. The leakage current was also reduced noticeably

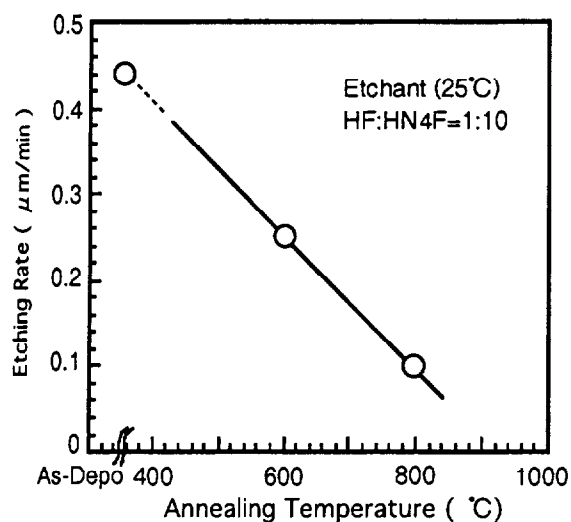


Fig. 2.63 Dependence of etching rate on annealing temperature.

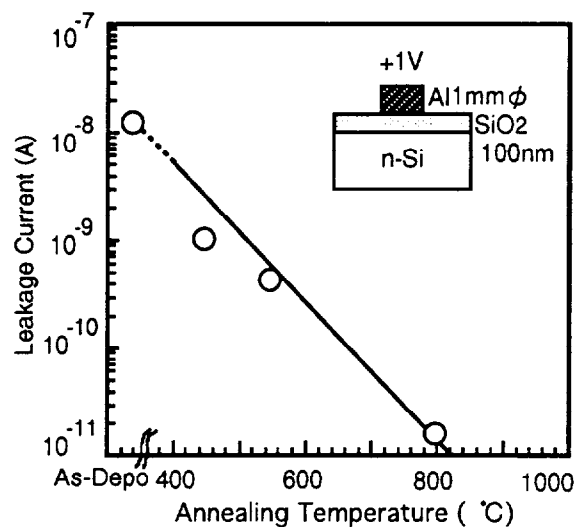


Fig. 2.64 Dependence of leakage current on annealing temperature.

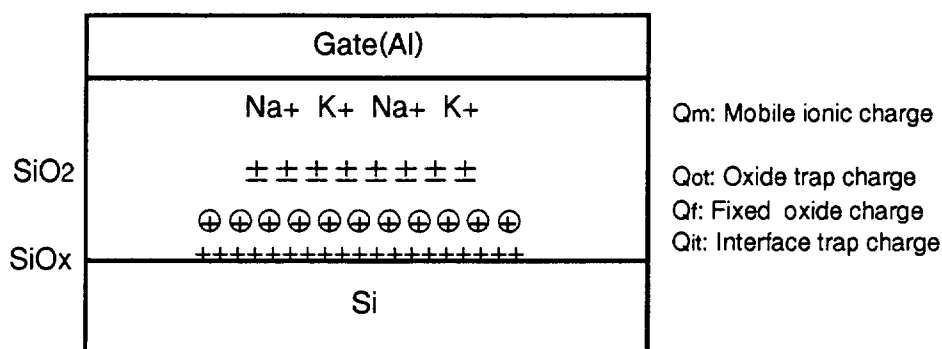


Fig. 2.65 Various charges in SiO₂ and interface.

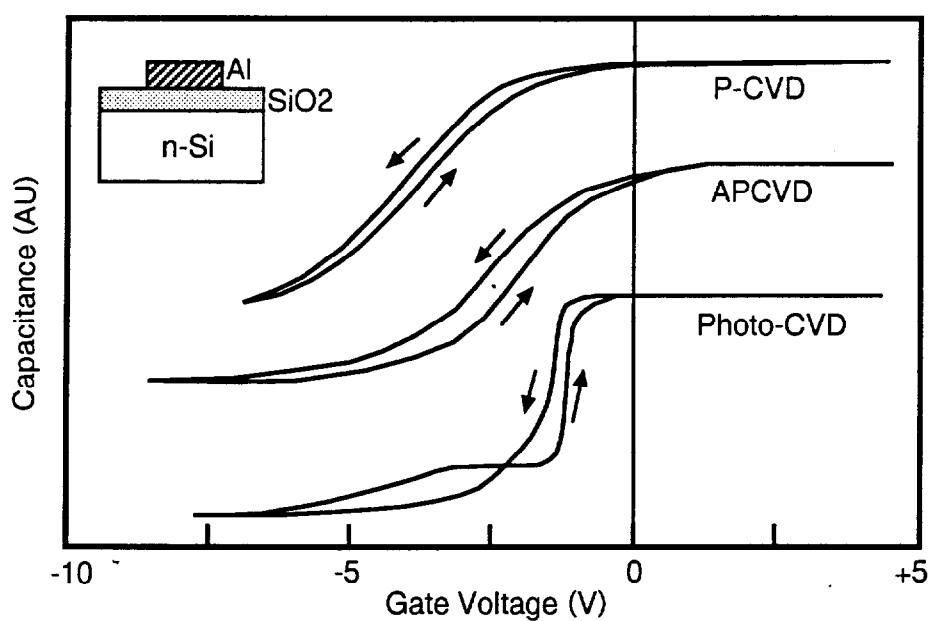


Fig. 2.66 Voltage-capacitance characteristics of CVD SiO₂.

by annealing at a higher temperature than that of deposition. From these results of chemical and electric characterizations, it was indicated that as-deposited photo-SiO₂ was coarse and leaky. Though these characteristics were improved by densification in post-thermal annealing which was applied in the TFT fabrication process, no further attempts were made to use single-layer photo-CVD SiO₂.

Fig. 2.65 illustrates four kinds of charges, Q_{it} , Q_m , Q_{ot} , and Q_f in the SiO₂-Si system [65]. Q_{it} is interface trap charge which originates from irregularity of the Si crystal lattice at the interface. Q_m , Q_{ot} , and Q_f are mobile ion charge such as Na⁺ and K⁺, oxide trap charge generated by irradiation, and fixed charge caused by excess Si or oxygen vacancies, respectively. Interface characteristics are affected by these charges, which are evaluated by C-V measurements.

Fig. 2.66 shows the C-V characteristics of PE-CVD, APCVD and photo-CVD SiO₂ films. All of the as-deposited SiO₂ films had hysteresis in their C-V curves. But it was clear that the photo-CVD film had the smallest threshold voltage among the three.

Table 2.8 summarizes the surface charge density (flat band concentration) N_{FB} of the single layer and two-layer SiO₂. N_{FB} reflects the above four kinds of charges and is an indicator of surface cleanness. It is calculated from the next equation assuming that charges are near the interface,

$$N_{FB} = (C_{OX} \cdot V_{FB}) / (q \cdot S) \text{ -----(2-16)}$$

where C_{OX} , V_{FB} , q , and S are capacitance of oxide, flat band voltage, electron charge, and electrode area, respectively. The photo-CVD SiO₂ film had a lower value than APCVD SiO₂ film. From this result and considering the moderate deposition rate, photo-CVD SiO₂ was used for SiO₂-poly-Si interface cleaning and protection layer, and the overlaid APCVD SiO₂ was used as the main component of the gate insulator. The two-layer oxide of photo-CVD SiO₂ and APCVD SiO₂ had the same surface charge density as the single-layer photo-CVD SiO₂. The two-layer oxide of thermal SiO₂ and APCVD SiO₂ also had the same value as that of photo-CVD SiO₂. But, in this experiment, this structure was not applied for TFT fabrication because the thermal oxidation step was very slow (0.014nm/min on single Si). Therefore, the two-layer structure of photo-CVD SiO₂ and APCVD SiO₂ was applied to TFT fabrication.

2.4.3 TFT fabrication process

Fig. 2.67 shows a cross-sectional view of the poly-Si TFT. Under-layer SiO₂ (400 nm thick) was deposited at 480°C by APCVD on a 3" diameter quartz substrate. Poly-Si (150 nm) was deposited at 580°C and 0.8 mbar to give the active layer which was annealed at 580°C for 18 h in N₂ for crystallization (in this experiment, the optimized conditions for poly-Si in section 2.2 were not yet applied). The poly-Si was patterned

Table 2.8 Surface charge density of single-layer and two-layer gate oxides

Oxide	Thickness	Temperature	Surface Charge Density(cm^{-2})
(1) Photo-CVD	100 nm	300 °C	9×10^{10}
(2) APCVD	100 nm	300 °C	5×10^{11}
(3) Photo-CVD/ APCVD	10 nm 100 nm	300 °C 300 °C	8×10^{10}
(4) Thermal Oxide/ APCVD	350 nm 100 nm	600 °C 480 °C	9×10^{10}

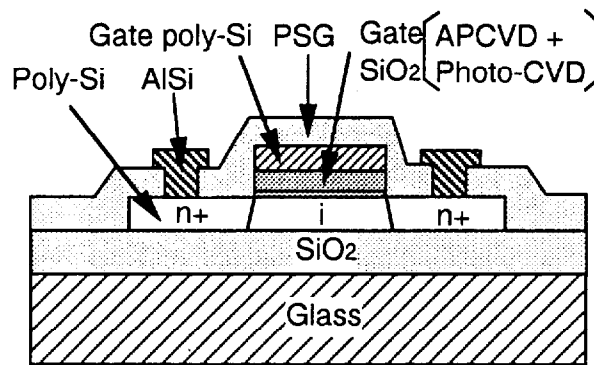


Fig.2.67 Cross-sectional structure of TFT with two-layer gate insulator.

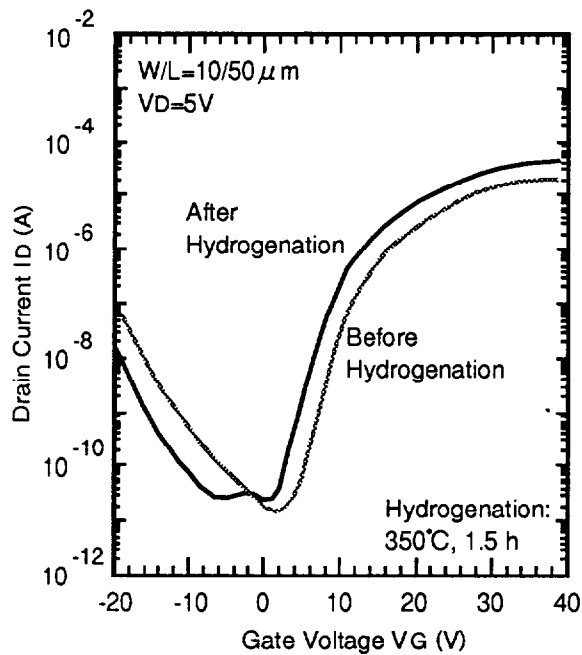


Fig. 2.68 Drain current-gate voltage characteristics of poly-Si TFT with photo-CVD gate SiO₂ before and after hydrogenation.

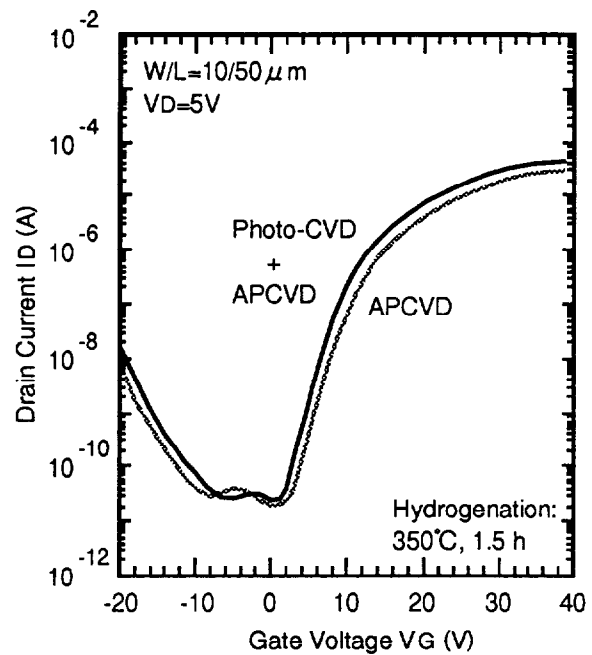


Fig. 2.69 Drain current-gate voltage characteristics of poly-Si TFT with single- and two-layer gate SiO₂.

into islands. Gate oxide was deposited by photo-CVD (10 nm) and APCVD (100 nm). Photo-CVD was carried out at 300°C by a conventional method [64] using the apparatus shown in Fig. 2.61. TEOS and O₂ were used for silicon and oxygen sources. Deposition rate was 4-5 nm/min. In the first stage of the photo-CVD process, the poly-Si surface was treated using UV light and O₂ for 5 min for the purpose of surface cleaning by ozone. During this period, about a 1 nm SiO₂ layer was grown. APCVD SiO₂ was deposited by the reaction of SiH₄ and O₂ in N₂ carrier gas at 480°C. Deposition rate was 50-60 nm/min.

Gate poly-Si (350 nm) was deposited by LPCVD. After gate patterning, phosphorous ions were implanted at a dose of $5 \times 10^{15}/\text{cm}^2$ and 70 kV to form the source and drain. After deposition of PSG, thermal annealing was carried out for 20 h at 600°C to activate implanted ions. After metallization by sputtered AlSi (2 % Si), the substrate was annealed at 400°C in forming gas for 30 min. Finally, hydrogenation was carried out in a plasma reactor at 300°C for 90 min.

2.4.4 TFT characteristics

Fig. 2.68 shows the V_G - I_D characteristics of two-layer gate oxide TFT before and after hydrogenation. The on-characteristics were improved by hydrogenation and the same generation current component in the off-region was observed as in the conventional TFTs (Fig. 2.25). Fig. 2.69 shows the V_G - I_D curves of TFTs with two-layer SiO₂ and single-layer APCVD SiO₂. The former showed better performance.

Fig. 2.70 plots the dependence of field-effect mobility on hydrogenation temperature. The field-effect mobility of TFT with two-layer gate oxide was increased 9 % by hydrogenation, though the value of the conventional TFT was not improved.

Fig. 2.71 plots threshold-voltage dependence on hydrogenation temperature. Threshold voltage was reduced by hydrogenation. The reduction ratios of the two-layer gate oxide TFT and conventional single-layer gate oxide TFT were 23 and 10 %, respectively. It is important to note that hydrogenation was more effective for the TFT with the two-layer gate oxide than for the conventional TFT.

Table 2.9 summarizes the fundamental characteristics of the developed TFT and conventional one-layer oxide TFTs. All values of μ_{FE} , V_{TH} , and on/off current ratio were improved.

Fig. 2.72 plots the operation characteristics of ring oscillators. An E-E type 21-step ring oscillator operated with a delay time of 240 ns/stage at V_{DD} of 32 V, which is about ten times faster than for the conventional TFT circuit. The TFT was as stable as the conventional TFTs in the continuous stress test ($V_G=20$ V, $V_D=5$ V, 25°C, 8 h).

The performance of the low-temperature poly-Si was improved and these results should also be realized for glass substrates.

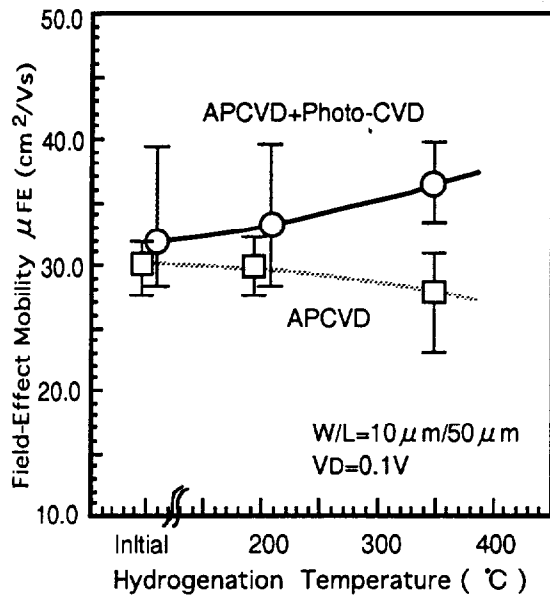


Fig. 2.70 Dependence of field-effect mobility on hydrogenation temperature.

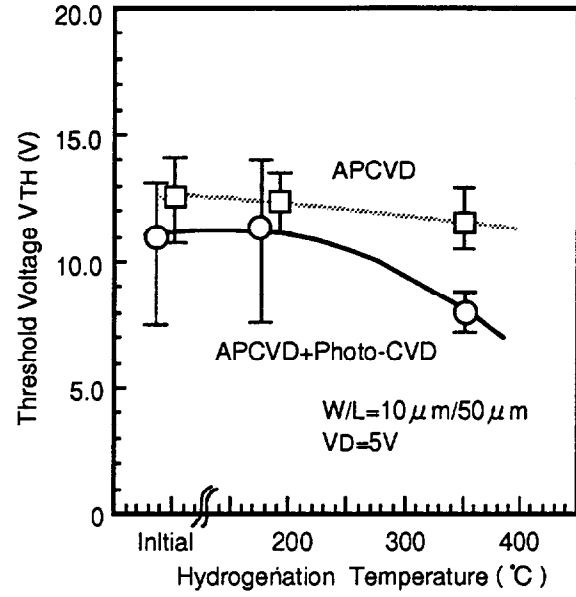


Fig. 2.71 Dependence of threshold voltage on hydrogenation temperature.

Table 2.9 Summary of fundamental characteristics of poly-Si TFTs

Gate Oxide	Photo-CVD + APCVD	APCVD
Field-Effect Mobility (cm²/Vs)	35	28
Threshold Voltage (V)	8.3	11.3
On-Off Current Ratio (Log(I _{ON} /I _{OFF}))	5.6	5.4

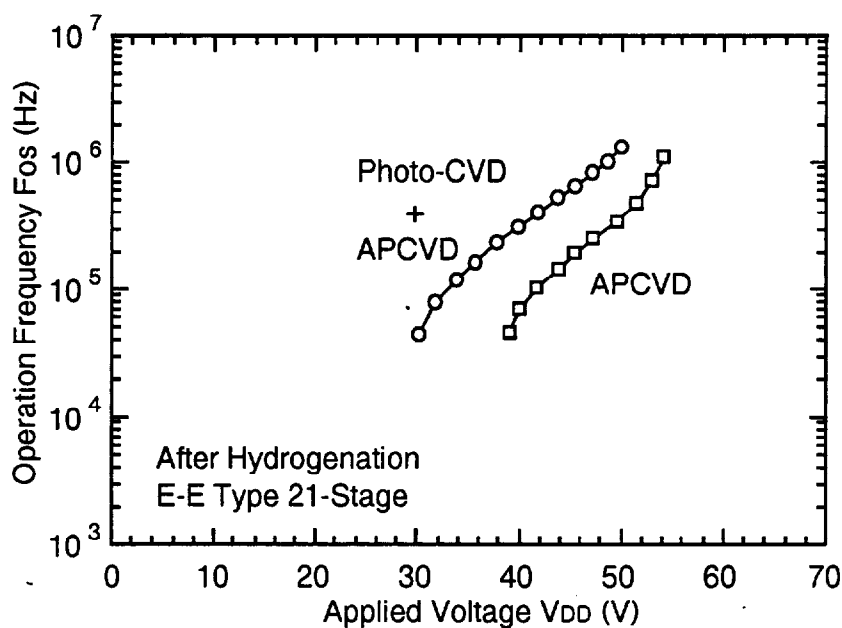


Fig. 2.72 Operation characteristics of ring oscillators.

2.4.5 Summary

Use of photo-CVD SiO_2 was studied for the gate insulator of low-temperature poly-Si TFTs fabricated by a 600°C process. As-deposited photo-CVD SiO_2 was coarse and unstable in the TFT fabrication process. Photo-CVD SiO_2 was used to ensure a clean interface of the SiO_2 -poly-Si. A two-layer gate oxide with photo-CVD SiO_2 (10 nm) and APCVD SiO_2 (100 nm) was applied to the poly-Si TFTs. Hydrogenation by H_2 plasma was more effective for the new TFT than the conventional TFT with single-layer oxide of APCVD SiO_2 regarding improved characteristics. The developed TFT had a V_{TH} of 8.3 V and μ_{FE} of $35 \text{ cm}^2/\text{V}\cdot\text{s}$ which were lower and higher than the respective values of the conventional TFT. The ring oscillator with new TFTs also operated faster than the conventionally TFT-equipped oscillator. Thus, the possibility of reduction of gate insulator SiO_2 deposition temperature and improved TFT characteristics were confirmed.

2.5 Poly-Si TFTs with SiO_2 gate insulator thermally oxidized at 600°C

2.5.1 Expectations for native oxide to improve TFT performances

To realize a low temperature process below 600°C for glass substrates, CVD technologies were used for the preparation of semiconductor Si film and insulator SiO_2 . High quality poly-Si films and gate insulator are indispensable for realizing high performance poly-Si TFTs. In section 2.2, LPCVD Si films were studied for active layer poly-Si to improve TFT characteristics. Gate insulator and passivation films were prepared by APCVD, PECVD, and photo-CVD as discussed before. Thus, poly-Si and gate SiO_2 are discontinuously deposited by CVD in individual reactors.

In this case, the gate SiO_2 -poly-Si interface is on the initial poly-Si surface. Therefore, there is a possibility for contaminants to be incorporated into the interface which degrade the TFT performance. But thermal oxidation forms the interface in the initial poly-Si film. Therefore, it should be ideal to apply native oxide of poly-Si to gate oxide as bulk Si LSI devices.

There have been a few trials on application of thermally oxidized SiO_2 for the gate insulator of poly-Si TFTs [12] and a-Si TFTs [66], [67], but precise relationships between characteristics of oxide and poly-Si TFTs were not reported. In section 2.4, it was confirmed that the photo-CVD method was useful to realize a clean interface and to improve TFT characteristics. It was also found that SiO_2 thermally oxidized at 600°C

realized clean interface, resulting in low N_{FB} (Table 2.8). In this section, application of thermal oxide to TFT gate insulator was studied.

2.5.2 Preparation and evaluation of thermally oxidized SiO_2 films

Fig. 2.73 illustrates the apparatus for thermal oxidation. Pure water was heated in the evaporator at 95 to 100°C and vapor was introduced into the closed quartz tube which was heated at 600°C in the furnace. Carrier O_2 flow was 30 to 50 sccm. APCVD SiO_2 was deposited at 480°C as reference film. Gas flow rates of SiH_4 with N_2 dilution, O_2 , and carrier N_2 were 800, 600, and 1600 sccm/min, respectively (Table 2.7). APCVD SiO_2 was annealed at 600°C for 20 h which was equivalent treatment to the activation of implanted ions to make the source and drain.

Thickness of oxide on Si (100) or poly-Si was measured by ellipsometry. Infrared absorption spectra were measured by depositing oxide on Si wafers to a thickness of 1 μm to avoid interference. Etching rate was measured by etching the oxide in diluted HF aqueous solution ($\text{HF}:\text{H}_2\text{O}=1:99$) at room temperature. Surfaces of Si films were observed by SEM. Cross sections of the interface of oxide and poly-Si were observed by TEM. Capacitance-voltage characteristics were measured using an MIS diode with an aluminum electrode of 1 mm diameter.

Fig. 2.74 shows the oxide layer structures used for evaluations. Thermal oxidized films were formed on LPCVD-Si with underlayer SiO_2 ((a)), LPCVD-Si ((b)), and crystal Si (100) ((c)).

2.5.3 Characteristics of thermally oxidized SiO_2 films

(1) Thermal oxidation kinetics

Oxidation kinetics was proposed by Deal and Grove [68]. Oxidation phenomenon consisted of three steps: (1) transportation of oxidizing species to the surface of oxide; (2) diffusion of oxidizing species in the present oxide; and (3) oxidation reaction at the Si surface. The general relation of oxide thickness X and oxidation time t in wet thermal oxidation is shown as

$$X^2 + AX = B \cdot t \quad \text{-----}(2-17)$$

where A and B are constants. For short oxidation times and low-temperature reaction, i.e., X is small, a linear law is obtained.

$$X = (B/A)t \quad \text{-----}(2-18)$$

For long oxidation times and high temperature reaction, i.e., X is large, a parabolic relationship is described.

$$X^2 = B \cdot t \quad \text{-----}(2-19)$$

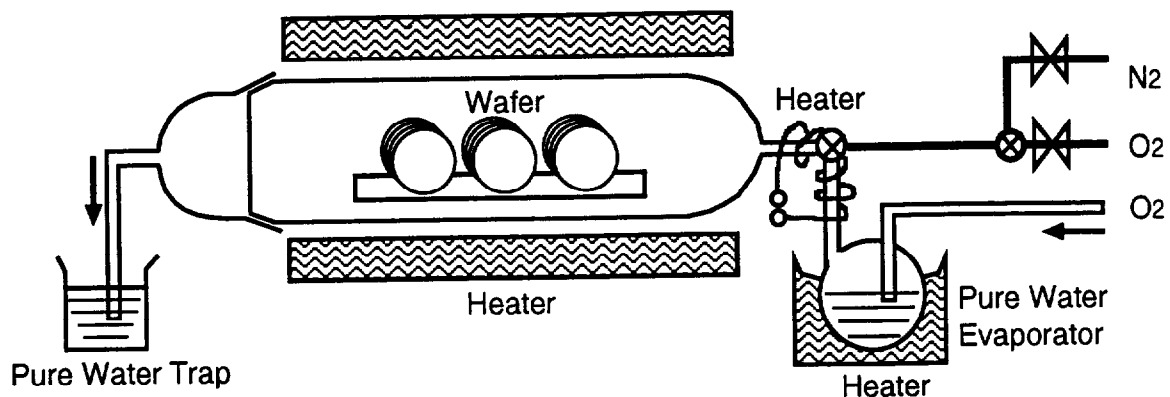


Fig. 2.73 Apparatus for wet thermal oxidation.

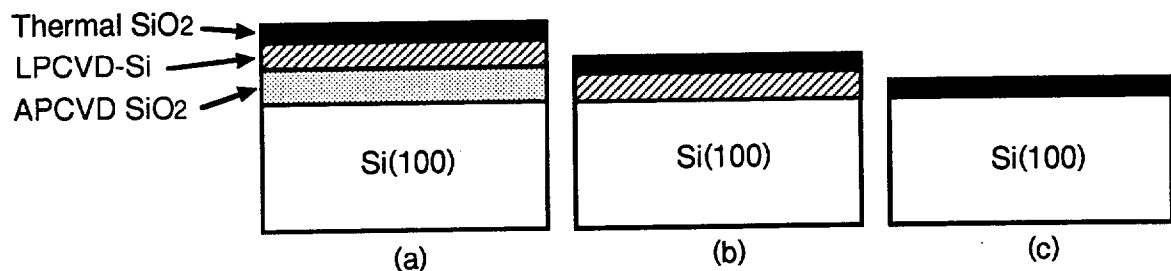


Fig. 2.74 Structures of wafers for evaluation of thermal oxide.

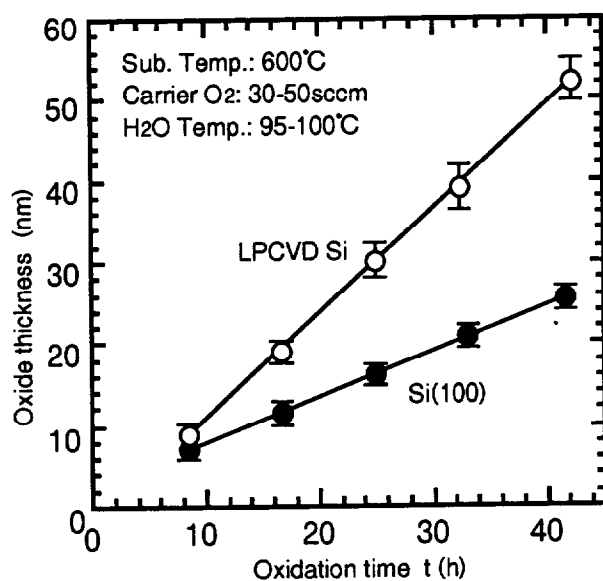


Fig. 2.75 Dependence of oxide thickness on oxidation time.

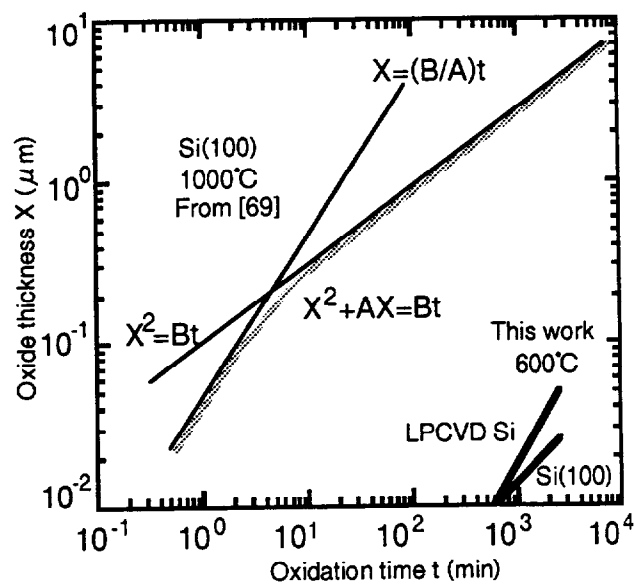


Fig. 2.76 General relations of oxide thickness and oxidation time in wet thermal oxidation.

Fig. 2.75 plots oxide thickness dependence on oxidation time. Thicknesses of oxide films both on LPCVD poly-Si and Si(100) were proportional to the oxidation time. Oxidation rate of LPCVD poly-Si was about two times higher than that of single Si (100).

Fig. 2.76 shows the general relations of oxide thickness and oxidation time in wet thermal oxidation. Results of Fig. 2.75 were replotted and the results of the oxidation of single crystal Si at 1000°C were also included from reference [69]. The slope of the curve for LPCVD-Si was almost 1 corresponding to the relation (2-18) and this showed that the oxidation phenomenon at 600°C was in accordance with a linear law. Generally, in equation (2-18), the constant B does not depend on crystal orientation, though surface (111) has a lower A value than surface (100). The LPCVD-Si film indicated a higher oxidation rate than single Si (100) because poly-Si grains were oriented and had (111) surface and many lattice defects as discussed in section 2.2.

(2) Chemical characteristics of SiO₂

Fig. 2.77 plots the relation of IR absorption and oxide thickness. Absorption was calculated from the largest absorption peak at 1080 cm⁻¹ which corresponded to the absorption of asymmetric stretching vibration of Si-O bond. The absorption was proportional to the film thickness. The absorptions of thermal SiO₂ on poly-Si and single Si (100) were almost the same and higher than those of APCVD SiO₂. The absorption is an indicator of compactness or density of SiO₂ films. Therefore, it was suggested that thermal SiO₂ of poly-Si had the same density as that of single Si (100) and higher density than APCVD SiO₂. In addition to these results, there were no peaks corresponding to Si-H or Si-OH bonds in the absorption curves.

Fig. 2.78 plots the etching characteristics of oxide films. Etching thicknesses were proportional to etching times for all films. The values of SiO₂ of poly-Si and single Si (100) were almost the same and lower than that of APCVD SiO₂. These results indicated that thermal SiO₂ had high density as implied in Fig. 2.77.

From these results, it was suggested that the thermal SiO₂ of poly-Si fabricated at 600 °C had almost the same chemical characteristics as that of high temperature thermal SiO₂.

(3) Observation of interface of thermal SiO₂ and poly-Si

Fig. 2.79 shows SEM photographs (1.5 kV) of surfaces of Si(100) and poly-Si after removal of thermal SiO₂ by HF aqueous solution (HF:H₂O=1:99) in a 90 min etching. Surface of single Si (100) was smooth as shown in photograph (a). But roughness increased when the thickness of the thermal oxide of poly-Si increased as shown in photographs (b) and (c). This was thought to correspond to the poly-Si grain shapes. The roughness of poly-Si surface was increased when poly-

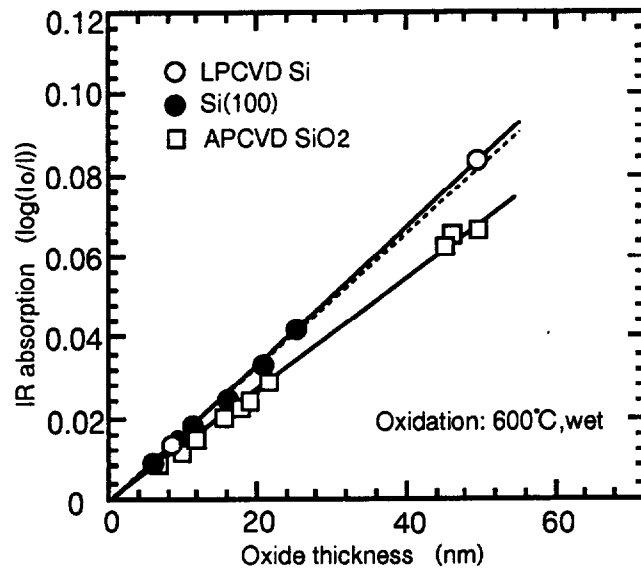


Fig. 2.77 Dependence of IR absorption on oxide thickness.

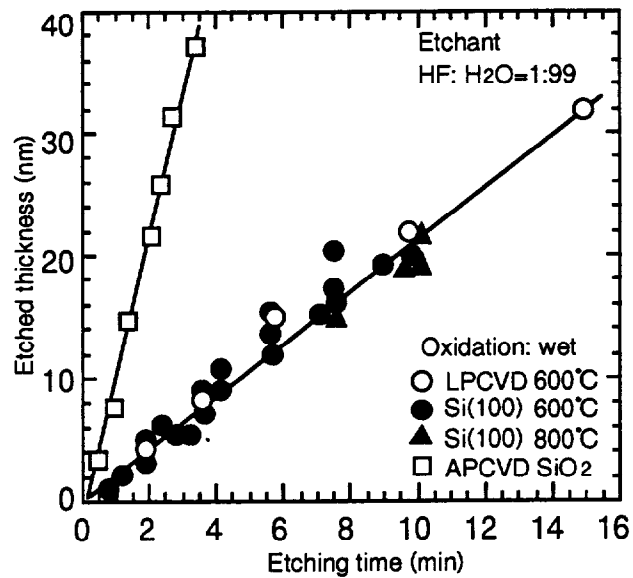


Fig. 2.78 Etched thickness dependence on etching time.

Si was deposited on underlayer APCVD SiO₂ as in (d). This suggested that the roughness of underlayer SiO₂ was reflected to that of poly-Si. These results implied that poly-Si was oxidized deeply along the grain boundaries.

Fig. 2.80 is a photograph of the cross section of oxidized poly-Si observed by TEM (200 kV). Surface was coated with a PtPd film that was 20 nm thick to get a clear observation. There were many grains and boundaries in poly-Si film. But the interface of poly-Si and SiO₂ was flat indicating that the oxidation progressed uniformly for all grains and grain boundaries. But considering the SEM observation results that roughness of the poly-Si surface increased by oxidation, the long time etching of SiO₂ by HF solution emphasized the grain boundaries.

(4) Electric characteristics of SiO₂

Thermal oxidation rate at 600 °C was too slow and the single layer gate insulator was not practical for TFT fabrication. In this experiment, two layer insulator with underlayer of thermal oxide and top layer of APCVD SiO₂ was evaluated. Single layer APCVD SiO₂ was used for a reference. Quasi-static C-V measurement method was introduced. Gate voltage was scanned constantly and gate current was measured. Fig. 2.81 shows the voltage-capacitance characteristics of MIS diodes with low-temperature oxides. MIS diode (b) with two-layer insulator showed minimum hysteresis and stable C-V characteristics. MIS diodes of (a) with APCVD SiO₂ and (c) with thick thermal oxide (30 nm) showed large hysteresis. Capacitance of MIS diode (c) in scanning to positive V_G was not saturated implying that injection of electrons into SiO₂ with a long time constant occurred. These results suggested that the two-layer structure with 10 nm thermal oxide and 90 nm APCVD SiO₂ was most stable.

Fig. 2.82 shows the total localized states density N_{TT} in SiO₂-poly-Si interface for single layer APCVD SiO₂ and two-layer oxides. N_{TT} is the total of trap density in poly-Si (N_T) and interface trap density (D_{it}). The surface charge density of thermal SiO₂ was one fifth of that of APCVD SiO₂ as shown in Table 2.8. But the values of N_{TT} at mid gap region of the two structures were almost the same and about 2×10¹⁸ eV·cm⁻³ which was ten times the value of a-Si. Considering these facts, it was suggested that trapping characteristics of the interface were almost completely determined by localized state density in poly-Si N_{TS} in the SPC poly-Si films.

Fig. 2.83 illustrates the gate voltage-leakage current characteristics of MIS diodes with various insulator structures. When the thickness of thermal SiO₂ increased, the breakdown voltage was noticeably decreased. These results corresponded with the fact that the surface roughness of poly-Si increased when the thickness of thermal oxide increased.

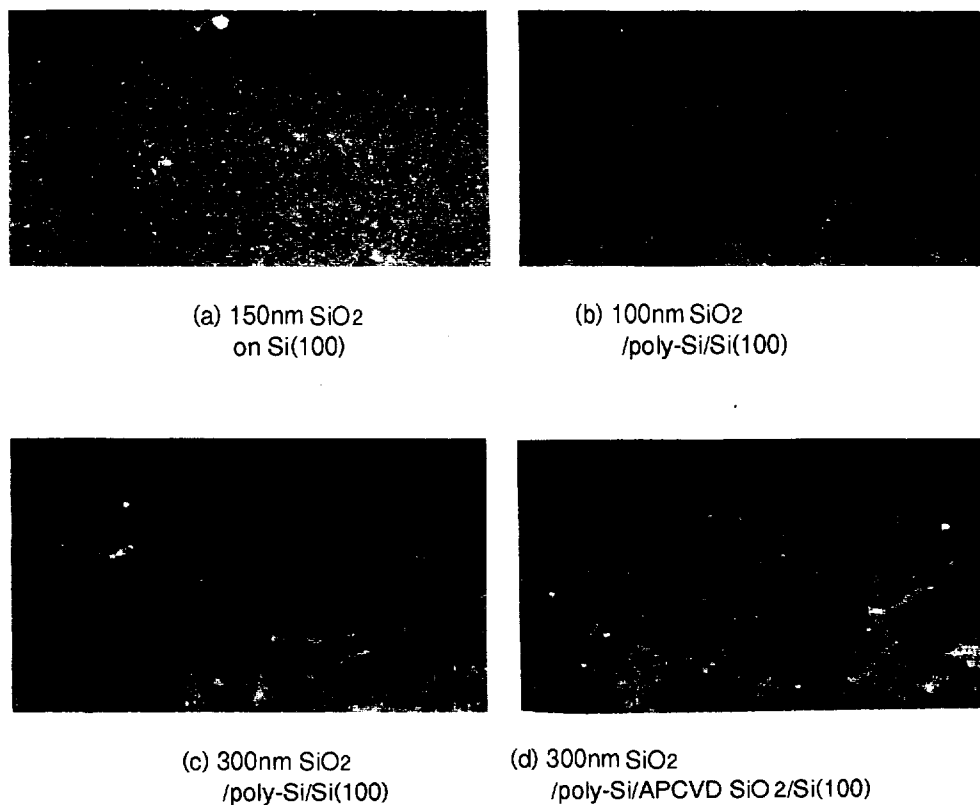
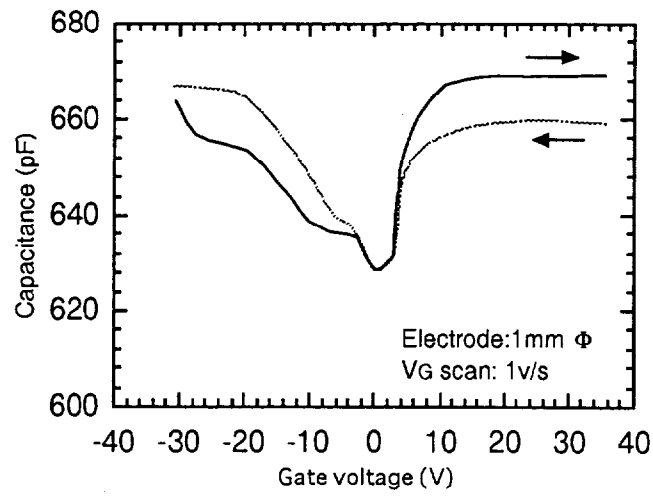


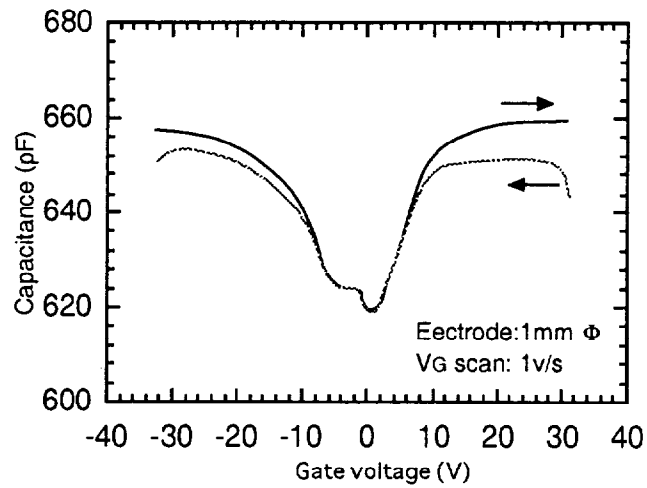
Fig. 2.79 SEM micrographs of oxide surfaces.



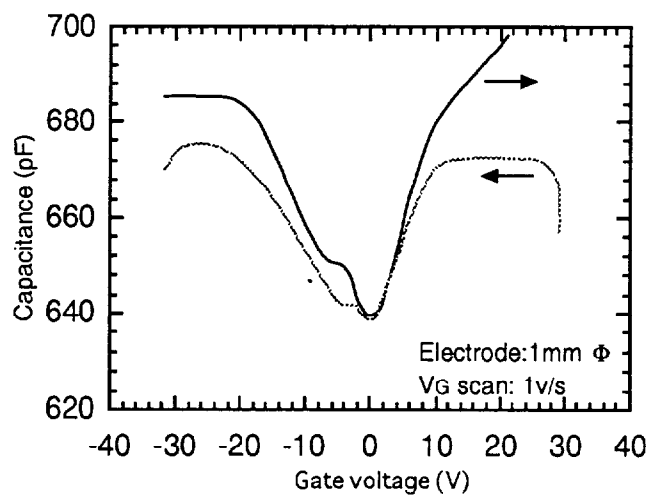
Fig. 2.80 TEM micrograph of cross section of SiO₂-poly-Si interface.



(a) APCVD SiO₂:100 nm



(b) APCVD SiO₂ 90nm + Thermal SiO₂ 10nm



(c) APCVD SiO₂ 70nm + Thermal SiO₂ 30nm

Fig. 2.81 Voltage-capacitance characteristics of low-temperature oxides.

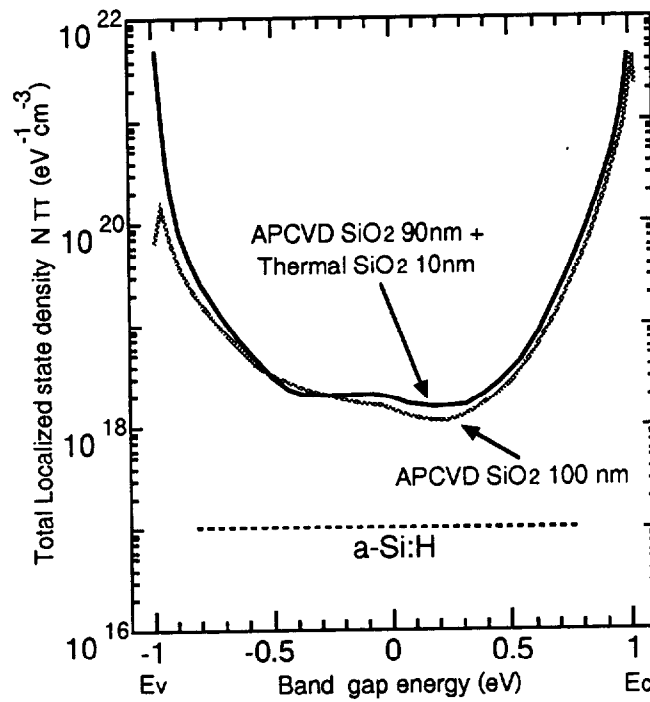
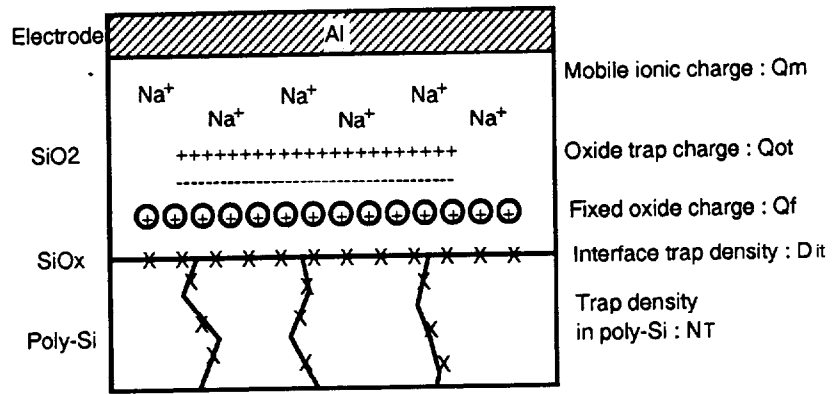


Fig. 2.82 Distribution of localized states in SiO₂-poly-Si interface.

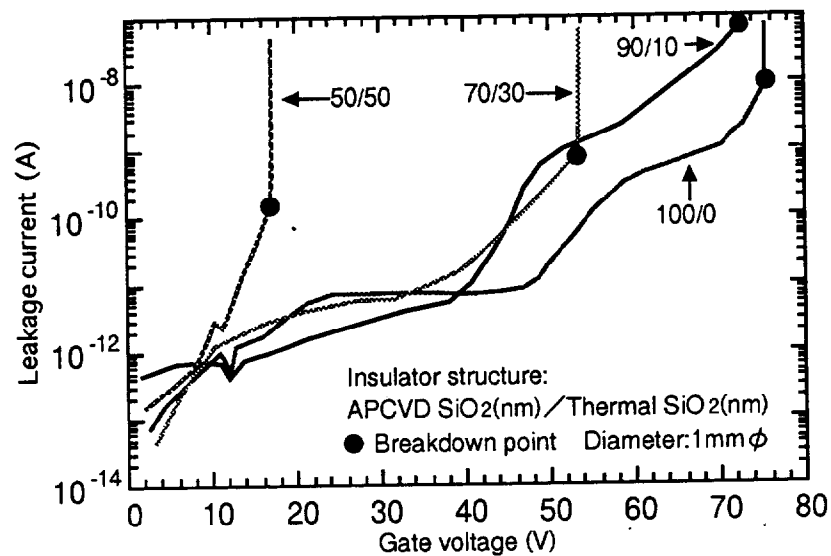


Fig. 2.83 Voltage-leakage current characteristics of MIS diodes.

2.5.4 TFT characteristics

Table 2.10 summarizes the TFT fabrication process. Fig. 2.84 shows the basic TFT structure and Fig. 2.85 illustrates the gate structures with various gate insulators. TFTs (b) and (c) had a thin thermal oxide for underlayer. TFT (d) had thermal oxide only on top of the poly-Si layer. Fig. 2.86 shows the basic characteristics of various TFTs. Mobility and threshold voltage were slightly improved for TFT (b) compared with conventional TFT (a) as expected from the results of C-V measurements described (Fig. 2.81). The performance of TFT (d) was not improved though contamination was avoided to eliminate photolithographic process before oxidation. In TFT (c) with an increased ratio of thermal oxide, the gate breakdown voltage decreased as measured by MIS diodes in Fig. 2.83. But TFT (d) also had low V_{GB} because the gate oxide was thin at the edge of the poly-Si island, though the ratio of thermal oxide was small.

2.5.5 Summary

Low temperature wet oxidation at 600°C for single crystal Si realized a lower number of localized states compared with APCVD SiO_2 . But thermal oxidation of poly-Si increased roughness of the poly-Si surface and decreased the insulator breakdown voltage. Two-layer gate insulator structure with APCVD SiO_2 (90 nm) and thin underlayer thermal oxide (10 nm) slightly improved TFT performance. From estimation of the localized state density at the interface, it was suggested that interface trapping characteristics were almost completely determined by localized state density N_{ts} in poly-Si in this SPC poly-Si film. So the process of fabrication of native oxide in poly-Si was not so effective to improve TFT performance when SPC poly-Si was used as the active layer. If the quality of poly-Si is improved further by laser crystallization, thermal oxidation will be useful to improve TFT performances.

2.6 Conclusions

The maximum TFT process temperature was set at 600°C considering the heat resistivity of mass-produced hard glass. To realize high-performance TFTs, optimization of SPC of active layer poly-Si and preparation of gate SiO_2 were studied. Crystal quality of poly-Si critically depended on the deposition temperature of LPCVD Si. Optimizing the deposition temperature Si film at about 550°C and using APCVD SiO_2 as gate oxide, TFT characteristics were drastically improved. Thin poly-Si gate TFT structure was developed for effective hydrogenation to improve TFT characteristics. High-performance n-channel TFTs were achieved to

Table 2.10 Summary of TFT fabrication process

Process	Conditions
Glass	Asahi AN
Underlayer SiO ₂	APCVD-SiO ₂ , 480 °C, 600 nm
Poly-Si	LPCVD-Si, 550 °C, 150 nm
Crystallization	600 °C, 20 h, in N ₂
Gate SiO ₂	(see Fig.2.85)
Ion Impl.	P ⁺ , 30 kV, 5x10 ¹⁵ /cm ²
Activation	600 °C, 20 h, in N ₂
Passivation	APCVD-PSG, 405 °C, 600 nm
Contact etching	wet and dry etching
Metallization	AlSi, 600 nm
Hydrogenation	300 °C, 300 W, 100 Pa, 60 min

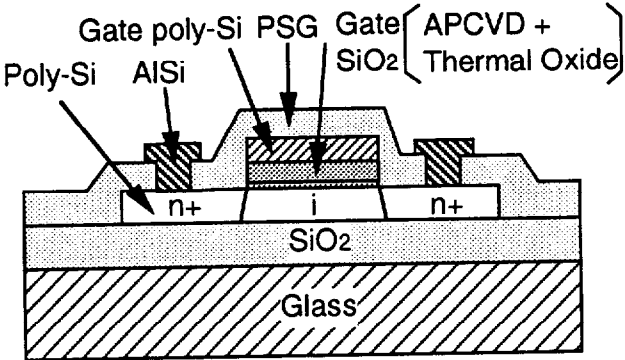


Fig.2.84 Cross-sectional structure of TFT with two-layer gate insulator.

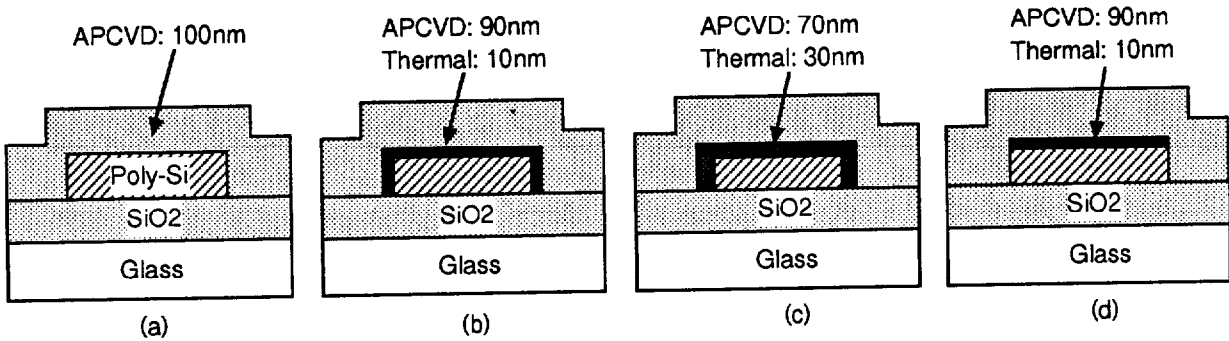


Fig. 2.85 Structures of gate insulator of TFTs.

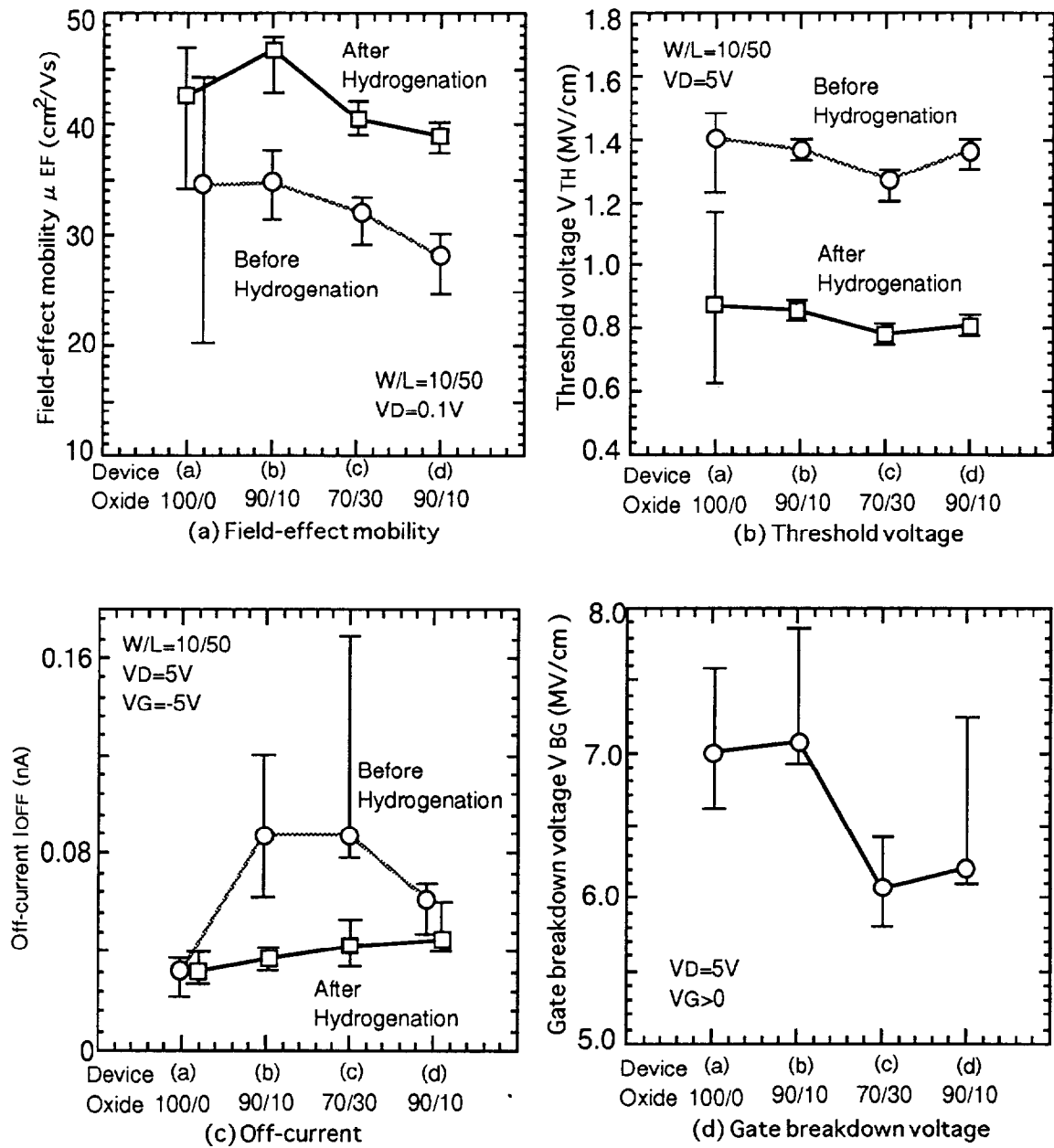


Fig. 2.86 Characteristics of TFTs with various gate oxides.
Oxide: APCVD/Thermal (nm).

realize the 3.3" poly-Si TFT-LCD with driver integration for the first time.

As the novel gate insulator preparation routes, photo-CVD at 300°C and thermal oxidation at 600°C were attempted. Both realized a cleaner interface of SiO₂ and crystal Si than APCVD SiO₂. The characteristics of the TFT with two-layer gate oxide of photo-CVD SiO₂ and APCVD SiO₂ were improved. But performance of TFT with two-layer gate oxide fabricated by thermal SiO₂ and APCVD SiO₂ had hardly any improvement because interface trapping characteristics were almost completely determined by the localized states in poly-Si in SPC quality poly-Si.

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Middle-Temperature Poly-Si TFTs by Two-Step Solid-Phase Crystallization

To realize high-performance middle-temperature poly-Si TFTs on the large quartz substrates below 900°C, high-temperature SPC technologies are reviewed. First, the high-temperature recrystallization procedure for poly-Si grains is investigated by observing the phenomena of contraction and shrinkage of thick poly-Si films at high temperature. Then, TFT characteristics are studied using devices fabricated by one- and two-step temperature SPC using LPCVD of SiH₄ and Si₂H₆.

For the proposed middle-temperature process, two-step SPC before patterning, gate insulator of CVD SiO₂, large area ion doping, and low temperature laser activation are introduced. The middle-temperature poly-Si TFT performances are noticeably improved over those of low-temperature process devices.

3.1 Introduction

3.1.1 Demands for very high resolution and small size poly-Si TFT-LCDs

Chapter 2 described the noticeable progress achieved for the performance of low-temperature poly-Si TFTs by optimizing the SPC at 600 °C. The possibility of monolithic integration of drive circuits for TFT-LCDs was shown. Furthermore, significant improvement of operation performance of circuits was also suggested by the CMOS configuration [1]. But the driving ability of the developed TFTs was still insufficient for application to actual poly-Si TFT-LCDs because the driving voltage was so high. The process temperature, 600°C may still be too high for mass-produced glass substrates.

But the developed low-temperature SPC technology should also be applicable to high-temperature poly-Si TFTs on quartz substrates. A high-temperature poly-Si TFT LCD was developed in 1984 [2]. In the high-temperature process, poly-Si quality was improved by a combination of low- and high-temperature two-step SPC using SiH₄ [3].

Typical product applications of high-temperature poly-Si TFTs are 0.5-1" LCDs for PJs, HMDs, etc. They are formed on 6-8" quartz wafers. But still larger size 2-3" diagonal very fine TFT-LCDs are also in

demand for high resolution projectors such as in HDTVs and XGA data PJs. In this case, heat resistive large substrates such as quartz plates would be better for mass production. In addition, the TFT fabrication rule should be reduced to a sub-micron one [4]. In these fine devices, uniformity of crystallinity as achieved by the recently used laser crystallization, would be insufficient.

In this chapter, at first, applications of SPC technologies are reviewed. Then a two-step temperature SPC for high-temperature poly-Si TFTs is studied and middle-temperature process technology is proposed to allow use of large area quartz substrates.

3.1.2 Proposal of middle-temperature poly-Si TFT process

Table 3.1 lists the characteristics of synthesized high purity quartz substrates. These substrates were first developed for high-temperature poly-Si TFT fabrication in LSI process equipment. Grades SX and SQ are for high- and middle-temperature process uses, respectively. Large quartz substrates have been conventionally produced for photolithography mask plates. And SQ grade large substrates with sizes up to about 300 mm X 400 mm are now available. Considering the substrate shrinkage and deformation, the maximum process temperature must be below 1000 °C.

Fig. 3.1 illustrates the fundamental technologies to fabricate high- and middle-temperature poly-Si TFTs. To realize high performance TFTs on large quartz substrates by the proposed middle-temperature process, introduction of two-step temperature SPC before patterning, use of a gate insulator of CVD SiO₂, exposure by high resolution LCD stepper, large area ion doping (see Chapter 6), and low-temperature laser activation (Chapter 6) were supposed.

Table 3.1 Characteristics of synthesized quartz substrates

Grade	Impurity (ppb)							Working Temp.	
	Al	Fe	Ca	Na	Mg	Na	Cl	-OH	(°C)
SX	1	2	1	0.1	0.1	0.1	200	50	1000-1100
SQ	1	2	1	0.1	0.1	0.1	100000	500000	950-1000

ShinEtsu Quartz: VIOSIL

3.1.3 High-temperature recrystallization and two-step SPC

In the high temperature poly-Si TFT process, deposited Si films were annealed at high temperature to get recrystallization and thus improve crystalline quality. Fig. 3.2 illustrates models of one- and two-step temperature SPC. Consideration of the results of low temperature SPC in Chapter 2 suggested that slow grain growth at low temperature SPC and continuous recrystallization at high temperature to promote grain growth and to reduce traps, were effective for realizing high quality poly-Si [3]. It is necessary to understand the mechanism of high-temperature SPC. First, the high-temperature recrystallization procedure of poly-Si grains

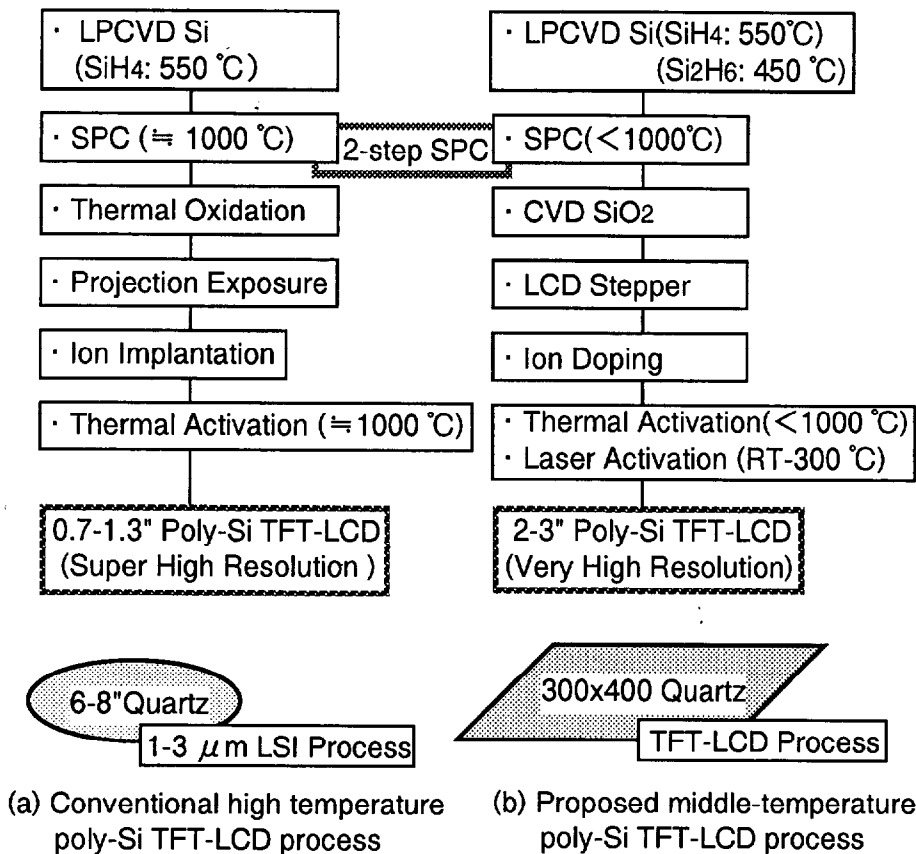


Fig. 3.1 A proposal in middle-temperature poly-Si TFT process.

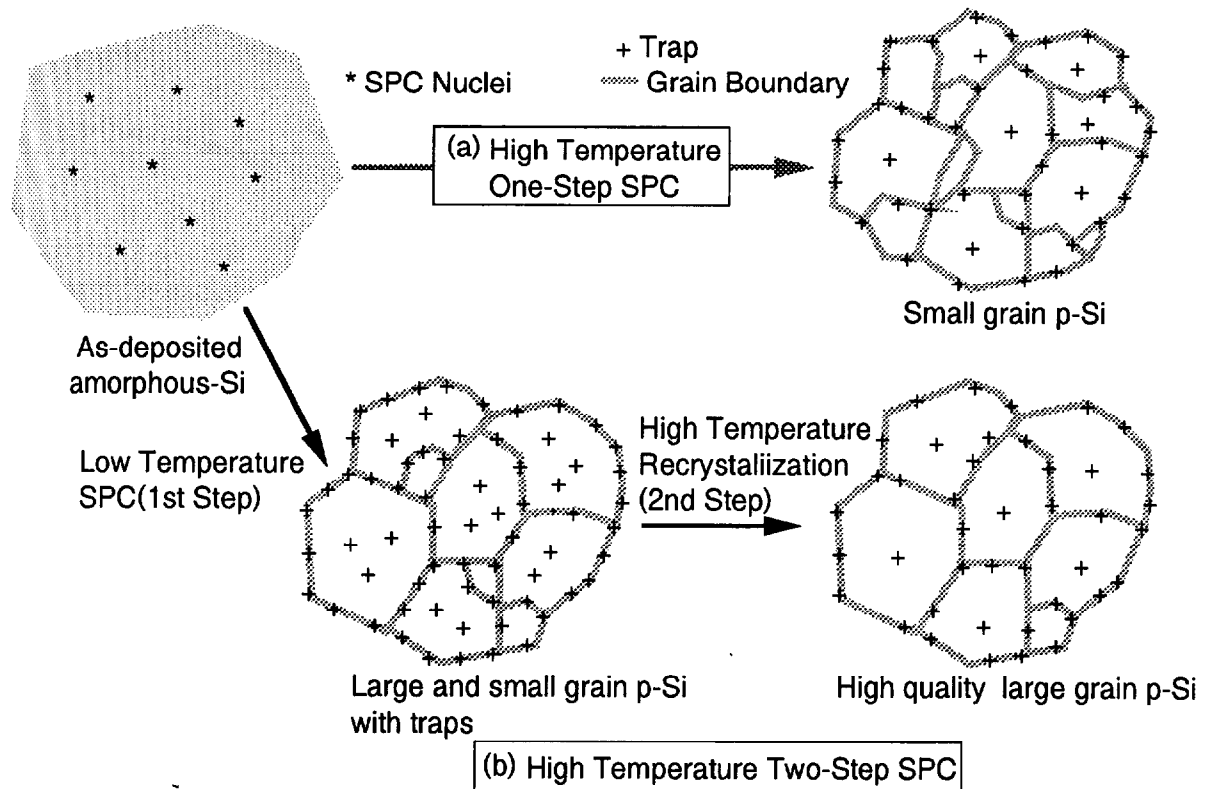


Fig. 3.2 Crystallization models for one- and two-step high temperature SPC.

was investigated by observing the phenomena of contraction and shrinkage of thick poly-Si films at high temperature. Then, TFT characteristics were studied for devices fabricated by one- and two-step SPC using SiH_4 and Si_2H_6 .

3.2 Expansion and contraction of thick poly-Si films at high temperature

3.2.1 Measurement of expansion and contraction of poly-Si films

Bulk poly-Si films were used for the experiments. Thick poly-Si layers (200-450 μm) were deposited in a conventional, vertical-type, RF-heated, epitaxial reactor by the hydrogen reduction of trichlorosilane (SiHCl_3) at 1100 - 1260 $^\circ\text{C}$. No doping impurities were intentionally added during the deposition. Substrates (50 mm diam) were n-type single crystal silicon wafers with a thickness of 300 μm and with a surface of (100) coated by a thermal oxide with a thickness of 1.7 μm .

Fig. 3.3 shows an example of a polished and Sirtle-etched cross section of a thick (220 μm) poly-Si layer grown at 1200 $^\circ\text{C}$. The poly-Si layer had a columnar grain structure. X-ray diffraction studies have shown that $\langle 110 \rangle$ texture predominated. Fig. 3.4 illustrates the poly-Si film sample used for the measurement of expansion and contraction. It was prepared by etching off both the single crystal silicon substrate and the SiO_2 film. The changes in length at high temperatures were measured with a dilatometer equipped with a differential transformer. The amount of expansion or contraction perpendicular to the growth direction was measured. High purity transparent quartz was used as a reference sample. The thermal expansion coefficient of quartz is about one order of magnitude smaller than that of single crystal silicon. The load for holding the samples was less than 10 g/mm^2 which is smaller than either the yield stress or nucleation stress of dislocations in single crystal silicon. The oxygen content of the high purity (99.999 %) nitrogen or argon which was used as the ambient gas in these measurements was monitored, and was always less than 2.0 ppm.

Fig. 3.5 shows typical measured results of the amount of expansion and contraction of a poly-Si sample heat-treated in nitrogen and oxygen atmospheres. The time interval from 0 to 112 min corresponded to the rise in temperature from room temperature to 1200 $^\circ\text{C}$ at a rate of about 10 $^\circ\text{C/min}$, and the time over 112 min corresponded to the heat-treatment process at the constant temperature of 1200 $^\circ\text{C}$. The poly-Si sample expanded with increases in temperature. However, the progress of the expansion slowed and contraction began to occur in the case of the nitrogen atmosphere when temperature exceeded about 1000 $^\circ\text{C}$. When the temperature reached 1200 $^\circ\text{C}$, contraction continued to proceed even when the temperature was held constant. Heat-treatments in an argon atmosphere have given the same results. In the case of the oxygen atmosphere, however, such contraction was not observed. It seemed that

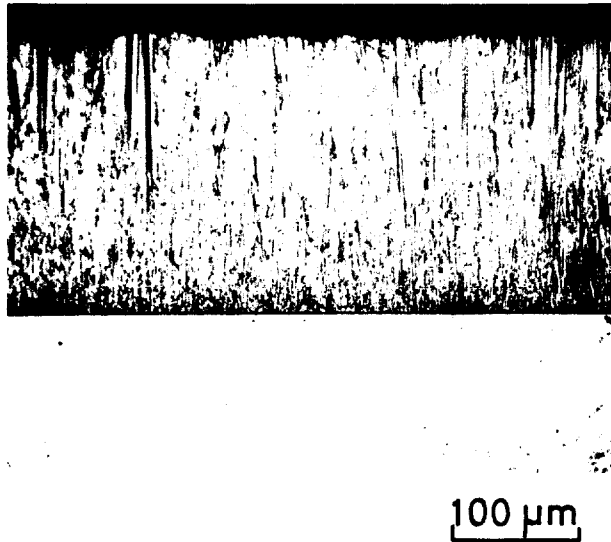


Fig. 3.3 Cross section of thick poly-Si layer deposited on an oxide-covered single Si wafer.

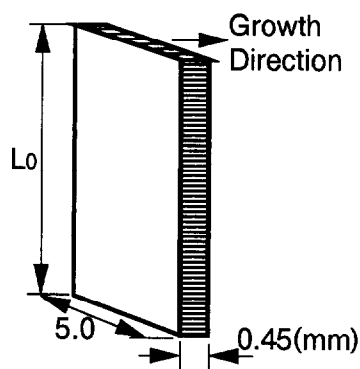


Fig. 3.4 Poly-Si sample used for measuring the expansion and contraction at high temperature.

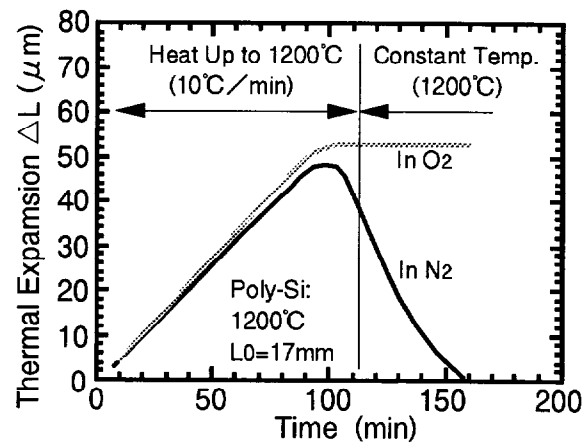


Fig. 3.5 Example graph of thermal expansion and contraction of poly-Si at 1200 °C.

volume expansion in the oxygen atmosphere compensated for the contraction of bulk poly-Si.

The measured thermal expansion coefficient for the single crystal silicon was 2.9-4.5 ppm/°C which agreed with the data reported by others [5], [6] in the temperature range of 100-900 °C. These results justified the measurement method used. The value of poly-Si deposited at 1230°C was 2.3-4.2 ppm/°C which was not so different from the value of single silicon.

3.2.2 A consideration for the contraction and recrystallization of poly-Si film at high temperature

Fig. 3.6 shows the influence of the growth temperature of poly-Si samples on contraction when heat-treated at 1200 °C in an argon atmosphere. The heat-treatment start ($t=0$) was defined as the time when the sample temperature reached 1200°C. The amount of contraction ΔL was obtained by subtracting the length at each time L from the initial length L_0 at $t=0$. The contraction of the poly-Si layer had a tendency to increase with decreases in growth temperature.

Fig. 3.7 plots the time dependence of the rate of contraction at different heat-treatment temperatures. The the poly-Si films were deposited at 1200 °C. The measured points fell approximately on straight lines, with a slope of 2/5, indicating that $L/L_0 \propto t^{2/5}$. The rate of contraction increased as the heat-treatment temperature increased.

These contraction phenomena of poly-Si film at high temperature implied there was recrystallization of poly-Si grains. Here, a sintering process such as in metals and ceramics grains was considered to explain the contraction. Fig. 3.8 illustrates the sintering model for grains proposed by Kingery and Berg. [7]. The rate of sintering is closely related to the mechanism of material transport at grain boundaries. Several types of models and theories of material transport have been reported. The model shown interprets the contraction during sintering as the decrease of distance between the center of two neighbor grains in contact. According to this model, substantial material transport into the contact region of the grains occurs and the grains approach one another, because the boundary acts as a sink for vacancy diffusion. The rate of decrease in the center-center distance L_0 of grains with radius r is expressed as follows:

$$\frac{\Delta L}{L} = \left[\frac{20\gamma a^3 D_V}{\sqrt{2}r^3 kT} \right]^{2/5} \cdot t^{2/5} \text{-----(3-1)}$$

where γ is surface tension at the contact point, a is the interatomic distance, r is the initial radius of a grain, k is the Boltzmann constant, T is the sintering temperature, t is the sintering time, and D_V is the self-diffusion coefficient. The self-diffusion coefficient D_V is given as

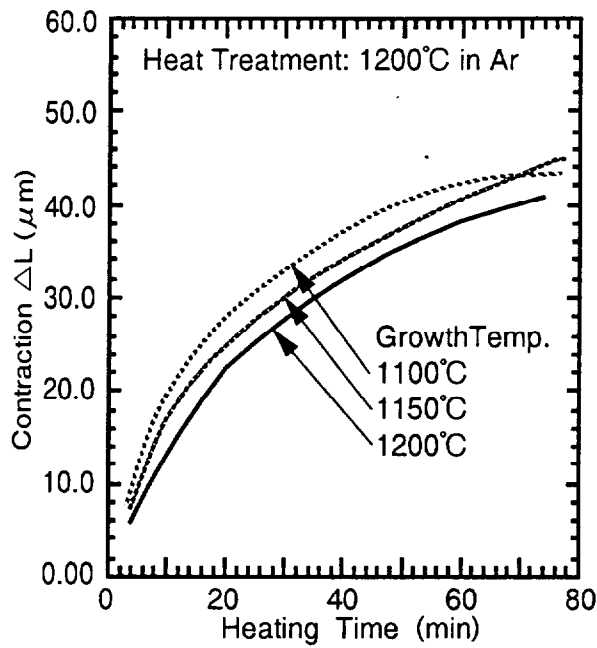


Fig. 3.6 Influence of growth temperature of poly-Si on contraction.

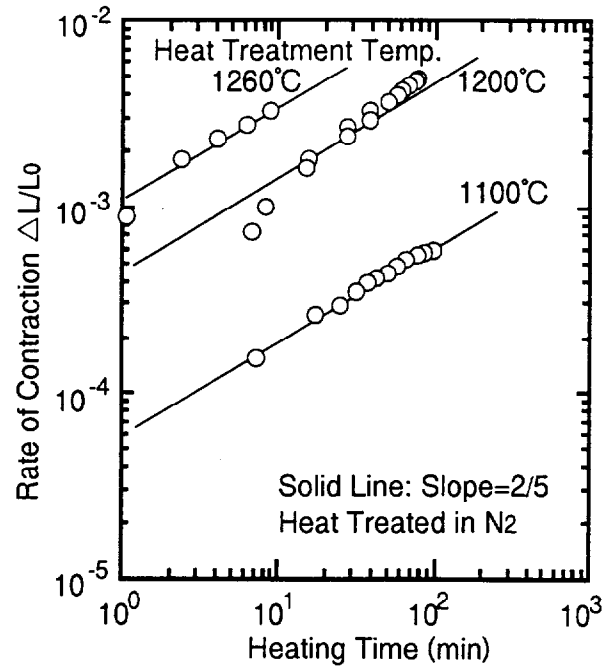


Fig. 3.7 Time dependence of the rate of contraction at various temperatures.

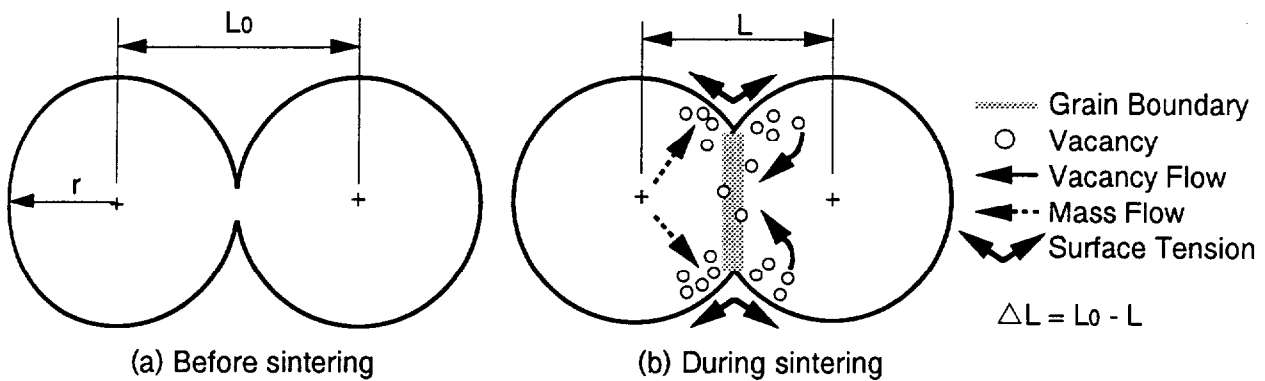


Fig. 3.8 Sintering model for grains proposed by Kingery and Berg [7].

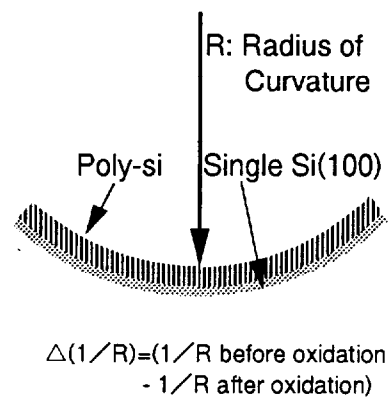
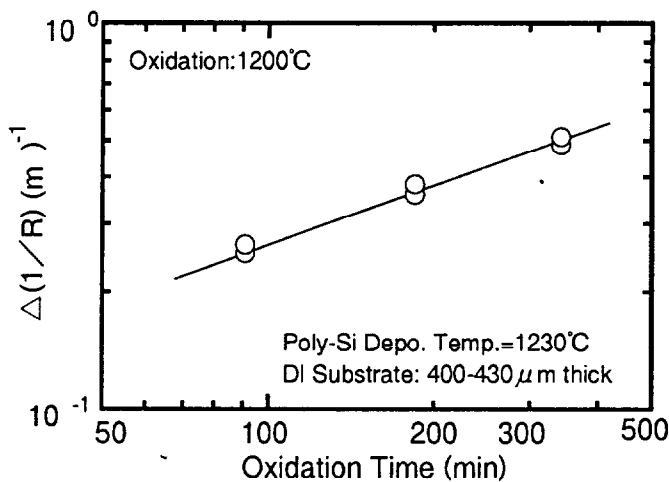


Fig. 3.9 Dependence of the amount of change in curvature on oxidation time in dielectrically isolated substrates.

$$D_V = D_0 \exp(-E_a/kT) \text{ -----(3-2)}$$

where E_a is the activation energy for self-diffusion of atoms.

The relation $\Delta L/L_0 \propto t^{2/5}$ was observed to hold in the contraction phenomena as shown in Fig. 3.7. The assumption was made that the contraction phenomena are ruled by this sintering model. If the temperature dependence of γ and a is ignored and t is assumed constant, equation (3-1) gives the next relation.

$$D_V \propto T \cdot (\Delta L/L_0)^{5/2} \quad (t=\text{constant})\text{----- (3-3)}$$

From the Arrhenius plot of $T \cdot (\Delta L/L_0)^{5/2}$ versus $1/T$, activation energy of 190 kcal/mole (8.2 eV) was obtained. This value is quite large compared to the activation energy of self-diffusion of Si in single crystal (112 kcal/mole = 4.9 eV) [8]. Therefore, the mechanism is not so simple as to be elucidated only by these models and assumptions. In an actual film, the grain shape and size are random, not ideal spheres. In addition, it is probable that small amounts of impurities such as oxygen in poly-Si affect the material transport and prevent the contraction as shown in Fig. 3.5. Under extreme conditions, expansion of poly-Si films was observed in high temperature oxidation. Fig. 3.9 shows the dependence of the amount of change in curvature on oxidation time in dielectrically isolated substrates which had thick poly-Si layer on a thin single crystal layer. The change of curvature indicated expansion of the poly-Si layer during oxidation and obstruction of Si atom self-diffusion.

From these experiments inspecting the contraction (perpendicular to the growth direction) of thick poly-Si film deposited at high temperature, it was suggested that poly-Si showed grain rearrangement. The rate of contraction increased when poly-Si deposition temperature was low and heat-treatment temperature was high. These phenomena should be expected to improve crystalline quality for low-temperature deposited thin poly-Si films which also have the same columnar grains.

3.3 Improvement of high-temperature poly-Si TFT characteristics

3.3.1 One-step SPC for LPCVD Si film using SiH_4

(1) Preparation of poly-Si films

The substrates were quartz or Si wafers coated by thermal SiO_2 (100 nm thick). Starting Si films with a thickness of 100 nm were deposited on these substrates by LPCVD using SiH_4 at 520-550°C. As-deposited films on quartz were recrystallized to get poly-Si at 1000 °C for 60 min in N_2 . Crystallinity of these films was investigated by thin film XRD.

Fig.3.10 shows XRD profiles of as-deposited Si films. Only broad peaks were observed corresponding to (111), (220), (311) surfaces.

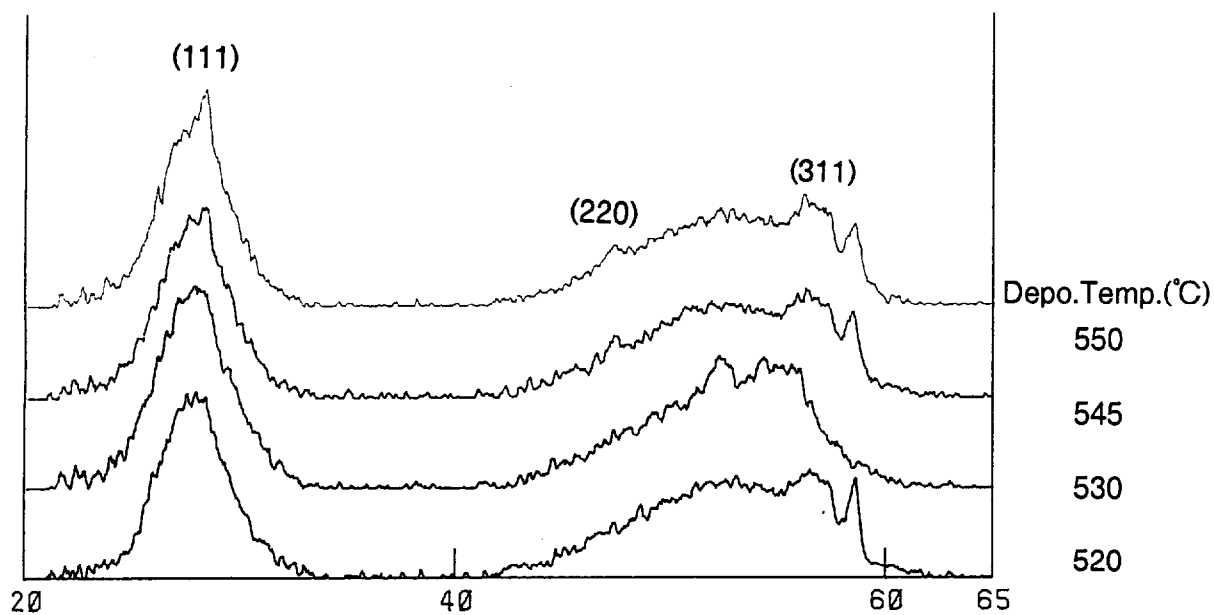


Fig. 3.10 X-ray diffraction profiles of as-deposited Si films using SiH_4 .

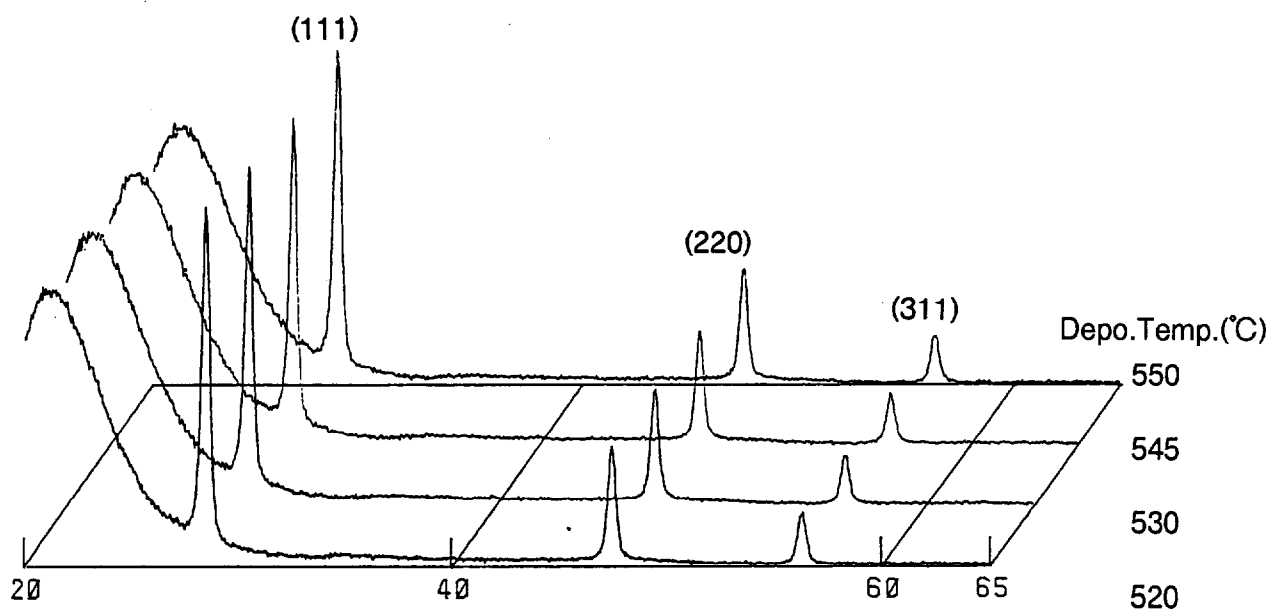


Fig. 3.11 X-ray diffraction profiles after high-temperature SPC.
Crystallization: 1000°C , 1h, in N_2 .

Therefore, these films were amorphous. This result agreed with that shown in Fig. 2.3.

Fig. 3.11 shows XRD profiles of crystallized poly-Si films on quartz substrates. Clear peaks of (111), (220), (311) were observed. The calculated grain sizes from each plane diffraction profile [9] are shown in Table 3.2. All grain sizes were almost the same though the values of the film deposited at 530 °C were slightly large. It was noted that the grain size was almost the same as that of 600°C SPC (Fig. 2.6). This may be caused by fast heating and fast increase of nucleation sites, though some recrystallization and grain growth were expected. But the trap state density must decrease as reported previously [3].

Table 3.3 shows the ratio of integrated intensity of X-ray diffraction from three surfaces. When the intensity of the (111) surface diffraction was normalized as 100, the values of (220) and (311) were smaller than the value of powder standard sample [10]. Therefore, all these films were preferentially orientated to $\langle 111 \rangle$ direction the same as for the 600°C SPC sample.

(2) TFT fabrication process

Fig. 3.12 shows the structures of n- and p-channel TFTs fabricated by high temperature SPC. Si film (100 nm thick) was deposited by LPCVD using SiH_4 on SiO_2 coated quartz substrates. The Si film was annealed at 1000°C for 1 h in N_2 for recrystallization. Then, the Si film was patterned into islands and oxidized in O_2 for 1 h to make 100 nm thick gate insulator. Poly-Si for gate was deposited by LPCVD and phosphorous was diffused at 950 °C. Gate poly-Si was patterned to make the gate and P^+ and B^+ ions were implanted for n-channel and p-channel regions. After PSG deposition for passivation, activation was carried out at 950 °C for 30 min. After contact hole etching, AlSi was deposited for metallization. Finally, the TFTs were annealed in forming gas at 400°C and hydrogenated by H_2 plasma at 300°C.

(3) TFT characteristics

Fig. 3.13 shows the effect of hydrogenation time on field-effect mobility of n- and p-channel TFTs. In this experiment, RF power and treatment time were reduced compared with previous experiments such as in Fig. 2.15. Increase of mobility for both n- and p-channel TFTs was saturated at treatment times over 10 min. The values of n-channel TFTs were larger than that of the 600°C SPC TFTs shown in Table 2.2. These results were supported by the fact that the trap state densities were decreased by high temperature SPC [3]. Fig.3.14 shows the V_G - I_D characteristics of high-temperature SPC TFTs before and after hydrogenation. The performance for both n- and p-channel TFTs was improved by hydrogenation. Fig.3.15 shows the V_G - I_D characteristics of TFTs by high- and low-temperature SPC [1]. The performance for both n- and p-channel TFTs was improved compared to the 600 °C SPC TFTs.

Table 3.2 Average crystallite size of poly-Si estimated from X-ray diffraction of (111), (220), (311) surfaces

Depo.Temp.	(Å)		
	(111)	(220)	(311)
530 °C	199	199	201
540 °C	195	195	198
545 °C	191	196	202
550 °C	195	194	186

Table 3.3 Ratio of integrated intensity of X-ray diffraction from three surfaces of poly-Si films fabricated by high-temperature SPC

Depo.Temp.	(111)	(220)	(311)
530 °C	100	37	17
540 °C	100	37	17
545 °C	100	37	17
550 °C	100	38	18
Powder Std.	100	55	30

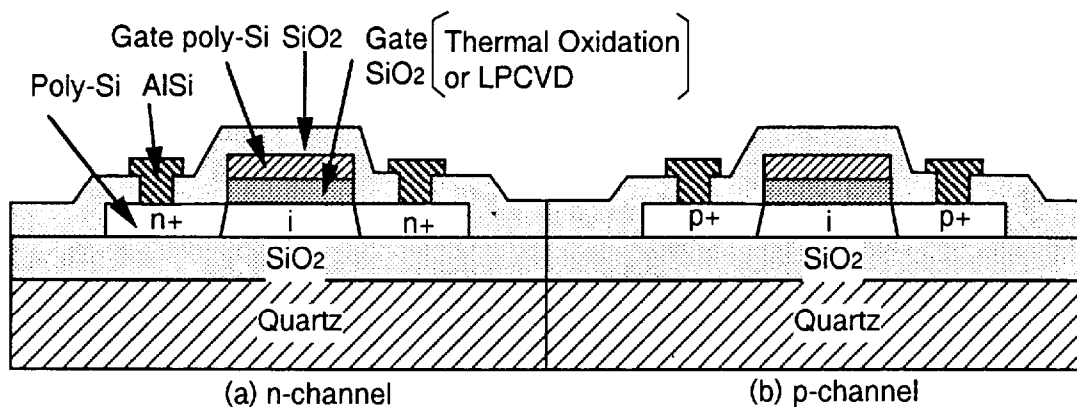


Fig.3.12 Cross-sectional structure of TFT fabricated by high-temperature SPC on quartz substrate.

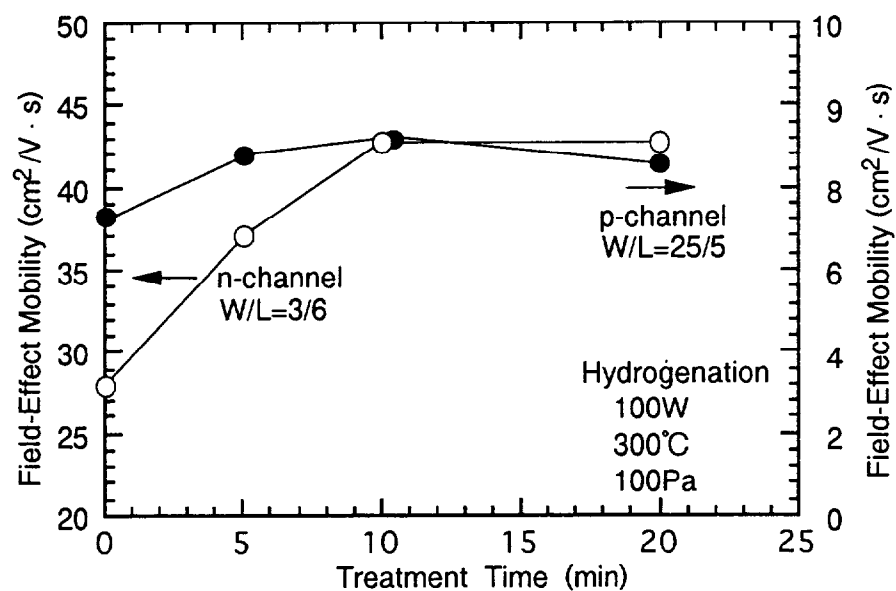


Fig. 3.13 Effect of hydrogenation time on field-effect mobility.

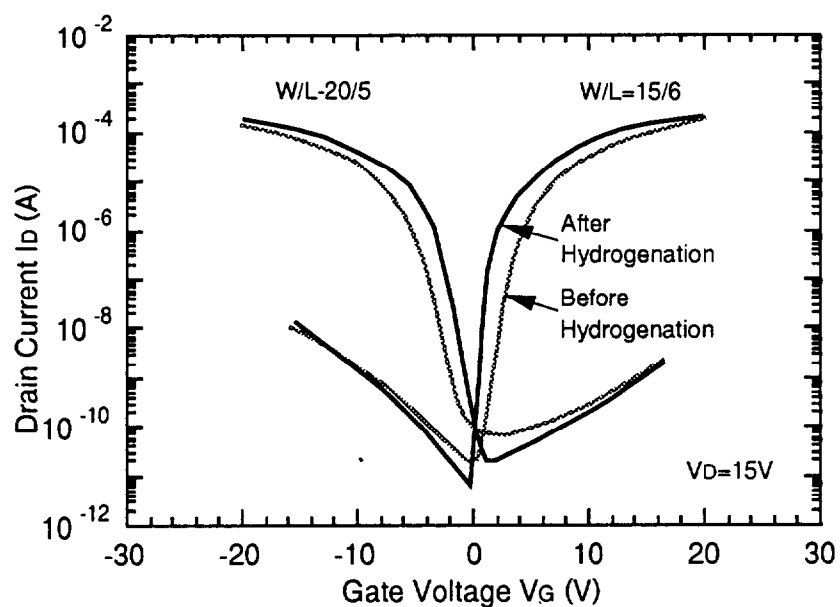


Fig. 3.14 Hydrogenation effect on V_g - I_d characteristics of high-temperature TFTs fabricated by one-step SPC.

3.3.2 Two-step SPC for LPCVD Si film using SiH_4 and Si_2H_6

(1) TFT fabrication process

The two-step SPC was proposed as the combination of 600°C SPC and 1000°C SPC using SiH_4 [3]. Also high-temperature TFTs were fabricated by LPCVD using Si_2H_6 [11]. These processes were reviewed. Si film (100 nm thick) was deposited by LPCVD using SiH_4 (550°C) or Si_2H_6 (450°C) on SiO_2 coated quartz substrates. First, the Si films were annealed to recrystallize at moderate speed at 600°C for 12 h in N_2 (first SPC). Then these films were annealed again at 1000°C for 1 h in N_2 (second SPC). The Si films were patterned into islands and oxidized in O_2 for 1 h to make 100 nm thick gate insulator. Poly-Si for gate was deposited by LPCVD and phosphorous was diffused at 950°C . Gate poly-Si was patterned to make the gate and P^+ and B^+ ions were implanted for n-channel and p-channel regions. After PSG deposition for passivation, activation was carried out at 950°C for 30 min. After metallization by contact hole etching and AlSi deposition, the TFTs were annealed in forming gas at 400°C .

(2) TFT characteristics

Fig. 3.16 shows V_G - I_D characteristics of TFTs fabricated by three recrystallization methods. The two-step SPC method was noticeably effective for improving TFT characteristics for both films deposited by SiH_4 and Si_2H_6 source gases. The TFT fabricated using Si_2H_6 showed the best performance (low off-current, sharp on-current raise, and high on-current) of the three TFTs. This was caused by the increase of crystallinity by large grain growth as shown in Fig. 3.18 below.

3.4 Middle-temperature poly-Si TFTs

3.4.1 TFT fabrication process

To use large quartz substrates, the maximum process temperature must be below 1000°C and it was set at 900°C . The basic concept of middle-temperature TFTs is to avoid high-temperature, long-time treatment and thus eliminate substrate shrinkage and deformation after patterning of films. Only middle-temperature SPC (2 h, 900°C) was used for starting Si films and the other procedures were carried out below 450°C .

Fig. 3.17 shows the proposed middle-temperature TFT process. The substrate was 100mm X 100mm quartz coated by SiO_2 . Starting Si film was deposited by LPCVD using Si_2H_6 at 450°C . The Si film was recrystallized by one-step annealing at 900°C for 2 h, or two step annealing with combination of 600°C SPC for 12 h and 950°C SPC for 2 h. Poly-Si films were patterned into islands and gate SiO_2 was deposited by LPCVD at 400°C . Ion doping (see Chapter 6) was used considering application to large substrates. After phosphorous and boron doping, activation was carried out by conventional thermal activation at 900°C for

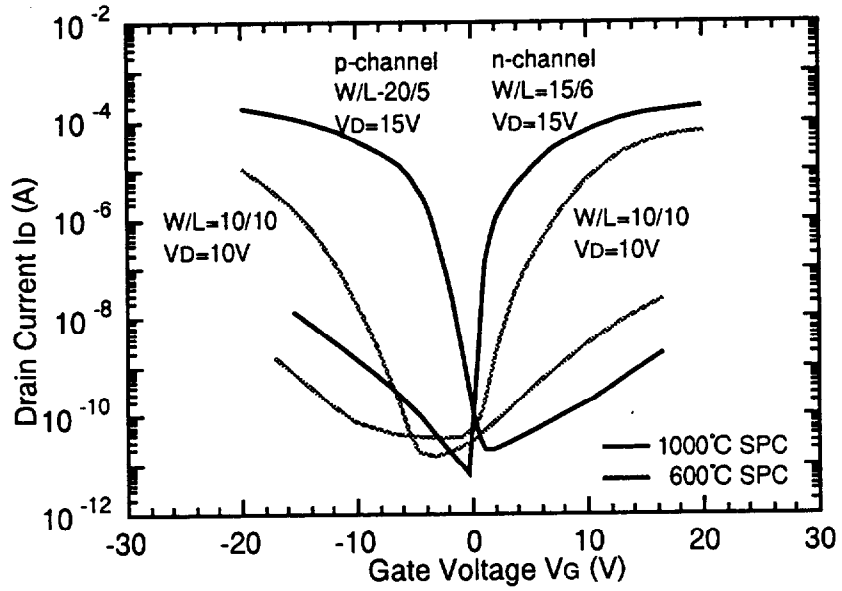


Fig. 3.15 V_G - I_D characteristics of TFTs fabricated by high- and low-temperature one-step SPC after hydrogenation.

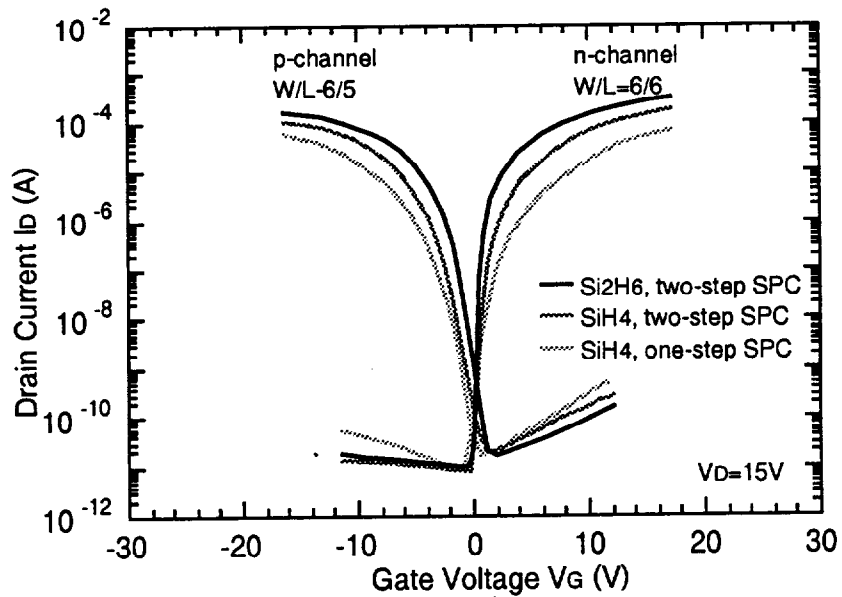


Fig. 3.16 V_G - I_D characteristics of TFTs fabricated by one- and two-step SPC using SiH_4 and Si_2H_6 .

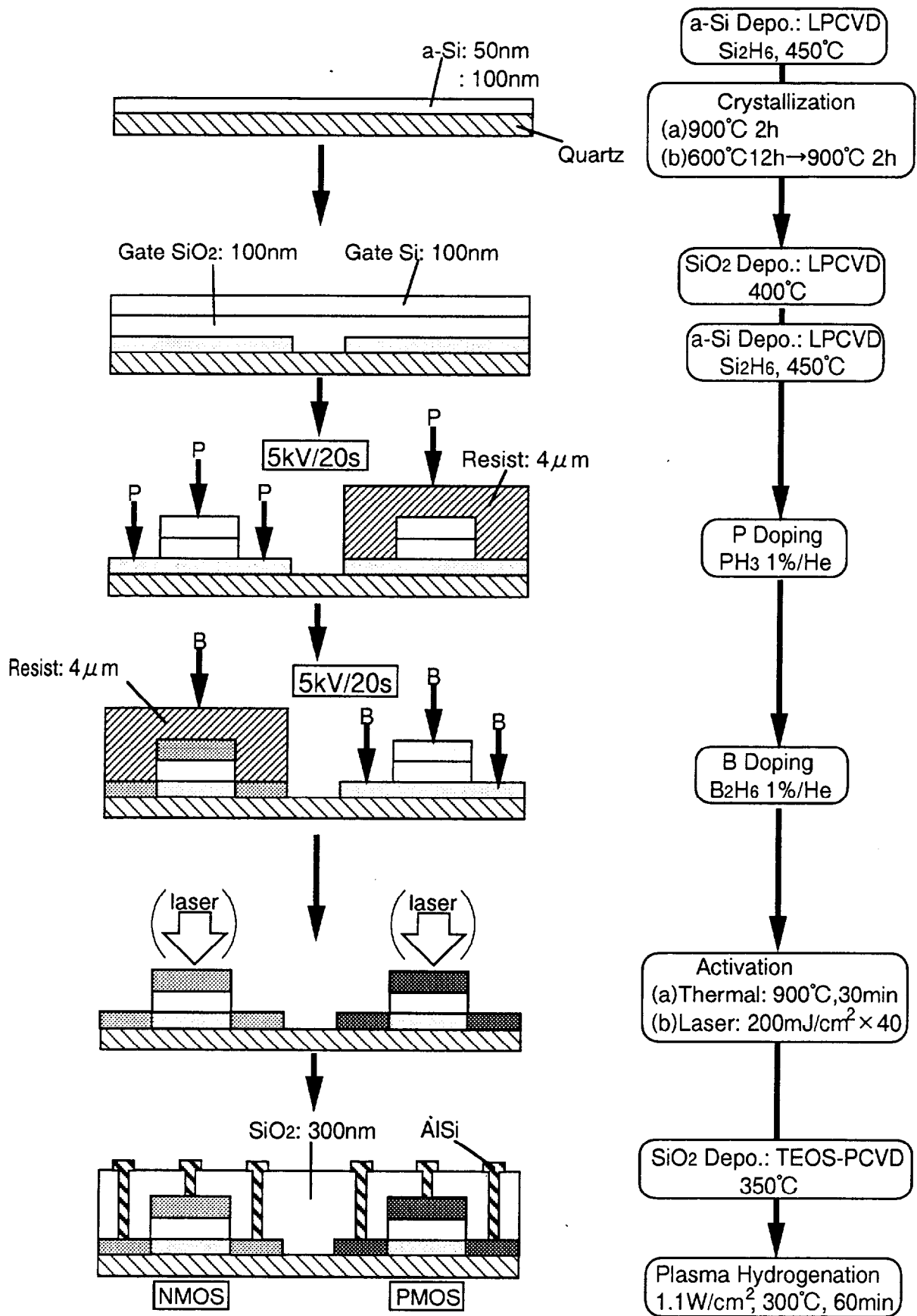


Fig. 3.17 Middle-temperature TFT fabrication process

30 min or low-temperature laser activation. After passivation by PECVD SiO_2 and metallization, TFTs were hydrogenated at 300°C .

3.4.2 One- and two-step SPC for LPCVD Si films using Si_2H_6

Starting Si films (50 nm and 100 nm thick) were deposited on quartz substrates by LPCVD using Si_2H_6 . At 600°C SPC, Si films deposited by Si_2H_6 showed better TFT characteristics than TFT from SiH_4 deposition [12]. In this experiment, the combination of 600°C and 900°C SPC was introduced. At first, Si films were crystallized at 600°C for 12 h in N_2 (first SPC), then, recrystallized at 900°C for 2 h in N_2 .

Fig. 3.18 shows SEM micrographs of Si film surfaces fabricated by one- and two-step middle temperature SPC using Si_2H_6 . Secco-etching [13] was used to reveal grain boundaries. Dendritic crystallites were observed for both films, but the 100 nm film with two-step SPC showed larger grains. This was attributed to promotion of large grain growth by two-step SPC and the capability of a thick film to get large grains because SPC started from the bottom interface of Si film as shown in Fig. 2.5 [14].

Fig. 3.19 shows the XRD diffraction profiles of one- and two-step SPC Si films with 50 nm and 100 nm thickness. Clear peaks of (111), (220), (311) were observed. Table 3.4 shows average crystallite size and intensity ratio obtained by XRD. As expected, the two-step SPC film with 100 nm thick had the largest crystallite size. It was almost the same as that of 1000°C one-step SPC (Table 3.2) though two-step SPC was carried out at 900°C . Thin 50 nm film showed the lowest value as implied in Fig. 3.18. The intensity ratio indicated that these films also had $\langle 111 \rangle$ preferential orientation as SiH_4 deposition.

The grain growth mechanism to get dendritic crystallites was reported by Noma et al. [15] for amorphous Si film by Si implantation. There are three possible kinds of grain growth due to the direction of {111} twin planes. Considering that poly-Si films have dendritic crystallites and $\langle 111 \rangle$ preferential orientation, the growth mechanism was thought to be as shown in Fig. 3.20. Generally, (111) surface has the slowest regrowth rate in solid phase epitaxy [16]. When the {111} facet is nucleated at the SiO_2 interface, the {111} microtwin is easily introduced. When the {111} twin planes are inclined to the film surface, $\langle 111 \rangle$ oriented growth occurs and dendritic growth to $\langle 110 \rangle$ direction is enhanced.

3.4.3 TFT characteristics

Fig. 3.21 shows the dependence of the field effect-mobility on channel width for the TFTs fabricated by one- and two-step SPC. For n-channel TFTs, the mobility of the two-step TFTs was about two times larger than that of the one-step TFTs and 600°C TFTs (Table 2.3). The mobility of p-channel two-step TFTs also had a larger value than the one-step TFTs.

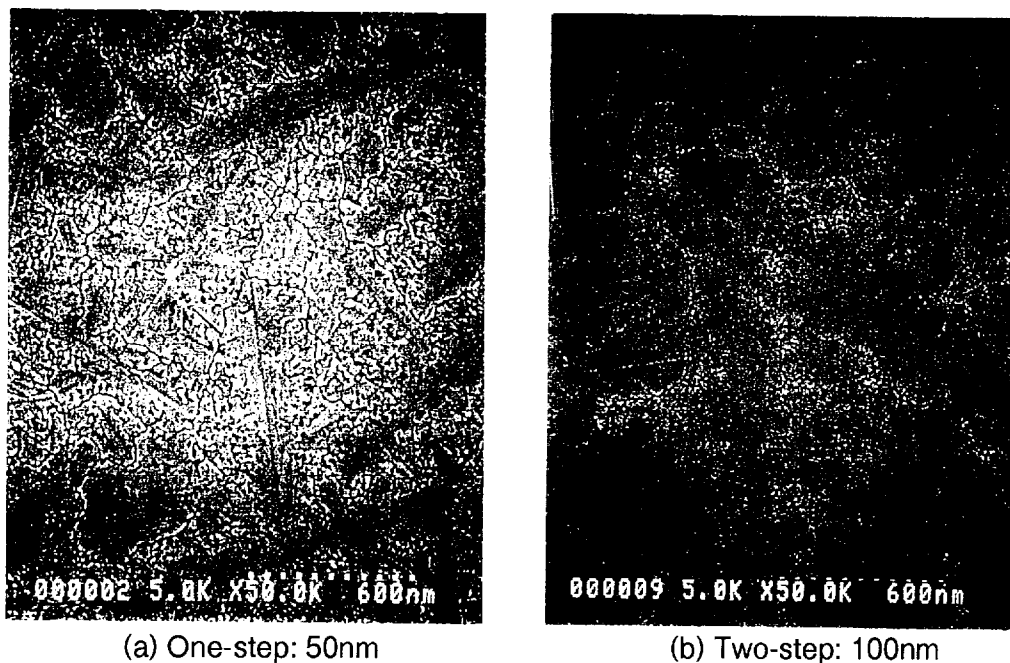


Fig. 3.18 SEM micrographs of poly-Si films prepared by one- and two-step middle-temperature SPC using Si_2H_6 .

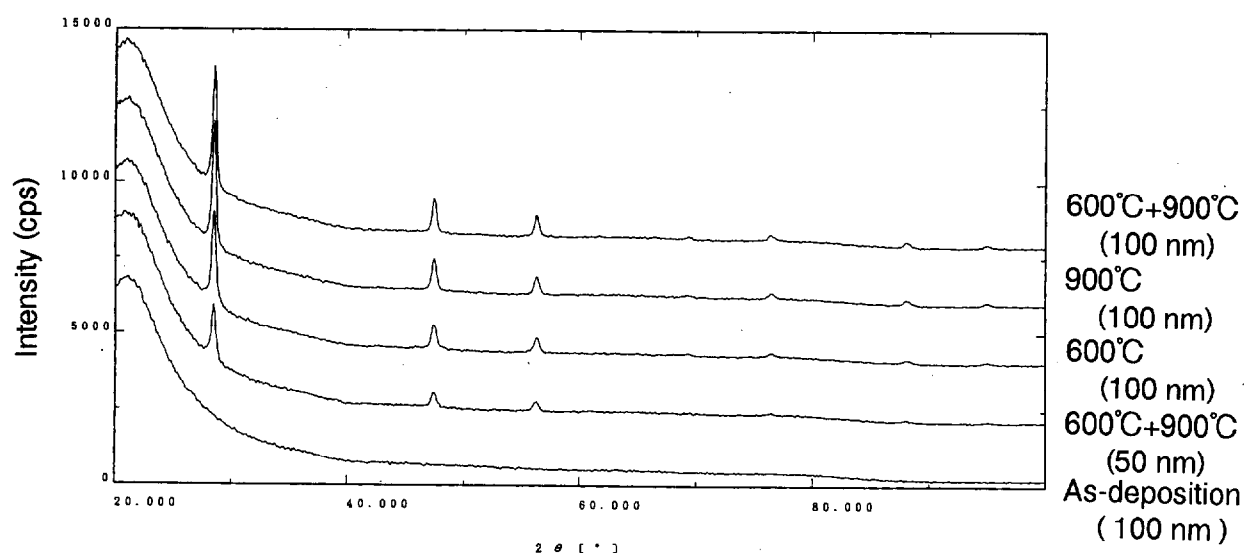


Fig. 3.19 XRD profiles of one- and two-step SPC films.

Table 3.4 Average crystallite size and intensity ratio obtained by XRD

	Sample	(111)	(220)	(311)
Crystallite Size (Å)	600°C (100 nm)	181	159	161
	900°C (100 nm)	193	176	176
	600°C+900°C (100 nm)	199	181	178
	600°C+900°C (50 nm)	177	154	164
Intensity Ratio	600°C (100 nm)	100	32	21
	900°C (100 nm)	100	31	18
	600°C+900°C (100 nm)	100	33	21
	600°C+900°C (50 nm)	100	35	19
	Powder Std.	100	55	30

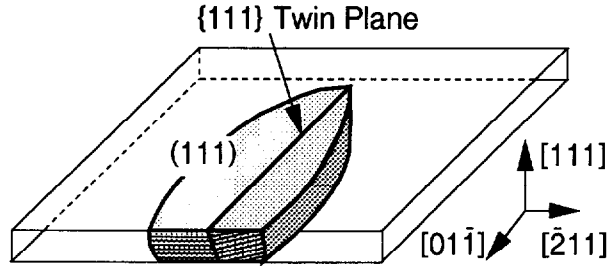


Fig. 3.20 Schematically depicted model of $\langle 110 \rangle$ preferential growth and (111) surface orientation [15].

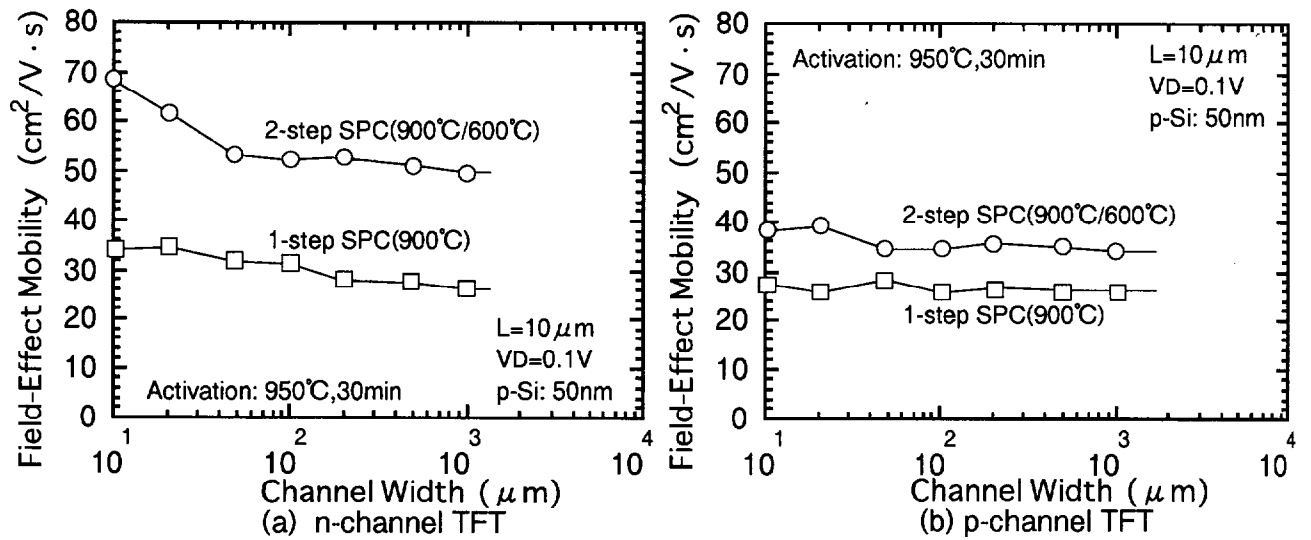


Fig. 3.21 Dependence of field-effect mobility on channel width for the TFTs fabricated by one- and two-step SPC.

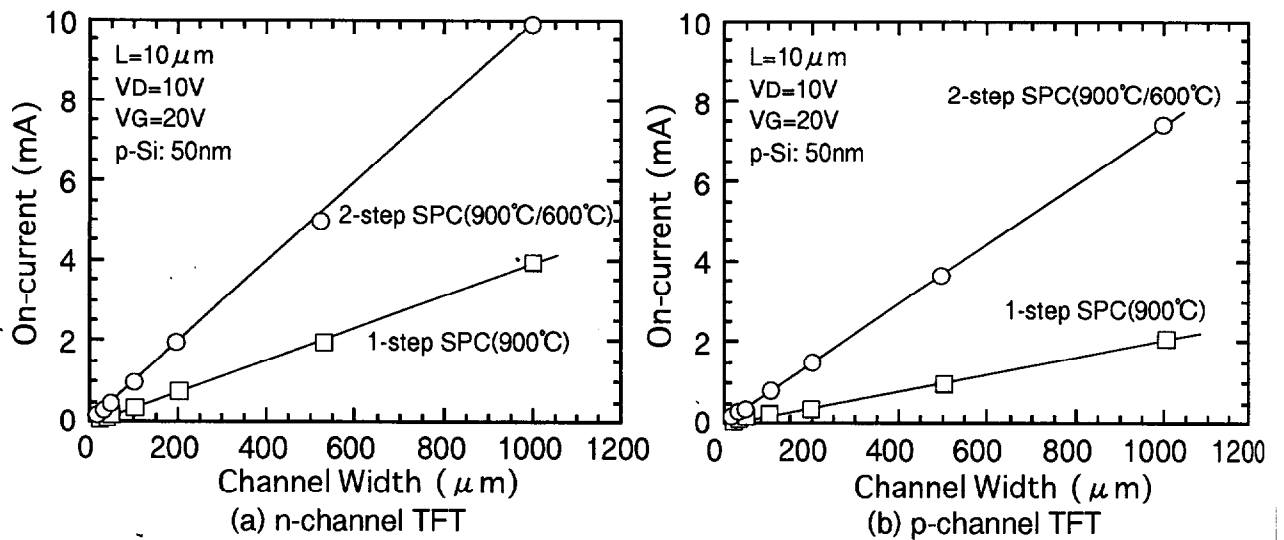


Fig. 3.22 Dependence of on-current on channel width for the TFTs fabricated by one- and two-step SPC.

These results showed suitability of two-step SPC for producing high performance TFTs.

Fig. 3.22 plots the dependence of the on-current on the channel width for the TFTs fabricated by one- and two-step SPC. On-current was clearly proportional to the channel width at the large widths. There was a report that on-characteristics had a dependence on channel width [4]. The on-current of two-step TFTs was more than two times larger than that of one-step devices.

Fig. 3.23 shows the dependence of field-effect mobility on channel width for the TFTs with poly-Si thicknesses of 50 and 100 nm. TFTs with 100 nm poly-Si had slightly high mobility than the 50 nm TFTs. This result agreed with the grain size difference shown in Fig. 3.18.

Fig. 3.24 shows the dependence of field-effect mobility on channel width for the TFTs fabricated by laser and thermal activation. The former TFTs had slightly higher mobility than the latter. It was considered that laser activation improved the crystallinity of source and drain region by melting and recrystallization though thermal activation contributed to recrystallization only by SPC. The results of laser activation indicated the effectiveness of the technology for middle-temperature TFT fabrication on large quartz substrates. These performances were comparable to those of conventional high-temperature poly-Si TFTs shown in Fig. 3.13.

3.4.4 Advance crystallization by hybrid method

In this study, SPC in N_2 ambient was used. For advanced crystallization, oxidation thinning of poly-Si film [11] and combination of SPC and laser crystallization were proposed for flat and high quality poly Si films [17].

Fig. 3.25 shows a example of combination of high-temperature SPC and laser crystallization (Chapter 7). At low laser energy of $350\text{mJ}/\text{cm}^2$ ((a)), after SPC grains were remained. At high energy of $450\text{ mJ}/\text{cm}^2$ which could melt poly-Si((b)), the poly-Si film has large grains and high ridges caused by SLG regime [18]. But twin boundaries remained. These poly-Si grains should have excellent characteristics such as a smoother surface and high mobility. On the WSi layer, poly-Si films had small grains because of high thermal conductivity of WSi.

3.5 Conclusions

The middle-size, very high-resolution driver integrated TFT-LCD is one possible application field for poly-Si TFTs. This TFT-LCD should be practically produced on large quartz substrates by the middle-temperature process below 1000°C . To realize high-performance middle-temperature poly-Si TFTs, high-temperature SPC technologies were reviewed. First, the high-temperature recrystallization procedure for poly-Si grains was investigated by observing the phenomena of expansion and contraction of

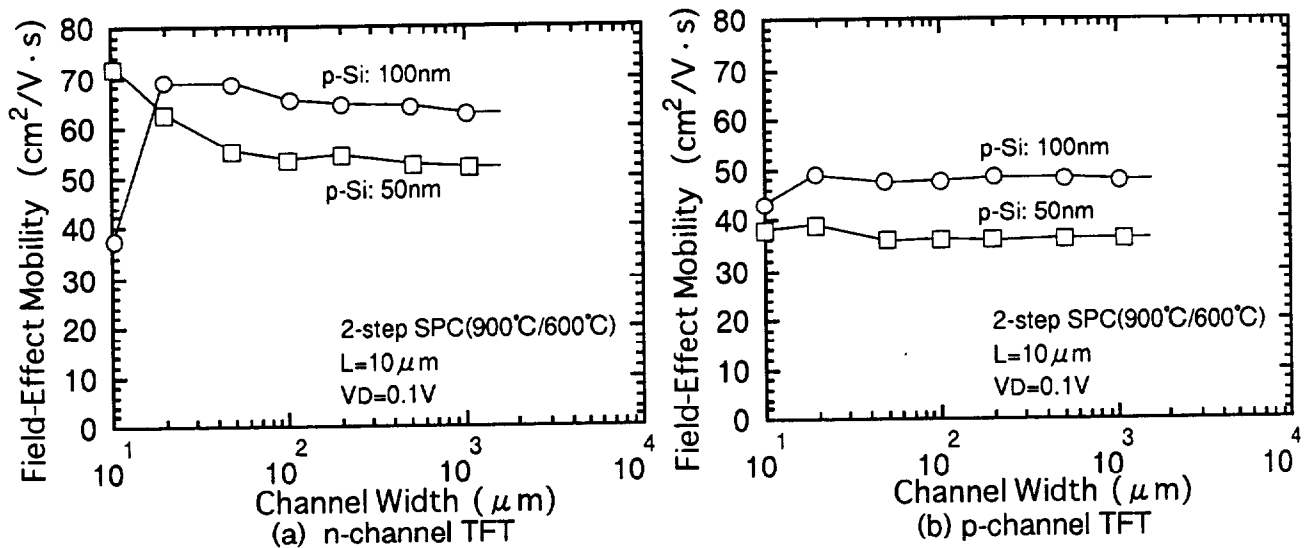


Fig. 3.23 Dependence of field-effect mobility on channel width for the TFTs fabricated by two-step SPC.

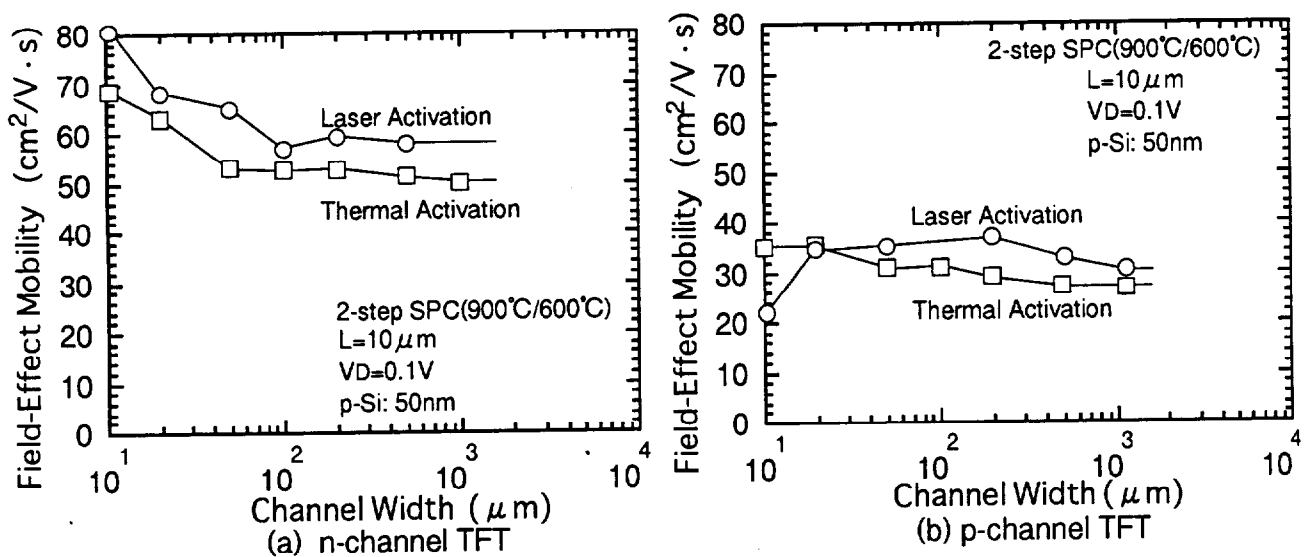
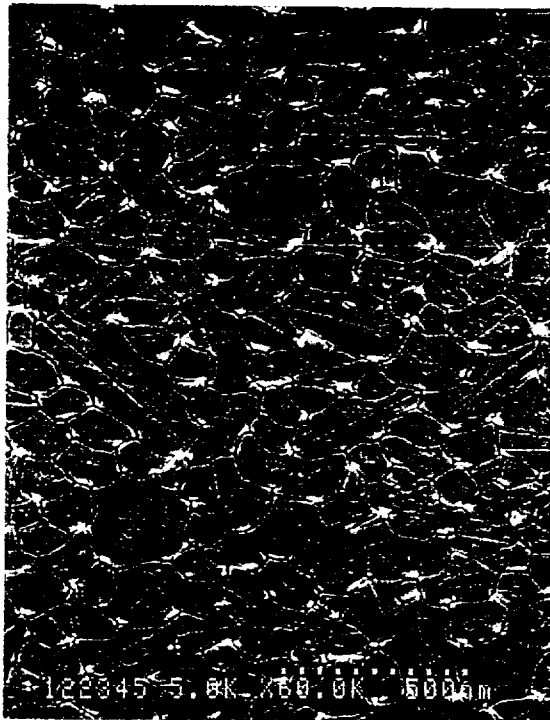
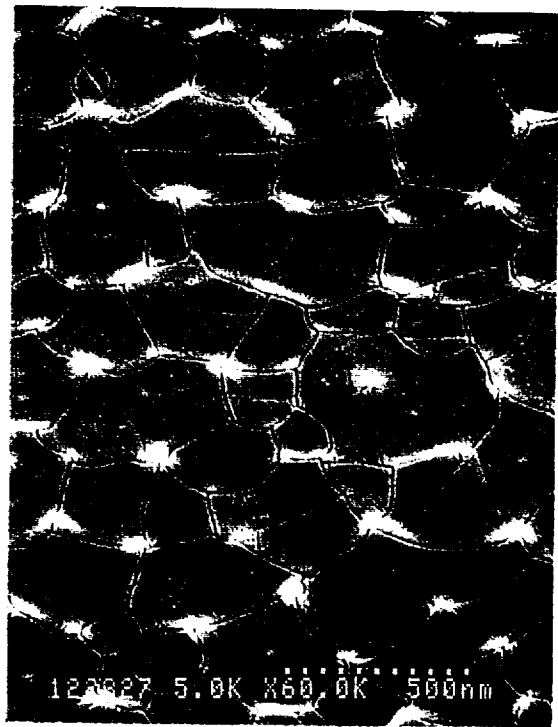


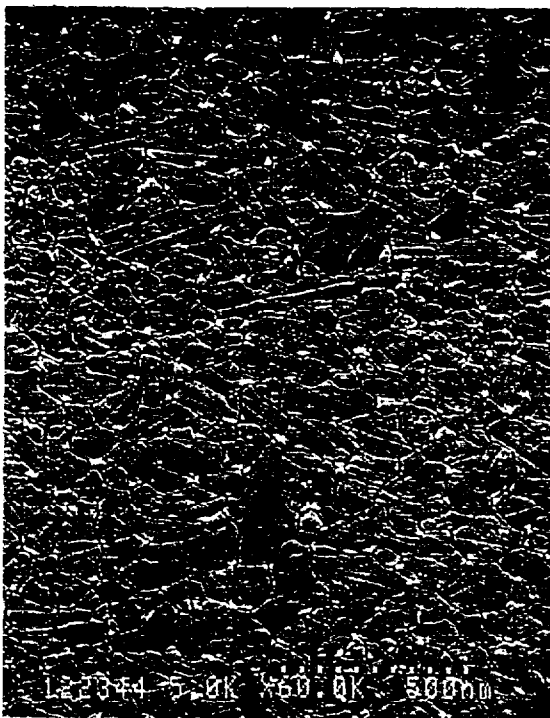
Fig. 3.24 Dependence of field-effect mobility on channel width for the TFTs fabricated by laser- and thermal-activation.



Si/SiO₂/Quartz

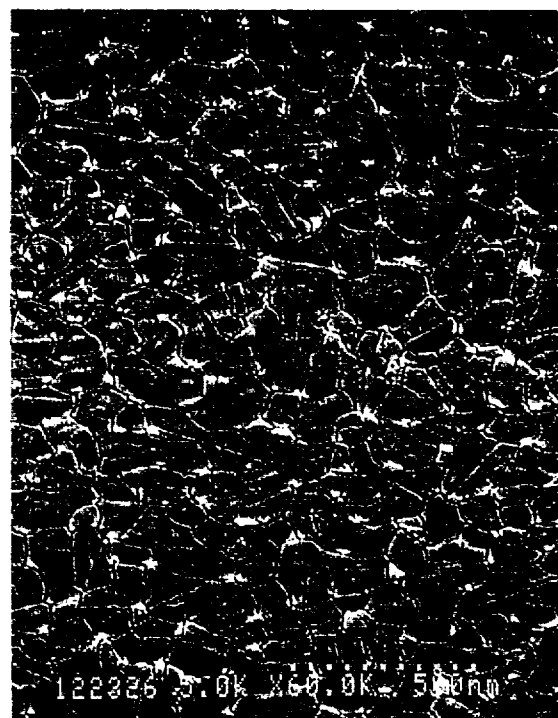


Si/SiO₂/Quartz



Si/SiO₂/WSi/Quartz

(a) 350mJ/cm²



Si/SiO₂/WSi/Quartz

(b) 450mJ/cm²

Fig. 3.25. Combination of HT-SPC and ELA

SPC: 1000°C, N₂

ELA: Excimer laser at RT

thick poly-Si films at high-temperature. Then, TFT characteristics were studied using devices fabricated by one- and two-step temperature SPC using LPCVD of SiH_4 and Si_2H_6 .

To realize high-performance TFTs on large quartz substrates by the proposed middle-temperature process, two-step SPC before patterning, gate insulator of CVD SiO_2 , large area ion doping, and low-temperature laser activation were introduced. The TFT performances were noticeably improved over those of low-temperature TFTs. This implied a possibility of fabrication of high performance TFT devices on large quartz substrates below 900°C for very high resolution LCDs.

3.6 References

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SOI TFTs by Zone-Melting Recrystallization

To realize high quality SOI on quartz substrates, radio frequency-heated zone-melting recrystallization (RF-ZMR) with connected islands is introduced. Large area crystallinity is inspected by thermal oxidation, wrinkle observation, and conventional etch pit methods. Micro-structure is inspected by TEM and EBD. Ultimate high-performance n-channel TFTs (SOI TFTs : c- TFTs) are obtained.

For a simple fabrication process, a p-channel poly-Si gate SOI TFT is adopted to realize a high-resolution active matrix for a LCD for the first time, by applying gate 3 μm LSI process. Effect of sub-grain boundary direction on field-effect mobility and off-current was studied. The TFT also has a high on-off ratio of 10^6 under illumination. These TFTs are used to fabricate very fine 1.15" diagonal LCD with 220 x 222 pixels, each 80 x 105 μm^2 .

A fundamental p-channel E-E type ring oscillator and a two-phase clock dynamic shift resistor are also evaluated to show the possibility of high-resolution active-matrix-type LCDs with a monolithically integrated driver using only p-channel SOI TFTs.

4.1 Introduction

The silicon TFT is a key component for new function devices and it is made from various starting films such as amorphous silicon, poly-Si and single crystal Si. Silicon on insulator (SOI) generally refers to high quality crystalline silicon films prepared on an insulator or isolated from the silicon substrate. Examples of the former include SOIs fabricated by zone-melting recrystallization [1], [2], energy beam recrystallization [3], [4], hetero-epitaxy using CVD such as silicon on sapphire (SOS), and solid-phase epitaxy. Typical examples of the latter are separation by implanted oxygen (SIMOX) or transfer bonding. SOI TFTs offer high quality, and their applications to three-dimensional devices [5] and high-speed LSIs [6], [7] have been studied. The SOI technology will be the main stream for high-speed low-power consumption ULSIs.

An especially important application of SOI TFTs on transparent quartz substrate is for addressing TFT arrays for LCDs. The current active-matrix-type LCDs use amorphous silicon TFTs or low-temperature poly-Si TFTs. These TFTs have lower mobilities ($1\text{--}150\text{ cm}^2/\text{V}\cdot\text{s}$) than SOI TFTs, but they are advantageous for large area LCDs because they are generally fabricated at low-temperature on glass substrates.

The very high mobility of SOI TFTs is an attractive characteristic that has the possibility of monolithic driver full integration to increase compactness and reduce the number of connections [8], [9]. Using a fine process and transparent substrate, small-size TFTs, and driver integration, a very high-resolution and transmissive (reflective) structures are realized. There are many possible uses for such high-resolution matrices in small-size LCDs, e.g., electronic view finders (EVFs) in video camera, HMDs, and PJ engines.

Some attempts to apply SOI TFTs as active matrices have been reported using n-channel TFTs [4], [9]–[11]. The n-channel TFTs have high mobility, but they also have a large kink effect. Therefore, the source-drain breakdown voltage is low and channel shortening is difficult in a simple structure and process. Furthermore, to suppress parasitic MOSFETs (the side channel and back channel), the TFT fabrication process becomes complex and long. The n-channel TFT has light sensitivity and it may be true for the p-channel TFT. From these considerations, the only disadvantage of the p-channel SOI TFT is that its mobility is lower than that of the n-channel. But this value may be sufficient for TFT-LCD use.

In this experiment, the RF-ZMR method [12] is used to obtain a high-quality nearly single crystal silicon layer over a large area. The quality of SOI films is examined. Then the p-channel TFT is adopted and fabricated by applying $3\text{ }\mu\text{m}$ LSL process. Discrete TFTs, basic p-channel E-E type logic circuits, and a high-resolution active matrix with 220×222 pixels (each $80 \times 105\text{ }\mu\text{m}^2$) are fabricated for the first time, and fundamental characteristics are studied. In addition, direct contact of ITO on SOI TFT is studied to simplify the TFT fabrication process.

4.2 Fabrication and evaluation of SOI films

4.2.1 RF-ZMR

A large recrystallization area is necessary to make an active matrix. To obtain high-quality crystalline silicon, the RF-ZMR method with connected silicon islands [11], [13] was introduced. Poly-Si ($0.5\text{ }\mu\text{m}$ thick) was deposited by APCVD at 900°C on a fused quartz substrate with 3" diameter and 0.5-mm thickness. The poly-Si layer was patterned into silicon islands that were connected with narrow silicon strips in the crystallization direction. The crystallinity and surface orientation critically depend on connection conditions [13]. The most serious fabrication problem is generation of cracks in SOI films in the cooling

stage after RF-ZMR because the thermal expansion coefficient of silicon is ten times larger than that of quartz.

Fig. 4.1 illustrates a Si island structure. To avoid the concentration of large tensile stress in large area Si films, the films were divided into random size islands and connected by a narrow stripe to facilitate zone-melting and recrystallization. Fig. 4.2 illustrates the general connection rule used in the experimental fabrication. Areas A, B, C, and D show the device area, dummy area, island-to-island connector, and chip-to-chip (cell-to-cell) connector, respectively. The device area was surrounded by X_1 and Y_1 dummy areas (each 10 μm wide) to avoid contact with island edges. The maximum X_0 and Y_0 were 230 μm to avoid cracks. To achieve (100) surface dominant recrystallization, choosing the dimensions of the connector is very important [13]. In this study, X_2 was 30mm and Y_2 was 0-30 μm , typically 30 μm . In the active matrix region, $Y_2 = 0 \mu\text{m}$. The minimum width of the windows (island-to-island) was 10 μm . In the first step of the connector layout design, chip-to-chip connectors were automatically arranged, then device areas were connected using the rule. The dummy islands were located and connected via chip-to-chip connectors when they were isolated in the direction of crystallization.

Fig. 4.3 shows photographs of the connected island patterns. A pair of matrices was located in the center area of the substrate. In the active matrix region, about 500 islands were connected by each line, with a total of 100,000 islands in a pair of matrices. In the test element group regions, there were some exceptions to the rule mentioned in Fig. 4.2.

After patterning of the poly-Si layer, SiO_2 (1.1 μm thick) was deposited as a cap layer using LPCVD at 740°C. The SOI substrates were recrystallized by the RF-ZMR method at about 1430-1450°C [2].

Fig. 4.4 shows the recrystallization apparatus for RF-ZMR and temperature profile. The carbon susceptor was heated at radio frequency of 13.56 MHz to provide a narrow high-temperature region. The SOI substrates were slid onto the carbon susceptor by a driving motor at a speed of 5 mm/s. At the maximum temperature region which was higher than the melting point of Si (1412°C), the poly-Si layer was melted. Recrystallization started when that melt passed the highest temperature region. In this stage, the upper reaches of the solid region acted as seed. Thus continuous zone-melting-recrystallization was carried out.

4.2.2 Evaluation of crystallinity

(1) Evaluation methods

To evaluate silicon layer quality, the etch pit method [14] is generally used. The cap SiO_2 layer in the RF-ZMR process or thermal oxide is used as an etching mask. Small through-holes are made in the SiO_2 layer using a photolithographic mask of contact-hole patterns for TFTs. Then aqueous potassium hydroxide (KOH) is applied at 60 °C to reveal anisotropic etch pits.

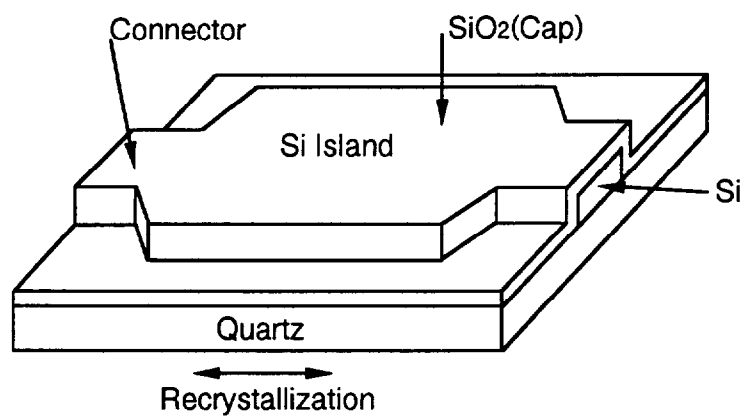


Fig. 4.1. Structure of Si island for RF-ZMR.

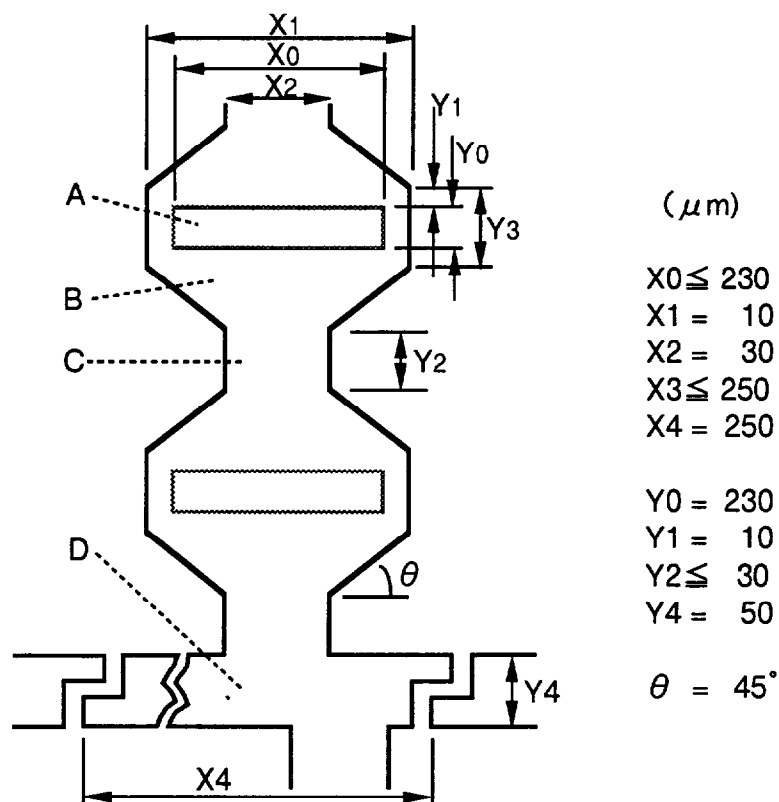


Fig. 4.2 . The general connection rule of Si islands used.

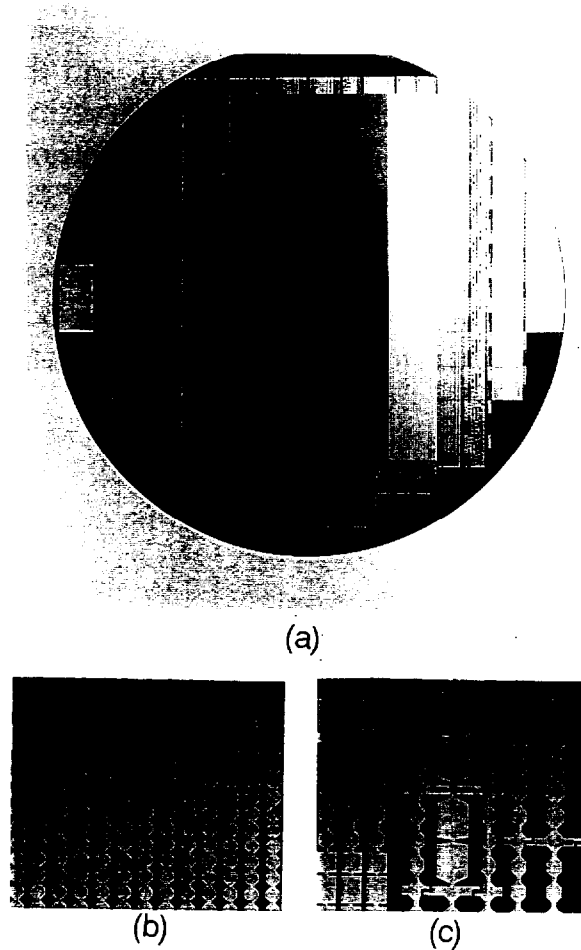


Fig. 4.3. The actual connected patterns used.
 (a) The entire substrate pattern. (b) The active matrix region pattern.
 (c) The test element group pattern.

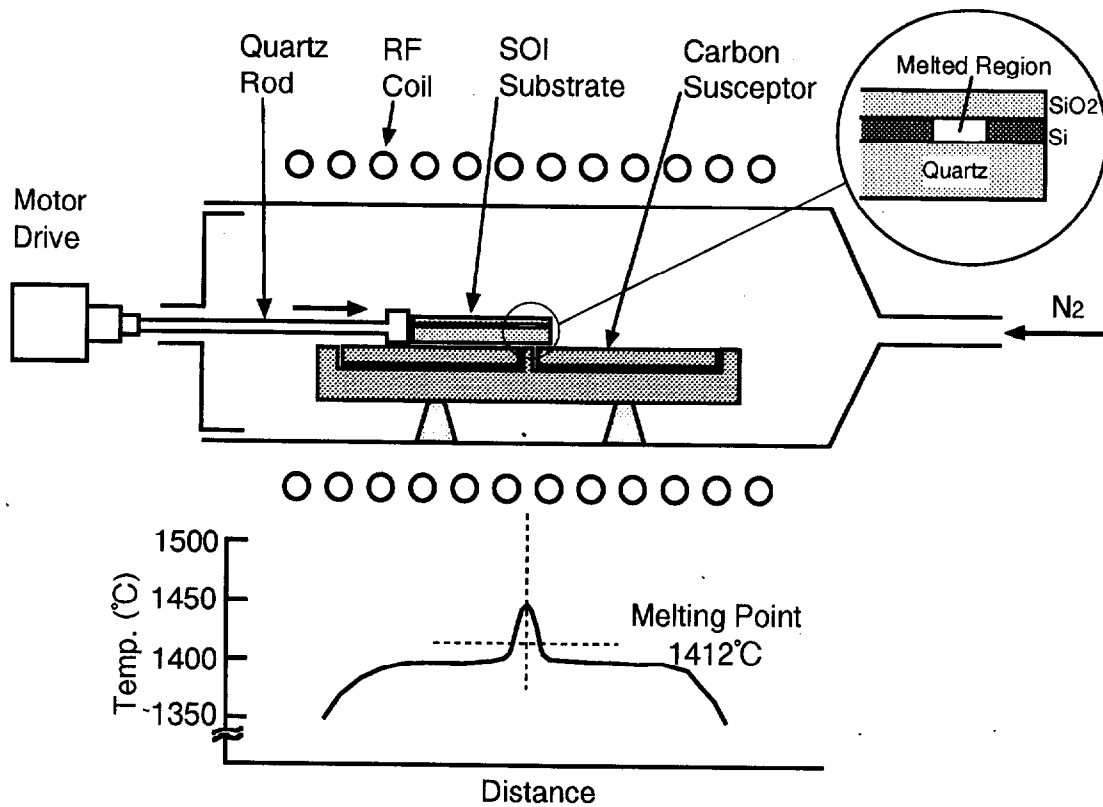


Fig. 4.4. Recrystallization apparatus and temperature profile.

The etch pit method is a destructive method, and the inter-pit region cannot be observed. To allow more careful observation, in-process and nondestructive methods were tried. The first method was a wrinkle observation method. After recrystallization, wrinkles appeared that were caused by liquid mass flow. The wrinkles flowed smoothly in the recrystallization direction in the normal region. Their disorder reflected the disorder of the recrystallization. Wrinkles could be clearly observed by projecting oblique light without magnification just after recrystallization.

The second method was interference color observation. The cap SiO_2 was removed and the silicon layers were thermally oxidized. Then the interference color was observed using a microscope. The difference in color was based on the oxidation speed difference caused by an orientation difference of the silicon surfaces. Under the conditions employed here, the oxidation speed of the (111) surface was 40 % higher than that of the (100) surface. When this technique was applied as the gate oxidation process, in-process observations could be made.

The SOI films were also investigated by TEM and EBD.

(2) Crystallinity of silicon layer observed by etch pit method

The entire substrate area was recrystallized. In the matrix area, about 100,000 connected islands were successfully recrystallized without failure. Macro-defects such as cracks were not observed. Generally, the silicon layers had a smooth (100) surface and small-angle grain boundaries [12].

Fig. 4.5 shows anisotropic etch pits along one line that has about 500 connected islands in a 7-cm length. Fig. 4.5 (a) was of the starting region without patterning of silicon layer. (b) and (e) were of test element group regions located in the matrix periphery and they had irregular shaped islands and connections. (c) and (d) were active matrix regions. The two lines in the active matrix regions were separated from one cell-to-cell connector after the (b) region and connected in one cell-to-cell connector before the (e) region. From the starting region to the end one, the etch pits were square indicating that the silicon layer was a single crystal that had a (100) surface and a large recrystallization area would be possible. Close observation of (d) and (e) showed the edge lines of the pits were slightly rotated to the left implying the existence of small-angle grain boundaries between the islands.

From these results, it was confirmed that the RF-ZMR method could result in a long line of islands and a large area of recrystallization, though the orientation of the silicon layer had a slight dependence on recrystallization length.

The (100) surface is ideal for MOSFETs. The yield of the (100) surface and the surface crystallinity were studied using thermal oxidation and wrinkle observation methods, in addition to the conventional etch pit method.

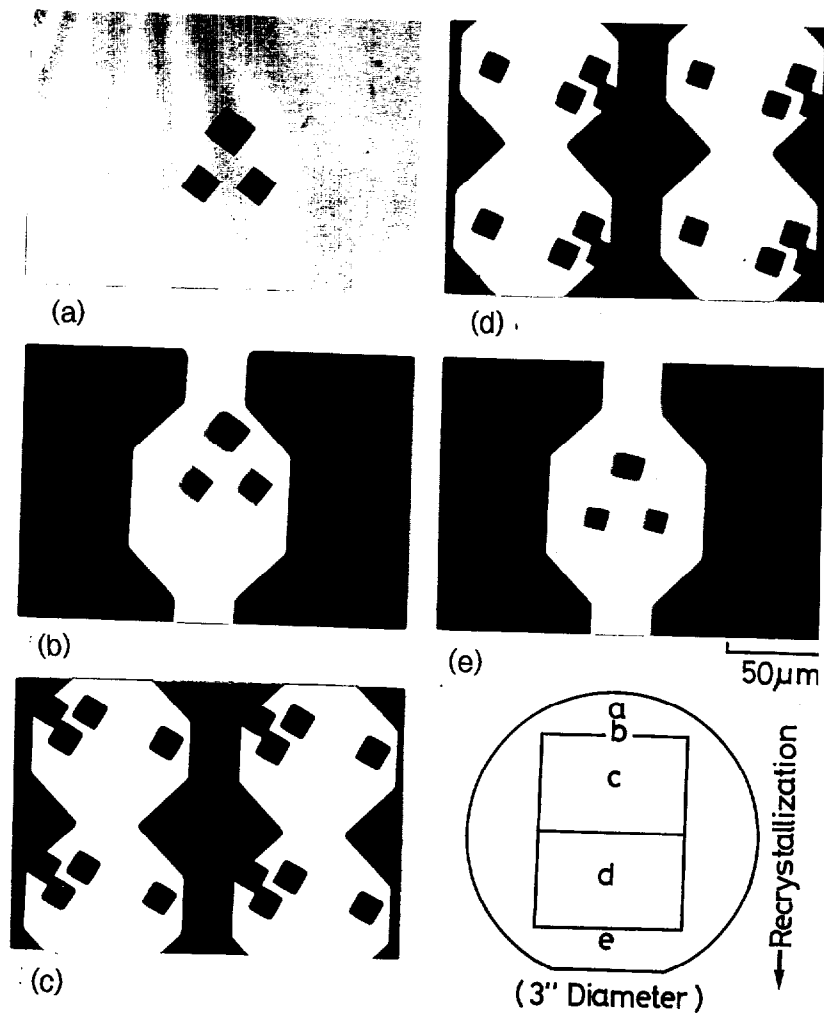


Fig. 4.5. Anisotropic etch pits in silicon islands along one line. (a) Starting region. (b),(e) Test element group regions. (c),(d) Active matrix regions.

Fig. 4.6 shows anisotropic etch pits masked with a thermal oxide layer 300 nm thick. In Fig. 4.6 (a), a normal region of crystallinity, the interference color of the oxide was uniform and all of the etch pits were square indicating that this area was high-quality single crystal with the (100) surface. In (b), there was an abnormal line L_2 that had the hexagonal etch pits. The interference color fringes in the inner area of the long islands in the upper part indicated a thickness distribution of the silicon layer. Line L_2 was a different color from the other lines and had irregular wrinkles. Considering information gathered in the etch pit observation, line L_2 had a (111) surface and was oxidized at a higher rate than the other ones. Its irregular wrinkles suggested that solidification in the recrystallization step did not proceed smoothly. In additional experiments, isolated silicon islands had a few ridges after recrystallization because heat flow was not controlled and solidification suddenly terminated at random points due to super cooling. Therefore, it was assumed that observed wrinkles were caused by interruption of the heat flow and continuous mass flow in solidification.

In another observation, the interference color change in a line indicated that the predominant (100) surface obstructed regrowth of the (111) surface that partially appeared in the side of the line. These results verified that the thermal oxidation method was useful for precise observations of crystallinity.

Fig. 4.7 plots the dependence of yield of the (100) surface on the heater structure. The maximum temperature at the projection must be higher than the melting point of Si (1412°C). In the solidification region, the substrate temperature must be below the melting point. When h_2 was 80 μm , yield of 90-95 % was obtained. The yield decreased when h_2 was 30 μm . Large h_2 contributed to making a large temperature difference between the projection and heater plate on the cooling side. These results indicated that when the solidification was conducted smoothly the yield of (100) surface was increased.

Using these recrystallization and observation methods, the yield of the (100) islands in the matrix region was estimated as 95 %. This value was large enough for trial manufacture of matrices. Yield improvements would be possible by eliminating photolithographic defects and precisely controlling the island connection conditions and recrystallization conditions.

(3) Crystal growth mechanism in RF-ZMR

Fig. 4.8 shows the crystal growth mechanism in RF-ZMR. When the zone-melting method is applied to the Si films, an interface of liquid and solid appears. Photos of (a) show cracks and sub-grain boundaries after Sirtle etching in non-prepatterned film. After etching, many cracks appeared because SOI film on quartz has very large tensile stress. The grain boundary where crack direction changed discontinuously had large-angle boundary. But, the crack line was almost straight at sub-grain

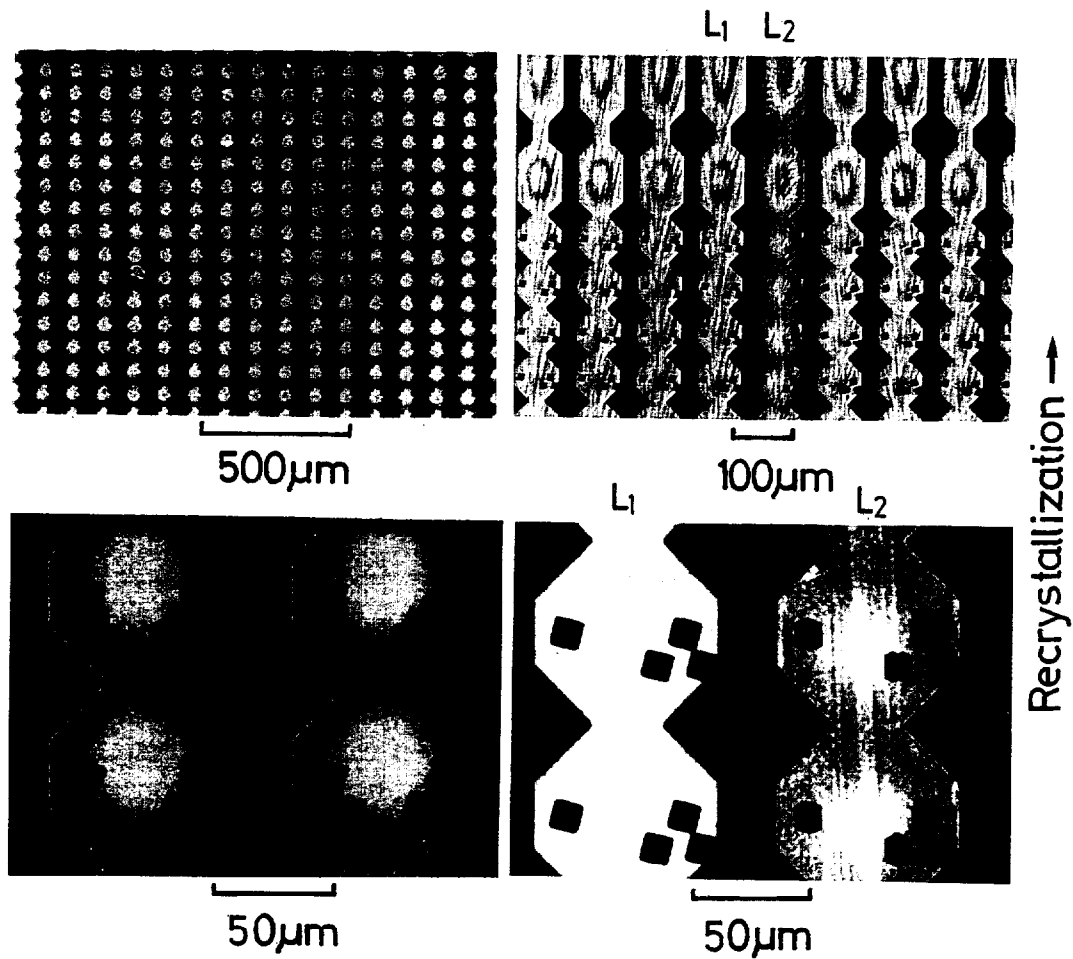


Fig. 4.6. Anisotropic etch pits masked with thermal oxide in active matrix regions.
(a) Normal region with (100) surface. (2) Abnormal region with (100) and (111) surfaces.

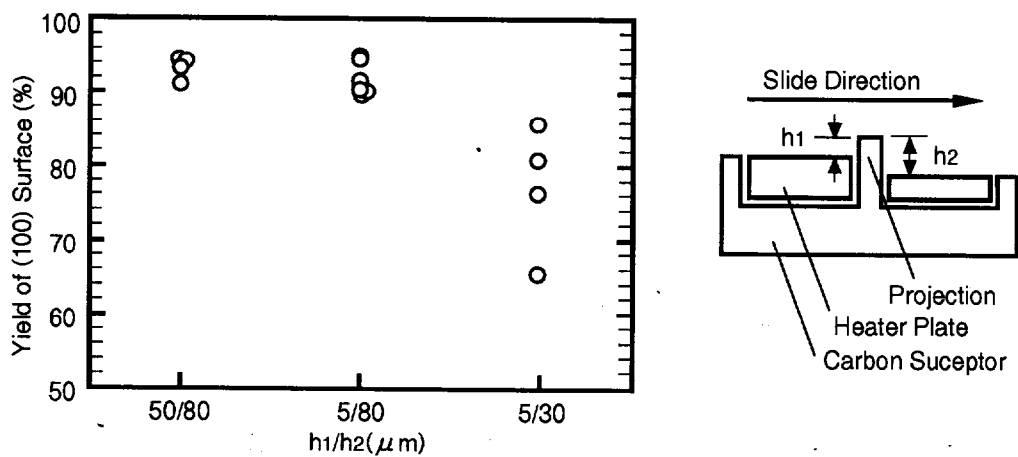


Fig. 4.7. Dependence of heater structure on the yield of (100) surface.

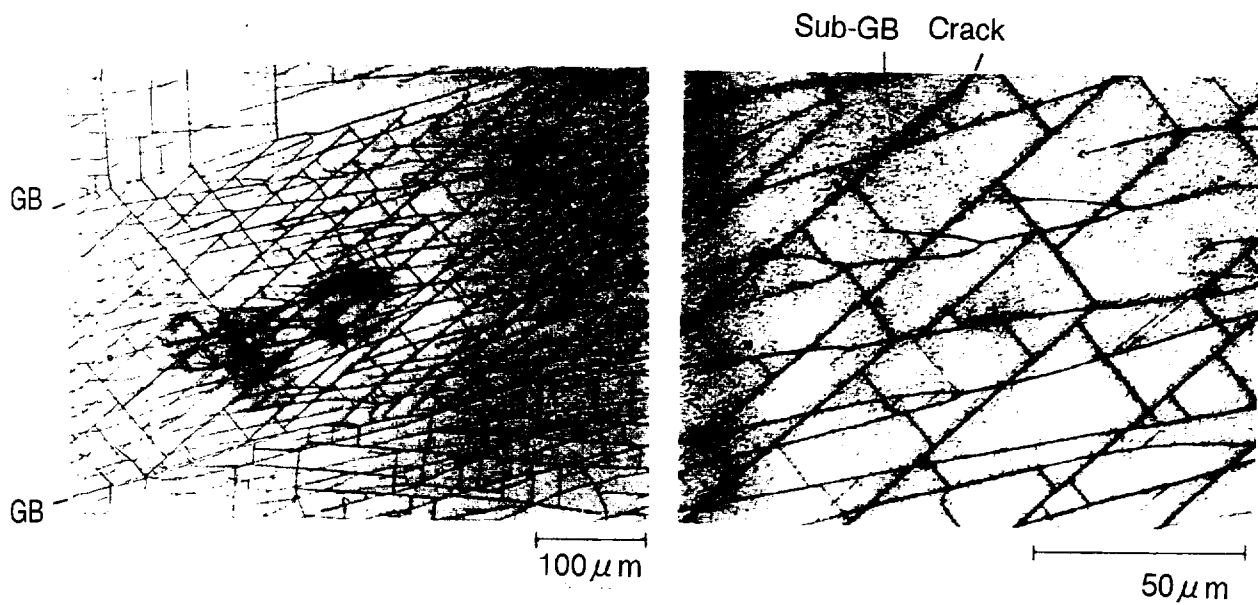
boundaries. The solidification front was not straight as shown in Fig.4.8 (b) [15]. Therefore, there were facet tops or an uneven solidification front. And sub-grain boundaries (small-angle grain boundaries) appeared behind the liquid-solid interface (the highest temperature front). The sub-grain boundaries were almost all parallel to the recrystallization direction. New sub-grain boundaries occasionally appeared when continuous solidification was interrupted by chance and two boundaries met in the lower reaches. It would be reasonable to eliminate the sub-grain boundaries, but they do not have a serious influence on device characteristics as shown later. The sub-grain boundary-free SOI was realized by controlling the growth front as shown in Fig.4.8 (c) [16].

Fig. 4.9 illustrates the etch pit shapes for films with different crystal orientation. (a) indicates a square pit enclosed by four (111) slopes on (100) surface. In alkaline etching, the etching rate of (111) is the lowest and etching automatically stops when the four (111) slopes are completed. (b) shows a example etch pit on a surface inclined from (100), such as (111). Hexagonal pit is surrounded by six (111) surfaces. From these considerations, crystal quality (orientation) of a large area was evaluated by the etch pit method.

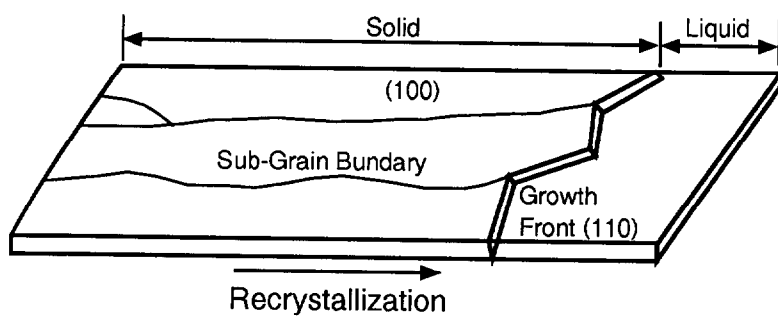
(4) Evaluation of microstructure by TEM and EBD

Fig. 4.10 shows a typical TEM micrograph and EBD pattern of the SOI island center area. (a) is the TEM micrograph of a cross section of SOI film perpendicular to the recrystallization direction. Crystal defects such as dislocations or grain boundaries were not observed on either the front surface or the bottom areas. Therefore the film was a single crystal. A broad hillock (arrow) was observed on the left side of the front surface. This should be a surface wrinkle flowing in the recrystallization direction. (b) is the EBD pattern for the same area as (a). The clear spot pattern showed that the cross section was a single crystal and had a {110} plane, and that the upper surface of the film was the {100} plane. These results confirmed that the SOI film was a high quality single crystal with (100) surface and without macro-defects such as dislocations and grain boundaries.

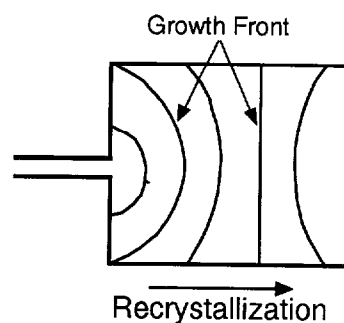
Fig. 4.11 shows a less common TEM micrograph and EBD pattern of SOI film with a grain boundary. (a) is the TEM micrograph of a cross section of SOI film perpendicular to the recrystallization direction. The grain boundary was almost perpendicular to the substrate surface implying that the boundary had the {110} plane. (b) is the EBD pattern for the same area as shown in (a). From the diffraction pattern, it was concluded that the cross section was basically (110) plane. But the diffraction spots were slightly split. The two diffraction patterns came from the two planes on both sides of the grain boundary. The orientation lag of the two planes was estimated from the (222) spots (arrows) to be about 2°. Therefore, the grain boundary was a small-angle grain boundary as reported previously [12].



(a) Cracks and sub-grain boundaries after Sirtle etching.

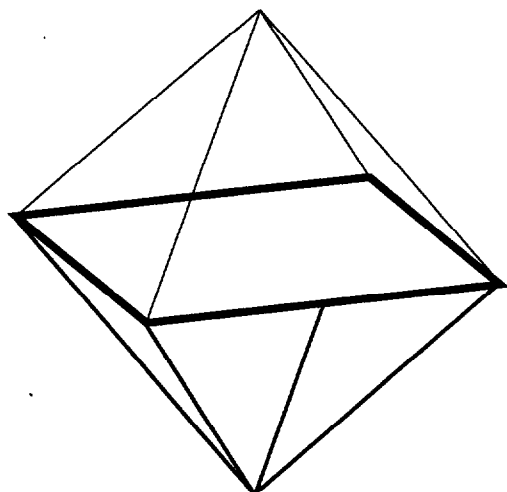


(b) Generation mechanism of sub-grain boundaries [15]

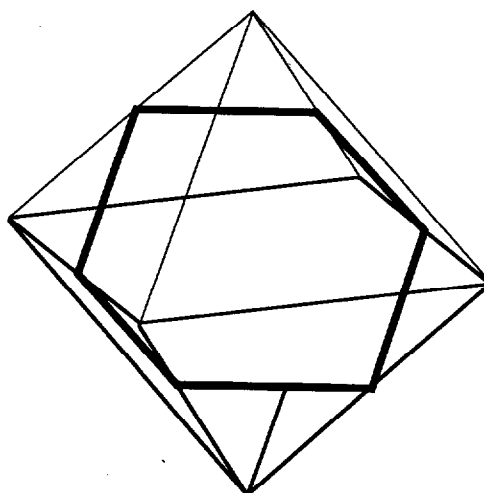


(c) Control of generation of sub-grains [16]

Fig. 4.8. Crystal growth mechanism in zone-melting recrystallization.



(a) Surface (100)



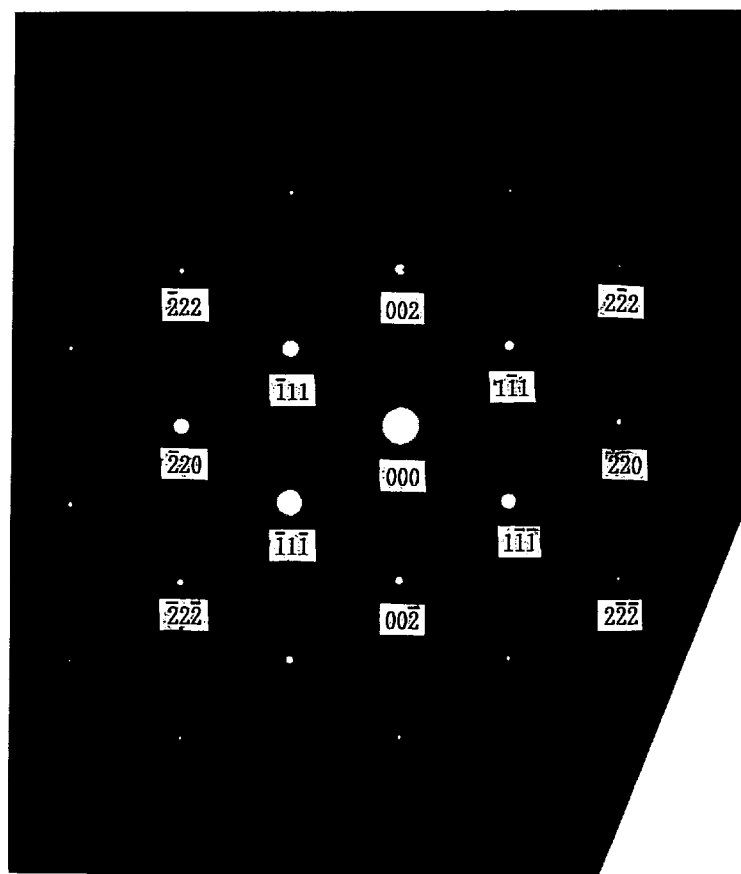
(b) Surface inclined from (100)

Fig. 4.9. Models of etch pit shapes in anisotropic etching of Si films.



(a) TEM

500nm



(b) EBD

Fig. 4.10. TEM micrograph and EBD pattern of the SOI island center area.

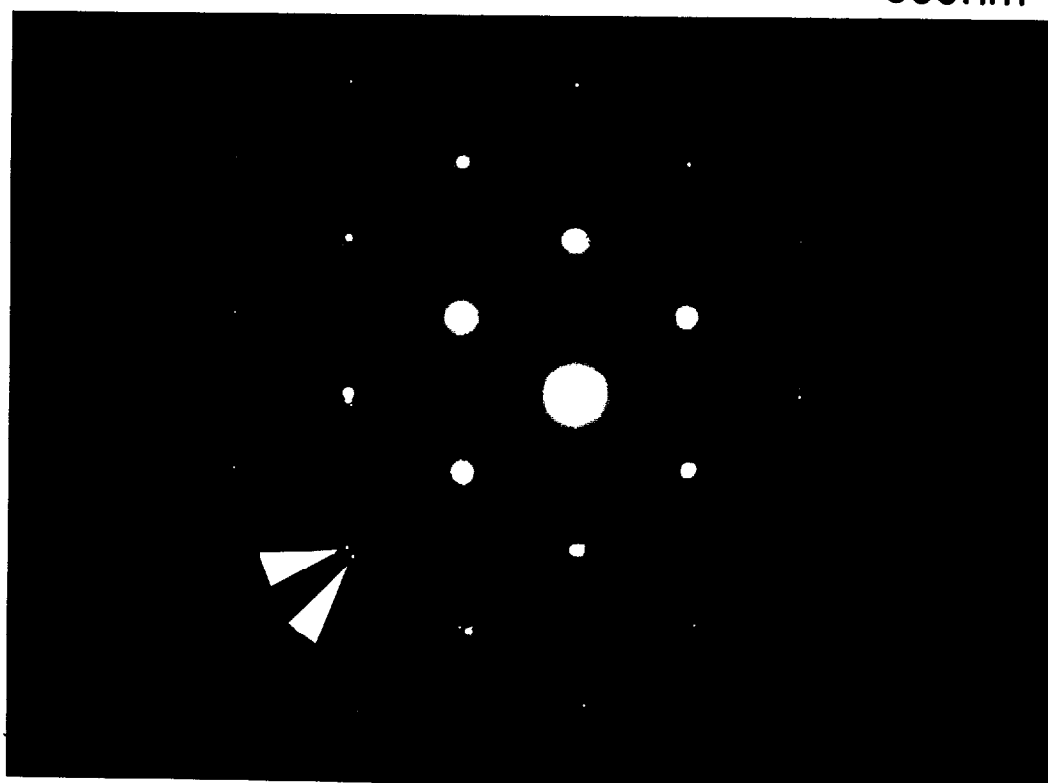
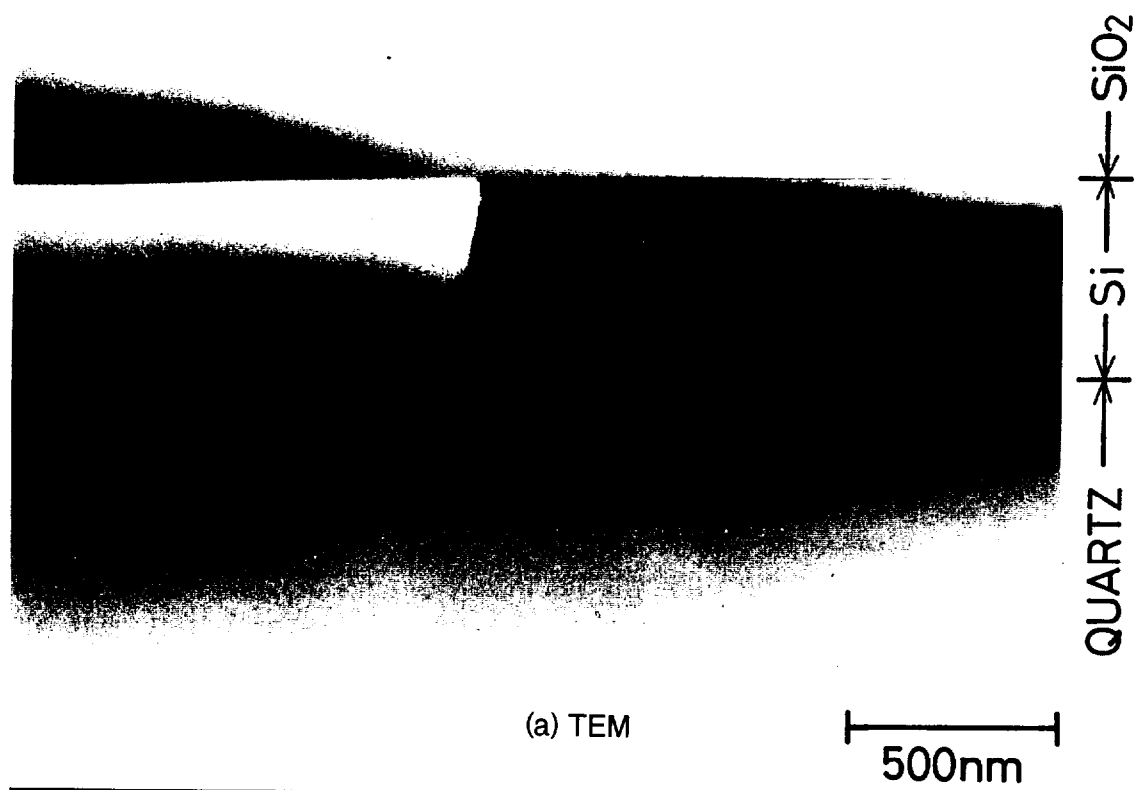


Fig. 4.11. TEM micrograph and EBD pattern of SOI film which contained a small-angle grain boundary.

Fig. 4.12 is a TEM micrograph of a cross section of SOI film around the edge region. The poly-Si film was dry etched to make islands and had a tapered edge as inset. But after recrystallization, the edge was rounded and the taper angle was roughly estimated to be about 60° . Therefore, it was assumed that the edge plane was between $\{111\}$ and $\{110\}$, which had Θ of 55° and 45° , respectively. All regions of the film, i.e. edge, surface, and bottom were also single crystal and had no macro-defects such as grain boundaries and dislocations.

Fig. 4.13 is a schematic of the SOI film structure with a normal (100) surface region and an abnormal orientation region after anisotropic etching. In the normal region, the surface was (100) and the etch pit was a square with four (111) surface slopes. Small-angle grain boundary was also observed, but lag of the angle of the two grains was less than 2° and therefore the area was almost single crystal. When continuous ZMR was interrupted, there was a different crystal orientation from the (100) surface. In this area, the etch pit became hexagonal. The angle Θ was 54.74° from crystallographic theory. The angle Θ' of SOI film edge was estimated as about 60° from the TEM observation in Fig. 4.12.

4.3 Characteristics of SOI TFTs

4.3.1 Al-gate SOI TFTs

(1) Fabrication of Al-gate SOI TFTs

To evaluate SOI crystallinity, Al-gate TFTs were fabricated. Fig. 4.14 shows the fundamental fabrication process for the Al-gate n-channel SOI-TFTs. After recrystallization, the cap SiO_2 was removed. Then, SiO_2 (300 nm thick) was deposited again. Using this SiO_2 layer as an island etching and diffusion mask, the connector region was etched out and high concentration boron was diffused into the edge region from BN substrates at 950°C to suppress the side channel (parasitic device) ((b)). To compare TFT characteristics, different TFTs using silicon islands with as-grown edge and without edge boron diffusion were fabricated (Fig. 4.15). After mask SiO_2 was removed, B^+ ions were deeply implanted at a dose of 3×10^{12} at 180 keV to suppress back channel formation ((c)). To form the source and drain regions, phosphorous was diffused at 900°C for 10 min, masking the channel region with the SiO_2 ((d)). The mask SiO_2 layer was removed and the gate oxide (120 nm) was formed by thermal oxidation at 1000°C . After opening windows for contact, an AlSi layer (800 nm) was sputtered to form the source, gate and drain electrodes.

(2) Characteristics of n-channel SOI TFTs

Fig. 4.15 illustrates the planar pattern and gate region cross section of TFTs. (a) shows a conventional TFT (type A) which was fabricated in the center of the island and had a p^+ layer at the edge and bottom to suppress side and back channels (Figs. 4.14 (b), (c)). Fig. 4.15(b) shows a TFT

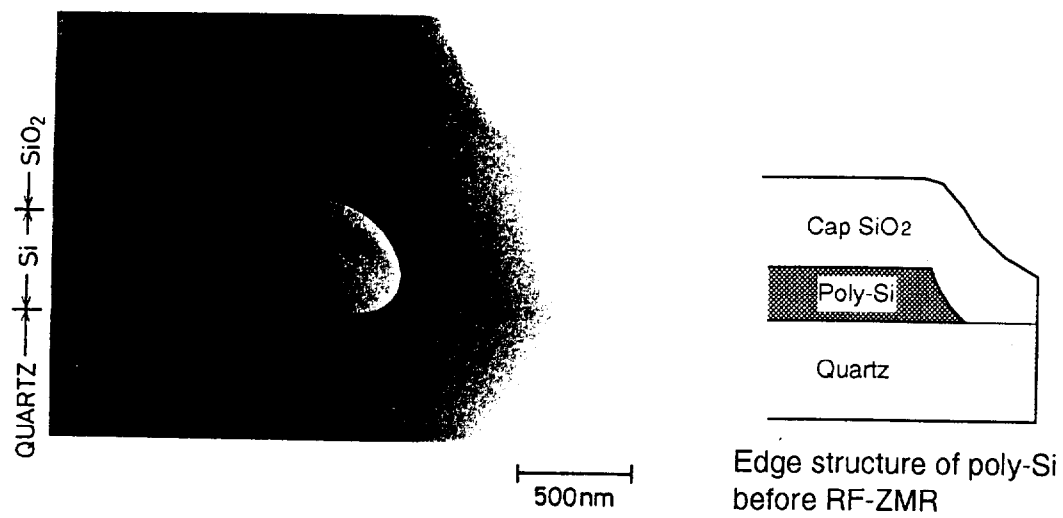


Fig. 4.12. TEM micrograph of edge region of SOI film.

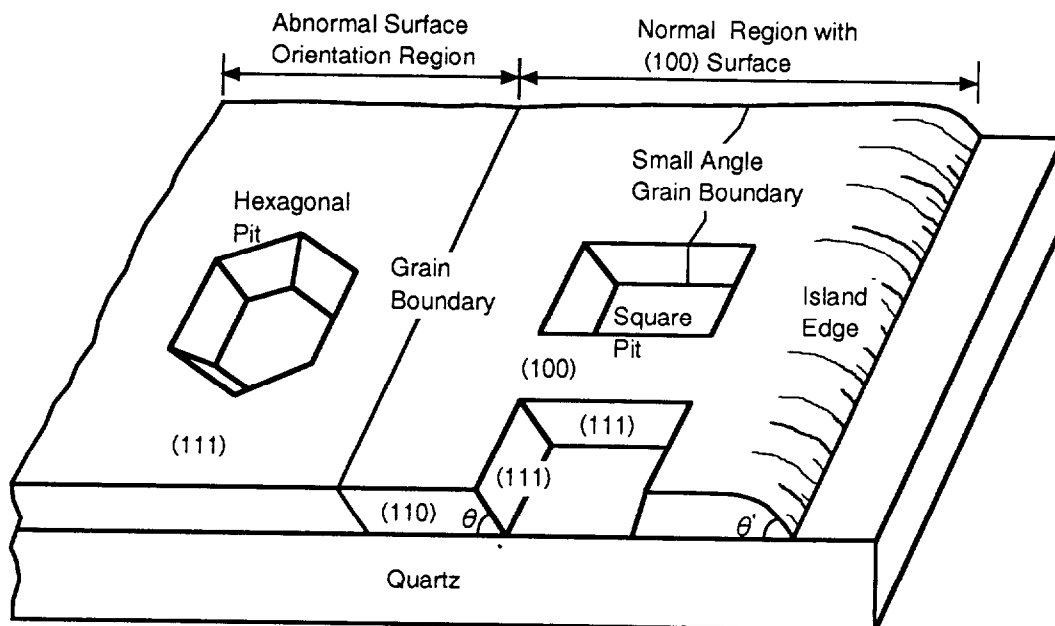


Fig. 4.13. Schematic structure of SOI film with normal (100) surface region and abnormal orientation region after anisotropic etching.

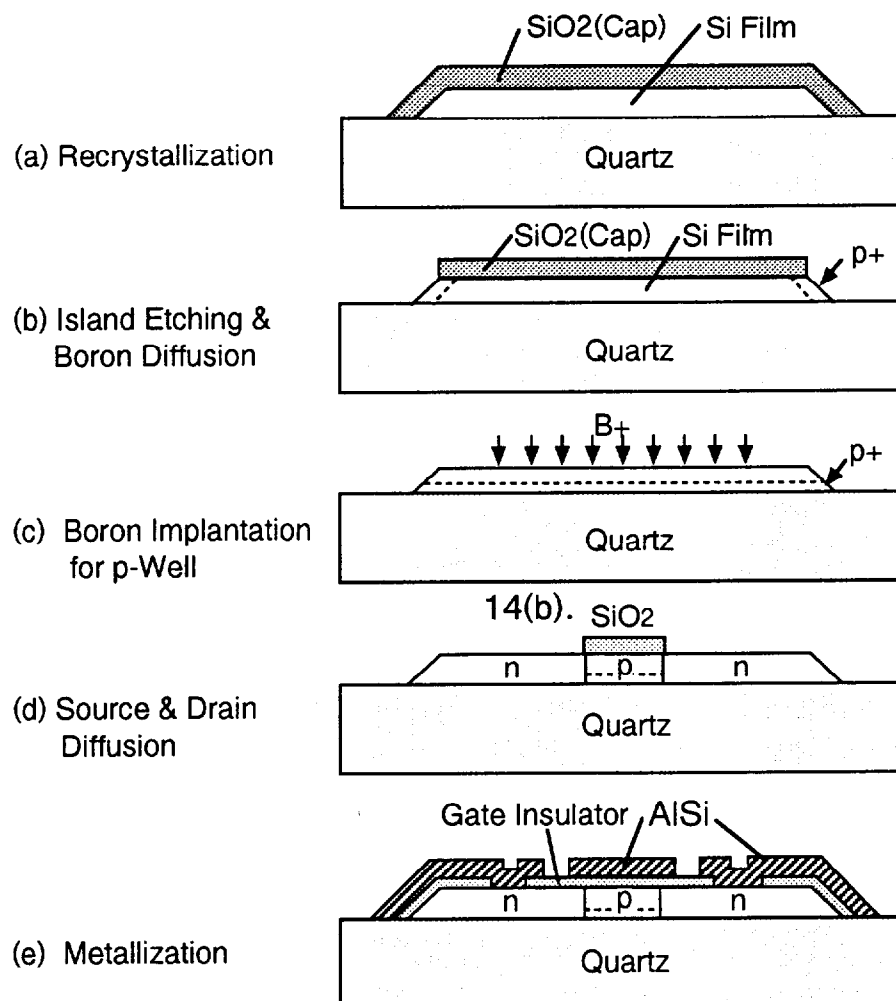


Fig. 4.14. Fabrication process for Al-gate SOI TFT.

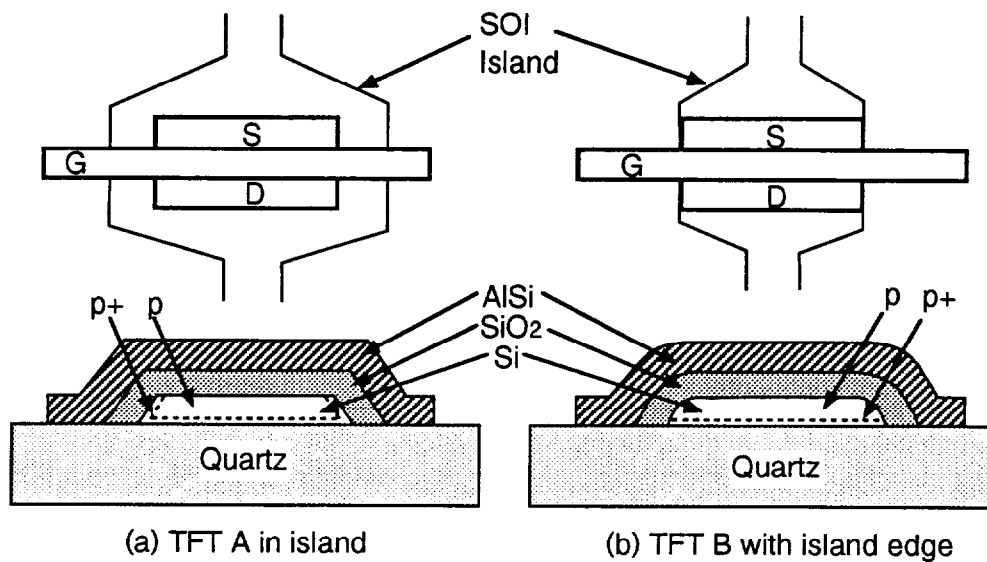


Fig. 4.15. n-Channel TFTs in SOI island and with island edge.

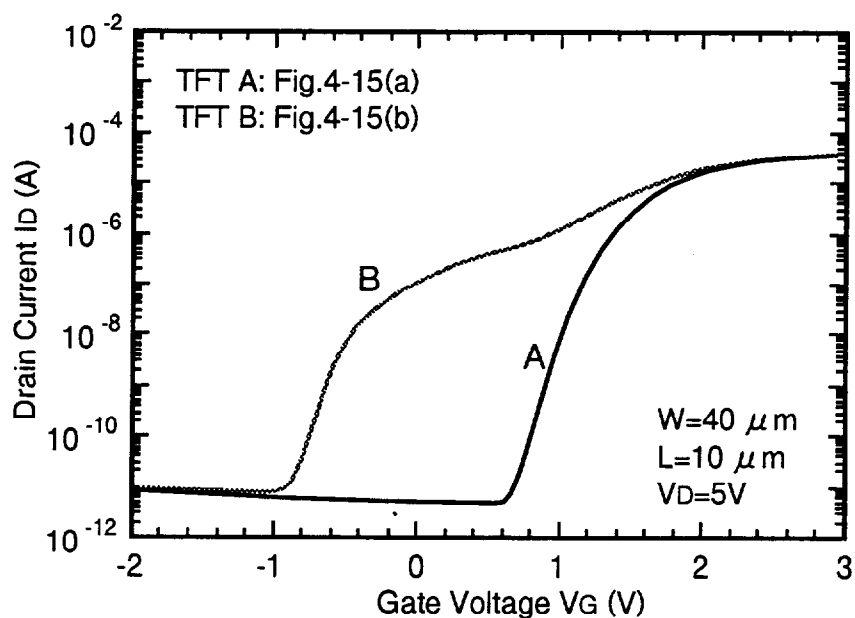


Fig. 4.16. VG-ID characteristics of TFTs in SOI island and with island edge.

(type B) with as-grown edge and without p⁺ layer in the edge region. These TFTs were fabricated on two islands connected by a line by the same process, except for the edge boron diffusion step.

Fig. 4.16 plots gate voltage-drain current characteristics of n-channel SOI TFTs. TFT A had normal and good characteristics, $V_{TH}=1.5V$, $\mu_{FE}=600 \text{ cm}^2/V.s$, $I_{ON}=5 \times 10^{-5}A$, $I_{OFF}=1 \times 10^{-11}A$. Low voltage (3-5V) drive may be possible. The field-effect mobility of SOI with (100) surface on quartz is larger than that of bulk device because large tensile stress for (100) surface reduces the effective electron mass [12]. The drain current of TFT B with the as-crystallized edge was raised in two steps. The back channel was suppressed the same as TFT A. So the first rise of drain current at a gate voltage of about -0.5V was caused by a parasitic device at the island edge. The second step rise was due to the main channel on (100) surface. The threshold voltage $V_{TH(A)}=1.0V$ of TFT A was that of the main surface channel and the $V_{TH(B)}=-0.5V$ of TFT B was that of the side channel. Therefore, threshold voltage shift $\Delta V_{TH}=V_{TH(A)}-V_{TH(B)}=1.5V$ should correspond to the difference of crystal quality (surface charge density) between the edge region and surface (100). Generally, V_{TH} is shown as the following equation [17].

$$V_{TH} = \sqrt{\frac{4qN_A\Phi_F\epsilon_{Si}}{\epsilon_0(\epsilon_{OX})^2}} \cdot X_{OX} + 2\Phi_F + \Phi_{MS} - \frac{Q}{C_{OX}} \text{ -----(4-1)}$$

N_A : acceptor concentration
 Φ_F : Fermi potential
 ϵ_{Si} : dielectric constant of Si
 ϵ_0 : dielectric constant of vacuum
 ϵ_{OX} : dielectric constant of oxide
 X_{OX} : thickness of oxide
 Φ_{MS} : work function of metal
 Q : net charge density
 C_{OX} : capacitance of oxide

The first and second terms depend on acceptor concentration. The third and fourth terms are related to gate material and net charge density, respectively. The first, second and third terms are the same for both TFTs because they were fabricated by the same process conditions. Therefore,

$$\Delta V_{TH} = \Delta Q/C_{OX} = 1.5V. \text{ -----(4-2)}$$

The Q of the (100) plane is generally small compared to that of the (111) or (110) planes. Thus, the estimated net charge density for the edge surface was $3.3 \times 10^{11} \text{ cm}^{-2}$. This value was the same as the net charge density of the surface between (111) and (110) of the single crystal [18], [19]. This result also confirmed the crystal model shown in Fig.4.13.

Therefore, the edge region also had good crystal quality comparable to that of single crystal.

4.3.2 Poly-Si gate SOI TFTs

(1) Fabrication of poly-Si gate SOI TFTs

Fig.4.17 shows the fabrication process for SOI TFTs and Table 4.1 summarizes the condition specifications which were based on the 3 μm LSI process. After recrystallization, the cap SiO_2 layer was removed. Then, using the conventional p-channel process, the TFT was made. Finally, ITO was deposited by sputtering to a thickness of 100 nm for a transparent electrode. An n-channel TFT was also made for reference. Boron ions were implanted for back channel stopping, p-well making, and threshold voltage control with doses of $2 \times 10^{12} \text{ cm}^{-2}$ at 180 keV, $3 \times 10^{11} \text{ cm}^{-2}$ at 40 keV, and $8 \times 10^{11} \text{ cm}^{-2}$ at 45 keV, respectively. The source and drain were made by phosphorous implantation at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ at 70 keV.

(2) Basic characteristics of poly-Si gate SOI TFTs

Fig.4.18 graphs the drain current-gate voltage characteristics of n- and p-channel TFTs. The off-current of each TFT was the same value as the bulk device and less than 1 pA, which was the measurable limit. The on-current of a 3- μm p-channel TFT was slightly lower than the bulk device, but it had an on-off current ratio of 10^8 , which was large enough for matrix TFT use. The n-channel TFT, used for reference, had comparable on-current to the bulk device. The field-effect mobilities of the n-channel TFTs ($L=5 \mu\text{m}$) with the channel direction perpendicular and parallel to the recrystallization direction were 450-900 and 500-1050 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. They would be driven by 5-8V. But they had a parasitic device (side channel) that operated at low positive gate voltage as shown in Fig.4.16. The boron concentration at island edges must be precisely controlled to stop side channel effects. This caused the complicated fabrication process for n-channel TFTs.

(3) Characteristics of p-channel SOI TFTs

Fig. 4.19(a) plots the field-effect mobility dependence on channel length. Values for bulk devices are also presented for reference. The channel direction of the TFTs was either parallel or perpendicular to the recrystallization direction. The mobility of the TFTs was 150-200 $\text{cm}^2/\text{V}\cdot\text{s}$, which was lower than for the bulk devices, but still sufficiently large enough for matrix TFT use. The TFTs that had parallel channels showed slightly higher mobilities than the TFTs that had perpendicular channels. The important result was that the off-current was below 1 pA for all TFTs and did not depend on crystal kind and crystallization direction in the range of 2-20 μm ((b)). The TFT with the minimum channel length of 1.3 μm operated successfully.

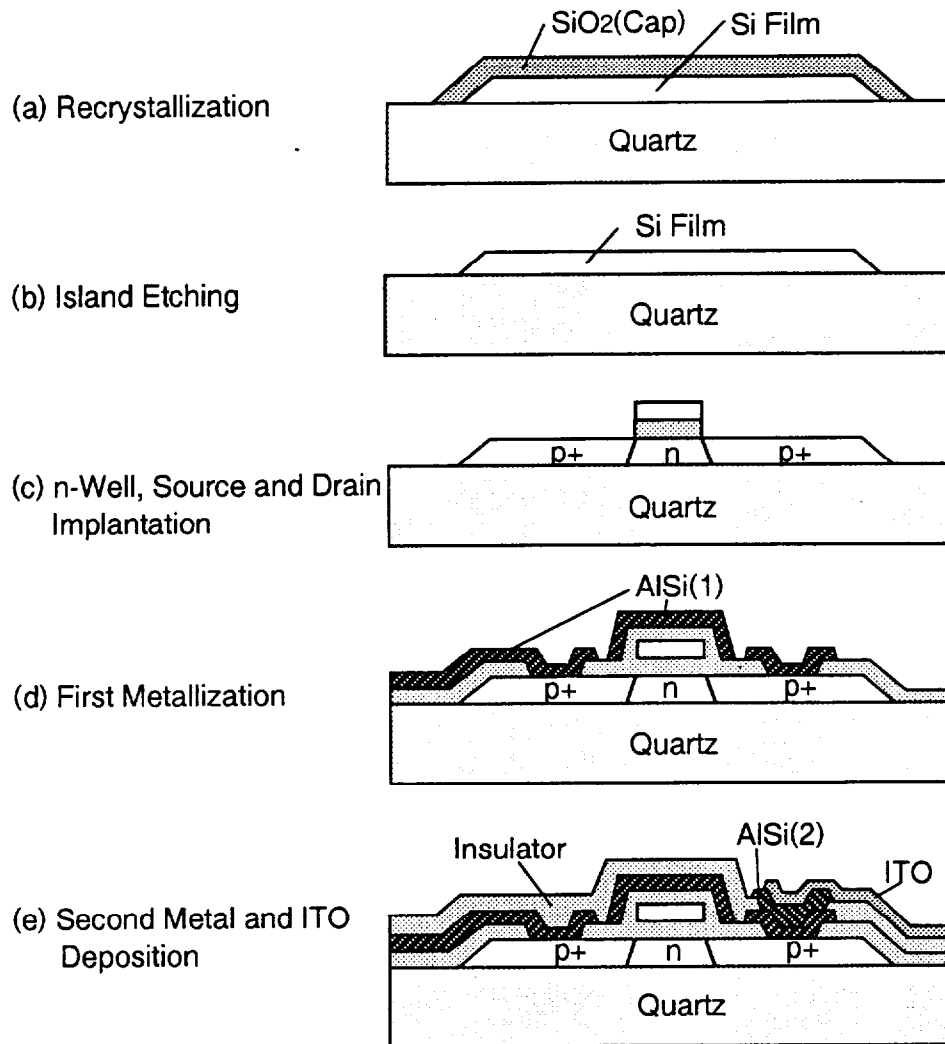


Fig. 4.17. Fabrication process for SOI p-channel TFT for LCD.

Table 4.1 Summary of the process specifications for SOI p-channel TFTs

Substrate : 3" Diameter Fused Quartz
Poly-Si Deposition : 500 nm, 900 °C, SiH ₄ APCVD
Connected Island Patterning : Dry Etching
Cap SiO ₂ Deposition : 740°C, 1.1 μm
Recrystallization : 1450 °C, RF-ZMR
n-Well Implantation : P ⁺ , 1x10 ¹² cm ⁻² , 125keV
n-Well Diffusion : 1000 °C, 4 hr
Island Etching : Dry Etching
Gate Oxidation : 105 nm
Gate Poly-Si Deposition : 350nm
S/D Implantation : B ⁺ , 3x10 ¹⁵ cm ⁻² , 30keV
S/D Diffusion : Furnace Annealing
Metallization(1): AlSi, 800nm
Insulator Deposition: PSG, 600nm
Metallization(2) : AlSi, 300nm
ITO Deposition : 100nm

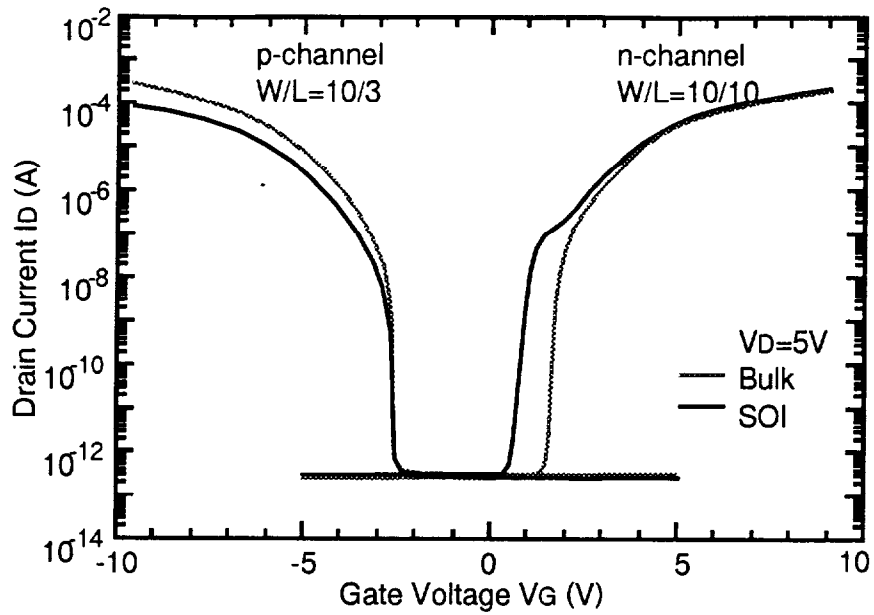


Fig. 4.18. Drain current-gate voltage characteristics of p- and n-channel SOI TFTs.

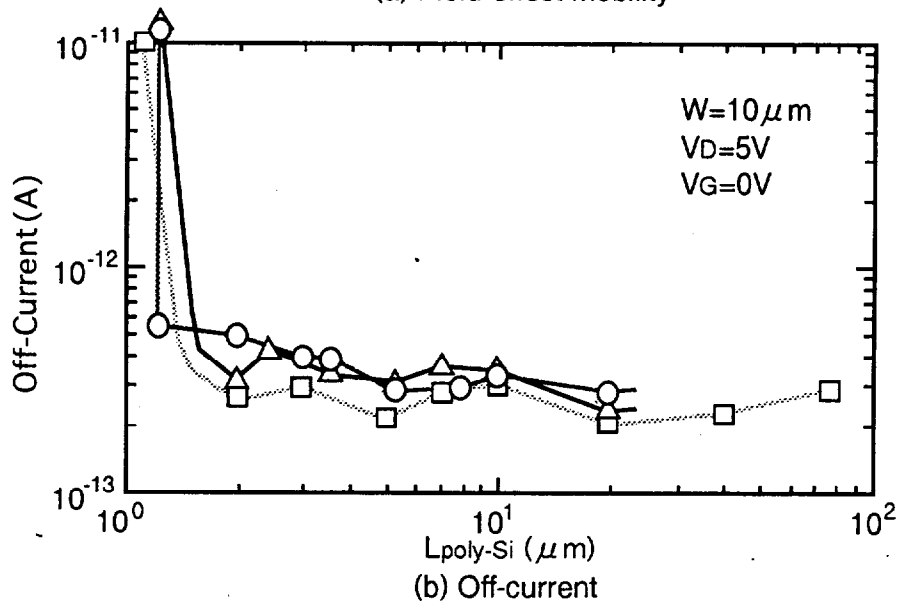
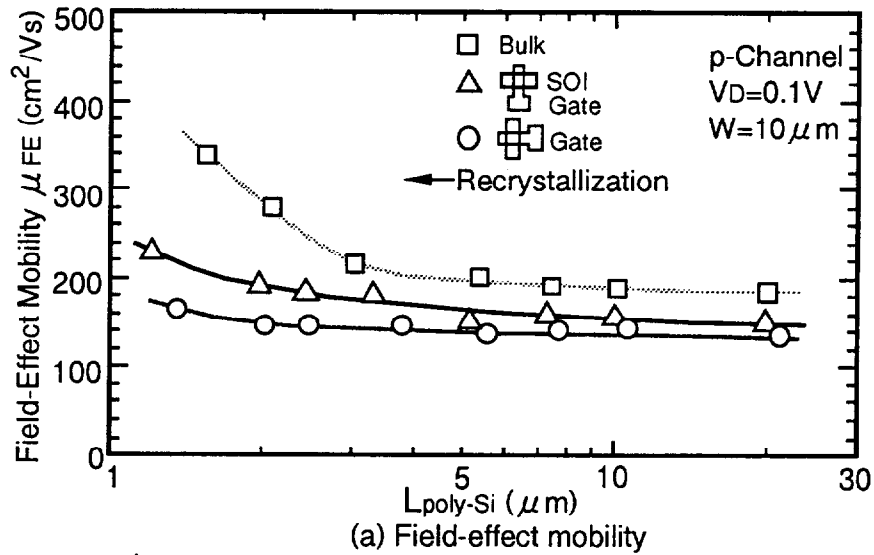


Fig. 4.19. Dependence of TFT characteristics on channel length (gate poly-Si length).

The uniformity of crystallinity in an island and in a connected line was investigated by measuring TFT characteristics. Fig. 4.20 shows the TFT characteristics in an island. Nine TFTs with a channel width and length of 10 and 3 μm , respectively, were fabricated on an island with an area of 100 $\times$ 100 μm^2 . The channel was perpendicular to the recrystallization direction. (a) plots the distribution of the field-effect mobility, which was very sensitive to the silicon layer crystal quality. The values of bulk devices were constant, showing uniformity of the LSI fabrication process and high quality of the bulk silicon. The field-effect mobility of the TFTs showed some irregularity and had a moderate peak in the center (position 5) of the island. This was attributed to a higher crystallinity in the center than the outer area which was caused by a smooth heat flow between the island connectors and solidification from the center to the edges. (b) shows the on-current of TFTs. The values of SOI TFTs were slightly lower than those of bulk devices and slightly higher in the center of the island. (c) plots the off-current. The values of off-current were almost the same for all TFTs and below 1 pA. In this experiment, the TFTs were generally fabricated in the center of the islands as mentioned before. The SOI had sub-grain boundaries, but they had little effect on off-characteristics.

Fig. 4.21 shows the TFT characteristics of TFTs on ten islands connected in a line. The mobility of SOI TFTs was slightly lower than that of bulk devices and the value of TFTs at the lower reaches of solidification showed slightly lower values. This may be caused by the increased number of sub-grain boundaries there. The off-current did not depend on island position.

(4) A consideration for TFT characteristics

From the results previously shown, the effects of quality of grain boundaries on TFT characteristics were considered. Two typical SOIs are the RF-ZMR SOI and CW laser crystallization SOI [4], [10]. The former is the SOI with single crystal or small-angle grain boundaries and the latter contains large-angle or twin grain boundaries. Fig. 4.22 (a) shows schematic V_G - I_D curves of TFTs with the two SOI films. Mobility of RF-ZMR SOI slightly depended on recrystallization direction, but off-current was independent of it (Fig. 4.19) and was almost the same as that of bulk devices (Figs. 4.20, 4.21). But off-current of CW laser crystallized SOI TFTs had a large value and dependence on the recrystallization direction [4], [10]. These two different characteristics were explained as follows. (b) illustrates models of barrier height in grain boundaries. Small-angle grain boundaries had a lower barrier height than the other boundaries, therefore RF-ZMR SOI TFTs had higher mobility than CW laser crystallized SOI TFTs. In both TFTs, mobility increased when the channel was formed parallel to the grain boundaries and carriers were conducted along them. (c) shows the supposed structure of source and drain junctions. In the junction diffusion process, abnormal diffusion occurred

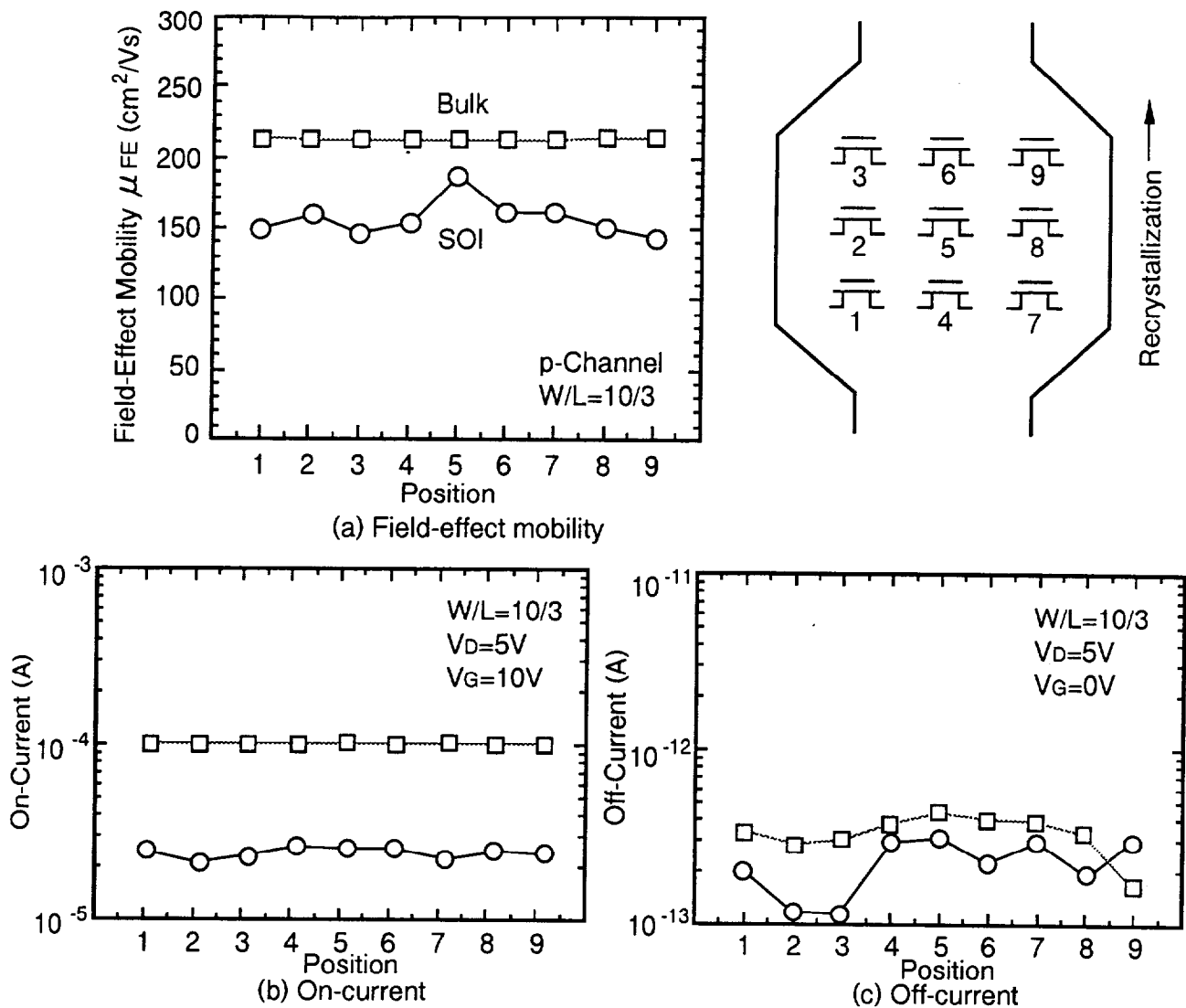


Fig. 4.20. Characteristics of TFTs fabricated on an island.

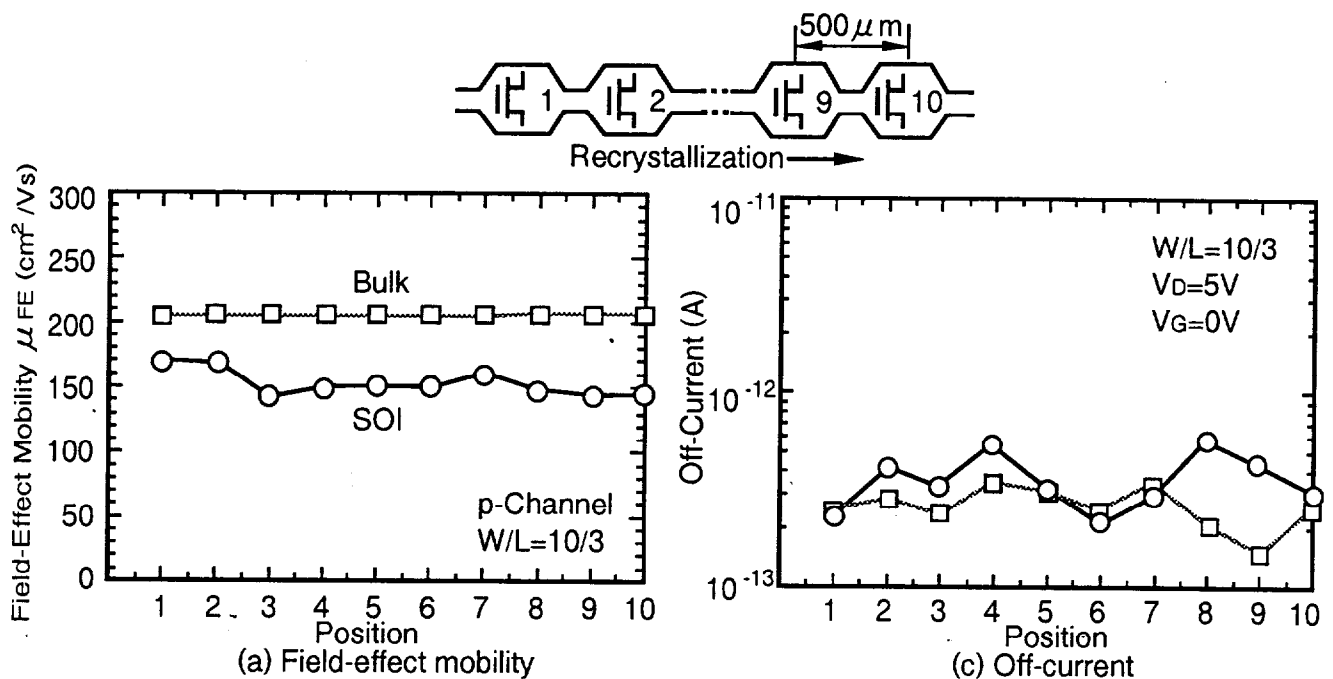


Fig. 4.21. Characteristics of TFTs on islands in a connected line.

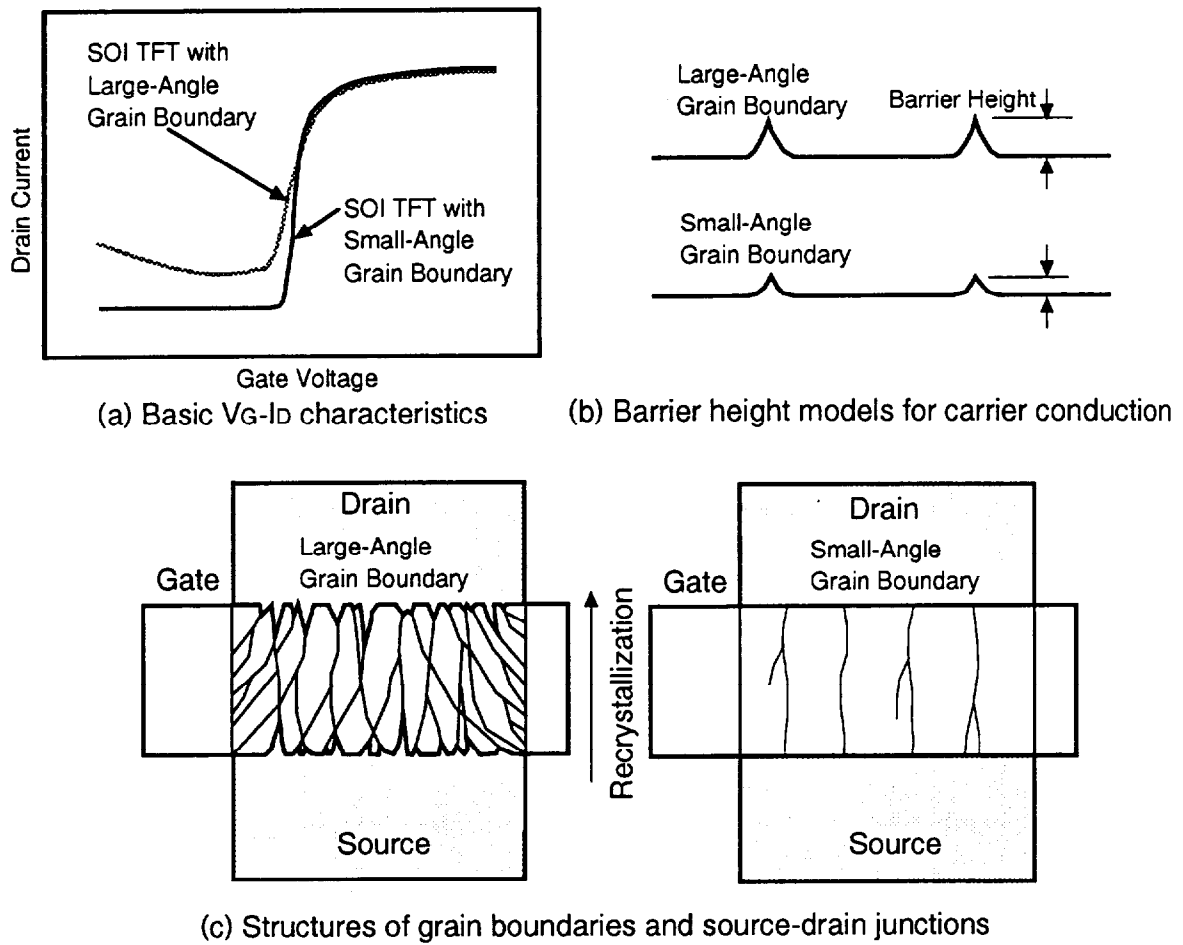


Fig. 4.22. Effects of grain boundaries on TFT characteristics and junction structures.

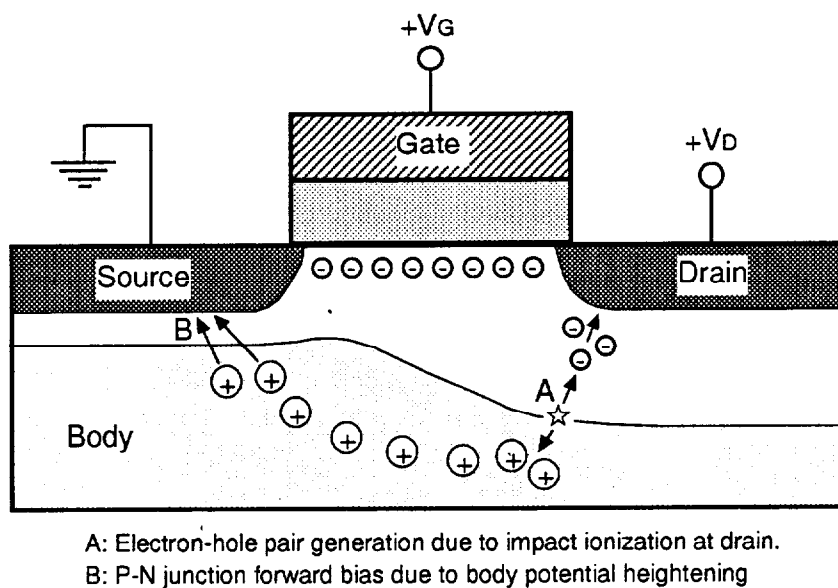


Fig. 4.23. A model for kink effect in high drain field in n-channel TFT [20].

along grain boundaries which had a high density of lattice defects. Also a high off-current was generated at high electric field points, especially in short channel TFTs. In small-angle grain boundaries, junctions were formed normally and leakage current did not depend on recrystallization direction.

One of the drawbacks of SOI TFTs is the kink effect which reduces the source-drain breakdown voltage, especially in n-channel TFTs. Fig.4.23 illustrates the kink effect mechanism in an n-channel TFT [20]. When the drain voltage is increased, a large number of electron-hole pairs is generated in the high-field depletion region. The excessively generated holes are accumulated at the body region to increase body potential. Thus, the parasitic bipolar transistor is turned on and drain current increases anomalously [20]. Practical means proposed to suppress the kink effect are off-set gate [21] and LDD structure [22], and multi-gate [23], [24] to reduce drain electric field. Recently, a new structure TFT with a body terminal (four terminal TFT) was proposed to pull out accumulated holes [25]. But in p-channel SOI TFTs, the kink effect is basically suppressed in hole conduction. Therefore, p-channel TFT matrices and logic circuits are a practical choice which realize a simple fabrication process.

4.4 Application of p-channel SOI TFTs to TFT-LCDs

4.4.1 Characteristics of p-channel TFTs for pixels

Fig. 4.24 is a photograph of a pixel that has a cell size of $80 \times 105 \mu\text{m}^2$. The TFT channel width (W) and channel length (L) were 8 and 15 μm , respectively. An aluminum layer, used as a light shield, was deposited on the poly-Si gate, which was passivated with PSG. The distance from p-n junction to the light shield edge was 10 μm . Both the data line and gate line widths were 4 μm . The crossover was composed of n⁺ poly-Si (gate line)-PSG-aluminum (data line). This pixel had no auxiliary capacitor.

Fig. 4.25 shows the drain voltage-drain current characteristics of pixel TFTs. The breakdown voltage of the source and drain (BV_{DS}) of SOI TFT was about 20 V, which was slightly lower than 30 V of the bulk device. The kink effect was not observed either for the p-channel SOI TFT which had a simple single-drain structure.

Fig. 4.26 shows drain current-gate voltage characteristics of a pixel TFT under illumination and in the dark. In the latter, the TFT had an on-off ratio of 10^8 and threshold voltage of 2.5 V. Illumination was 1200 lx provided by a tungsten lamp from the gate side, and the on-off ratio was reduced to about 10^6 . However this value would be sufficiently large for the present size active matrix. In an actual LCD panel, the off-current should be reduced because the back light is absorbed by a polarizer, liquid crystal layer and alignment layer. The off-current showed hardly any dependence on the size of the light shield (without the aluminum layer and 5-20 μm from the p-n junction edge). These results indicated that the photocurrent (off-current) was mainly induced by the light conducted laterally through the PSG film (600 nm thick) or the quartz substrate and

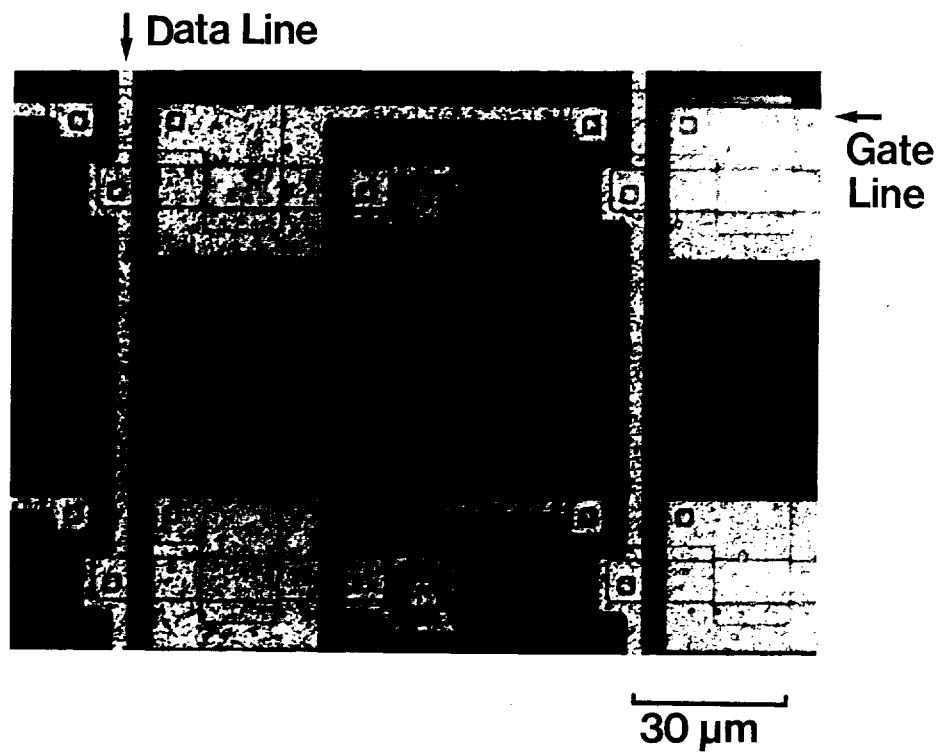


Fig. 4.24. Photograph of pixel ($80\mu\text{m} \times 105\mu\text{m}$).

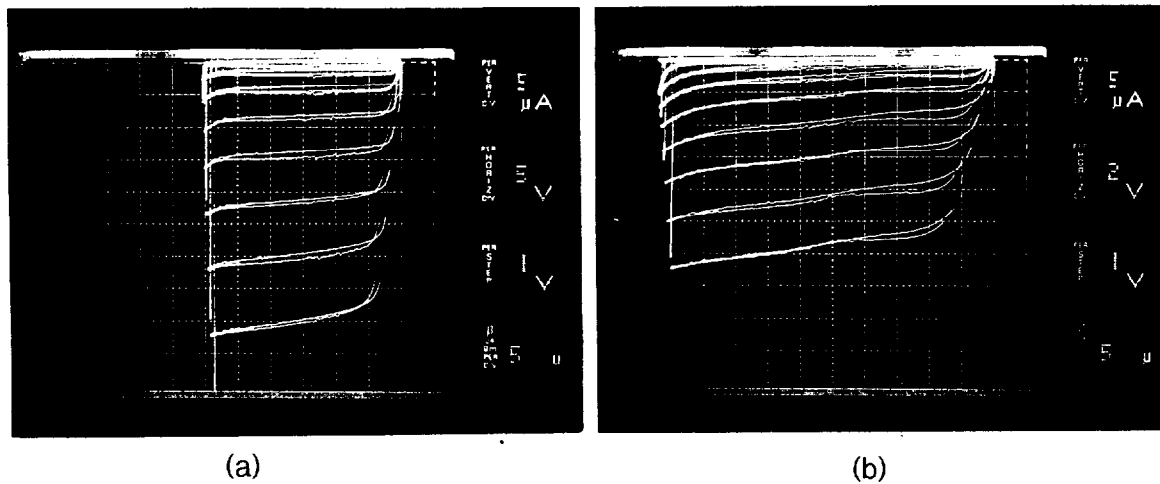


Fig. 4.25. Drain voltage-drain current characteristics of pixel TFTs.
 (a) Bulk Device: Horizontal(V_D): 5V/div. Vertical(I_D): $5\mu\text{A}$
 (b) SOI Device: Horizontal(V_D): 2V/div. Vertical(I_D): $5\mu\text{A}$

by the light reflected from the back surface of the quartz substrate, not by the light that directly illuminated the TFT surface. Considering these facts, the p-channel SOI TFT with a light shield still had light sensitivity which was comparable to that of n-channel SOI TFTs and was higher than that of large-grain [10] and fine-grain [20] poly-Si TFTs, as also shown in section 2.3.4.

Therefore, a trade-off of high crystallinity (high mobility) and low off-current (low-photocurrent) would be very important for matrix TFT uses such as projection-type LCDs with very strong back light.

Table 4.2 summarizes the characteristics of the pixel TFTs. The drain-source breakdown voltage BV_{DS} , gate-source breakdown voltage BV_{GS} , and gate line-data line breakdown voltage BV_{CROSS} are also important characteristics to consider for active matrices using TFTs. These values were 20, 45, and 80 V, respectively, sufficiently large enough for active matrix use.

Fig.4.27 reproduces two photographs of display images. Alphanumeric and graphic images were displayed on the SOI TFT-LCD panel that had a $17.6 \times 23.31 \text{ mm}^2$ (1.15") active area and 220×222 pixels. The size of each pixel was $80 \times 105 \text{ } \mu\text{m}^2$ and the aperture ratio, i.e., the ratio of the effective area to total cell area, was 63 %. An auxiliary capacitor to assist in holding the applied voltage on the liquid-crystal layer was not fabricated.

These displays were transmissive mode, illuminated by back light (1000 lx) from a fluorescent lamp. The liquid crystal layer was the TN type. A line-at-a time addressing scheme with a duty ratio of 1/220 was used. Scanning pulses with amplitudes of -15V were applied to the gate electrodes, and data pulses with amplitudes of 5V, for which the polarity was reversed in each frame, were applied to the source electrodes. The frame frequency was 50Hz. Under these drive conditions, a good contrast ratio of 20:1 was achieved. This showed that the off-resistance of the SOI TFT could be kept high enough under illumination, and a sufficient on-off voltage ratio for the liquid-crystal layer could be obtained.

4.4.2 Characteristics of logic circuits with p-channel TFTs

Table 4.3 summarizes the p-channel logic circuit operation characteristics. The ring oscillator and shift resistor were composed of E-E type inverters fabricated by the same process as the matrix TFTs. The 21-stage ring oscillator was operated at a delay time of 13 ns per stage ($V_{DD} = -30\text{V}$), which was compatible to the value of the bulk devices.

Fig. 4.28 shows the operational characteristics of the shift resistor. The two-phase clock dynamic shift resistor operated at 200 Hz-100 kHz with a practical output voltage. Its operation speed was comparable to that of bulk devices, though its mobility was 20-30 % lower than them as shown in Fig. 4.18. This excellent operation reflected the effect of the SOI structure to reduce parasitic capacitance in metallization lines. For this size active matrix, the horizontal driver must operate at 2.9 MHz. So

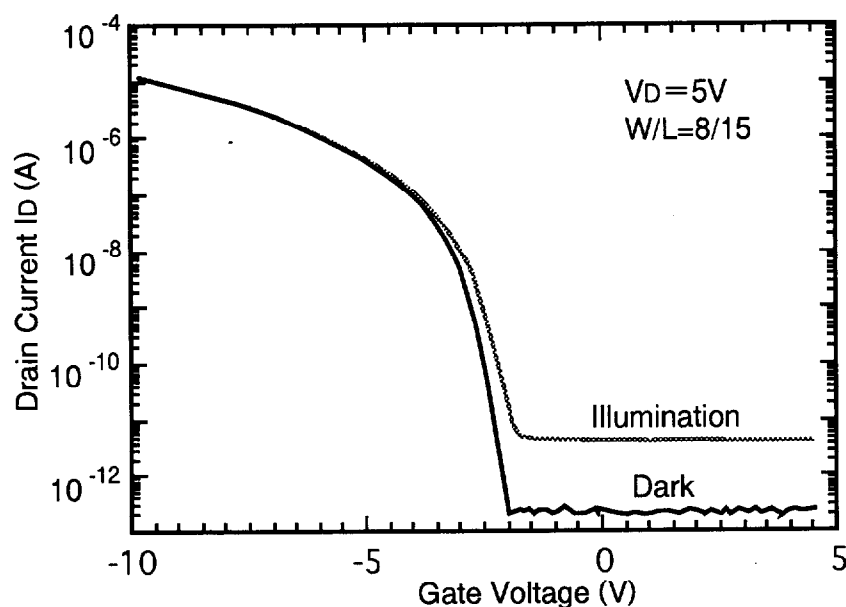


Fig. 4.26. Drain current-gate voltage characteristics of pixel TFT under illumination (1200 lx) and in the dark.

Table 4.2 Summary of the characteristics of the pixel TFTs

Channel Length	15 μm
Channel Width	8 μm
Gate Oxide Thickness	105 nm
Light Shield Thickness (AlSi)	800 nm
I_{ON} ($V_{\text{G}}=10\text{V}$, $V_{\text{D}}=5\text{V}$)	50 μA
I_{OFF} ($V_{\text{G}}=0\text{V}$, $V_{\text{D}}=5\text{V}$)	
Dark	0.5 pA
Illumination(1200 lx)	5 pA
$I_{\text{ON}}/I_{\text{OFF}}$ Ratio(1200 lx)	10^6
Threshold Voltage	2.5V
Field-Effect Mobility	170 cm^2/Vs
BV_{DS} (Drain-Source)	20V
BV_{GS} (Gate-Source)	45V
BV_{CROSS} (Gate Line-Drain Line)	80V

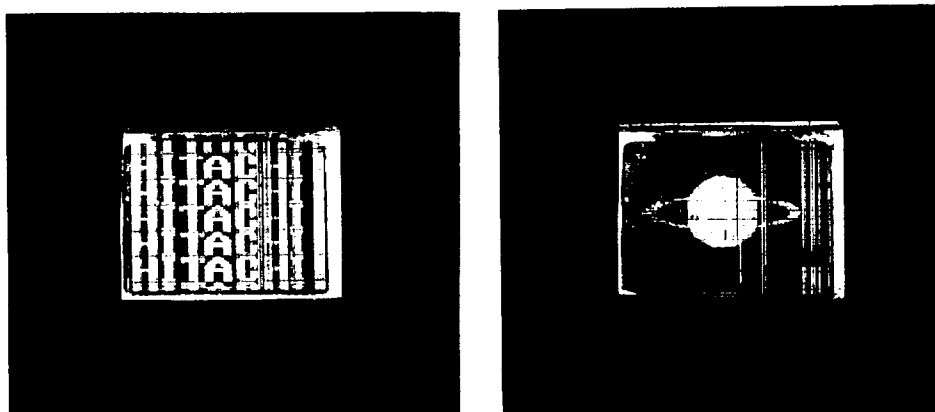
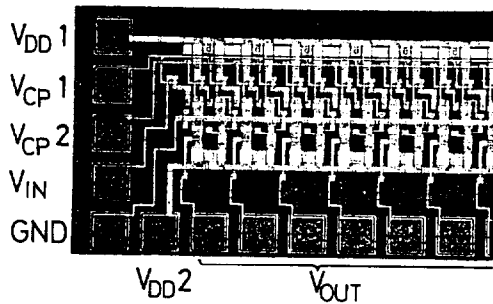


Fig. 4.27. Example display images of p-channel SOI TFT-LCD.

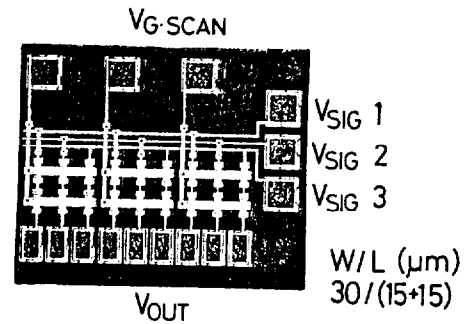
Table 4.3 Summary of operation characteristics of p-channel SOI TFT logic circuits

Circuit	Structure	Operating Conditions	Operating Speed
Ring Oscillator	E-E Type, 21 Stages Driver MOS: W/L=50/10 Load MOS TFT: W/L=30/60	$V_{DD}=-30V$	13 ns/stage (12 ns/stage)
Shift Resister	E-E 6 MOSFET, 10 Stages 2-Phase Clock, Dynamic Type Driver:W/L=50/5 Load: W/L=40/40	$V_{DD}=-14V$ $V_G=-10V$	100 kHz (100 kHz)
Switch Matrix Type Driver	3-Phase Signal Type W/L=30/15x2	$V_G=-10V$ $V_{IN}=10V$	1 MHz

(Bulk Device)



2-Phase Clock Dynamic Shift Register



Divided Switch Matrix

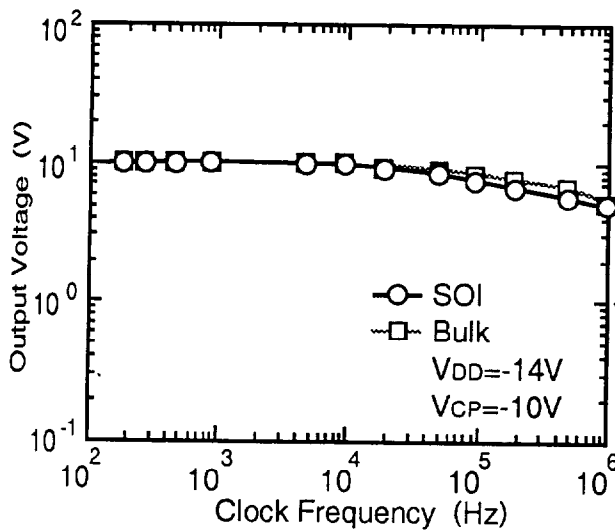


Fig. 4.28. Operation characteristics of 2-phase clock dynamic shift register.

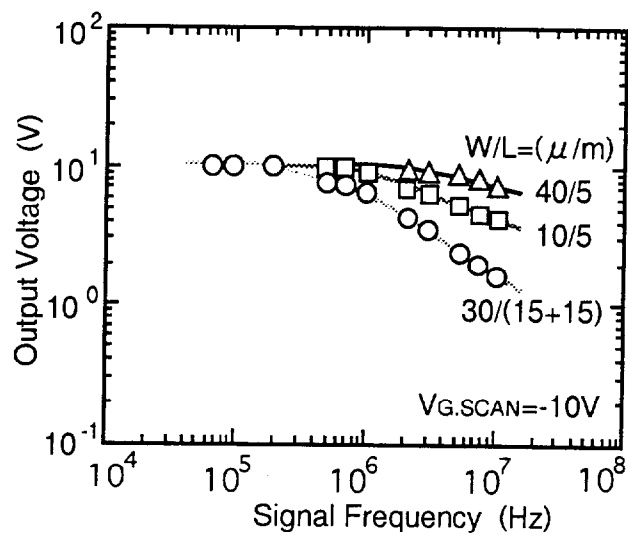


Fig. 4.29. Operation characteristics of the 3-phase signal divided switch matrix-type driver.

this operating speed of the shift resistor was insufficient for the horizontal driver, but sufficient for the vertical one which must operate at 24 kHz.

Fig. 4.29 shows the operational characteristics of the divided switch matrix, whose speed depends only on the speed of the discrete TFTs. Using a three-phase signal clock, the scanning speed of the horizontal driver was reduced to 980 kHz. The three-phase signal divided switch matrix-type driver was operated at 1 MHz ($L=30\mu\text{m}$) to 10 MHz ($L=5\mu\text{m}$) successfully. This circuit was applicable to the horizontal driver using only p-channel TFTs.

In this section, only p-channel TFTs were used for matrices and logic circuits to simplify the fabrication process. But considering demands for increased operation speed and decreased power consumption, short channel CMOS configuration should be reasonable [6].

4.5 SOI TFTs with directly contacted ITO

4.5.1 LCD and ITO contact structure

The SOI TFTs have high driving ability corresponding to that of bulk devices and it should be possible to achieve a very fine active matrix using integrated monolithic driver circuits as mentioned in the previous section.

The LCD panels which are typically used in consumer products require a simple fabrication process to achieve good cost performance. In the active matrix, transparent electrodes of ITO are used. In the previous section (Figs. 4.17, 4.24) underlayer Al was used to make contact with ITO. Thus it seems reasonable to use ITO for metallization material as in the poly-Si TFT matrix [23]. In this technique, it is necessary to ensure direct contact of ITO with the SOI TFT. In this section, direct contact of ITO on the n^+ source area of SOI TFTs was considered to simplify the pixel fabrication process.

4.5.2 Fabrication of Al-gate n-channel SOI TFTs

Fig. 4.30 shows the fabrication process of Al-gate n-channel SOI TFTs. RF-ZMR discussed in section 4.2 was used for SOI preparation ((a)). After recrystallization, the connector region was removed and the Si islands were separated ((b)). To make the p-well and suppress the back channel leakage current, B^+ ions were implanted in a dose of $3 \times 10^{12} \text{ cm}^{-2}$ at 180 keV ((c)). To form the source and drain, phosphorous was diffused at 900°C for 10 min, masking the channel region with SiO_2 . The mask layer was removed and the gate oxide (120-nm thick) was formed by thermal oxidation at 1000°C . An aluminum layer (800-nm thick) was sputtered to form the data line and gate. In this structure, the gate metal acted as a light shield layer ((d)). An insulator of phospho-silicate glass (PSG, 600-nm thick) was deposited by CVD and ITO (500-nm thick, Sn: 5 %) was deposited directly on the source region by sputtering. The resistivity of ITO was $7 \times 10^{-4} \Omega\cdot\text{cm}$. Then ITO was patterned by two methods. In the conventional wet-etching method using HBr at 45°C , heat-

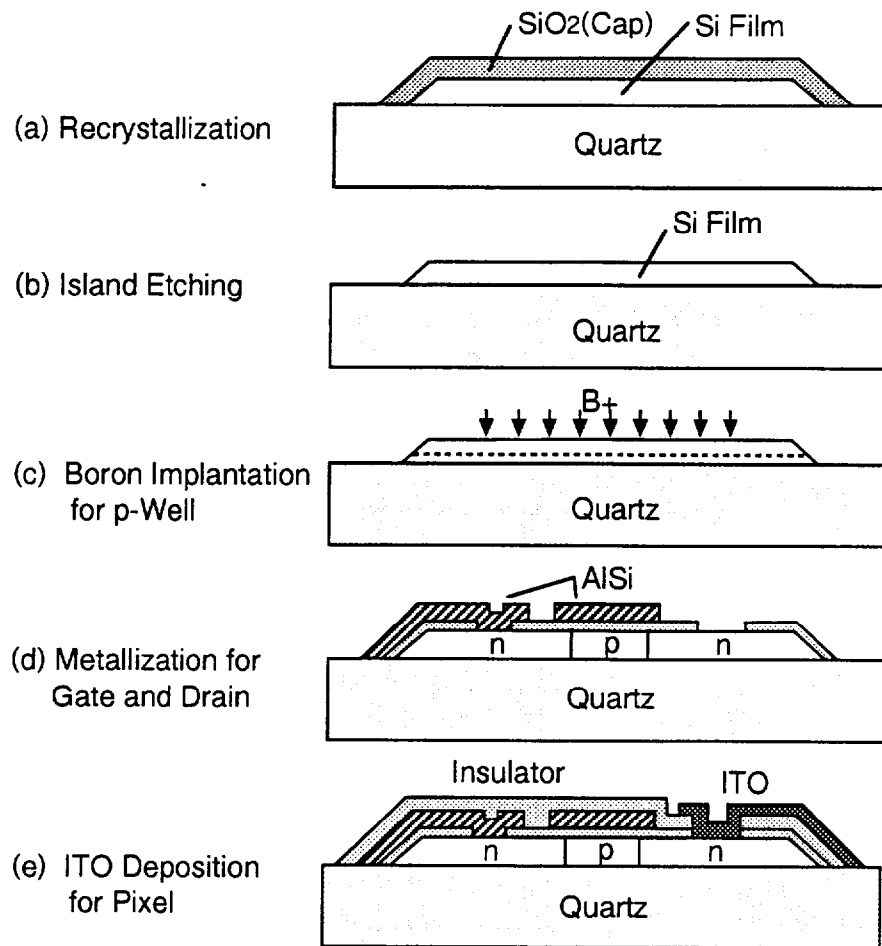


Fig. 4.30. Fabrication process for Al-gate n-channel SOI TFT for pixel with ITO direct contact.

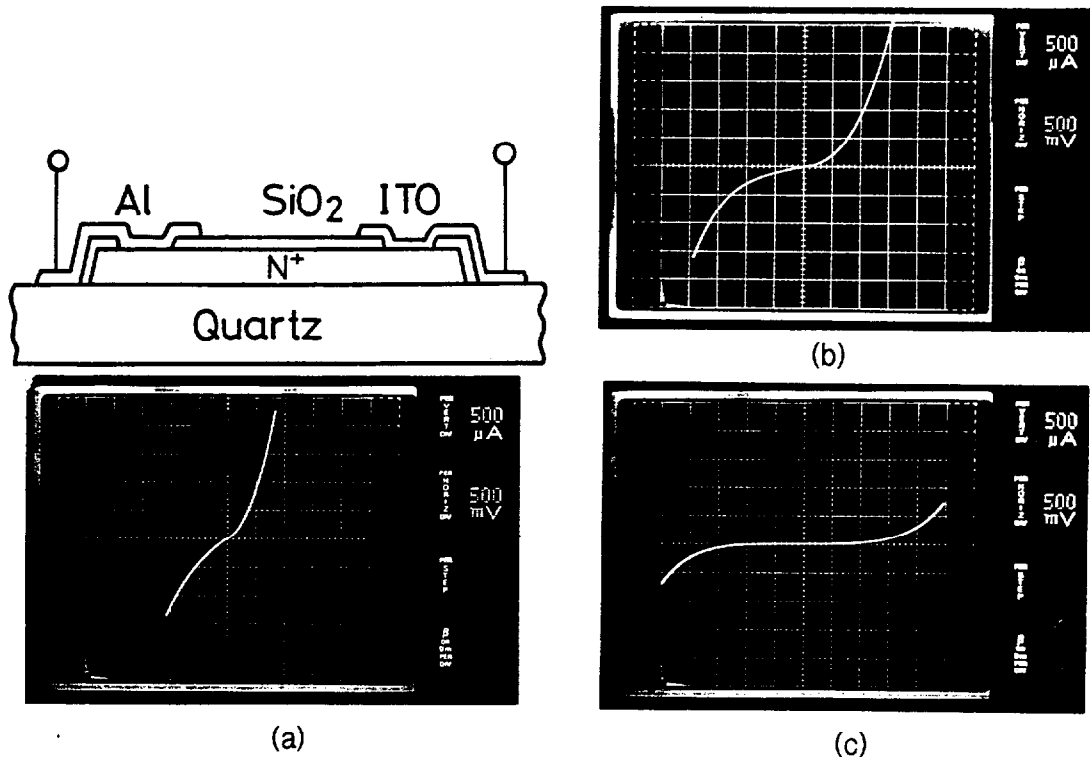


Fig.4.31. The dependence of annealing conditions on the conduction characteristics of ITO and n⁺ silicon. (a) 200°C, 30 min. (b) 400°C, 30 min. (c) 600°C, 30 min in N₂. At 1st and 3rd quadrants, ITO was positively and negatively biased, respectively. The contact area was 20 x 60 μm².

treatment (400°C, 30min) before etching was necessary to improve adhesion between ITO and PSG for accurate patterning. The other was the lift-off method. The positive type photoresist (1.2 μm thick) was patterned and ITO was sputtered without substrate heating. In the sputtering process, the resist was crumpled by self-heating from the plasma energy. The crumpling assisted the later lift-off process of ITO in an acetone wash by ultrasonic waves ((e)).

4.5.3 ITO contact characteristics

Fig. 4.31 shows the conduction characteristics of ITO and n^+ SOI. The characteristics were investigated using the test device schematically illustrated. The aluminum was metallized on the n^+ Si layer to make a complete ohmic contact as the opposite side electrode. The ITO was deposited and patterned by the lift-off method. Then, heat-treatment was used. (a) shows the practical conduction characteristics after a 30-min annealing at 200 °C which is necessary for resist baking to assist in the ITO lift-off. The waveform was not symmetrical and had a slight dependence on polarity of conduction. The contact barrier increased as the annealing temperature was raised. (b) shows the characteristics after conventional 400°C annealing. Finally, (c) indicates that higher temperature 600°C annealing increased the barrier drastically.

It was assumed that the most probable cause of the contact barrier formation on the heat treatment was the thin silicon oxide layer formed by excess oxygen in the ITO [26] and the oxygen from sputtering plasma, because the resistivity of the ITO itself was not changed by annealing in the range of 200-600°C in N_2 . The interface was investigated by a model experiment using electron spectroscopy for chemical analysis (ESCA). A thin ITO (10nm) film was deposited on single crystal silicon with a (100) surface and annealed at 500°C for 30 min in N_2 . The binding energies of electrons in Si and In were measured while sputtering the substrate surface with an Ar^+ ion beam.

Fig. 4.32 plots the binding energy dependence on the sputter etching time. The binding energy for In was hardly dependent on heat treatment which meant that In existed only as In_2O_3 . The binding energy for Si on the substrate as-deposited ((a)) depended slightly on etching time and increased from 100.6 to 101.0 eV, while the value for Si on the annealed substrate in (b) clearly depended on etching time and decreased from 101.6 to 100.9 eV. The results indicated that heat treatment had a critical influence on binding energy in Si. Considering that the binding energies of electrons in Si-Si and Si-O (SiO_2) bonds are 101 and 103 eV, respectively, and that the value of annealed substrate was increased to 101.6 eV, it was reasonable to assume that a thin silicon oxide layer (SiO_x) was formed by heat-treatment which created the barrier.

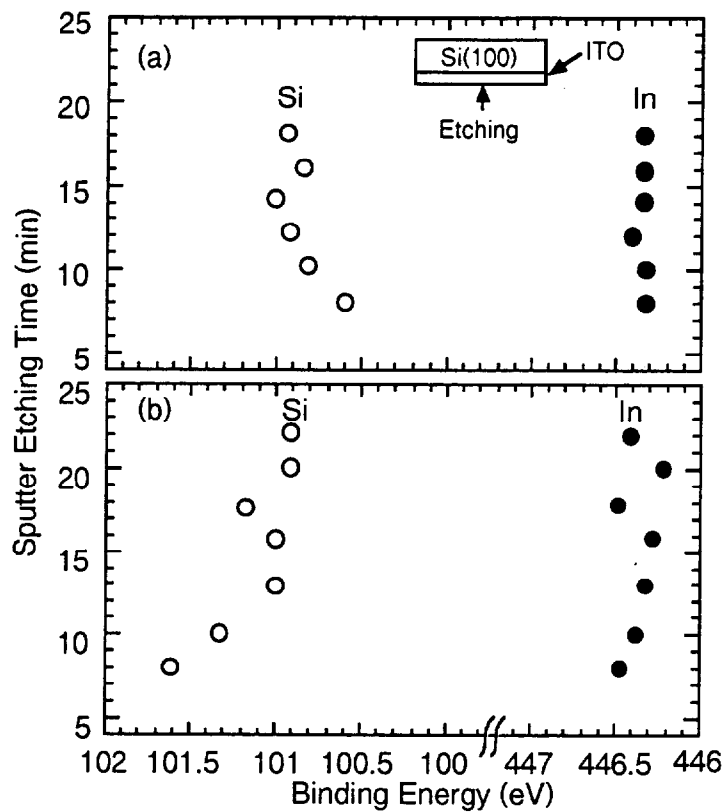


Fig. 4.32. Electron binding energies in Si and In: dependence on sputter etching time of the ITO deposited on Si (100). (a) As-deposited ITO. (b) After annealing at 500°C for 30 min in N₂.

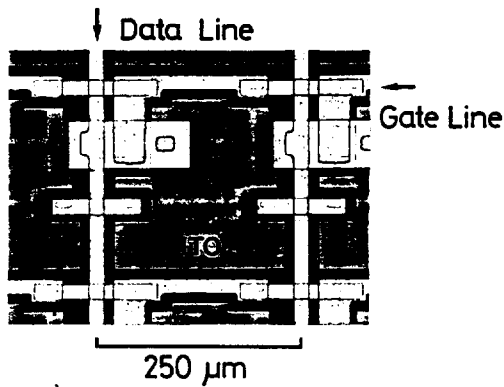


Fig. 4.33. Photograph of pixel.

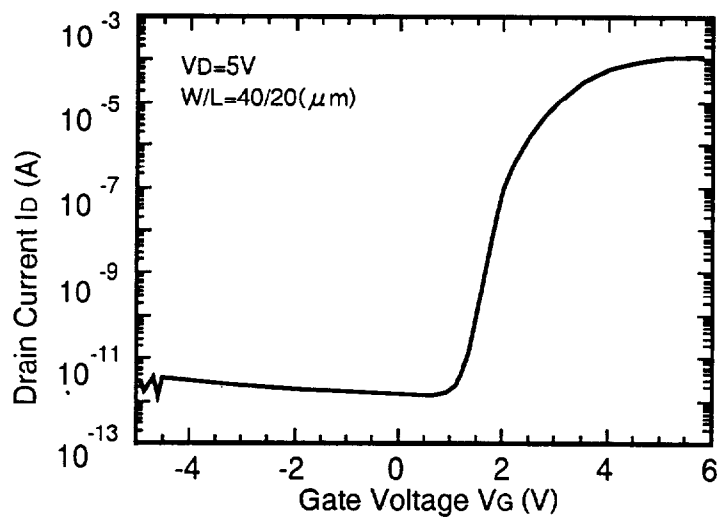


Fig. 4.34. V_G - I_D characteristics of a n-channel Al gate SOI TFT with ITO direct contact for pixel of Fig. 4.33.

4.5.4 Characteristics of pixel TFTs with direct contact ITO

To avoid formation of a contact barrier, the low-temperature ITO lift-off method (200°C process) was applied to fabricate a small scale (40x40 elements) active matrix. Fig. 4.33 shows the fabricated pixel. The channel length and width of the TFT were 20 and 40 μm , respectively. The data line was composed of aluminum and the crossover was composed of n^+ SOI (gate line)- SiO_2 (gate oxide)-aluminum (data line). The ITO of the pixel electrode made direct contact with the n^+ source of the TFT.

Fig. 4.34 shows typical V_D - I_D characteristics of the pixel TFT. The leakage current, on-off current ratio, and threshold voltage at a drain-source voltage of 5V, were 3 pA, 10^8 , and 2V, respectively. It would be driven by 3-5V. These values confirmed that the ITO had good contact on n^+ Si and a high performance TFT could be realized. These results also showed the possible application of ITO to data line material which is used in direct contact with the n^+ drain region of SOI TFTs.

4.6 Conclusions

To realize high quality SOI on quartz substrates, RF-ZMR was introduced. A large and long area was successfully recrystallized by using the connected island method. Large area crystallinity was inspected by thermal oxidation, wrinkle observation, and conventional etch pit methods. Micro-structure was inspected by TEM and EBD. The silicon layer had high quality with small-angle grain boundaries, and the ratio of the (100) surface was 95 %.

Al-gate TFTs were fabricated to investigate crystal quality and direct contact of ITO to SOI TFTs.

Ultimate high-performance n-channel TFTs (SOI TFTs : c- TFTs) are obtained which had field-effect mobility of 500-1000 $\text{cm}^2/\text{V}\cdot\text{s}$ and would be driven by 3-5V. But they also had parasitic devices. To simplify the fabrication process, a p-channel poly-Si gate SOI TFT was adopted to realize a high-resolution active matrix for a LCD for the first time. The TFT was fabricated by applying poly-Si gate 3 μm LSI process. The TFT had a field-effect mobility of 150-200 $\text{cm}^2/\text{V}\cdot\text{s}$, which was a little lower than that of a bulk device, and had a threshold voltage of 2.5 V. Sub-grain boundary direction had slight effect on field-effect mobility but did not affect off-current. The TFT also had a high on-off ratio of 10^6 under illumination though leakage current increased. Using these TFTs, an active matrix chip that had a 17.6 x 23.31 mm^2 (1.15") active area and 220 x 222 pixels, each 80 x 105 μm^2 , was fabricated, and a monochrome transmissive display with good contrast was achieved.

A fundamental p-channel E-E type ring oscillator and a two-phase clock dynamic shift resistor were operated at 13 ns per stage and 200Hz to 100kHz, respectively, which was the same speed as the bulk devices. A divided switch matrix-type driver was operated at 1-10MHz, suitable for use as a horizontal driver.

These results showed that the SOI TFTs (c-TFTs) had comparable characteristics to that of bulk devices to be driven by 3-5V. And it was also indicated that the possibility of high-resolution active-matrix-type LCDs with a monolithically integrated driver using only p-channel SOI TFTs made by a simple fabrication process.

4.7 References

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Large-Area Low-Temperature Poly-Si TFTs by Laser Crystallization

In this chapter, large area laser crystallization is studied as the second technique for melt and regrowth. Excimer laser crystallization of LPCVD Si by two-step energy irradiation at elevated temperature is introduced to achieve uniform crystallization on 350mm X 450mm glass substrates. Large-area ion doping and laser activation (Chapter 6) are also introduced. The crystallinity of poly-Si films and characteristics of TFTs are investigated. Using these TFTs, the world's largest 18.2" poly-Si TFT-LCD is fabricated for the first time to confirm the possibility of large-area low-temperature poly-Si TFTs.

5.1 Introduction

5.1.1 Laser crystallization to reduce thermal load for substrates

As one of the melt and regrowth processes, zone-melting recrystallization achieved very high-quality SOI. But both Si film and substrate were heated to the melting point of Si (1412°C), therefore, the use of quartz substrates was indispensable. To realize the melt and regrowth process on glass, thermal load for the substrate must be reduced. A promising method for this is excimer laser crystallization to heat and melt only Si films on the substrates. Fig. 5.1 classifies energy beam crystallization methods. These techniques started with research on SOIs for application to three dimensional LSIs. An electron beam [1], [2] or CW laser beam such as Ar laser [3], [4] were used. To control Si film orientation, seeding from (100) substrate was also introduced [5]. But electron beam operation was limited to a vacuum. To avoid thermal damage of substrates, these methods need high-speed beam scanning which limits crystallization of random positions though some successful results have been reported [6], [7]. Recently, an excimer laser (KrF), which was commonly used for the LSI stepper light source, was applied to crystallization. The short-duration (a few tens of nanoseconds) pulse and short-wave (ultra-violet) laser beam is absorbed almost completely in the thin poly-Si film, so only the poly-Si film on the substrate is heated and melted. Both KrF and XeCl have been used for laser crystallization.

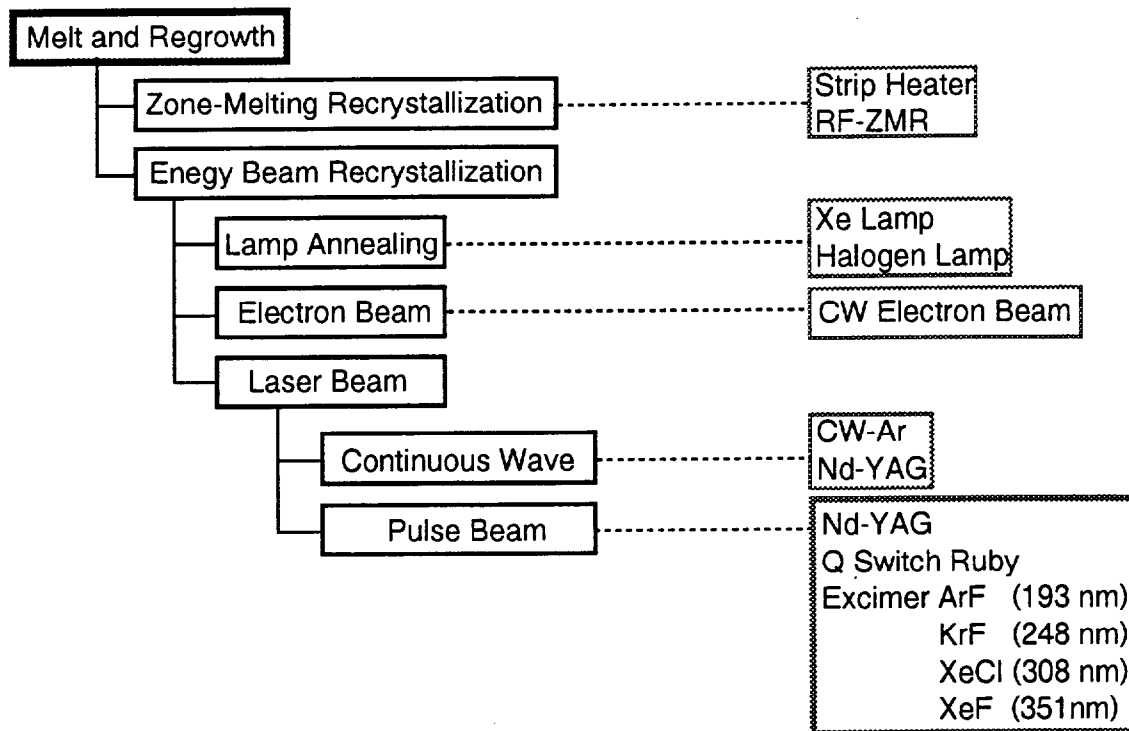


Fig. 5.1. Classification of recrystallization methods by melt and regrowth processes.

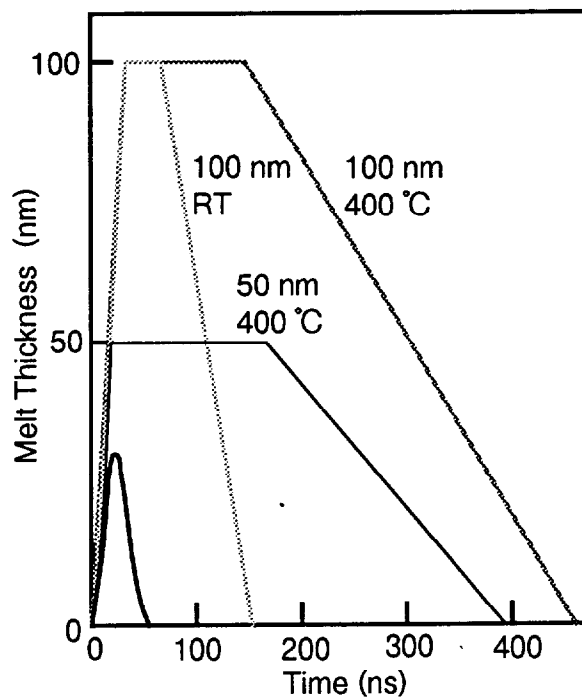


Fig. 5.2. Effect of the substrate temperature on solidification speed. After Kuriyama et al. [20].

But the latter was developed for high power generation. In this study, the XeCl excimer laser was used for large area crystallization.

5.1.2 Excimer laser crystallization for LPCVD Si

A large number of studies have been reported for excimer laser crystallization [8]-[19]. Recently, Kuriyama and co-workers [20], [21] proposed substrate heating and optimized the laser process conditions for PECVD Si films to make large grains.

Fig. 5.2 shows the effect of substrate temperature on the solidification velocity. With substrate heating at 400°C for 50 nm thick film, solidification velocity was reduced to 1/5 of the value of 100 nm film at room temperature [20]. Fig.5.3 shows the effect of underlayer SiO₂ thickness on the glass surface temperature. The interface temperature was suppressed below the strain points of the glass substrate (610°C) when underlayer SiO₂ thickness was 1.0-1.5 μm [21].

In the large-area crystallization, laser beam scanning is indispensable. The problem of excimer laser crystallization has been uniformity of crystal quality in the boundary area of the beam spots. Kuriyama et al. [20] were able to improve crystal uniformity in the beam boundary region and increase grain size remarkably. In this study, excimer laser technology was introduced to achieve large area uniform crystallization for LPCVD Si films.

5.2 Large-area laser crystallization for LPCVD a-Si films

5.2.1 Laser crystallization method

Fig. 5.4 is a schematic of laser irradiation apparatus for crystallization and activation. Two types of laser sources were used. The high power source with power of 150 W, irradiation frequency of 300 Hz and duration of 45 μs was used typically for crystallization. The low power source with power of 38W, irradiation frequency of 80 Hz and duration of 28 μs, was used for activation as shown in Chapter 6. The strength of laser light was controlled by the attenuator and scanned in the X-direction by scanning a set of a mirror and a homogenizer. Reflected light was homogenized by fly-eye lenses and irradiated through the quartz window onto the glass substrates set on the heater in the vacuum chamber. The heater was scanned in the Y direction and thus the whole area of 350mm x 450mm was irradiated.

Fig. 5.5 shows typical laser beam scanning methods for crystallization and activation. The crystallization was carried out by heating the substrate at 350°C. First, low-energy 0.2 mm fine pitch irradiation was applied for dehydrogenation. Then, high-energy 6 mm pitch irradiation was applied for final crystallization. Additionally, fine pitch irradiation [8] was tried for the final crystallization. With activation, fine pitch irradiation with low energy was used.

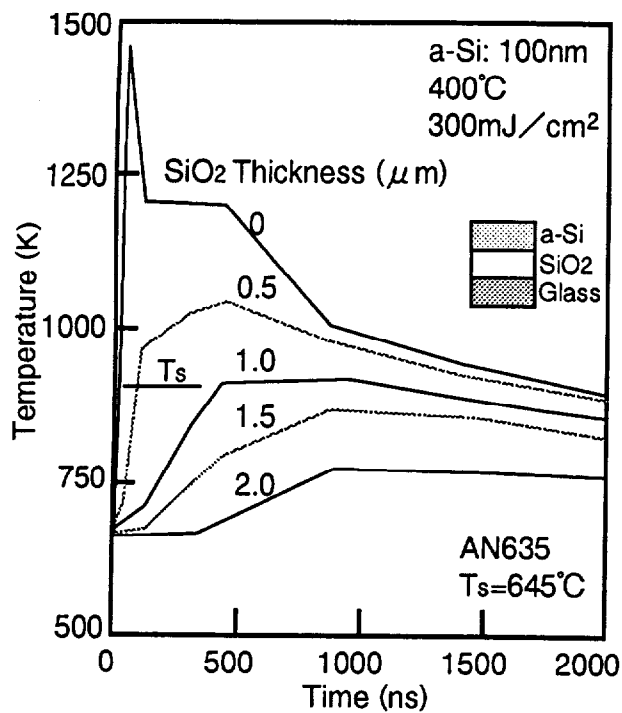


Fig. 5.3. Effect of SiO₂ thickness on the glass surface temperature. After Kuriyama et al. [21].

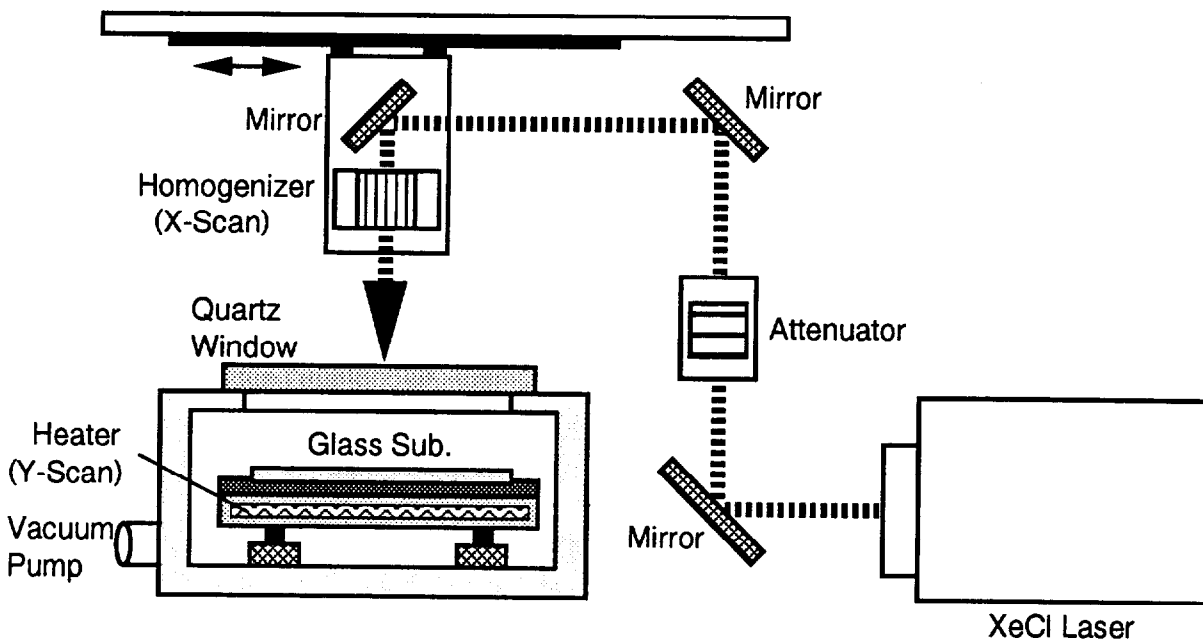


Fig. 5.4. Laser irradiation apparatus for crystallization and activation.

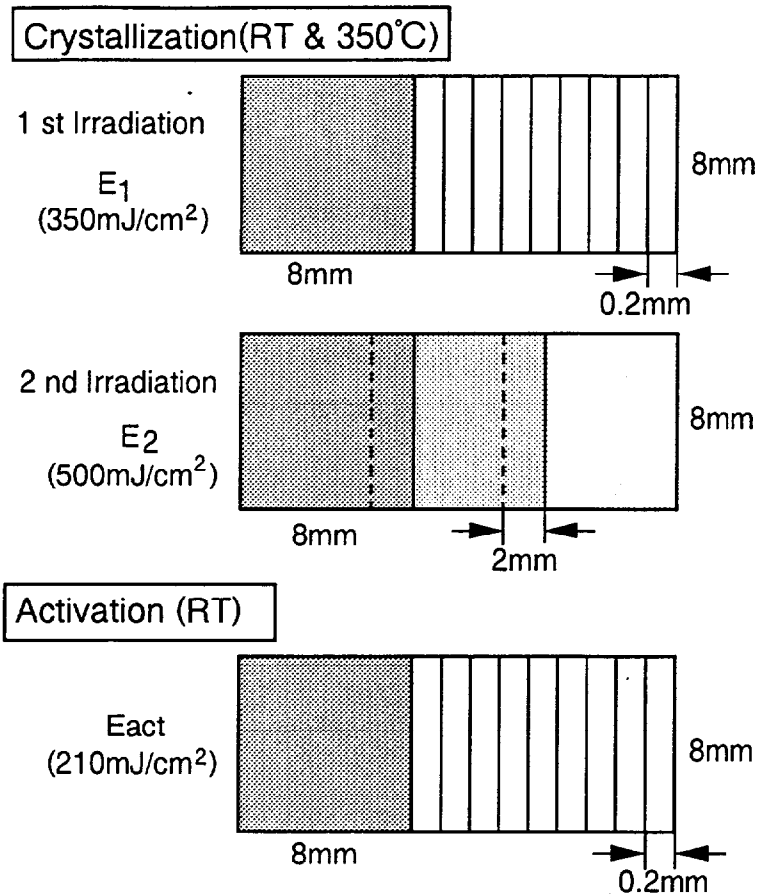


Fig. 5.5. Typical laser scanning methods for crystallization and activation.

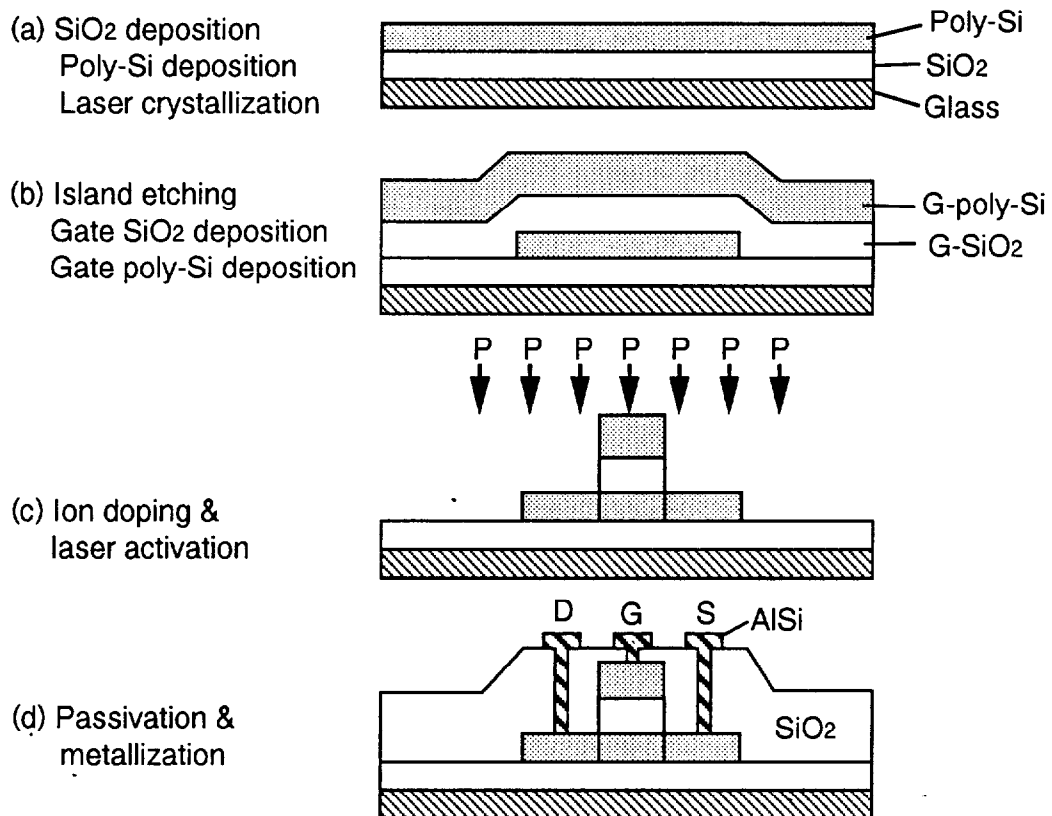


Fig. 5.6. Fabrication process of n-channel TFT.

5.2.2 TFT fabrication process

Fig.5.6 shows the fabrication process of the coplanar n-channel TFT. The typical substrate size was 350mm x 450mm which was the largest for poly-Si TFT fabrication. Therefore, conventional wet processes for LSI devices were not applicable. An all dry-etching process (Appendix 5) was tried for the first time and simplified wet cleaning processes were used. In the photolithography step, and LCD-stepper was used for exposure. The underlayer SiO₂ (300 nm) was deposited by PECVD using the TEOS-O₂ system. Then active layer poly-Si (60 nm) was deposited by the LPCVD reactor developed for this experiment at 450°C and 27 Pa using 100% Si₂H₆. High uniformity of film thickness ($\pm 6.4\%$) was achieved by optimizing deposition conditions (Appendix 4). After the two-step laser crystallization, the Si film was patterned into islands. Gate SiO₂ (150 nm) and gate poly-Si (100 nm) were deposited by PECVD and LPCVD, respectively. No chemical cleaning was applied before gate SiO₂ deposition. After gate patterning, phosphorous ions were doped at 1 and 5 kV by an ion doping technique and activated by XeCl laser as studied in Chapter 6. After SiO₂ deposition (300 nm) for passivation and contact hole etching, AlSi (300 nm) was deposited and patterned for metallization. Hydrogen annealing at low pressure and 200°C was applied. In basic studies, 100mm x 100mm substrates and almost the same steps were applied to TFT fabrication, and hydrogenation was applied at 300°C for 30 min, after N₂ annealing.

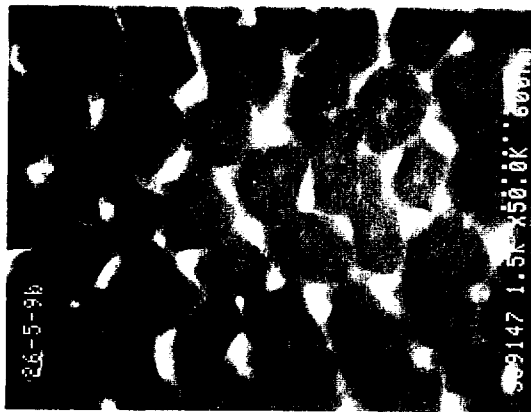
5.2.3 Characterization of poly-Si films

(1) Observation by SEM

Fig.5.7 shows SEM photographs of poly-Si films. The dependence of morphology on laser energy and position in substrate were studied. There were many ridges and nodes. The morphology depended on laser energy and high energy irradiation decreased the number of ridges. Generally, grain boundaries exist in the ridges (Fig.5.8 (b)). Therefore it was suggested that high-energy irradiation increased grain size ((e), (f)). Fine pitch irradiation seemed to decrease ridge height ((c), (d)). The morphology was almost the same in the center and periphery of the substrate. Therefore, it was implied that the whole area of the substrate could be irradiated uniformly with this technology.

(2) Observation by TEM

Fig. 5.8 shows TEM photographs of the plane and cross section of position (c) (Fig.5.7(c)). In the TEM photograph of the plane (a), grains were clearly observed. The color of each grain was random and these grains were not oriented. However, the color in a grain was uniform and the grain boundary was clear. The grain size was estimated to be 0.1-0.3 μm .

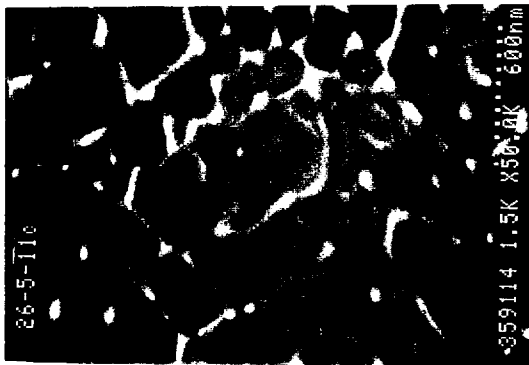


(a)

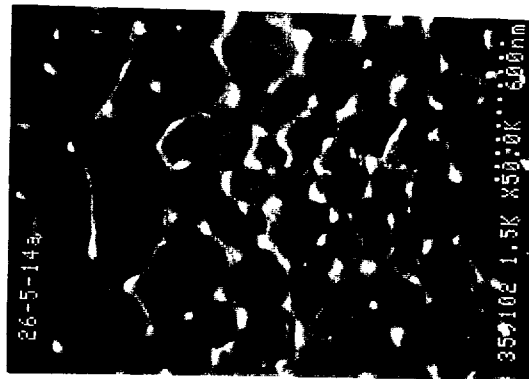


(b)

(1) 490/356 (mJ/cm²)(10 shots)



(c)



(d)

(2) 538/337 (mJ/cm²)(80 shots)



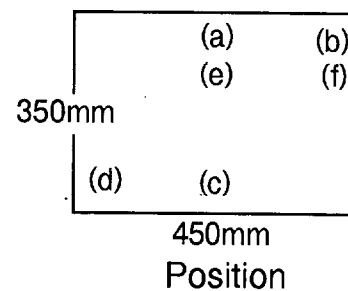
(e)



(f)

(3) 558/356 (mJ/cm²)(10 shots)

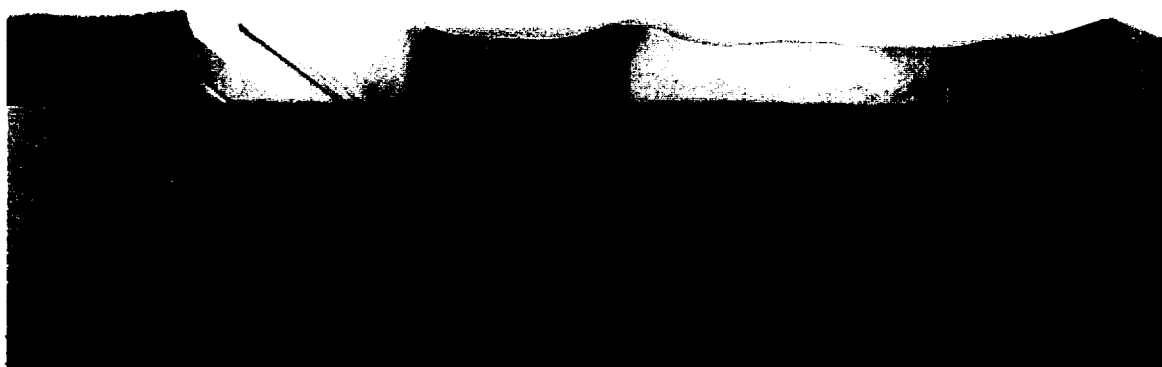
Fig. 5.7. Surface morphology dependence on laser energy and position observed by SEM. Poly-Si : 57 nm. Crystallization: RT.





(a) TEM of plane: x150,000

100nm



(b) TEM of cross section: x150,000

100nm

Fig. 5.8. TEM photographs of plane and cross section of position c (Fig.5.7).
Laser energy: 538/337 mJ/cm², 80 shots.

In the TEM photograph of the cross section (b), ridges and grain boundaries were observed. The ridge height was about 50 nm which was the same as the film thickness. In a grain between ridges, only twins were observed. Therefore, each grain had uniform and high-quality crystallinity compared with poly-Si grains by SPC as shown in Fig.3.18.

Fig.5.9 shows the lattice image of the plane film in Fig.5.8(a). The width of the transition region was narrow. The arrangement of atoms in the center grain was periodic over a long range and triangular showing that the grain had (111) surface.

(3) Observation by AFM

Poly-Si had many ridges. The height was quantitatively measured by AFM. Fig.5.10 (a) shows a plane view with crater-like morphology. The height was measured crossing the ridges and peaks ((b)). The maximum height was estimated to be about 120 nm (peak #3) which was much larger than the film thickness (60 nm). The too-high ridge would be harmful in gate operation of TFTs.

(4) Mechanism of ridge formation

The mechanism of ridge formation is illustrated in Fig.5.11 [22]. When the laser is irradiated, the Si film is heated and melted ((a)). After irradiation is finished, the heat flows to the substrate and cooling starts. After an incubation time (super cooling), solidification starts from the nuclei which remained in the interface. High-speed solidification advances from the interface in the lateral direction. In lateral solidification, mass flow is induced to the ridge because the volume of solid is increased. The specific densities of melt and solid Si are 2.53 and 2.30 g/cm³, respectively [23]. Finally, lateral growth of two grains is terminated at the ridge and the grain boundary is generated. Therefore, formation of ridges is inevitable in conventional laser crystallization. To obtain a flat surface, chemical-mechanical polishing (CMP) [24] and laser annealing with cap SiO₂ [25] were attempted.

5.2.4 TFT characteristics and fabrication of 18.2" LCD

(1) TFT structures

Fig.5.12 shows a photograph of 350 mm x 450 mm TFT substrate with test device chips. This substrate was used to evaluate the uniformity of characteristics of TFTs in a large area. Fig.5.13 shows three gate structures used in this experiment. Fig. 5.14 is a photograph of an array of gate, source and drain resistors and TFTs. The test device chips were used to evaluate the uniformity of sheet resistance and TFT characteristics in a short range region. Device pitch was 0.2 μm which was the same as that of the fine pitch laser beam scan in Fig. 5.5.

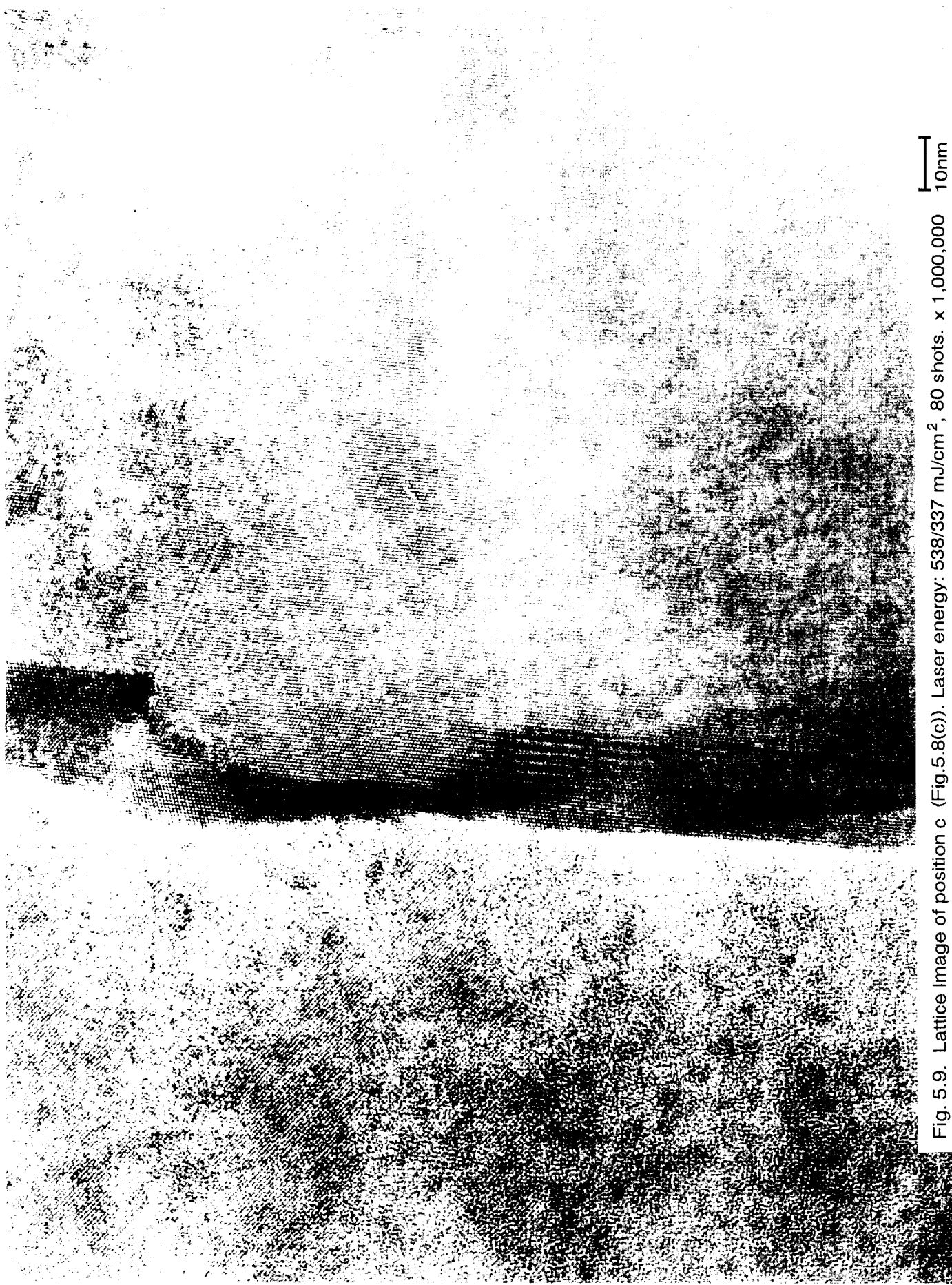
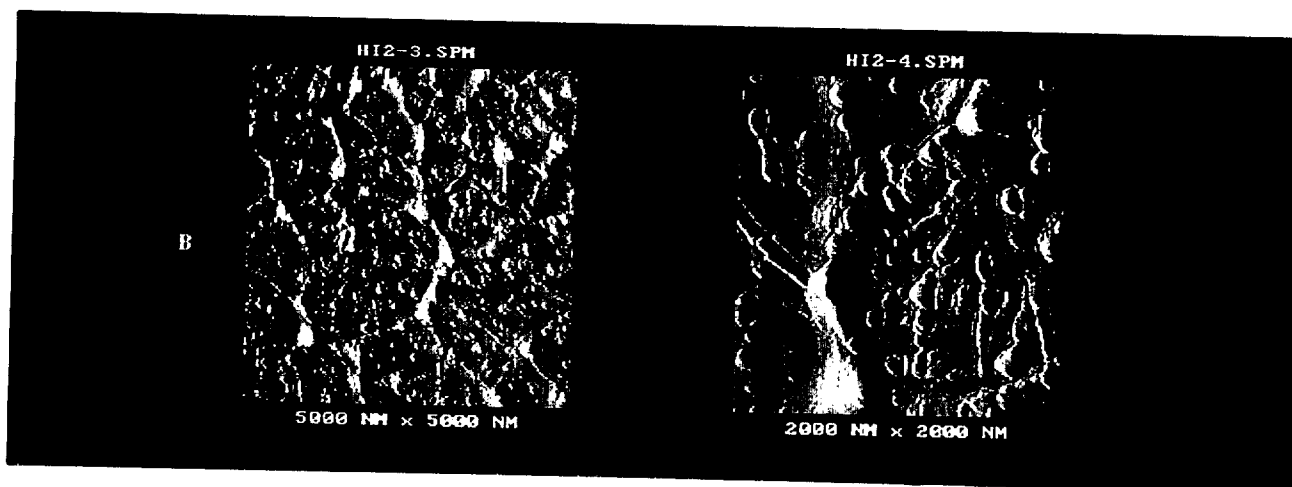
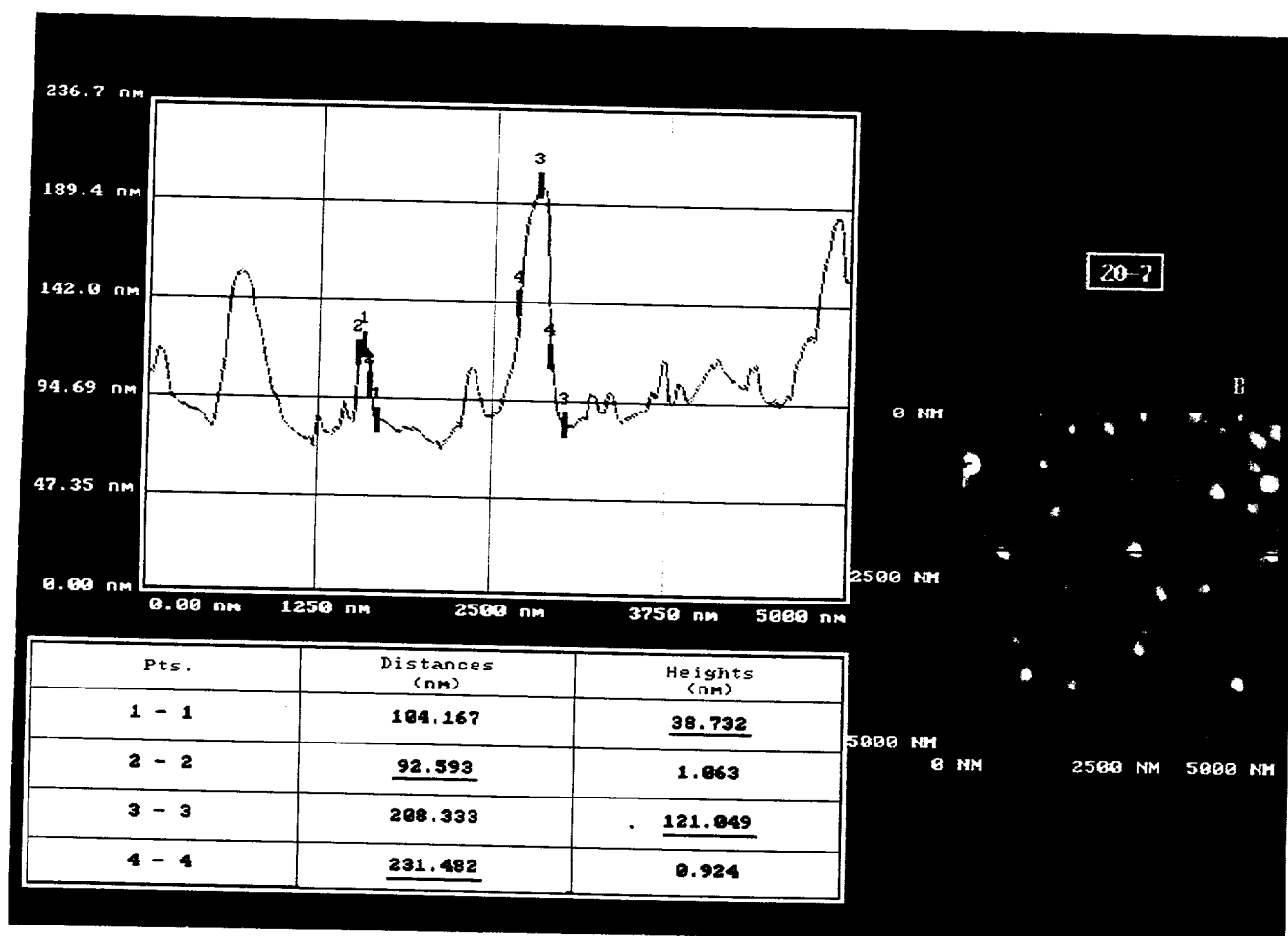


Fig. 5.9. Lattice Image of position c (Fig. 5.8(c)). Laser energy: 538/337 mJ/cm², 80 shots. x 1,000,000



(a) AFM images of plane



(b) Height of ridges along the line

Fig. 5.10. Example of surface morphology observed by AFM.
Laser energy: $450 \times 10 / 350 \times 4$ ($\text{mJ}/\text{cm}^2 \times \text{shot}$).

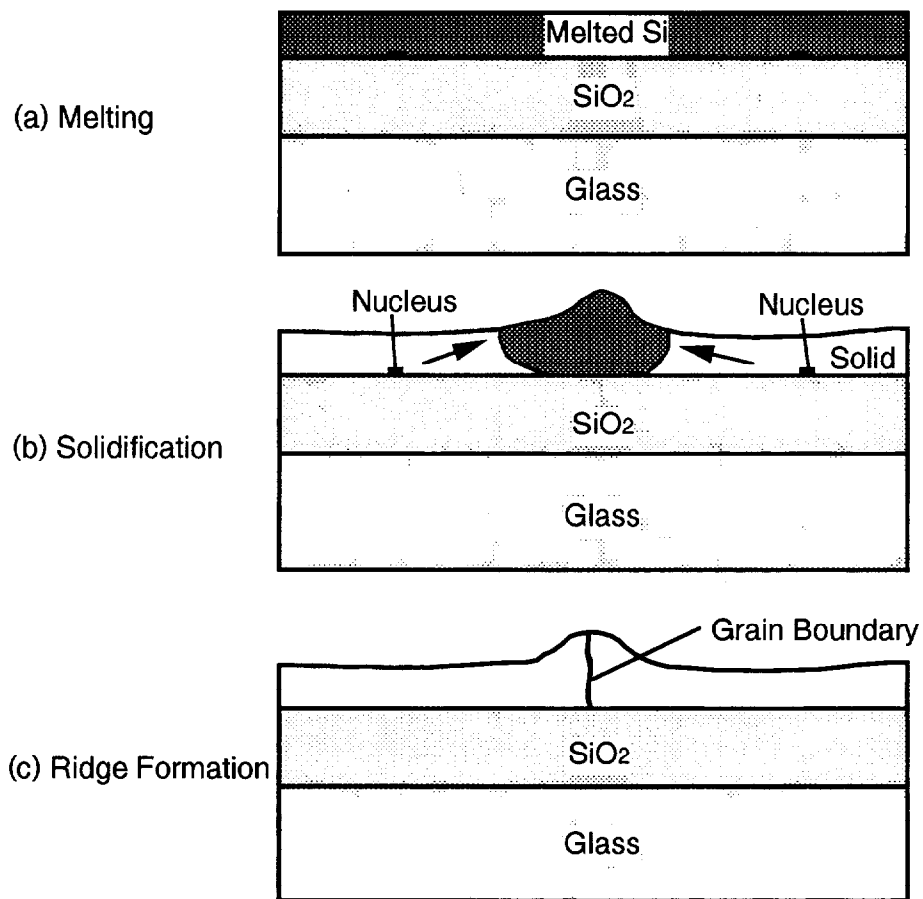


Fig. 5. 11. Process model of solidification and ridge formation [22].

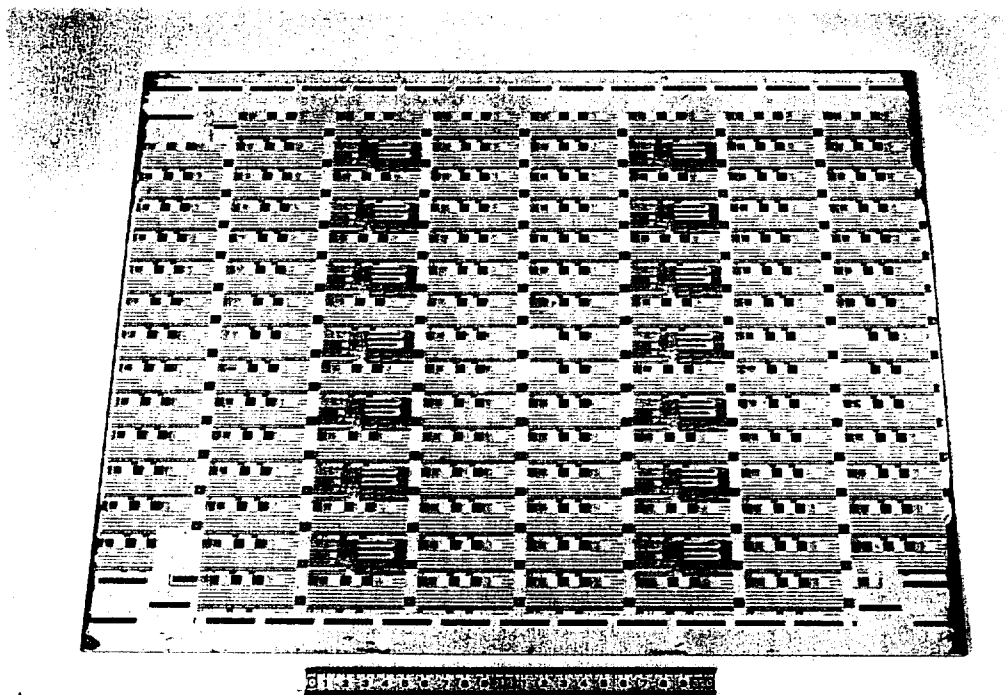


Fig. 5.12. Photograph of TFT substrate with test device chips. Substrate size is 350mm x 450mm.

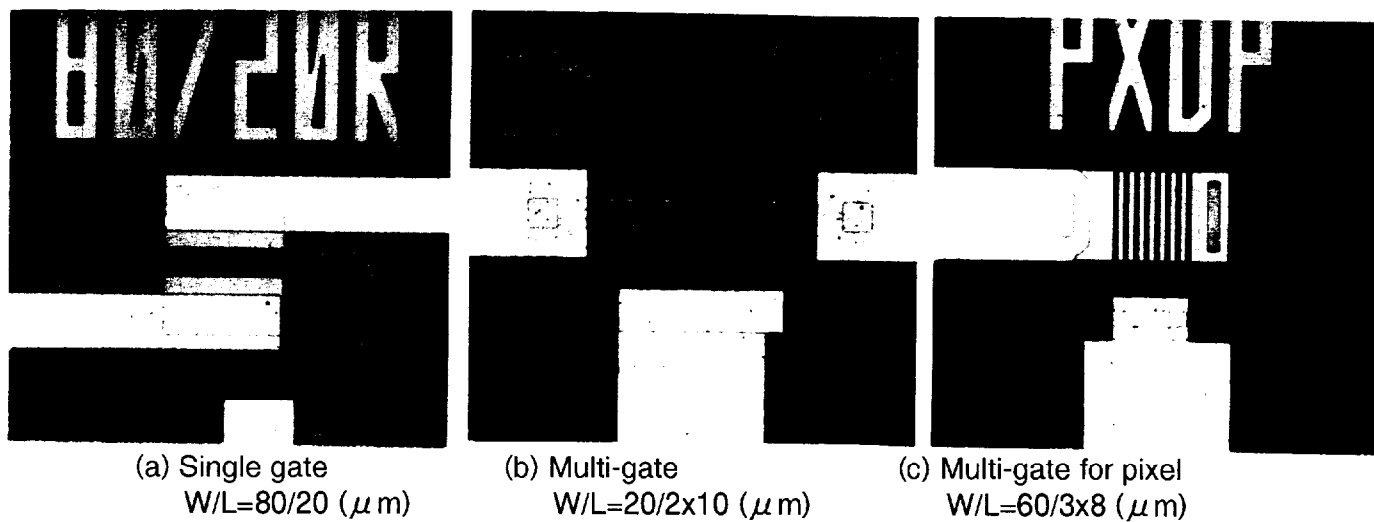


Fig. 5.13. Fabricated single- and multi-gate TFTs.

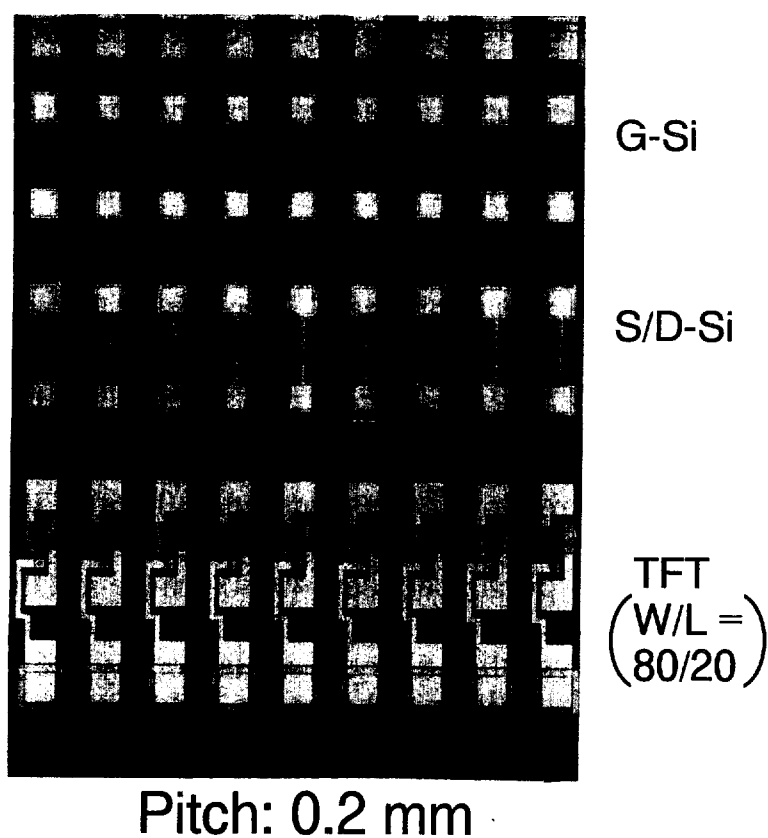


Fig. 5.14. Photograph of array of gate, source and drain resistors and TFTs.

(2) Multi-gate TFTs on 100mm x 100mm substrates

The reduction of leakage current is also important in laser crystallized TFTs. In this study, the multi-gate structure was introduced for SPC TFTs (Fig.2.16).

Fig.5.15 shows typical V_G - I_D characteristics of single- and multi-gate (10 divisions) TFTs. It was clear that the multi-gate structures were also effective to reduce leakage current at a negative gate voltage region in laser crystallized poly-Si TFTs. Fig.5.16 shows the quantitative effect of gate structure on TFT characteristics. Field-effect mobility was almost constant and independent of gate structure. Off-current, especially its minimum value was drastically reduced from 100 pA to 0.3 pA at $V_D=10V$. It was shown that the multi-gate structures could reduce off-current using the same fabrication process as single gate TFTs.

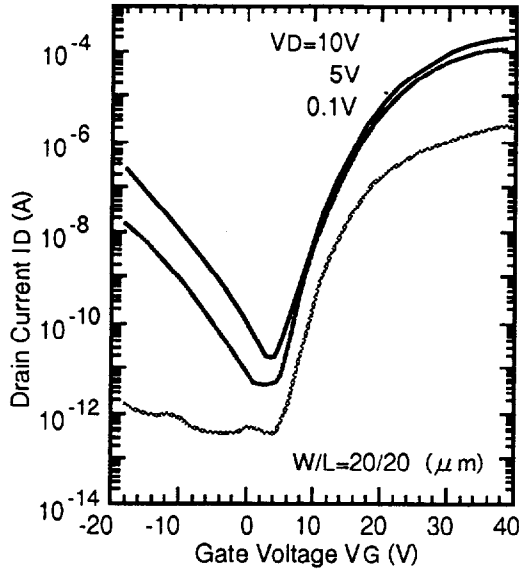
(3) Multi-gate TFTs on 350mm x 450mm substrates

Fig.5.17 shows typical V_G - I_D characteristics of a multi-gate TFT on 350mm x 450mm substrates. As mentioned in the TFT fabrication process, chemical cleaning was not applied before gate SiO_2 deposition. Thus performances of these TFTs were slightly degraded compared with the TFTs on the 100mm x 100mm substrate.

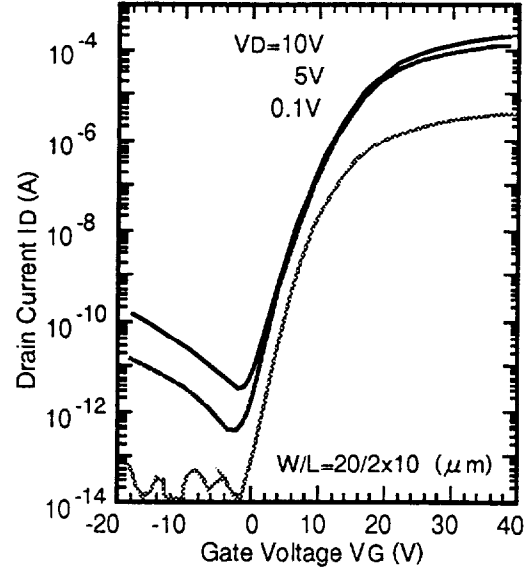
Fig.5.18 shows the distribution of field-effect mobility on the glass substrate. One of the multi-gate TFTs with a ten-division gate (Fig.5.13 (b)) in each chip was measured. The laser energy of crystallization (E_2) and activation were varied. In the substrate center region with crystallization energy larger than 475 mJ/cm² and an activation energy of 210 mJ/cm², field-effect mobilities of 60-90 cm²/V·s were obtained. The maximum value was 109 cm²/V·s. Thus, uniformity of the performance in a large area of substrate was confirmed. Then the short range uniformity was evaluated using the device shown in Fig.5.14.

At first, the uniformity of array components was evaluated. The substrate was crystallized at room temperature by a one-step irradiation (6 mm pitch) and doped at 1 keV for 45 s. The sheet resistances of gate and source and drain were almost constant and 180-260, 130-180 Ω /sheet, respectively. But field-effect mobility periodically changed (6 mm pitch same as the laser beam pitch) between 40-80 cm²/V·s. Off-current also changed similarly. Thus, the conventional laser irradiation conditions were not sufficient to crystallize a large area uniformly [26].

Next, improved conditions shown in Fig.5.5 were applied and uniformity of characteristics was evaluated in the chip enclosed by the thick line in Fig.5.18. Fig.5.19 plots the field-effect mobility and sheet resistance of TFTs in the 40 mm range. The sheet resistance of the source and drain was almost constant and 250-350 Ω /sheet, which was low enough for TFT use. The sheet resistance of the gate was also low enough for gate use and 400-800 Ω /sheet. But the value changed periodically. This change depended on the slight difference in pitch between the gate resistor position and laser beam (the difference was about 5 μ m and the

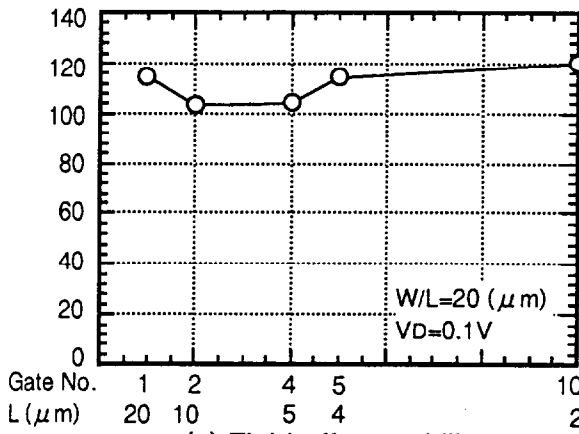


(b) Single-gate TFT

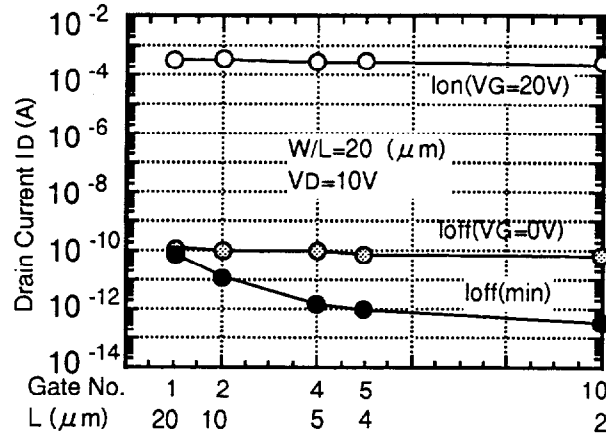


(b) Multi-gate TFT (10 divisions)

Fig. 5.15. Characteristics of single- and multi-gate TFTs (100mm x 100mm substrates).



(a) Field-effect mobility



(b) Drain current

Fig. 5.16. Dependence of TFT characteristics on multi-gate structures (100mm x 100mm substrate).

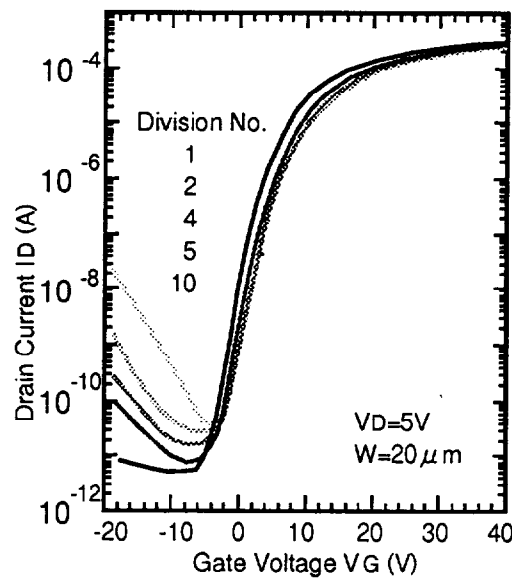


Fig. 5.17. Characteristics of single- and multi-gate TFTs (350mm x 450mm substrates).

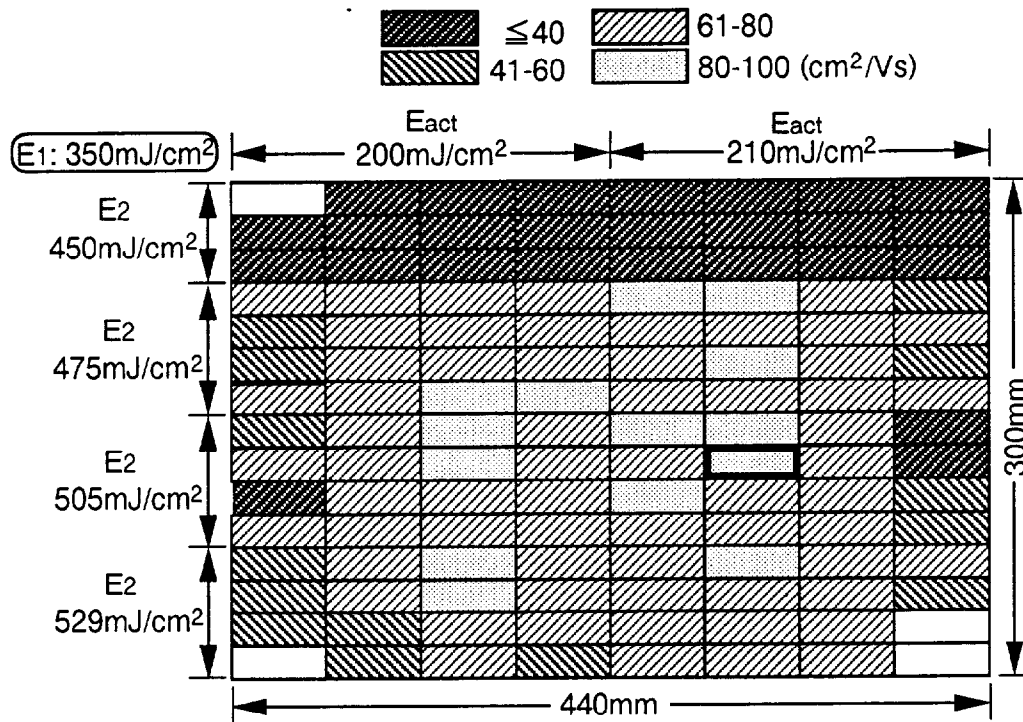


Fig. 5.18. Distribution of field-effect mobility in 350mm x 450mm substrate. $W/L=20\mu\text{m}/2\mu\text{m} \times 10$.

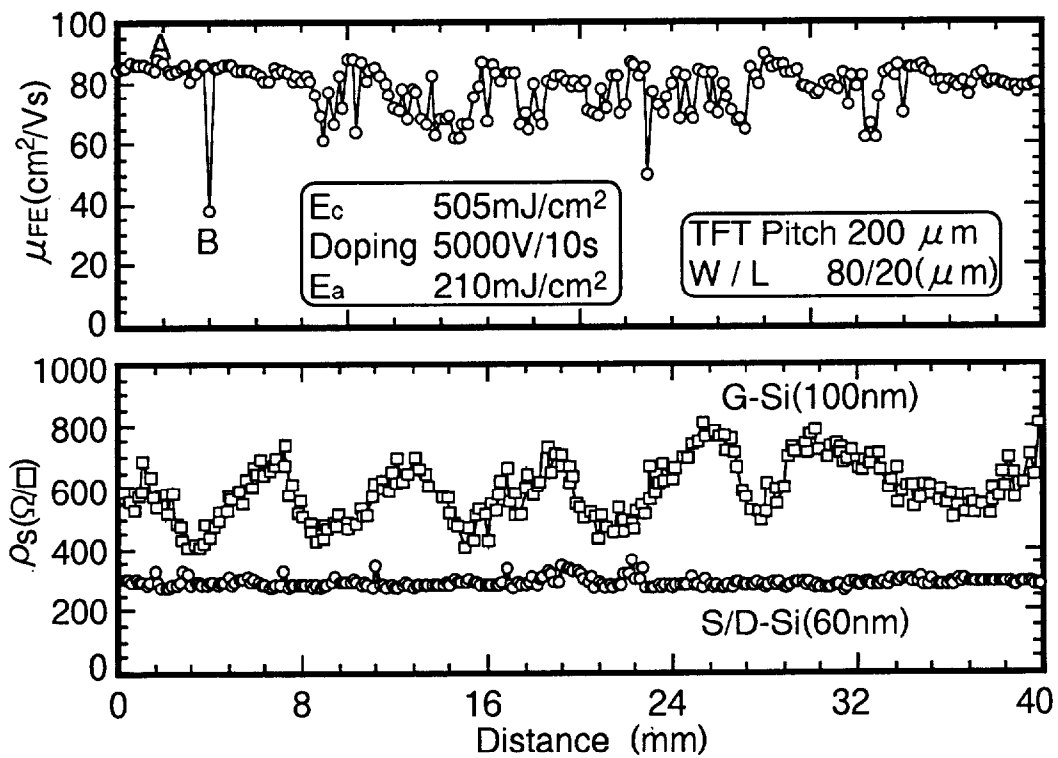


Fig. 5.19. Uniformity of μ_{FE} and ρ_s in 25 mm length. TFTs were fabricated by two-step crystallization. Doping conditions: 5000 V, 200mA, 10 s.

least common multiple length was about 8 mm). The sheet resistance showed a minimum value when the strongest part of the beam hit the Si island. The gate sheet resistance was higher than that of source and drain because the gate was amorphous before ion doping and activation were carried out. With the exception of two TFTs, the field-effect mobility was 60-90 cm²/V·s. Thus, performance and uniformity were improved by the new crystallization conditions.

The abnormal TFT B was inspected to identify the reason for its low mobility compared with the normal device A. Fig.5.20 shows photographs of these two TFTs observed from the poly-Si gate side in the dark field mode. The gate poly-Si surface reflected the surface morphology of active layer poly-Si. The channel region of TFT A had a fine spotted plane with good uniformity which reflected the uniform crystallization of poly-Si. But in TFT B, spots were not uniform and partial dark areas (flat) were observed. This implied that the crystallization was not uniform. The crystallinity of channel region was inspected by TEM.

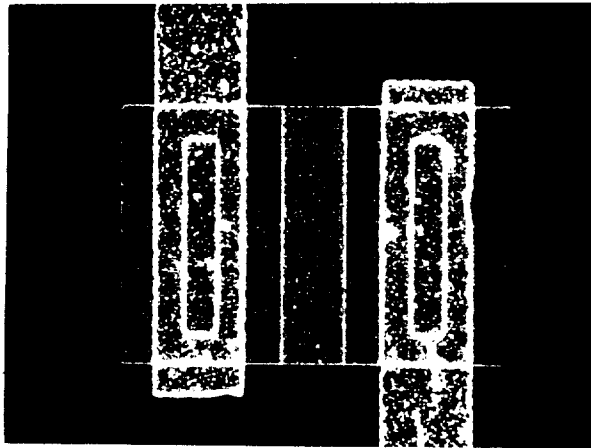
Fig.5.21 shows TEM photographs of cross section of TFTs. In TFT A, active layer poly-Si had large grains proving that the TFT had large mobility. In TFT B, large grains were observed in source and drain region, but grains were very fine in the channel region. The results proved that the low mobility of TFT B was caused by imperfect crystallization. The reason for appearance of fine grains in the localized area was not clear. But appearance of TFT B curves were not periodical in Fig.5.19. Therefore, it was most probable that the poly-Si film was accidentally contaminated locally before crystallization.

(4) Application of TFTs to 18.2" LCD

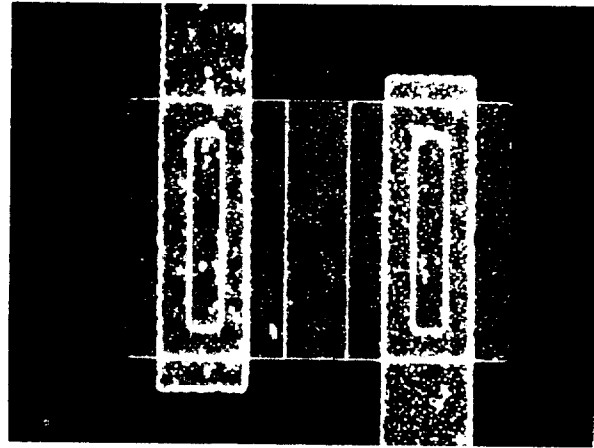
Table 5.1 summarizes the specifications of the fabricated 18.2" poly-Si TFT-LCD. It is assumed that one of the final goals of poly-Si TFT-LCDs is for 40" class HDTV. Therefore, fabrication of a quarter size (quarter dot number) of the 40" HDTV was attempted on 350mm x 450mm substrates. Multi-gate structure was introduced for pixel TFTs to reduce off-current. Considering resolution of the LCD stepper, an 8- division gate with lines and spaces of 3 and 4 μm was used. To compensate the leakage current, a storage capacitor with 1 pF (C_{LC}=0.38 pF) was fabricated considering the high driving ability of poly-Si TFT as shown in section 2.3.

Table 5.1. Specifications of 18.2' poly-Si TFT-LCD

Display Size	403.2 x 227.0 (16:9)
Dot Number	960 x 3 x 517
Pixel Size	140 μm x 439 μm
Storage Capacitance	1pF (C _{LC} =0.38pF)
Pixel TFT	W/L=60 μm/3 μmx8



(a) TFT A: $\mu_{FE}=87\text{cm}^2/\text{Vs}$



(b) TFT B: $\mu_{FE}=38\text{cm}^2/\text{Vs}$

20 μm

Fig. 5. 20. Surfaces of TFTs with the highest and lowest mobilities in Fig. 5.19.



(a) TEM micrograph of TFT A with mobility of $87\text{cm}^2/\text{Vs}$.



(b) TEM micrograph of TFT B with mobility of $38\text{cm}^2/\text{Vs}$.

Fig. 5.21. TEM micrographs of TFTs with the highest and lowest mobilities in Fig. 5.19.

Fig. 5.22 is a photograph of the TFT array substrate for the 18.2" TFT-LCD. The test device chips were located in the peripheral region of the substrate. Fig. 5.23 is a photograph of pixel TFTs. After the first passivation SiO_2 layer (100 nm) was deposited on gate poly-Si, the first AlSi layer (200 nm) was sputtered as a gate metal line and storage common line. Then the second passivation SiO_2 layer (300 nm) was deposited. Finally ITO was sputtered (140 nm). All four materials were patterned by dry etching (Appendix 5). Fig. 5.24 shows photographs of a pixel TFT after laser activation. The whole area of the large substrate was uniformly activated. Fig. 5.25 shows TEM photographs after first passivation SiO_2 layer deposition. One unit gate region was observed. Actual length of the unit gate was $2.6\text{ }\mu\text{m}$ though the designed value was $3\text{ }\mu\text{m}$ ((a)). It was difficult to control length precisely on a large substrate because photoresist was thick ($4\text{ }\mu\text{m}$) and control of spin developing was difficult. Active layer (channel region) poly-Si was of good quality and had some ridges ((b)). The maximum height of ridges was about 20 nm. The film thickness of the source and drain region was slightly reduced by the gate oxide dry etching. But its quality was also good even though ion doping and laser activation were applied. The crystallinity was recovered by laser activation. The gate Si was amorphous in the first stage but became polycrystalline as a result of ion doping and laser activation. The gate bottom region had small grains because the activation laser energy was low and the gate Si was thick (100 nm). Generally, the silicon films were well crystallized and gate structure was well patterned in spite of the introduction of an all-dry etching process.

Fig. 5.26 shows typical V_G - I_D characteristics of a pixel TFT. The performances were slightly inferior to that of TFTs on the 100mm x 100mm substrates shown in Fig. 5.15. But the former was sufficient for pixel TFT use. The degradation of TFT characteristics was observed after ITO dry etching, probably because of plasma damage. But characteristics were almost completely recovered by low pressure hydrogen annealing at 200°C . The maximum process temperature was 450°C for the first LPCVD of Si film and 300°C for the following TFT fabrication process. Substrate shrinkage was less than -10 ppm and it was successfully compensated by using an LCD stepper with image shrink control between 0 to -40 ppm.

Fig. 5.27 shows an example display image of the 18.2" TFT-LCD. The white dotted area was observed in the upper left of the panel because of incomplete etching of the contact-hole for pixel ITO. There were many dot and line defects, but the whole area worked successfully. Thus, the usefulness of large area laser crystallization, ion doping and laser activation, PECVD SiO_2 deposition, and all-dry etching process for large poly-Si TFT-LCDs, as well as conventional small and middle size TFT-LCDs, was confirmed.

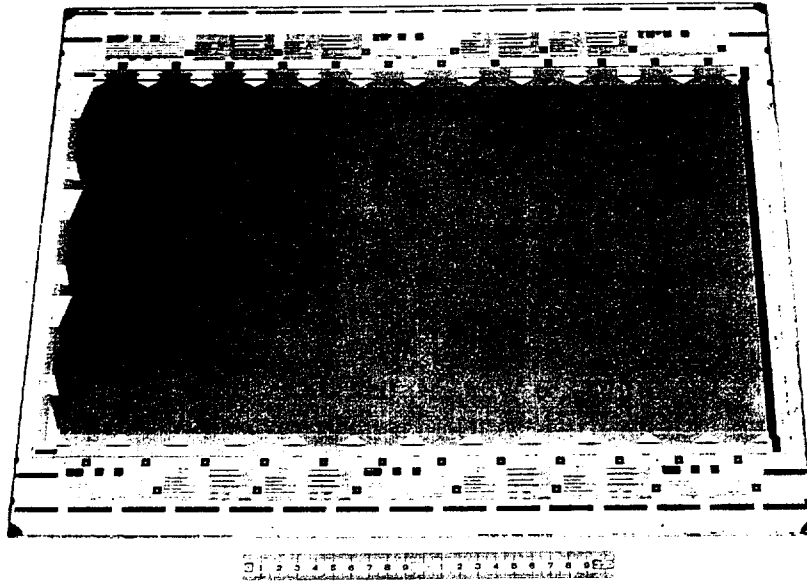


Fig. 5.22. Photograph of TFT array for 18.2" LCD.

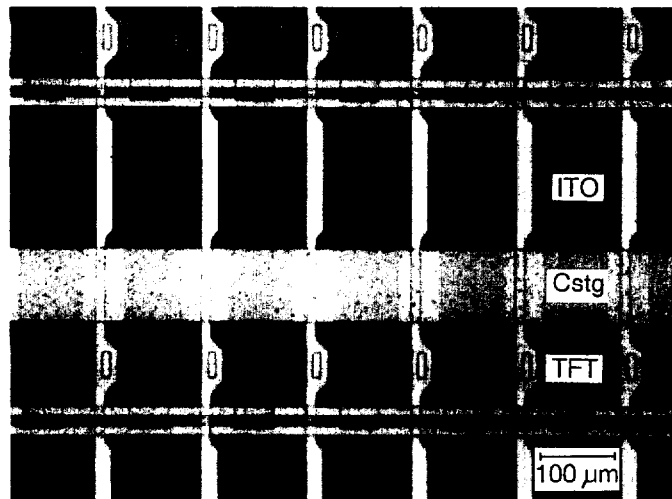
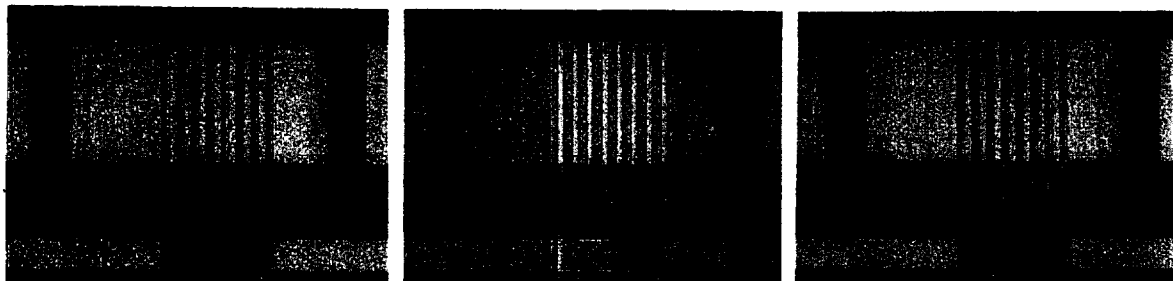


Fig. 5.23. Photograph of pixels patterned by all dry etching process.



(a) Left

(b) Center

(c) Right

S/D Si	66 nm
G Si	100nm

Doping	1000V/45s
Activation	200mJ/cm ²

50 μm

Fig. 5.24 Surface of TFTs after laser activation in 350mm x 450mm substrate.



(a) Unit gate



(b) Edge region of unit gate

Fig. 5.25. TEM micrograph of gate region of pixel TFT. Ion doping: 1000V, 45 s; Activation: 200 mJ/cm².

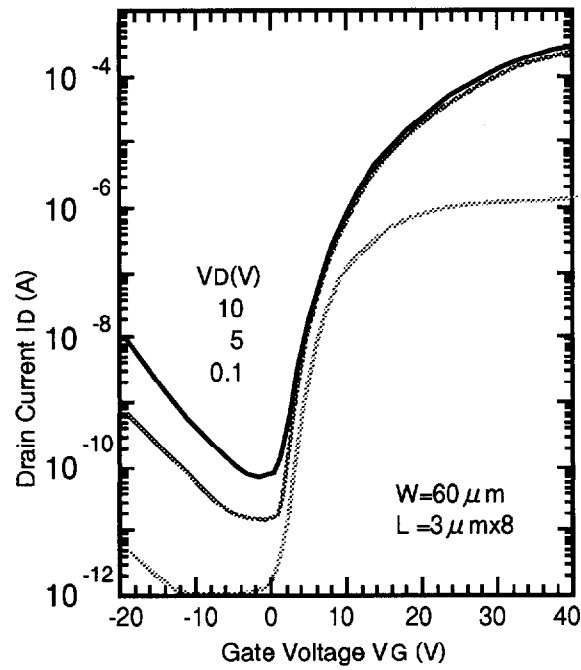


Fig. 5.26 V_G - I_D characteristics of pixel TFT.

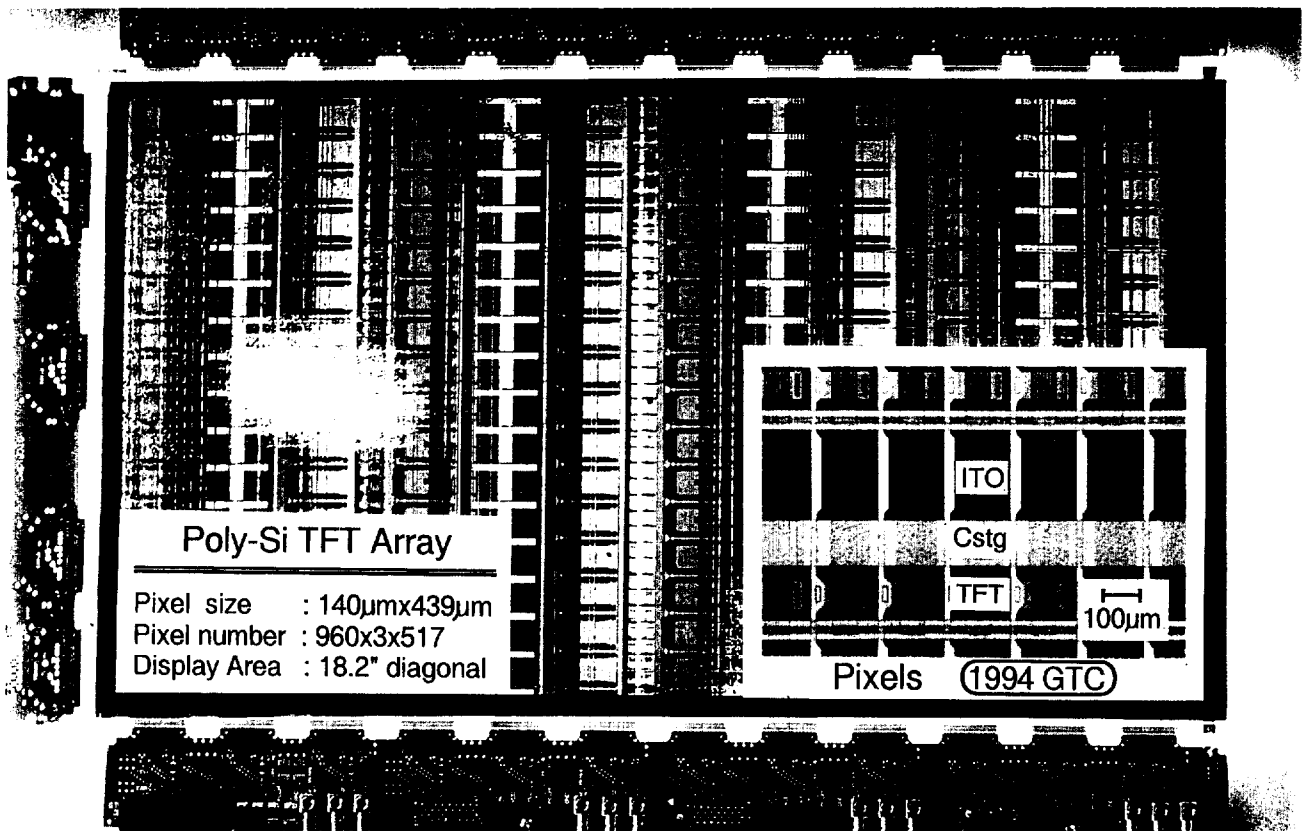


Fig. 5.27. Example display image of 18.2" TFT-LCD

5.3 Conclusions

The large-area laser crystallization was explored for the 350mm x 450mm substrates by using excimer laser crystallization. As a precursor of Si film, LPCVD film was deposited by using Si_2H_6 at 450°C. Excimer laser crystallization with square beam of 7 x 7mm was used. The large area was almost uniformly crystallized. The poly-Si film had ridges with the same height as film thickness.

Applying ion doping and laser activation, n-channel TFTs were fabricated on the substrates. Field-effect mobility of 60-90 $\text{cm}^2/\text{V}\cdot\text{s}$ was obtained. The world's largest 18.2" TFT-LCD with 960x3x517 pixels was fabricated and operated successfully. The maximum process temperature was 450°C which was sufficiently low enough for large glass use. Excimer laser crystallization is a promising way to crystallize large-area substrates at low temperature.

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Large-Area High-Speed Ion Doping Technologies

Novel ion doping and activation technologies are proposed for TFTs on the large glass substrates. The bucket-type (Kaufman-type) ion source which can generate a high density ion beam is introduced to non-mass-separated ion doping for the first time to realize high-speed low-energy treatment. Laser activation is employed for low-temperature activation. Doping apparatuses with ion sources of 150 mm diameter and a linear 100mm x 400mm shape are developed. A 10-s doping technology is achieved for source and drain of TFTs on 350mm x 450mm substrates. And its doping mechanism is also discussed.

6.1 Introduction

6.1.1 Doping technologies for poly-Si TFTs

One of the key processes for TFTs is doping and activation. To realize good switching characteristics in TFTs, proper junction formation is indispensable. In CMOS TFTs which have two type channel conductions, two type ions, namely, donor and acceptor doping is necessary. Single polar TFTs may be fabricated by deposition of a doped semiconductor layer, but the CMOS structure can be simply realized by just doping impurity ions into source and drain.

Table 6.1 summarizes doping and activation technologies for semiconductor devices. In LSI fabrication, ion implantation with mass-separation and furnace activation have been basic technologies though plasma doping and rapid thermal annealing for shallow doping are being introduced today. Considering the fabrication of TFTs on large glass substrate for which thermal conductance is much lower than that of Si wafer, a special doping concept to reduce heat damage of resist is needed. Thickness of poly-Si is less than 100nm, therefore low energy doping is essential in direct doping without cap. High-rate doping with a simplified apparatus is also an important issue for large glass substrates. High-throughput, such as one substrate / min, the same as for a-Si TFT-LCD, is required.

Table 6.1 Summary of doping and activation technologies for semiconductor devices.

Dopant source	Doping Species	Doping method	Activation	Application
Ion beam (Mass-separated)	P+, As+ B+, BF ₂ +	Ion Implantation	FA, RTA, (LA)	LSIs
			FA, RTA, LA	TFTs
Ion beam (Non-mass-separated)	P+, B+, H+	Ion doping	FA, RTA, LA	TFTs
			(FA, RTA)	(LSIs)
Gas phase	POCl ₃	Deposition	FA	Power Devices, ICs
	PH ₃	Plasma doping	FA, LA, RTA	TFTs, (LSIs)
	B ₂ H ₆	Laser doping	LA	TFTs
Solid	BN	Deposition &	FA	Power Devices, ICs
	PSG	Solid diffusion		

FA: Furnace annealing, RTA: Rapid thermal annealing, LA: Laser activation

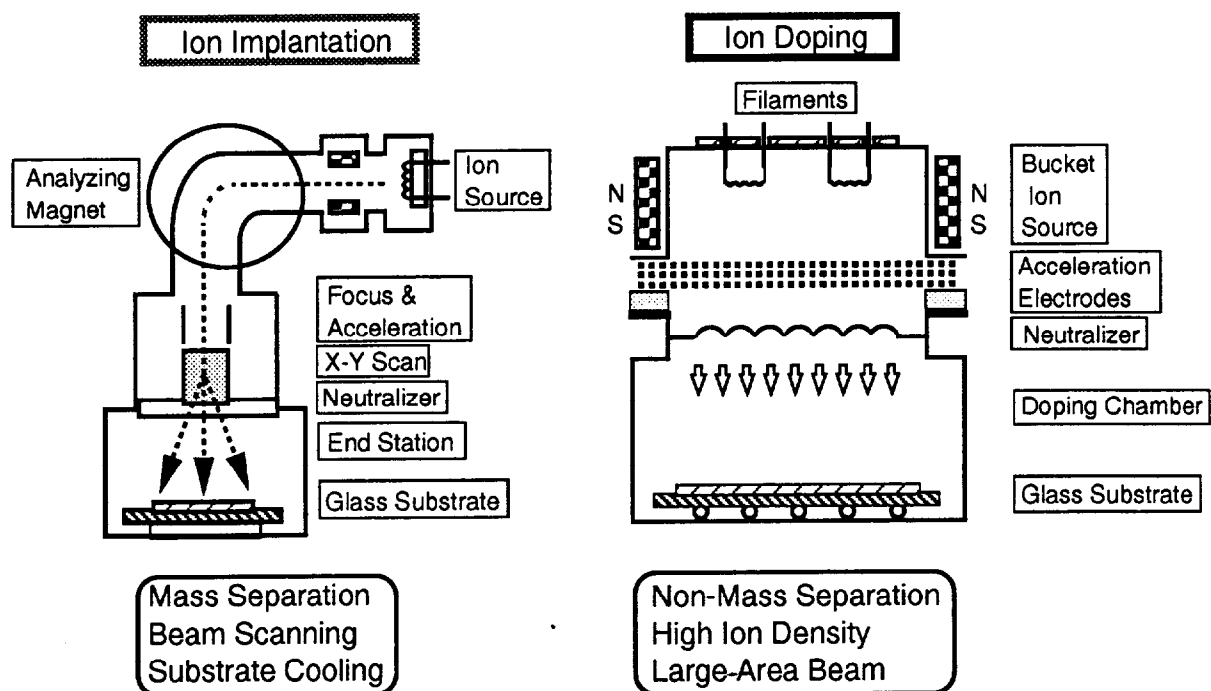


Fig. 6.1. Schematic structure and characteristics of ion implantation and ion doping apparatuses.

Generally, in LSI fabrication, high-temperature treatment is used to recover crystallinity and activate implanted ions. But the maximum process temperature must be below 600 °C when glass substrates are used. Therefore, a low-temperature activation method is also indispensable for poly-Si TFTs.

Considering these requirements, a new doping and activation process must be developed. Large-area doping, plasma doping and laser doping, without using implanter has been proposed for solar cell fabrication. Plasma doping was used with non-mass-separated ions from DC or RF discharge plasma as dopant source. These ions were diffused and activated by laser irradiation [1]. General laser doping was done with a gaseous source. Deposition and activation were carried out simultaneously by laser irradiation [2]. In these methods, the plasma or gas source contacted directly with Si films and ion energy was not positively controlled. Laser activation should be a promising means for low-temperature activation for poly-Si TFTs, too.

Improved plasma doping technologies which accelerated ions without mass-separation were proposed for shallow doping. Ions were generated by RF discharge [3], [4] or electron cyclotron resonance (ECR) [5] in quartz chamber. Ion energy was controlled artificially by acceleration electrode. These methods have been generally referred to as ion doping (I/D) compared with conventional ion implantation (I/I). RF discharge chamber can be scaled up for large substrates. But ion beam density is about 10 $\mu\text{A}/\text{cm}^2$ [3] and high-rate doping is difficult. In this study, a bucket-type (Kaufman-type) ion source which can generate a high density ion beam, was introduced to ion doping.

6.1.2 Ion implanter and bucket-type ion source

Fig. 6.1 shows the schematic structures and characteristics of ion implantation and ion doping apparatuses. The ion implanter consists of plasma ion source, analyzing magnet for mass separation, resolving slit, acceleration tube, X-Y scanner, neutralizer, and end station with substrates and Faraday gage. High selectivity for the ion species, excellent controllability of dose and projection range, and high uniformity are realized. But, generally, the implanter is very complicated and machine cost is relatively high for TFT use. The acceleration voltage for LSI use is generally high and shallow doping with high rate for thin poly-Si film is difficult. The beam scanning is also a drawback for large substrate treatment because getting a high-current large-area beam is difficult.

The bucket-type ion source was developed for a high-density ion source and applied to ion milling or ion mixing for thin film etching or deposition. A typical application was as a large-area and 500 kV ion beam source to heat plasma for the atomic fusion apparatus JT60. This ion source has been proposed for high-speed ion doping for large substrates [6]-[8]. The doping unit includes an arc discharge chamber with filaments for thermal electron source and permanent magnet, electron extraction

and acceleration electrodes, neutralizer, and doping chamber. The arc discharge chamber wall, and extraction and acceleration electrodes are fabricated from hard metal plates to reduce ion sputtering.

The high-density and uniform-discharge plasma is formed by thermally emitted electrons and the cusp field of the permanent magnets which are set outside the chamber. The ion beam is extracted from the arc discharge chamber through electrode holes and irradiated onto a sample without mass separation. The ion beam current can be controlled by varying the filament current, arc discharge voltage, arc current, and acceleration voltage. A typical ion beam intensity of 0.5 mA/cm^2 which is ten times higher than that of conventional ion doping [3] can be realized. The maximum bucket-type ion source for ion milling which has a 580-mm diameter has 4 filaments, and operates at an acceleration voltage of 500 V [9]. Thus, a sufficiently large and high-ability ion source should be realized.

6.1.3 High-speed low-energy ion doping

Mass-produced a-Si TFT-LCDs have used a reversed-staggered structure. Poly-Si TFTs have also been made by the reversed-staggered structure [10], [11]. Generally, the coplanar structure has been used in Si LSI devices to realize high performance circuits. Therefore, the coplanar structure [12] was also used for TFT fabrication here.

Fig. 6.2 shows two TFT structures during ion doping. Today, for fine TFT-LCDs, ion implantation is carried out to penetrate the gate insulator by applying a high acceleration voltage such as 80 keV as shown in Fig. 6.2.(a). In this process, the glass substrate temperature is raised by the ion beam energy. Therefore, substrate cooling or moderately long-time doping with low ion beam density is necessary [12]. In this study, direct doping to bare source, drain and gate was carried out as shown in Fig. 6.2.(b). Low-energy and high ion beam density could be utilized to realize high-speed doping which suppresses the substrate temperature rise for resist mask use. Laser activation was introduced to realize low-temperature activation.

Fundamentals of ion beam current characteristics, doping by using 150-mm diameter ion source, and activation characteristics have been reported [6], [7]. In this thesis, high-speed 10-s doping technology using the 150-mm diameter ion source was studied. Then, large area doping technology using a newly developed 100mm x 400mm linear ion source for 350mm x 450mm substrate was studied, and the doping mechanism was discussed.

6.2 Ion doping with 150-mm diameter ion source

6.2.1 Ion doping

Fig. 6.3 shows a schematic diagram of the bucket-type ion doping apparatus with 150-mm diameter ion source. The arc discharge chamber

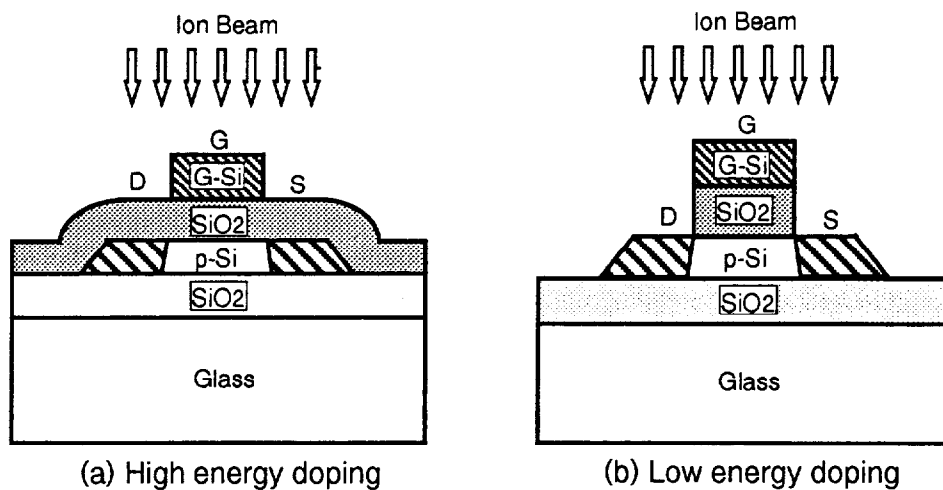


Fig. 6.2. TFT structures in two doping processes

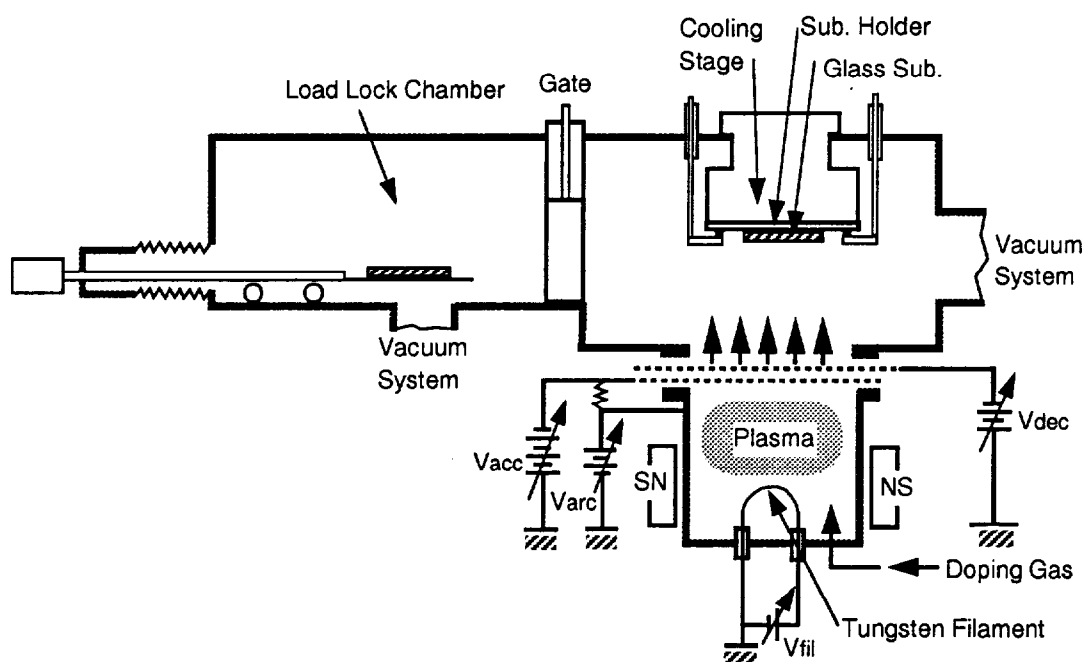


Fig. 6.3. Schematic diagram of the bucket-type ion doping apparatus with 150 mm diameter ion source.

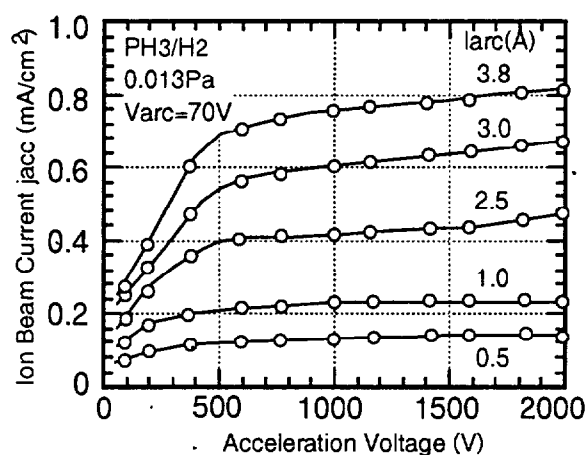


Fig. 6.4. Dependence of ion beam current on acceleration voltage with arc current as a parameter.

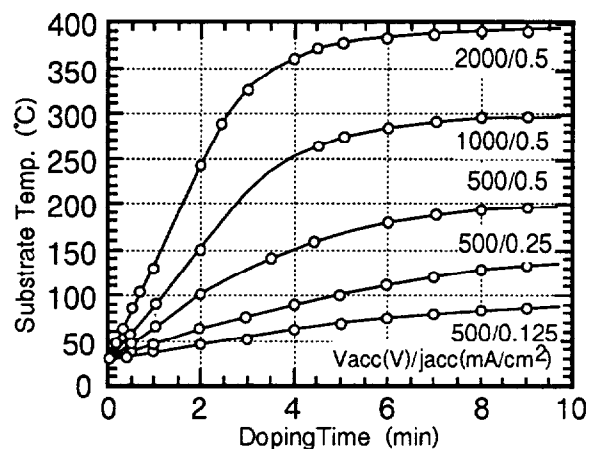


Fig. 6.5. Dependence of substrate temperature rise on doping time with acceleration voltage and beam current as parameter.

size was 250 mm in diameter with 24 permanent magnets on the outer wall. The doping chamber size was 585mm x 540mm. The extraction and acceleration electrodes had 120 holes of 4-mm diameter. The maximum acceleration voltage was 2000 V. The ion beam current (j_{acc}) could be controlled by varying the filament current (I_{fil}), arc discharge voltage (V_{arc}), arc current (I_{arc}), and acceleration voltage (V_{acc}). The maximum j_{acc} of 1.2 mA/cm² was achieved at V_{acc} of 2000 V and I_{arc} of 2 A. The typical values were: V_{arc} =70V; V_{acc} =500V; deceleration voltage V_{dec} =100V; j_{acc} =0.25mA/cm²; and pressure in arc chamber= 2.7×10^{-2} Pa.

The glass substrate (100mm x 100mm) was fixed tightly on the aluminum holder (300mm x 300mm). The apparatus could irradiate the entire area of 200mm x 300mm with six shots of the ion beam by moving the substrate and holder manually. The doping gas was 1 % PH₃ diluted by H₂ (conventional dilution gas for LSI fabrication) and He. Doping time was varied from 10 to 1800 s.

Fig. 6.4 plots the dependence of ion beam current on acceleration voltage with arc current as a parameter. The ion beam current mostly depended on arc current. It was almost saturated when acceleration voltage was higher than 500 V. The DC discharge was affected by electrode stability, i.e., contamination on the arc chamber wall or tungsten filament. After 20-h operation, no quality change was observed for the tungsten filament. After 10-h operation, the ion beam current decreased slightly. This phenomenon may depend on the arc chamber wall contamination. But the ion current could be restored after a pure hydrogen discharge. Therefore, practical long and stable operation was possible using periodic cleaning discharge.

Fig. 6.5 shows the dependence of substrate temperature rise on doping time with acceleration voltage and beam current as parameter. The temperature was measured by using a thermocouple pasted on the glass substrate. Too high a temperature rise caused damage to the resist and glass substrates. The temperature rose with doping time and ion beam energy (V_{acc} and j_{acc}). But under practical doping conditions used in this experiment such as V_{acc} of 500 V, j_{acc} of 0.25mA/cm², and doping time of 10-300 s, the substrate temperature was less than 100°C which is allowable for photoresist mask doping and other materials such as aluminum for metallization. By improving the contact between the holder and the substrate using gas cooling, the temperature rise can be reduced more effectively in higher energy doping.

6.2.2. Impurity activation

(1) Impurity profile in doped layer

In the basic study (Figs.6.6-6.9), a-Si film (typically 60 nm) was deposited by LPCVD and crystallized at 600°C. Doping was carried out without patterning of Si film. The substrate was dipped into 1 % HF aqueous solution to remove natural oxide. Doped phosphorous was activated without cap SiO₂ film by thermal annealing at 600°C for 1h in

N₂ or XeCl excimer laser pulse. The laser beam was homogenized by using a fly-eye lens integrator. The wavelength, beam area, puls duration, and beam uniformity were 308 nm, 8mm x 8mm, 28 ns, and $\pm 6\%$, respectively. Irradiation power was typically 200 mJ/cm². The overlap length of the laser beams was 0.2 mm. The overlap did not cause a nonuniformity of the sheet resistance [7].

Fig. 6.6 plots the phosphorus (³¹P) concentration profile in poly-Si film for a doping time of 10 s and also the maximum concentration dependence on doping time. For the 10-s doping, phosphorus concentration had a maximum value of $1.3 \times 10^{22}/\text{cm}^3$ (26 at %) at about 2-nm depth and it decreased exponentially with the depth. The projection range was too shallow to measure precisely but it was almost consistent with the doping energy [4]. A high-concentration tail was a peculiar feature and was considered to depend on lattice excitation resulting from ion bombardment [5]. Thus the technique was able to provide high-speed, very shallow, and high-concentration doping. The maximum concentration had its highest value at 30 s and decreased with doping time. A long-time doping reduced surface concentration and also film thickness (20 nm/1800 s). Chemical etching would be more dominant than sputter etching by proton with light mass.

Heavy metal impurities in doped single-crystal silicon were analyzed by SIMS. As expected, molybdenum (⁹⁶Mo) which is a component of the electron extraction electrodes and arc chamber wall was detected. In addition, chromium (⁵²Cr) and (⁴⁸Ti) were also detected. The intensity ratios of these three atoms for silicon were about 10^{-4} . The intensity of tungsten (¹⁸⁴W), a component of the thermal filament, was below the background level. Iron (⁵⁶Fe) and nickel (⁵⁸Ni), chamber materials, were not observed because of interference from ²⁸Si₂⁺ and ²⁹Si₂⁺ signals. Heavy metals such as Fe, Ni, Ti, and Cr generally make deep levels in silicon and become paramagnetic centers which can be observed by ESR. But in this sample, signals of Fe and Ni were not detected in the X-band at room temperature.

(2) Activation of doped phosphorus

Fig. 6.7 plots poly-Si sheet resistance dependence on excimer laser intensity at activation. The sheet resistance was sharply reduced at 150 mJ/cm² and decreased gradually when laser intensity was higher than this value. This was independent of dilution gas. The threshold energy was lower than that of the ion-implanted sample, probably because the heavily doped layer had a high absorption coefficient for the excimer laser. The surface of the poly-Si films became rough when the laser energy was too high. One shot irradiation was sufficient to activate doped phosphorus; multiple shots caused surface roughening. The tendency was the same as for the poly-Si layer implanted by P⁺ ions with a dose of $5 \times 10^{15}/\text{cm}^2$ at 20 keV. Therefore, one pulse annealing with 200 mJ/cm² was used for activation in this experiment.

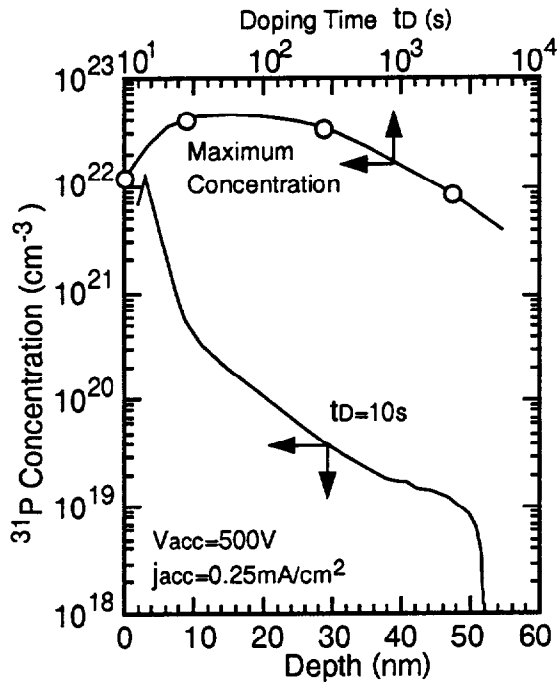


Fig. 6.6. Phosphorus concentration profile in poly-Si film and maximum concentration dependence on doping time.

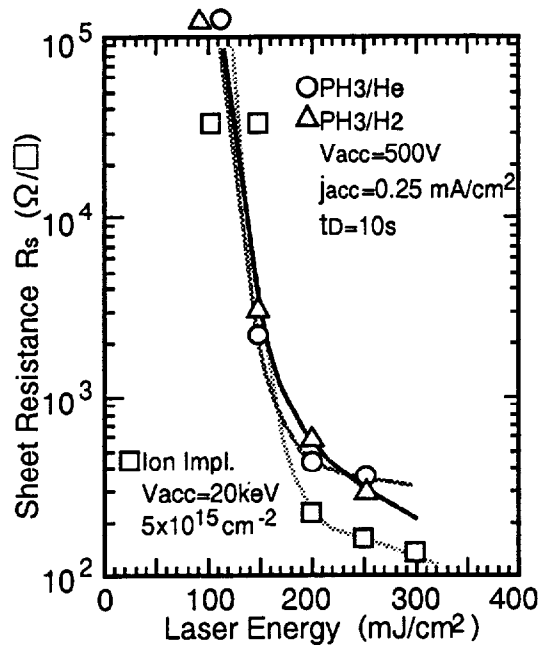


Fig. 6.7. Sheet resistance dependence of poly-Si on excimer laser energy at activation

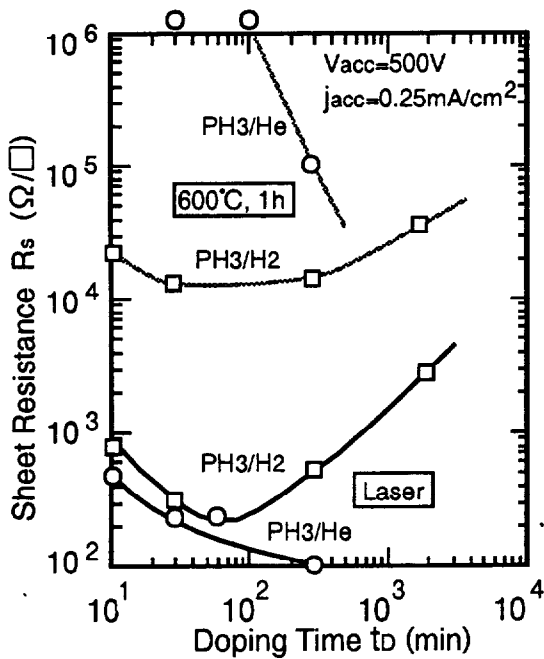


Fig. 6.8. Sheet resistance dependence of poly-Si on ion doping time with different dilution gases.

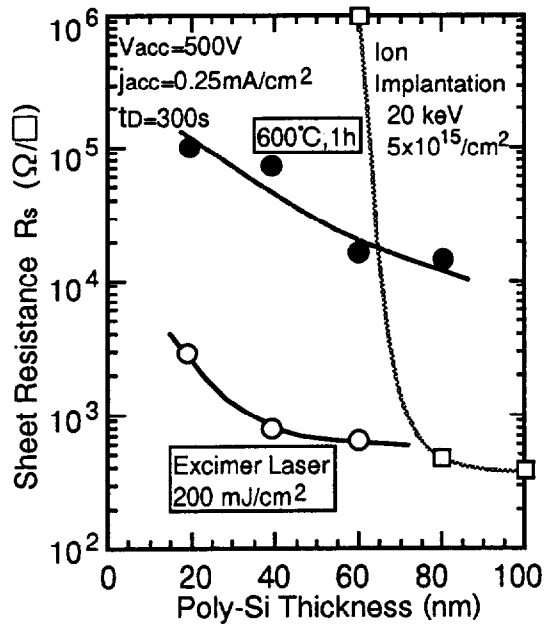


Fig. 6.9. Sheet resistance dependence on poly-Si thickness. Dopant: PH₃/H₂.

Fig. 6.8 shows sheet resistance dependence on ion doping time. As doping gases, PH_3/H_2 and PH_3/He were used. For comparison, the results of thermal annealing are also plotted. With PH_3/H_2 doping and laser activation, the sheet resistance decreased with doping time and showed a minimum value at 30 s, after which it increased. This behavior was considered to be caused by surface chemical etching reducing both film thickness and surface concentration as shown in Fig.6.6. With PH_3/He doping, the sheet resistance decreased with doping time and was 100 Ω/sheet at 300 s. It was assumed that surface etching was suppressed by using inert light He as a dilution gas. It was noteworthy that sheet resistances of 900 and 500 Ω/sheet were achieved with a doping time of 10 s for PH_3/H_2 and PH_3/He , respectively. The sheet resistance of gate poly-Si which was doped by PH_3/He without crystallization was about 1000 Ω/sheet . The uniformity of sheet resistance with PH_3/He at 10 s doping was $\pm 5\%$.

The sheet resistance values obtained by thermal annealing for PH_3/H_2 doping were about one order of magnitude higher than those by laser activation. Incomprehensively, for PH_3/He doping, the sheet resistances at 30 and 60 s were higher than $10^6 \Omega/\text{sheet}$, and but a value of only $10^5 \Omega/\text{sheet}$ was obtained at a doping of 300 s. This may imply that the appropriate amount of hydrogen supported activation.

Fig. 6.9 shows sheet resistance dependence on poly-Si thickness. For comparison, the values for ion implantation are also plotted. The sheet resistance increased with decreasing poly-Si thickness and was about 3000 Ω/sheet at 20 nm which was low enough for TFT operation. The values of thermal annealing were about one order of magnitude higher than the value of laser activation (Fig. 6.8). In ion implantation, sufficiently low values are obtained by 600 °C, 1-h annealing for poly-Si thickness of 80 and 100 nm. But at 60 nm, the value sharply rose to $10^6 \Omega/\text{sheet}$, marking the limit of shallow implantation with an acceleration voltage of 20 keV (lower limit of the machine). Therefore, techniques such as implantation through gate SiO_2 or deposition of thin SiO_2 cap for deceleration are necessary for thinner poly-Si film doping and TFT fabrication.

6.2.3 TFT fabrication process

Fig. 6.10 shows the low-temperatur poly-Si TFT fabrication process. A glass substrate (100mm x 100mm, 1.1 mm thick, Asahi AN) was SiO_2 coated by APCVD. Then poly-Si film (60 nm) was deposited by LPCVD at 550°C, 133 Pa and crystallized for 20 h at 600°C in N_2 . Gate oxide (100 nm thick) was deposited by APCVD at 550°C. After gate patterning, phosphorus was doped using the developed apparatus at V_{acc} of 500V and j_{acc} of 0.25 mA/cm². Doping times were 10, 30, and 300 s. Cap SiO_2 (100 nm thick) was deposited by APCVD to avoid roughening and contamination of the poly-Si layer in he laser activation process. After laser activation at 200 mJ/cm², PSG was deposited by APCVD for

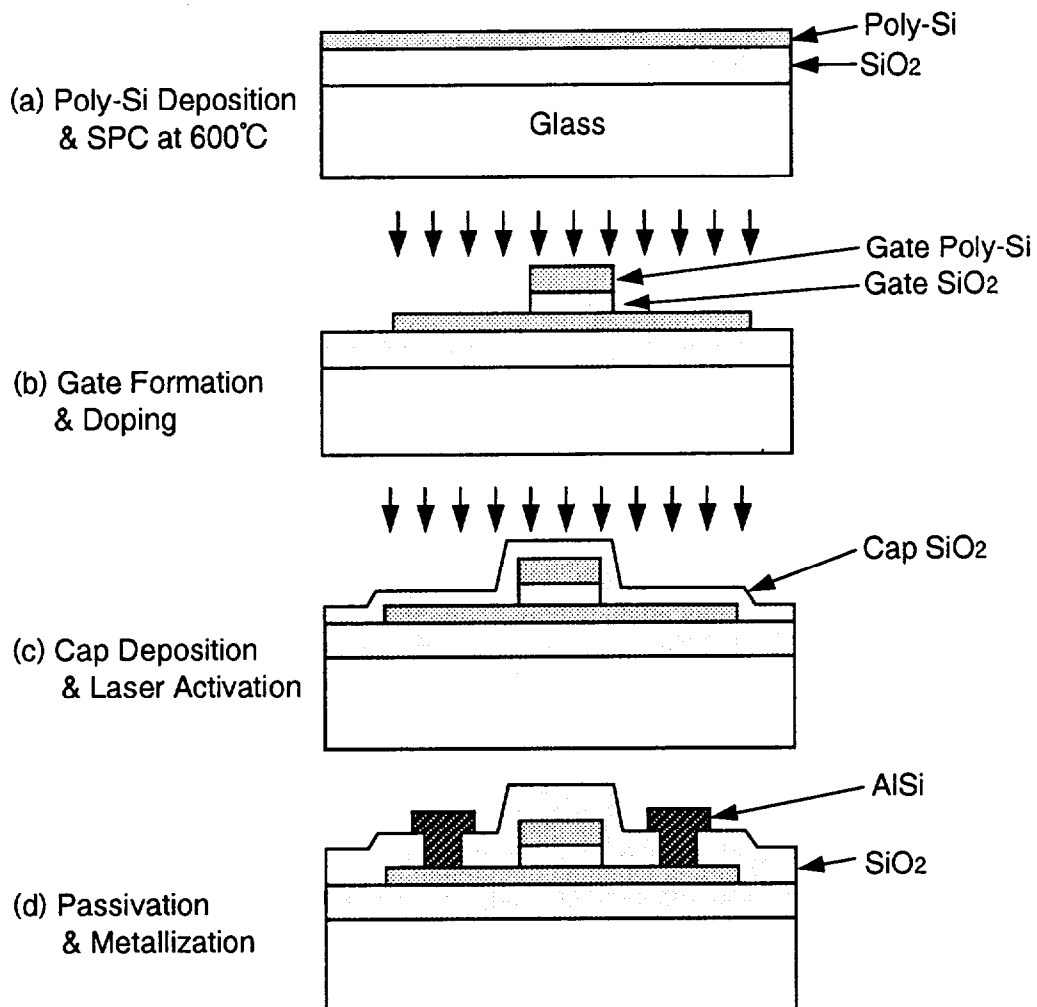


Fig. 6.10. Fabrication process for low-temperature poly-Si TFT.

Table 6.2 Fundamental characteristics of low-temperature poly-Si TFTs

(Doping gas: PH₃/He, TFT size: W/L=10/10(μm), V_{TH}: V_D=5V, I_{ON}: V_D=5V, V_G=20V, μ_{FE}: V_D=0.1V, I_{OFF}: V_D=5V, V_G=0V)

Doping Time	10s	30s	300s	Ion Implantation
Activation	Laser	Laser	Laser	600°C, 1h
V _{TH} (V)	5.6	5.3	5.0	9.4
μ _{FE} (cm ² /Vs)	22	28	28	26
I _{ON} (μA)	34	47	51	44
I _{OFF} (pA)	21	24	24	15

passivation and after contact windows were opened, AlSi was sputtered for metallization. Finally, hydrogenation was carried out using a pure hydrogen RF plasma at 300°C to improve device characteristics. For comparison purposes, P⁺ ions were implanted at 20 keV with a dose of $5 \times 10^{15}/\text{cm}^2$ and activated by thermal annealing at 600°C for 1 h. In implantation, 15-nm SiO₂ was deposited onto TFTs to decelerate and control the projection range of the P⁺ ions.

6.2.4 TFT characteristics

Fig. 6.11 shows V_G - I_D characteristics dependence on doping gas and doping time. The TFT doped by PH₃/He at 10 s operated normally the same as in Fig. 6.12. But the on-current of TFT doped by PH₃/H₂ was about 10⁻⁵ A and saturated at gate voltages higher than 20 V. Increasing the doping time to 300 s, the on-current was slightly improved, but still low compared with the TFT doped by PH₃/He at 10 s. The fabrication process was the same for all TFTs, except for the doping gas. Therefore, the difference of the on-characteristics was assumed to depend only on the difference of doping phenomena or doped surface characteristics between PH₃/He and PH₃/H₂. Possible reasons are an increase of Al contact resistance or sheet resistance of source and drain for PH₃/H₂ doping in the activation with cap SiO₂, caused by absorption of phosphorus into cap SiO₂ to make PSG.

Fig. 6.12 shows V_G - I_D characteristics dependence on doping time. It was noteworthy that the TFT fabricated with a doping time of 10 s had comparable characteristics with TFTs fabricated with longer time dopings and conventional ion implantation. Generally, in these devices, the subthreshold characteristics are improved for laser-activated ones. It was considered that high-temperature treatment by laser activation for gate poly-Si, gate SiO₂, and the active poly-Si would improve their interface characteristics. Table 6.2 shows fundamental characteristics of TFTs (mean values). The TFT with 10-s doping had slightly inferior on-characteristics compared with the other TFTs. As the doping time decreased from 300 to 10 s, V_{TH} increased, and μ_{EF} , I_{ON} , and I_{OFF} decreased. The μ_{FE} had slight dependence on channel length at $L=10 \mu\text{m}$ region implying the effect of parasitic resistance on conduction. Therefore, degradation of on-characteristics in short-time doping would be caused by slight increase of sheet resistance of the source and drain as in Fig. 6.8. The sheet resistance should be improved by using high-density and high-voltage doping conditions.

6.2.5 Doping for TFTs with PECVD Si

The previously mentioned low-temperature poly-Si TFTs uses LPCVD Si for active layer. But considering TFTs on large-area glass substrates, PECVD Si is useful for providing precursor of active layer poly-Si [13],

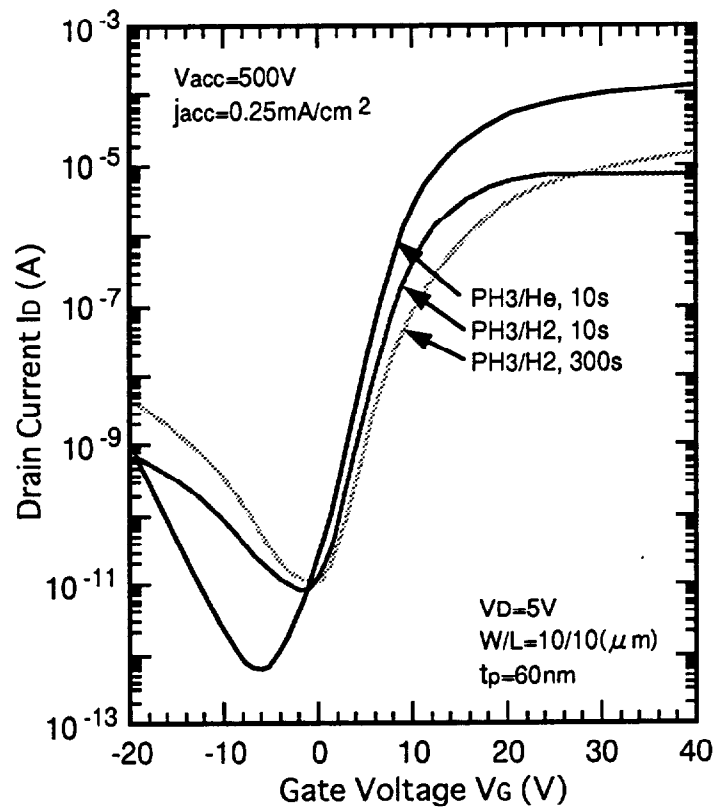


Fig. 6.11. Dependence of V_G - I_D characteristics of poly-Si TFTs on dilution gas and doping time.

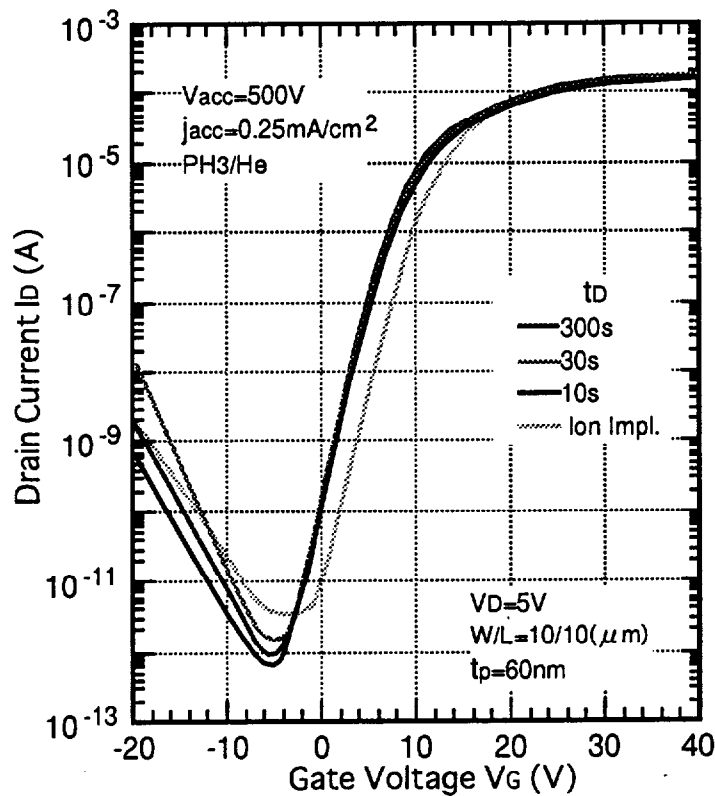


Fig. 6.12. Dependence of V_G - I_D characteristics of poly-Si TFTs on doping time.

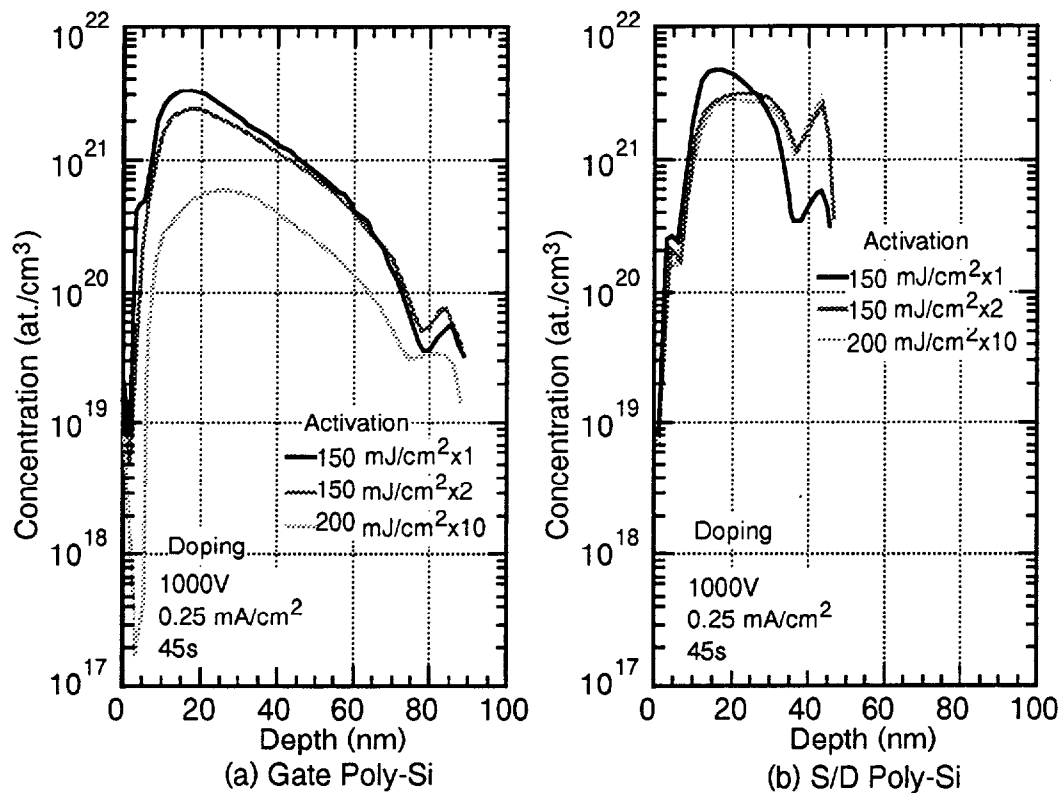


Fig. 6.13. Phosphorus concentration profiles in poly-Si TFTs using PECVD Si. Dopant: PH_3/He .

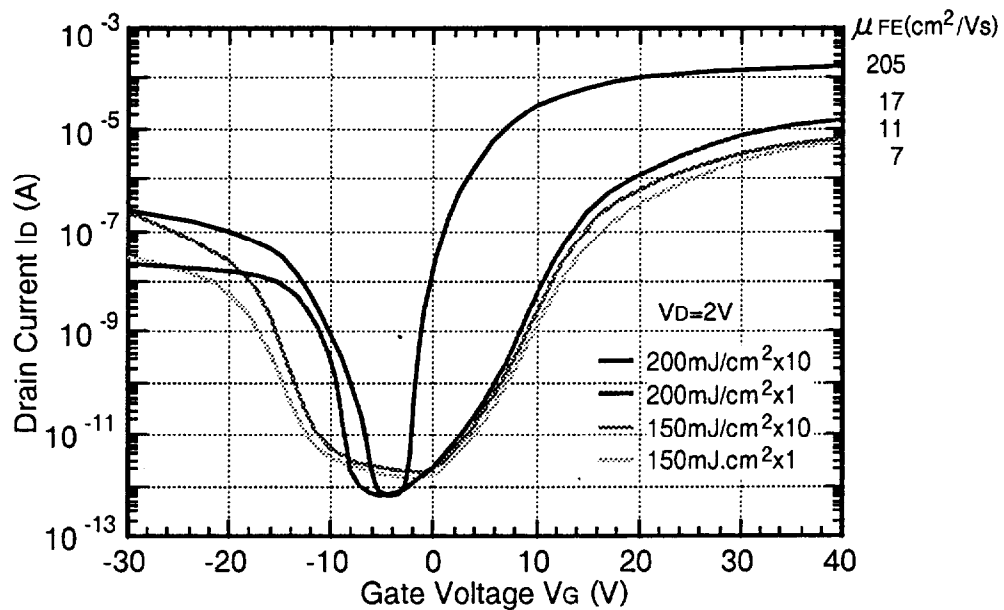


Fig. 6.14. Dependence of V_g - I_d characteristics on activation conditions in poly-Si TFTs using PECVD Si.

[14]. Ion doping for poly-Si obtained by the laser crystallization of PECVD Si with 50 nm thick was also studied.

Fig. 6.13 shows phosphorus concentration profiles in poly-Si TFTs using laser crystallized PECVD Si. The total and maximum concentrations decreased with increasing activation laser energy for both gate-poly-Si and source and drain poly-Si. The results also proved that the total content of phosphorus was reduced by laser irradiation as described later (section 6.4). The sheet resistances of source and drain, and gate were 800 and 400 Ω /sheet, respectively.

Fig. 6.14 shows dependence of V_G - I_D characteristics on laser activation conditions. By increasing laser energy and shot numbers, on-characteristics were remarkably improved and the highest mobility of 205 cm^2/Vs was obtained at 200 mJ/cm^2 and 10 shots. The optimum activation energy and shot number should recover ion doping damage and achieve sufficient activation, and also should improve characteristics of SiO_2 -poly-Si interface.

6.3 Large-area ion doping with 100mm x 400mm ion source

6.3.1 Ion doping for 350mm x 450mm substrates

(1) Concept for large-area doping

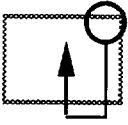
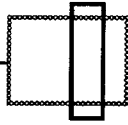
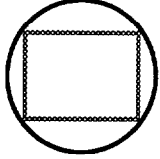
The bucket-type ion source itself has an ability to increase machine scale to at least a 580-mm diameter [9]. One-shot irradiation for large substrates would be possible using the large ion source. But total performance must be considered, including maintenance of the apparatus for mass-production.

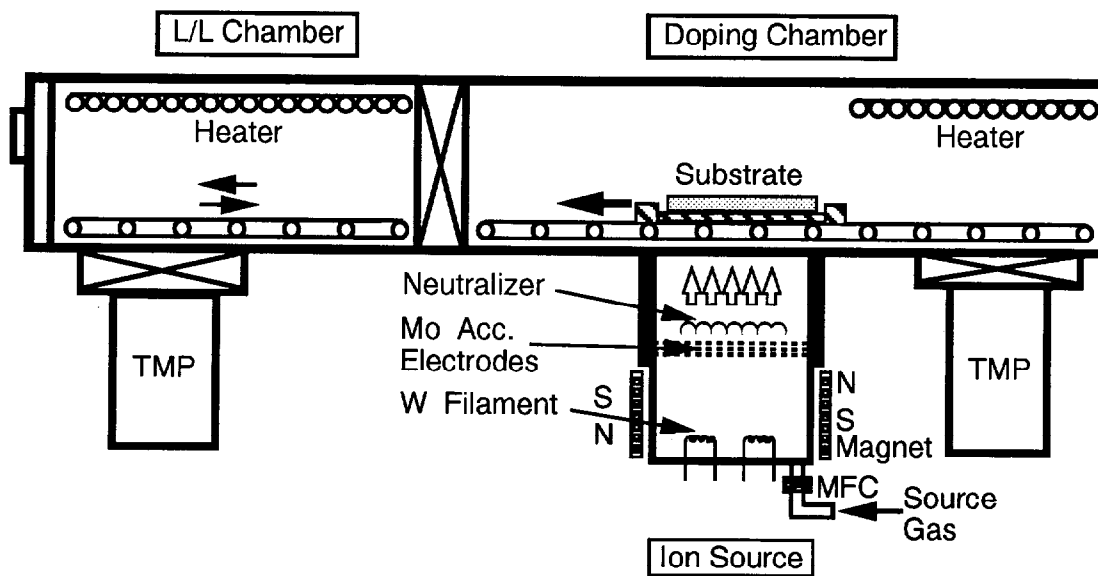
Table 6.3 summarizes the performances of three ion sources for large glass substrates such as to 1 m square. (a) uses the spot ion source described in section 6.2 and the beam is scanned over the substrate. The small size of the ion source is convenient for operation but uniformity of dose and throughput are insufficient. (c) uses a large-area ion source for one-shot irradiation. A 10-s doping should be possible for 1 m square substrate, but machine maintenance would be a problem. The compact linear ion source and substrate scanning should be reasonable for treating large substrates as shown in (b). In this section, the 100mm x 400mm ion source for 350mm x 450mm substrates which is the second generation size for a-Si TFT-LCD production, was developed.

(2) Structure of doping apparatus

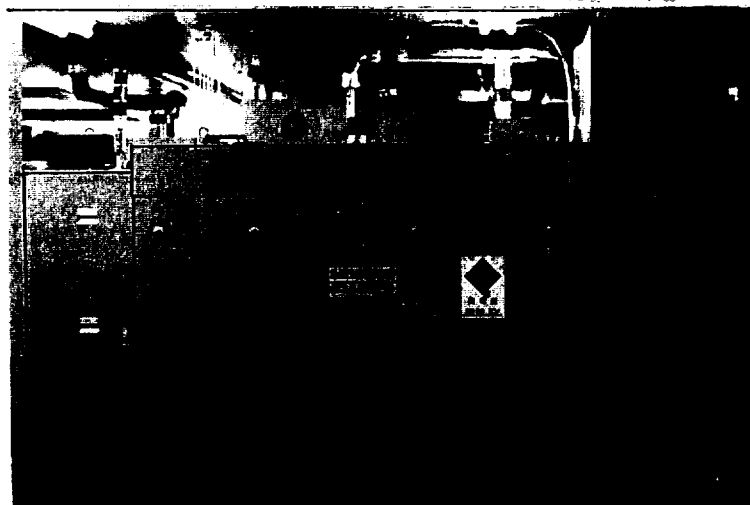
Fig. 6.15 shows a schematic and photograph of the developed doping apparatus. The bucket type ion source with a size of 100mm x 400mm was attached on the bottom of the doping chamber. The arc discharge chamber consisted of two tungsten filaments for the thermal electron source, permanent magnets, and three-layer ion extraction electrodes. A high-density and uniform discharge plasma was formed by thermally emitted electrons and the cusp field of the permanent magnets, set outside

Table 6.3 Performance of three ion sources for large substrates

Ion Source	(a)Spot	(b)Linear	(c)Large Area
	X-Y Scan	Y-Scan	One Shot
Irradiation			
Throughput	low	intermediate	high
Machine Size	small	intermediate	large
Uniformity	not good	intermediate	intermediate



(a) Schematic structure of ion doping apparatus.



(b) Photograph of front view.

Fig. 6.15. Developed ion doping apparatus with 100mm x 400mm linear ion source.

of the chamber. The ion beam was extracted from the arc discharge chamber and accelerated and irradiated onto a sample without mass separation. The maximum acceleration voltage was 20 kV. The glass substrate could be transported horizontally in its longitudinal direction through the beam. It was supported by an aluminum holder and irradiated from below.

(3) Doping and activation conditions

Fig. 6.16 plots the arc current dependence on filament current. V_{arc} and V_{acc} were fixed at 100V and 5kV, respectively. I_{acc} rapidly increased when I_{fil} exceeded 37 A and reached at 2.5A at I_{fil} of 39A. Fig. 6.17 plots the dependence of beam current on I_{arc} . A j_{acc} of 200mA was obtained at I_{arc} of 2.5 A. Fig. 6.18 plots the beam current dependence on filament current. In actual operation, ion beam was set by filament current control. The condition j_{acc} of 200mA corresponded to the ion beam density of 0.5 mA/cm². Ion beam characteristics comparable to those of the 150-mm diameter ion source, were achieved in this large area ion source. The ion beam density is about two orders of magnitude higher than that of conventional ion doping apparatus [12].

Fig. 6.19 show the substrate scanning methods. The substrate was transported in its longitudinal (Y) direction. The doping time was defined as the time required for length of 100 mm to pass through the ion source. It was controlled by the substrate transportation speed. The doping condition to realize 10-s doping and treatment time for 350mm x 450mm substrate were estimated as follows.

$$\text{Transportation speed } 100 \text{ mm} / 10 \text{ s} = 10 \text{ mm/s} \text{ -----(6.1)}$$

$$\text{Treatment time } (450+100)(\text{mm})/10(\text{mm/s}) = 55 \text{ s} \text{ -----(6.2)}$$

The throughput should be sufficient for mass-production.

Tables 6.4 and 6.5 summarize the ion doping conditions and laser activation conditions, respectively. Typical V_{arc} , I_{arc} , V_{dec} , I_{neu} were 100V, 2A, 280V, and 350 mA, respectively. Typical doping conditions were 1 kV for 45 s and 5 kV for 6-10s. Laser activation was carried out in the vacuum chamber at room temperature and 350°C using the apparatus shown in Fig.5.5.

6.3.2 Doping and activation characteristics

(1) Effect of doping conditions on sheet resistance

Fig. 6.20 plots the dependence of sheet resistance on activation energy, V_{acc} , at two doping times. Long-time doping realized low sheet resistance and high-energy activation caused the increase of sheet resistance because of poly-Si film damage. Precise relations between doping condition and activation are discussed later.

Fig. 6.21 shows sheet resistance dependence on doping time for three V_{acc} values. At V_{acc} of 1-3 kV, sheet resistance normally decreased with

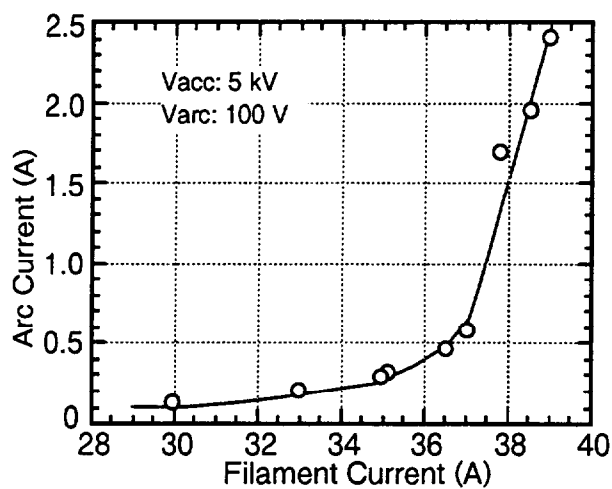


Fig. 6.16. Arc current dependence on filament current in ion source.

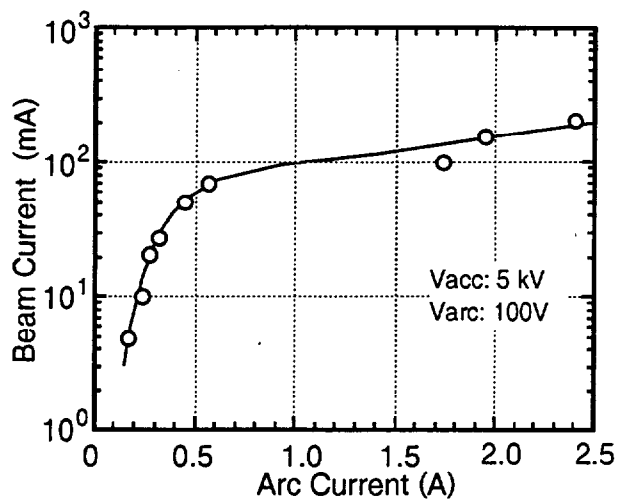


Fig. 6.17. Beam current dependence on arc current in ion source.

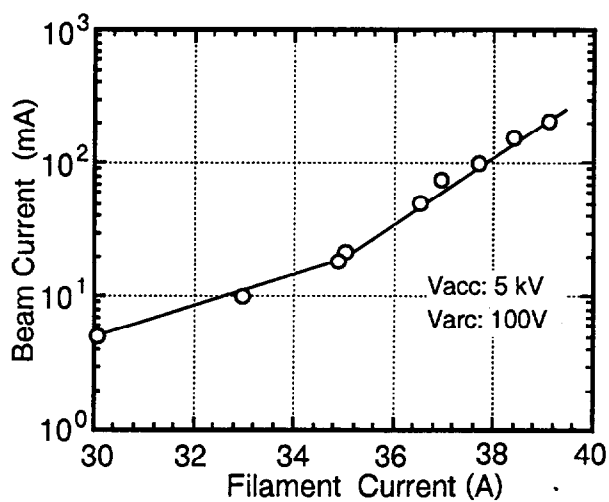


Fig. 6.18. Beam current dependence on filament current in ion source.

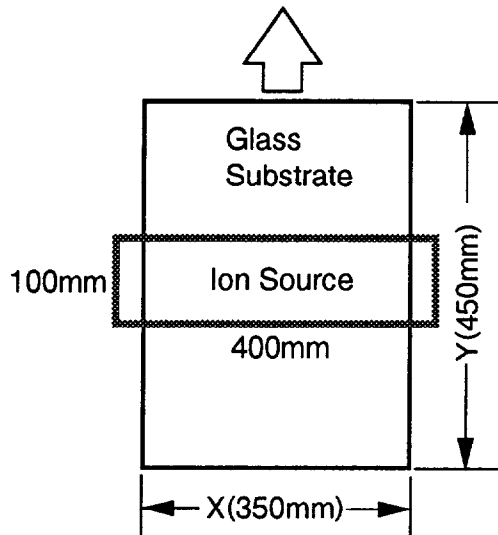


Fig.6.19. Substrate scanning method.

Table 6.4 Ion doping conditions

Ion Beam Size	100 mm x 400 mm
Ion Beam Density	0.125, 0.5 mA/cm ²
Acceleration Voltage	1.0 - 5.0 kV
Source Gas	PH ₃ , B ₂ H ₆ (1%)/He
Irradiation Time	6 - 45 s

Table 6.5 Laser activation conditions

Laser Energy	150-250mJ/cm ²
Beam Size	8mmX8mm
Shot Number	10-40 shots
Sub. Temperature	25 °C, 350°C
Pressure	2.7 Pa

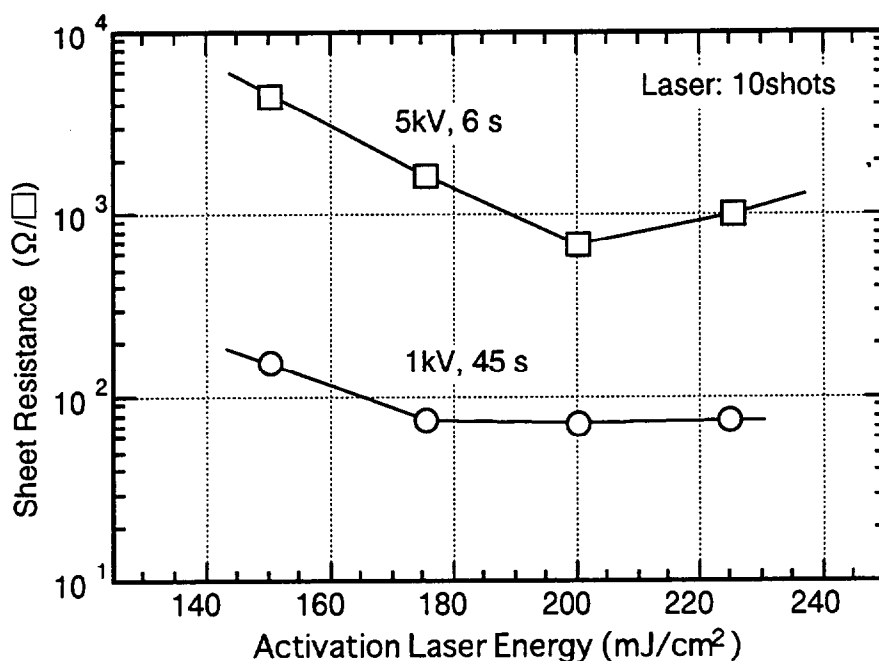


Fig. 6.20. Dependence of sheet resistance on activation energy in phosphorus doping.

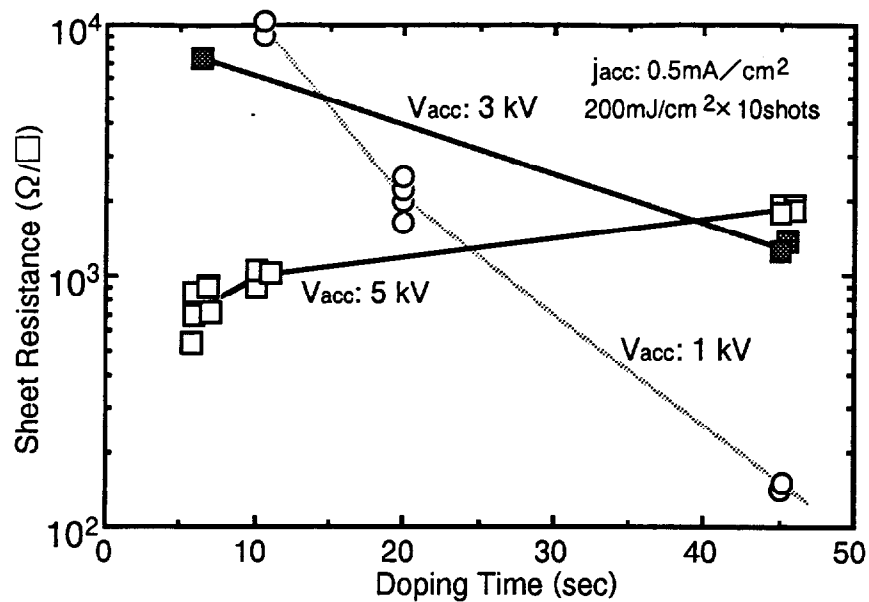


Fig.6.21. Dependence of sheet resistance on doping time in phosphorus doping.

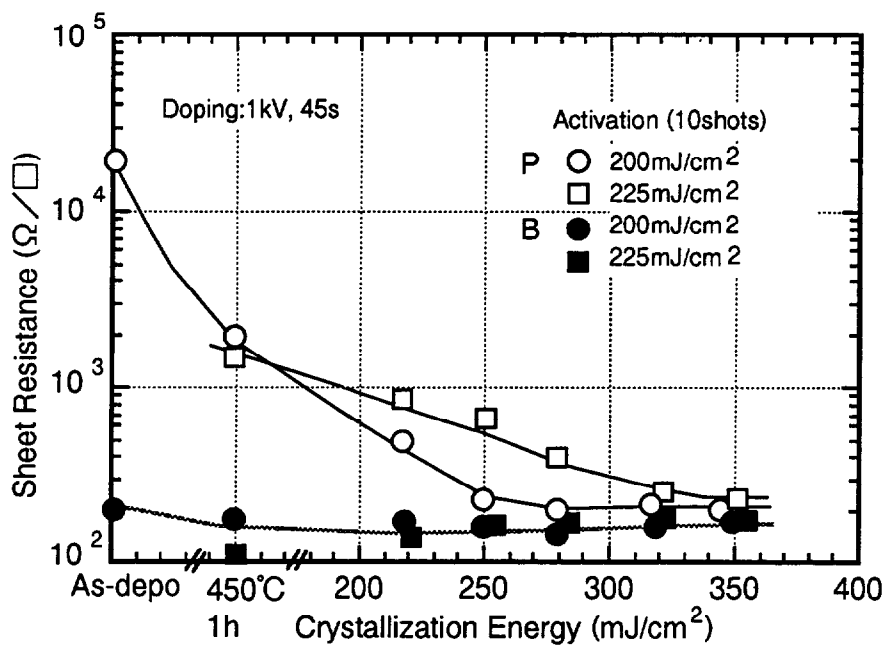


Fig. 6.22. Dependence of sheet resistance on crystallization conditions in laser activation.

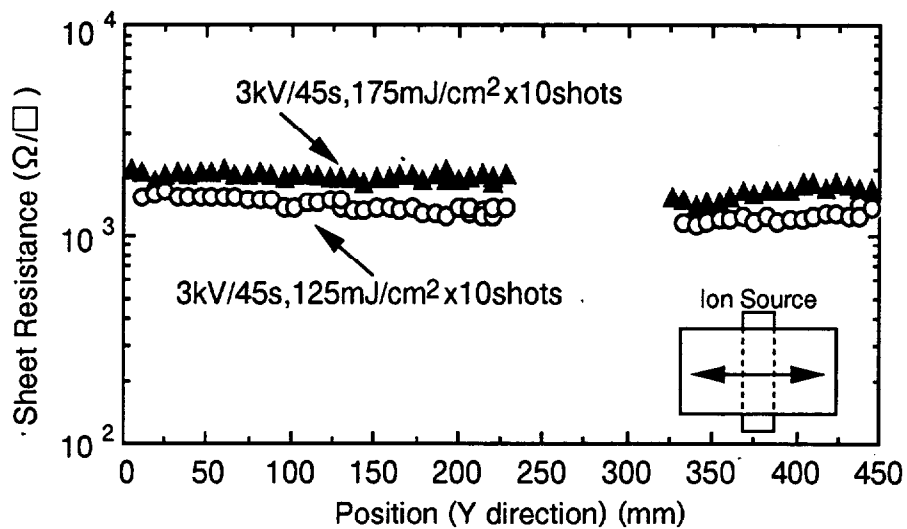


Fig. 6.23. Sheet resistance uniformity in substrate scanning Y direction.

increasing doping time. But at 5 kV, sheet resistance slightly increased with increasing doping time because poly-Si film was damaged by ion bombardment.

Fig. 6.22 shows dependence of sheet resistance on crystallization conditions of poly-Si film. In phosphorus doping, sheet resistance critically depended on crystallization conditions and decreased with increasing crystallization energy, namely with increasing crystallinity. The laser activation also contributed to promote crystallization of poly-Si, but initial crystallinity affected the sheet resistance. In boron doping, initial crystallinity had hardly any effect on sheet resistance. It was supposed that phosphorus doping degraded crystallinity and pre-crystallized poly-Si supported recovery of crystallinity in laser activation. In activation of boron doping, crystallization was promoted fairly well for all poly-Si films.

(2) Uniformity of sheet resistance

Fig. 6.23 plots the sheet resistance profile in the substrate longitudinal direction Y, that is the substrate transportation direction. The center region without data was used for evaluation of lateral direction. The profile was very uniform implying that very constant doping was possible when the ion beam and transportation were stable.

Fig. 6.24 plots uniformity of sheet resistance in the substrate lateral direction for phosphorus doping. For reference, ion currents measured by Faraday cup and poly-Si film thickness are also plotted. The ion source had two moderate peaks for each of the V_{acc} curves, 1kV and 5kV. The ion source had two filaments as shown in Fig. 6.15. But the intensity peak position did not agree with their positions. So nonuniformity of profile may depend on the nonuniformity of the acceleration electrode gaps caused by deformation of electrodes due to heat of the plasma or filaments. A uniform profile should be gotten by optimizing the electrodes structure. The area of high ion beam intensity indicated low sheet resistance because of its high phosphorus content. Low enough sheet resistance below $1\text{k}\Omega/\text{sheet}$ was obtained also for 6 and 10s doping at 5kV. A 6-s doping corresponded to the substrate transportation speed of 1m/min which was feasible for production process.

Fig. 6.25 shows uniformity of sheet resistance in X direction for boron doping. The area of high ion beam intensity also indicated low sheet resistance because of its high boron content. Low enough sheet resistance below $1\text{k}\Omega/\text{sheet}$ was obtained also for 6-s doping at 5kV.

Fig. 6.26 shows photographs of surface poly-Si films in the beam overlap area after laser activation for phosphorus and boron doping. In both doping and activation conditions, beam overlap areas were smooth and no damage was observed.

Fig. 6.27 plots the sheet resistance profile in the beam overlap area in laser activation in phosphorus and boron doping. In phosphorus doping, sheet resistance varied from 1600 to $2200\ \Omega/\text{sheet}$. Higher uniformity

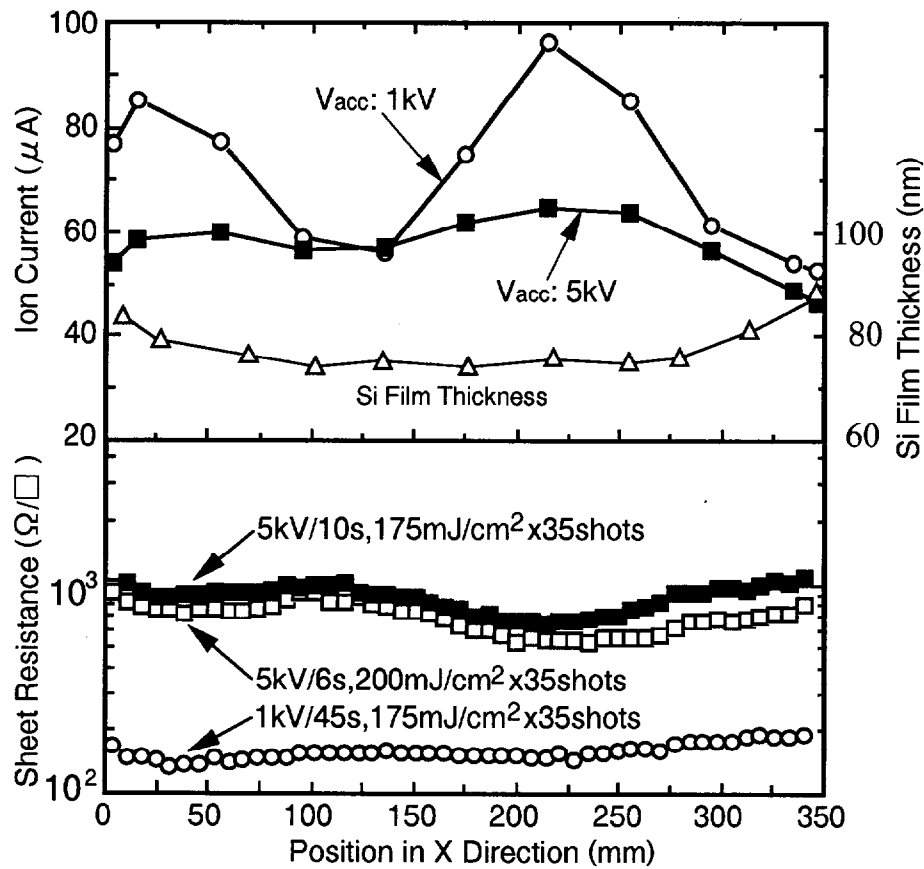


Fig. 6.24. Uniformity of ion current and sheet resistance in X direction for phosphorus doping and activation.

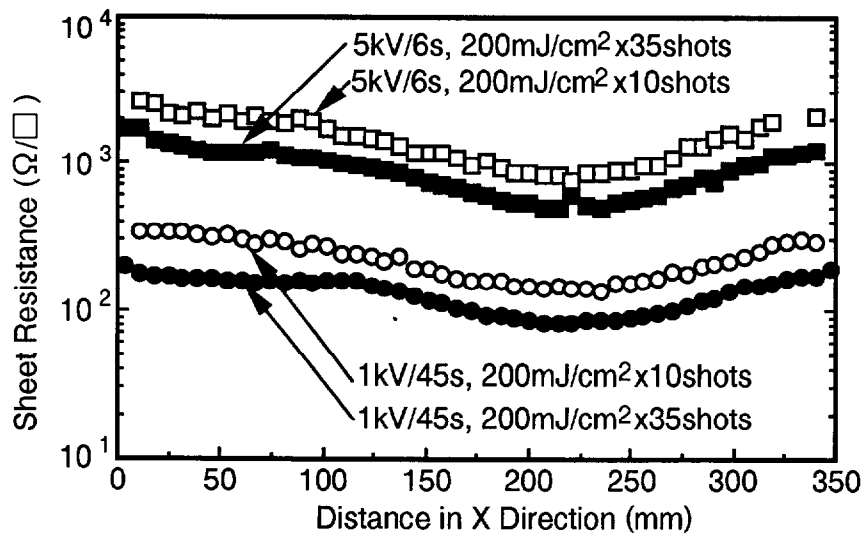


Fig. 6.25. Uniformity of sheet resistance in X direction for boron doping and activation.

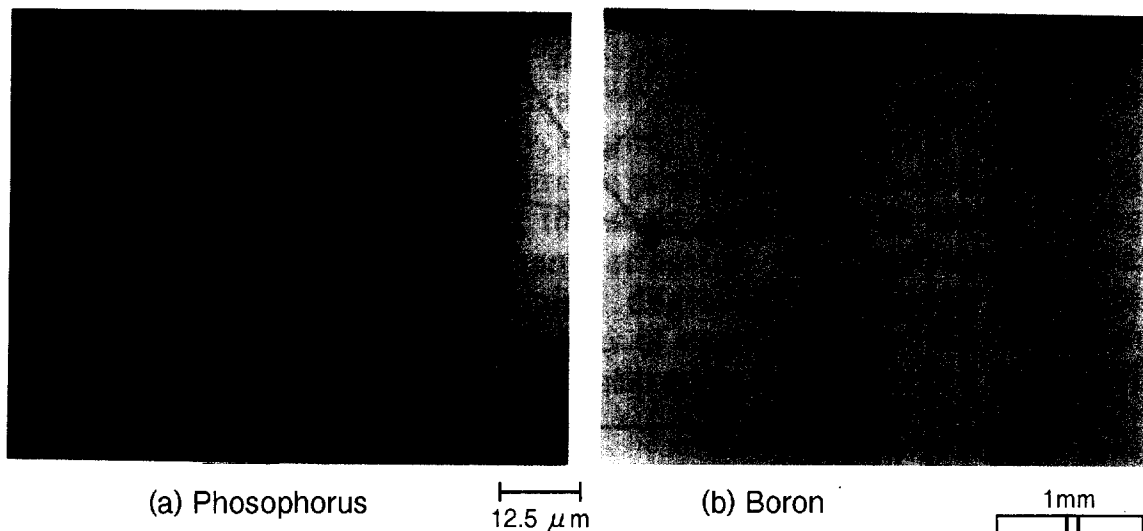


Fig. 6. 26. Photographs of poly-Si films after laser activation in beam overlap area.

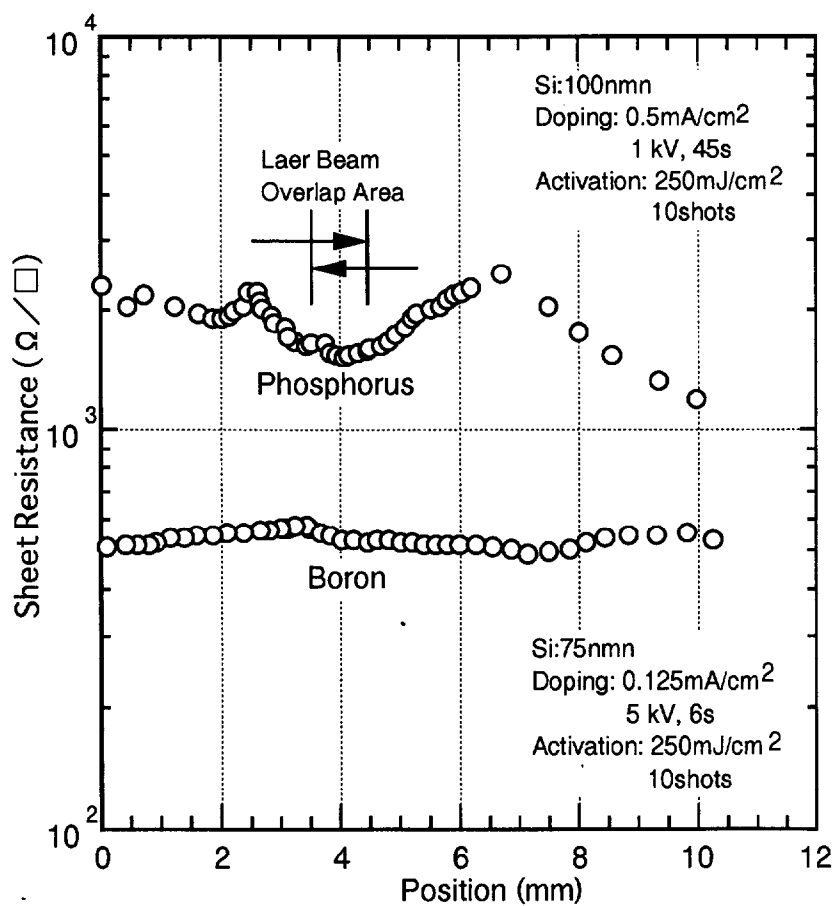


Fig. 6.27. Uniformity of sheet resistance in laser beam overlap area.

should be possible by using uniform line beam and fine pitch scanning. In boron doping, a uniform profile was obtained.

6.4 Doping mechanism in ion doping and laser activation

6.4.1. Dopant profiles measured by SIMS

Fig. 6.28 shows the dependence of concentration profiles of phosphorus and hydrogen on laser activation energy. Significantly, phosphorus concentration decreased exponentially in the as-doped profile the same as for the small-size ion source mentioned in section 6.2. Secondly, total content increased for activation at 150 mJ/cm², but profiles became lower and flatter with increasing laser energy. The results implied there was dopant source on the surface and the source was evaporated by too high energy irradiation. The hydrogen content decreased with increasing laser energy indicating that dehydrogenation was enhanced.

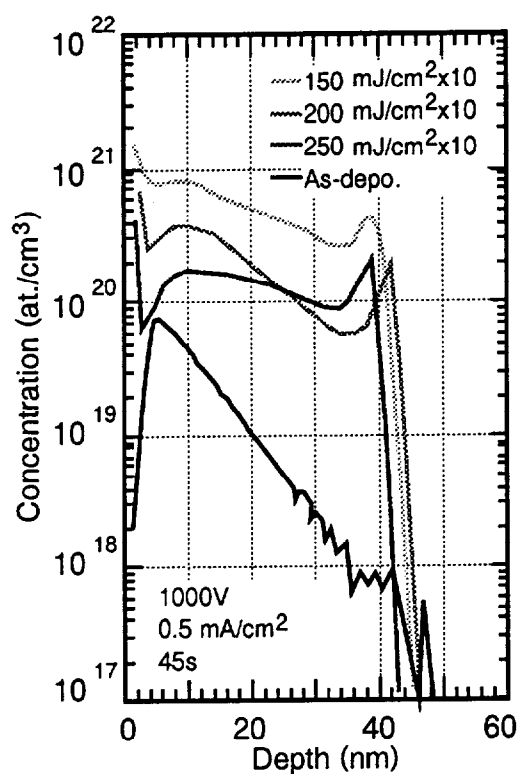
Fig. 6.29 shows dependence of phosphorus concentration on laser shot number. In 150 mJ/cm² activation, total content was dramatically increased and the profile became flat when shot number increased from 1 to 10. For 250 mJ/cm², the profile became very flat, but total content was slightly increased. These results also implied the presence of dopant source on the surface and evaporation of source by high energy laser.

Fig. 6.30 shows dependence of phosphorus concentration profiles on laser activation conditions in 5 kV, 6 s doping. A high concentration profile was still obtained. When the laser energy was increased, the profile became flat but total content was almost constant because projection range was deep enough and evaporation was suppressed. The total content of hydrogen was also decreased by laser activation.

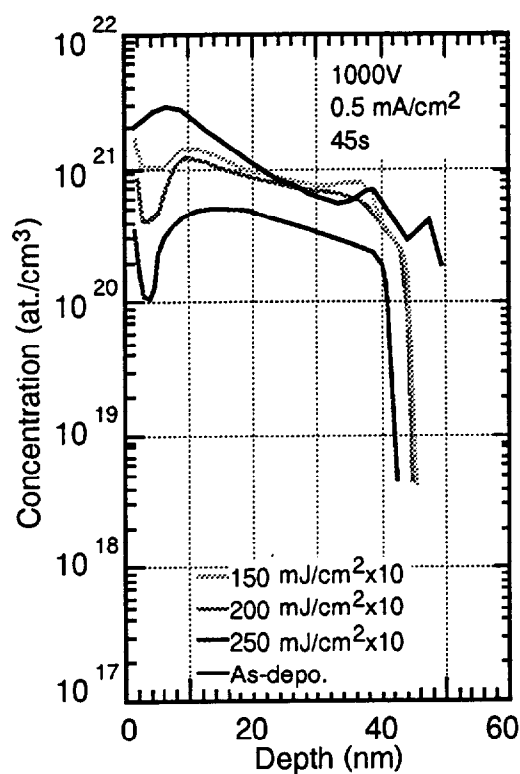
Fig. 6.31 shows dependence of boron concentration profile on laser activation conditions. In the as-doped profile, concentration decreased exponentially too. For the 1 kV, 45 s doping, the profile became very flat after laser activation but total content was almost constant. For the 5kV, 6 s doping, the profile showed clear peaks and boron diffused into the bottom, but total content was also constant. In the boron doping, evaporation was suppressed during laser activation because boron had a somewhat deep projection range.

6.4.2. Surface observation by SEM

Fig. 6.32 shows SEM micrographs of poly-Si surfaces after laser irradiation in phosphorus doping. For a very low energy, long time doping (1 kV, 45s) as shown in (a), partial peeling of the thin deposited layer was observed. The peeled layer may be the deposited phosphorus layer or heavily doped silicon layer. For a slightly higher energy, short time doping (5kV, 6s), peeling was not observed ((b)). Ridges which originated from the melt and solidification process in laser activation, were observed. These phenomena were also observed in boron doping.

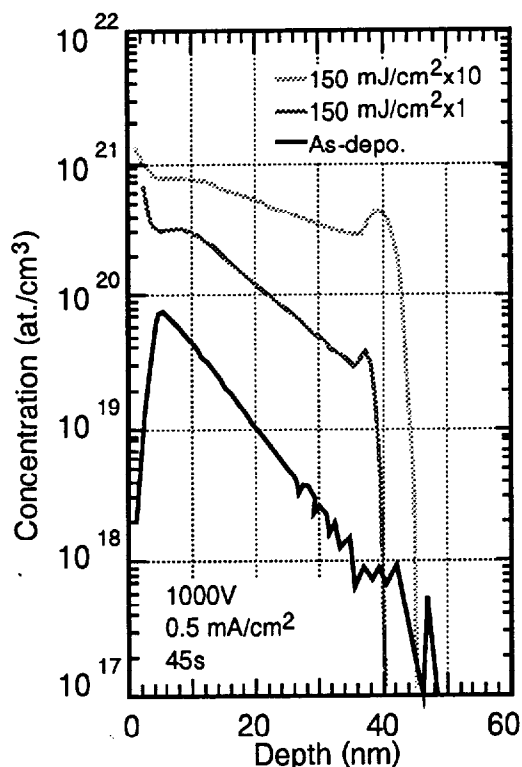


(a) Phosphorus

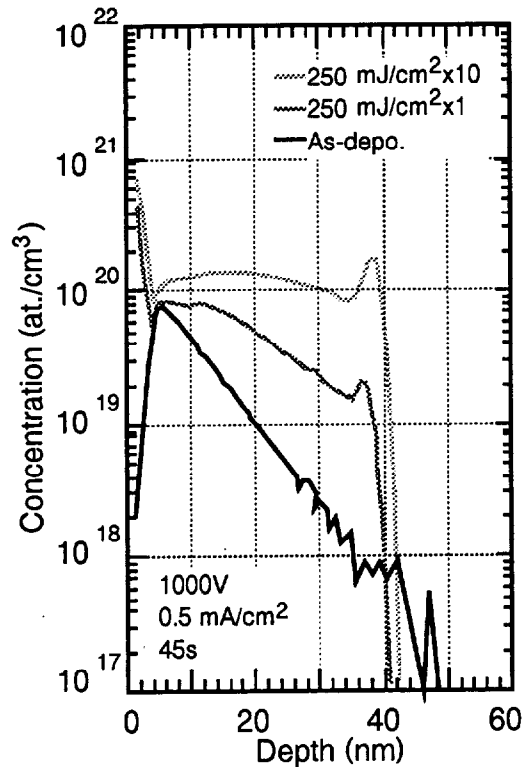


(b) Hydrogen

Fig.6.28. Dependence of phosphorus and hydrogen concentration profiles on laser activation conditions.

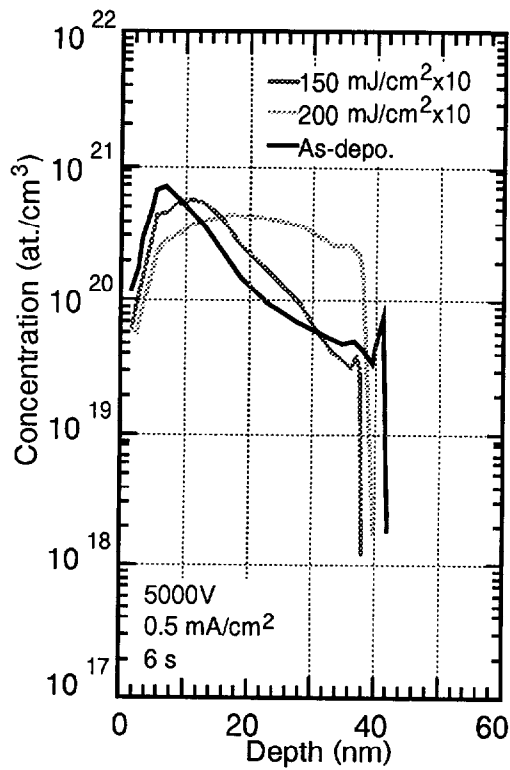


(a) Activated at 150 mJ/cm²

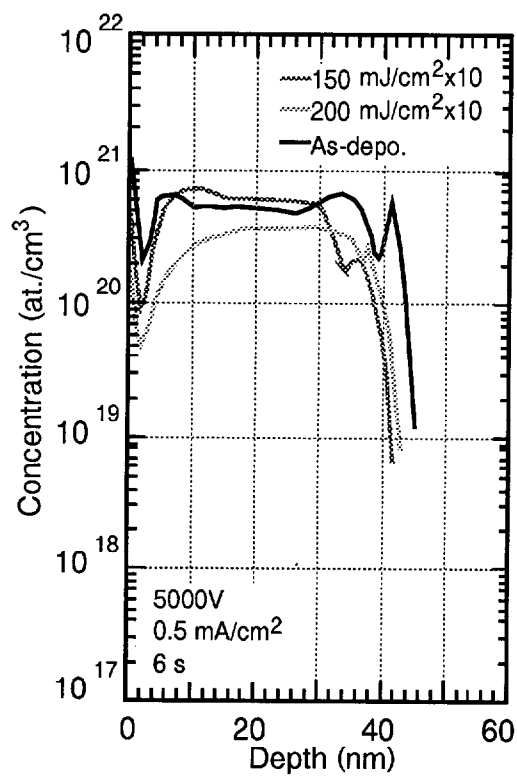


(b) Activated at 250 mJ/cm²

Fig.6.29 Dependence of phosphorus concentration profiles on laser shot numbers.

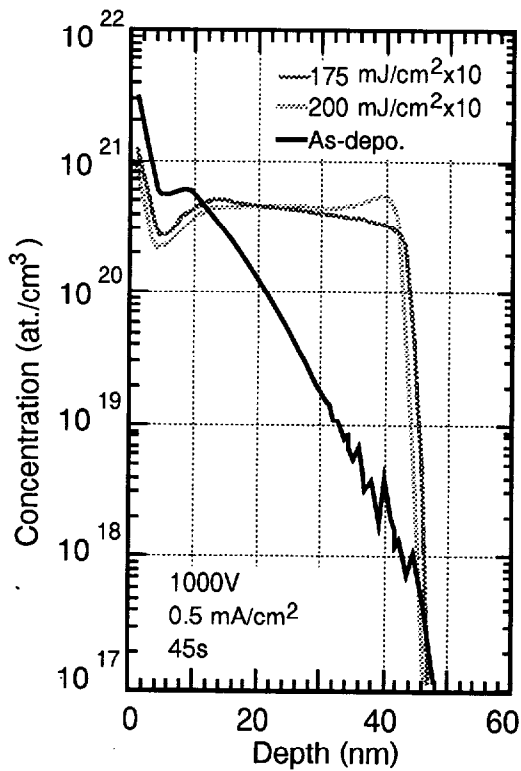


(a) Phosphorus

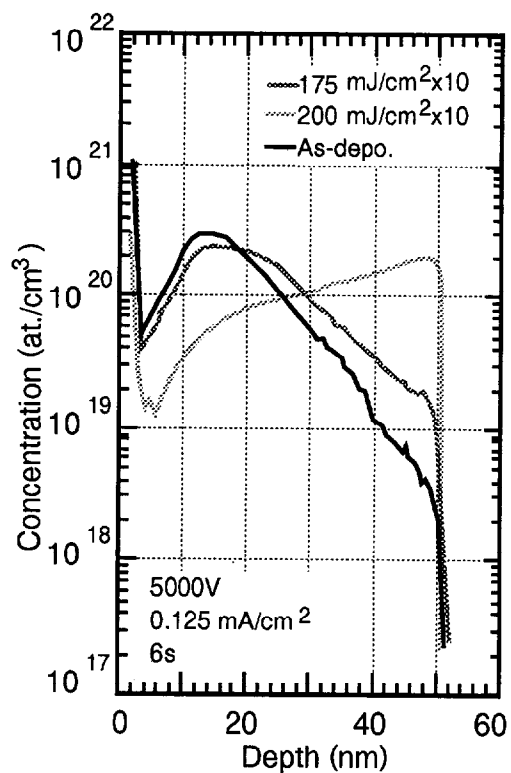


(b) Hydrogen

Fig.6.30. Dependence of phosphorus concentration profiles on laser activation conditions in 5 kV, 6s doping.

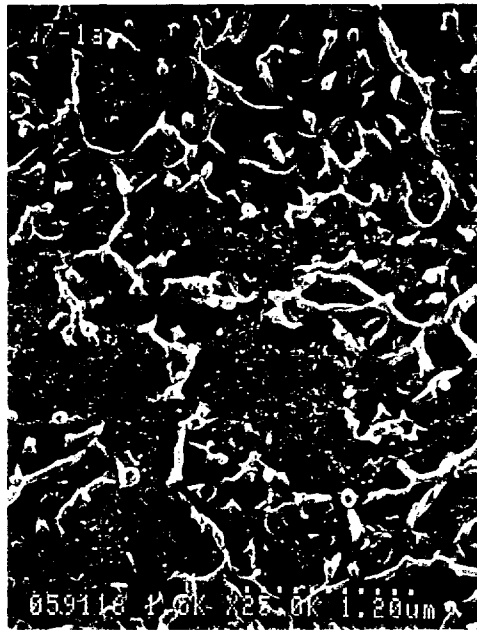


(a) Doping: 1 kV, 45s

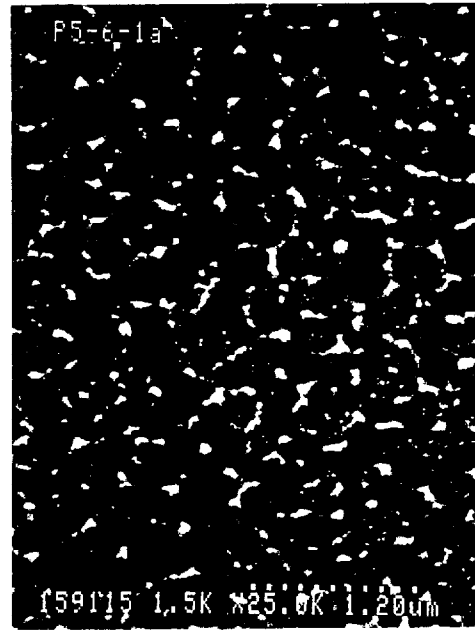


(b) Doping: 5 kV, 6s

Fig.6.31. Dependence of boron concentration profiles on laser activation conditions.



(a) Doping: 1 kV, 45 s
Activation: 150mJ/cm²



(b) Doping: 5 kV, 6 s
Activation: 150mJ/cm²

Fig. 6.32. SEM micrographs of poly-Si surface after laser activation.

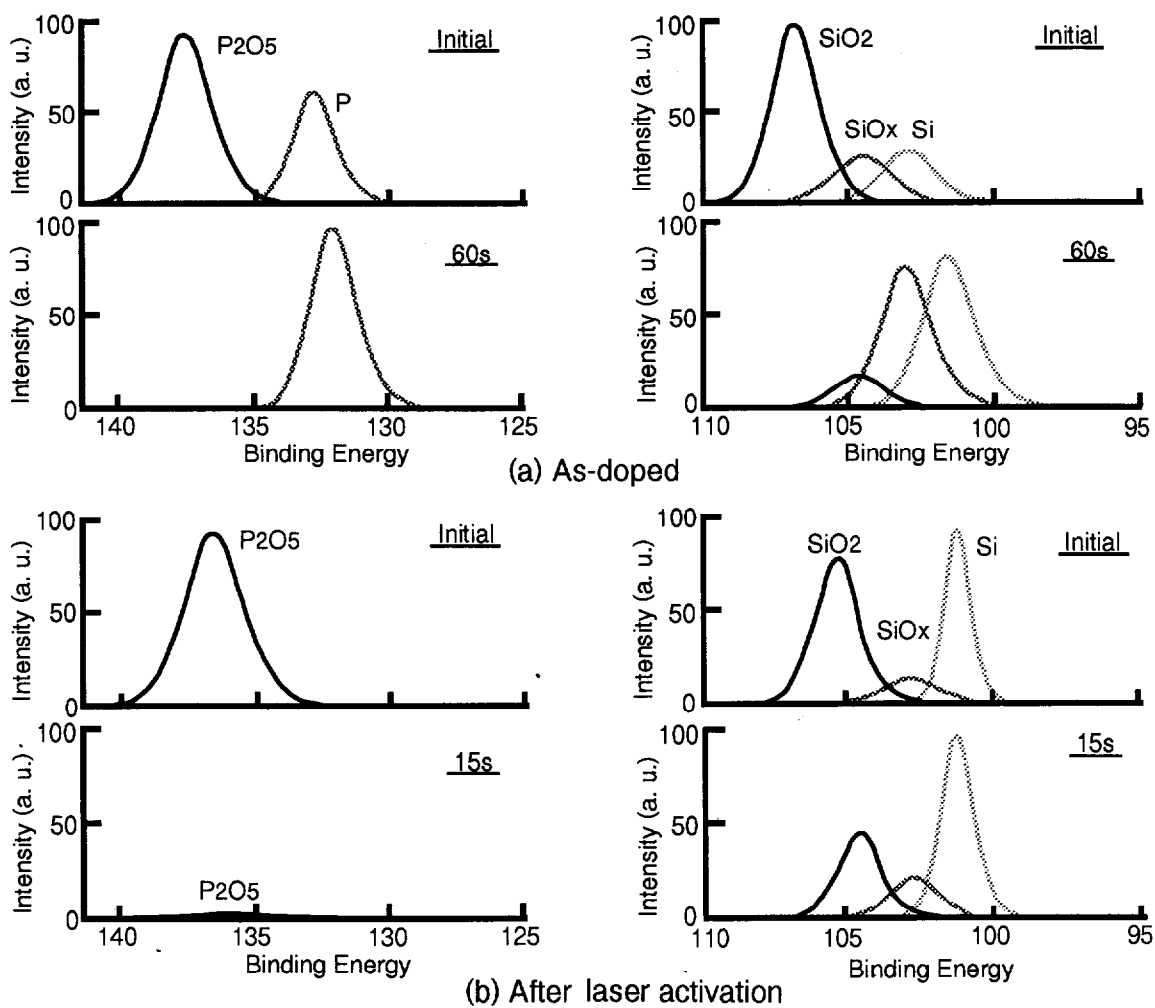


Fig.6.33. XPS profiles of phosphorus and Si before and after laser activation.
Doping: 1kV, 45s. Activation: 200mJ/cm², 10shots.

6.4.3. Chemical bonding states of dopants observed by XPS

Fig. 6.33 shows XPS profiles of phosphorus and Si in as-doped Si film ((a)) and laser activated film (b). Binding energy profiles were measured by step etching with low energy Ar ions. Etching depth after 1 min was about 1-2 nm. After doping, phosphorus and its oxide were clearly observed. This indicated the existence of the thin phosphorus layer and its surface oxidation. The results also implied that the silicon was excessively doped and there was a possibility for shorter time doping to reduce deposition. SiO_2 was also observed, indicating the existence of natural oxide without reduction. As in Fig. 6.33 (b), after laser activation, only trace phosphorus oxide was observed and natural silicon oxide was partially destroyed. For the 5kV, 6 s doping, the same XPS analysis showed that the deposited phosphorus amount was less and natural oxide was almost completely destroyed.

6.4.4. Laser activation at 300°C

Fig. 6.34 shows dependence of sheet resistance on laser activation energy for different conditions of boron doping and activation. For the 1 kV, 45 s doping, sheet resistance at 300°C activation was higher than the value at 25°C activation. By contrast, in the 5kV doping, sheet resistance decreased at 300°C activation. And sheet resistance of 1 k Ω /sheet was obtained at 0.125 mA/cm² and 6 s doping which corresponded to the doping of 1.5 s at 0.5 mA/cm².

Fig. 6.35 shows dependence of boron concentration profiles on doping and laser activation conditions. For the 1 kV, 45 s doping, the total content decreased at 300°C activation because of enhanced boron evaporation. Reduction of film thickness was estimated to be 10 nm from bottom depth of the concentration profile. For the 5kV, 6 s doping, the diffusion depth was increased by increasing the substrate temperature to 300°C. The total content of boron was almost the same. The X-ray diffraction analysis showed that the crystallization of poly-Si film was increased by increasing activation temperature. These results indicated that a slightly higher energy doping suppressed the evaporation, and more effective activation was achieved by heating the substrate at activation.

6.5 Low-energy doping and laser activation mechanism

6.5.1 Doping and activation mechanism

Considering the results obtained from SIMS, SEM, and XPS analyses, a doping mechanism was proposed. Fig. 6.36 illustrates the ion doping and laser activation models for low-energy long-time doping such as V_{acc} of 1 kV and doping time of 45s, as mentioned in section 6.4. As shown in (a), after ion doping, the thin phosphorus layer is deposited and natural

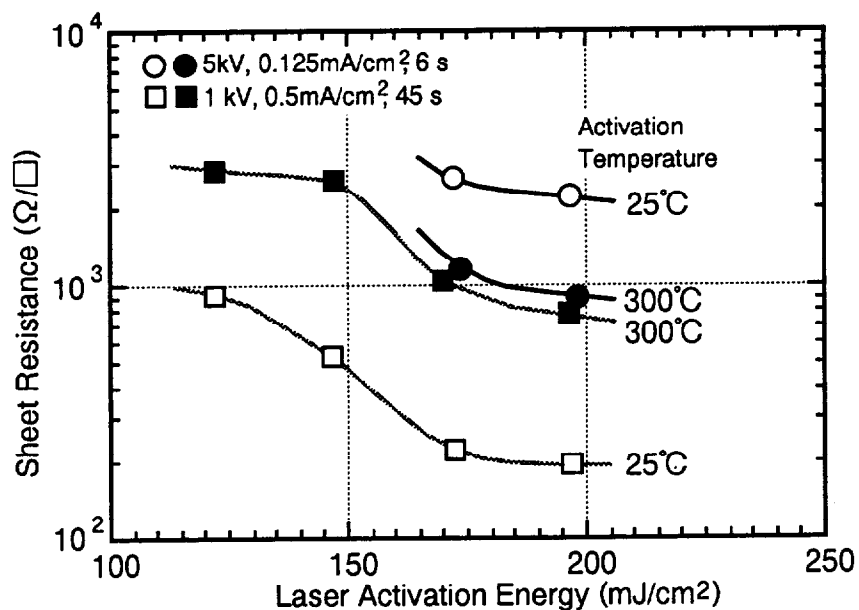


Fig. 6.34. Dependence of sheet resistance on laser activation energy for different conditions of boron doping and activation.

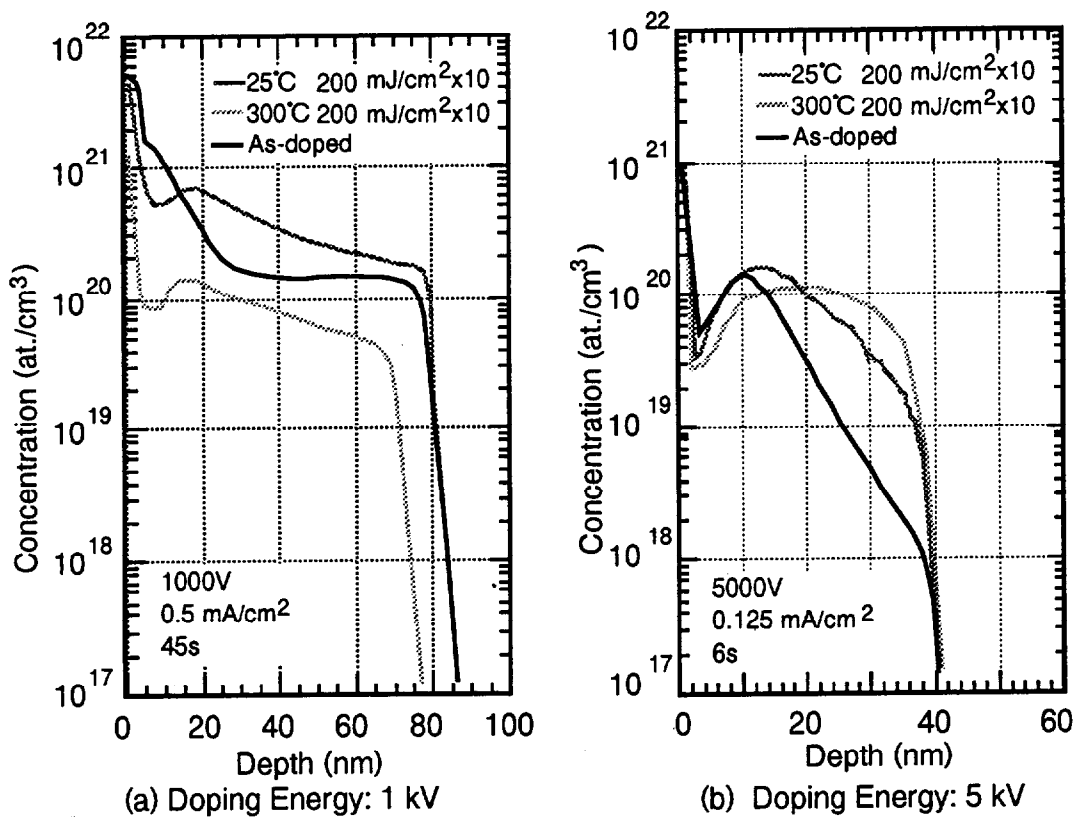


Fig. 6.35. Dependence of boron concentration profiles on doping and laser activation conditions.

silicon oxide is partially destroyed. The surface layer of phosphorus is oxidized. In laser activation (b), the deposited phosphorus layer acts as a diffusion source and a part of the phosphorus is evaporated. It is also suggested that removing natural oxide before doping promotes effective diffusion of dopant into silicon as introduced in Chapter 7.

From these results, it was concluded that a somewhat high energy to destroy natural oxide and a shorter time doping, such as 5 kV and 6-10 s doping, effectively suppress excess deposition and evaporation in laser activation.

6.5.2 Comparison with solid and liquid diffusion models

In the excimer laser activation, there are two possible kinds of phase states of poly-Si, the heated solid state and melt state. Both of the states can be realized by controlling laser energy and in these states, impurity diffusion characteristics are different. In this section, the diffusion mechanism in laser activation is discussed in comparison with conventional solid diffusion.

The solid-state diffusion technique of impurities have been a basic technology in LSI fabrication and is summarized as follows [15]. There are two basic diffusion models, a vacancy mechanism and an interstitial mechanism. The diffusion of typical substitutional impurities such as boron, arsenic, and phosphorus is described by the former mechanism. The diffusion mechanism (Fick's second law) is described by the following equation assuming that diffusion coefficient D is constant and an electric field is not applied:

$$\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \quad \text{-----} \quad (6-1)$$

where, C , t , and x are impurity concentration, diffusion time and diffusion depth, respectively.

The impurity diffusion can be carried out under two conditions, namely, constant surface concentration and constant total impurity condition. These typical conditions correspond to a pre-deposition step and a drive-in diffusion step. Diffusion from an implanted layer is in accordance with the latter step.

In the constant surface concentration condition, considering initial and boundary conditions, the solution of equation (6-1) is given by

$$C(x,t) = C_s \operatorname{erfc} \frac{x}{2\sqrt{Dt}} \quad \text{-----} \quad (6-2)$$

where erfc is a complementary error function and C_s is surface impurity concentration. In constant total impurity condition, the solution of equation (6-1) is described as

$$C(x,t) = \frac{Q}{\sqrt{\pi Dt}} e^{-x^2/4Dt} \quad \text{-----} \quad (6-3)$$

where Q is total impurity. This is a well-known Gaussian distribution.

Fig. 6.37 plots distribution of impurities for a complementary error function and the Gaussian distribution. Fig. 6.38 plots the schematic profiles of implanted phosphorus at 5 kV in solid-phase diffusion in RTA mode estimated by process simulator. The result showed that flat profile was realized in 1 min at high-temperature solid-diffusion.

In the laser activation shown in Figs. 6.28-6.31 and Fig. 6.35, as-doped profiles of boron or phosphorus decreased exponentially and did not agree with the Gaussian distribution which is the basic profile in ion implantation. A high-concentration tail is a peculiar feature of ion doping and is explained as lattice excitation resulting from ion bombardment promotes deep diffusion [5].

In low-energy long-time doping such as 1 kV for 45s doping, thin deposited dopant layer was formed. The layer may act as a diffusion source for constant surface concentration mode. But in laser activation, the peculiar phenomenon was observed that total content was increased by specific laser energy irradiation and increasing of shot numbers. This result showed the possibility that the laser irradiation raised the surface temperature and increased the impurity solubility. In the 5 kV and short time 6 s doping, the total content was kept almost constant as for ion implantation. Another noticeable feature of laser activation was that concentration profiles became almost flat at high laser energy. Duration of the laser puls was 28 ns. Assuming that a high-temperature duration for poly-Si film was about 50 ns, the total duration time in ten shots was estimated to be 0.5 μ s. The formation of flat profiles can not be explained by such a short diffusion time. And after activation, concentration of the film bottom indicated a high concentration almost the same as the solubility of $4 \times 10^{20} \text{ cm}^{-3}$ for phosphorus and $6 \times 10^{20} \text{ cm}^{-3}$ for boron [15]. SEM observation of poly-Si film also showed morphology of solidification from melt (Fig. 6.32). These results suggested that the doping process was promoted by liquid-phase diffusion and regrowth.

Liquid-phase diffusion has been considered when ions implanted into single Si were activated by laser recrystallization [16]. In this case, segregation of dopants occurs in the liquid-solid interface according to the laser-annealed segregation coefficient k' . Fig. 6.39. shows schematic profiles of doped ions. (a) is as-doped profile. When laser irradiated and a part of Si layer has melted, the profile in the liquid becomes almost flat and segregation occurs at the interface if $k' < 1$ as in (b). After regrowth ((c)), accumulation of dopant at surface occurs when $k' < 1$. In ion implantation and laser activation, k' is almost 1 for boron and phosphorus [16]. In laser activation of ion doping, a liquid-phase recrystallization mechanism was supposed and the regrowth step shown in the figure is expected. The analysis of surface concentration of dopant is difficult by SIMS. But in the phosphorus doping in Figs. 6.28 and 6.29, an abrupt increase of concentration at the surface was observed though no increase was observed in the as-doped stage. This may imply the segregation of phosphorus though k' was estimated to be almost 1.

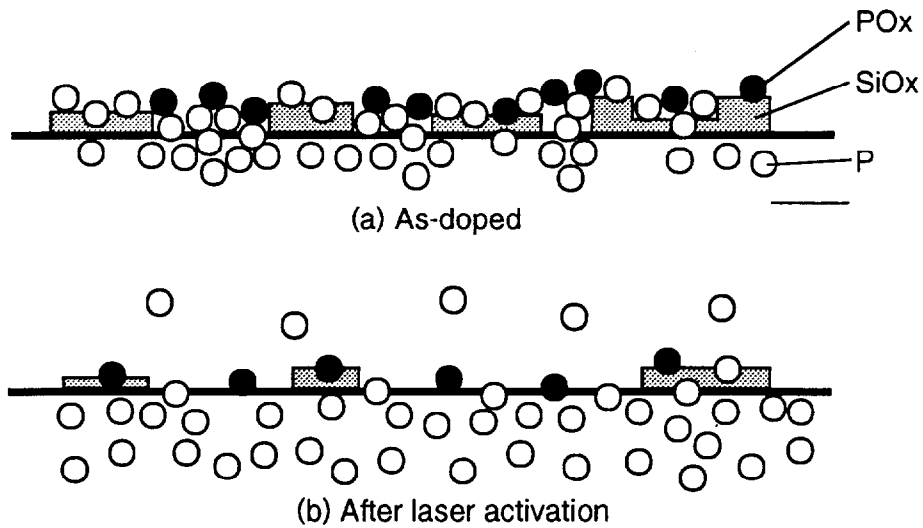


Fig. 6.36. Doping and laser activation models for low energy long time ion doping such as $V_{acc}=1$ kV for 45 s.

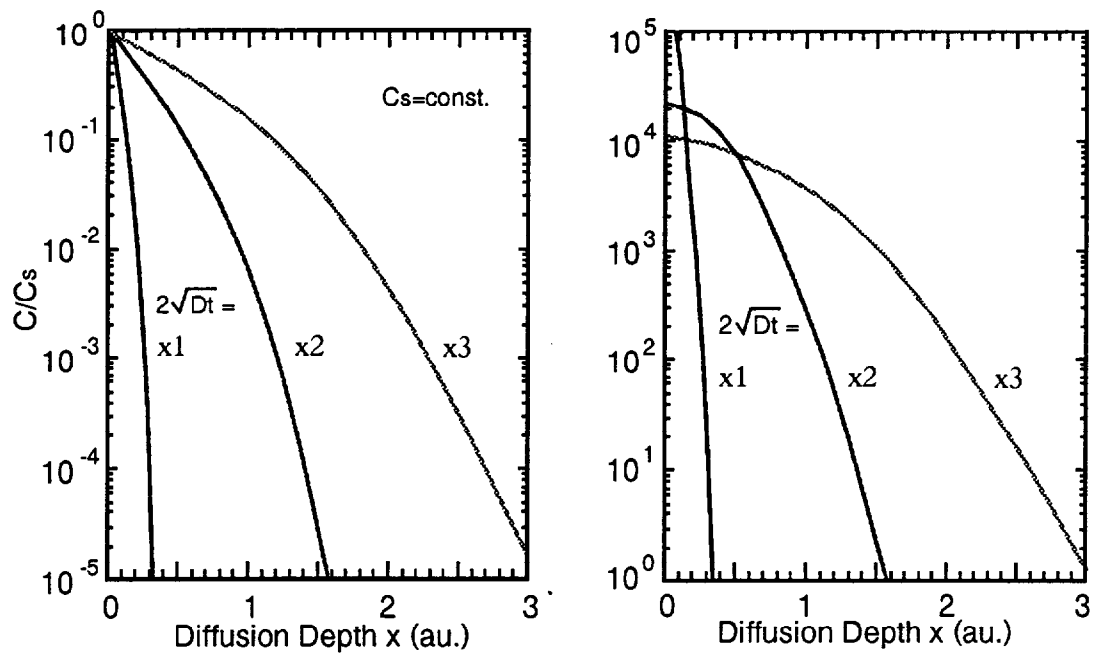


Fig. 6.37. Comparison of solid-phase diffusion models [15].

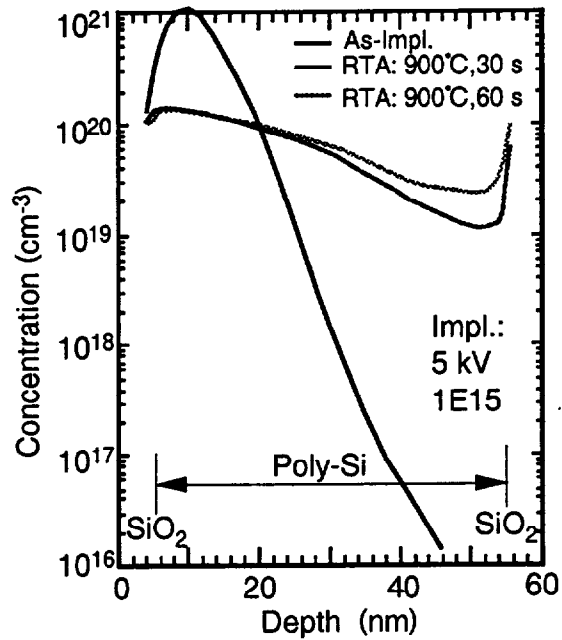


Fig.6.38 Concentration profiles of implanted phosphorus (Gaussian Profile) in solid diffusion.

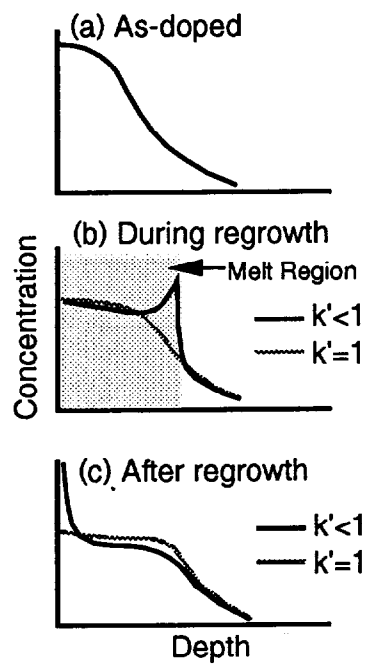


Fig.6.39 Segregation models in laser melting and recrystallization [16].

6.6 Conclusions

For realizing high-speed low-energy non-mass-separation doping to Si film on large glass substrates, the bucket-type ion source which can generate a high density ion beam was introduced. Excimer laser activation was employed for low-temperature activation. The doping apparatuses with ion sources of 150-mm diameter and with a linear shape of 100mm x 400mm were developed. A 10-s doping technology to obtain sheet resistance below 1k Ω /sheet was developed for source and drain of TFT and large-area doping for 350mm x 450mm substrates. The TFTs fabricated by these processes had the same performance as ion implanted ones. The doping technology was successfully applied to the poly-Si obtained by laser crystallization of PECVD Si and field-effect mobility of 205 cm²/V·s was obtained. In activation, the surface of doped poly-Si films was melted and fast liquid-phase diffusion was thought to be the possible doping mechanism.

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High-Performance Low-Temperature CMOS Poly-Si TFTs for AM-LCDs

The key process technologies for large glass substrates are refined to realize high-performance CMOS poly-Si TFTs. an excimer laser line beam is introduced and irradiation conditions are optimized for uniform crystallization. PECVD for high quality gate SiO_2 is studied using TEOS- O_2 system. Ion doping and laser activation conditions are also optimized for resist mask doping of phosphorus and boron to achieve CMOS configuration. Leakage current of TFTs is reduced by applying off-set gate or LDD structures. Using these optimized fabrication processes, high-performance CMOS TFTs are developed and applied successfully for monolithic integration of the driving circuit on 3.8" poly-Si TFT-LCDs.

7.1 Introduction

7.1.1 Necessity of CMOS configuration

The first purpose of this thesis is to develop key process technologies for high-performance poly-Si TFTs and to test their practicalities. Therefore, only n-channel TFTs were fabricated and E-E type inverters were used in the circuit fabrication. But for the actual driver circuits in TFT-LCDs, operation speed, power consumption and the housing for the circuit area must be evaluated. Large power consumption is a serious problem for TFTs on glass substrates since their thermal conductivity is very low. As discussed in Chapter 2, E-E type circuits showed large power consumption [1] and this caused thermal breakdown of TFTs. Therefore, the CMOS configuration of circuits is indispensable in actual applications. Ion doping of two types of impurities, doner and acceptor, were necessary. In this chapter, the ion doping conditions were also optimized to dope phosphorus and boron with a resist mask.

7.1.2 Key technologies for CMOS poly-Si TFTs

The key process technologies to realize high-performance low-temperature n-channel poly-Si TFTs on large glass substrates such as crystallization, gate insulator formation, doping and activation have been

studied. These technologies are refined here to realize high-performance CMOS poly-Si TFTs.

In Chapter 2, APCVD SiO₂, photo-CVD SiO₂, and thermally oxidized SiO₂ were investigated for low-temperature TFTs. In chapter 5, the square beam was used in the first study of laser crystallization.

In Chapter 7, to improve uniformity of the crystallization, beam shapes such as square and linear, beam intensity profiles such as top flat and Gaussian, and beam scanings such as fine pitch scan and step scan are evaluated. Finally, the linear beam with a top flat profile is introduced and irradiation conditions are optimized for uniform crystallization. Also, PECVD of high-quality gate SiO₂ is studied using the TEOS-O₂ system [2], [3] for large glass substrate applications. To reduce leakage current of n-channel TFTs, multi-gate structures are studied. In this chapter, the off-set gate [4] and LDD [5] structures are investigated to minimize the TFT size.

Fig.7.1 illustrates the key technologies developed in this study. They were combined to realize high-performance CMOS poly-Si TFTs and monolithically driver integrated 3.8" TFT-LCDs.

7.2 TFT Fabrication Process

7.2.1 Standard TFT process

Fig.7.2. illustrates the standard coplanar process for CMOS TFT on 100mm x 100mm glass substrates. The underlayer SiO₂ (300 nm thick) was formed by PECVD using TEOS-O₂ system. A 55 nm thick a-Si film was deposited by LPCVD at 450°C using Si₂H₆. After laser crystallization using XeCl excimer laser with an energy of 400 mJ/cm², poly-Si film was patterned into islands. A gate insulator SiO₂ (100 nm thick) was deposited by PECVD using TEOS-O₂. Then 100 nm gate poly-Si was deposited by LPCVD using Si₂H₆ at 450°C. After gate patterning, the p-channel region was protected by photoresist and phosphorus was doped by ion doping at 5 kV for 10 s in the n-channel region. After removing the resist by plasma ashing, the n-channel region was covered by resist and boron was doped into the p-channel region. Laser activation was carried out at 200 mJ/cm² after removing the resist. Final annealing was done at 300°C for 60 min after passivation by PECVD SiO₂ (300 nm) and AlSi metallization.

In these steps, individual key process conditions were optimized as described later.

7.2.2. Off-set gate and LDD structures

In the off-set gate formation, one more photoresist mask step was added to the n-channel TFT. After gate and gate SiO₂ etching, the off-set region was covered with photoresist and ion doping was applied for source and drain regions. In LDD formation, low concentration phosphorus was first doped for both n- and p-channel TFTs without resist mask. Then, n-channel and p-channel regions were doped individually

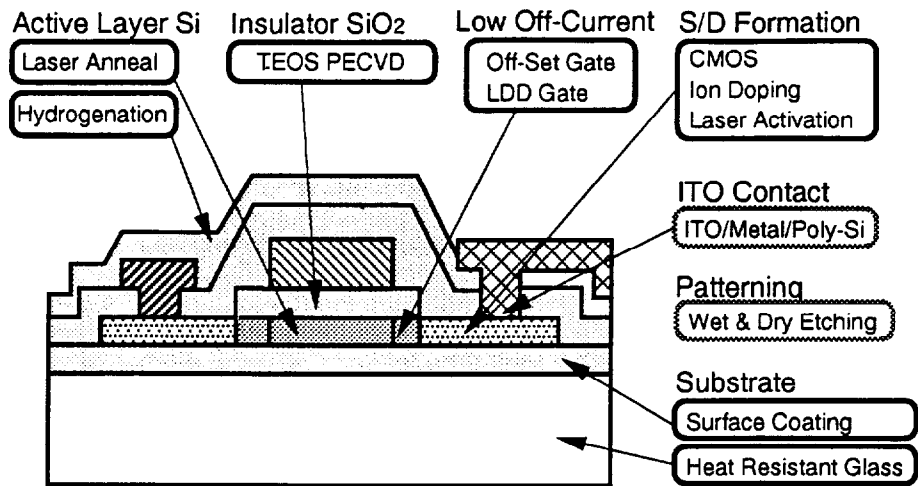


Fig. 7.1. Key technologies developed and employed to realize high-performance CMOS poly-Si TFTs. Maximum process temperature was 450°C.

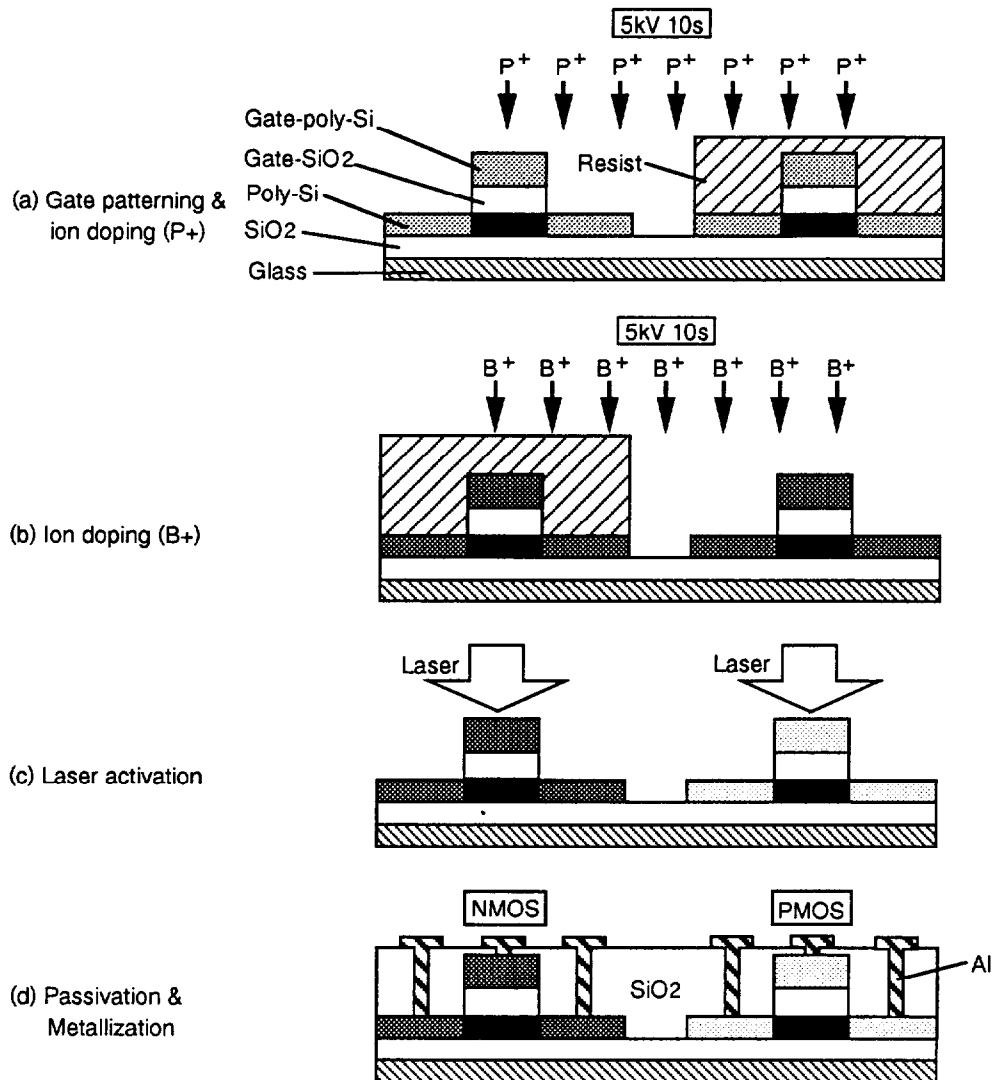


Fig.7.2. Fundamental fabrication process for CMOS TFTs.

using resist mask. Setting the length of the off-set or LDD as zero, a conventional single drain structure was fabricated at the same time.

7.3 Improvement of uniformity of laser crystallization

7.3.1 Laser beam shapes and scanning methods

Fig.7.3 illustrates the laser beam shapes and scanning methods. The fundamental square beam ((a)) has been used in various studies [6]-[8] including the large area crystallization study in Chapter 5. A basic scanning method with a reasonable throughput is the step scan with 1 mm overlap. The fine pitch scan with square beam and an overlap of 0.2 μm ((b)) should improve uniformity of crystallization as reported [6]. But the square beam requires two-dimensional scanning and it is difficult to achieve high throughput and uniformity in the Y direction. The line beam is applicable for mass production because only one-dimensional scanning is needed which means potential to improve uniformity ((c)). There are two intensity profiles for line beam usage, top flat [9] and Gaussian [10] types. The former needs a fine optical system for two-dimensional modulation, but the latter needs only one-dimensional modulation. The top flat shape should be useful in studying fundamental phenomena of crystallization. Overlap ratios of 90-98% are typical. Then, effect of the beam shape and scanning method on crystallization was studied.

Fig.7.4 shows SEM photographs of poly-Si films that were laser crystallized with four irradiation methods after Secco-etching [11]. XeCl excimer laser (308 nm) was used for (a), (b), and (c), and KrF excimer laser (248 nm) was used for (d). The optimum conditions were selected for each method. The morphologies of poly-Si grains were almost the same for all methods. The results showed that almost the same grain size could be realized by these optimized irradiation methods, at least in the short range area.

To improve uniformity of laser crystallization, optimization of laser energy and long range uniformity were studied. Fig.7.5 shows dependence of morphology of poly-Si grain and field-effect mobility of TFT on laser energy. The square beam step scan mode in Fig.7.3(a) was used. The field-effect mobility increased to 200 $\text{cm}^2/\text{V}\cdot\text{s}$ with increasing laser energy up to 400 mJ/cm^2 because grain size increased ((B)). But the value rapidly decreased when laser energy surpassed 400 mJ/cm^2 . In this region ((C)), the grain size was very small, and microcrystalline. Points B and C were characterized as a super-lateral growth regime (SLG) with almost complete melting and rapid homogeneous crystallization after super-cooling by full melting, respectively [12]. To obtain maximum performance of TFTs, optimum laser energy must be selected, adjusted to poly-Si film conditions. But the range of optimum laser energy (laser process window) was not sufficiently wide and improvement was necessary.

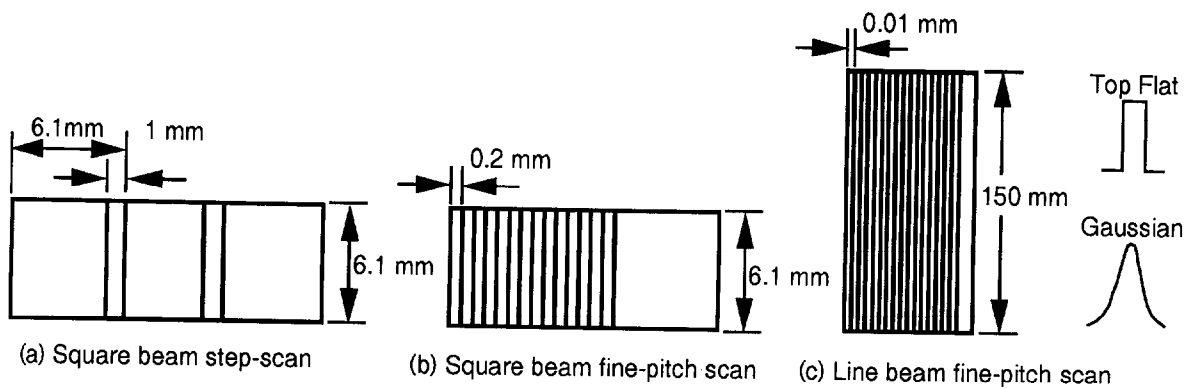
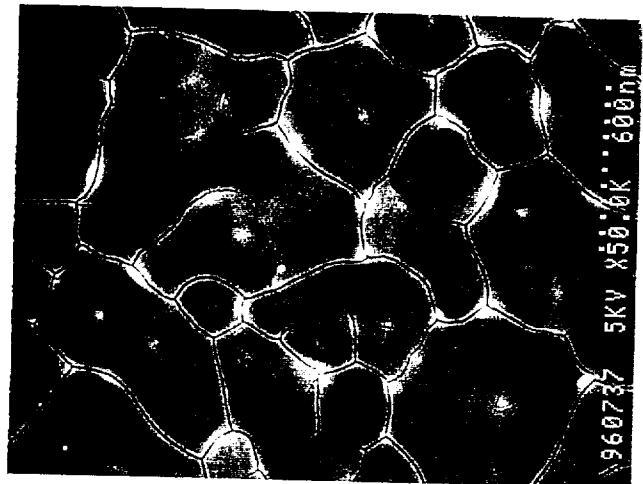


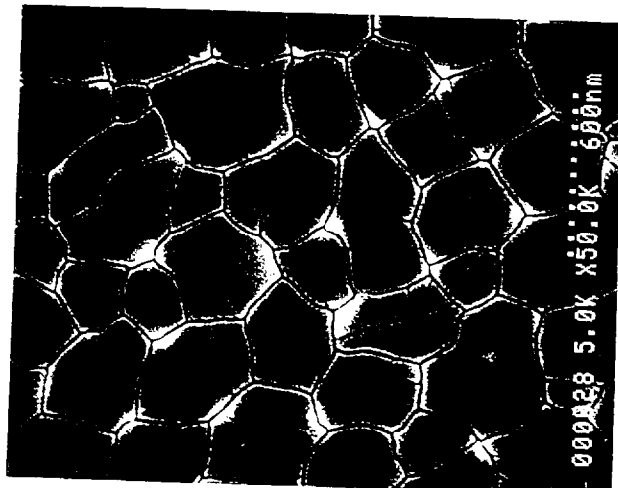
Fig. 7.3. Scanning methods of laser beams.



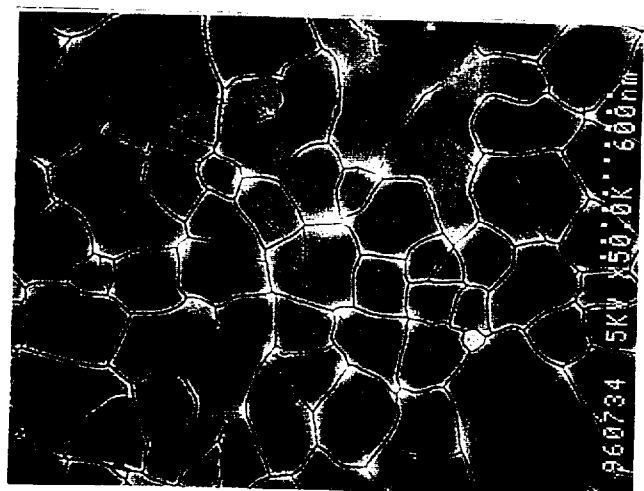
(a) Square beam step-scan.
402 x 10 ($\text{mJ}/\text{cm}^2 \times \text{shots}$).



(b) Square beam fine-pitch-scan.
244x40 and 350x40 ($\text{mJ}/\text{cm}^2 \times \text{shots}$)

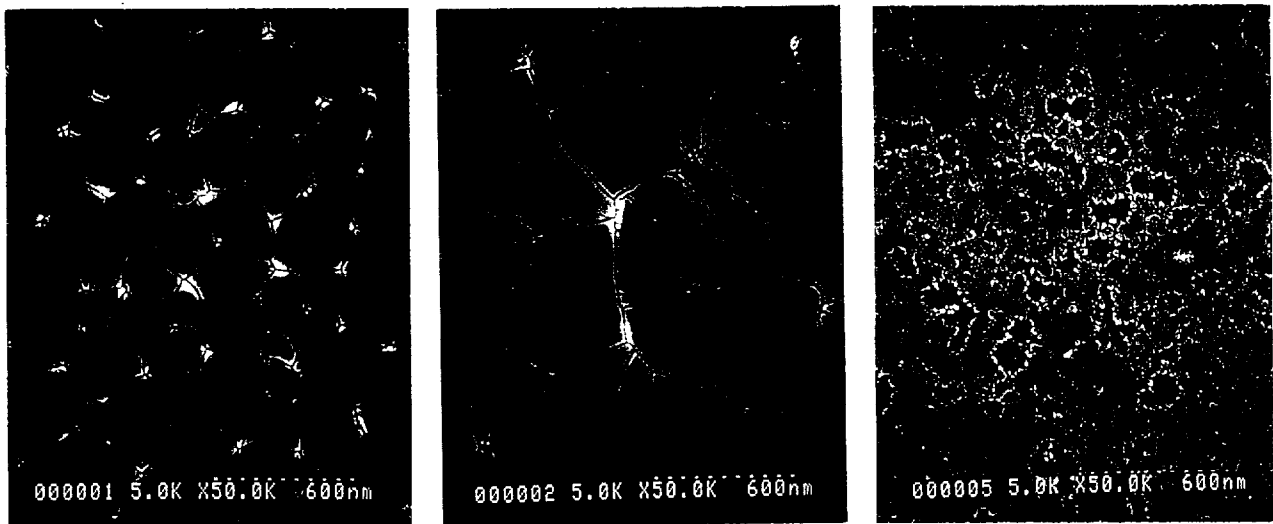


(c) Line beam fine-pitch scan.
Top flat beam: 380x10 ($\text{mJ}/\text{cm}^2 \times \text{shots}$).



(d) Line beam fine-pitch scan.
Gaussian beam: 300x10 ($\text{mJ}/\text{cm}^2 \times \text{shots}$).

Fig. 7.4. SEM photographs of poly-Si grains treated by various laser irradiation methods.

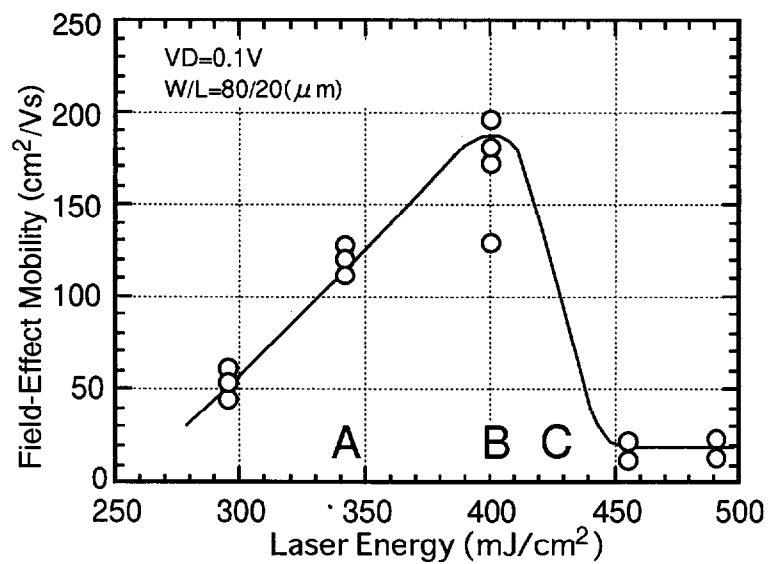


A: 347 mJ/cm²

B: 402 mJ/cm²

C: 424 mJ/cm²

(a) Surface morphology



(b) Field-effect mobility vs laser energy

Fig. 7.5. Dependence of morphology and field-effect mobility on laser energy.

7.3.2 Improvement of uniformity of TFT characteristics

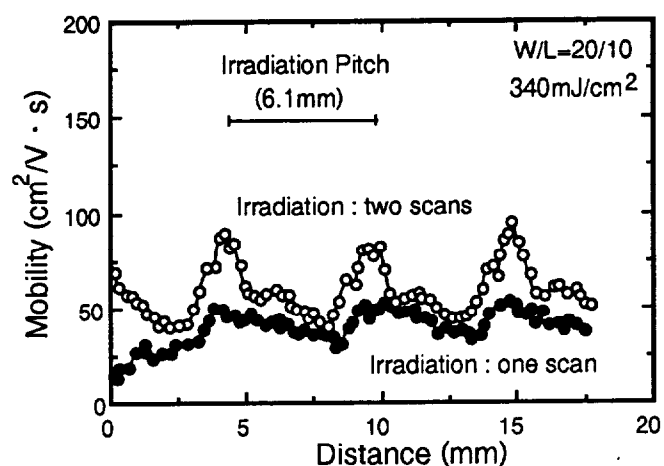
Fig.7.6 plots the uniformity of field-effect mobility of TFTs within a 20 mm range for three laser scanning methods. As the TFTs were in different fabrication lots, the level of the values were not the same for the three cases. TFT array with 200 μm pitch was used as shown in Fig.5.15. In square beam step scanning ((a)), there were periodic changes in value (6.1 mm pitch same as beam scanning pitch) and high values appeared at the beam overlap areas. The values increased by scanning twice. This meant that the energy intensity of the beam edge was slightly higher than that of the center area. Step scanning could not compensate for the nonuniformity of the laser intensity profile. Very flat intensity profiles were proved indispensable. In square beam fine pitch scanning ((b)), uniformity was noticeably improved and the values were slightly increased during high-energy laser activation. The 0.2 μm pitch irradiation corresponded to 30 shots, therefore, uniformity of crystallization was improved by multi-irradiation [6]. The multi-irradiation compensated for the nonuniformity of the intensity profile of the beam and also for the instability of individual light emissions. In line beam fine pitch scanning ((c)), almost perfect uniformity was realized. A laser source able to provide higher power and higher repetition frequency than the small power laser used in (a) and (b), was introduced. The line beam (100 mm length) had a completely top flat shape and intensity uniformity of $\pm 5\%$ in both long and short axes. The uniformity of other TFT characteristics such as V_{TH} , on-current, was also improved. Thus, using the optimized laser apparatus and beam scanning method, uniform characteristics of TFTs were realized in long range areas.

7.4 Reduction of TFT leakage current

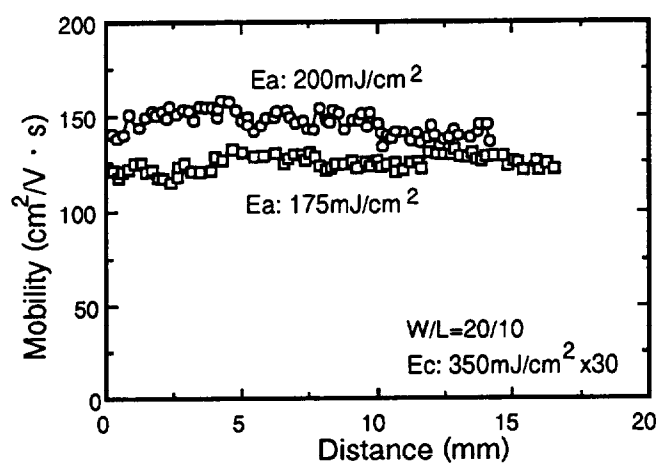
7.4.1 Drain engineering

In the application of poly-Si TFTs to AM-LCDs, especially to pixel TFTs, off-current must be reduced. The leakage current is generated by traps in the drain region. The poly-Si film fabricated by SPC has a high spin density of $2 \times 10^{17}/\text{cm}^3$ [13] and drain engineering to reduce off-current is indispensable. For the TFTs which were used in the large pixels discussed in cChapters 2 and 5, a multi-gate structure was applied. The multi-gate structure enlarged the TFT size, but the ratio of TFT area in the pixel was not so large. When pixel size was decreased in high resolution TFT-LCDs, reduction of TFT size was also considered to maintain high aperture ratio.

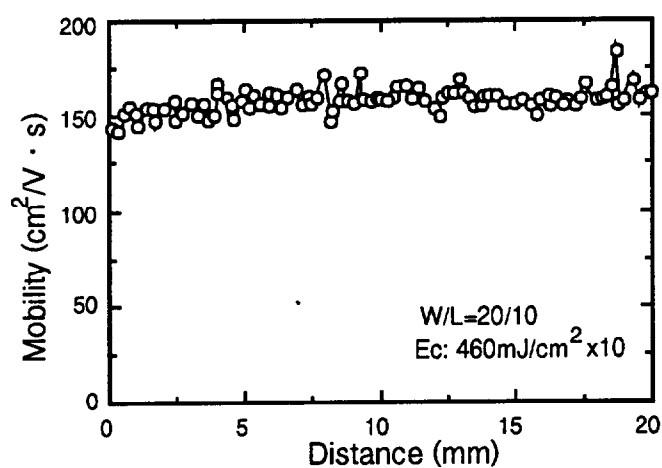
Laser crystallization increased grain size but trap state density at grain boundaries should still be high. Therefore, drain engineering to reduce off-current was still necessary, as studied in Chapter 5 using the multi-gate structure. Other TFT structures have been proposed to reduce off-current without increasing TFT size. These basic techniques reduce electric field strength at the drain junction. The off-set gate [4] and LDD



(a) Square beam step-scan



(b) Square beam fine-pitch scan



(c) Line beam fine-pitch scan

Fig. 7.6. Uniformity of field-effect mobility in various laser beam scanning methods.

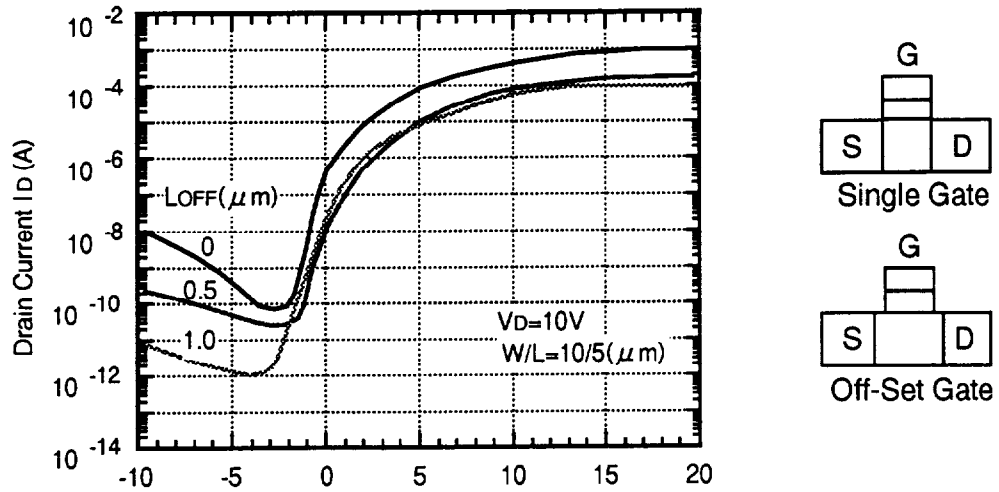
[5] are typical structures which need only one additional photomask step in fabrication. A gate overlapped lightly doped drain (GOLDD) [14] was also an effective structure, but its structure was slightly complicated for TFT use on large glass substrates. A four-terminal device [15] was a newly proposed structure which could suppress both the kink effect and leakage current. But this TFT structure is not applicable to fine driver circuits.

Below, off-set gate and LDD structures were studied considering TFT size and simplicity of the fabrication process.

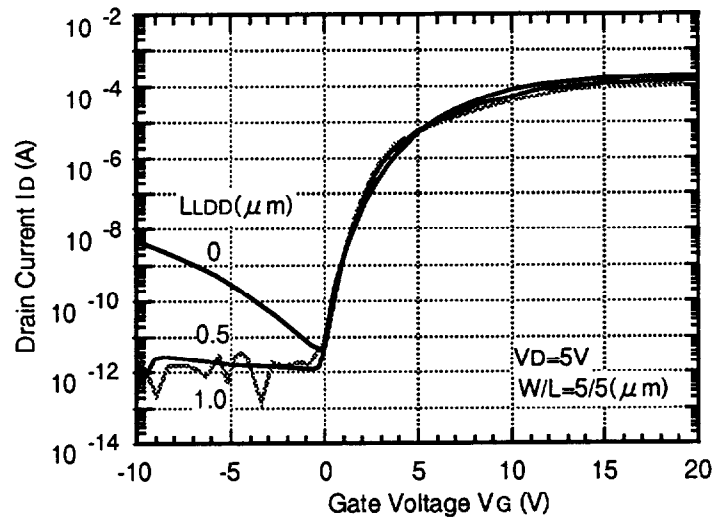
7.4.2 Application of off-set gate and LDD to TFTs

Fig. 7.7 shows V_G - I_D characteristics of TFTs with single drain, off-set gate and LDD structures. Because all the TFTs were not in the same fabrication lot, the level of TFT performance was not the same among the three figures. The off-set length (L_{off}) of zero meant a single drain structure. In off-set structures, off-current was noticeably decreased by increasing L_{off} to 0.5 and 1.0 μm . But as predicted previously, on-current was also reduced to less than 50 % of the value of the single drain TFT. The length of 0.5 μm may be optimum but there was still some trade-off between on- and off-currents. The reduction of on-current was caused by the high resistance of intrinsic poly-Si in the off-set region and was not prevented. Therefore, the structure would be applicable to pixel TFTs which attach more importance to off-current than on-current. But it may not be suitable for driver TFTs which need high on-current to maintain high-speed operation.

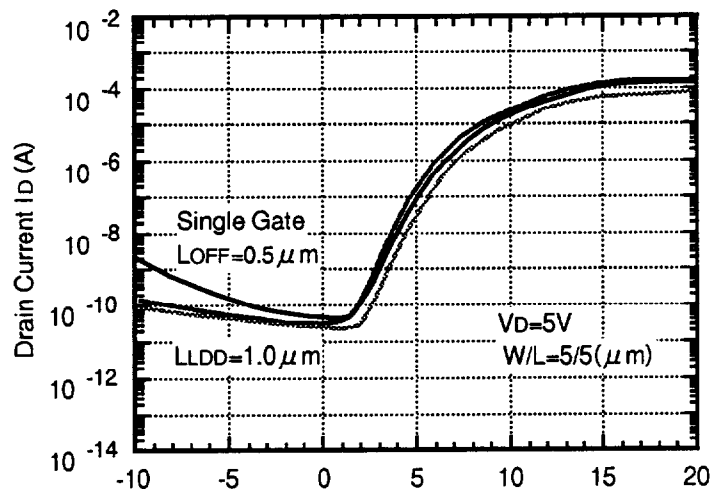
In the LDD structure ((b)), off-current was also effectively reduced using LDD with a length of 0.5-1.0 μm . Low concentration doping was carried out by keeping beam current low in non-mass separated ion doping. The ratio of reduction of the on-current was minimized compared with the off-set structures, even with a LDD length of 1.0 μm . LDD structure should be a promising means to reduce leakage current while maintaining high on-current, although it requires an additional photomask step and low concentration ion doping. Fig.7.7(c) shows V_G - I_D characteristics of TFTs with three kinds of gate structures fabricated in the same lot. Concerning off-current, a TFT with a 0.5 μm off-set gate and another TFT with a 1.0 μm LDD structure had almost the same performance. Compared to the single drain TFT, the ratio of reduction of the on-current of the off-set gate structure was still large at -34 %, but that of the LDD structure was almost zero. The performance of TFTs also depends on the characteristics of the gate insulator SiO_2 . The ultimate drain structure should be selected considering the total TFT process configuration.



(a) Off-set gate structure



(b) LDD structure



(c) Comparison of drain structures in a substrate

Fig. 7.7. Dependence of V_G - I_D characteristics on drain structures.

7.5 PECVD of SiO₂ using TEOS

7.5.1. PECVD of SiO₂ by TEOS-O₂ system

In LSI fabrication, the SiH₄-O₂ (N₂O) system has been used for the thermal deposition of SiO₂ at 400-450°C (750-850°C) because the system does not contain C atoms and it realizes high purity oxides with a high deposition rate [16]. Plasma CVD lowers reaction temperature to 200-350°C. But step coverage characteristics are not sufficient and SiH₄ gas is very explosive. TEOS has also been widely used for the formation of thick interlayer insulators of LSI devices by thermal decomposition at low pressure or atmospheric pressure at about 650-750°C [16]. In these high temperature depositions, gas ratio of TEOS was large. Deposition rate was very high, but good step coverage was realized. In the application of SiO₂ to the thin gate insulator (100 nm), good step coverage was an important characteristic. But, impurities such as C or contents of -OH or -H radicals must be reduced. Therefore, deposition conditions must be optimized for gate insulators of TFTs on glass substrates. Plasma CVD method is an attractive means for low-temperature and large-area deposition [2], [3]. In this section, plasma-enhanced CVD using 13.56 and 27.12 MHz RF was studied.

Fig.7.8 illustrates the manual reactor for TEOS SiO₂ CVD with parallel electrodes of 300 mm diameter. This apparatus was used to confirm the possibility of SiO₂ PECVD using the TEOS-O₂ system. A glass substrate (100 mm x 100 mm) was fixed on the heater plate and the chamber was vacuumed to a 0.13 Pa. After substrate heating, a mixture of TEOS and O₂ was introduced. Then, the gas pressure was maintained at a fixed value and PECVD was carried out by 13.56 MHz RF discharge.

Fig.7.9 shows the configuration of the developed multi-chamber type auto processor with three CVD reactors and laser annealer with a line laser beam. Reactor R1 was for TEOS SiO₂ deposition. The substrates were set in the loader in the load-lock chamber and transported in vacuum to an appointed chamber by a robot. This apparatus was used for the study of the effect of CVD parameters on the characteristics of SiO₂ films. The discharge area was shielded by inner cups. The glass substrate was heated on the anode electrode by the heater. The cathode electrode was also auxiliary heated to avoid particle generation from the upper cathode electrode. Two RFs at 13.56 or 27.12 MHz were applied to the cathode.

7.5.2. Step coverage characteristics

As the insulator was deposited on the patterned films, step coverage was an important parameter for the gate SiO₂ and also for the interlayer SiO₂.

Fig.7.10 shows SEM micrographs of cross sections of metal films with SiO₂. Photograph (a) shows a 130 nm thick SiO₂ layer on a 70 nm thick Cr layer simulating gate SiO₂ deposition (13 nm/min). The Cr was conformally covered. Coverage ratio (side thickness/top thickness) was 0.75 which was thought to be sufficient for gate insulator deposition.

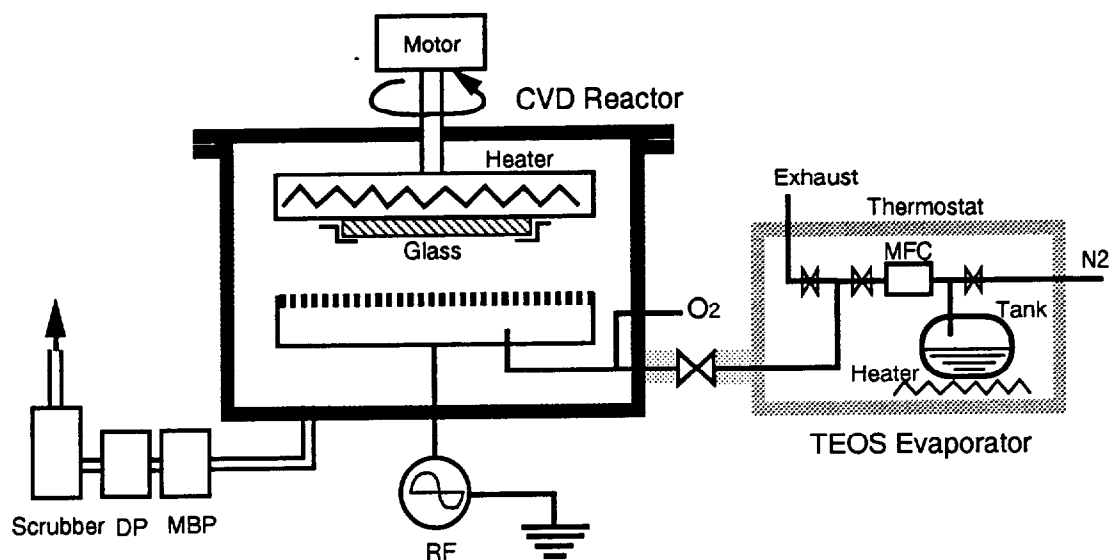


Fig.7.8. Manual reactor for TEOS SiO₂ CVD with 300-mm diameter parallel electrodes.

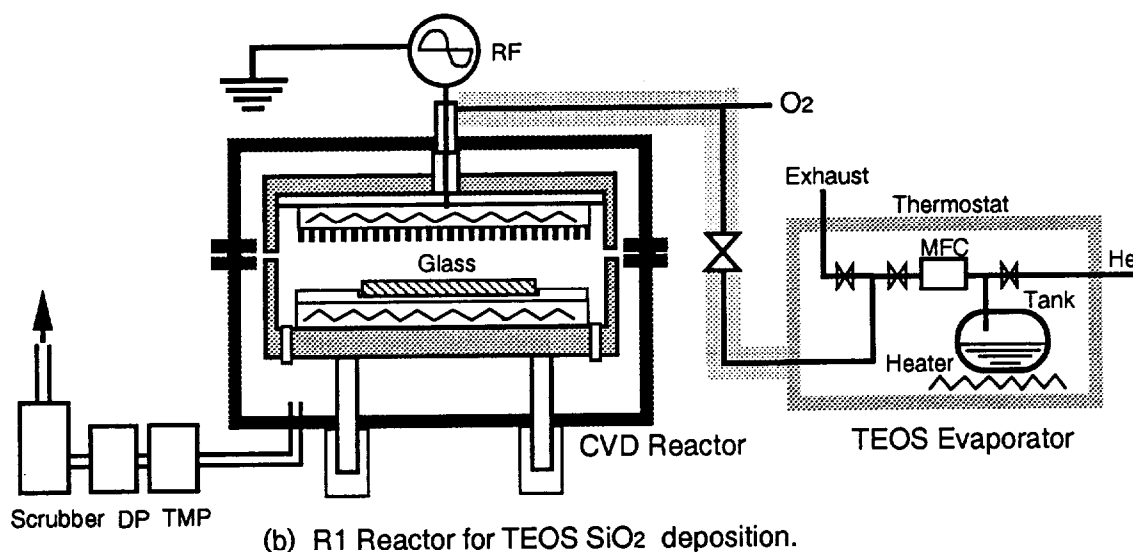
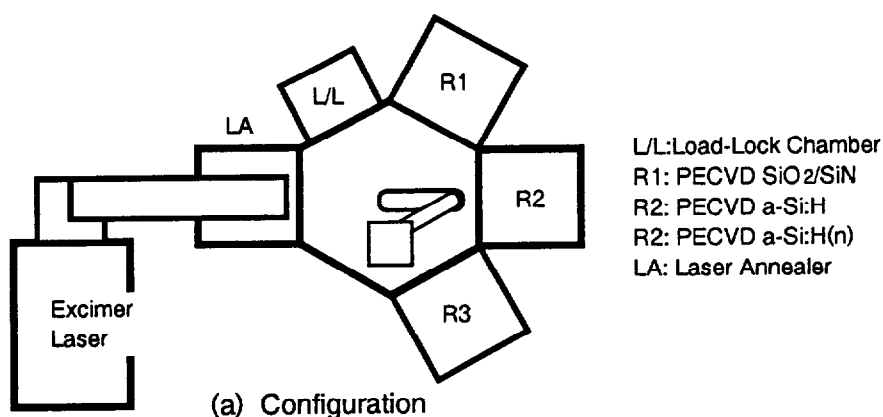
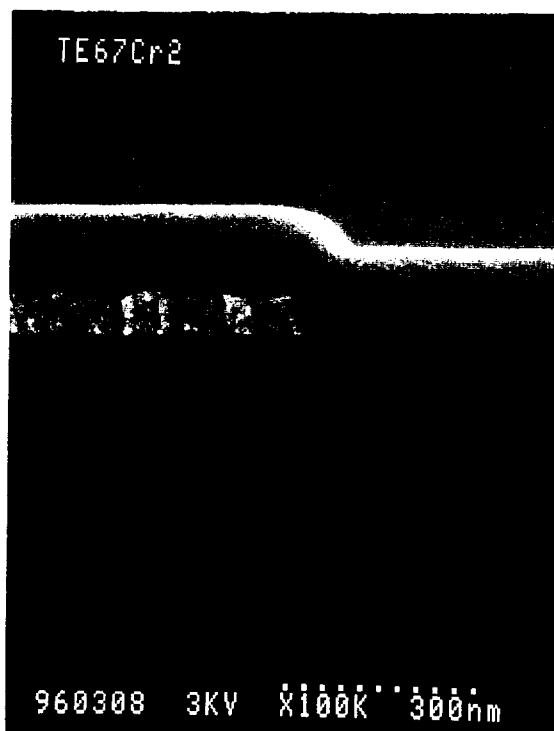
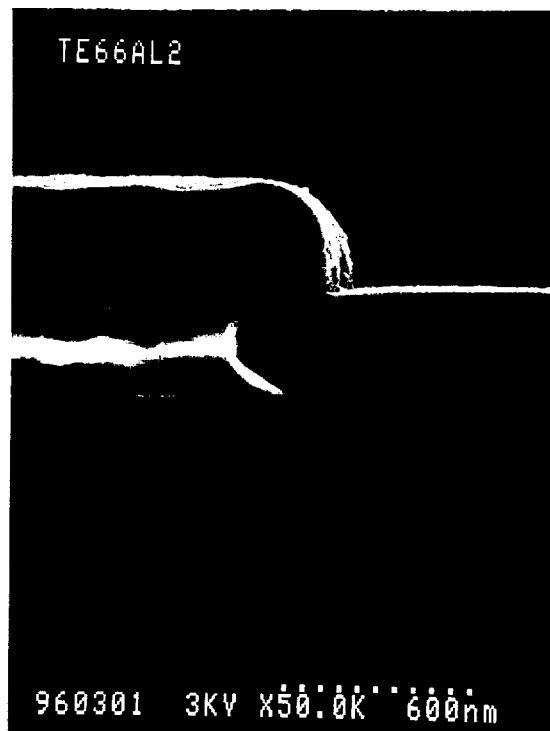


Fig.7.9. Multi-chamber type autoproccessor for poly-Si TFTs.



(a) Stepcoverage for 70 nm thick Cr.
TEOS/O₂=5/250(sccm), 107 Pa.



(b) Stepcoverage for 300 nm thick Al.
TEOS/O₂=10/200(sccm), 107 Pa.

Fig. 7.10. Stepcoverage of TEOS SiO₂ for Cr and Al electrodes.
Reactor: Manual type in Fig.7.8, Power: 200W, Temperature: 350 °C.

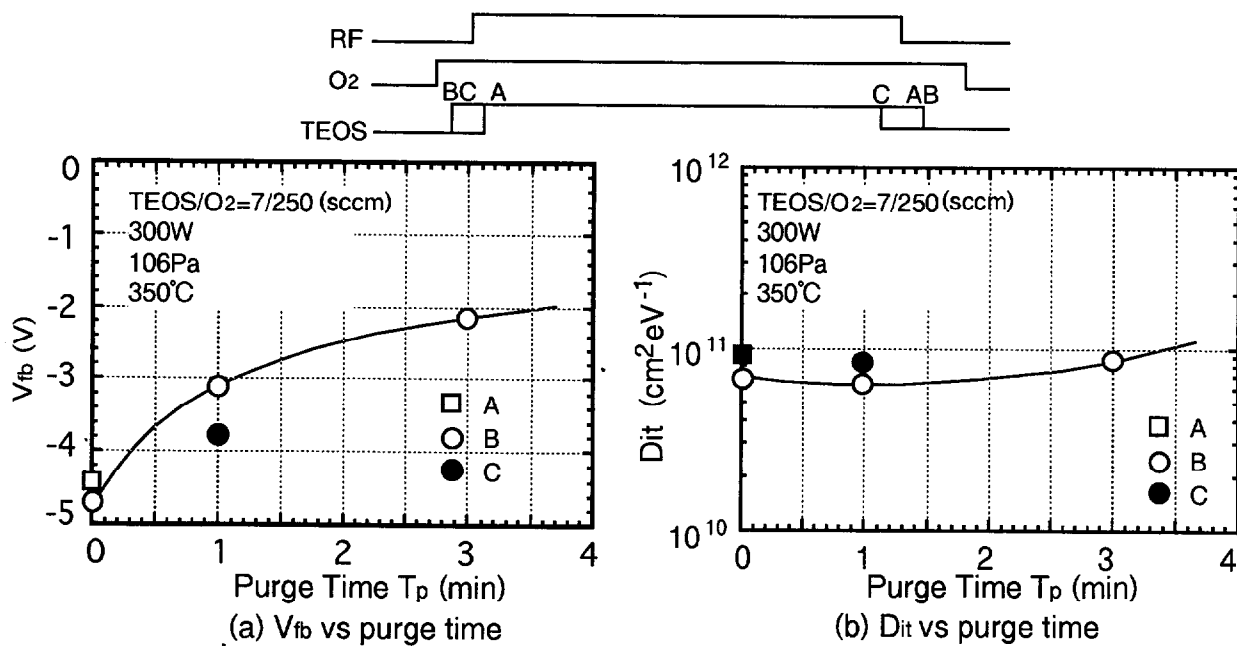


Fig. 7.11 Dependence of SiO₂ characteristics on TEOS purge time before RF discharge.

Photograph (b) shows a 350 nm SiO₂ layer on a 300 nm Al layer for passivation SiO₂ with a higher deposition rate (29 nm/min). The deposition of SiO₂ was also conformal but the coverage ratio was 0.54. If the conditions should be applied to the interlayer insulator between two metallization layers, coverage must be improved and taper etching of the first metal layer would be necessary.

7.5.3 Optimization of deposition conditions for gate SiO₂

The TFT characteristics should depend on SiO₂ film quality itself as well as SiO₂-poly-Si interface conditions. Here, dependence of SiO₂ film quality on deposition conditions was studied. Deposition conditions such as TEOS purge time, gas ratio, RF power, gas pressure, and anode heater temperature were investigated. High frequency C-V and Quasistatic C-V characteristics were measured by MIS diode evaporating Al electrodes. From these data V_{fb} and D_{it} were calculated [17]. IR absorption profiles of Si-O-Si stretching mode around 1070 cm⁻¹ were measured by the FT-IR method. Etching rate was evaluated from etching in HF:NH₄F=1:10 buffer solution at 21 °C.

Fig.7.11 shows dependence of SiO₂ characteristics (V_{fb} and D_{it}) on TEOS purge time before RF discharge. The reactor of Fig.7.8 which mixed O₂ and TEOS in the chamber was used. In this case, TEOS purge time has critical effect on V_{fb} . Then, an excess amount of TEOS was introduced when the MFC was opened and TEOS concentration was gradually reduced to a set value after about three minutes. As shown in Fig. 7.12, excess TEOS degraded film characteristics. Therefore in the following experiments using the new reactor (Fig.7.9), TEOS was mixed with oxygen before introduction into the chamber.

Fig. 7.12 shows dependence of as-deposited SiO₂ film characteristics on deposition conditions. Deposition rate was almost proportional to the TEOS flow rate ((a)). V_{fb} was reduced by increasing RF power and reaction pressure ((c),(e)). D_{it} was clearly reduced by increasing RF power ((d)). TEOS flow rate and reaction pressure showed no significant effect on D_{it} ((b),(f)). RF application of 27.12 MHz showed little effect in improving film quality ((a)-(d)).

Fig. 7.13 shows dependence of chemical properties of SiO₂ on the deposition conditions. An increase of RF power contributed to a shift in peak position of Si-O-Si bond to the thermal SiO₂ position although TEOS flow rate had little effect on Si-O-Si bonding characteristics((a),(b)). Etching rate was reduced by decreasing TEOS flow rate and increasing RF power((c),(d)). This meant that dense SiO₂ was deposited in these conditions.

From these experiments, the quality of as-deposited SiO₂ itself, was improved with the increase in RF power and decrease in TEOS flow rate. Increasing gas pressure seemed to improve SiO₂-poly-Si interface conditions (V_{fb}). Finally, various SiO₂ deposition conditions were applied to actual TFTs to see the effects on their characteristics.

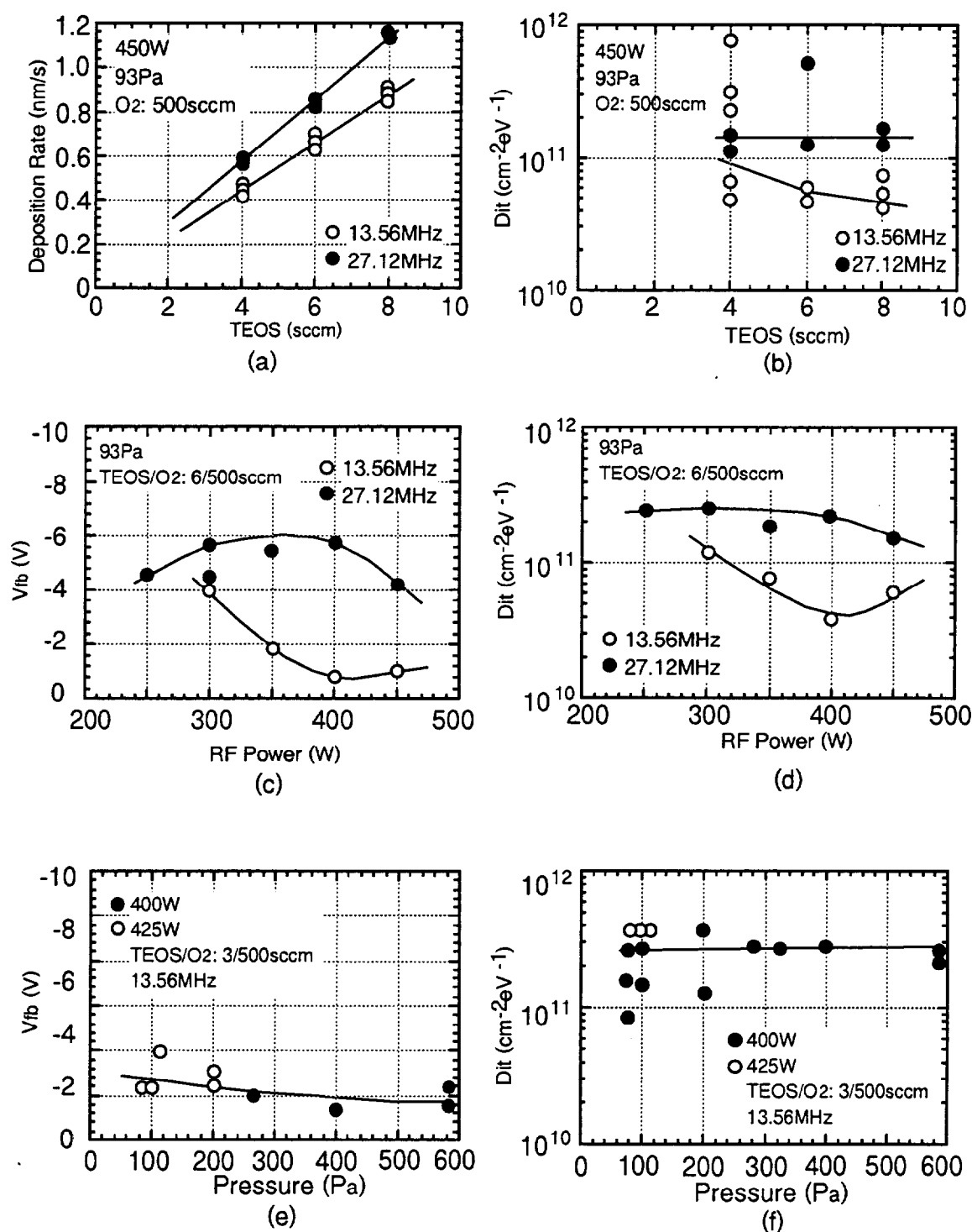


Fig. 7.12. Dependence of SiO₂ film characteristics on the deposition conditions. Anode temp. / Cathode temp. = 300°C/315°C.

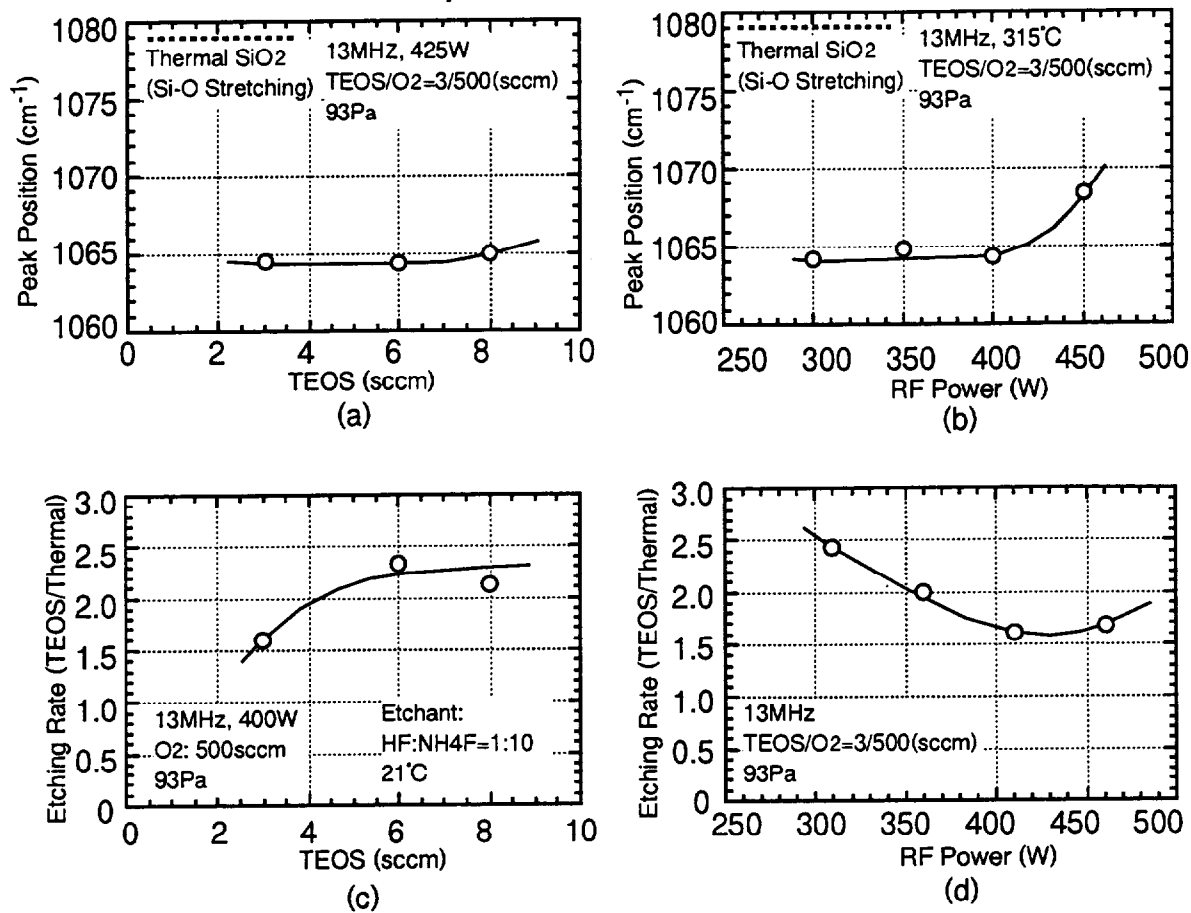


Fig. 7.13. Dependence of chemical properties of SiO₂ films on the deposition conditions. (Cathode temp./ Anode temp.=300°C/315°C)

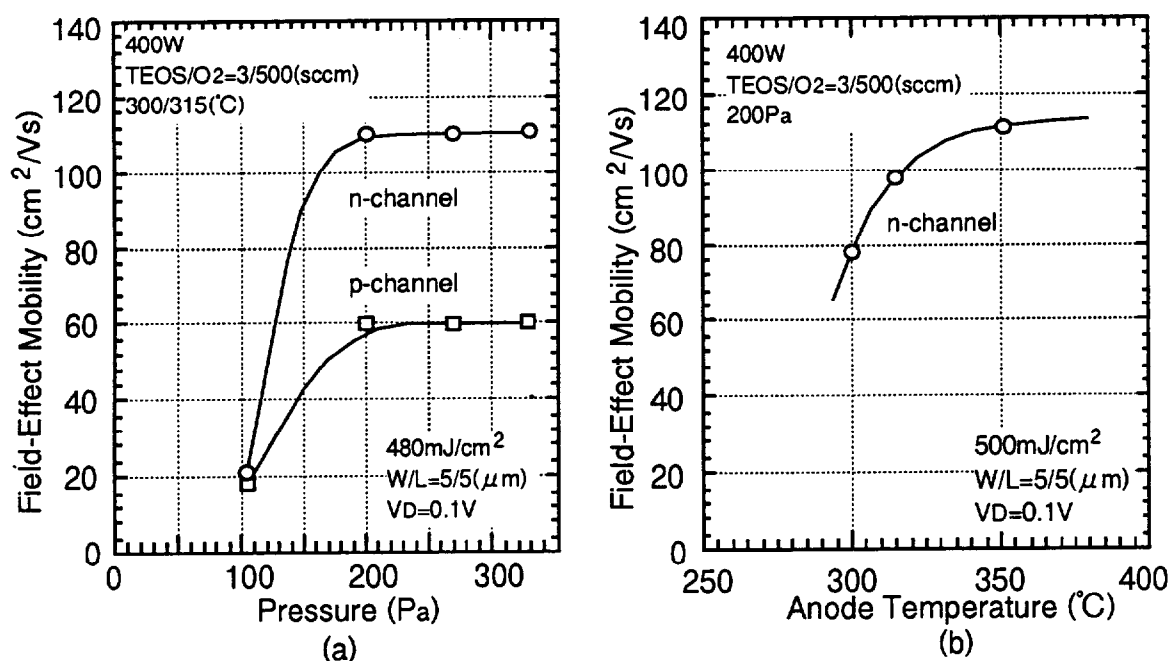


Fig. 7.14. Dependence of TFT characteristics on SiO₂ deposition conditions.

Fig. 7.14 shows the dependence of TFT characteristics on SiO₂ conditions. Increase of gas pressure was very effective in obtaining high field-effect mobility ((a)). At pressures over 200 Pa, the mobility was saturated. Increasing anode heater temperature over 315°C was also effective in increasing field-effect mobility. Decreasing gas pressure had only moderate effect in reducing V_{fb} and D_{it} but it had a noticeable effect in increasing field-effect mobility. High power 450 W deposition helped to densify SiO₂ but also increased V_{fb} and D_{it} . These results implied that preferable conditions to improve SiO₂ film quality were not always acceptable for TFT fabrication and that they may cause plasma damage of interface or poly-Si film. Considering the dependence of both SiO₂ film quality and TFT characteristics on SiO₂ deposition conditions, increasing RF power, gas pressure, and heater temperature were effective in improving TFT performance.

7.6 Fabrication of CMOS TFTs

7.6.1 Ion doping for CMOS TFTs

In the doping apparatus used in this experiment (Fig.6.15), a heat sink was not attached to the glass substrates. To prevent deformation or breakage of the glass substrate by thermal stress, the temperature rise must be below approximately 300°C. Considering the use of resist mask doping, the temperature should be further limited to below 150°C. To realize CMOS structure, doping of phosphorus and boron into individual TFTs is necessary. As a general fabrication process, resist mask doping is used to cover the opposite type region. In this process, first the damage to the photoresist must be avoided when it is removed by conventional resist ashing and wet remover. Secondly, in the resist ashing steps, the reduction of the surface concentration of dopant must be avoided. Therefore, moderately high doping energy is necessary to achieve optimum depth and low heat damage doping.

Fig.7.15 plots the substrate temperature dependence on acceleration voltage and doping time during the doping step. The temperature rise increased with increasing V_{acc} and doping time. Considering that heat resistivity of the resist was 150°C, doping time must be less than 20 s at a V_{acc} of 5 kV. In this study, V_{acc} of 5 kV was selected as a standard condition.

Fig.7.16 shows dependence of sheet resistance on laser activation energy with and without ashing process. The sheet resistance increased when poly-Si was activated after oxygen ashing treatment which corresponded to resist ashing. This meant that a part of the doped phosphorus or boron was removed by ashing. But the sheet resistance of about 1 k Ω /sheet which was low enough for TFT source and drain, was obtained.

Fig.7.17 shows the surfaces of a resist mask after a 5 kV, 10 s doping and resist removing process. There was no damage to the resist after 5 kV

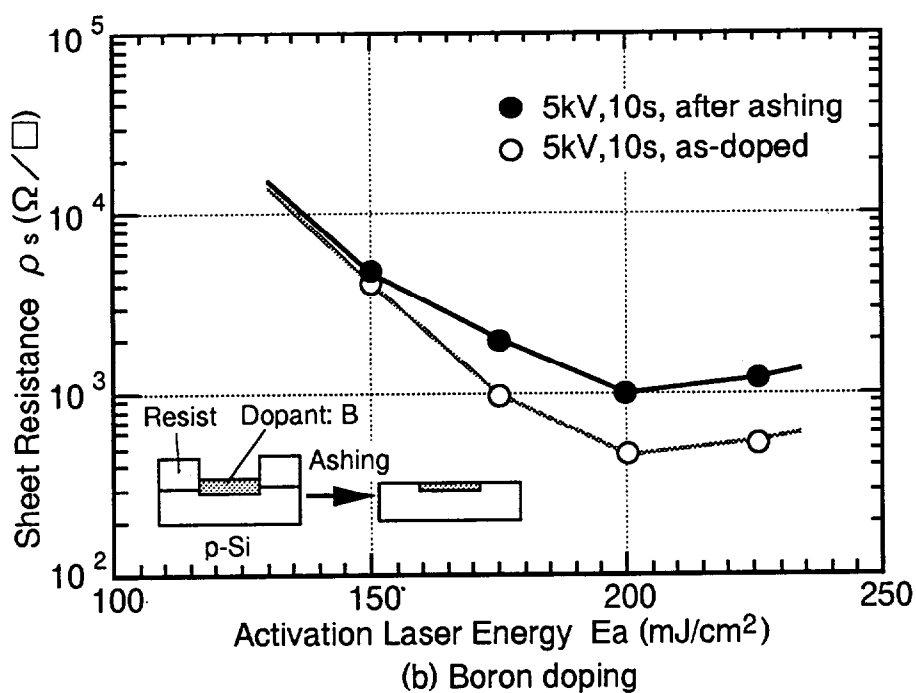
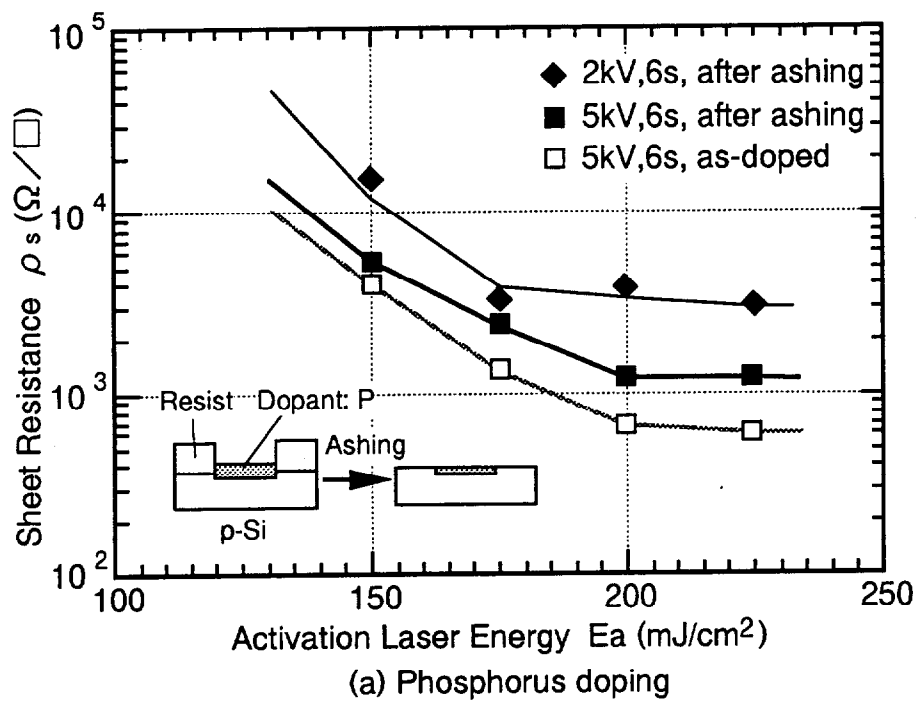


Fig.7.16. Dependence of sheet resistance on activation laser energy and resist ashing.

doping of phosphorus and boron, and the resist was successfully removed without residue using the conventional O_2 ashing and wet process.

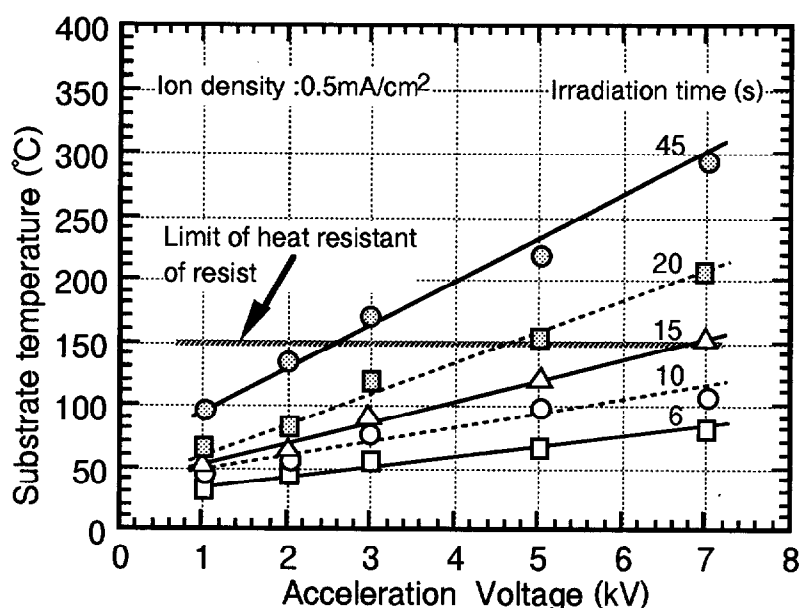


Fig. 7.15. Dependence of substrate temperature on ion irradiation conditions.

Fig.7.18 plots sheet resistance of poly-Si films doped by using the resist mask process with the 5 kV short doping time. A low enough sheet resistance, below $1k\Omega/\text{sheet}$, was obtained by optimizing the activation laser energy. It was confirmed that 6 s doping was sufficient to operate the poly-Si TFTs [18]. Thus, it was shown that the resist mask process with a short doping time (6-10 s) could realize the CMOS structure.

7.6.2. Application of TFTs to CMOS driver integrated LCDs

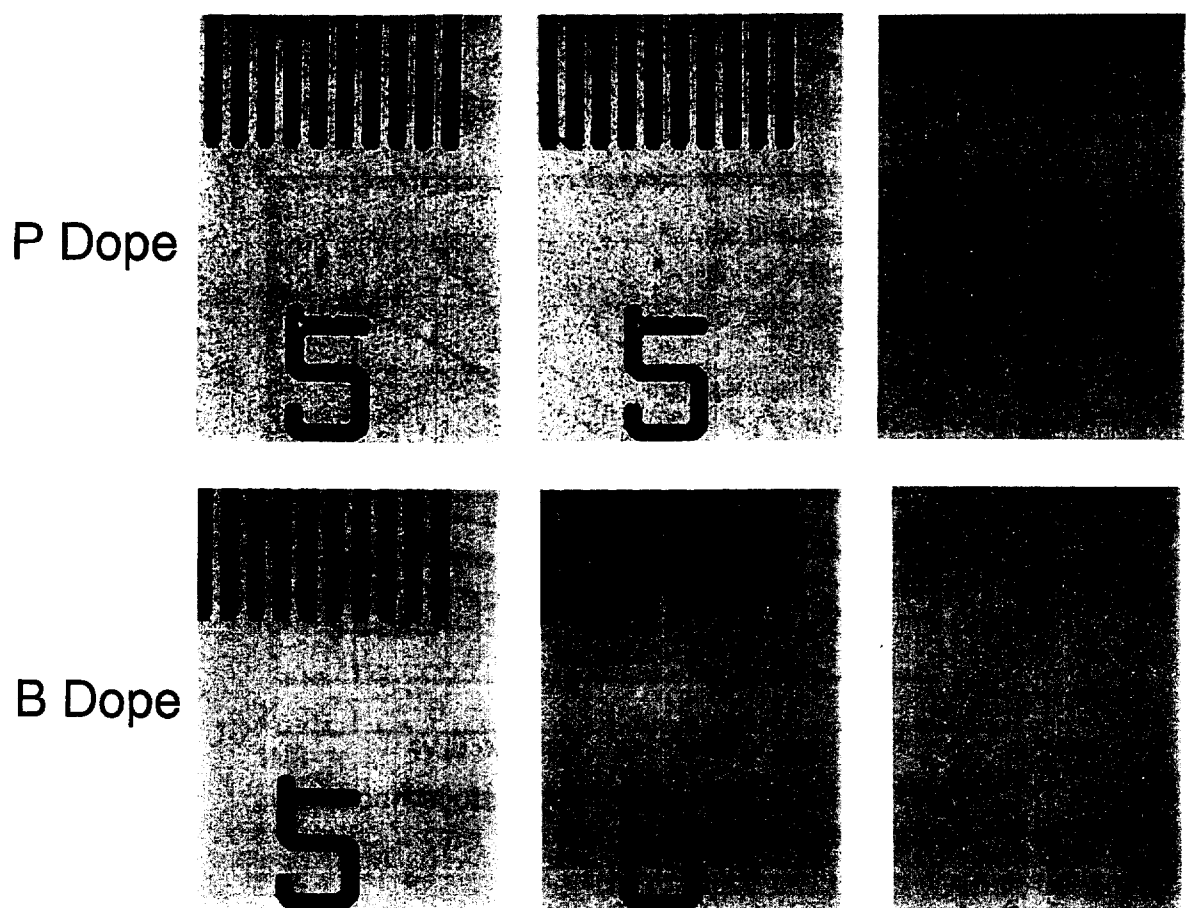
Fig.7.19 illustrates TFT structures in three LDD doping process. (a) is an example of conventional high energy ion implantation. (b) uses low-energy ion doping for both LDD and source and drain formation. (c) is a hybrid doping technology which uses ion implantation for LDD and low-energy high-speed ion doping for source and drain.

Fig.7.20 shows photographs of surfaces of fabricated CMOS TFTs. Both n- and p-channel TFTs were well fabricated without damage.

Fig.7.21 shows uniformity of field-effect mobility of CMOS TFTs in short range area ($200\ \mu\text{m}$). Each TFT was fabricated with a $10\ \mu\text{m}$ pitch. Both n- and p-channel TFTs were uniformly fabricated. Other characteristics such as V_{TH} , I_{ON} and I_{OFF} were also very uniform.

Fig.7.22 shows typical V_G - I_D characteristics of CMOS TFTs fabricated by an optimized fabrication process. Table 7.1 summarizes typical characteristics of CMOS TFTs. Well balanced threshold voltages, high mobilities, and low S values were realized.

Fig.7.23 describes a logic circuit operation. The CMOS shift register with $W/L=10/5\ (\mu\text{m})$ operated at 18 MHz with a V_{DD} of 15 V. The



(a) After development (b) After ion doping (c) After resist removal

Fig. 7.17. Photographs of resist at ion doping processes at 5 kV for 10 s.

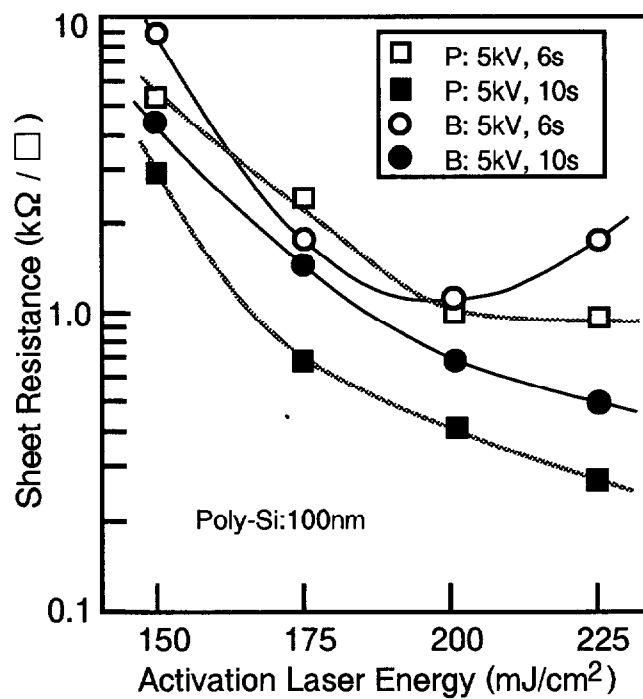


Fig.8.18. Sheet resistance of doped poly-Si films after resist mask removal.

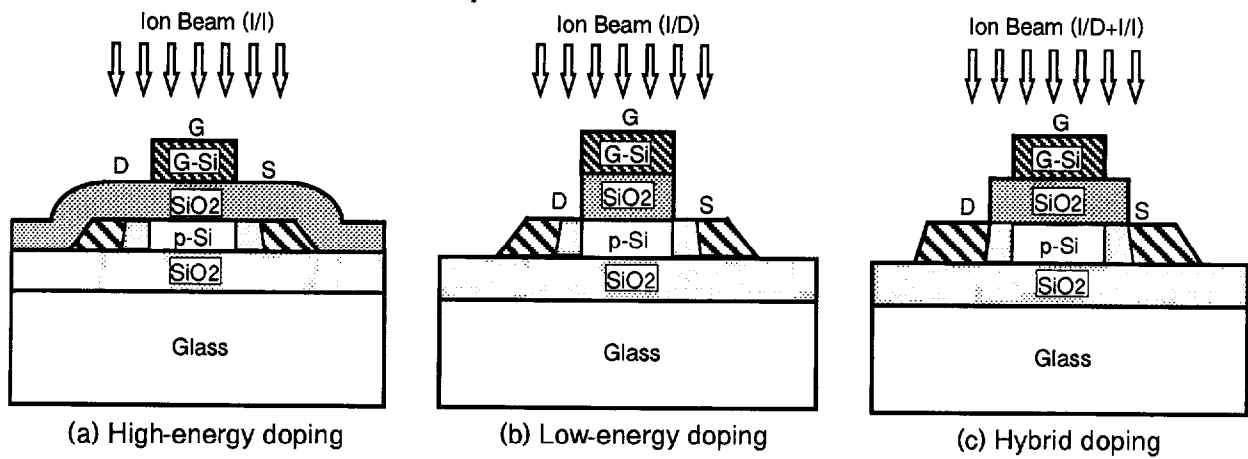


Fig. 7.19. TFT structures in three LDD doping processes

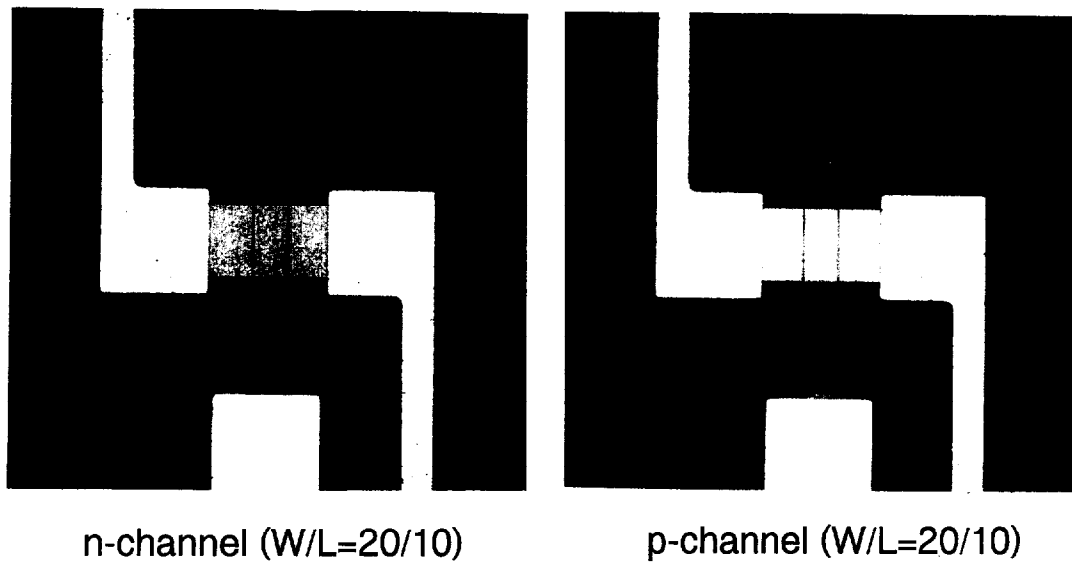


Fig. 7.20. Photographs of CMOS TFTs

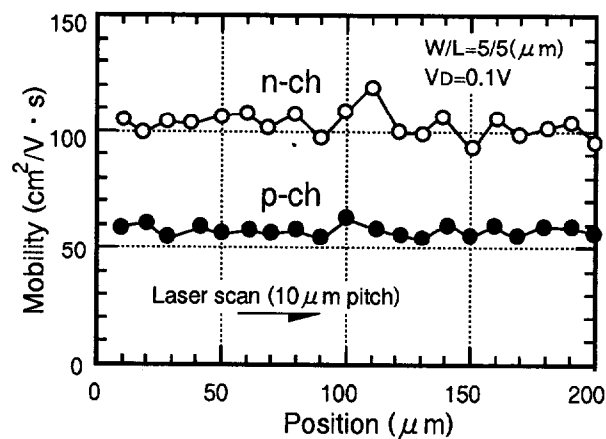


Fig. 7.21. Uniformity of field-effect mobility in short range area.

Table 7.1. Summary of typical characteristics of CMOS TFTs.

	n-channel	p-channel
Mobility (cm^2/Vs) : $V_D=0.1\text{V}$	135	67
Threshold Voltage (V) : $V_D=5\text{V}$	2.7	-1.0
S Value (V/dec.) : $V_D=5\text{V}$	0.32	-0.25

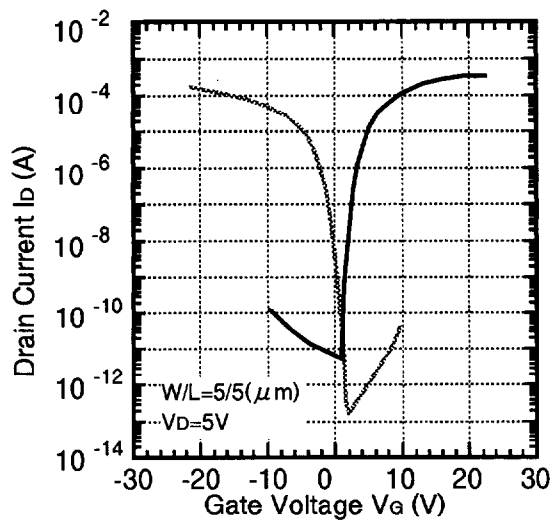


Fig. 7.22. Typical V_G - I_D characteristics of CMOS TFTs.

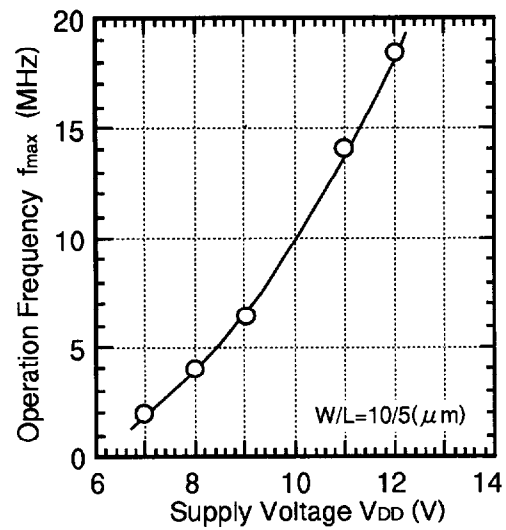


Fig. 7.23. Operation characteristics of 21-stage shift register.

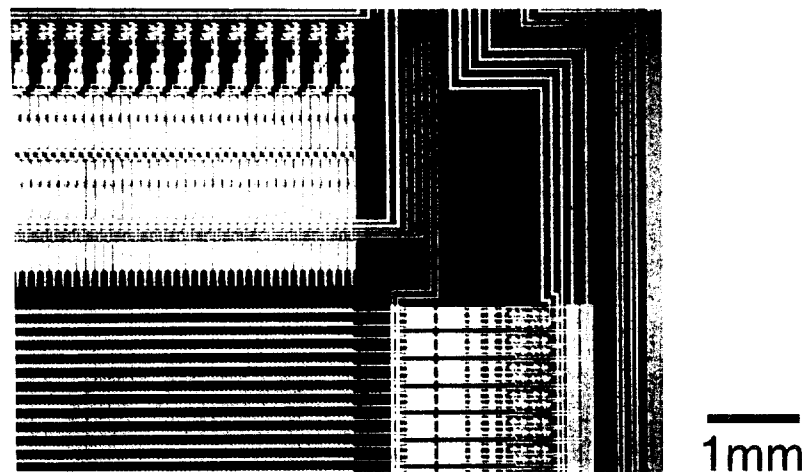


Fig. 7.24. Configuration of 3.8" poly-Si TFT-LCD with full integration of CMOS driver.

operation speed of the data driver of the TFT-LCDs with various resolutions (frame frequency 60 Hz) were estimated as follows:

VGA(640x3x480):	12.5 MHz
XGA(1024x3x768):	5.1 MHz (8 phase video signal)
	3.4 MHz (12 phase video signal)

Therefore, 18 MHz was sufficiently high enough for driver integration in TFT-LCDs.

Fig.7.24 shows configuration of a 3.8" poly-Si TFT-LCD with full integration of CMOS driver. Off-set gate structure was used for these n-channel TFTs. Data drivers were composed of shift resistors and sampling and holding circuits. Scan drivers were composed of shift resistors and multi-step inverter drivers. Fig. 7.25 is an example display image in full color presentation of the poly-Si TFT-LCD with CMOS driver. Operation performance of the large scale driver circuits and the full area display presentation proved that uniformity and high-performance TFT characteristics were realized in large substrate area using developed process technologies.

Fig.7.26 shows operation characteristics and application fields of various circuits. In this study, the 18 MHz circuit performance was confirmed which should be applicable to mobile communicators, but considering future systems on panels which will integrate interface and controller circuits, high operation logics of over 100 MHz should be expected. A c-TFTs will be the next target.

7.7 Conclusions

The key technologies to realize high-performance CMOS TFTs were developed.

In laser crystallization, step scanning using a square beam cannot compensate for nonuniformity of laser intensity in the beam and instability of the laser pulse generation. Introducing a line laser beam with a top flat shape and fine pitch scanning, noticeably improved uniformity of the TFTs.

Leakage currents of n-channel TFTs were reduced by employing off-set gate or LDD structures.

PECVD of SiO₂ using TEOS-O₂ system was optimized. Increasing reaction gas pressure and heater temperature improved TFT performance.

Ion doping conditions were optimized to use the resist mask for CMOS doping. Slightly high energy (5 kV) and short doping time (6-10s) realized resist mask doping of phosphorus and boron.

These developed key technologies were used to get high-performance CMOS TFTs. Shift resistor was driven at 18 MHz and V_{DD}=12V and a

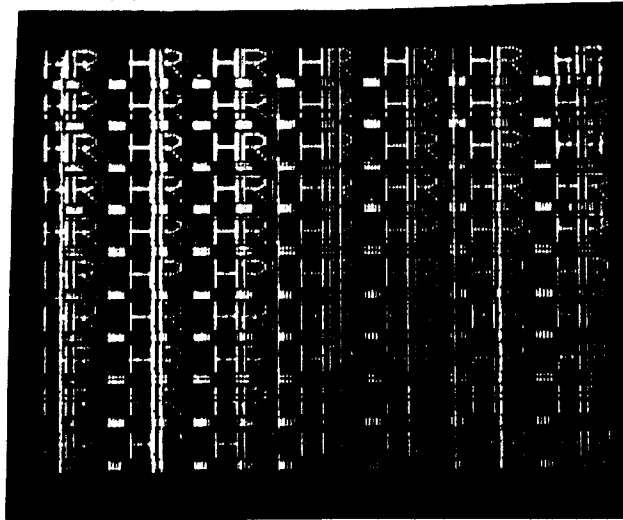


Fig. 7.25. Example display image of the poly-Si TFT-LCD with CMOS driver.

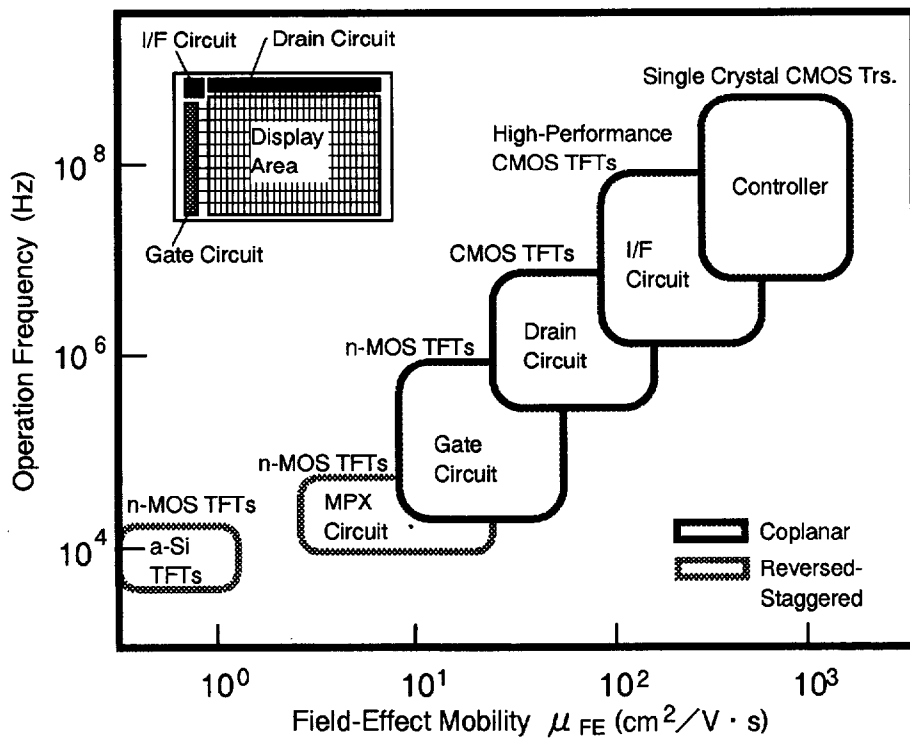


Fig. 7.26. Operation frequency and applicable fields of various circuit types.

3.8" poly-Si TFT-LCD with fully integrated CMOS driver was operated successfully and full color presentation was realized.

7.8 References

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Evolutionary TFT-Process Technologies

Today's LSI technologies have originated from the development of simple polycrystalline TFTs. But the current poly-Si TFT fabrication process has returned to the complicated LSI process.

To simplify the fabrication process and to advance the performance of CMOS poly-Si TFTs for system integration, enterprising technologies are studied. A novel CMOS ion doping technology with a one resist mask process is proposed using compensation and inversion of the thinly doped layer. The TFT characteristics are comparable to those of the conventional two mask CMOS TFTs.

In addition, a new multi-chamber processor with three PECVD reactors and laser annealer is developed to realize the novel crystallization process. Underlayer SiO_2 and a-Si deposition, and direct laser crystallization are continuously carried out in the processor and flat ($R_{\text{rms}} \leq 4$ nm) and large ($0.5\text{-}1\mu\text{m}$) poly-Si grains are obtained. Moreover, the continuous process of laser crystallization of pre-patterned Si island and gate SiO_2 deposition is also explored to realize a clean interface. A location control technique of the large grains ($1\text{-}1.5\mu\text{m}$) is also confirmed.

8.1 Introduction

8.1.1 Demands for more advanced process technologies

Low-temperature poly-Si TFTs should be a promising route to realizing large area microelectronic devices. Producing low-temperature poly-Si TFTs on glass substrates, however, required additional technologies. Compared to the a-Si TFT, further processes, including laser crystallization, gate insulator SiO_2 deposition, and ion doping and activation were needed.

These key technologies have been refined and utilized to realize high performance CMOS poly-Si TFTs below the 450°C process temperatures as described. A 3.8" TFT-LCD with full driver integration, that is nearly commercially practical, was successfully demonstrated in the previous chapter. To maintain the advantage of driver integration in poly-Si TFT-LCDs, TFT fabrication cost (process steps) must be minimized, since in the CMOS configuration, two photomask steps were added.

Concerning poly-Si film preparation, deposition of SiO₂ and a-Si film, and laser irradiation have been carried out in discrete CVD machines and the laser annealer. The precursor of Si was deposited by LPCVD in the batch process which should be converted to a single plate treatment capable of handling large substrates. In an ideal production, procedures for transportation between the machines, pre-heating and pre-cleaning must be minimized to avoid contamination and to increase throughput.

In particular, the higher performance poly-Si TFTs should be used for the novel system integration on the display panel (SOP) [1]. The total TFT performance can be increased by the scaling rule [2], such as decreasing channel length and gate SiO₂ thickness. A TFT located in a single crystal grain should have ideal performance [3]. Therefore, even larger, flatter, and higher quality poly-Si grains in which their positions can be predesignated, will become indispensable.

8.1.2 Simple CMOS doping process

An application of a bucket-type ion source for non-mass-separated ion doping and laser activation for large glass substrates had been implemented. But in CMOS configuration, the number of photomask steps was increased from 6 to 8 because the ion doping process required two more masking steps. To maintain the advantage of poly-Si TFT-LCDs in fabrication cost, process steps must be minimized. For one-mask CMOS doping, there are conventional ideas to compensate by higher dose rates using ion implantation which can control the rate precisely. In the beginning of this chapter, shallow doping conditions are optimized to simplify the ion doping process using the machine developed in Chapter 6. Then, a novel technology for the one-mask CMOS ion doping is proposed using compensation and inversion of the thinly doped layer.

8.1.3 Flat and large poly-Si for system on panel

The grain boundary has a high density of states and acts as a barrier for carriers and a generation center for leakage current. The ideal TFT performance should be realized by TFT fabrication in the single crystal region eliminating the grain boundary, at least in the channel region. Considering the integration of interface and logic circuit with higher performance, the operation of the TFT must be maximized. For example, in the constant-voltage scaling rule, the effect of channel length and gate SiO₂ thickness can be shown as follows.

$$\begin{aligned} I_D &\propto 1/L && \text{-----(8-1)} \\ I_D &\propto 1/t_{ox} && \text{-----(8-1)} \end{aligned}$$

And the operation frequency f of TFT is shown as follow.

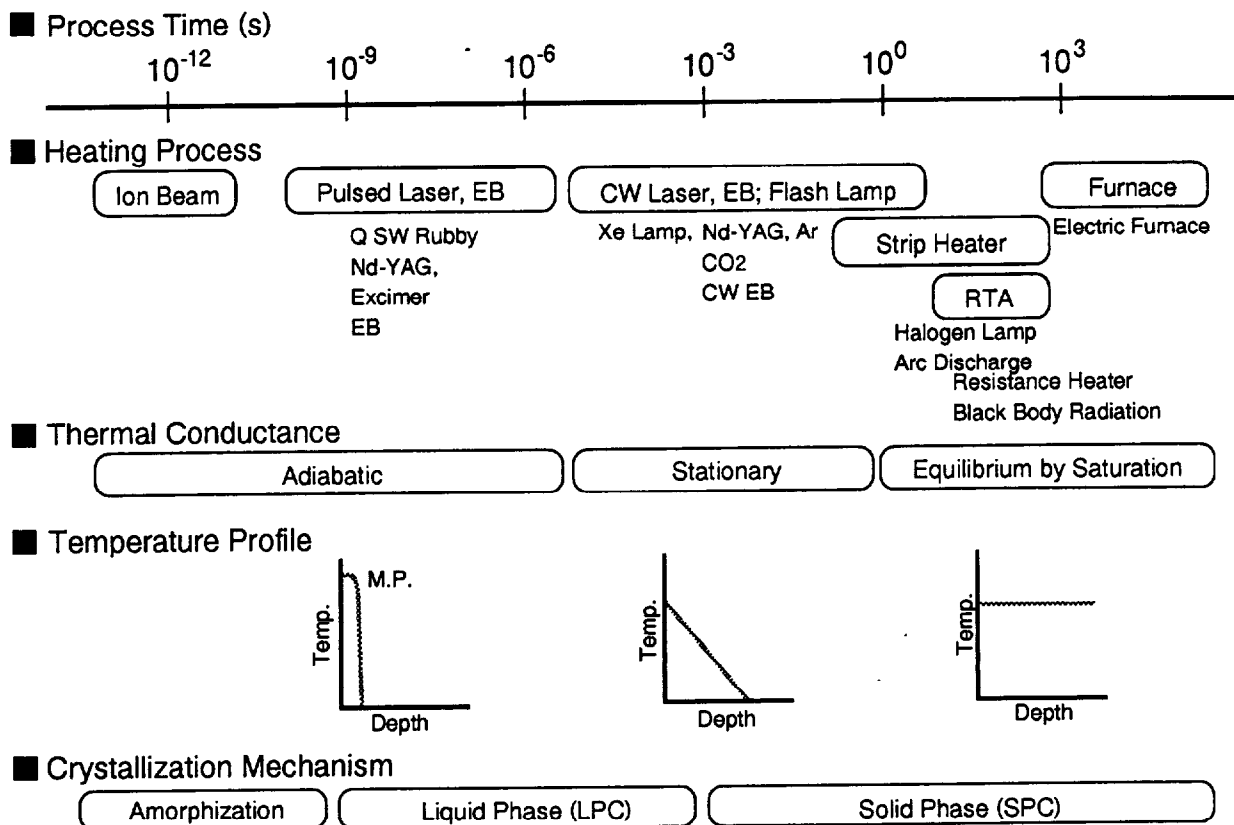
$$f \propto 1/L^2 \text{ -----(8-3)}$$

Thus, reducing the channel length and thinning the gate oxide are effective in increasing TFT performance. If TFTs with lengths in the order of submicrons are used in logic circuits, fortunately, single crystalline grain sizes of only $1\mu\text{m}$ square are necessary to build the TFT into it. The thin gate oxide TFT can be easily realized by only depositing a thin CVD SiO_2 , but a high quality oxide with good step coverage must be applied. The problem characteristic to laser crystallized poly-Si film is that ridges exist and this causes degradation of the on-characteristics and stability of TFTs [4]. Therefore, poly-Si with flat surfaces is indispensable to use thin gate oxide.

Fig.8.1 illustrates the relationship between heat processing time, thermal conduction, and the crystallization mechanism [5], [6]. Long heating times are applied for solid phase epitaxy (SPE) [7] or SPC. Slightly shorter heating times using CW laser [8], CW electron beam [9], or strip heater [10] (or RF-ZMR) show stationary heat flow and may easily cause lateral crystallization. However, there is a trade-off in that as glass substrate temperature rises during the crystallization process, very fast CW Ar laser beam scanning is necessary [11]. Short wave pulsed laser irradiation (20-200 ns) can selectively heat only the Si film surface to the melting point without substrate damage. But in such short process times, control of the lateral heat flow must be explored to realize lateral crystallization.

Low-temperature crystallization of Si films by excimer laser pulse has made great progress. Linear beams with lengths of 150-360 mm were developed for high throughput annealing. By optimizing the conditions of Si film deposition, Si film thickness, laser irradiation and substrate temperature, very high electron field-effect mobilities of 440-640 $\text{cm}^2/\text{V.s}$ are attained [12], [13]. To obtain these high performances in a practical process, the effective route is to ultimately increase the crystalline quality of poly-Si films [12]. Recently, many novel studies based on crystallization techniques for large grains have been presented.

Fig.8.2 shows typical examples of lateral growth methods. The basic idea in obtaining large grains is to have the same lateral growth as RF-ZMR (Chapter 4). In RF-ZMR ((a)), lateral heat flow under compulsory control is obtained with a zone-melting speed (5 mm/s) which is very low compared to the solidification speed from the liquid state ($\geq 1 \text{ m/s}$) [14]. Thus, complete lateral growth is realized. On the contrary, in conventional excimer laser crystallization ((b)), heat flow is almost perpendicular to the substrate and crystal growth is initiated from the interface to the film surface. When the laser intensity is controlled to survive seeds, large grains are formed by the super-lateral growth regime [15]-[17], as in Fig.7.5. Further large grain growth is enhanced mainly by recrystallization by multi-irradiation [12], [14]. The induced lateral growth is realized by suppressing the heat flow to the bottom of the Si film and draining the heat to the heat sink surrounding the poly-Si film ((c)) [18]. Producing large grains and controlling their location are



Fog.8.1. Processing time and thermal behavior associated with the various beam-processing or bulk-heating techniques. The lower part of the figure shows solidification processes in Si [5], [6].

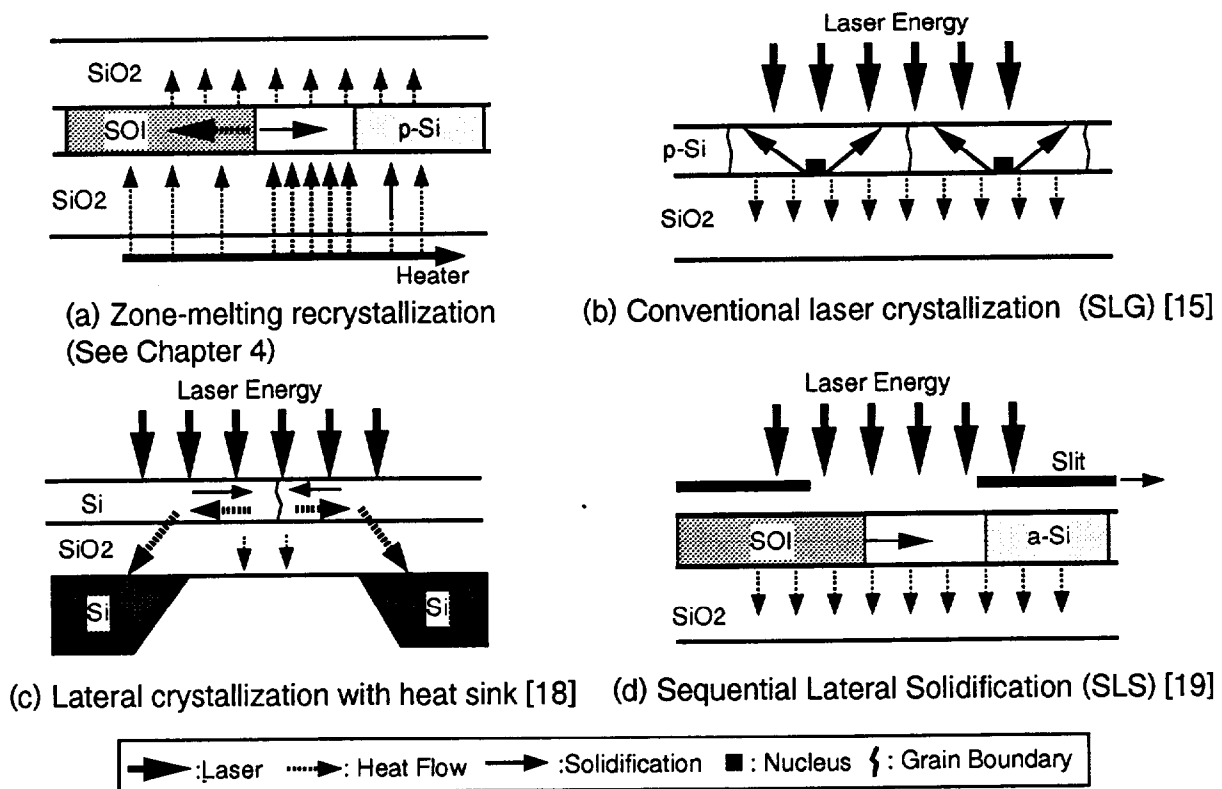


Fig.8.2. Examples of lateral growth by controlling heat flow.

realized simultaneously by sequential lateral solidification (SLS). Step irradiation through the scanning slit and using the previously crystallized poly-Si grain as a seed, lateral solidification speed is enhanced ((d)) [19].

Fig. 8.3 shows a schematic image of the crystal-Si TFT (c-TFT or x-TFT) which is expected to give ultimate performance. The channel region is fabricated in the large single crystal grain. Since the TFT has no grain boundary in the channel region, extremely high field-effect mobility and low off-current are expected. The TFT active area had no grain boundary which gives a high density of states to cause generation of the field-enhanced thermal generation leakage current. The c-TFT is a reasonable structure to realize on glass substrates and should be the key device for SOP.

To realize c-TFT, more advanced techniques for the control of the location of large grains have been proposed. Fig.8.4 shows typical examples to locate nuclei sites (low temperature region) and promote and to control lateral growth produce large grains. The basic technique promotes lateral growth using a temperature gradient. The temperature gradient is formed by spatial modulation of the laser irradiation by the phase shift technique ((c)) [20], [21] or by using a film structure with a heat sink ((d)) [22], [23]. But these techniques need special conditions for proper laser energy, film thickness, materials and structures.

In this experiment, a new multi-chamber processor was developed for poly-Si TFTs (Fig.8.13). Fig.8.5 illustrates the configuration of the CVD process and laser annealing. In the conventional process, the substrates are transported between discrete machines. In the new process, substrates are transported in the vacuum automatically and various novel process combinations become possible.

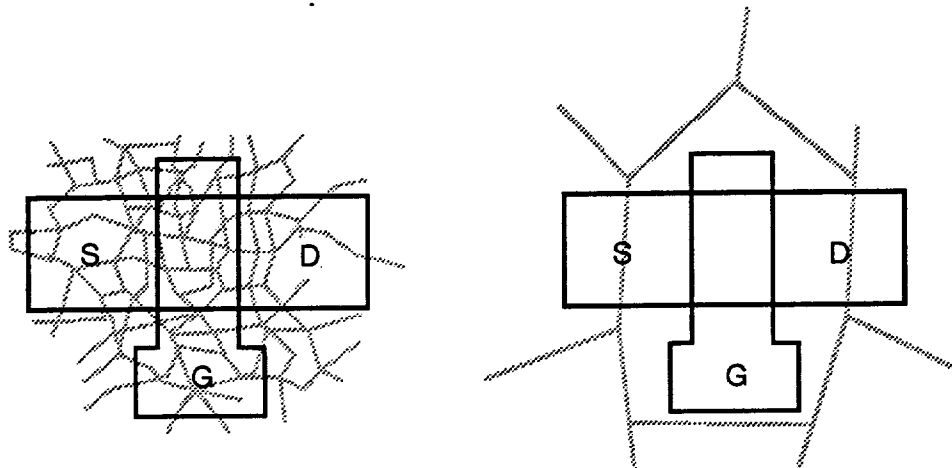
First, the continuous process of PECVD deposition of underlayer SiO_2 and a-Si, and direct laser crystallization of a-Si were studied to obtain flat, large grains. Furthermore, the continuous process of laser crystallization of pre-patterned Si islands and gate SiO_2 deposition is also explored to realize a clean interface. Finally, control of the large grain locations is explored by applying the step of underlayer SiO_2 .

8.2 One-mask CMOS doping

8.2.1 One-mask CMOS doping process

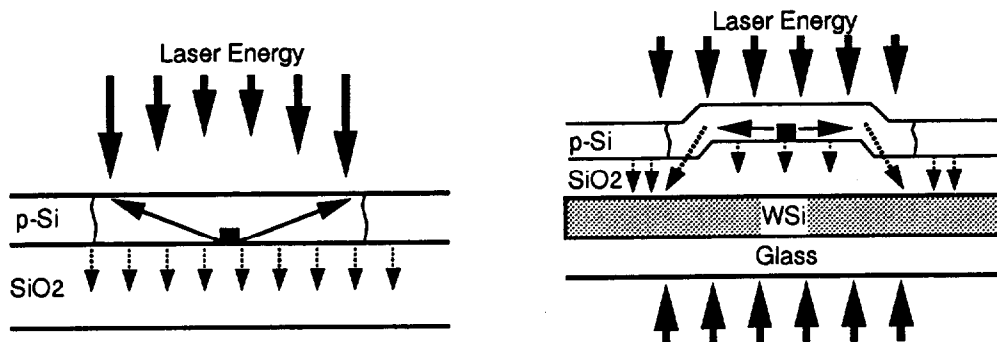
The basic technology of one-mask CMOS doping is compensation and inversion of thinly doped layer. Reduction of high surface concentration is preferable for easy compensation. Phosphorus doping was selected for the first doping because its projection range is shallow and its removal is easy.

Fig.8.6 illustrates the coplanar CMOS TFT process on 100 mm x 100 mm glass substrates using the conventional two-mask doping process and the novel one-mask doping process. In the two-mask doping process, first a 50 nm thick Si film was deposited by LPCVD at 450°C using Si_2H_6 on the underlayer PECVD SiO_2 . After laser crystallization using XeCl



(a) Conventional TFT with grain boundaries in channel region (b) c-TFT without grain boundary

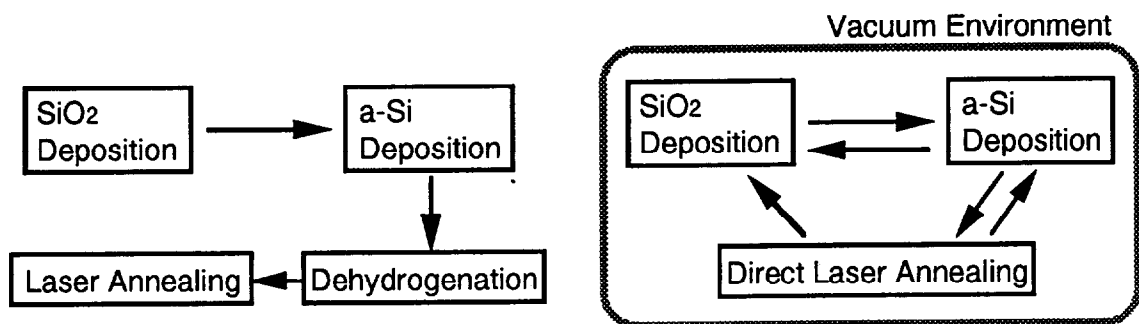
Fig.8.3 Schematic structure of crystal-TFT (c-TFT) without grain boundary.



(a) Temperature gradient method [20], [21] (b) Patterned heat sink method [22], [23]



Fig.8.4. Examples of location control of large poly-Si grains.



(a) Conventional discrete process

(b) Proposed continuous process in vacuum

Fig: 8.5. The proposed continuous process with CVD and laser annealing.

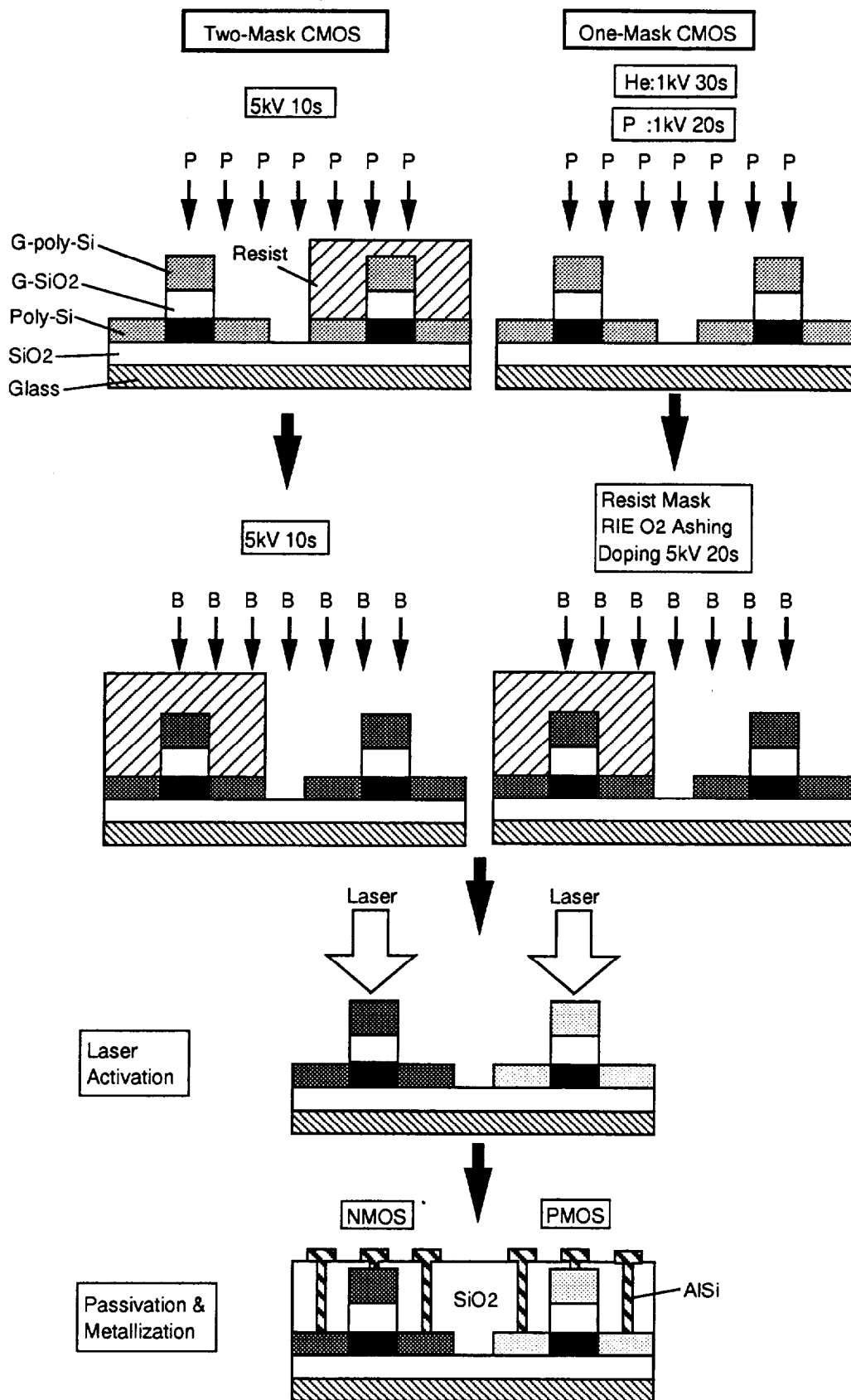


Fig.8.6 Two-mask and one-mask doping processes for CMOS TFTs.

excimer laser with an energy of 400 mJ/cm^2 , the poly-Si film was patterned into islands. Gate insulator SiO_2 and gate poly-Si with thicknesses of 100 nm were deposited by PECVD and LPCVD, respectively. After gate patterning, the p-channel region was protected by photoresist and phosphorus was doped at 5 kV for 10 s in the n-channel region. After removing the resist, the n-channel region was covered by resist and boron was doped into the p-channel region. Laser activation was carried out at 200 mJ/cm^2 after removing the resist. Hydrogenation was done at 300°C for 60 min after passivation by PECVD SiO_2 and AlSi metallization.

In the one mask CMOS doping process, first, helium ions were irradiated at 1 kV for 30 s to remove natural oxides and phosphorus was continuously doped at 1 kV for 20 s in the same doping chamber. Then, the n-channel region was protected by resist. Oxygen ashing was applied on the p-channel region for 6 min in the RIE machine to remove the high concentration surface layer. Then, boron was doped at 5 kV for 20 s to invert the doped area from n-type to p-type. In this process, low energy shallow doping of phosphorus and reduction of the surface concentration by RIE ashing completed the inversion.

Fig.8.7 shows the effect of surface cleaning before shallow ion doping of phosphorus (1 kV) on sheet resistance. Chemical cleaning with HF solution only slightly reduced sheet resistance because the Si surface was re-oxidized in the air before setting in the doping chamber. Ion beam surface treatment followed by ion doping in the same doping chamber greatly reduced the sheet resistance. Hydrogen ion beam irradiation clearly reduced the sheet resistance implying effects of both reduction and ion bombardment. Helium ion irradiation was more effective in increasing doping efficiency and reducing sheet resistance. A low energy helium ion beam should have a moderate ability in removing natural oxides.

Fig.8.8 shows plots for XPS profiles of silicon with and without helium ion treatment before phosphorus doping. The surface was step etched during analysis by low energy Ar ions. Profiles of initial and 60 s etching are shown. Helium ion irradiation before ion doping reduced the natural oxides to promote shallow doping, and these data supported the results of Fig.8.7.

The key process in one-mask CMOS doping was reduction of the surface concentration before opposite type doping to facilitate inversion. Fig.8.9 shows concentration profiles measured by SIMS and the effect of RIE ashing of the thinly doped phosphorus layer before boron doping (Fig.8.6). Without the ashing process, the phosphorus showed a high concentration profile. With ashing, the shallow and high concentration phosphorus layer was removed and after laser activation, the concentration became one order of magnitude lower than the as-doped one. Thus, boron compensated for the phosphorus well in the p-channel region ((b)).

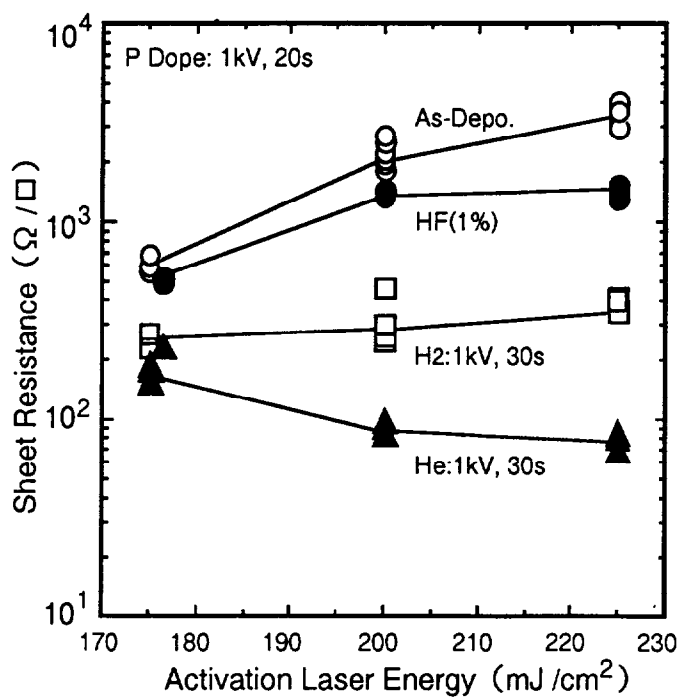


Fig.8.7 Effect of surface cleaning before ion doping on sheet resistance.

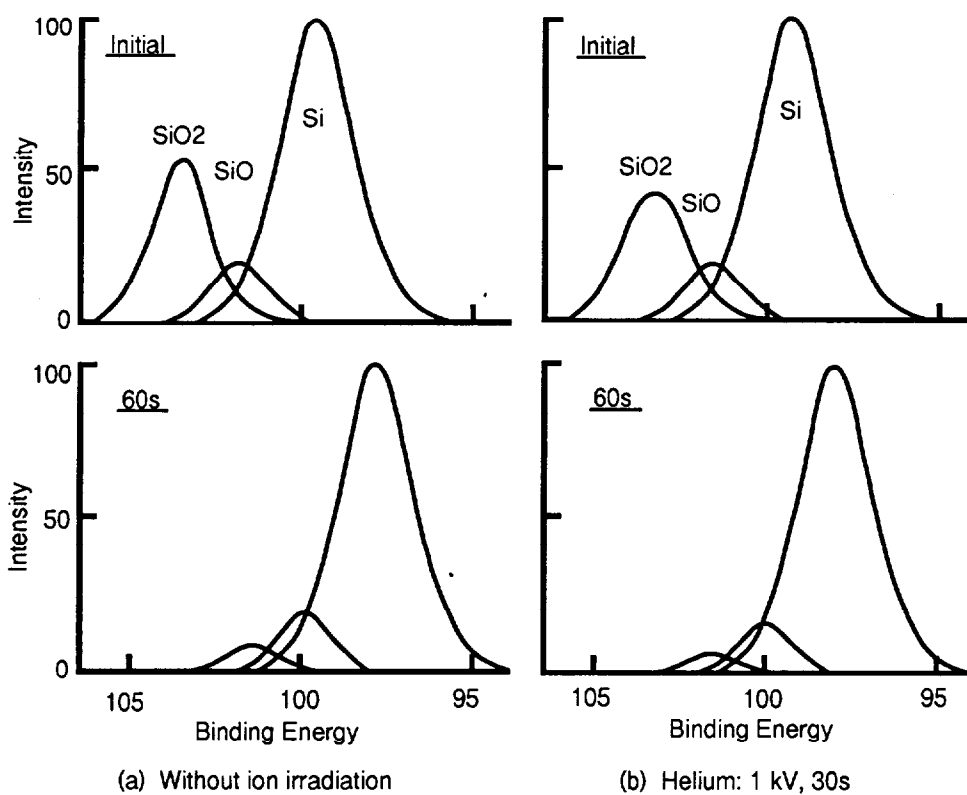


Fig.8.8 Effect of surface cleaning by helium ions on XPS profiles of silicon.
Doping: P, 1000V, 20 s.

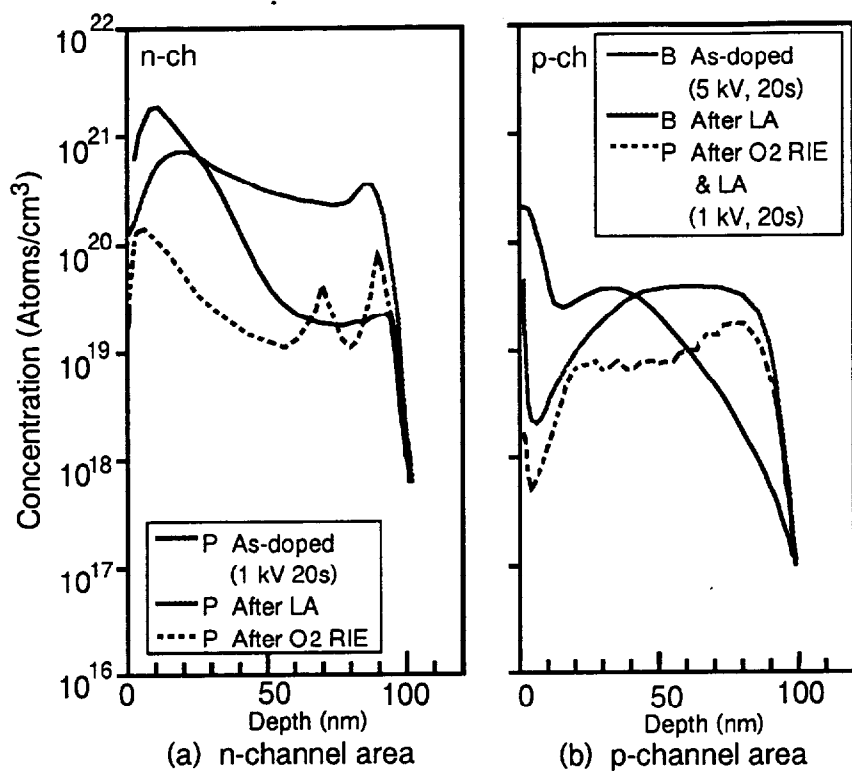


Fig.8.9 Concentration profiles of P and B doped by one-mask process.

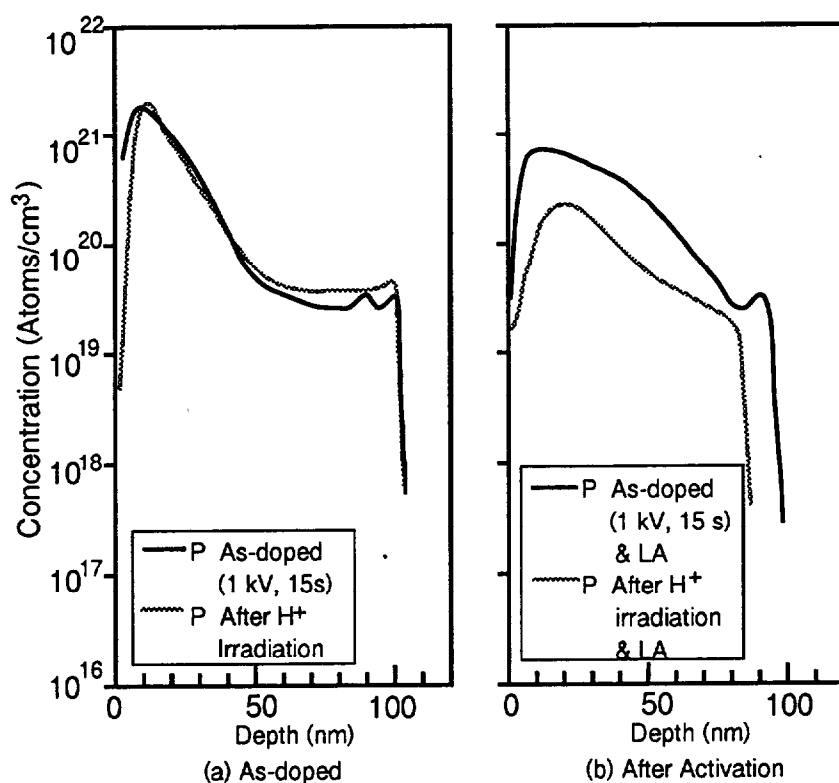


Fig.8.10 Effect of H^+ ion irradiation on phosphorus concentration profiles measured by SIMS.

Fig.8.10 shows effect of hydrogen ion irradiation on phosphorus concentration profiles. Hydrogen ion treatment also reduced the surface concentration and total content of phosphorus after laser activation. This process is carried out in the doping chamber continuously followed by opposite type ion doping.

8.2.2 Characteristics of one mask CMOS TFTs

Fig.8.11 shows the V_G - I_D characteristics of TFTs fabricated by one- and two-mask CMOS doping processes using pre-RIE O_2 ashing. Both the one- mask and two-mask processed TFTs had high performance characteristics, though mobility was slightly lower for the p-channel TFT and the off- current was slightly higher for n-channel TFT produced by the one mask process. Fig.8.12 shows the V_G - I_D characteristics of TFTs fabricated by one- and two-mask CMOS doping processes using hydrogen ion pre-irradiation before boron doping. Though, the n-channel TFT of one-mask process had a slightly higher off-current, it had comparable characteristics to the two-mask TFT.

Thus, the novel one-mask doping is a promising way to simplify the CMOS doping process using a large-area, high-speed ion doping machine.

8.3 Fabrication of flat and large poly-Si grains

8.3.1 Novel multi-chamber processor for poly-Si TFTs

The usefulness of continuous process for crystallization and gate insulator deposition was reported [13], [24] and a multi-chamber type processor for poly-Si TFT was proposed [25]. In the present study, a prototype apparatus was developed to identify the effects of the continuous process and to develop new process configurations.

Fig.8.13 shows the multi-chamber processor with three PECVD reactors and the laser annealer. The substrates (150 mm x 150mm) were transported in a vacuum between four chambers by automated handling. Underlayer and gate SiO_2 , and a-Si were deposited by TEOS- O_2 and SiH_4 - H_2 systems, respectively. PECVD a-Si is a reasonable precursor of Si because it is available on large glass substrates at low temperatures. The deposition of a-Si was based on a-Si TFT process conditions. The a-Si films were crystallized by the line beam of an excimer laser (308 nm) with substrate heating. Thus, all procedures could be carried out continuously and reciprocally at elevated temperatures.

Fig.8.14 illustrates possible examples of continuous processes. The fundamental procedure continues depositions of the underlayer SiO_2 and a-Si with laser annealing in the processor ((a)). The technique should contribute to omitting pre-heating and pre-cleaning of the substrates at each step. In a-Si TFT fabrication, gate insulator SiN and a-Si layer are continuously deposited to realize stable production. And also in staggered poly-Si TFT, a-Si deposition, laser crystallization and gate SiO_2 deposition are continuously carried out and high performance can be realized [13]. In the coplanar structure, laser annealing and successive

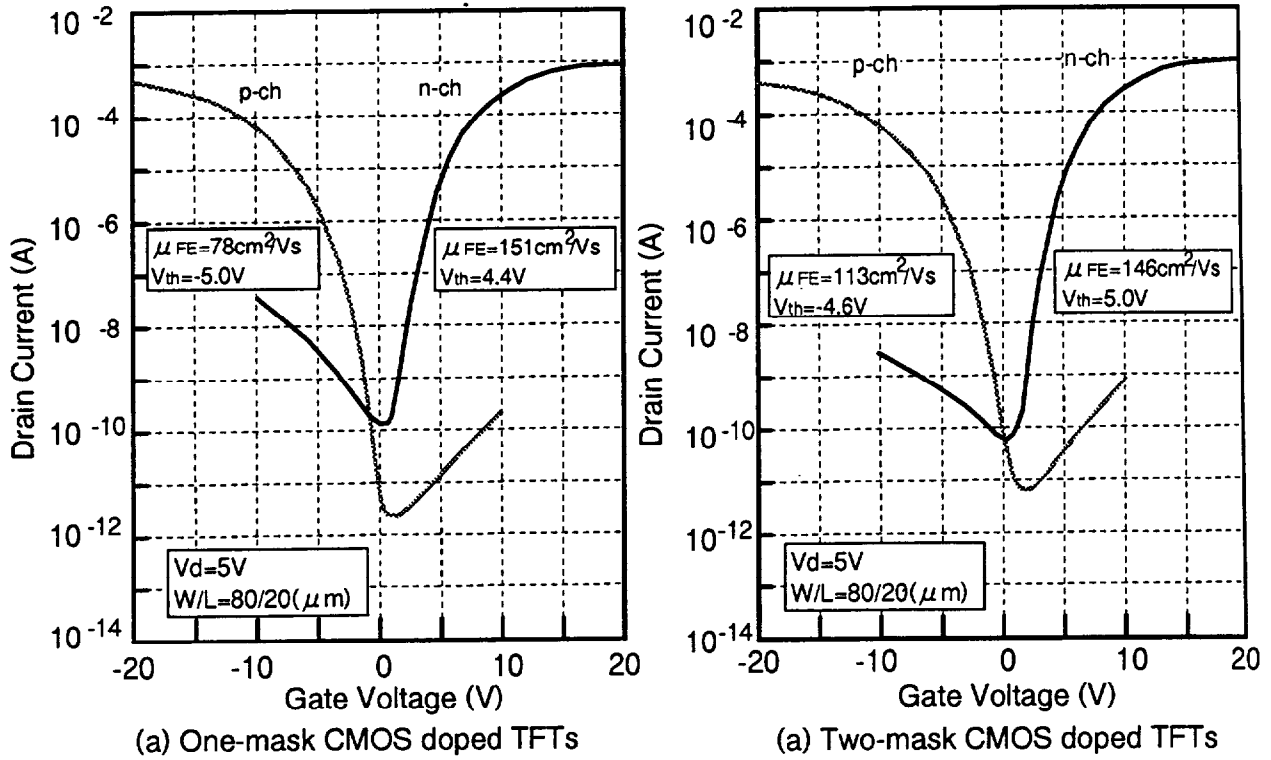


Fig.8.11 Gate voltage-drain current characteristics of CMOS TFTs by one- and two-mask doping processes using He ion pre-cleaning.

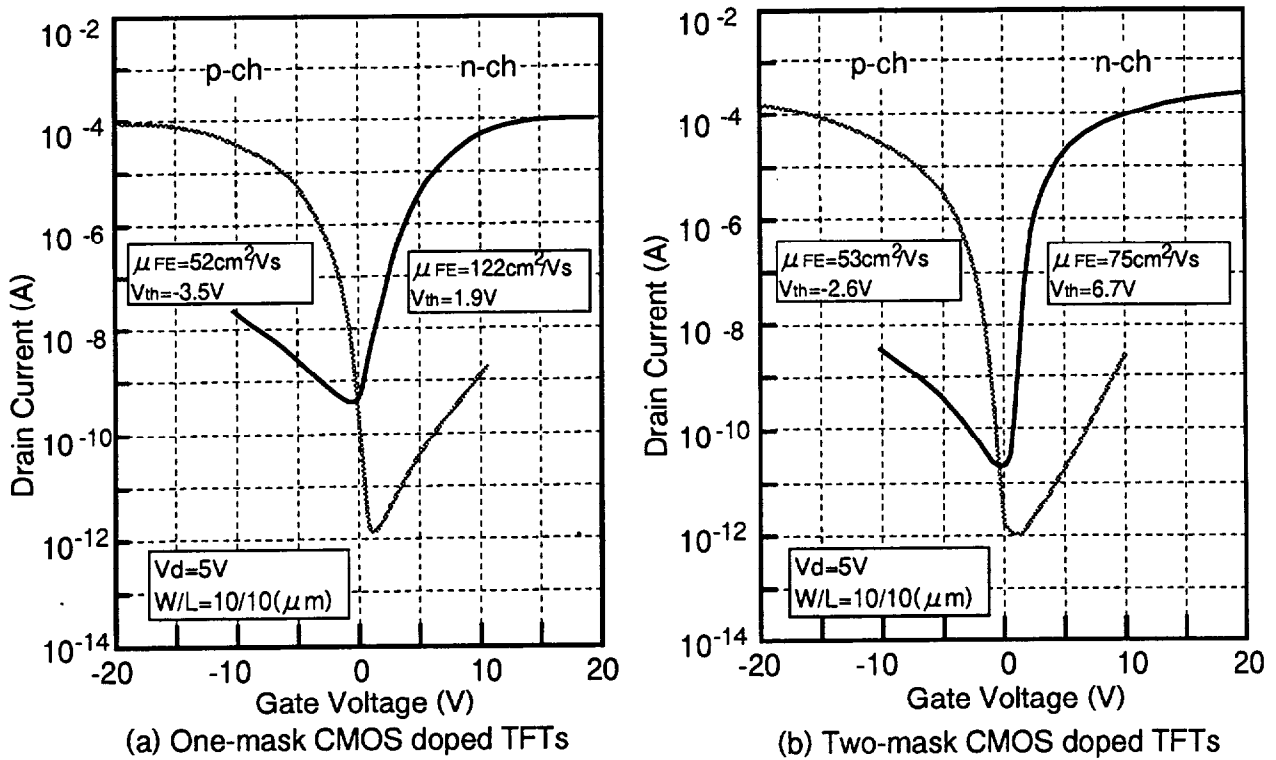
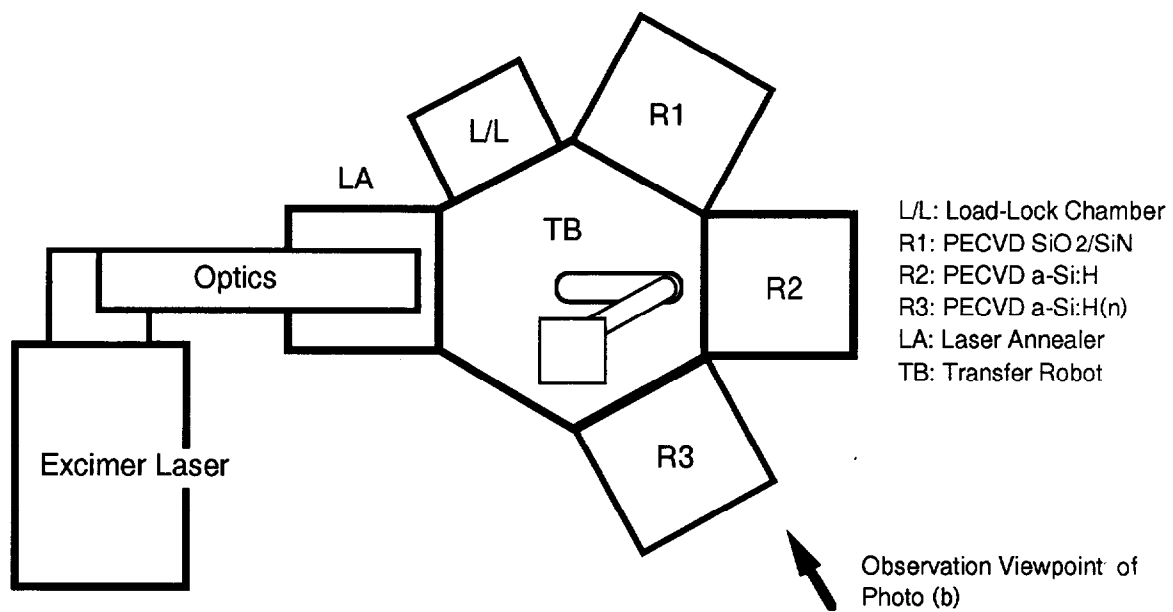
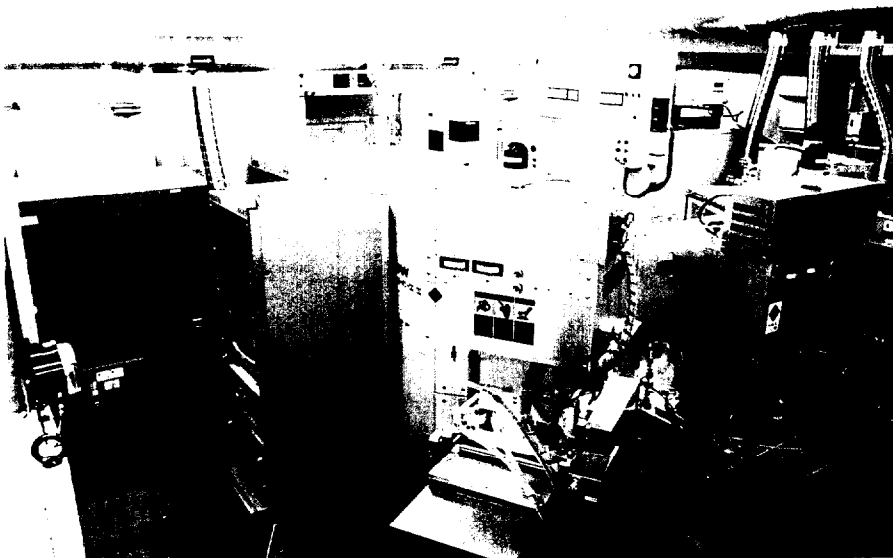


Fig.8.12 Gate voltage-drain current characteristics of CMOS TFTs by one- and two-mask doping processes using hydrogen ion pre-etching.

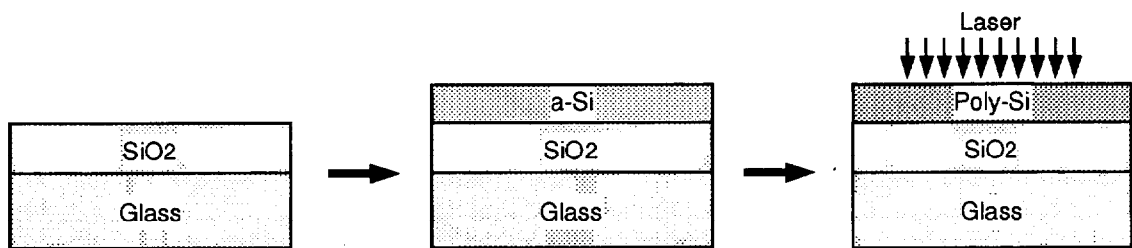


(a) Schematic of total configuration

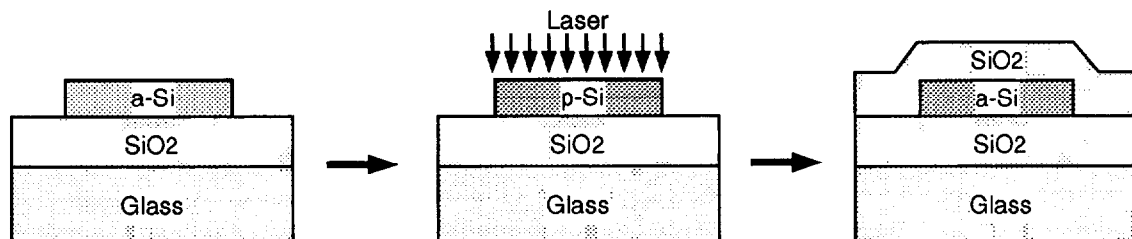


(b) Photograph of the apparatus

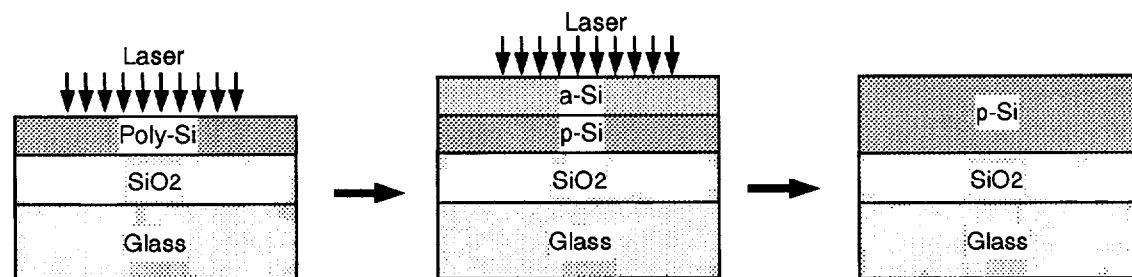
Fig.8.13. Developed multi-chamber processor for poly-Si TFTs.



(a) SiO₂ and a-Si deposition and direct laser crystallization



(b) Crystallization of Si islands and gate SiO₂ deposition



(c) Two-layer poly-Si crystallization with continuous a-Si deposition and laser irradiation

Fig.8.14. Examples of continuous processes for poly-Si TFTs in vacuum.

gate SiO₂ deposition ((b)) corresponds to that process and realization of a clean interface is expected. In this process, laser irradiation on Si islands is necessary [26], [27]. In process (c), large poly-Si grain should be generated. A trial was reported using discrete means to enlarge the laser energy window and to obtain large grains [28]. Many other novel applications should be possible.

In this section, examples of the studies for processes (a) and (c) are described.

8.3.2 Preparation of PECVD a-Si

Fig.8.15 shows the dependence of hydrogen content on a-Si deposition conditions. Hydrogen content depended neither on dilution gas nor on gas pressure. It depended on RF power ((a)), and strictly speaking, on anode heater temperature((b)). Low power reaction reduces the Si-H radicals and high temperature deposition is generally an effective means to reduce hydrogen content [25]. The hydrogen content after heat treatment at 450°C for 60 min is also plotted. The value was almost the same with about 4 at.% for all films deposited at various conditions. The annealed Si film was crystallized successfully with one energy step crystallization.

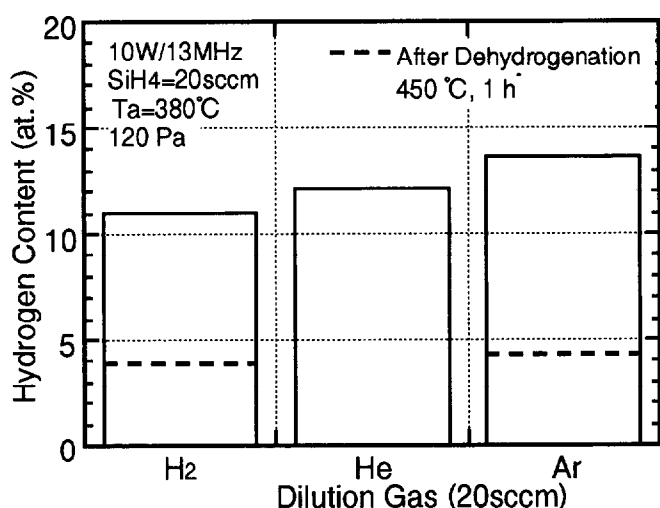
Since the content of 9-11 at.% of the as-deposited film was too large for a one-energy step crystallization without dehydrogenation (direct crystallization), three-step irradiation was applied in this experiment.

Fig.8.16 shows surface photographs of the as-deposited PECVD a-Si films on the underlayer SiO₂ observed by AFM and the dependence of the surface morphology on RF power. At 10 W deposition, the surface was uniform and roughness was less than 5 nm. But at 15 W deposition, roughness was increased and spherical projections were observed. This may be caused by degassing or H₂ emission from the underlayer TEOS SiO₂ at higher RF power. In this study, 10 W deposition was used because discharge at 5 W was unstable.

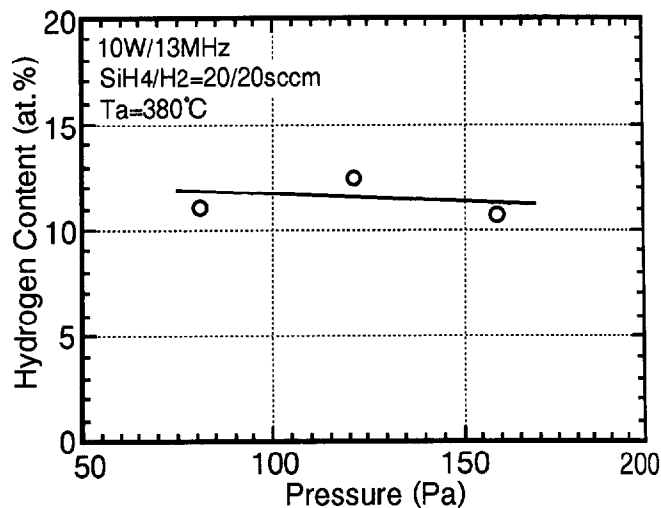
8.3.3 Direct crystallization of thin PECVD a-Si

(1) Discrete crystallization at room temperature

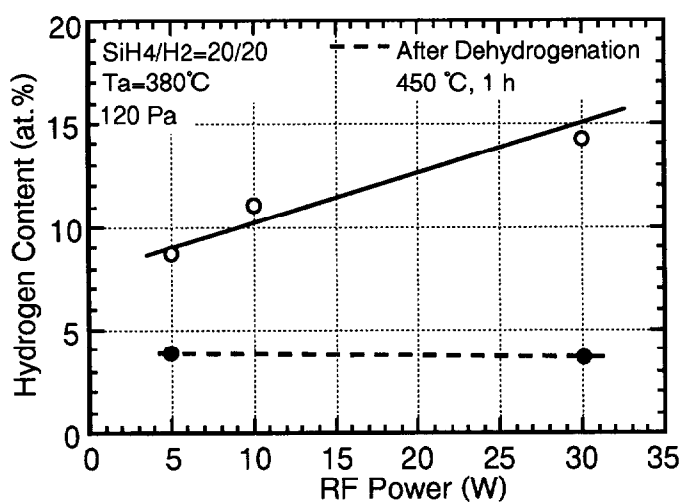
For the basic study of crystallization of PECVD a-Si, the discrete laser process was utilized at room temperature. Surfaces after Secco's etching and cross sections were observed by SEM. Initially, for reference, poly-Si films by LPCVD were observed. Fi.8.17 shows the dependence of morphology on LPCVD Si film (Si₂H₆, 450°C) thicknesses. The optimum energy was selected for each film thickness, but the laser energy value for the 55 nm film was low compared to the standard value because the laser optics were not the same for 35 nm film. The grain size of the 55 nm film was larger than that of the 35 nm film. However both films had high ridges and the values were almost the same as the film thickness. In the one-energy step crystallization of LPCVD Si films, height of the ridges was not reduced by thinning of the film.



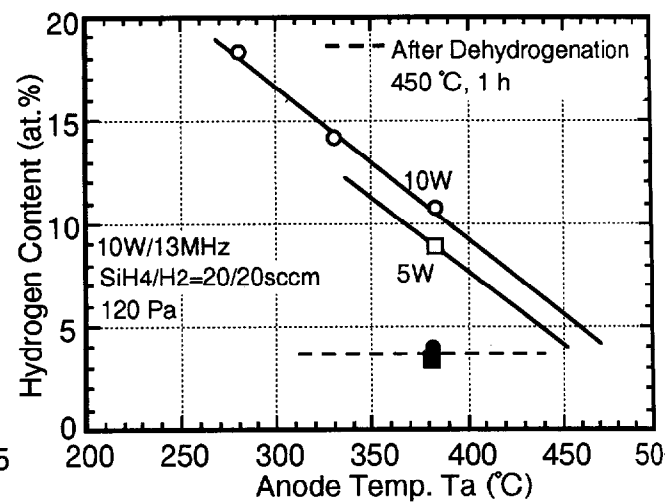
(a) Hydrogen content vs. dilution gas



(b) Hydrogen content vs. gas pressure

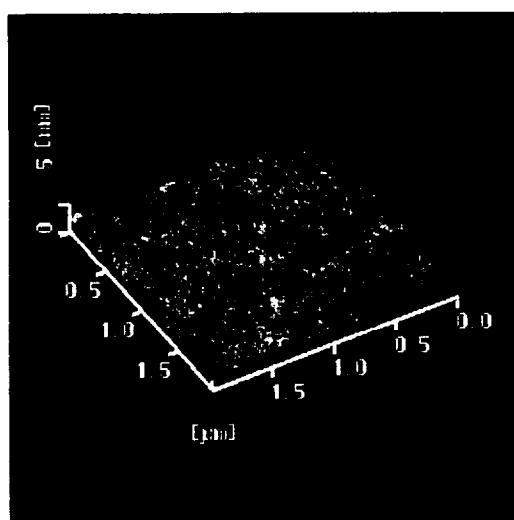


(c) Hydrogen content vs. RF power

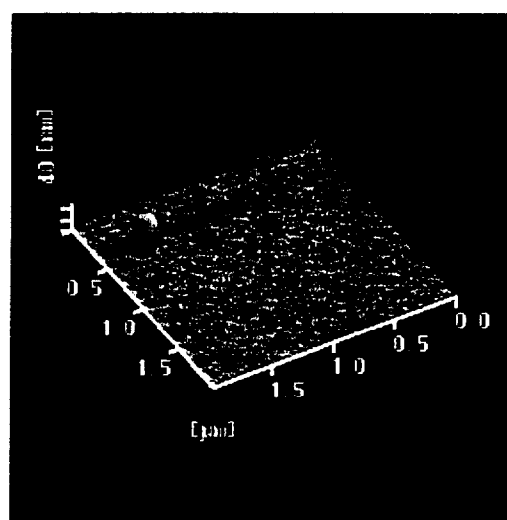


(d) Hydrogen content vs. anode temperature

Fig. 8.15. Dependence of hydrogen content on PECVD conditions.

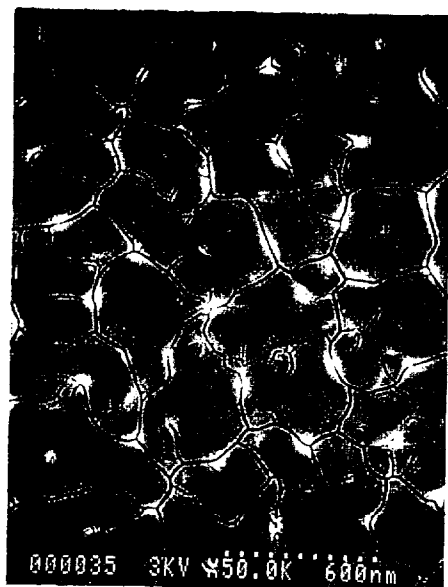


(a) RF: 10 W

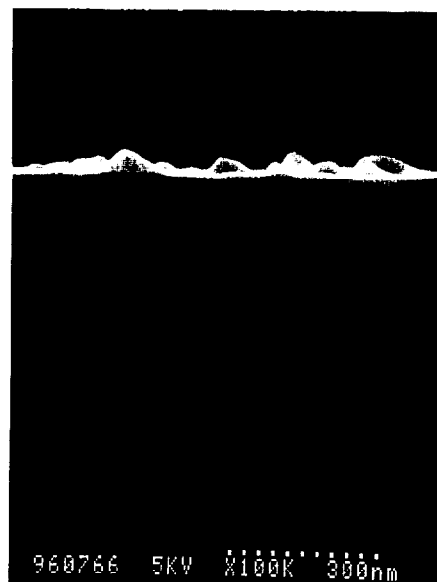


(b) RF: 15 W

Fig. 8.16. Dependence of surface morphology of PECVD a-Si films on RF power.
a-Si(50 nm)/SiO₂(300 nm)/Quartz



(a) a-Si: 35 nm, E_c : 420 mJ/cm²



(b) a-Si :55 nm, E_c : 340 mJ/cm²

Fig.8.17. SEM micrographs of LPCVD Si films crystallized at RT.

Fig.8.18 shows the dependence of surface morphology on PECVD Si thickness. To avoid film abrasion, a three-energy step irradiation was used. The optimum energy settings were selected for each film. In the 25 nm film, grain size was slightly smaller because applied energy was limited to avoid abrasion and formation of pin holes. The other films had almost the same grain size. In the films with thicknesses of 52-44 nm, the ridges were high. But, in film thicknesses below 35 nm, the height was reduced. Considering both grain size and flatness of film, film thickness around 35 nm should be optimum. In the 55 nm film, grain size was almost the same in the energy range of 380 to 420 mJ/cm². The dependence of number of energy steps (max.: 11 steps) was also studied for each thickness. The optimum energy for crystallization was increased by increasing the numbers of steps.

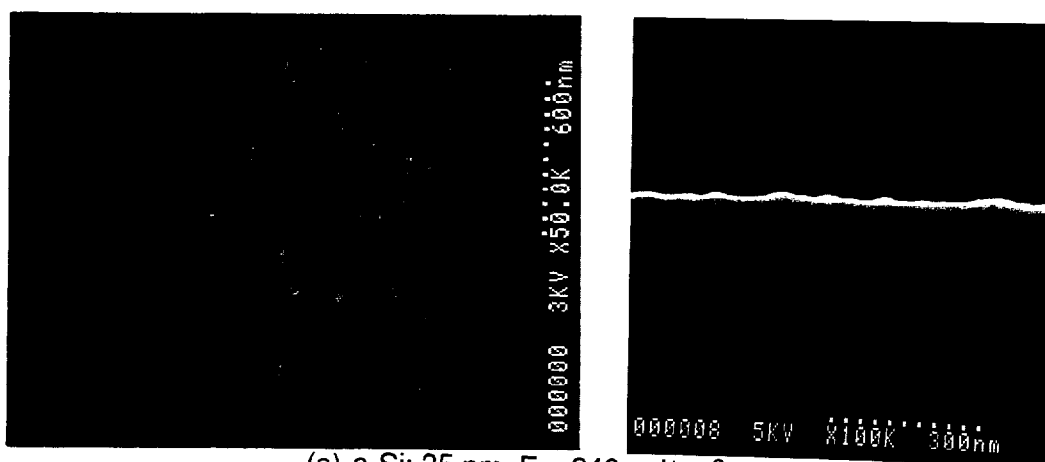
Fig.8.19 shows the dependence of field-effect mobility on film thickness and laser energy. Maximum output laser energy of the machine was 520 mJ/cm². The optimum energy to obtain maximum mobility for each film thickness was decreased by thinning of the film. The maximum mobility was obtained in the TFTs with 35 nm film crystallized at 380 mJ/cm². The results showed that the optimum laser energy was reduced by thinning the poly-Si film. The maximum value of mobility was about 100 cm²/V.s which should be increased by optimizing process conditions such as gate SiO₂ deposition. Thus, in the direct crystallization process of PECVD Si film by multi-energy step irradiation, thinning of the poly-Si film was useful in improving TFT characteristics, just as it was reported that the maximum grain size was increased [29].

(2) Direct crystallization by continuous process

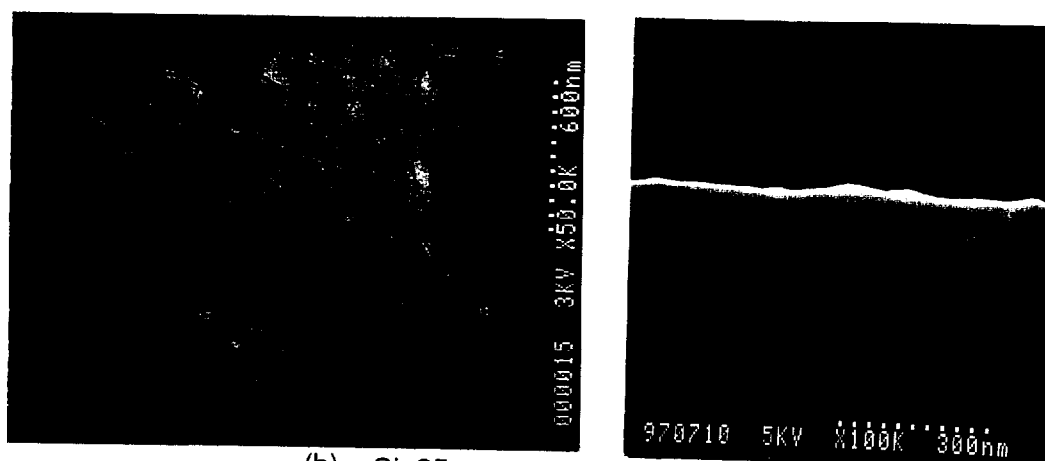
The continuous process at elevated temperatures was studied for thin PECVD Si films.

Fig.8.20 shows SEM micrographs of PECVD Si films with 40 nm thick crystallized at 350°C by continuous process. Photographs (a)-(d-1) and (d-2)-(d-3) were after Secco's etching and as-grown, respectively. The grain size was increased by increasing laser energy and about 1 μm grains were observed at 380 mJ/cm² which was 10% lower than the value at room temperature (Fig.8.18(c)). The laser crystallization at elevated temperatures reduced optimum laser energy even further. The surface was smoother compared to that of the films treated by discrete processes at room temperature. The height of ridges was less than 10 nm.

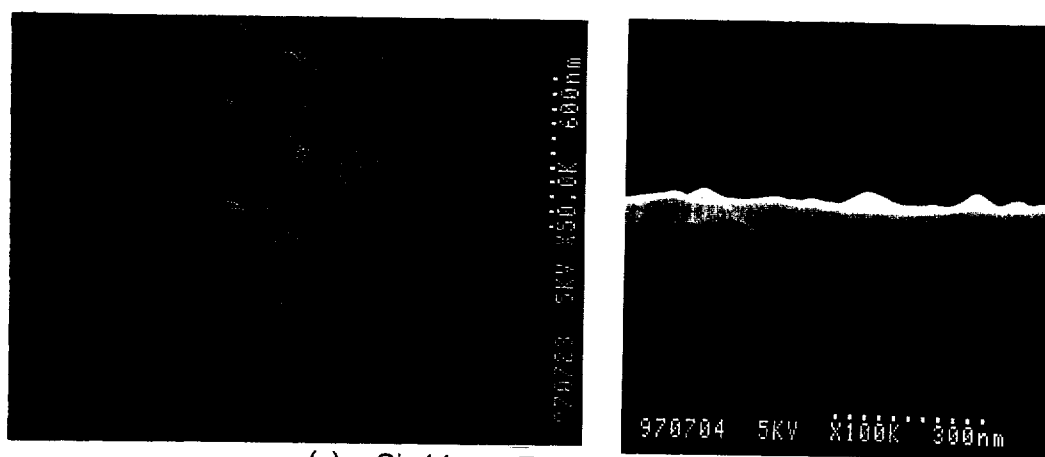
Fig. 8.21 shows scanning electron microscope (SEM) photographs of Secco-etched poly-Si surfaces and as-grown surface morphology in a TFT size area (4x4 μm²) observed by atomic force microscope (AFM). Film thickness was 55 nm. Photo (a) shows the morphology of the conventional film deposited using reactor R2 at 340 °C with the hydrogen content of 11 at.%, and three-step irradiation was used. Photos (b) and (c) are new films with hydrogen content of 6 at.% deposited at 430 °C using reactor R1 with a new high-temperature heater and crystallized by one-step and



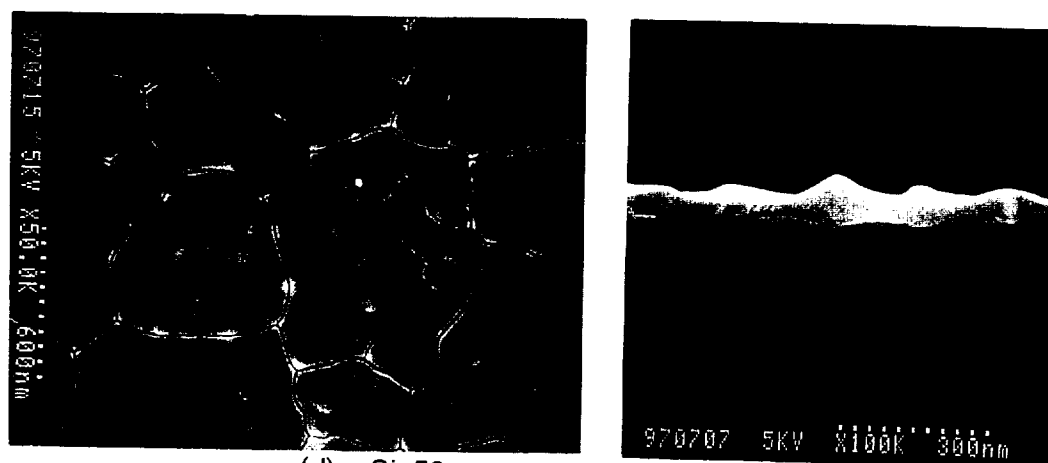
(a) a-Si: 25 nm, Ea: 340 mJ/cm²



(b) a-Si: 35 nm, Ea: 420 mJ/cm²



(c) a-Si: 44 nm, Ea: 420 mJ/cm²



(d) a-Si: 52 nm, Ea: 460 mJ/cm²

Fig.8.18. SEM micrographs of PECVD Si films crystallized at RT.

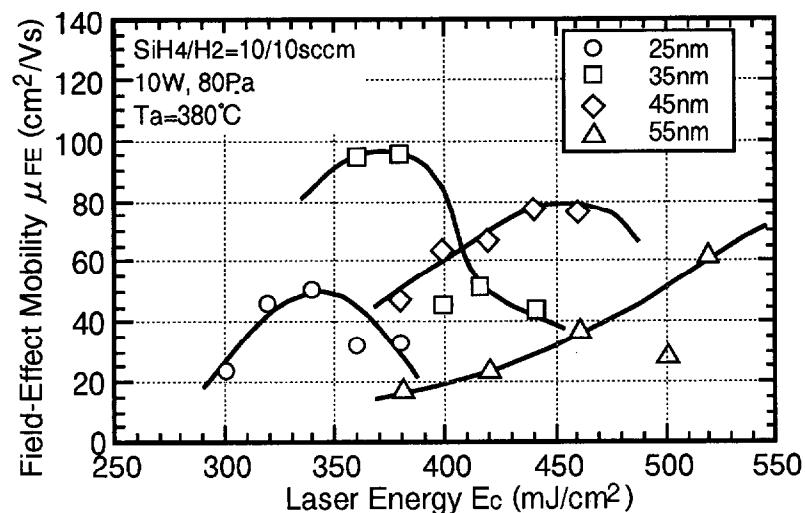
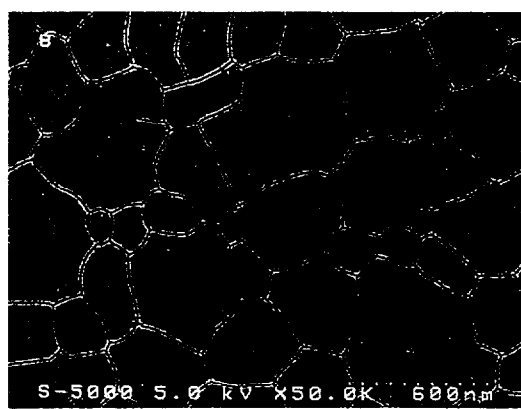


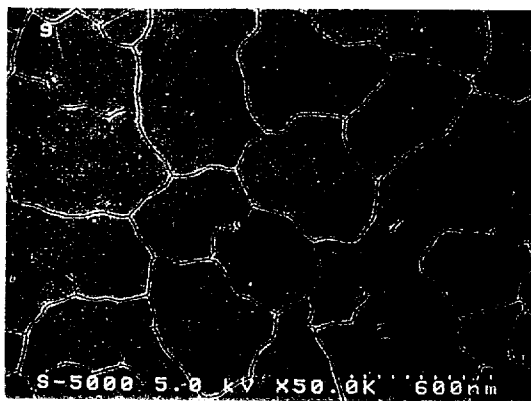
Fig.8.19. Dependence of field-effect mobility on laser energy and film thickness.



(a) 320 mJ/cm²



(b) 340 mJ/cm²



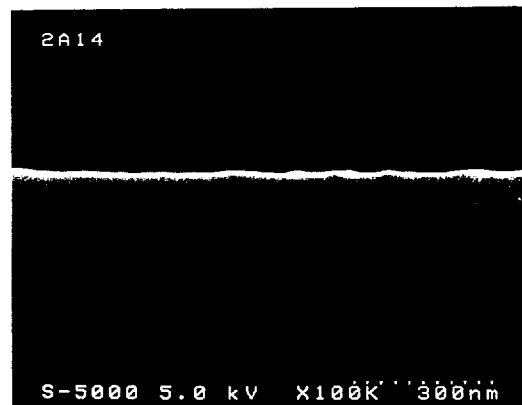
(c) 360 mJ/cm²



(d-1) 380 mJ/cm²



(d-2) 380 mJ/cm²



(d-3) 380 mJ/cm²

Fig.8.20 SEM micrographs of PECVD Si films (40 nm) crystallized at 350 °C by continuous process

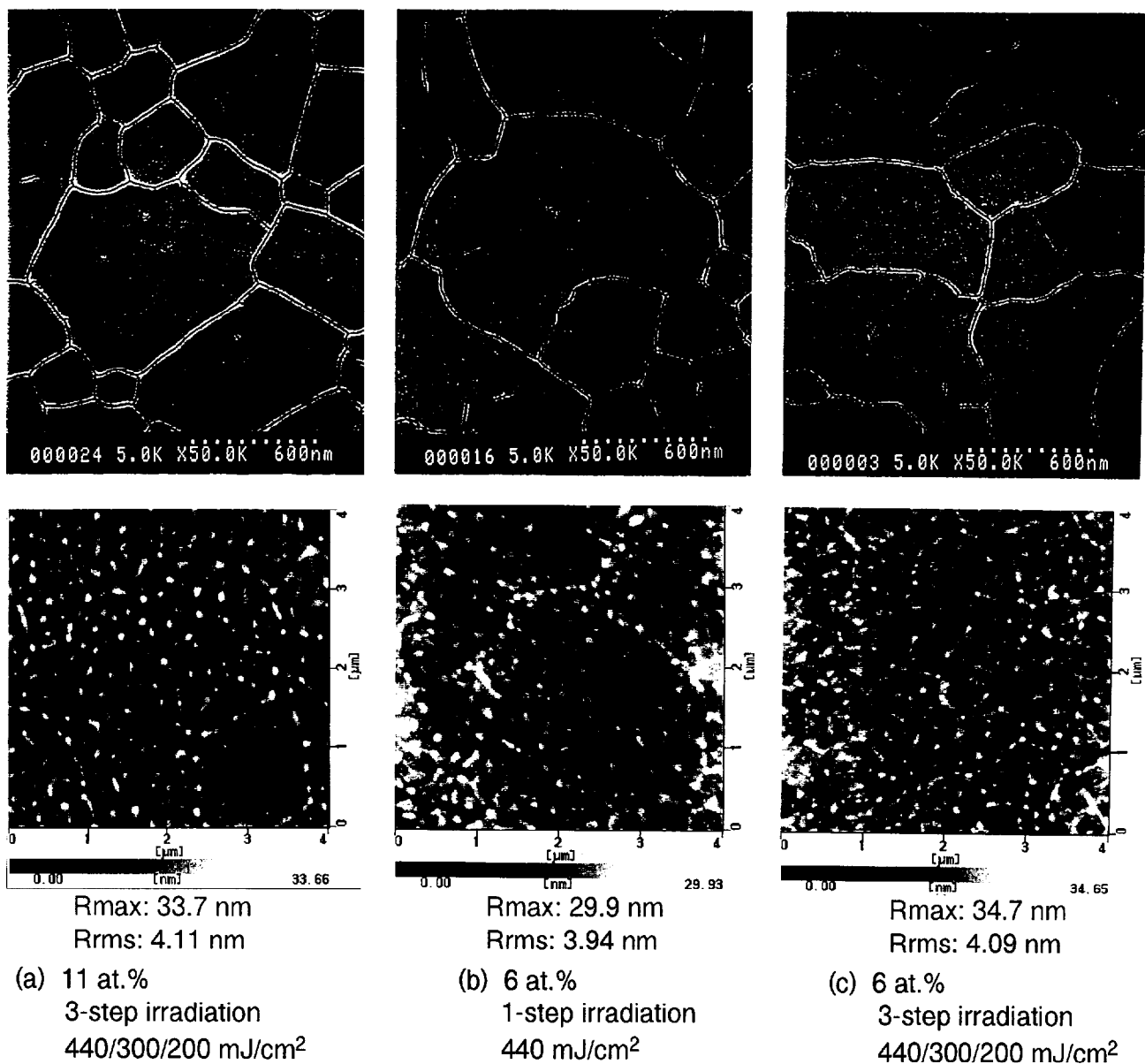


Fig. 8. 21. Surface morphologies of poly-Si films (55nm) prepared by continuous and direct laser crystallizations at 350°C. (a) Conventional film with 11 at.% hydrogen. (b) and (c) Developed films with 6 at.% hydrogen.

three-step irradiations, respectively. Flat and large poly-Si grains were obtained by one-step irradiation without film abrasion comparable to those obtained by the conventional three-step irradiation. Mean value of flatness R_{rms} was small and almost 4 nm and grain size was sufficiently large for all three films with practical thickness of 55 nm. Maximum value of flatness (peak to valley) R_{max} of one-step irradiation was 29.9 nm. It has been reported that flatness was improved for the films with hydrogen content of 2-5 at.% [30]. But, dehydrogenated film (3-4 at.% hydrogen) had large R_{rms} and R_{max} of 5.9 and 47.8 nm, respectively. The results implied that a moderate amount of hydrogen such as 6 at.% contributed to better flatness. The role of hydrogen in this phenomenon must be clarified in the future.

(3) Mechanism of flat and large grains formation

The mechanism of formation of flat and large grains in direct crystallization by continuous process at elevated temperature was considered. In the beginning, degassing from a-Si and SiO_2 by heating in the laser irradiation process was estimated.

Fig.8.22 shows TDS spectra for PECVD films. In (a) of the single SiO_2 layer, absorbed H_2O was emitted at around 200°C and H_2 and H_2O were emitted by the decomposition of -OH radicals at temperatures over 400°C [31], [32]. It was suggested that most of the absorbed H_2O may be removed before deposition of a-Si (340°C) in the discrete process. For the continuously deposited double layer film of a-Si/ SiO_2 (b), H_2 emission from a-Si started at 400°C but emission level of H_2O was low in the total temperature range. Emission of CO_2 was measured as an indicator of contamination of organic gases, but the intensity level was low and there were no significant differences between the two film structures. Thus, it was implied that in the continuously deposited a-Si/ SiO_2 structure, impurity gas emission, at least of H_2O , should be reduced in the laser crystallization process in which SiO_2 contacts to Si melt, though there were H_2 emission from -OH radicals and a-Si.

Fig.8.23 illustrates the models for the laser crystallization process for thick and thin PECVD a-Si films. In thick films as shown in (a), at low energy irradiations (200 and 300 mJ/cm²), only the surface was crystallized [33]. At high energy irradiation, the total area was melted and super lateral growth (SLG) occurred to form ridges [15]. Large mass flow of melt caused the high ridges. During this stage in the conventional process, there was gas emission from the underlayer SiO_2 and a-Si as shown in Fig.8.22 and they may have enhanced the high ridge formation. In thin films under 40 nm as shown in (b), small grains were formed at low energy irradiation. At higher energy irradiation, large grain growth occurred by the rearrangement of small grains and degassing progressed moderately throughout the thin films in the new process. The lateral mass flow of Si melt was also suppressed in thin films. Thus, moderately thin films realized flat and comparably large grains in the continuous process.

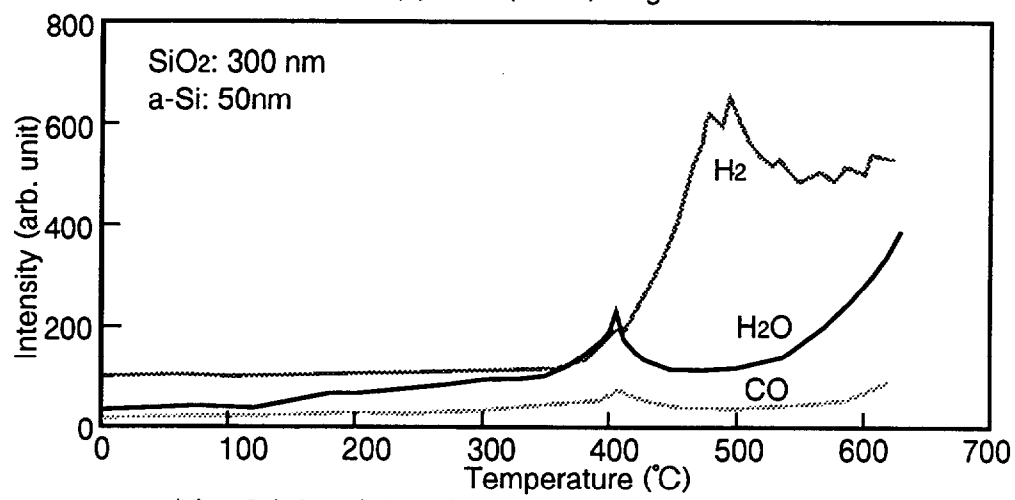
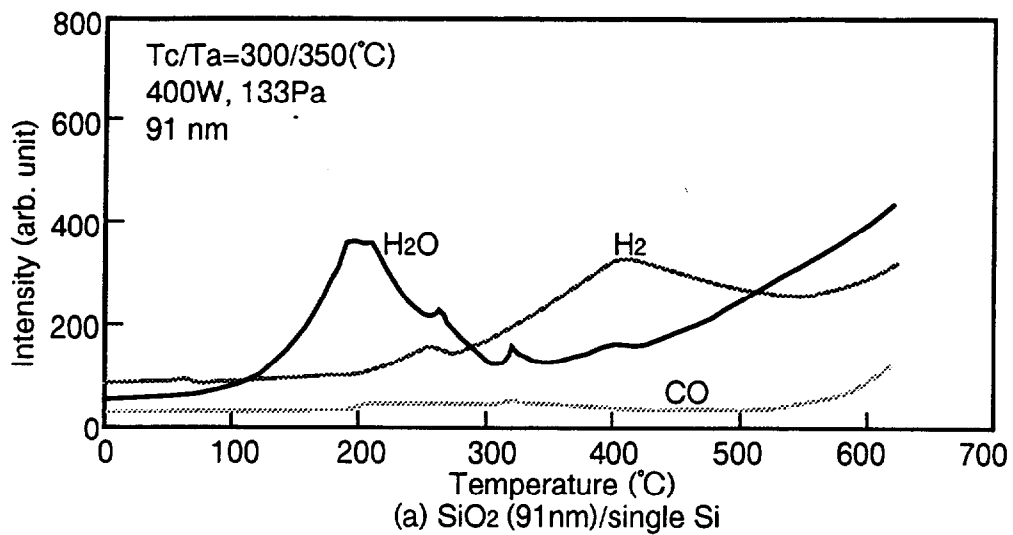


Fig.8.22. TDS spectra of PECVD films.

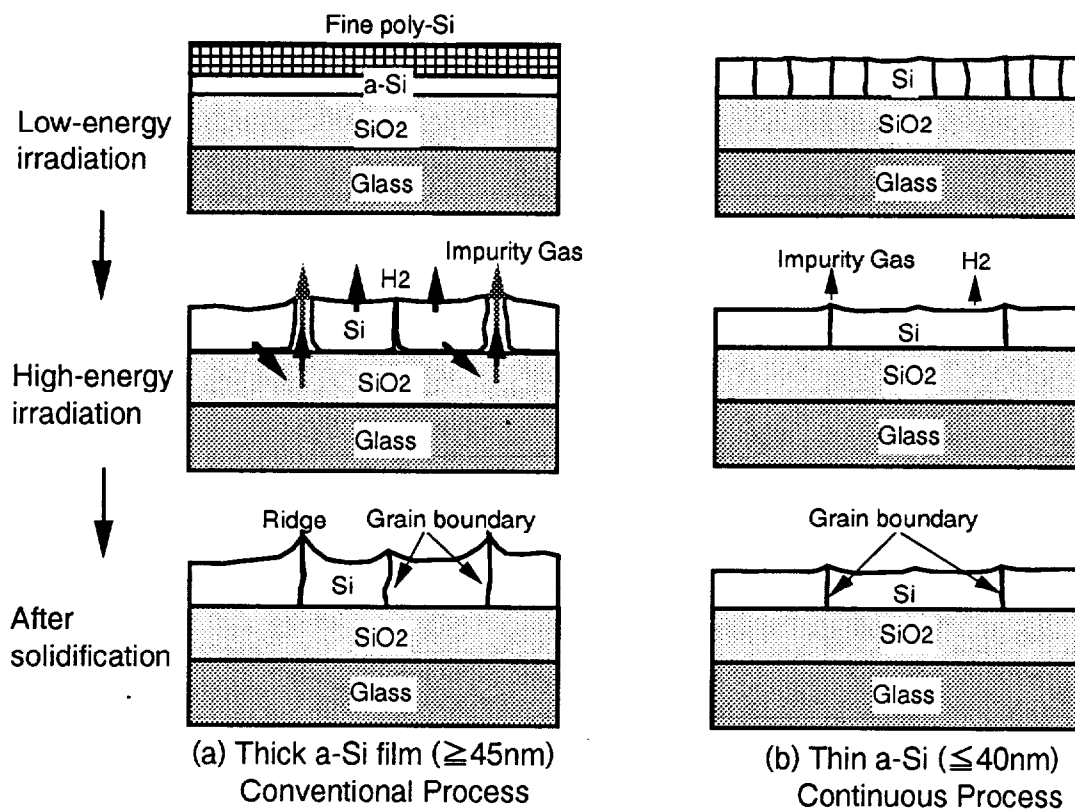


Fig.8.23 Models for the laser crystallization process for thick and thin PECVD a-Si films.

8.4. Continuous process of laser crystallization and gate SiO₂ deposition

8.4.1 Laser crystallization of pre-patterned Si films and continuous deposition of gate SiO₂

The as-crystallized poly-Si film by a laser in vacuum should have a clean surface because natural oxide and absorbed gases are evaporated. Therefore, as shown in Fig. 8.14(b), the laser crystallization of Si films and continuous gate SiO₂ deposition should be useful to realize a clean interface [24]. This process allows the chemical cleaning just before gate SiO₂ deposition to be omitted. But in coplanar TFT, Si films must be patterned into islands.

Fig.8. 24 shows photographs of Si islands before and after laser crystallization. (a) shows Si film islands with 3 μm width after patterning. After laser crystallization, the island dimensions became smaller because edge regions were retreated ((b)). It has been reported that edge regions became thicker than the inner area [26], [27]. But the grain was sufficiently large (d)). Slight retreatment was also observed in laser irradiation at room temperature ((c)). The phenomenon is related to the balance of adhesion to underlayer SiO₂ and surface tension of Si melt. The retreatment will be reduced by using an adhesive underlayer such as SiN.

8.4.2 TFT fabrication

A glass substrate was coated with PECVD SiO₂. Then, LPCVD Si (55 nm) was deposited at 450°C. The Si film was patterned into islands. After chemical cleaning, the substrate was set in the multi-chamber processor. After laser crystallization at 350°C, the substrate was transported to PECVD chamber and gate SiO₂ (100 nm) was deposited continuously. After gate formation, boron and phosphorus were implanted. Activation was carried out at 450°C after SiO₂ deposition for passivation. SiN was deposited as a second passivation film. After metallization, the substrate was annealed at 400°C for hydrogenation.

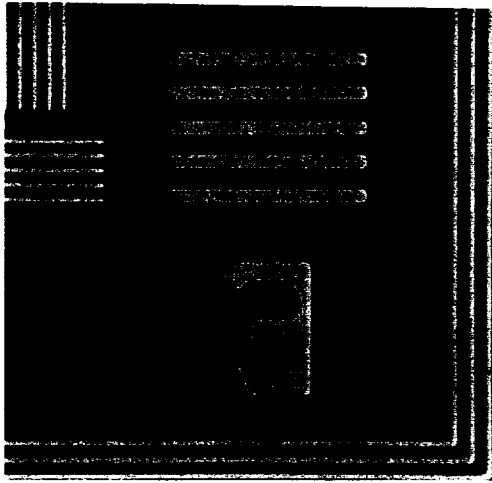
Fig.8.25 shows V_G - I_D characteristics of CMOS TFTs fabricated by continuous process of laser crystallization and gate SiO₂ deposition. High performance which was comparable to conventional TFTs was realized. The technology should contribute to stable production of high-performance poly-Si TFTs.

8.5 Location control of flat and large grains

8.5.1 The presumed mechanism

As mentioned in Fig.8.4, there are many ideas to fix the grain location by controlling heat flow [19]-[22]. In this study, location control was explored using simple patterning of underlayer SiO₂.

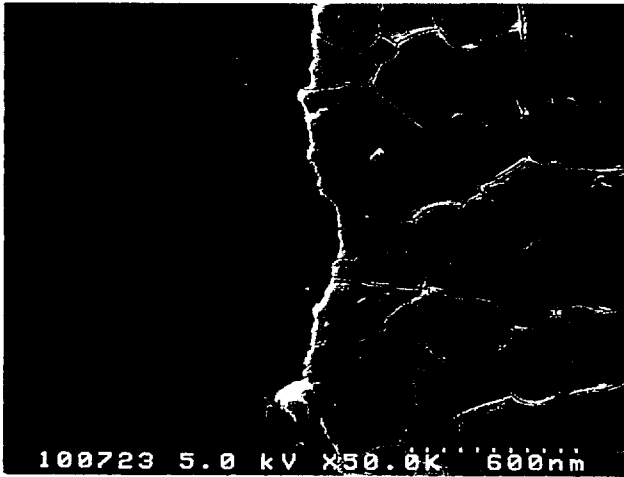
Fig.8.26 illustrates the presumed model of the control of the grains location at step edge of the underlayer SiO₂ in the multi-deposition and



(a) After patterning



(b) After laser crystallization
at 400 mJ/cm², 350°C



(c) After laser crystallization
at 480 mJ/cm², RT



(d) After laser crystallization
at 400 mJ/cm², 350°C

Fig. 8.24. Laser crystallization of pre-patterned LPCVD Si films (Width: 3 μ m).

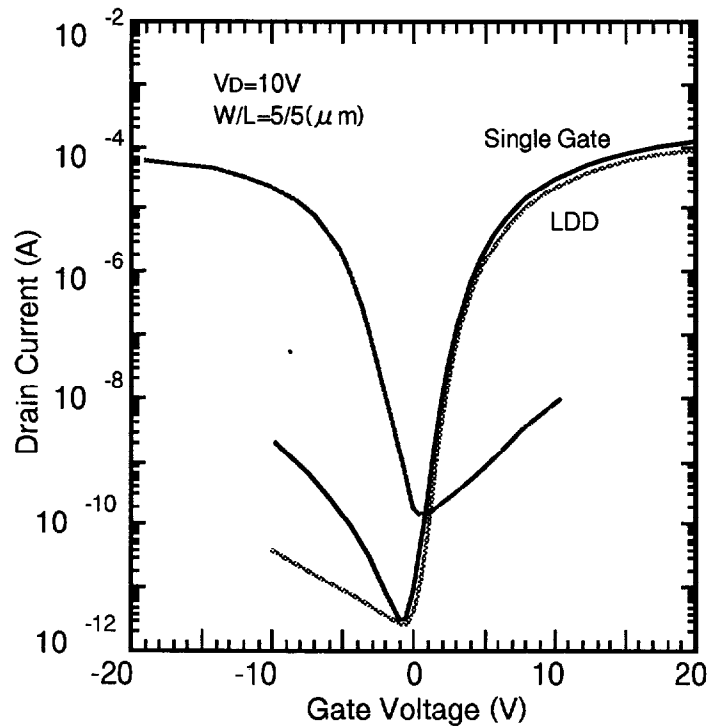


Fig. 8.25. V_G - I_D characteristics of CMOS TFTs fabricated by continuous process of laser crystallization and gate SiO₂ deposition.

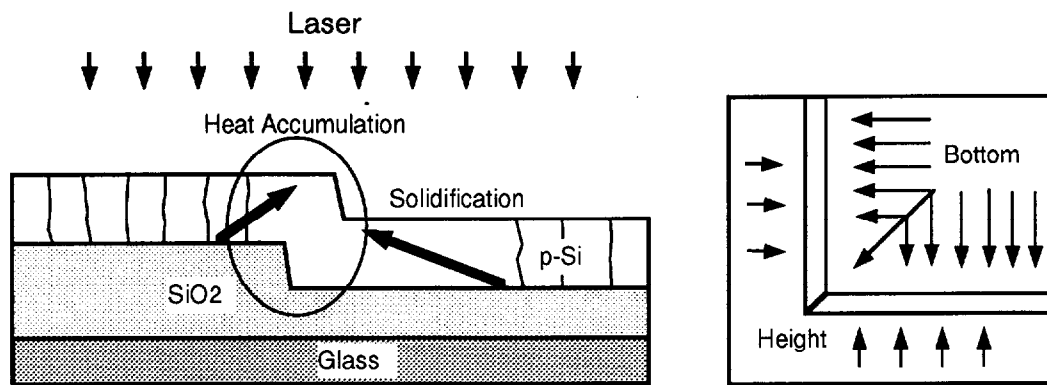
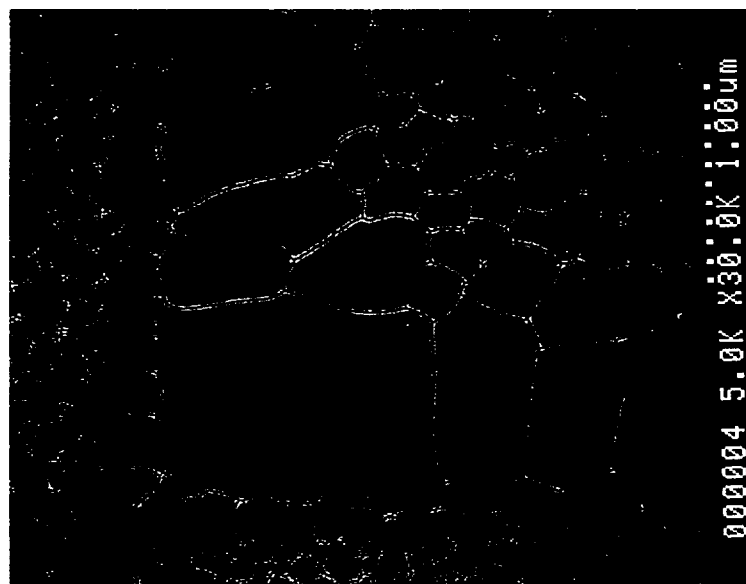
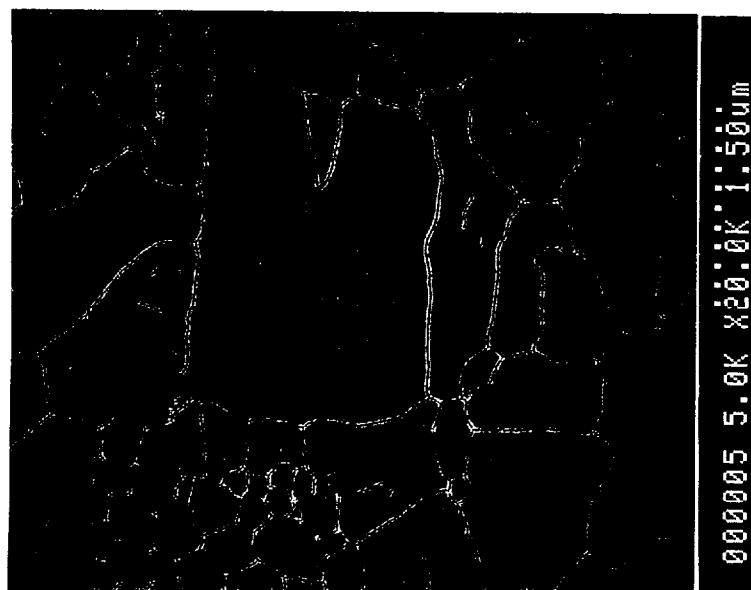


Fig. 8.26. A model of location control of large grain at step edge of underlayer SiO₂.



(a) 480 mJ/cm²



(b) 500mJ/cm²

Fig. 8.27. Examples of location controlled large poly-Si grains at the step of underlayer SiO₂.

multi-step laser irradiation process. The poly-Si at the step edge region was particularly thick in the vertical direction. In the laser irradiation, the step edge region acted as both heat sink and heat accumulator. Generally, during low energy irradiation, the poly-Si of the step region acted as a heat sink because the region was not sufficiently heated and the temperature was low [34]. But during high energy irradiation, the heat accumulates in the thick poly-Si film region, and the step region becomes a terminal for solidification as shown in the inset. Thus, it is expected that fixing of the location and also large grain sizes should be realized by the multi-step laser irradiation method.

8.5.2 An example of location control

Fig.8.27 shows SEM micographs of location control for PECVD Si with total thickness of 60 nm. Depth of step of the underlayer SiO₂ was 40 nm. Two-layer film deposition (11 at.%) and three-step laser irradiation technique were used. Photograph (a) shows the surface of poly-Si crystallized at 480 mJ/cm². A large square grains of 1 × 1 μm² was observed at the corner of the edge. Photograph (b) shows the surface of the poly-Si crystallized at 500 mJ/cm². Square and larger grains of 1.5 × 1.5 μm² were also observed at the corner of the edge. These grains had no grain boundary and they should have high crystal quality as discussed in RF-ZMR SOI (Chapter 4). The size of the grains at the corner will be controlled by varying step height, Si film thickness and laser energy. This technique should be a promising means to realize high performance c-TFTs comparable to SOI TFT for system integration on display panels.

8.6 Conclusions

A novel CMOS ion doping technology with the one-resist mask process was proposed using compensation and inversion of the thinly doped layer. To facilitate the inversion, surface ashing or surface etching by hydrogen ions were applied. The TFT characteristics were comparable to those of the conventional two-mask CMOS TFTs.

A new multi-chamber processor with three PECVD reactors and laser annealer was developed for 150mm × 150mm substrates to realize the novel crystallization process. Under layer SiO₂ and a-Si deposition, and direct laser crystallization could be continuously carried out in the processor. It was shown that the thinning of PECVD a-Si films to 40 nm was effective in reducing surface roughness. In these processes, very flat (Rrms ≤ 4 nm) and large (0.5-1 μm) poly-Si grains were realized. The continuous process of laser crystallization of pre-patterned Si islands and gate SiO₂ deposition was developed to realize a clean interface for high performance poly-Si TFTs. Location control of the large grains (1.5 × 1.5 μm²) was also achieved by using underlayer SiO₂ step.

These processes technologies should contribute to simplify the fabrication process and to advance the performance of CMOS poly-Si TFTs for future system integration on panel.

8.7 References

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Conclusions

In this thesis, key technologies for realizing high-performance low-temperature poly-Si TFTs for small and middle size, high resolution LCDs were studied. First, categories of crystallization processes were SPC and melt-regrowth. For the SPC, low-temperature SPC below 600°C, and middle- and high-temperature SPCs between 900-1000°C were studied. As for the melt and regrowth method, zone-melting recrystallization by RF heating (RF-ZMR) and excimer laser crystallization were explored. Second, large-area ion doping and excimer laser activation were introduced. Third, gate SiO₂ fabrication technologies such as APCVD, PECVD, photo-CVD, and thermal oxidation at 600°C were also investigated. Refining and combining these process technologies led to high-performance CMOS TFTs and fully driver integrated poly-Si TFT-LCDs. The results obtained by this thesis were as follows.

1. For the basic crystallization technology, low-temperature SPC was studied.

(1) In low-temperature SPC, the maximum process temperature was set at 600°C for glass substrates. Amorphous phase LPCVD Si film with maximum spin density showed maximum crystallinity after SPC. Poly-Si film quality and TFT characteristics critically depended on the deposition temperature. This technique is universally applicable for the low-temperature SPC of LPCVD Si films. Optimizing deposition temperature at 550°C and applying plasma hydrogenation, high performance of the n-channel poly-Si TFTs and logic circuits for monolithic integration were realized to drive a 3.3" TFT-LCD for the first time.

(2) Configuration of a two-layer gate oxide was proposed to realize a clean interface of gate oxide-poly-Si. The film structures of APCVD SiO₂/photo-CVD SiO₂, APCVD SiO₂/thermal oxide contributed to improved TFT characteristics. But, it was implied that the trap density in 600 °C SPC poly-Si was dominant in the interface. Therefore it was also suggested that improvement of poly-Si quality in combination with these oxide structures should increase TFT characteristics.

(3) The performances of low-temperature n-channel poly-Si TFTs and E-E type circuits by SPC process were not sufficient for actual driver circuit application because V_{TH} and power consumption were too high. The CMOS configuration was also indispensable for high performance driver circuits.

2. The information from low-temperature SPC experiments was applied to high-temperature poly-TFTs and the middle-temperature TFT process was proposed.

(1) From the observation of contraction of thick poly-Si film at high-temperature, it was suggested that poly-Si film showed grain rearrangement at high-temperature annealing and its rate increased when the poly-Si preparation temperature was low.

(2) To improve performance of conventional high-temperature poly-Si TFTs which were made by one-step SPC, a two-step SPC was introduced. First, applying the optimum SPC conditions developed previously, long time annealing at 600°C was used for moderate crystallization to obtain large grains. Then, high-temperature (1000°C) and a short time SPC was finally applied for recrystallization to reduce defects.

(3) The performance of TFTs by the two-step SPC of LPCVD Si using Si_2H_6 was improved compared with that of TFTs using conventional SiH_4 .

(4) Choosing the merits of low- and high-temperature poly-Si TFTs, the middle-temperature (900°C) process which was compatible to large quartz substrates with two-step SPC, CVD gate oxide, ion doping and laser activation, was proposed.

3. SOI by zone-melting recrystallization was investigated to realize very high quality Si film on transparent substrates and high-performance TFTs for very fine TFT-LCDs using 3 μm LSI processes.

(1) RF heated zone-melting recrystallization was introduced and large area was successfully crystallized by using connected island method. The Si layer had high quality with small-angle grain boundaries and (100) surface.

(2) Direction of sub-grain boundary slightly affected field-effect mobility but did not affect off-current. It was shown that controlled lateral heat flow realized lateral growth of single crystal SOI film which was applicable to fine TFTs.

(3) The n-channel TFTs had a high field-effect mobility of 500-1000 $cm^2/V \cdot s$ comparable to that of the bulk devices and could be operated by 3-5 V drive. To simplify the fabrication process, a p-channel SOI TFT was adopted. The TFT had a field-effect mobility of 150-200 $cm^2/V \cdot s$ and threshold voltage of -2.5 V and on-off ratio of 10^6 though it had high light sensitivity.

(4) Using these p-channel SOI TFTs, very fine TFT-LCD with 220 x 222 pixels and 17.6 x 23.31 mm² (1.15") display area was fabricated for the first time. Logic circuits operation was confirmed using E-E type inverters. The SOI TFT has an ability to realize very fine TFT-LCDs with low voltage driver integration.

4. Large-area and high-speed ion doping by bucket-type (Kaufman-type) ion source without mass-separation was developed. Activation was carried out by excimer laser at low-temperature.

(1) Ion doping using a high ion density bucket type source (150-mm diameter) realized high surface concentration and shallow doping at 500V. Laser activation in vacuum also realized room temperature activation. In 10-s doping using PH₃ or B₂H₆ with He dilution, sheet resistance below 1k Ω /sheet was obtained for source and drain of TFTs.

(2) The TFTs fabricated by ion doping showed almost the same performance as TFTs by conventional ion implantation.

(3) An ion doping apparatus with an ion source of 100 mm x 400 mm was developed to treat 350 mm x 450 mm substrates within 1 minute.

(4) In the long doping process, the deposited thin layer of dopant was formed which acted as a doping source. In high energy laser activation, the concentration profile became almost flat. Rapid diffusion should be promoted by liquid-phase diffusion during laser irradiation.

5. The large-area laser crystallization was explored for 350 mm x 450 mm glass substrates by using an excimer laser and a low-temperature 18.2" poly-Si TFT-LCD was fabricated by the process below 450°C.

(1) As a precursor of poly-Si, LPCVD film was deposited by using Si₂H₆ at 450°C and excimer laser crystallization with a square beam of 7 mm x 7 mm was used. The large areas were almost uniformly crystallized. But the poly-Si film had ridges with a height the same as that of the film thickness.

(2) Applying ion doping and laser activation, n-channel TFTs were fabricated on the substrates. Field-effect mobilities of 60-90 cm²/V-s were obtained. The world's largest 18.2" TFT-LCD with 960x3x517 pixels (quarter size of 40" HDTV) was fabricated by combination with the all-dry etching process and operated successfully.

(3) These process technologies including excimer laser crystallization were promising means to fabricate large area poly-Si TFT-LCDs at low-temperature on large glass substrates.

6. To realize high performance CMOS TFTs for practical driver circuits, key process technologies were refined.

(1) In laser crystallization, a top flat line beam and fine pitch scanning were introduced and uniformity of crystal quality and TFT performance were noticeably improved.

(2) For the application of TFTs to pixels, leakage current of n-channel TFT was reduced by using an off-set gate of 0.5 μm and LDD of 1 μm .

(3) High quality gate insulator SiO_2 was obtained by optimizing PECVD conditions using TEOS- O_2 system.

(4) Ion doping conditions were optimized to use resist mask for CMOS doping. Slightly high (5kV) and short process time (6-10 s) doping was utilized for phosphorus and boron doping.

(5) These developed key technologies realized high-performance CMOS TFTs to operate a shift register at 18 MHz. A 3.8" poly-Si TFT-LCD with fully integrated CMOS driver was operated successfully and full color presentation was achieved.

(6) The developed process technologies are applicable to commercial production of small and middle size high resolution poly-Si TFT LCDs.

7. For the advanced simple TFT processes, one-mask CMOS doping was proposed to simplify the doping process. Continuous processes were proposed to realize flat and large grains, their location control and clean poly-Si interface which should contribute to realize high performance c-TFTs for system on panel.

(1) A novel CMOS ion doping technology with one-mask process is explored using compensation and inversion of a thinly doped layer. Surface ashing or surface etching by He or H ions facilitated the inversion. The TFT characteristics were comparable to those of the conventional two-mask CMOS TFTs.

(2) A new multi-chamber processor with three PECVD reactors and laser annealer was developed. Underlayer SiO_2 and a-Si depositions, and direct laser crystallization could be continuously carried out, applying one- and three-step laser irradiations.

(3) Continuous and one-step direct laser crystallization was achieved by reducing hydrogen content of precursor a-Si film to 6 at.% using high-temperature deposition.

(4) Flat ($R_{\text{rms}} \leq 4 \text{ nm}$) and large (0.5-1 μm) poly-Si grains were obtained by these technique.

(5) Laser crystallization of pre-patterned Si islands and continuous gate SiO_2 deposition were carried out in the processor and high-performance CMOS TFTs were obtained.

(6) Location control of flat and large grains with $1.5 \times 1.5 \mu\text{m}^2$ was realized by using the step of underlayer SiO_2 .

8. From these results, it was concluded that excimer laser crystallization and ion doping have an ability to realize high performance poly-Si TFTs on large glass substrates. The proposed continuous process of CVD and laser crystallization should contribute to realizing simple TFT process and to advance the performance of CMOS poly-Si TFTs for future system on panel.

Acknowledgements

The author is greatly indebted to Professor Masakiyo Matsumura, Tokyo Institute of Technology, for the privilege of being able to write this thesis and for the constant encouragement and support he gave throughout this endeavor.

The author is also very grateful to Professor Hiroshi Ishiwara, Professor Kazihito Furuya, Professor Makoto Konagai, and Professor Shunri Oda, Tokyo Institute of Technology for their valuable discussions and comments for this thesis.

The author would like to thank the Professors of the Technical Engineering Course, Shinshu University, who gave the fundamental scientific knowledge behind this thesis.

During very long periods of this work, the author had a good deal of encouragement and support from many managing staffs. Feelings of gratitude are expressed to Drs. Junzou Kawakami, Hideyo Kodama, Eiichi Maruyama, Yoshito Tsunoda, Katsuki Miyauchi, Takaya Suzuki, Naohiro Monma, Takahiro Nagano and Yutaka Kobayashi, all of Hitachi Research Laboratory (HRL), Hitachi, Ltd.; Messers. Kouichi Maruyama, Masayuki Satou, Zenzou Tajima, Kiyoshige Kinugawa, Kenji Miyata, Hideaki Kawakami, Yoshiharu Nagae, Toshio Miyazawa, Shigeo Shimomura, Kenkichi Suzuki, and Hayao Kouzai, of the Display Group (DP), Hitachi Ltd.; Messers Harushige Kurokawa and Fumio Muramatsu, of Kokusai Electric Co.(KE); Dr. Hiroshi Asano, Dr. Eiji Kaneko, Mr. Kouzou Odawara and Mr. Yoshinobu Komuro, of Giant Electronics Technology Co., (GTC).

The author is also very grateful to colleagues for their good suggestions and encouragement: Mr. Yoshikazu Hosokawa, Dr. Y. A. Ono, Dr. Genshirou Kawachi, Mr. Yoshirou Mikami, Dr. Masatoshi Wakagi, Mr. Youmei Shinagawa, Ms. Etsuko Nishimura, Dr. Minoru Nakamura, Dr. Takashi Aoyama, Mr. Takeshi Satou, Mr. Yoshiaki Toyota, Dr. Masahiko Ando, Mr. Hiroshi Suga, Mr. Masaichi Nagai, Dr. Yousuke Inoue, Mr. Yasuhiro Mochizuki, Mr. Kazuhiro Kuwabara, HRL, Hitachi Ltd.; Dr. Toshihiko Satou, Mr. Hidehiko Ishizu, Mr. Jun-ichi Ohwada, Mr. Yuji Mori, Mr. Kikuo Ono, Mr. Takeshi Tanaka, Mr. Takashi Suzuki, Mr. Katsutoshi Saitou, Mr. Masakazu Saitou, Ms. Hiroko Hayata, DP, Hitachi Ltd.; Dr. Makoto Ookura, Dr. Takeo Shiba, Mr. Yoshinobu Kimura, Central Research Lab., Hitachi Ltd.; Dr. Hiroyuki Kuriyama, Dr. Seiichi Kiyama, GTC; Messers. Takeshige Ishida, Tomohiko Takeda, Masayuki Hara, Michihide Nakamura, Tatsushi Ueda, Takashi Ozaki, KE; Mr. Masanao Yamamoto, Hitachi Device Co.

The author would like to express appreciation to Mr. Saburou Oikawa, Mr. Isao Ikuta, and their team members for sample preparation and machine operation.

A part of the sample preparation was supported by other companies. The author would like to express thanks to ULVAC Japan, Japan Steel Works Ltd., Plasma System Co., Seiko Instruments Inc., Gasonics International Co., Mitsui Ship Building Co.

The author would like to thank Dr. Carol Kikuchi for her advices about the paper preparation in English .

Finally, the author would like to express grateful acknowledgements to Dr. Tetsurou Minemura, Dr. Kenichi Onisawa, HRL, and Mr. Nobutake Konishi, DP, Hitachi Ltd., for their suggestion to write this thesis and their constant encouragements.

List of Publications

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APPENDIX

A1. Application of thick poly-Si film for dielectric isolation

A1.1 Dielectric isolation

In IC fabrication, discrete devices must be isolated electrically to suppress mutual interaction. LSI devices which have shallow junctions, have used pn junction isolation and LOCOS structure. The SOI structure has been considered recently for ULSIs. For high voltage power ICs, dielectric isolation (DI) has been proposed [1]. It realized radiation hardened devices, high voltage isolation, isolation for an alternating current, reduction of parasitic capacitance. But there were serious problems in DI substrate manufacturing concerning the substrate deformation. Fig.1 shows the fabrication process for DI substrates. The first deformation occurred in thick poly-Si film deposition for the support layer [2]. The poly-Si film side was concave. The second deformation was observed in the oxidation process for device fabrication [3]. There, the substrate deformed convexly toward the side of the poly-Si layer. These macroscopic deformations created undesirable effects in the subsequent grinding process for substrate fabrication and in the photolithography process for junction formation. These phenomena originated from the structural change of thick poly-Si films in high temperature heat treatments. The considerations for these phenomena should contribute to optimize high temperature SPC conditions for poly-Si TFTs.

A1.2 Deformation in poly-Si deposition process

Fig.2 shows an example of a polished and Sirtle-etched cross section of a thick (220 μm) poly-Si deposited at 1200°C by $\text{SiHCl}_3\text{-H}_2$ system. Columnar grains were observed. X-ray diffraction studies have shown that a $\langle 110 \rangle$ texture predominated. Fig.3(a) shows a typical interference pattern of the deformation observed with a flatness tester. Poly-Si film was deposited at 1200°C (400 μm). The poly-Si film side was concave as shown schematically in Fig.3(b). The degree of bowing was expressed by the reciprocal of the radius of curvature R calculated from the deformation height h measured by surface roughness measuring instrument.

Fig.4. shows the influence of the poly-Si thickness on bowing. The degree of bowing, $1/R$, increased monotonically with the thickness of the poly-Si layer. Fig.5 plots the influence of the deposition temperature on the bowing. As the deposition temperature decreased, the degree of bowing $1/R$ showed gradual increase. These tendencies could not be explained by mismatching of the thermal expansion coefficients of poly-Si and single Si wafer [4]. The inclusion of trace quantities of oxygen in

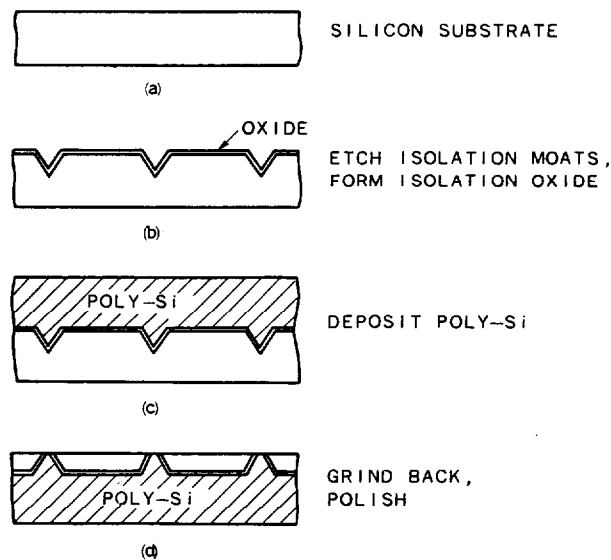


Fig. 1. Fabrication process of DI substrates.

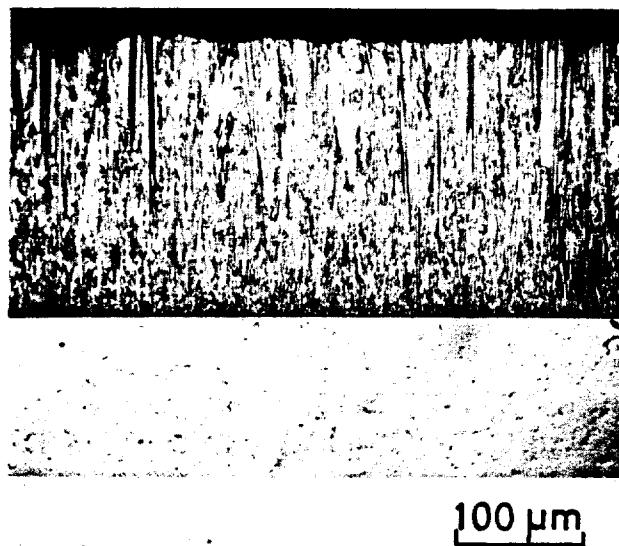


Fig. 2. Cross section of a thick poly-Si layer grown on an oxide-corted Si substrate.

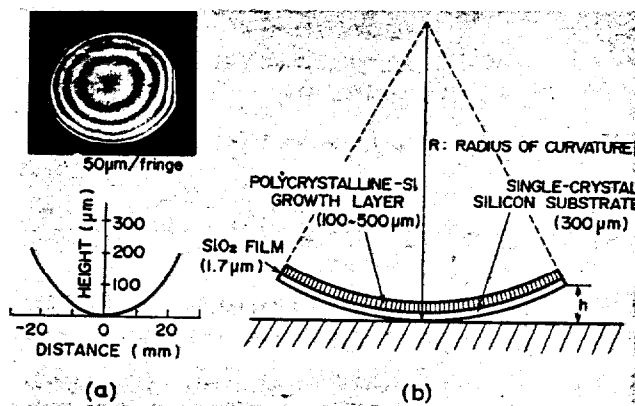


Fig. 3. Bowing of wafer with thick poly-Si layer:
 (a) A typical interference pattern of the deformation;
 (b) Schematic illustration of the bowing.

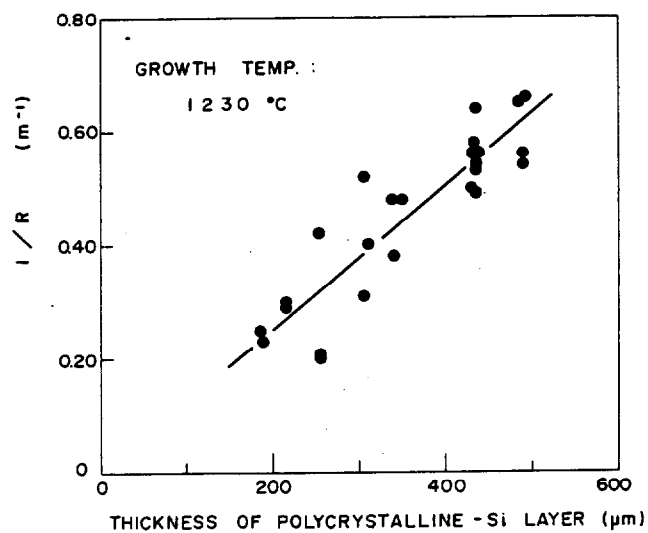


Fig. 4. Influence of thickness of poly-Si layer on wafer curvature.

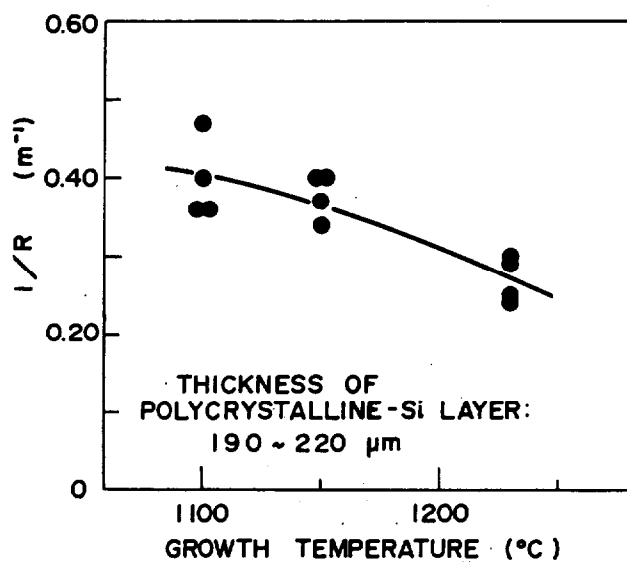


Fig. 5. Influence of growth temperature on wafer curvature.

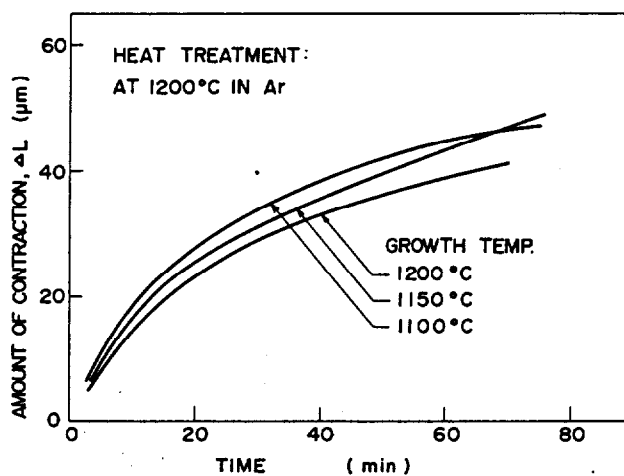


Fig. 6. Influence of growth temperature of poly-Si layer on contraction.

poly-Si was thought to be another possible reason [5]. When the thickness of the single crystal substrate was reduced by successive etching, the bowing increased monotonically and reached the maximum after single silicon and SiO₂ were etched out. These results indicated that the bowing in poly-Si deposition seemed to be caused by some internal stress arising from an intrinsic property of the poly-Si layer itself.

Fig.6 shows the influence of the deposition temperature of poly-Si on contraction when heat-treated at 1200°C [3]. The contraction had a tendency to increase with decreasing deposition temperature. This may imply that internal film stress was reduced by increasing deposition temperature. The contraction of poly-Si layer may be induced by a mechanism similar to sintering [6] as described in chapter 3.2.

A1.3 Deformation in oxidation process

Fig.7 shows the variation in degree of deformation during various wafer processes. The poly-Si was deposited at 1230°C. The thermal oxidation was performed at 1200°C in a wet oxygen atmosphere. Boron diffusion was carried out at 1200°C. The wafers underwent curved deformations in the plus direction after the poly-Si deposition and had a tendency to deform in the minus direction during the thermal oxidation process. The DI substrates with thinner poly-Si support layer showed remarkable change.

Fig.8 shows bowing recovery of the DI substrates deformed by thermal oxidation as measured by successive etching of the surface of the poly-Si layer side. By etching off the oxidized poly-Si surface of about 30-40 μm, bowing in the minus direction was almost restored to the initial bowing in the plus direction that had been observed before thermal oxidation. The etched thickness necessary to return to the initial bowing was roughly consistent with the depth of high oxygen concentration (40 μm) measured by SIMS.

A1.4 Control of deformation using multi-layer poly-Si structure

Two different direction deformations of DI substrates were controlled by using poly-Si-SiO₂ multi-layer structures.

Fig. 9 shows the cross-sectional examples of the multi-layer poly-Si structures. The poly-Si and SiO₂ layers were deposited alternatively by conventional vertical epitaxial reactor using SiHCl₃-H₂ and SiHCl₃-CO₂-H₂ systems, respectively. Deposition rates were about 6 and 0.3 μm, respectively.

Fig.10 shows a relation between the number of poly-Si layers in a multi-layer structure and the magnitude of bowing of the substrates for two different total thicknesses of support layer. The degree of bowing decreased with increasing numbers of poly-Si layers. Above a certain number of layers, the direction of bowing was reversed. Fig. 11 shows

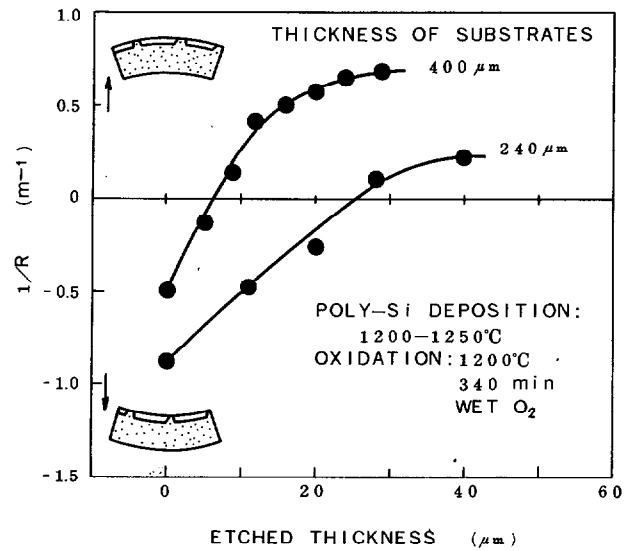


Fig. 7. Effect of process steps on wafer deformations.

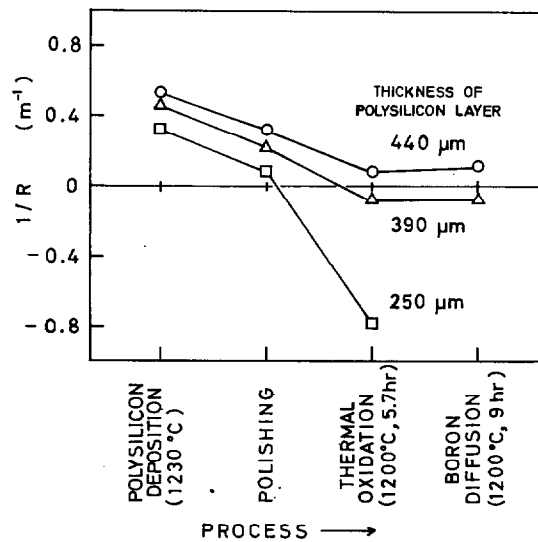
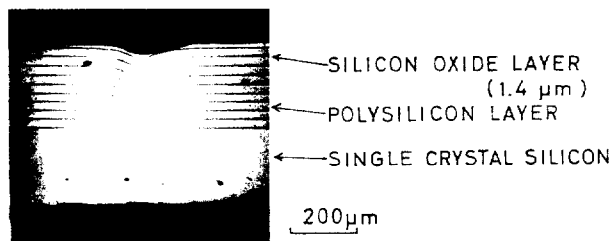
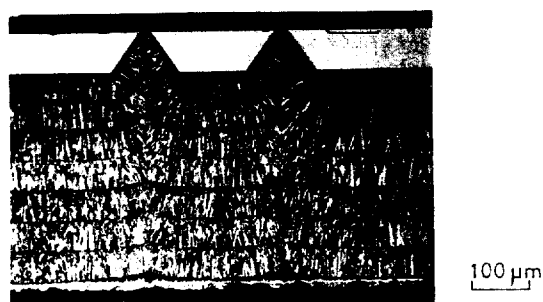


Fig. 8. Bowing recovery of DI substrates deformed by thermal oxidation as measured by successive etching of the surface of the poly-Si layer side.



(a) AFTER POLYSILICON DEPOSITION



(b) AFTER POLISHING AND SIRTIL-ETCHING

Fig. 9. Cross-sectional views of the multi-layer poly-Si support structure.

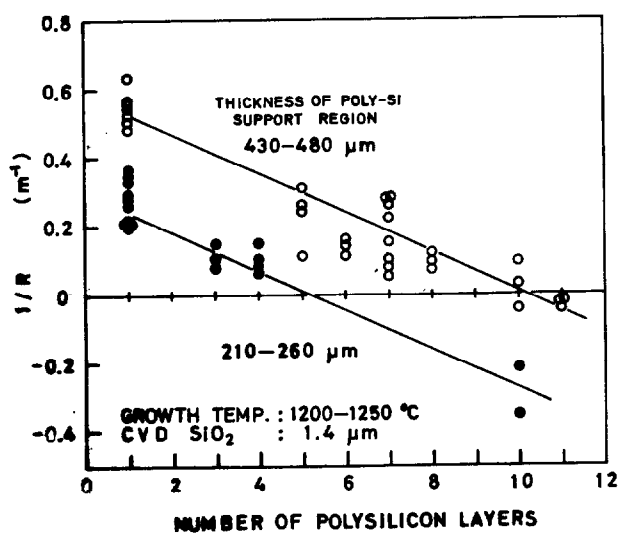


Fig. 10. Relation between the number of poly-Si layers in a multi-layer poly-Si support and the degree of bowing of wafers.

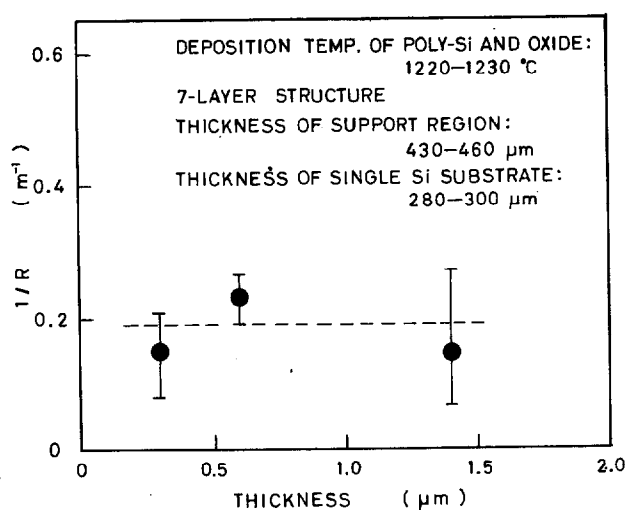


Fig. 11. Effect of the thickness of the Si oxide films between the poly-Si layers on the degree of bowing of wafers with a multi-layer poly-Si structure.

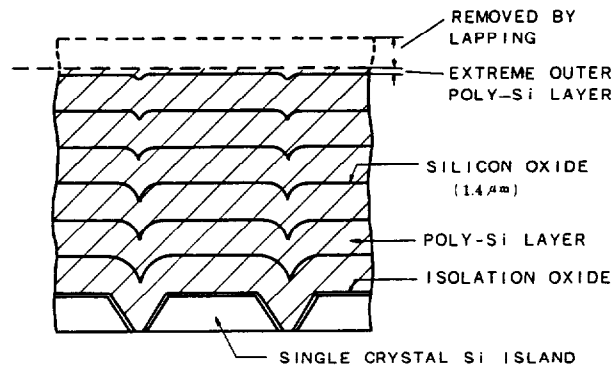


Fig. 12. Schematic cross-sectional view of the multi-layer poly-Si support structure in which the thickness of the extreme outer poly-Si layer was thinned.

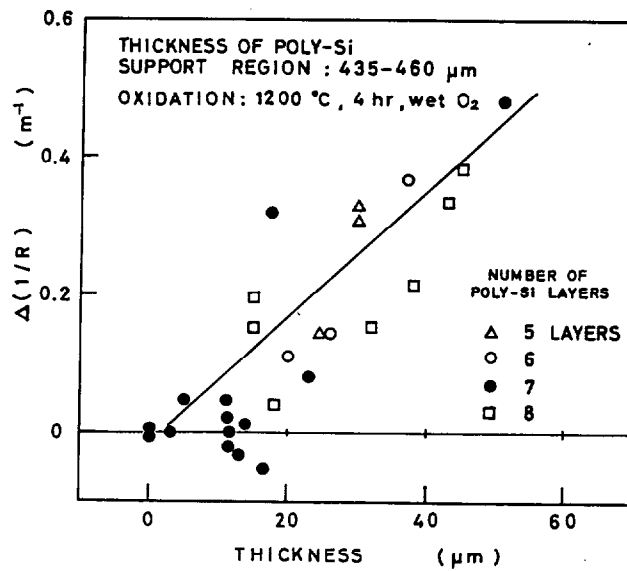


Fig. 13. Relation between the ultimate thickness of the extreme outer poly-Si layer after polishing and the change in the degree of bowing, $\Delta(1/R)$, due to thermal oxidation.

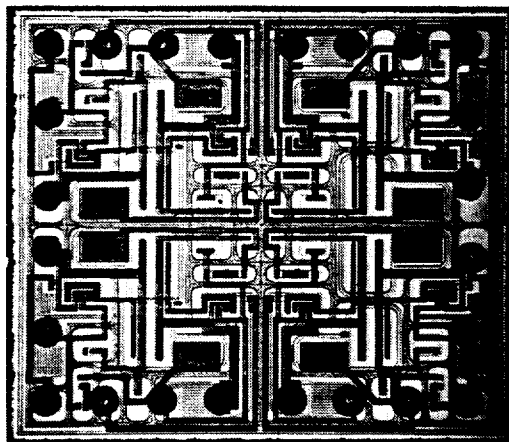


Fig. 14. Fabricated high-voltage IC on DI substrate.

the effect of the thickness of the SiO₂ film on the degree of bowing of the multi-layer DI substrates. The value was hardly affected by the thickness of SiO₂ films in the range from 0.3 to 1.4 μm . Therefore, SiO₂ layers with low thermal expansion coefficient did not contribute to suppress deformation. The penetration or diffusion of oxygen into the poly-Si layer should take place in the case of high-temperature CVD of SiO₂ as thermal oxidation at high temperature. It was proposed that during the formation of the multi-layer poly-Si support structure, contraction stress, caused by poly-Si deposition, and expansion stress, caused by SiO₂ deposition, are occurring alternately to compensate each other to form a wafer with little deformation.

One possible technique to suppress deformation of DI substrate in the oxidation process is to prevent deep oxygen diffusion into the poly-Si layer. Fig.12 shows a schematic cross-sectional view of such a DI wafer used for the experiments. Fig.13 plots the relation between the ultimate thickness of the extreme outer poly-Si layer after polishing and the change in the magnitude of bowing toward the minus direction, $\Delta(1/R)$, due to thermal oxidation. Although scatter in the measured values was seen, it was evident that the change in magnitude of bowing decreased as the thickness of the extreme outer poly-Si layer was decreased. The DI substrates in which the whole extreme outer poly-Si layer was removed by etching and SiO₂ layer was exposed showed little change in bowing. It was found that the extreme outer SiO₂ layer acted as the preventive film for oxygen diffusion into the poly-Si layer.

It was concluded that the deformations of DI substrates due to inner film stress of poly-Si in deposition and thermal oxidation were controlled by the multi-layer poly-Si support structure. Fig. 14 shows an example photograph of high voltage crosspoint switches with capability of 250 V, 200 mA fabricated on DI substrates [6].

A1.5 References

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A2. SIPOS Passivation

A2.1 SIPOS technology

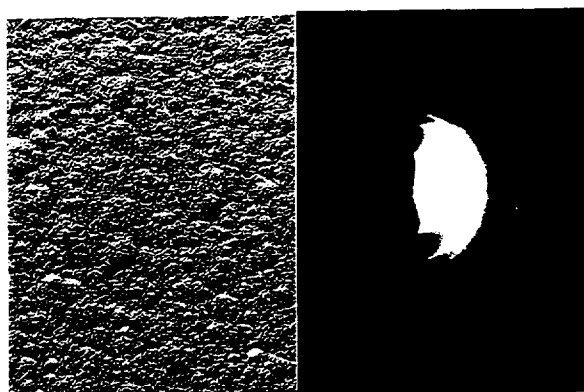
The passivation of semiconductor junction is an important technology to maintain reliability of high-voltage devices. Mesa structure, field-limiting ring, field-plate have been combined passivation materials such as silicone gum, poly-imide resin, and low-temperature melting point glass. In planar devices, insulation films like PSG have been employed conventionally, since they keep leakage current low. But, when the insulation film is directly placed on the semiconductor junctions, a field effect (MOS action) appears. For example, contamination of ion particles on the passivation film induces opposite polar charges on the semiconductor surface causing it to become unstable. In considering the demand for device reliability, use of insulation film is not the best passivation technique, especially for very high-voltage devices.

Semi-insulating polycrystalline silicon (SIPOS) was first applied to passivation for very high-voltage (1-10 kV) coplanar transistors [1]-[3]. In this case, ions induced by the field effect were trapped in the SIPOS films and the semiconductor surface was always kept stable and high reliability was achieved. SIPOS has a wide-band gap than crystal silicon. The second application of SIPOS was as emitter for hetero-junction bipolar transistor for high h_{FE} [4]. The third application was in low leakage current poly-Si TFTs [5].

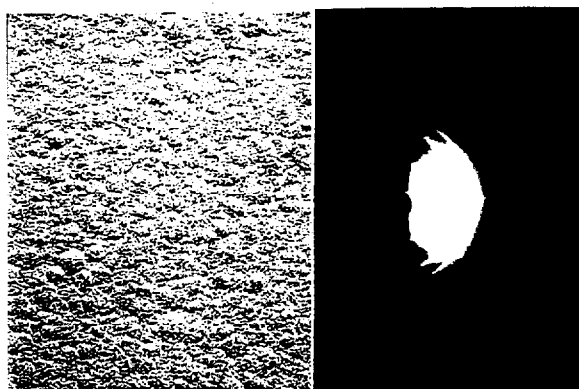
In passivation applications, SIPOS films were generally fabricated by CVD and the junction surface was liable to be contaminated by impurities in the reaction gases. Therefore, leakage current (mainly surface generation current) was large compared with that obtained for insulation film (PSG) passivated devices. Another method was then proposed in which SIPOS was placed on SiO_2 film [6]. The structure realized very high junction breakdown voltage by using field-plate effect. In this study, passivation of a high-voltage planar transistor with various film structures, such as SiO_2 -PSG- SiO_2 , SiO_2 -SIPOS, and SiO_2 -SIPOS- SiO_2 [7], was studied.

A2.2 Preparation of SIPOS films

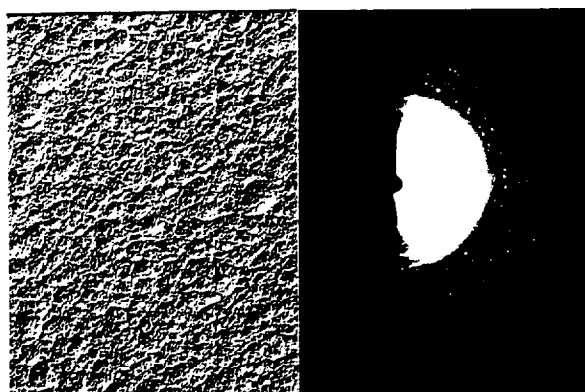
The resistivity of SIPOS is 10^{10} - $10^{15} \Omega\cdot\text{cm}$ which was achieved by doping oxygen or nitrogen into poly-Si in CVD process. In this study, O-SIPOS (oxygen doped) was fabricated by APCVD using a vertical type epitaxial reactor and SiH_4 - N_2O - N_2 system at 650°C . N-SIPOS (Nitrogen doped) was deposited by LPCVD horizontal reactor and SiH_2Cl_2 - NH_3 - N_2 system at 770°C . Fig.1 shows SEM micrographs (replica method) and EBD patterns of O-SIPOS films deposited at various gas ratios. As-grown films showed rings and small dots in EBD patterns indicating that these films had very fine polycrystalline and randomly oriented crystallites. After sintering at 1000°C for 30 min in N_2 , EBD patterns were almost a



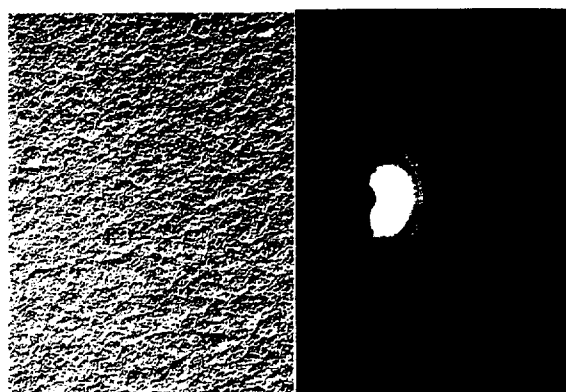
(a) $\gamma = 0$



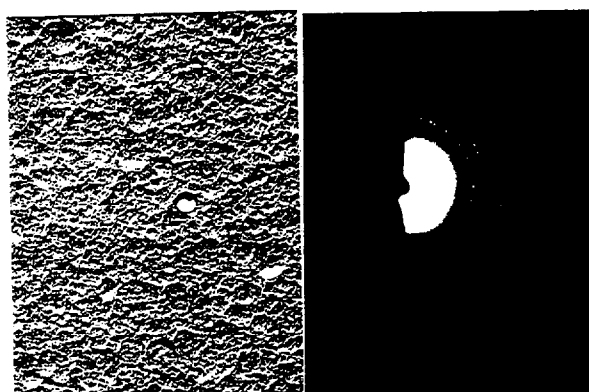
(e) $\gamma = 0$



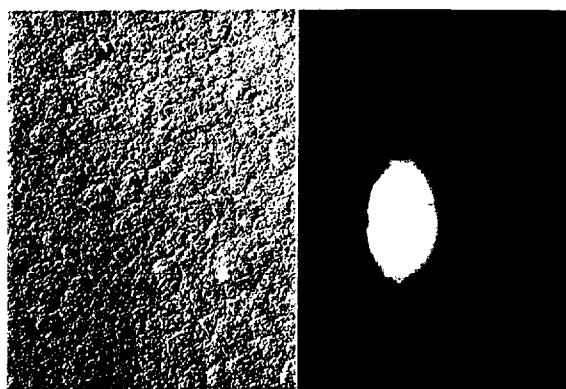
(b) $\gamma = 0.2$



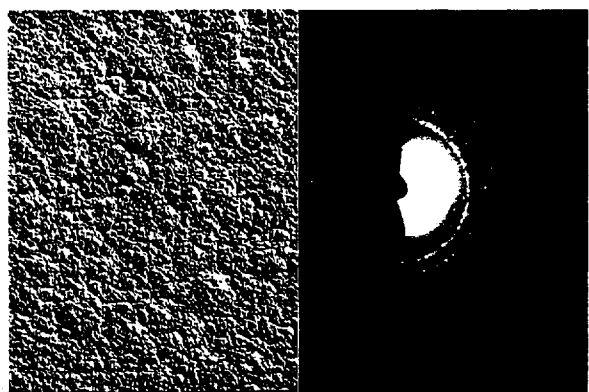
(f) $\gamma = 0.2$



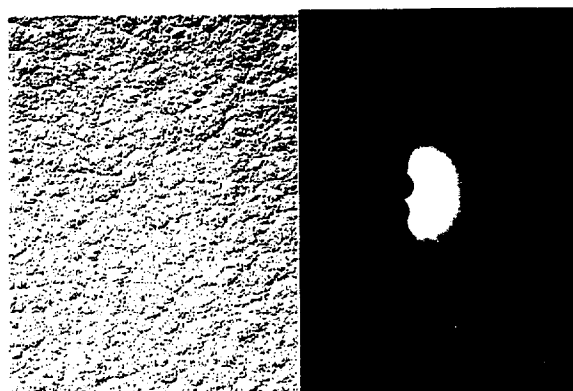
(c) $\gamma = 2.0$



(g) $\gamma = 2.0$



(d) $\gamma = 5$



(h) $\gamma = 5$

as-grown

after sintering

Fig. 1. Surface morphologies and EBD patterns of O-SIPOS films. (X 20000)

halo pattern showing that these films became amorphous. Fig.2. shows SEM micrographs (replica method) and EBD patterns of N-SIPOS films deposited at various gas ratios. Without nitrogen, the film had grains in an amorphous matrix. EBD pattern showed that the film was polycrystalline. When nitrogen was doped, the film became amorphous. Figs. 3 and 4 plots dependence of resistivity on gas ratios for O- and N-SIPOS, respectively. The resistivity increased monotonically by increasing dopant gas ratio. Wide range resistivities were obtained by controlling gas ratio.

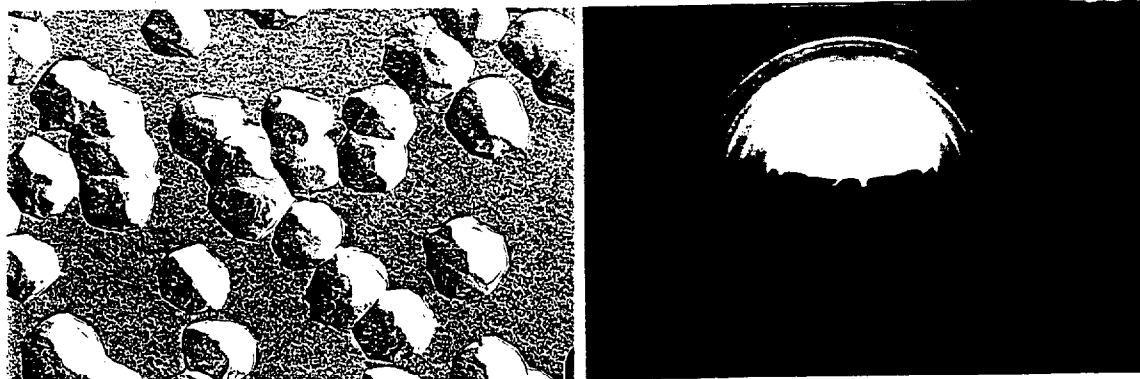
A2.3 Application for high-voltage planar transistors

Fig.5 shows a schematic cross section of a transistor passivated with various films. The film structures were designated as PSG, under SIPOS and over SIPOS. The PSG type consisted of thermal SiO_2 (520 nm) and CVD-PSG(350 nm, phosphorous 6 at.%) and CVD SiO_2 (250 nm). The under SIPOS type was passivated by O-SIPOS (600 nm), N-SIPOS (51 at.%, 200 nm) and CVD SiO_2 (600 nm) which protects the SIPOS layer. The over SIPOS type was passivated by thermal SiO_2 , O-SIPOS (27 at.%, 600 nm) and CVD- SiO_2 (600 nm). Thermal SiO_2 thicknesses were 14nm (800°C), 40 nm (1000°C), 103nm (1000°C), and 520 nm (1100°C).

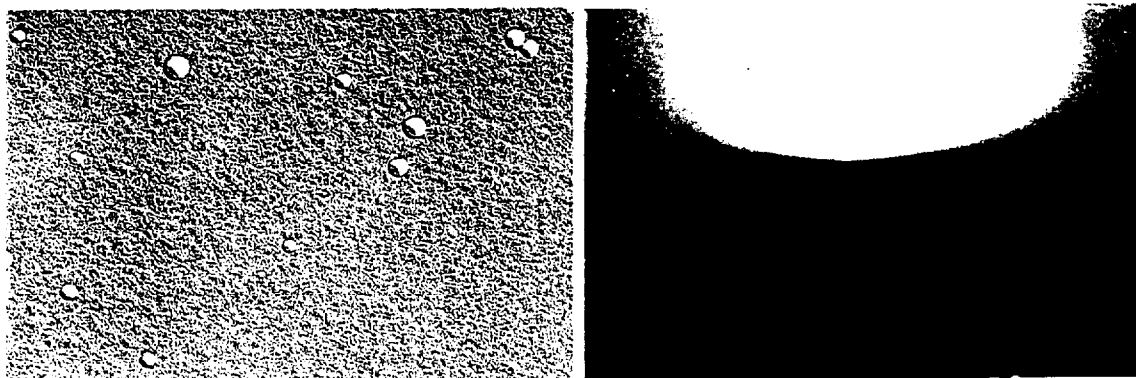
The starting Si wafer was CZ-N, (111), 70 Ω -cm, 390 μm thick. The transistors were fabricated by phosphorous and boron diffusion. Base-emitter junction depth, base-collector junction depth, and collector n^+ depth were 40, 70, 30 μm , respectively. Fig.6 shows a plane view of device chip with 3.5 mm square.

Fig.7 shows the BV_{CBO} dependence on W_C . In the under SIPOS and PSG types, BV_{CBO} did not depend on W_C and it was 100V higher for the former. This indicated that the depletion layer expansion in the PSG type was limited by plus charges in the passivation film. In the under layer SIPOS type, no field-plate effect was observed. The BV_{CBO} was determined by base junction shape. In the over SIPOS type, BV_{CBO} depended on W_C and a high BV_{CBO} was obtained when W_C was larger than 210 μm . This high value was due to the field-plate effect. It is important to note that BV_{CBO} was independent of thermal SiO_2 thickness though the value critically depended on SiO_2 thickness in the metal-field plate structure [8].

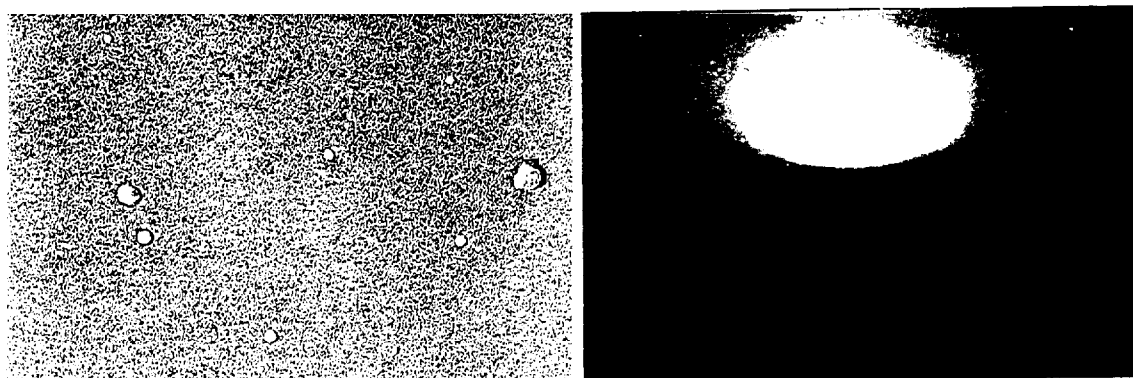
Fig. 8 show the reverse-voltage-current characteristics of the base-collector junction. Conduction current in the O-SIPOS film which had the same dimensions (resistor) was also plotted. Leakage current of the over SIPOS type was lower than the under SIPOS (surface generation current was reduced), but higher than the PSG type. In the over SIPOS type, leakage current increased when thermal SiO_2 thickness decreased. By gettering thermal SiO_2 as PSG type using SiO_2 -PSG-SIPOS- SiO_2 structure, the leakage current was reduced to 1×10^{-10} A at $V_{\text{CB}}=10\text{V}$. The leakage current of the over SIPOS type increased stepwise at a certain applied voltage. For the device with thermal SiO_2 of 520 nm, this critical



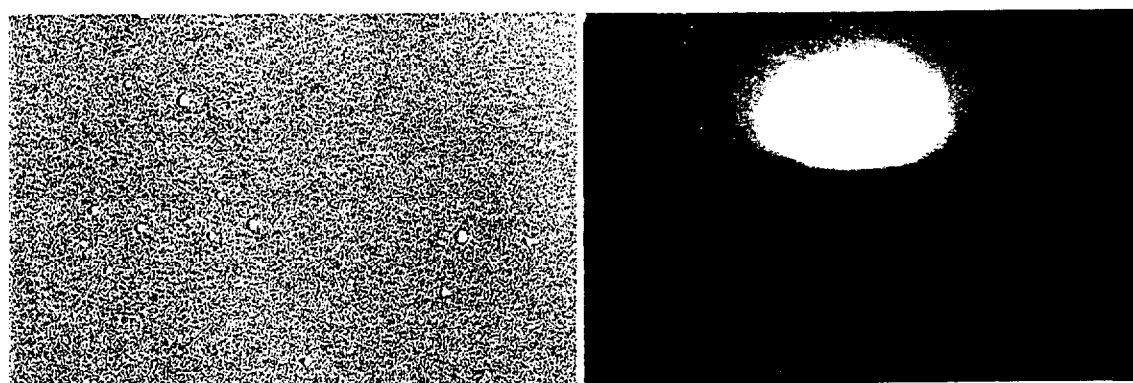
(A) $R_N=0$ (0.0 at%) 200 nm



(B) $R_N=0.02$ (34 at%), 210 nm



(C) $R_N=0.1$ (49 at%), 250 nm



(D) $R_N=0.5$ (55 at%), 270 nm

(X20000)

Fig. 2. Surface morphologies and EBD patterns of N-SIPOS films.

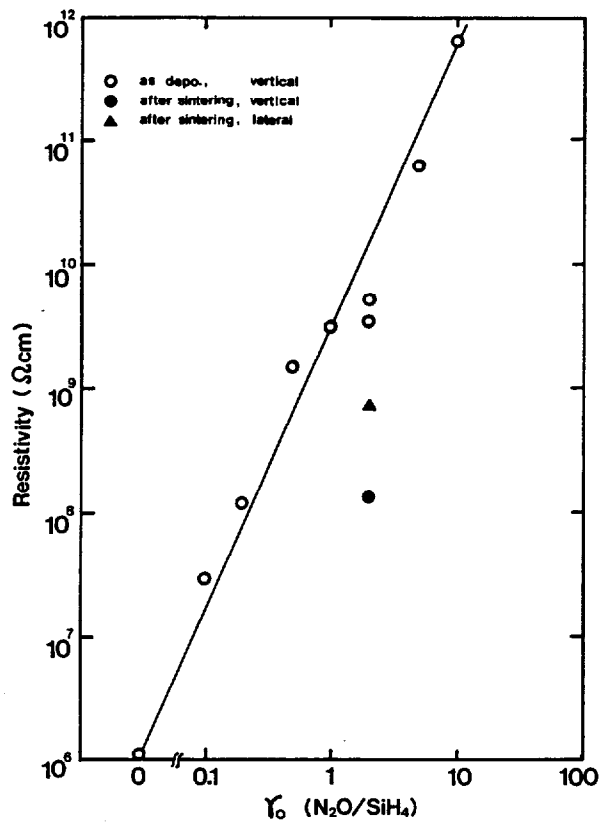


Fig. 3. Dependence of sheet resistance on gas ratio in O-SIPOS.

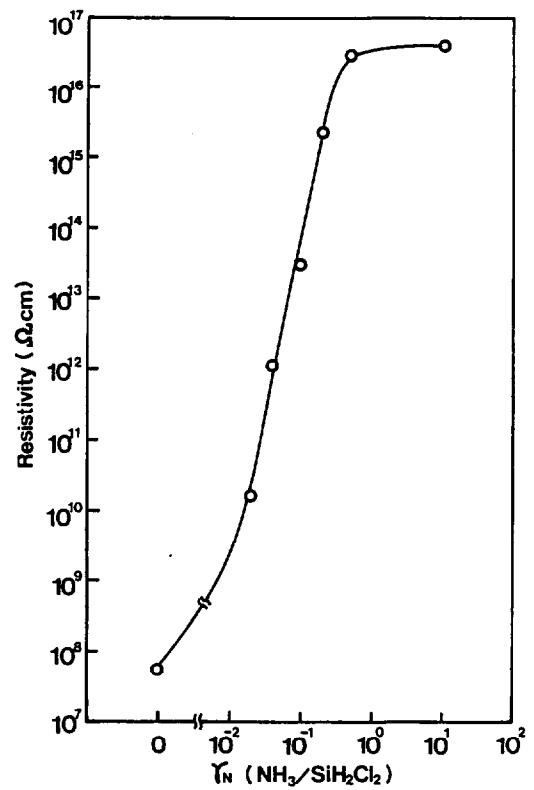


Fig. 4. Dependence of sheet resistance on gas ratio in N-SIPOS.

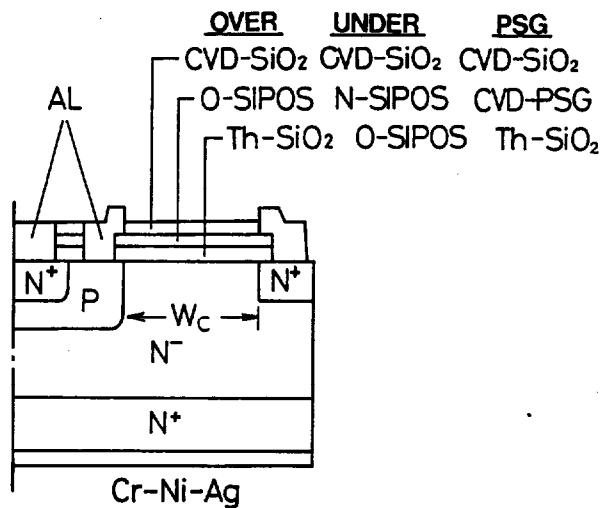
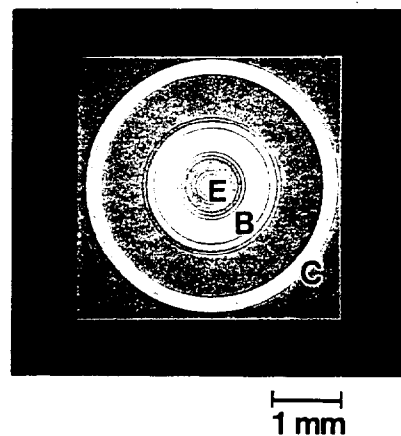


Fig. 5. Cross section of transistor.



E: EMITTER
B: BASE
C: COLLECTOR

Fig. 6. Planar structure of high-voltage transistor.

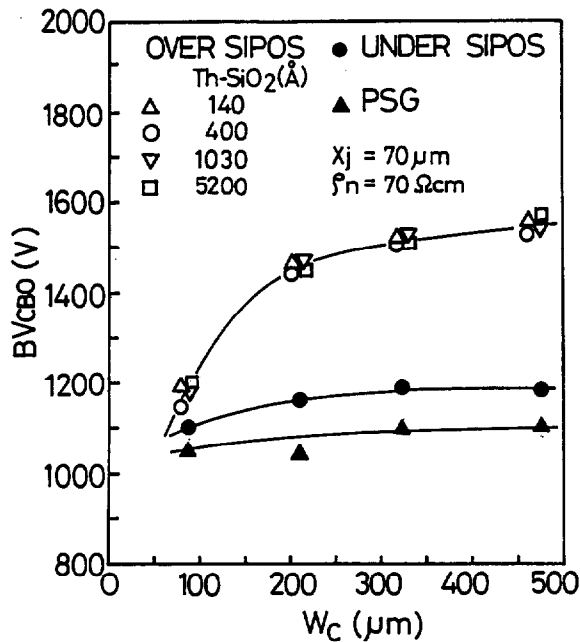


Fig. 7. BVcbo dependence on W_c .

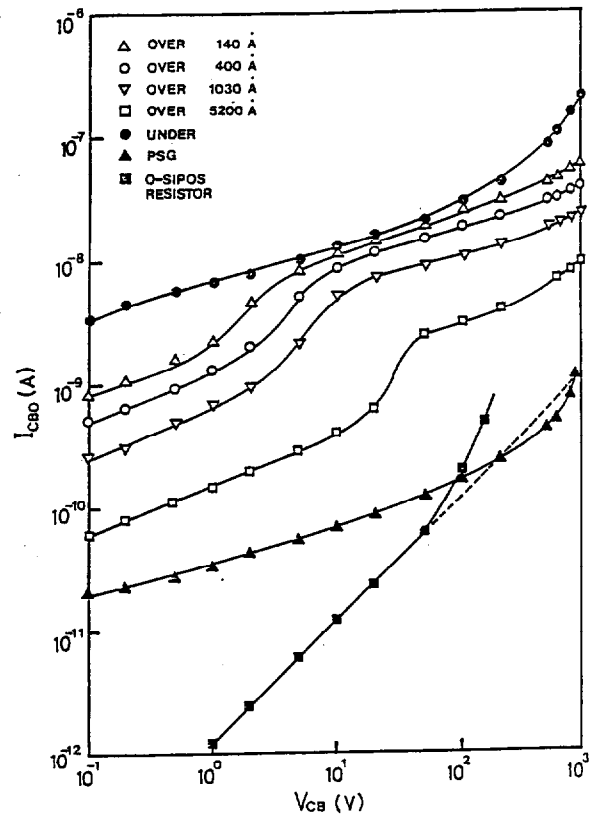


Fig. 8. Reverse voltage-current characteristics of a base-collector junction.

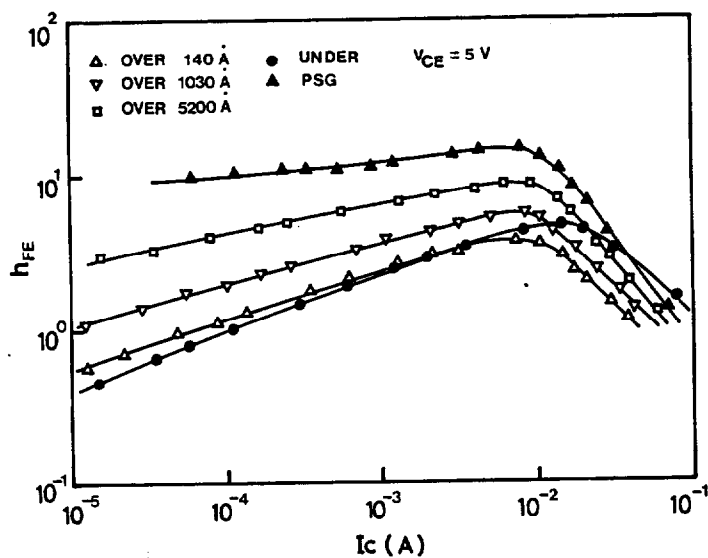


Fig. 9. Collector current- h_{FE} characteristics of a planar transistor.

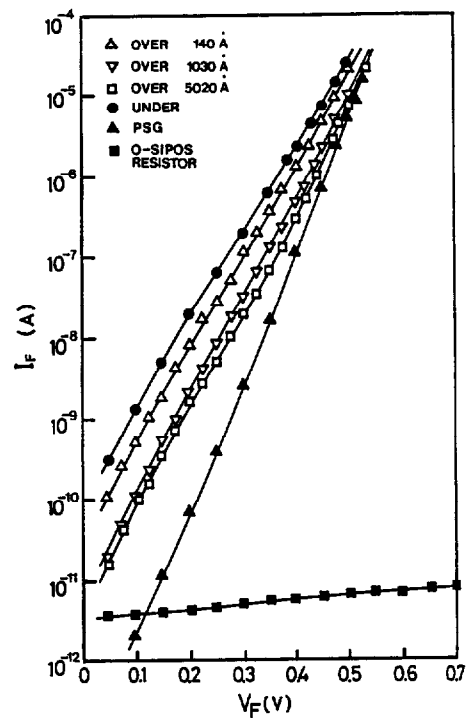


Fig. 10. Forward characteristics of a base-emitter junction.

voltage was about 20 V. This value was almost equal to the V_{FB} of the thermal SiO_2 (18 V). The result indicated that the field-plate effect occurred and the depletion layer began to spread over n^- collector surface when the applied voltage reached 20 V. By the addition of surface generation current in this depletion layer, leakage current increased stepwise at 20 V. Thus field-plate effect occurred in all over SIPOS type devices, in support of the results in Fig. 7.

Fig. 9 shows collector current- h_{FE} characteristics of devices. In the low collector current region, h_{FE} was in the order of PSG type > over SIPOS type > under SIPOS type. To understand I_C - h_{FE} characteristics, forward and reverse conduction currents (I_F and I_R) of the base-emitter junction were measured. Fig. 10 shows forward characteristics of base-emitter junction. These results showed that I_F or I_R was in the order of under SIPOS type > over SIPOS type > PSG type and that the main component of I_F or I_R was surface generation current not conduction current in SIPOS. The over SIPOS type is a useful high-voltage low-loss planar structure.

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A3 Preliminary study of SPC technology

A3.1 TFT fabrication process

The first poly-Si TFT was fabricated on glass by using MBD Si [1]. To see the key technologies to improve TFT performance, preparation methods of active layer poly-Si and gate insulator were reviewed.

Fig. 1 (a) and (b) show the TFT fabrication process and cross-sectional structure. Quartz substrates and 3 μm LSI process were used. As Si film preparation, MBD [1], PECVD, and LPCVD at 580 °C or 640 °C were examined. MBD should have a limit to treat large substrates but PECVD and LPCVD have a possibility to be applied to large ones. Gate SiO_2 was fabricated by APCVD, PECVD and high temperature thermal oxidation.

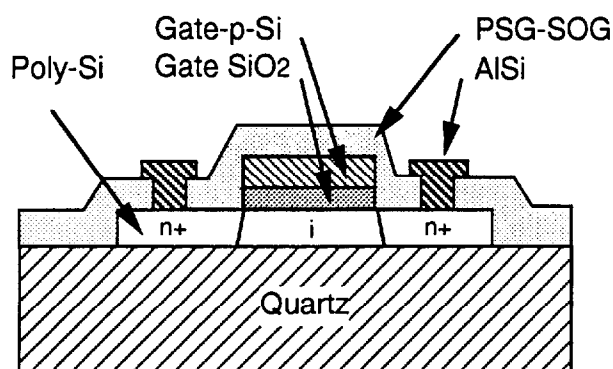
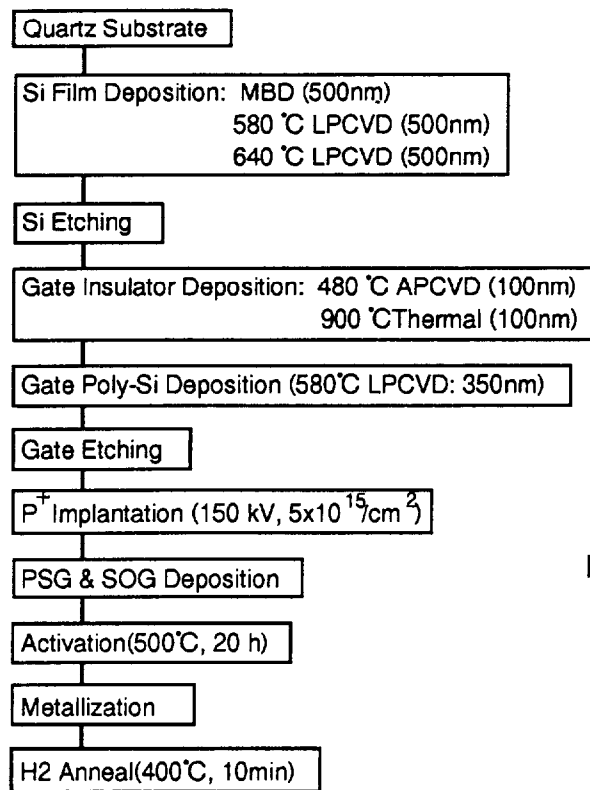
A3.2 TFT characteristics

In these experiments, none of the TFTs had sufficient performances. But, the TFT fabricated by MBD Si and APCVD SiO_2 showed the best. Fig. 1(c) plots the V_G - I_D characteristics of typical TFTs. They had high V_{TH} and low mobility. Fig. 1(d) shows the relation of mobility and threshold voltage. The TFTs with LPCVD Si deposited at high temperature (640 °C) showed low threshold voltage. Threshold voltages of TFTs with thermal gate oxide were low. But mobility was also very low, contrary to expectation. The TFTs with APCVD and PECVD gate SiO_2 showed almost the same mobility.

Considering these results, and that the grain size of PECVD Si after SPC at 580 °C was not drastically increased [2], the optimization of the SPC process of LPCVD Si and combination of APCVD SiO_2 would be key technologies to improve TFT characteristics.

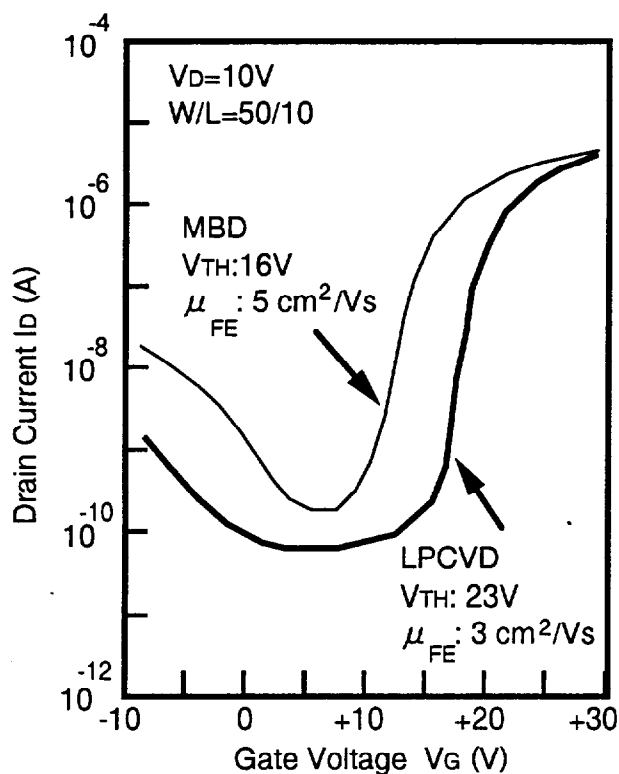
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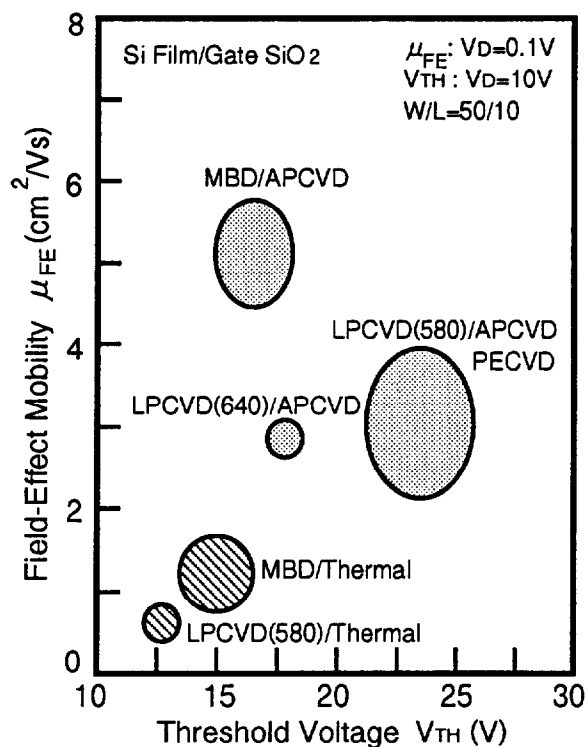


(a) TFT fabrication process

(b) Cross-sectional structure



(c) Gate voltage-drain current characteristics



(d) Field-effect mobility and threshold voltage

Fig.1 Preliminary fabrication of poly-Si TFTs.

A4. Large area LPCVD of Si

A4.1 LPCVD Apparatus

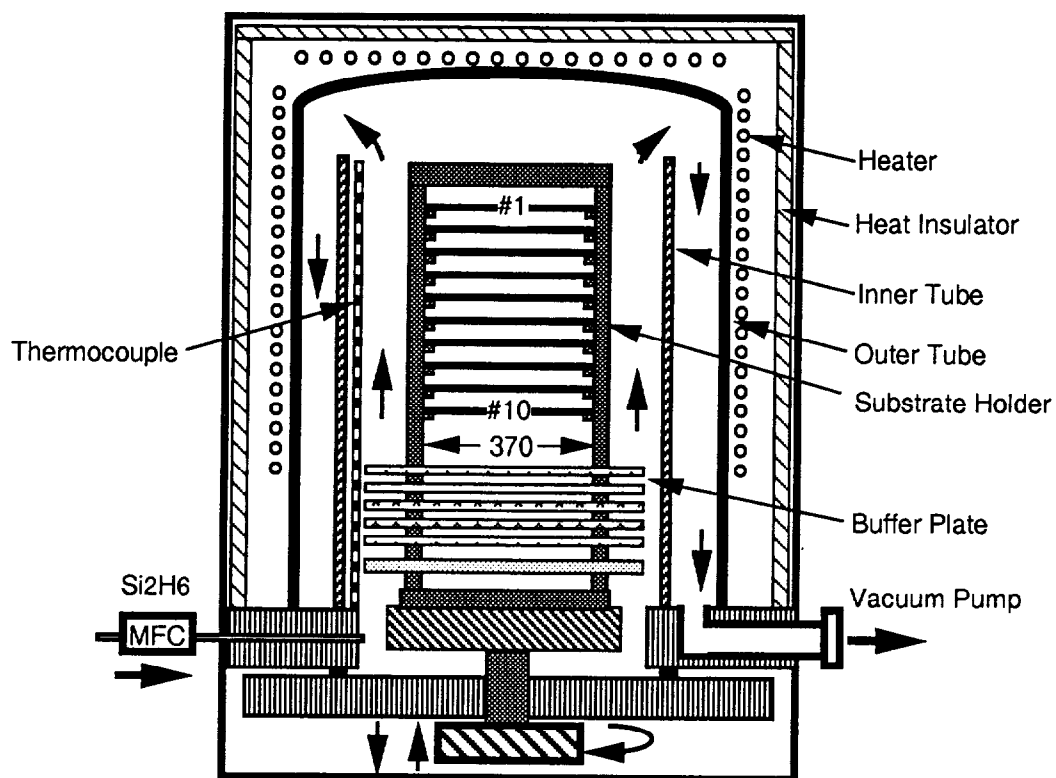
Fig. 1 shows a schematic structure of the developed LPCVD apparatus and a photograph of the substrate holder. Ten substrates (350 mm x 450 mm) (Asahi AN 635) were set horizontally on the substrate holder. The holder was rotated at 5 rpm. Reaction gas Si_2H_6 was introduced into the bottom of inner tube and exhausted from the top through the space between the inner and bell jar tubes. The substrates were heated in N_2 ambient for 2 h at 450°C . Then the chamber was pumped down to 6×10^{-3} Pa and reaction gas was introduced. The space between substrate was set to 20 mm to improve film thickness uniformity in the substrate. The chamber was heated by a three-zone heater. Generally, in the vertical type reactor, the bottom region showed low temperature at the same input power. The introduced gas also cooled the bottom region substrates. To realize uniform film thickness, the temperature of bottom region was raised by about 5°C . When reaction pressure was increased to 67 Pa, the gas phase reaction occurred and particles were generated. Considering uniformity of thickness, pressure of 27 Pa was selected as a standard. In these processes, no deformation of the substrates were observed. The machine was an original model for the production apparatus of large-area LPCVDs.

A4.2 Uniformity

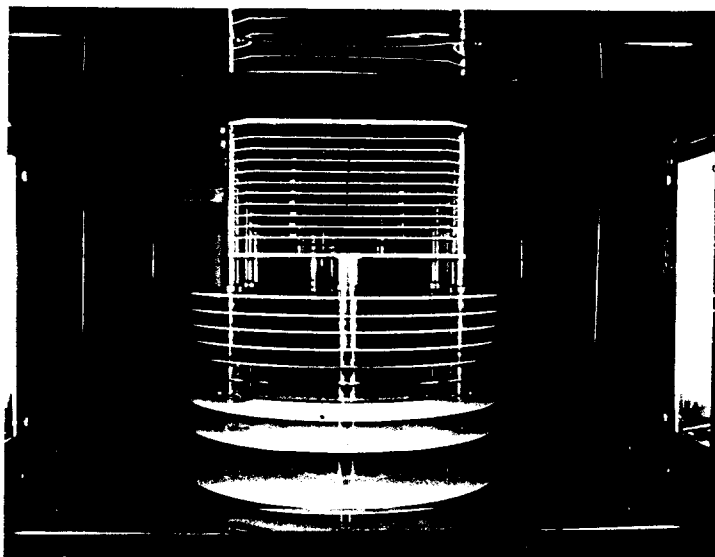
Fig.2 plots the film thickness dependence on substrate position in seven batches. The deposition time was changed. Though temperature was balanced to improve uniformity, the bottom region showed a slightly low deposition rate. Substrates #1-2 and #8-10 were used as dummies and #3-7 were used for TFT fabrication. The uniformities of 3.3% in a batch (5 substrates) and 1.0% (substrate center value) between batches were realized. Fig.3. shows example distribution of thickness in a substrate. The center region had a slightly low deposition rate, but uniformity of $\pm 6.4\%$ was obtained [1]. The whole area of the substrate was uniformly laser crystallized and 18.2" poly-Si TFT-LCDs were successfully fabricated [2].

A4.3 References

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(a) Schematic cross section



(b) Photograph of substrate holder

Fig.1. Developed LPCVD apparatus for 350 mm x 450 mm substrates.

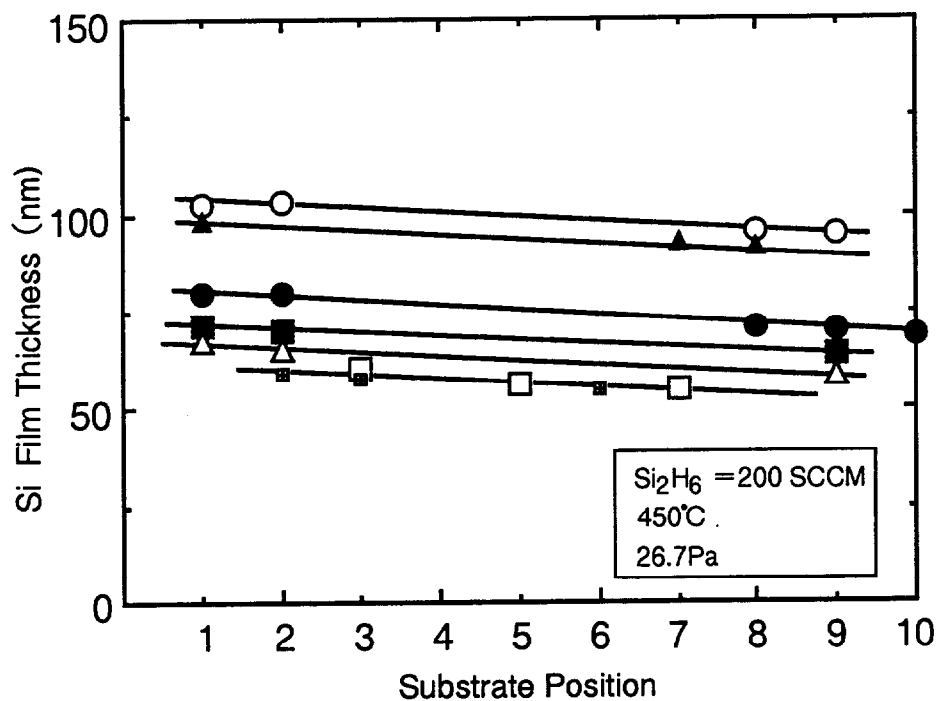


Fig. 2 . Dependence of substrate position on film thickness in seven deposition lots.

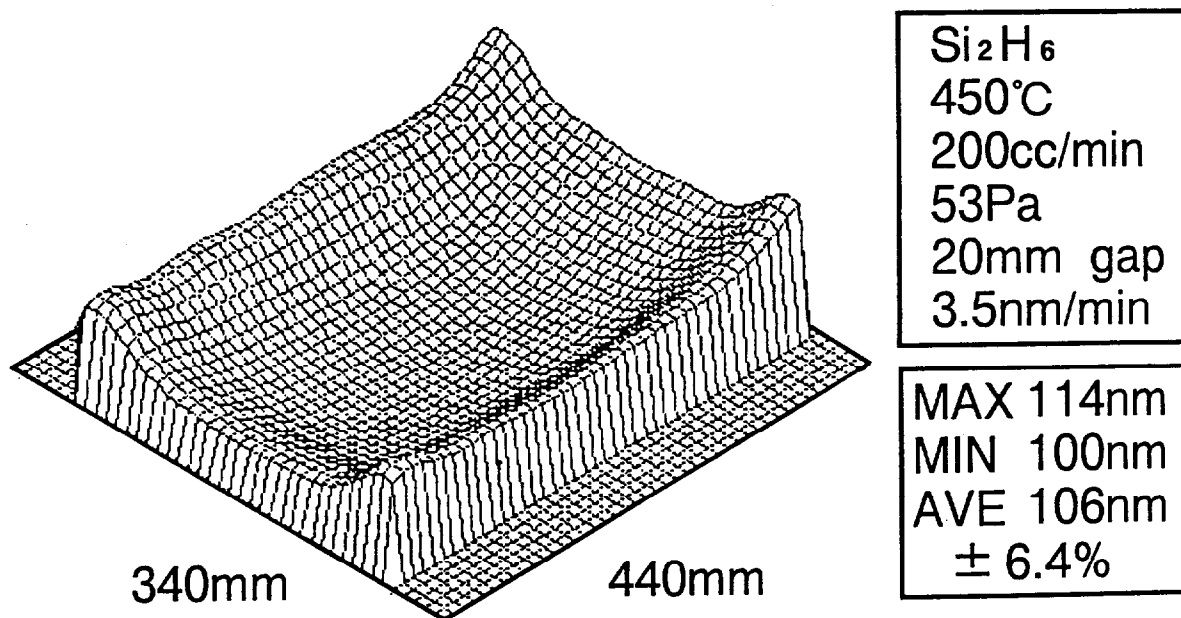


Fig.3. Typical uniformity example of film thickness in a substrate.

A5. ITO dry etching technologies

A5.1 Dry etching for ITO in TFT-LCDs

ITO is a special material used in TFT-LCDs, which is not used in LSI devices. Generally, large-area a-Si TFT-LCDs on large glass substrates are produced by wet etching for ITO. Recently, glass substrate size has been increased to 650mm x 830 mm. Thus, conventional wet etching needs a huge amount of chemicals. On the contrary, very high resolution TFT-LCDs such as high-temperature poly-Si TFT-LCDs need fine pattern etching (2-3 μ m) to realize a high aperture ratio and high performance. From this viewpoint, ITO dry etching should be indispensable not only for high performance AM-LCDs but also for "Green Technology".

In a typical fabrication process, a-Si films and insulator films (SiN) are already dry-etched. Recently, metallization materials such as MoW, Ta have been dry-etched.

In ITO etching, two kinds of etching gases were used. Halogen gases such as HBr, HI, HCl, HCl were tested. They have relatively high etching rates, but selectivity for other materials is not so good. Organic gases such as CH₃OH, CH₄, C₃H₆O were also studied. Their etching rates are not sufficient, deposits appear, but selectivity is good. These gases should be selected considering film structure and ITO film quality.

A5.2 Large-area etching by CH₃OH-Ar

CH₃OH (methanol) is used because it is non-toxic and is easy to handle [1]. A 13.56 MHz RF RIE type dry-etching chamber equipped with parallel electrodes (510 mm x 510 mm) was used. Total gas flow rate was 500 sccm. Maximum RF power was 2500 W. Amorphous ITO was deposited on a glass substrate at room temperature by DC magnetron sputtering to a thickness of 140 nm. Photoresist pattern (2 mm thick) was made on ITO film using OFPR 800.

Fig.1. shows etching characteristics of the CH₃OH-Ar system. Etching rate of ITO increased with increasing Ar content and saturated at about 50 %. It was suggested that etching rate depended on the physical etching of Ar ions, not on chemical etching by CH₃OH. Etching rate of glass also increased with increasing Ar content. Large selectivity of 10 for glass was obtained at 50% Ar. Considering etching rate and selectivity, Ar content of 50 % was used in the experiments. Fig. 2 shows etching characteristics dependence on gas pressure. When gas pressure was decreased, etching rate of ITO and resist were increased, and V_{dc} was increased. Increased ion energy enhanced the etching of both ITO and resist. The lower limit of RF discharge was about 1.3 Pa.

Fig. 3 shows SEM micrographs of the cross section of ITO dry-etched by CH₃OH-Ar(50 %) system. At 1.6 Pa, there was a very small amount of deposition on the resist wall, though many needle-like deposits were observed on the resist for 3.6 Pa etching. Formation of deposits critically

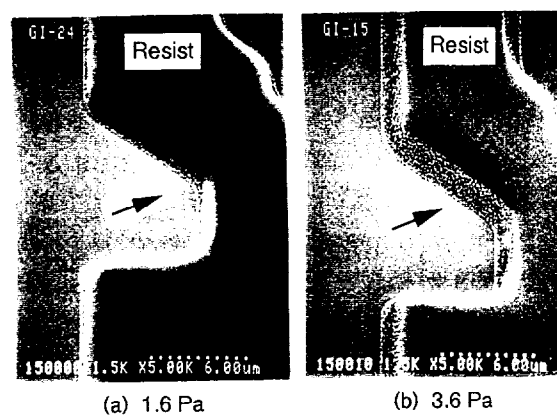
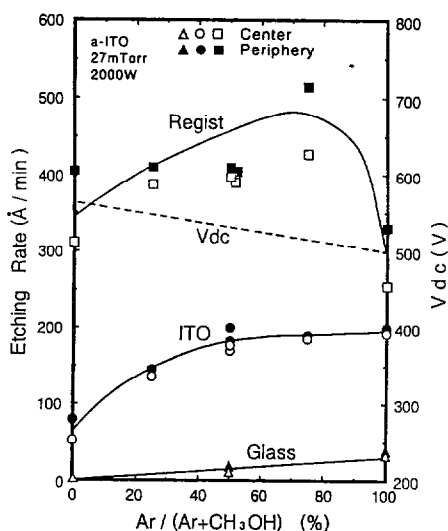


Fig. 4. SEM micrographs of surfaces of ITO dry-etched by CH₃OH-Ar system.

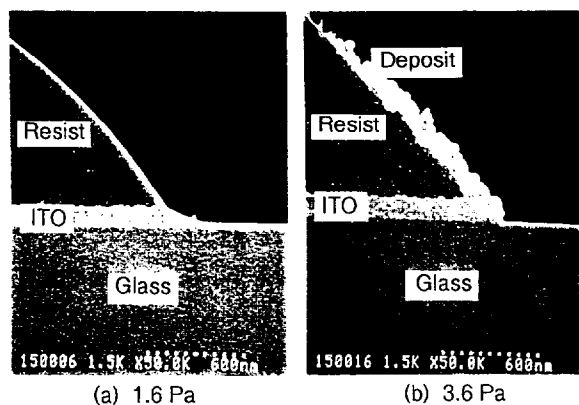
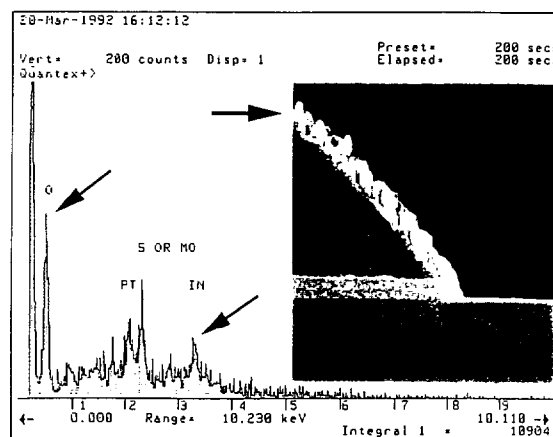
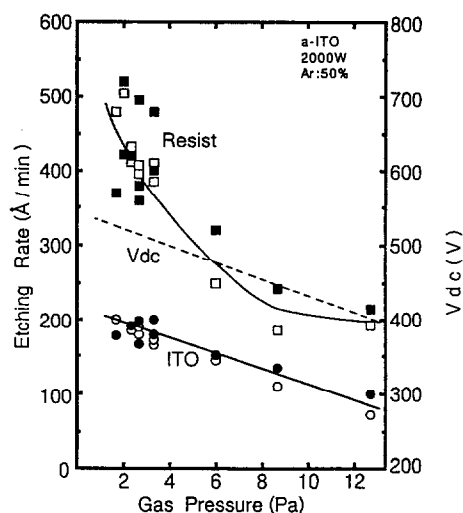


Fig. 3. SEM micrographs of cross section of ITO dry-etched by CH₃OH-Ar system.

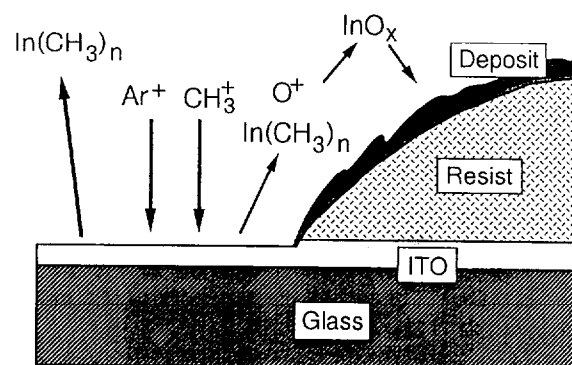


Fig. 6. A model of etching and deposition.

depended on gas pressure. Fig. 4 shows SEM micrographs of the plane surface the ITO and resist after dry etching. At 1.6 Pa, some deposits were observed on the concave side wall of resist (arrow). In the concave region, diffusion of the etching reaction products was interrupted and the apparent gas pressure was increased to enhance deposition. At 3.6 Pa, large amounts of deposits were observed on both straight and concave side walls. There were no deposits on the surface of the resist because physical etching by Ar ions dominated.

Fig. 5 shows the SEM-EDX spectrum of the deposited layer on the plane surface of resist for a 6.0 Pa etching. Peaks of indium and oxygen were observed. This indicated that the deposit was composed of indium oxide. It was not removed by ashing in oxygen plasma or with a resist remover and it remained as a residue. So, inhibition of deposits using low pressure etching is indispensable. Fig. 6 illustrates a model for the mechanism of etching and formation of deposits considering previous results.

Fig. 7 is a photograph of a 18.2" p-Si TFT array fabricated by the all dry etching process [2]. Four materials were dry-etched as follows.

Material	Gas	Etching Rate (nm/min)	Selectivity
ITO	CH ₃ OH-Ar(50%)	15	10-20 (SiO ₂)
AlSi	BCl ₃ +Cl ₂	55	2.1-3.8 (SiO ₂)
p-Si	CClF ₃ +O ₂	100	2.7- 2.8 (SiO ₂)
SiO ₂	CHF ₃	30	7-14 (Si)

The pixel ITO was well patterned using this technology and the TFT-LCD operated successfully [3].

Fig. 8 shows the effect of hydrogen ion irradiation on etching rate. Hydrogen ions were irradiated by a high density ion doping apparatus [4]. Etching rate increased with increasing acceleration voltage of hydrogen ions. Long time irradiation had a notable effect on increasing etching rate. Fig. 9 shows SEM micrographs of the cross section of ITO after hydrogen ions irradiation. Small grains ((a)) and large grains ((b)) were observed on the surface of the ITO in short-time and long-time irradiations, respectively. Fig. 10 shows XPS spectra of ITO films before and after hydrogen ion irradiation. The ITO surface was successively etched by Ar ions in analysis. Before irradiation, mainly indium oxide was detected. After irradiation, ratio of indium was clearly increased by reduction and the etching by CH₃OH-Ar was enhanced.

A5.3 Etching by CH₄-H₂

Preliminary etching experiments were made using CH₄-H₂ to increase etching rate. A small size RF RIE reactor with parallel electrodes of 225 mm x 225 mm and gap of 40 mm was used.

Fig. 11 plots the etching characteristics of the CH₄-H₂ system. A high etching rate of 73 nm/min was obtained at 100 % CH₄ and RF power of

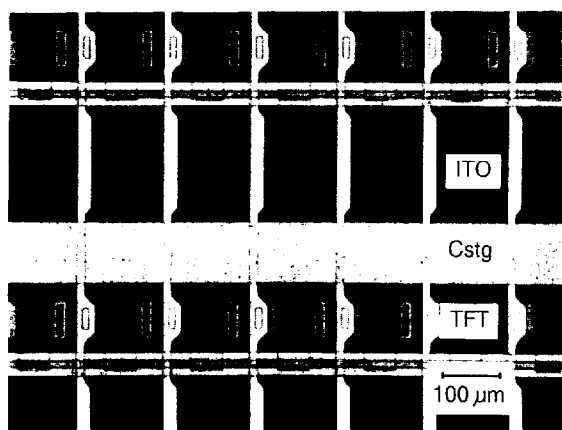


Fig. 7. Photograph of a 18.2" poly-Si TFT array with dry-etched pixel ITO.

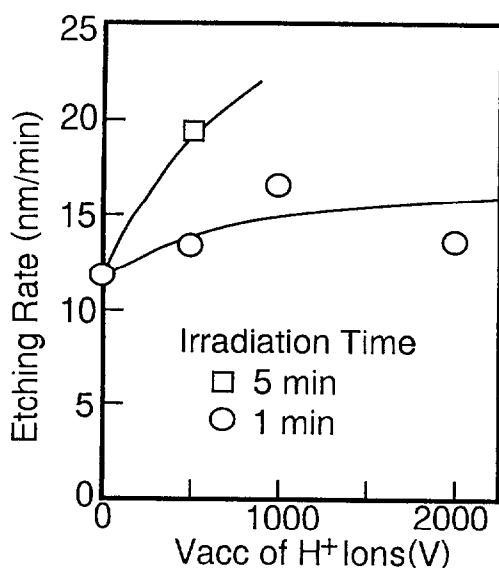


Fig. 8. Etching rate increase in CH₃OH-Ar system after H⁺ ion irradiation.

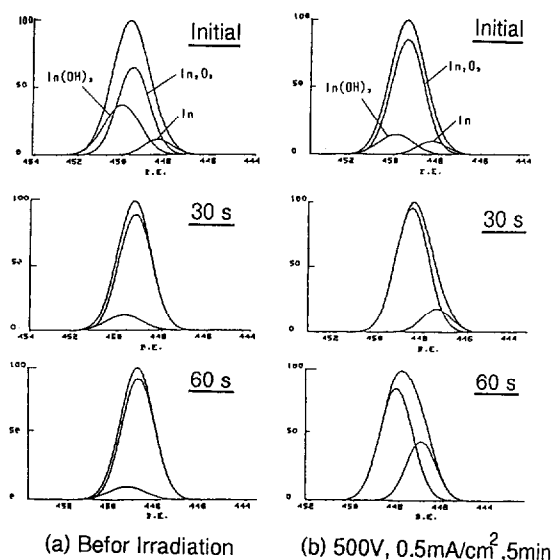


Fig. 10. XPS spectra of ITO films before and after H⁺ ion irradiation.

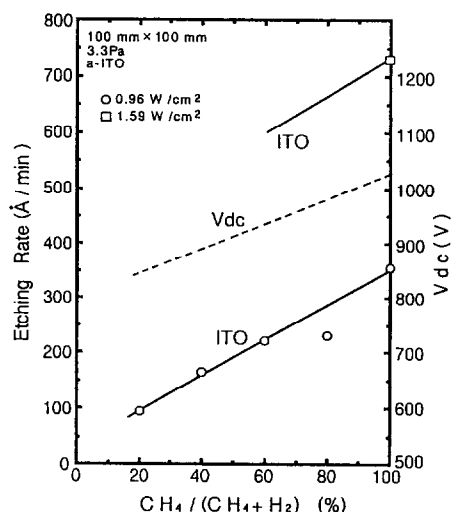
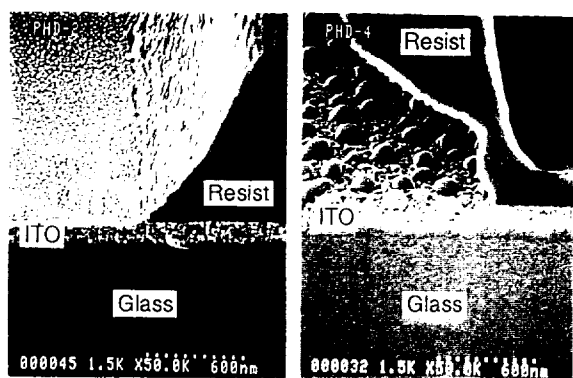
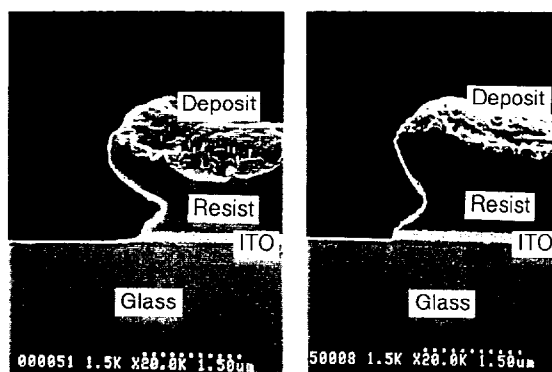


Fig. 11. Etching characteristics of CH₄-H₂ system.



(a) 1000V, 0.5 mA/cm², 1 min (b) 500V, 0.5 mA/cm², 5 min

Fig. 9. SEM micrographs of ITO after H⁺ ion irradiation.



(a) SiH₄ : 40% (b) SiH₄ : 100%

Fig. 12. SEM micrographs of cross sections dry-etched by CH₄-H₂ system.

1.59 W/cm². Fig. 12 shows SEM micrographs of the cross section dry-etched by CH₄-H₂. At the CH₄ ratio of 40 % and 100 %, deposits were needle-like and film-like, respectively. Careful optimization of etching conditions should achieve high etching characteristics.

A5.4 Dry etching by HI

The etching experiments were also made using HI-H₂-Ar to increase etching rate. A small size RF RIE reactor with parallel electrodes of 225 mm x 225 mm and gap of 60 mm was used.

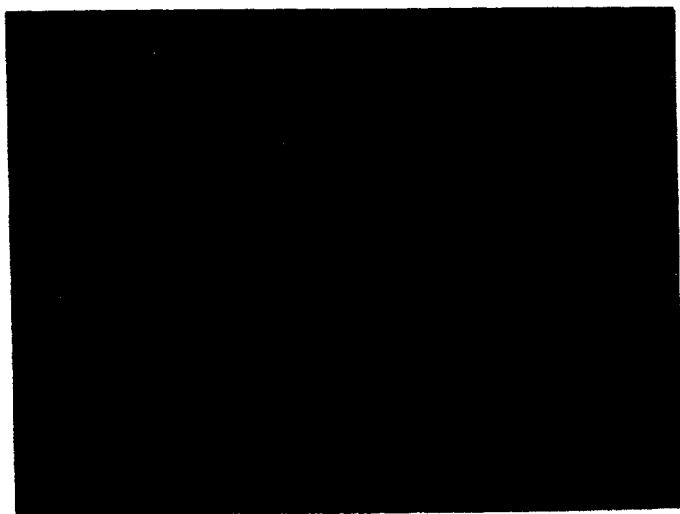
Fig. 13 shows surface of resist with and without baking after dry etching. High temperature resist baking was effective to reduce resist damage in etching.

Fig. 14 shows SEM micrographs of the cross section and side view of ITO after dry etching. Poly-ITO was well etched without residue. Taper angle was about 70 °.

In the fabrication of 18.2" poly-Si TFT-LCDs, four materials, poly-Si, SiO₂, AlSi, and ITO were all dry etched. Example cross sections of AlSi and SiO₂ are shown in Fig. 15. AlSi layer was dryetched well on the large substrates with positive taper angle of about 80°. Interlayer SiO₂ and pixel ITO were deposited with good step coverage on it. SiO₂ was also dry-etched well with good selectivity on poly-Si with taper angle of about 80°.

A5.5 References

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- [2] A. Mumura, Y. Mikami, K. Kuwabara, Y. Mori, M. Nagai, Y. Nagae and E. Kaneko: *Conf. Record 1994 Int. Display Research Conf.* (1994) 126.
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- [4] A. Mimura, G. Kawachi, T. Aoyama, T. Suzuki, Y. Nagae, N. Konishi and Y. Mochizuki: *IEEE Trans Electron Devices T-ED* **40** (1993) 513.

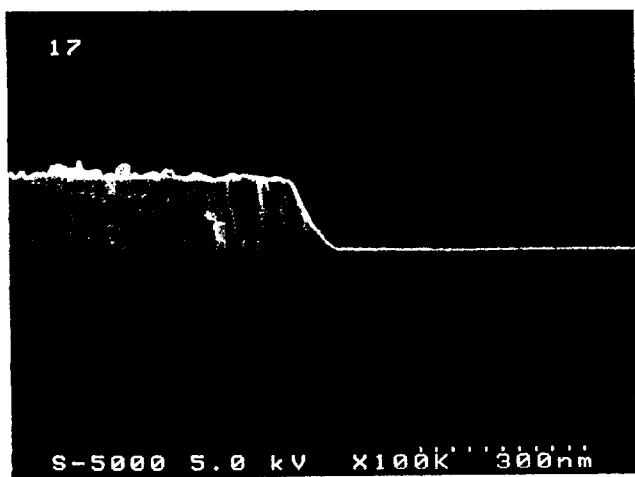


(a) Resist baking at 120°C

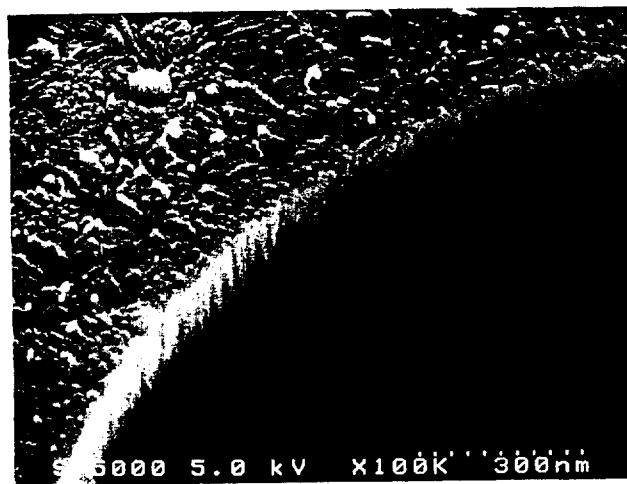


(b) Resist baking at 180°C

Fig. 13. Dependence of resist damage on baking temperature in ITO etching by HI.

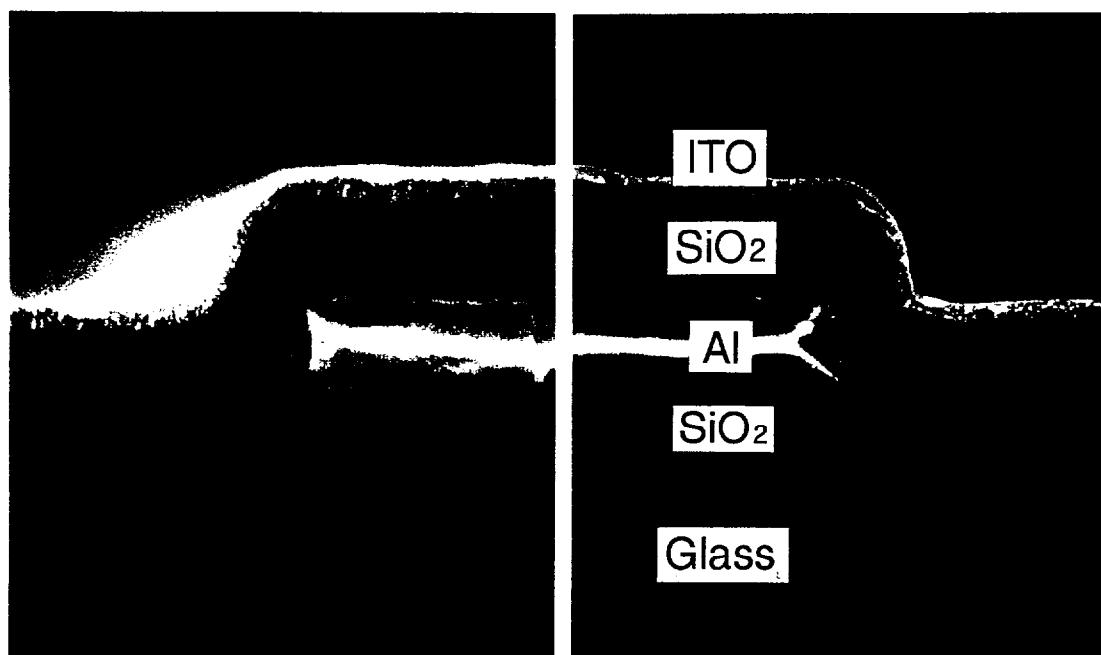


(a) Cross section



(b) Side view

Fig. 14. SEM micrographs of cross section and side view of ITO dry-etched by HI.



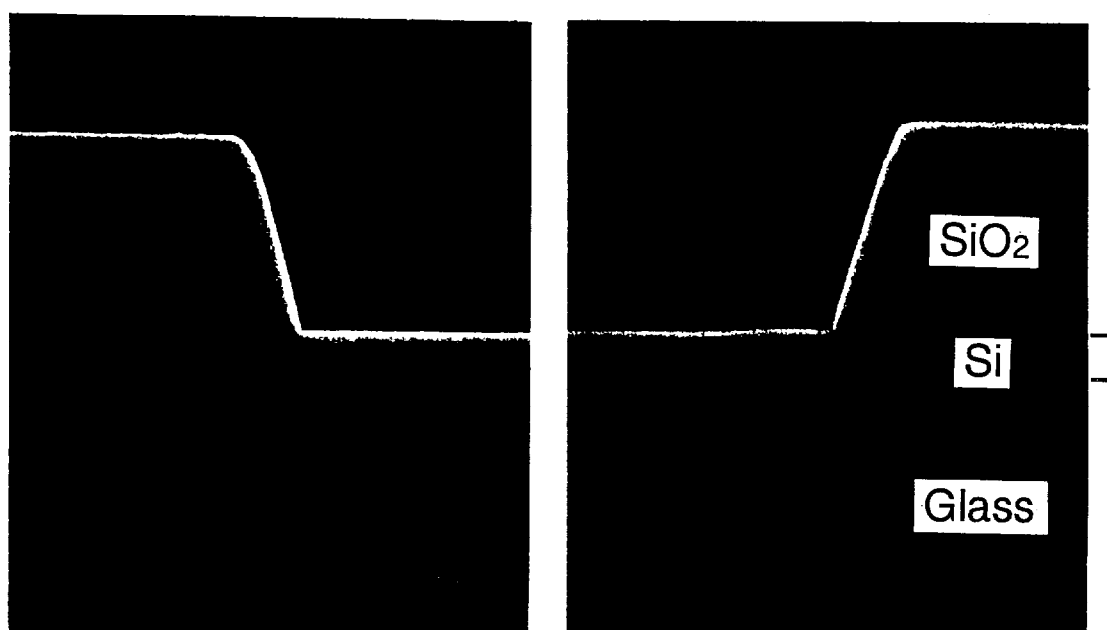
(a) periphery

(b) center

300nm

$\text{BCl}_3 + \text{Cl}_2$	$0.77\text{W}/\text{cm}^2$	$45\text{nm}/\text{min}$
(14 : 1)	4.7Pa	

(a) AlSi layer with SiO_2 and ITO



(a) center

(b) periphery

CHF_3	$0.77\text{W}/\text{cm}^2$
4.0Pa	$40\text{nm}/\text{min}$

200nm

(b) SiO_2 on poly-Si layer

Fig. 15. SEM micrographs of dry-etched cross section of AlSi and SiO_2 layers.

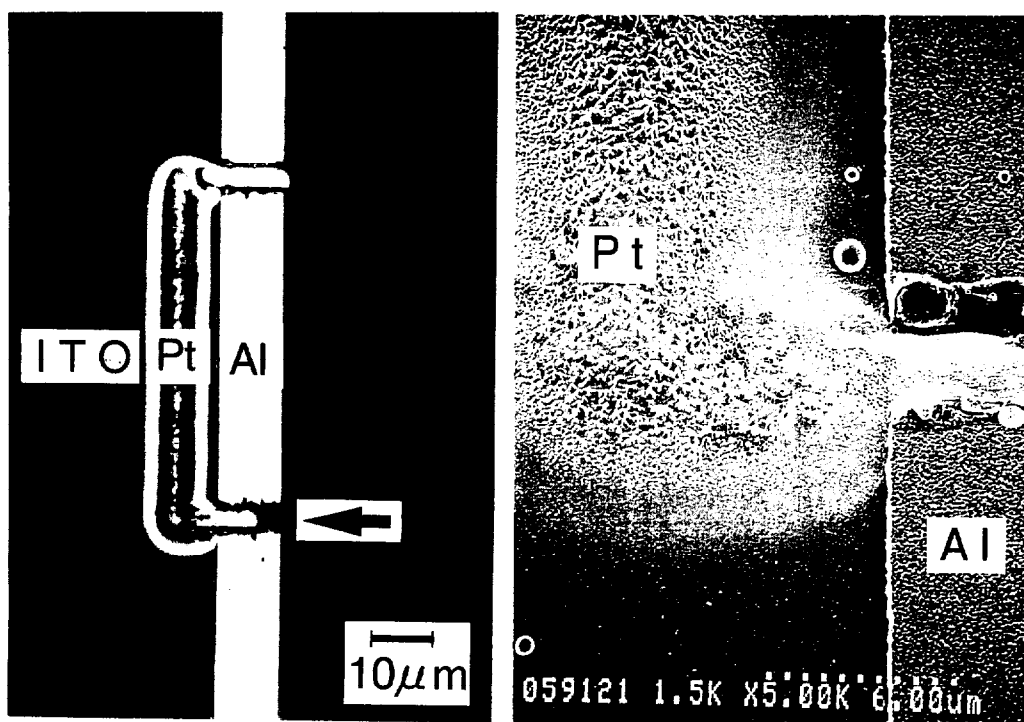
A6 Repair technology

A6.1 Repair technology

Laser cutting repair is a common technique in a-Si TFT production. Repair of connection must be indispensable, especially for large TFT-arrays. Pt metal deposition was recently developed for TFT repair applications [1]. Thermal decomposition of $\text{Pt}(\text{PF}_3)_4$ by CW Ar laser was used. Fig.1 shows example repairs for poly-Si TFTs. (a) shows deposition for an Al line. Because Al is a good thermal conductor, heating of Al was not sufficient and Pt deposition on bare Al was imperfect. To improve deposition efficiency, a high power Ar laser was introduced and Pt was deposited on the pre-cut (YLF laser) bare Al region. Poly-Si conductors (gate, source and drain) were also cut and connected ((b)). Fig. 2. shows example characteristics of a TFT before and after repair treatment for drain electrode (cut and deposition) (refere to Fig.1.(2)(a)). Conduction of the drain was recovered and the TFT was successfully operated after the repair treatment without damage for TFT.

A6.2 Reference

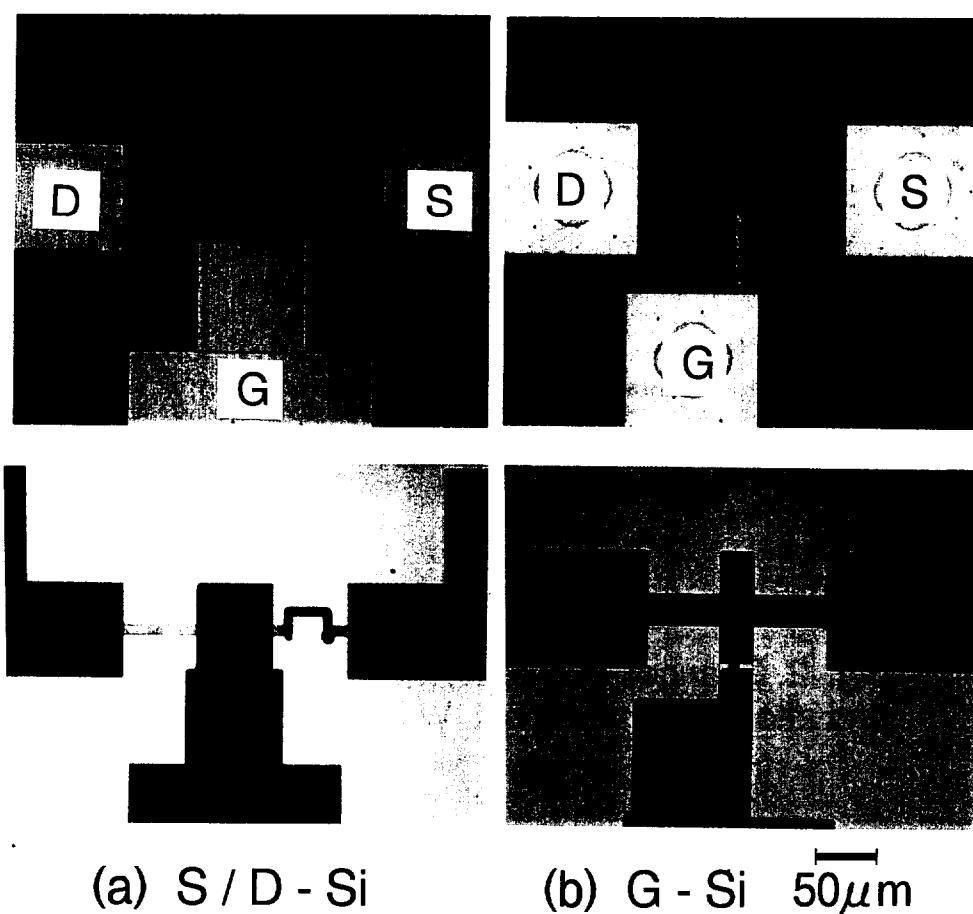
[1] R. Comunale et al.: Information Display Vol. 7 (1991) 9.



(a) Photo - M S

(b) S E M

(1) Aluminum line

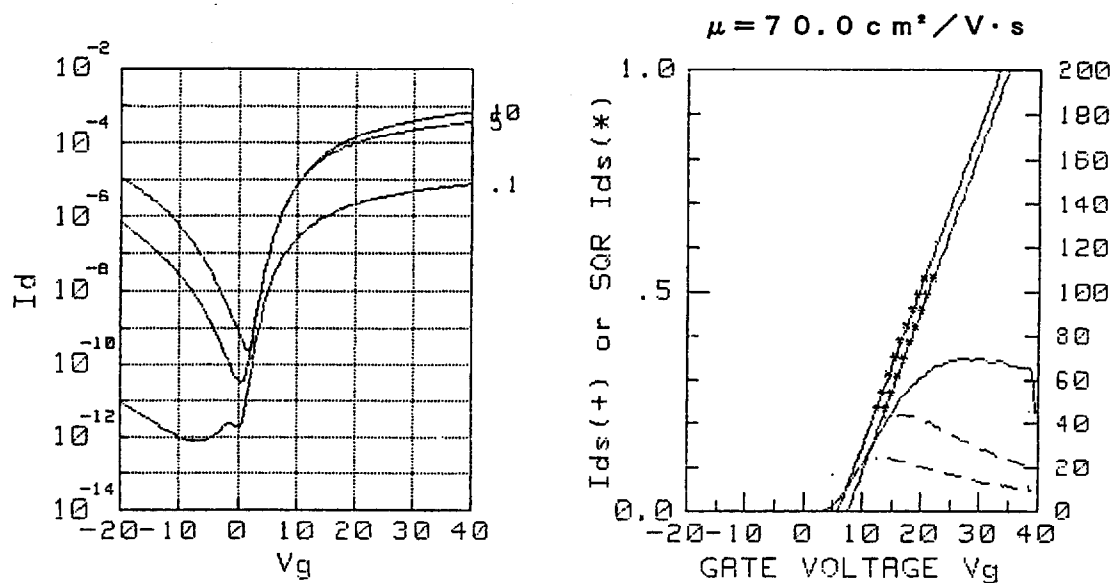


(a) S / D - Si

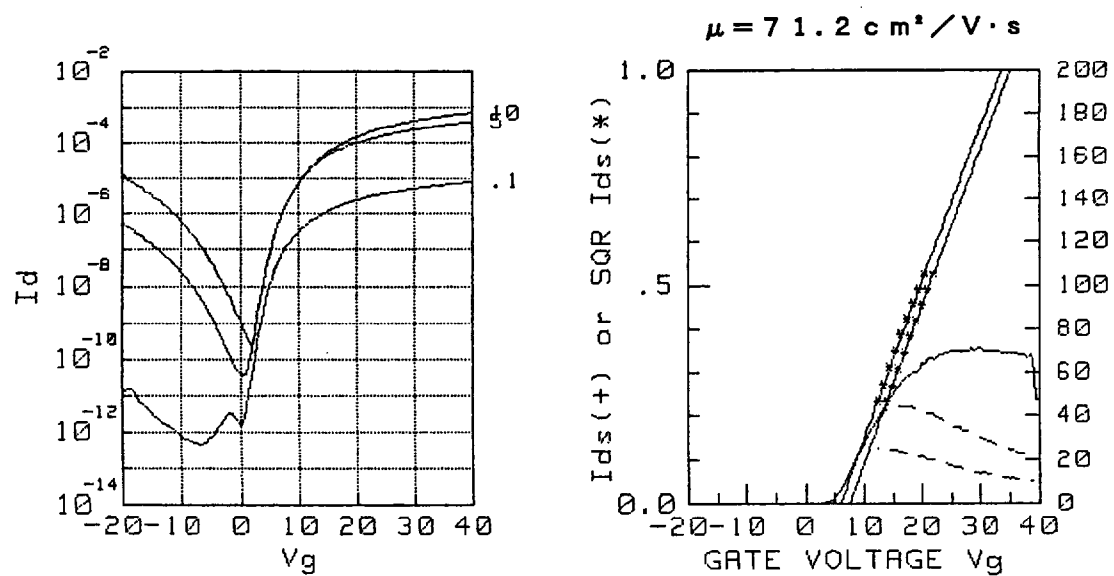
(b) G - Si 50μm

(2) Poly-Si gate, source and drain

Fig. 1. Repair technology for poly-Si TFTs.



(a) Before repair



(b) After repair

Fig. 2. Changes of characteristics of TFT before and after repair treatment. $W/L=180/100$ (μm).