# 論文 / 著書情報
# Article / Book Information

| | |
|---|---|
| 題目(和文) | NRZデータ・ストリームに適応可能なクロック及びデータ再生用PLL |
| Title(English) | A Clock and Data Recovery PLL Applicable to NRZ Data Stream |
| 著者(和文) | 出井義純 |
| Author(English) | Gijun Idei |
| 出典(和文) | 学位:日本,<br>学位授与機関:東京工業大学,<br>報告番号:甲第5731号,<br>授与年月日:2004年3月26日,<br>学位の種別:課程博士,<br>審査員: |
| Citation(English) | Degree:Japan,<br>Conferring organization: Tokyo Institute of Technology,<br>Report number:甲第5731号,<br>Conferred date:2004/3/26,<br>Degree Type:Course doctor,<br>Examiner: |
| 学位種別(和文) | 博士論文 |
| Type(English) | Doctoral Thesis |

# A Clock and Data Recovery PLL Applicable to NRZ Data Stream

**Gijun Idei**

**Adviser: Professor Hiroaki Kunieda**

**Department of Communications and Integrated Systems**
**Graduate School of Science and Engineering**
**Tokyo Institute of Technology**

**March, 2004**

# Contents

# Summary

A new adaptive 4-state phase-frequency detector (PFD), which is an augmentation of traditional 3-state PFD to enable the function both of frequency- and phase-detector even in the presence of missing data transitions, for clock and data recovery (CDR) PLL of non return to zero (NRZ) data, is presented. The PLL achieves false-lock free operation with rapid and wide frequency- and bit-rate-capture range.

Applications of the PFD to a fixed bit rate and variable bit rate CDR are presented.

The variable bit rate operation is achieved by adaptive delay control of data delay. Circuitry and overall architecture are described in detail.

z-Domain analysis for third order loop is also presented as well as its effectiveness for evaluation of loop stability and jitter peaking.

Key words:
Capture Range, CCO, CDR, clock and data recovery, false lock, jitter, NRZ, PFD, phase frequency detector, PLL, VCO, z-Domain Analysis.

# Chapter 1

# Introduction

One of the main challenges for designing phase-frequency detectors (PFD) or phase detector (PD) in clock and data recovery (CDR) systems arises from the need to deal with missing data transitions in non return to zero (NRZ) data. There are several examples of designs that deal with the issue of missing data transitions, but they each suffer some drawbacks.

A PD proposed by Hogge [1] operates for NRZ data, but can incur large jitter due to a ripple on the charge pump output even in the phase-matched state from successive charging and discharging cycles. The "tri-wave" method [2, 3] is an improvement over the Hogge PD, but only provides phase locking and still lacks frequency detection. Therefore, a frequency capture aid such as a rotational slip detector [6] is required [2]; otherwise, application is restricted to a narrow frequency range.

Another clock recovery system called a “quadricorrelator” is possible [4, 5], but frequency capture range is restricted to plus or minus 50% [5, 6].

In applications with continuous pulses such as frequency synthesizers, a 3-state PFD [7] is widely used. However, this PFD cannot be used for coded data streams with missing data transitions because it falsely generates error pulses.

This thesis presents a 4-state augmentation of the traditional 3-state PFD to enable both frequency and phase lock even in the presence of missing data transitions. The proposed PFD relies on a current-controlled delay line for data differentiation [9] in order to detect original clock frequency component and data transitions, and operate for coded NRZ data streams.

For fixed bit rate application, the delay is adapted through negative feedback to avoid false-lock conditions that can occur for this PFD [12].

For variable bit rate application, adaptive data delay is proposed. Narrow and wide variable bit rate applications are also presented.

The proposed PFD and accompanying PLL design for clock and data recovery are described in detail and robust operation is verified through simulation results.

z-Domain analysis of the third order loop is also presented as an effective tool for stability issues.

Function and operation of the PFD were verified by simulations and fabricated LSI.

# Chapter 2

# Conventional PD and PFD

## 2.1 Summary

This chapter presents the overview of the current technologies of PD and PFD as well as their features or drawbacks. PD or PFD are categorized in linear- and binary-PD or PFD. In the former, the out put of the PD or PFD is linear to the phase difference of the inputs, and in the latter the output is only polarity of the phase error and lacks in the magnitude of the phase difference.

In principle, the NRZ data does not have explicit frequency component of original clock by which the NRZ data their selves are generated. Therefore, if it is required that a detector should have the function of frequency detector, and make frequency capture and lock-in, first of all, the frequency component of original clock should be extracted. For this purpose, the differentiation of NRZ data to RZ (Return to Zero) is mandatory.

In those pints of view, current PD or PFD will be analyzed next.

First Hogge PD, second Quadricorrelator, third Rotational Slip Detector, forth Bang Bang PD (binary PD), fifth published papers on CDR for NRZ and sixth Market available product are described.

## 2.2 Hogge PD

There is a PD known as Hogge PD, which is directly applicable to NRZ data stream with missing transitions [1] as shown in Fig. 2.1. As seen in Fig. 2.1, pulse width of U1 varies with phase difference, whilst D1 is fixed in same width of local clock Xck as a reference pulse. Therefore this is a linear PD. Fig. 3.2 shows the Verilog simulated waveforms of U1 and D1 at phase matched state. Fig. 2.2a and 2.2b show the SPICE simulated output waveform of charge pump circuit at phase matched state. This simulation was done so that the charging current is intentionally larger than discharging current considering wafer fabrication process fluctuations. As shown in Fig. 2.2a, even at phase matched state, during U1 high, the charge pump circuit is charging, and during next D1 high, discharging successively.

At missing pulse state, no charging nor discharging occurs. However, as shown in Fig. 2.2a the charge re-distribution occurs between C1 and C2 (Fig. 3.7) of charge pump circuit. Therefore, the ripple is very large.

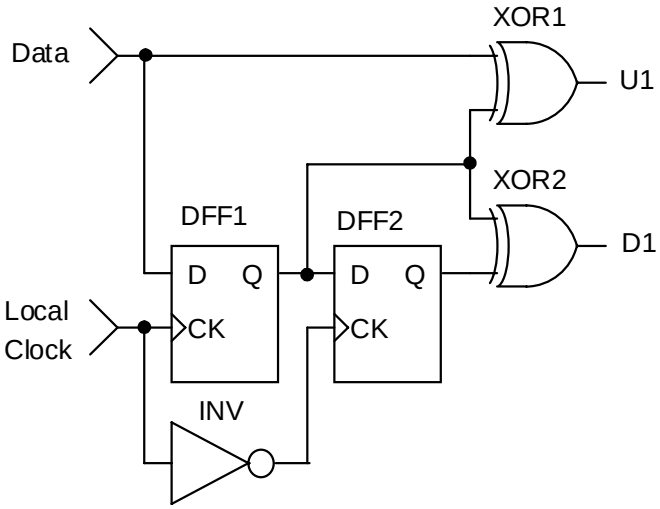
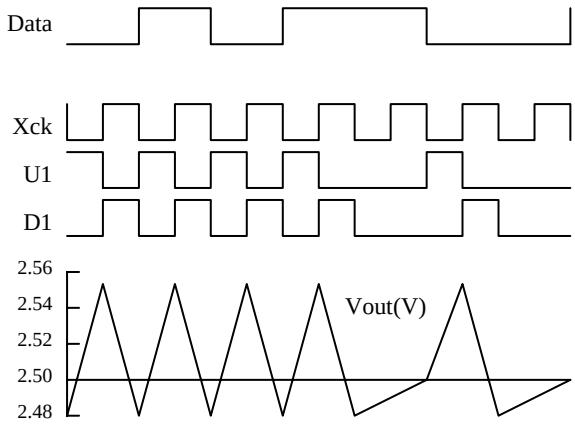



Fig. 2.1 Hogge's PD



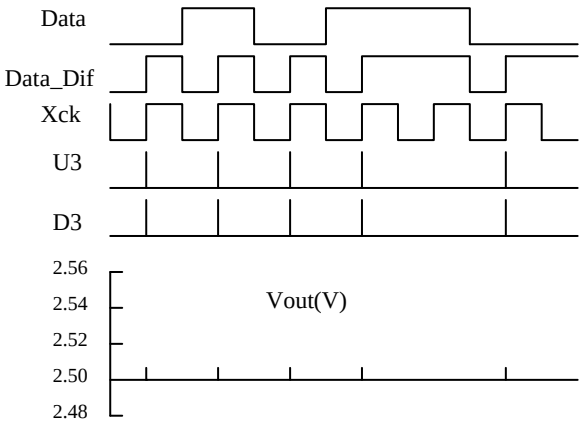




Fig. 2.2a Charge pump output: Hogge's PD

Fig. 2.2b Charge pump output: New PFD

Fxck = 100MHz, C1 = 20pF, C2 = 0.047uF, R1 = 390 ohm,
PMOS: W/L = 4u/4u, NMOS: W/L = 4u/12u, Vdd = 5V

Moreover, this ripple has a data pattern dependency. In practical application of this PD, the adjustment for charging and discharging currents is very critical because the width of output pulses is very large even at phase locked state. If there is un-match in charging and discharging currents, phase offset occurs even at phase locked state. If the charging current is I +ΔI, the pulse width of charging T +ΔT, discharging current I and discharging pulse width T, at frequency and
phase locked state, electronic charge is equal between charging and discharging as shown in (2.1).

$$(\mathbf{I}+\Delta\mathbf{I})(\mathbf{T}+\Delta\mathbf{T})=\mathbf{IT} \qquad (2.1)$$

Hence,

$$\Delta\mathbf{T}=-\frac{\Delta\mathbf{I}}{\mathbf{I}+\Delta\mathbf{I}}\,\mathbf{T} \qquad (2.2)$$

In Hogge PD, T is half of local clock period and it is very large. To maintain low offset ΔT, low ΔI is required. This makes the current adjustment very critical. Therefore, zero-offset compensation is required in real applications.

Another drawback of this PD is its weakness or lack in function as a frequency detector. Therefore, at the frequency acquisition stage, another frequency capture aid such as rotational slip detector should be required. However, it is an advantage of this PD that it is applicable to wide bit clock frequency range if it is used with adequate frequency acquisition aid, because this PD has no time restricted component such as delay element.

## 2.3 Quadricorrelator

Bellisio introduced a linear PFD applicable to NRZ data which is called Qaudricorrelator [5], which was derived as a digital version PFD from color signal demodulator of NTSC color TV system. In NTSC color TV system, the color signals are transmitted as a quadrature modulation on sub-carrier of 3.58MHz, and its frequency and phase is synchronized by the “Color Burst” signal, which is a repetition of “1010” signal, during the retrace interval of horizontal scanning. Therefore it is a kind of NRZ signal.

The quadricorrelator is shown in Fig. 2.3. As shown in Fig. 2.3 the quadricorrelator consists of three multipliers U, U0 and U1, low pass filters, and a differentiator. RZ data is required as an input data. Special attention should be paid about this point that the extraction of the frequency component of original clock should be made first.

The differentiated RZ data is fed to two multipliers U and U0. Other input of U0 is fed by VCO signal, and 90 degree ($\pi/2$) shifted VCO signal is fed to U.

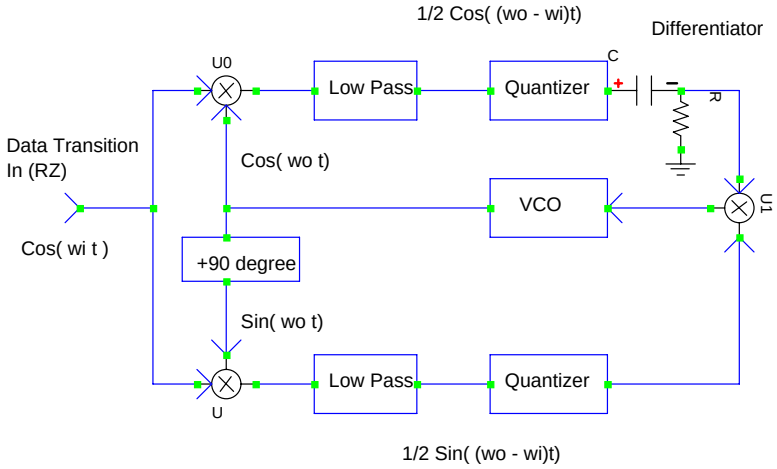



Fig. 2.3 Quadricorrelator, Two differentiators required
U, U0, U1: Multiplier- Gilbert Circuit = Exclusive OR

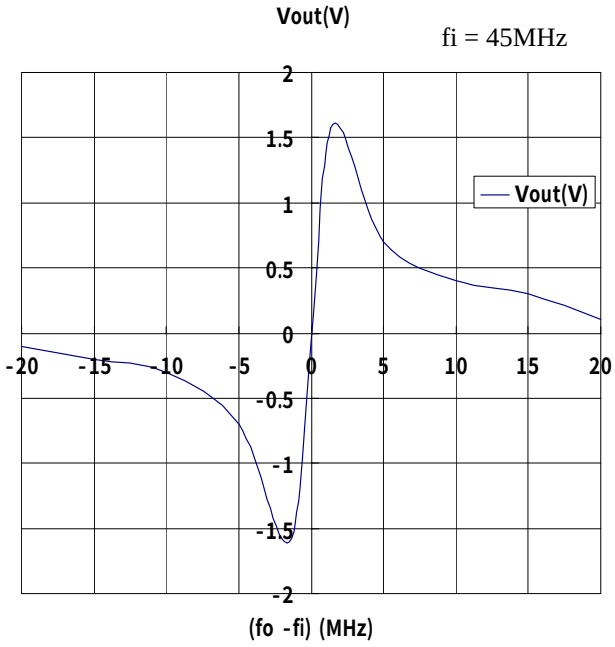



Fig. 2.4 Characteristics of Qadricorrelator

J. A. Bellisio "A phase-Locked Timing Recovery Method for Digital Regenerator" IEEE Int. Comm. Conf. Rec., vol. 1, pp. 10-17 to 10-20, June 1976
B. Razavi, "A 2.5-Gb/sec 15-mW BiCMOS Clock Recovery Circuit", Symposium on VLSI Circ. Dig. Of Tech. Papers, pp83-84, 1995

$\pi/2$ shifted signal can be easily attained from the center tap of the VCO which consists of even stage of delay elements. Gilbert circuit is used for U, U0 and U1. Gilbert circuit functions as a multiplier in small signal, and an Exclusive OR circuit in large signal.

Fig. 2.4 is the characteristics of the quadricorrelator [5]. As shown in Fig. 2.4, the frequency capture range of the quadricorrelator is only +/- 50 % of VCO frequency.

## 2.4 Rotational Slip Detector

Afonso introduced a rotational slip detector [6] as shown in Fig. 2.5. It is a kind of frequency detector, and functions as a frequency capture aid .

Four DFFs are used in rotational slip detector. Incoming differentiated RZ data is fed to all clock input of DFFs, and local VCO clock Xck is fed to DFF1, and output of DFF1 is connected to D input of DFF3. The differentiation of incoming data is required for the function of frequency detector.

$\pi/2$ phased local clock is fed to DFF2, and output of DFF2 is connected to D input of DFF4. All outputs are connected to combinational circuit, and frequency up pulse Fup and down pulse Fdown are generated in case of the frequency of Xck is different from the frequency of incoming RZ data. If the frequencies are matched, no output is generated on both of Fup and Fdown.
In other word, the circuit does not have the function of phase detection, and only has that of frequency detection. Therefore the circuit is used for a frequency capture aid.

The characteristics of frequency capture is showm in Fig. 2.6. As seen in Fig. 2.6, the frequency capture range is also +/- 50%.

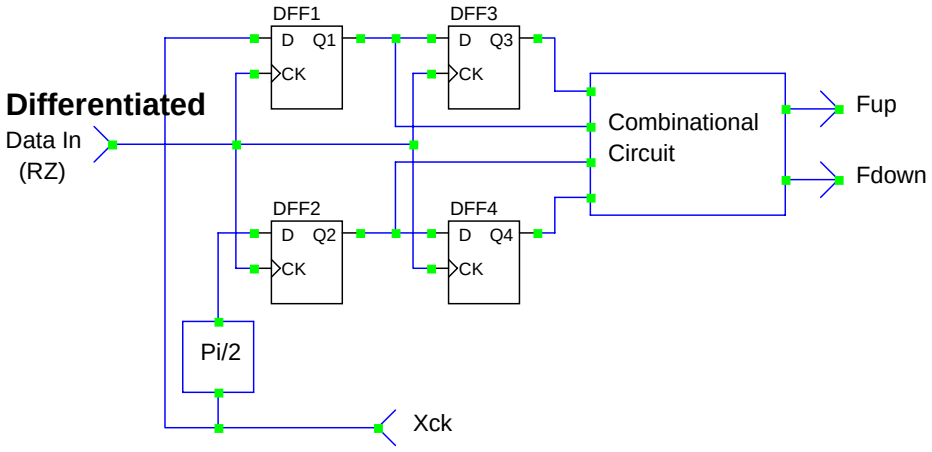



Fig. 2.5 Rotational Slip Detector

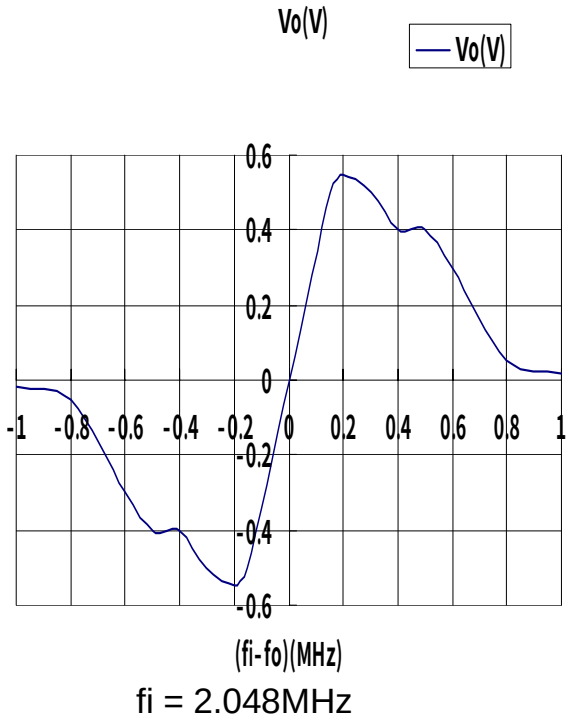



Fig. 2.6 Characteristics of Rotational Slip Detector

Rotational Slip Detector

J. A. Afonso etal, “A Phase-Locked Loop with Digital Frequency Comparator for Timing Signal Recovery” National Telecom. Conf. Rec. paper 14.4 1979

## 2.5 Bang-Bang Phase Detector (Binary PD)

In high bit rate application such as Giga bps area, it is very hard to realize the linear phase detector. Therefore, binary phase detector so called Bang Bang phase detector is used. The binary phase detector detects the polarity of the phase difference only, and neglects the magnitude of phase difference. Therefore, nonlinear behaviors are recognized.

Fig. 2.7 (a) shows a Bang Bang Phase detector [32]. As seen in Fig. 2.7, 4 DFFs are used, DFF1 to DFF3. DFF1, DFF2 and DFF4 are triggered by VCO clock $\Phi$, and DFF3 is triggered by inverted $\Phi$. Data inputs D of DFF1 and DFF3 are connected to input NRZ data stream. Data inputs of DFF2 and DFF4 are connected to output of DFF1 and DFF3 respectively. Exclusive OR is taken between the outputs of DFF2 and DFF4 as Up pulse output, and that of DFF1 and DFF4 as Down pulse. Recovered data is taken from the output of DFF1.

As seen in Fig. 2.7, DFF1 acts as a data sampler and DFF3 acts as a timing sampler. Since identical samplers are used both of data and timing sampler, there is no systematic timing offset. This is the feature of this PD. Another feature is the amenity for other digital systems because this PD is full digital and no analogous component.

However, the gain curve of this PD is very large, and there is no linear zone as shown in Fig. 2.7 (b), and very wide width Up and Down pulses are generated as shown in Fig. 2.8. Therefore, if the charge pump current Icp is selected improperly stability issue occurs. Moreover, if the jitter of the input data itself is high, the output jitter is exaggerated to high. Fig. 2.9 shows an example of SPICE simulation. As seen in Fig. 2.9 (B), even at phased matched state, large ripple is generated. Therefore, the constant of filter in charge pump, small R1 and large C1, should be required to reduce the jitter, which means inherently large time constant and large lock-in time.

This PD does not have the function of frequency detector. However, the integrator of charge pump filter, series connection of R1 and C1, functions a narrow frequency detector as shown in Fig. 2.9 (A). Capture range of this frequency detection is roughly equal to the magnitude of the ripple at phase locked state [27]. Therefore, if certain amount of rock-in range is required, certain amount of jitter is unavoidable.

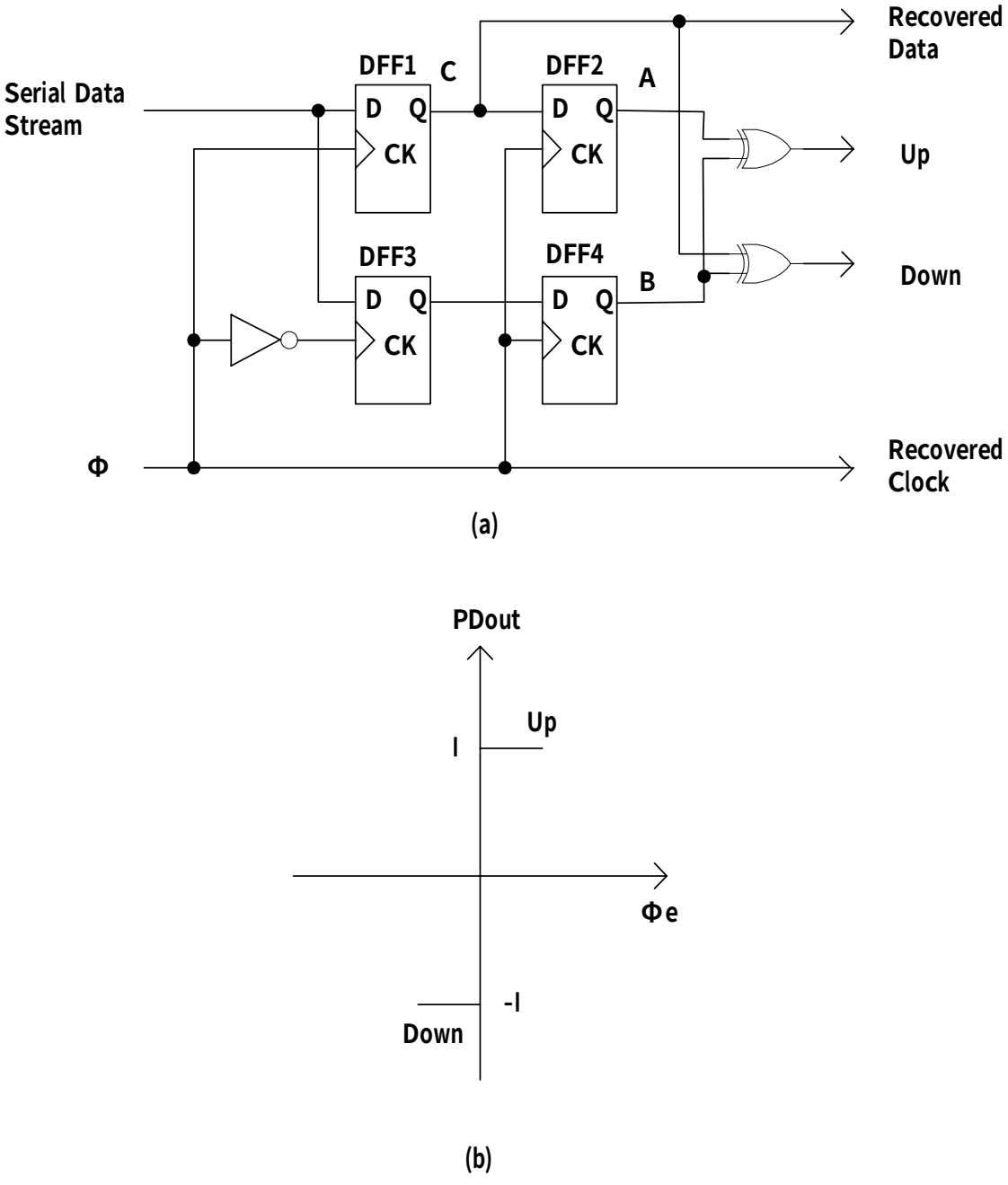



Fig. 2.7 Bang Bang Phase Detector,
(a) Circuit diagram, (b) Phase detector gain curve

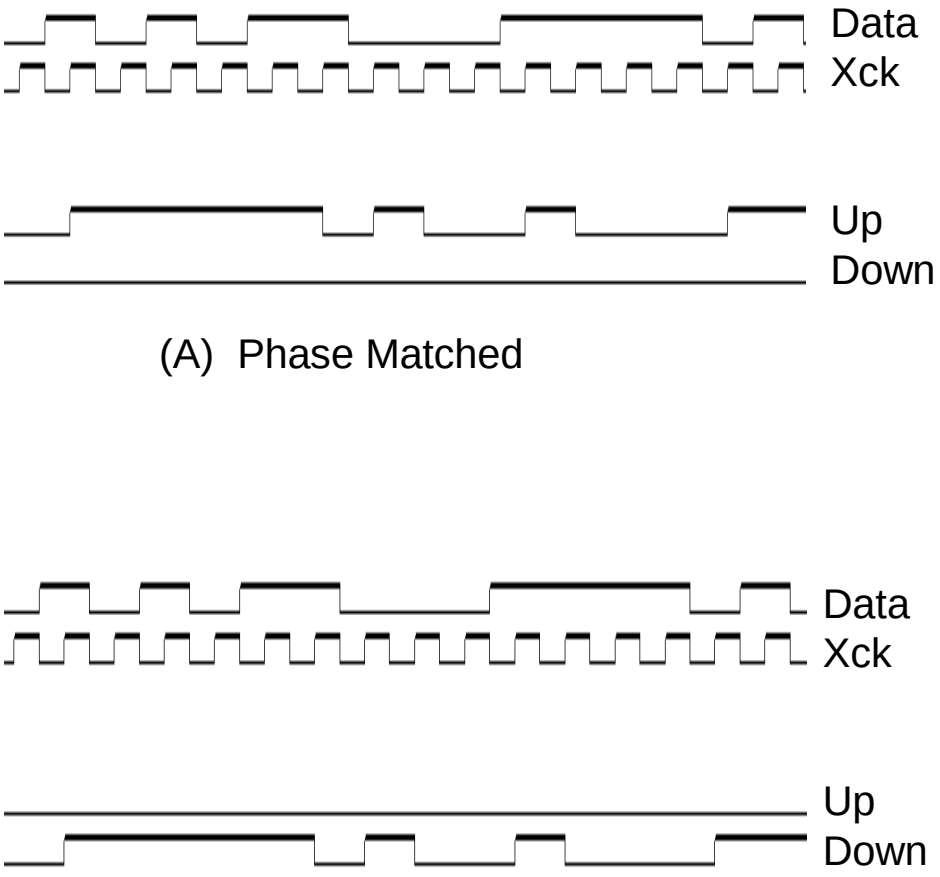
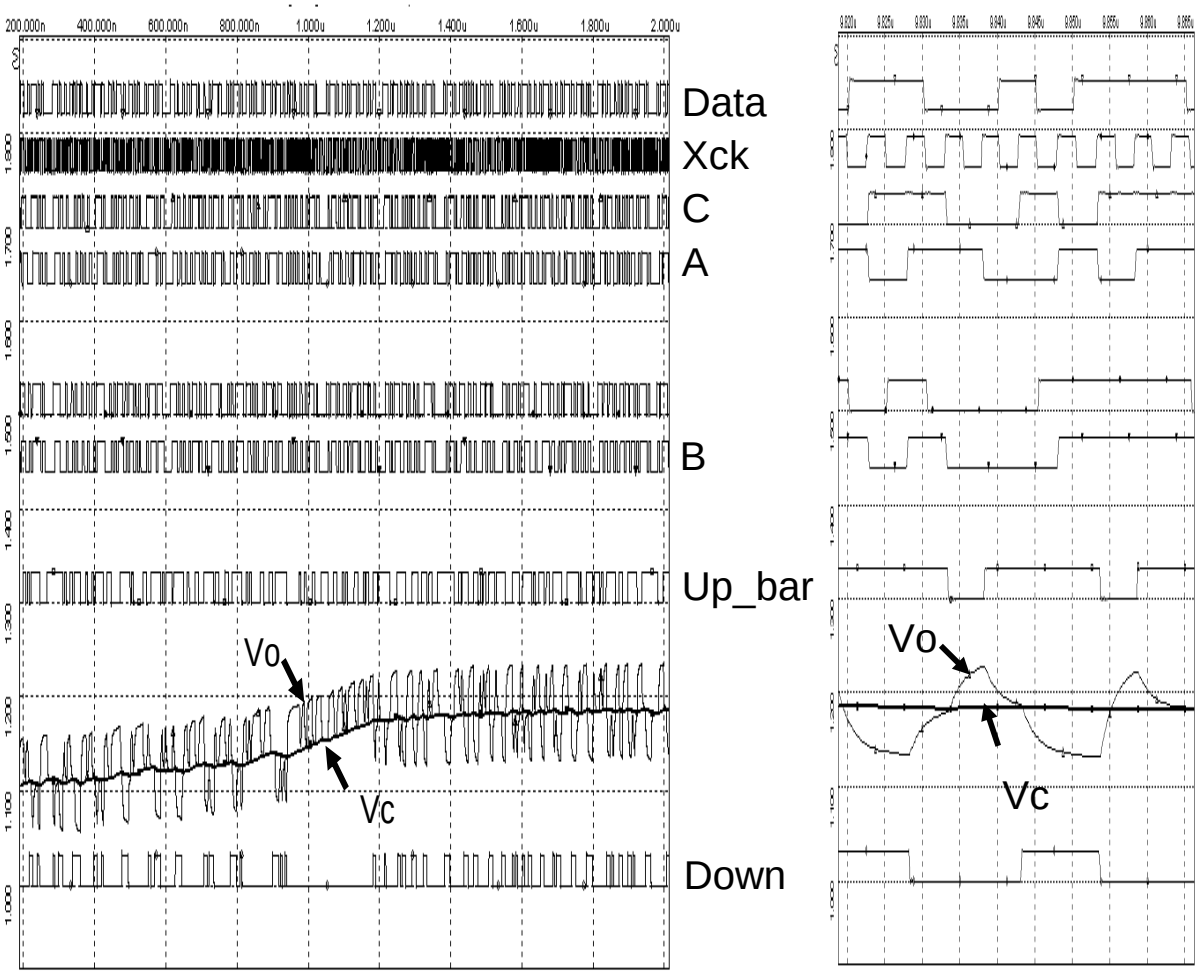



Fig. 2.8 Verilog Simulated Waveforms of Bang Bang Phase Detector




(A) Frequency Capture Stage

(B) Frequency and Phase Matched State

Fig. 2.9 SPICE simulated waveforms of Bang Bang PD
Icp = 50uA, R1 = 1K, C1 = 200pF, C2 = 2pF, 200Mbps

## 2.6 Published papers on CDR for NRZ

In the past, many papers on PD, PFD and CDR for NRZ were published as tabulated in Table 2.1. As seen in Table 1, most of the system uses the Hogge or Quadricorrelator. Among those Triwave is a kind of Hogge, and Dual Edge Trigger is a kind of Quadricorrelator.

Table 2.1 Published Papers

| Year | Author | Institution | Paper | System | Data Differentiation | Phase Detector | Frequency Detector | Bit Rate | Jitter |
|---|---|---|---|---|---|---|---|---|---|
| 1976.09 | C. A. Sharpe | Bendix | EDN Magazine, September 20, 1976 | 3-State | - | 3-State | 3-State | | |
| 1979 | J. A. Afonso et al | Universidae Estadual | National Telecom, Conf. Rec.1979 | Slip Detector | Yes(RZ) | AND, INV+NAND | Rotational | | |
| 1979.06 | J. A. Bellisio | Bell Lab. | IEEE Int. Comm. Rec. vol. 1, June, 1979 | Quadricorrelator | Yes | Multiplyer | Diff. & Quantizer | | |
| 1979.12 | R. Cordell et al | | IEEE J of Solid State Cir. Dec. 1979 | Quadricorrelator | Yes | Gilbert(Temaly) | Gilbert | 50M | |
| 1985.1 | I. Shahariary et al | Hughes Aircraft | IEEE GaAs IC Symp. Dig. Oct. 1985 | 3-State(4 Latches) | - | 3-State(4-Latchs) | 3-State(4-Latchs) | | |
| 1985.12 | C. R. Hogge | Rockwell International | IEEE J. Lightwave Tech. Dec. 1985 | Hogge's Detector | Direct | Hogge's Detector | - | | |
| 1991.1 | H. Ransjin | AT&T Bell Lab | IEEE J of Solid State Cir. Oct. 1991 | Quadricorrelator | Yes | Gilbert | Gilbert | 2.5G | 7 deg rms |
| 1992.12 | S. K. Enam et al | UCLA | IEEE J of Solid State Cir. Dec. 1992 | Data Multiply X2 | No | Double Gilbert | Quadricorrelator | 1.5G | 13ps rms |
| 1992.12 | A. Pottbacker et al | Ruhr-Universitat Bochum | IEEE J. of Solid-State Circuit, Dec. 1992 | Quadricorrelator | No(DualTrig. DFF) | Bang-Bang | Dual Triggerd DFF | 8 Gb/s | 1,9ps(rms) |
| 1992.12 | T. H. Lee et al | Analog Device | IEEE J of Solid-State Circ. Dec. 1992 | Triwave | No | Triwave | No(Vcxo) | 155M | 0.93deg.rms |
| 1993.12 | M. Soyuer | IBM | IEEE J of Solid-State Circ. Dec. 1993 | Dual Edge Trigg. | No | Dual Edge Trigg. | No(VCO Calibration) | 2.3Gb/s | Sigma7.7ps |
| 1994.12 | A. Pottbacker et al | Ruhr-Universitat Bochum | IEEE J of Solid-State Cir. Dec. 1994 | Quadricorrelator | No | Bang-Bang | Gilbert | 8G | 1.6ps rms |
| 1995 | B. Razavi | AT&T Bell Lab | Sympo. on VLSI Circ. Dig. 1995 | Qadricorrelator | Yes | Gilbert | Gilbert | 2.5G | |
| 1996 | L. Devito | Analog Device | IEEE Monolithic PLL & Clock Recovery | Triwave | No | Triwave | Rotational | 155M | 3.5deg.rms |
| 2000.6 | M. T. Hill et al | Curtin U Tech, Australia | IEEE Trans. on Circuits and Systems | Frequency Steered | Yes | Hogge's Detector | Rotational | 155.52M | |
| 2000.9 | Y. M. Greshishchev | Nortel Networks | IEEE J of Solid-State Circuit, Sept. 2000 | | No | Hogge's Detector | No | 10G | SiGe |
| 2001.5 | J. Savoy, B. Razavi | UCLA | IEEE J of Solid-State Circuit, May 2001 | Half Rate | No | Dual Hogge | No | 10G | 0.18u CMOS |

## 2.7Market available CDR for NRZ

There is a very few market available PFD or CDR applicable to NRZ data. As an example, Analog Devices AD807 is shown in Fig. 2.10. As seen in Fig. 2.10, the CDR employs phase detector φdet and frequency detector Fdet. There is no explicit description on data sheet about φdet and Fdet. However Lee, with Analog Devices, published a paper about "Triwave Method" [3] as shown in Fig. 2.11, which is a modification of Hogge PD, and Analog devices has a patent of Triwave Method. Even though the ripple is improved in Triwave from Hogge PD, the pulse width is large. So, the offset occurs.
To compensate the offset, Zero Compensation circuit is required as seen in Fig. 2.7. Therefore the φdet is estimated as Triwave. Fdet is also estimated to be a slip detector.

Table 2.2 shows the data sheet of the AD807. As seen in Table 2.2 a large value of filtering capacitor 0.1uF is used even though triwave method is applied which is intending to decrease the ripple of the out put, resultantly acquisition time is very large $4 \times 10^5$ bit time, i.e. 2.4 ms in 155Mbps.

Frequency capture and tracking range is very small, only 1 MHz in 155.52 Mbps. This means that the frequency range of VCO should be maintained inside of the lock-in rage. Therefore, Laser trimming of resistor etc. might be needed.

In other point of view, regarding RC series circuit of the charge pump filter, voltage drop on R is sometimes described as a phase detector, and integrated voltage on C as a frequency detector. In this sense, there is no specific frequency detector, and the frequency capture range is very narrow such as 1MHz at 155Mbps.

The final target of the research work of the author is intending to exceed these specifications.

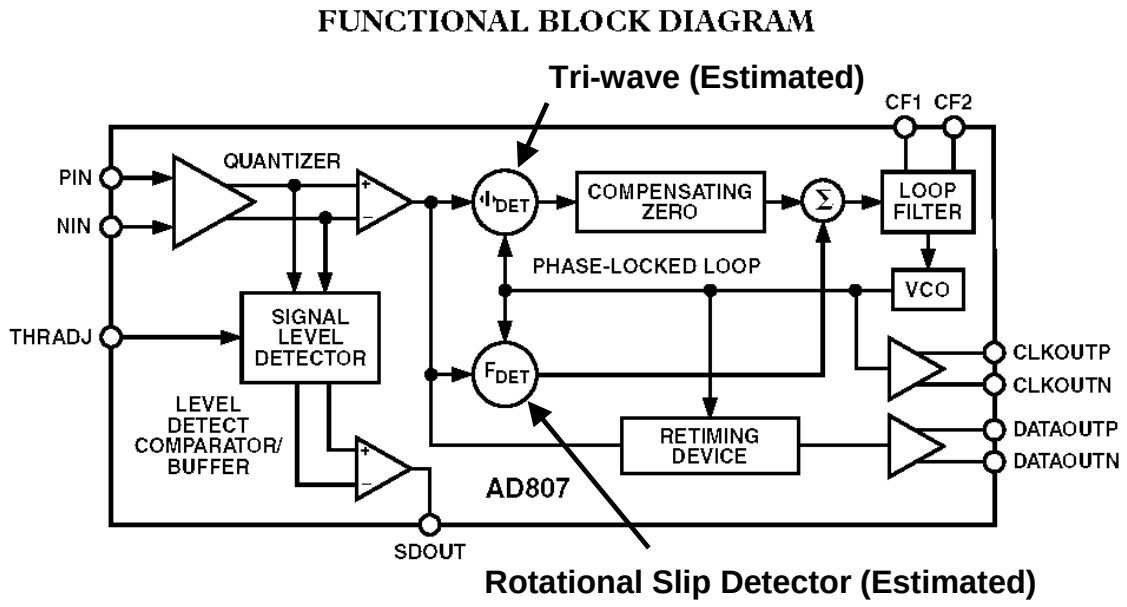



Fig. 2.10 An example of market available CDR, Analog Devices AD807

## Triwave Phase Detector

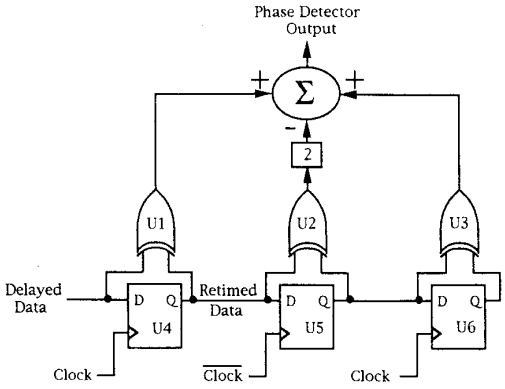



Fig. 15. Triwave phase detector.

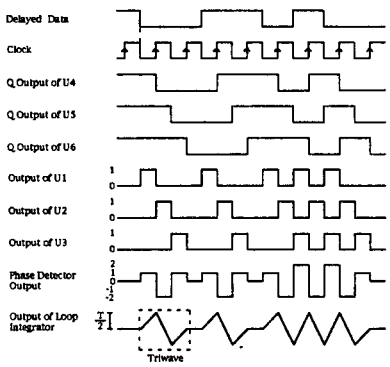



Fig. 16. Waveforms of triwave detector with clock and data aligned.

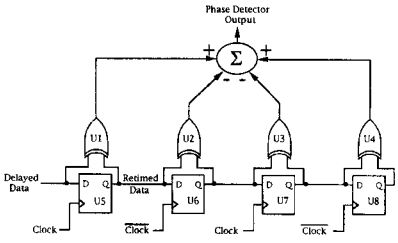



Fig. 17. Modified triwave phase detector.

Fig. 2.11 Triwave PD

"A 155-MHz Clock Recovery Delay- and Phase-Locked Loop"
T. H. Lee, J. F. Bulzacchelli, IEEE J. of Solid-State Circuits, vol. SC-27, pp. 1736-1746, December 1992
Lee was with Analog Devices, Bulzacchelli is with M.I.T.

Table 2.2 Specification of AD807

## AD807–SPECIFICATIONS ($T_A = T_{MIN}$ to $T_{MAX}$, $V_{CC} = V_{MIN}$ to $V_{MAX}$, $C_D = 0.1\ \mu F$, unless otherwise noted.)

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| QUANTIZER–DC CHARACTERISTICS | | | | | |
| Input Voltage Range | @ $P_{IN}$ or $N_{IN}$ | 2.5 | | $V_{CC}$ | V |
| Input Sensitivity, $V_{SENSE}$ | $P_{IN}$–$N_{IN}$, Figure 1, BER = ≤ $1 \times 10^{-10}$ | 2 | | | mV |
| Input Overdrive, $V_{OD}$ | Figure 1, BER = ≤ $1 \times 10^{-10}$ | 0.001 | | 2.5 | V |
| Input Offset Voltage | | | 50 | 500 | µV |
| Input Current | | | 5 | 10 | µA |
| Input RMS Noise | BER = ≤ $1 \times 10^{-10}$ | | 50 | | µV |
| Input Peak-to-Peak Noise | BER = ≤ $1 \times 10^{-10}$ | | 650 | | µV |
| QUANTIZER–AC CHARACTERISTICS | | | | | |
| Upper –3 dB Bandwidth | | | 180 | | MHz |
| Input Resistance | | | 1 | | MΩ |
| Input Capacitance | | | 2 | | pF |
| Pulsewidth Distortion | | | 100 | | ps |
| LEVEL DETECT | | | | | |
| Level Detect Range | $R_{THRESH}$ = INFINITE | 0.8 | 2 | 4.0 | mV |
| | $R_{THRESH}$ = 49.9 kΩ | 4 | 5 | 7.4 | mV |
| | $R_{THRESH}$ = 3.4 kΩ | 14 | 20 | 25 | mV |
| Response Time | DC-Coupled | 0.1 | | 1.5 | µs |
| Hysteresis (Electrical) | $R_{THRESH}$ = INFINITE | 2.3 | 4.0 | 10.0 | dB |
| | $R_{THRESH}$ = 49.9 kΩ | 3.0 | 5.0 | 9.0 | dB |
| | $R_{THRESH}$ = 3.4 kΩ | 3.0 | 7.0 | 10.0 | dB |
| SDOUT Output Logic High | Load = +4 mA | 3.6 | | | V |
| SDOUT Output Logic Low | Load = –1.2 mA | | | 0.4 | V |
| PHASE-LOCKED LOOP NOMINAL CENTER FREQUENCY | | | 155.52 | | MHz |
| CAPTURE RANGE | | 155 | | 156 | MHz |
| TRACKING RANGE | | 155 | | 156 | MHz |
| STATIC PHASE ERROR | $2^7$–1 PRN Sequence | | 4 | 20 | Degrees |
| SETUP TIME ($t_{SU}$) | Figure 2 | 3.0 | 3.2 | 3.5 | ns |
| HOLD TIME ($t_H$) | Figure 2 | 3.0 | 3.1 | 3.3 | ns |
| PHASE DRIFT | 240 Bits, No Transitions | | | 40 | Degrees |
| JITTER | $2^7$–1 PRN Sequence | | 2.0 | | Degrees RMS |
| | $2^{23}$–1 PRN Sequence | | 2.0 | 2.7 | Degrees RMS |
| JITTER TOLERANCE | f = 10 Hz | | 3000 | | Unit Intervals |
| | f = 6.5 kHz | 4.5 | 7.6 | | Unit Intervals |
| | f = 65 kHz | 0.45 | 1.0 | | Unit Intervals |
| | f = 1.3 MHz | 0.45 | 0.67 | | Unit Intervals |
| JITTER TRANSFER | | | | | |
| Peaking (Figure 11) | $C_D$ = 0.15 µF | | 0.08 | | dB |
| | $C_D$ = 0.33 µF | | 0.04 | | dB |
| Bandwidth | | 65 | 92 | 130 | kHz |
| Acquisition Time | | | | | |
| $C_D$ = 0.1 µF | $2^{23}$–1 PRN Sequence, $T_A$ = 25°C | | $4 \times 10^5$ | $2 \times 10^6$ | Bit Periods |
| $C_D$ = 0.33 µF | $V_{CC}$ = 5 V, $V_{EE}$ = GND | | $2 \times 10^5$ | | Bit Periods |
| POWER SUPPLY VOLTAGE | $V_{MIN}$ to $V_{MAX}$ | 4.5 | | 5.5 | Volts |
| POWER SUPPLY CURRENT | $V_{CC}$ = 5.0 V, $V_{EE}$ = GND, $T_A$ = 25°C | 25 | 34.5 | 39.5 | mA |
| PECL OUTPUT VOLTAGE LEVELS | | | | | |
| Output Logic High, $V_{OH}$ | $V_{CC}$ = 5.0 V, $V_{EE}$ = GND, $T_A$ = 25°C | –1.2 | –1.0 | –0.7 | Volts |
| Output Logic Low, $V_{OL}$ | Referenced to $V_{CC}$ | –2.0 | –1.8 | –1.7 | Volts |
| SYMMETRY (Duty Cycle) | ρ = 1/2, $T_A$ = 25°C, | | | | |
| Recovered Clock Output, Pin 5 | $V_{CC}$ = 5 V, $V_{EE}$ = GND | 50.1 | | 54.1 | % |
| OUTPUT RISE / FALL TIMES | | | | | |
| Rise Time ($t_R$) | 20%–80% | | 1.1 | 1.5 | ns |
| Fall Time ($t_F$) | 80%–20% | | 1.1 | 1.5 | ns |

Specifications subject to change without notice.

## 2.8 Conclusion in Conventional PFD or CDR

Conventional PFD or CDR is summarized as follows,

1) Hogge PD is able to connect directly to NRZ data, however it does not have the function of frequency detector. Therefore the frequency acquisition aid such as slip detector is required.

2) Hogge PD has large ripple in its output. This has been improved by triwave method, however still large value of capacitor is required for the low pass filter, and resultantly acquisition time or lock-in time becomes very large.

3) Frequency capture range of quadricorrelator or slip detector is +/- 50 % of local VCO clock. Because these circuit uses $\pi/2$ shifted signal of VCO.

4) Quadricorrelator and slip detector are both required the differentiator to convert NRZ data to RZ data.

5) Bang Bang PD, binary PD, is widely used in high Gbps application. However it lacks in frequency detection. To reduce the jitter, large filter constants, and inherently large lock-in time is unavoidable.

Requirements for idealistic PFD are concluded as follows;

- Data differentiation is mandatory for Frequency Detector function

  NRZ data does not have explicit clock frequency information which is used for generation of NRZ data itself. To realize the frequency detector function, first of all, an extraction of frequency component of original clock by differentiation of data is required. For the differentiation, a combination of delay element and exclusive OR is effective.

- Linear PD is better than Bang Bang (binary) PD for control-ability

  According to the control theory, more precise and predictable control can be done in linear PD than binary PD.

# Chapter 3

# New 4-State PFD

## 3.1 Summary

To realize a linear PFD having a capability of frequency detector even in NRZ data, the analysis about traditional 3-state PFD was made in the point of view, why it has been abandoned in NRZ world in spite of such outstanding features in continuous pulses. In application on continuous pulses such as frequency synthesizer, usage of 3-state PFD may be more than 95%.

The analysis was made comparing with pre- and post-processing to eliminate the error pulses which are generated if it is used on NRZ data. Then it was found that the post processing is effective in keeping the function of frequency detector.

To augment the application from continuous pulse area to NRZ world, a 4th state, “Missing Transition State” and its register was introduced. The facts are verified by Verilog simulation and FPGA test.

Next will be explained the behavior of 3-State PFD first, then its new augmentation to 4-State PFD and verification on FPGA.

## 3.2 Conventional 3-State PFD under NRZ data

In continuous pulse area such as a frequency synthesizer, 3-state PFD is widely used due to its outstanding features having the function of frequency detector and large figure of merit in phase detector, which means that the output is linear to the phase difference, and very low at phase locked state and resultantly it has low jitter characteristics.

However, this PFD cannot be used for coded data streams with missing transitions under NRZ data because it falsely generates error pulses.

Due to this reason, 3-state PFD has been abandoned long time in NRZ world. However, if the countermeasure to coupe with this false pulse generation be successful, an idealistic PFD for NRZ would be realized.

Author’s research purpose lies in this point.

Fig. 3.1 shows the 3-State PFD, strictly speaking the circuit in Fig. 3.1 is a 3-State PFD with data differentiation circuit.

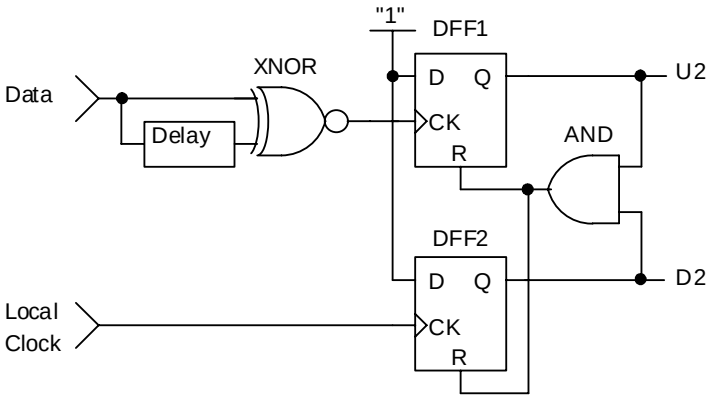



Fig. 3.1 3-State PFD + Differentiation Circuit

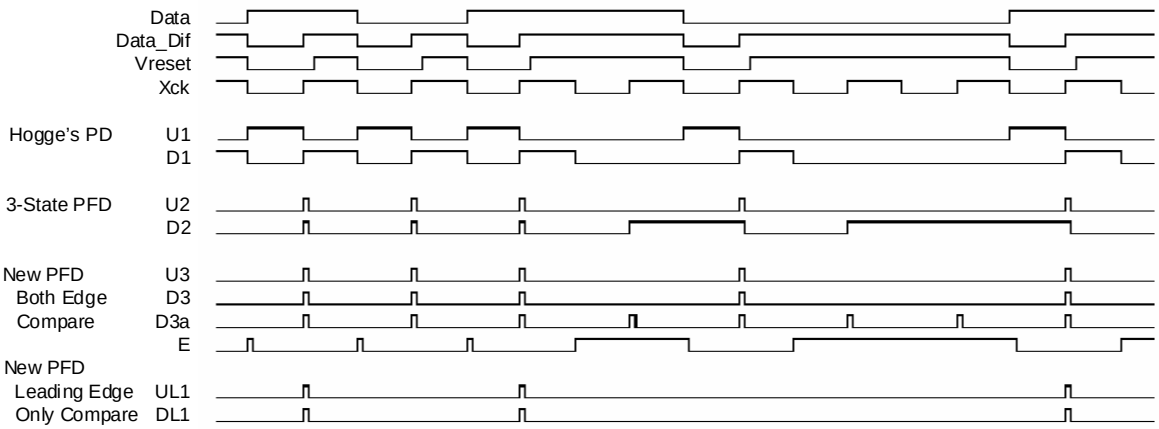



Fig. 3.2 3-State PFD generates false pulse in D2
At missing data transition
Phase and frequency matched state,
Delay1 = 0.5Tb, Delay2 = 0.2Tb

The data differentiation circuit is mandatory required to extract original clock frequency component from NRZ data. Fig. 3.2 shows the Verilog simulated waveforms. As seen “3-State D2” in Fig. 3.2, error pulses are generated at missing data transition. Therefore, this PFD can not be used on NRZ data.

## 3.3 New Augmentation of 3-State PFD to 4-State PFD

In order to eliminate the error pulses in 3-State PFD under NRZ data, Llewellyn, National Semiconductor, invented a combination of Hogge PD and 3-State PFD as a pre-processing by Hogge PD in front of 3-State PFD [8]. The error pulses are eliminated successfully, however the function of frequency detector is lost. The reason of failure lies in pre-processing.

The newly proposed PFD is a modification of 3-state PFD to eliminate error pulses arising from missing data transitions without losing the function of frequency detection. To this end, a post-processing method is applied.

Results of analysis are summarized as follows.

1) In NRZ data streams, a missing data transition cannot be predicted with a single bit time. It can only be recognized by comparing a pair of symbols, current and 1bit previous timing, to detect a transition. Therefore, a form of 1-bit memory such as a delay line memory is required.

2) A NRZ data stream lacks explicit frequency information of the transmitter original bit rate clock. To extract the original clock frequency component from the NRZ data, a differentiation is required. A differentiation by a delay element and exclusive-OR is effective for differentiation of the incoming signal to determine the presence of a data transition.

3) As a whole, effective use of data delay for both of data differentiation and detection of missing transition should be a solution to extract both of bit rate frequency and missing data transitions.

Fig. 3.3 shows the block diagram of new phase frequency detector.

In Fig. 3.3, Delay1, Differentiator1 and 3-State PFD consist the traditional 3-State PFD plus differentiator. Delay2, Differentiator2, INVA and “Missing Transition State” Detector consist the missing transition detector. When missing transitions are detected, 3-State PFD is reset via Post Processing Circuit at the timing of next rise up of local clock Xck, and simultaneously the error

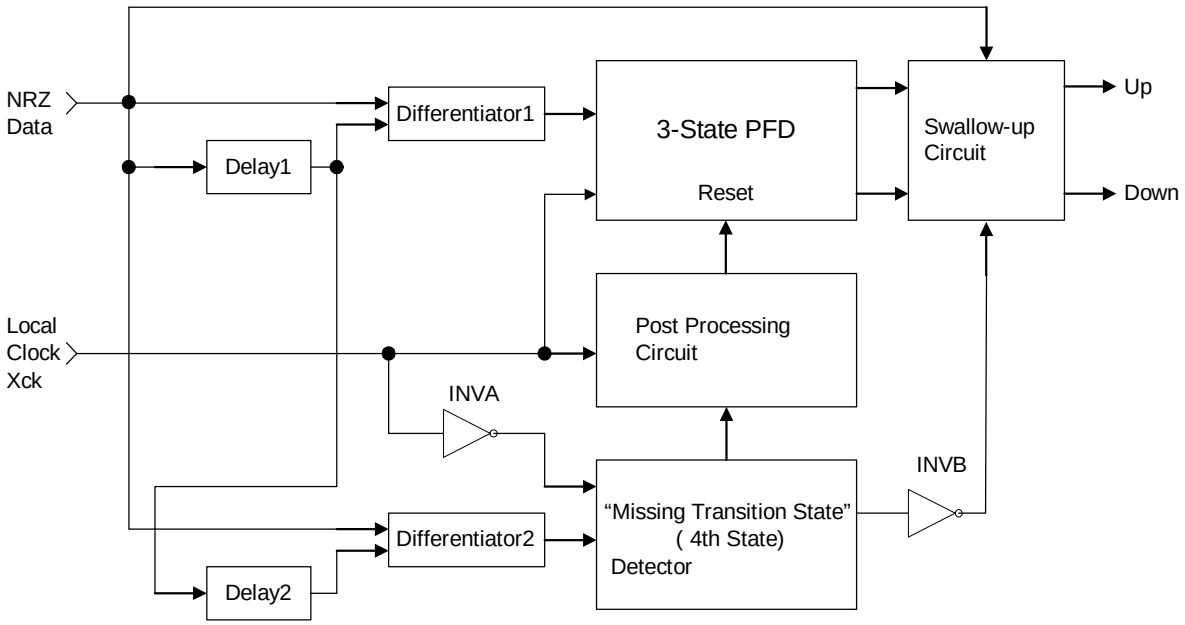



Fig. 3.3 Block diagram of New Phase Frequency Detector

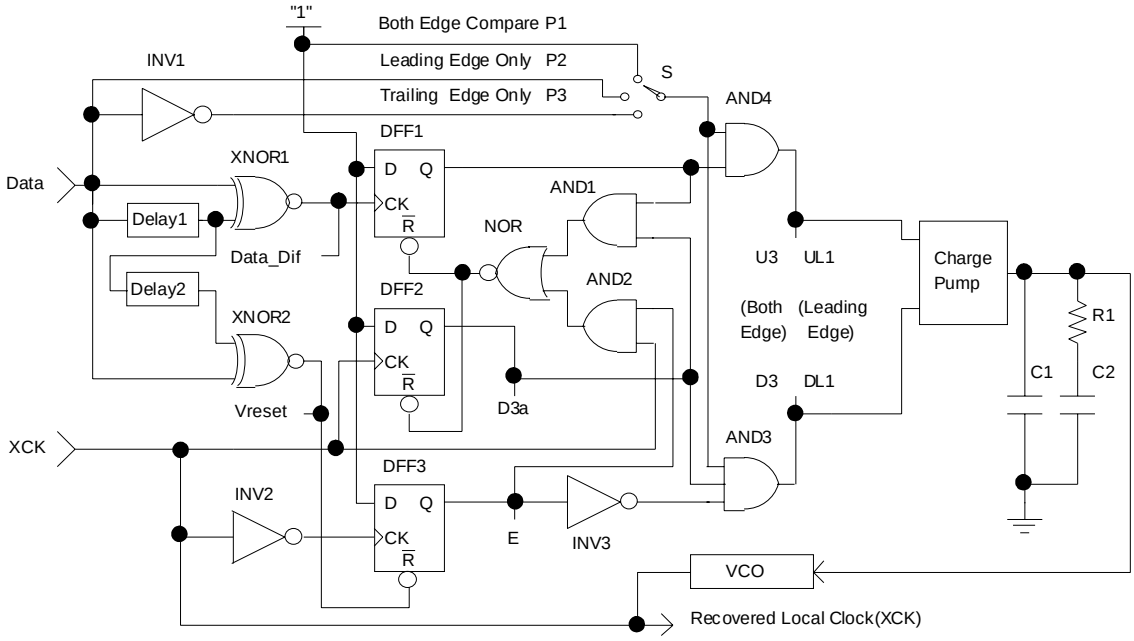



Fig. 3.4 Circuit of New Phase Frequency Detector( PFD )

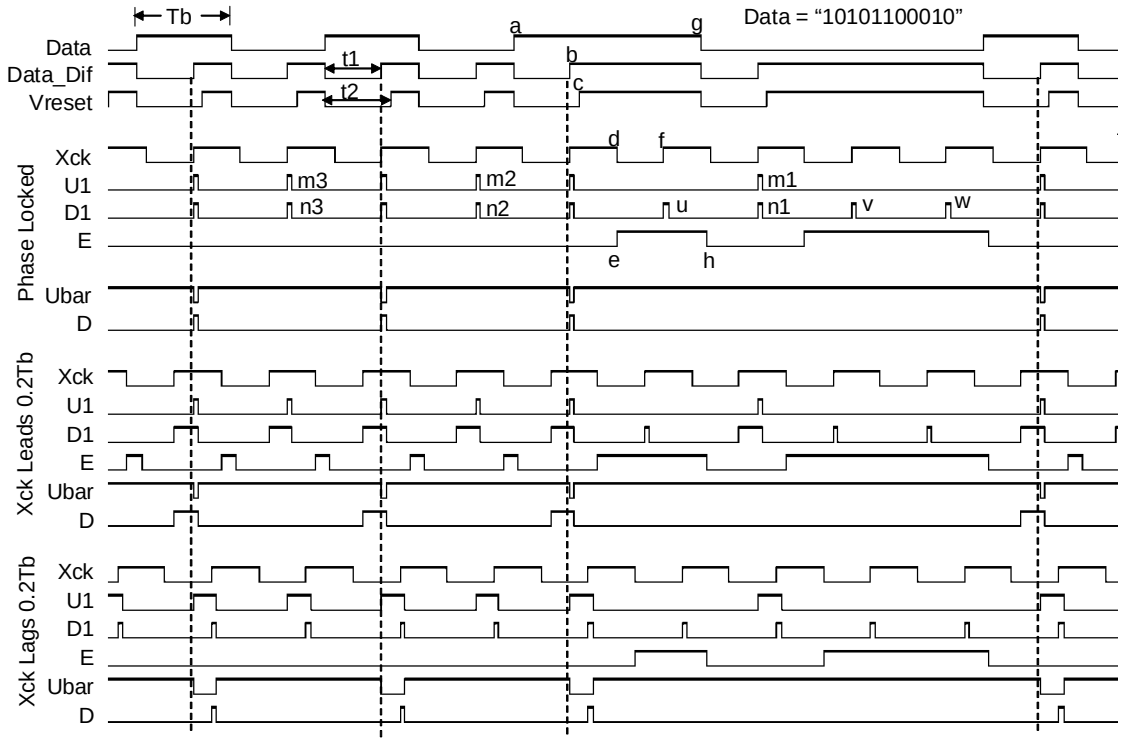



Fig. 3.5 Simulated waveforms, Xck Phase locked, lead and lag

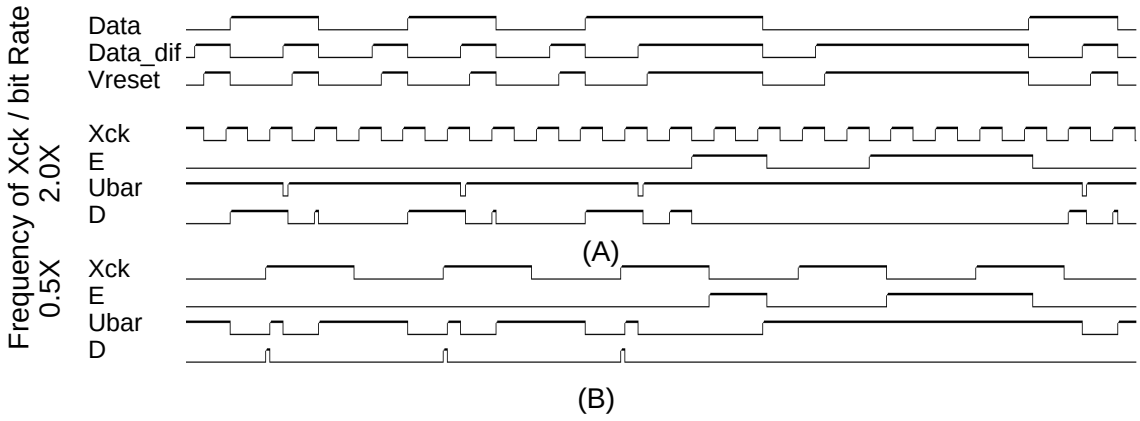



Fig. 3.6 Waveforms of PFD, t1 = 0.6Tb, Function of frequency detector, (A) Frequency of Xck is twice (2.0X), (B) a half (0.5X) of data bit rate

pulses out of the PFD are eliminated by INVB and Swallow-up Circuit since the pulses do not correctly capture the phase difference.

The operation of the PFD will be explained using the detailed circuit schematic shown in Fig. 3.4 and Verilog simulated waveforms illustrated in Fig. 3.5 for a "10101100010" data pattern. Following explanation will be done at the position P2 on switch S. Function of the switch S will be explained later.

As seen in Fig. 3.4, the PFD consists of 3 delayed flip-flops (DFF), DFF1, DFF2 and DFF3, and all data inputs are connected to Vdd, corresponding to the logical “1" high level. A differentiated data pulse Data_dif is connected to the clock input of DFF1 and the local clock Xck is connected to the clock input of DFF2.

XNOR1 generates rising transitions of delayed pulse by Delay1(t1) after Data has changed with respect to the previous data symbol. The Delay1 is designed so that t1 is less than a bit period, i.e. t1 = 0.5~0.6Tb. Tb is a interval time of 1 bit of data. Thus, differentiated pulse Data_dif can be attained by XNOR1.

Upon arrival of rising edges of Data_dif and Xck, the outputs of DFF1 and DFF2 transition high, respectively. When both outputs have transitioned high, a logical AND via AND1 resets the DFFs and they are ready for the next set of rising edges. Thus, DFF1, DFF2, and AND1 function as a traditional 3-State PFD.

As shown in the upper phase-locked waveforms of Fig. 3.5, at point b, Data_dif goes high coincident with the leading edge of Xck. Moreover, the PFD produces short up and down pulses to avoid dead band issues [11]. These minimum pulse widths are determined by the delay through DFF1, DFF2, AND1 and NOR1. When there are missing data transitions, error pulses are generated at the output of DFF2 even though the clock and data may be in lock.

To eliminate these error pulses, an extra register, DFF3, and another differentiation circuit of Delay2 and XNOR2, which generate differentiated pulse of Vreset. Delay time of Vreset, t2, is the sum of delay time of Delay1 and Delay2, i.e. t2 = 0.6~0.7Tb.

DFF3 is introduced which stores information corresponding to the 4th "Missing Data Transition State." DFF3 is triggered at the trailing edge of Xck and reset while Vreset is low, identified as t2 in Fig. 3.5. t2 is designed to be longer than the delay time t1 of Data_dif.

Thus, DFF3 takes comparing action after time of t2 + half of period of local clock Xck. The time interval is 0.6 ~0.7Tb + 0.5Tb = 1.1Tb~1.2Tb at frequency locked state, which means more than 1 bit delay. Therefore, DFF3 can compare the present bit status with previous bit data symbol.

In Fig. 3.5, time points labeled from “a” through “g” illustrate the operation of the PFD in the absence of a data transition. DFF3 is reset during “a”-“c” due the data transition at “a”, but does not reset again until the next data transition at “g”. Hence, on the falling edge of Xck, the output of DFF3 (E) goes high, signifying a missing data transition state. E is used to swallow the error pulse out of DFF2 and prevent it from propagating to the charge pump. Furthermore, the high state of E causes both DFF1 and DFF2 to reset through AND2 on the subsequent rising edge of Xck and prepare them for the next set of edges.

In some applications, the delay times of leading and trailing edges of data may not be the same due to the characteristics of amplifiers or buffers included in the transmitter and receiver of the transceiver system. Therefore, phase detection on both rising and falling data edges can lead to higher jitter, and this jitter is data pattern dependent. So, single edge comparison is sometimes preferable. As a result, in order to make leading edge only comparison, pulses corresponding to trailing edge comparison, m1~m3, n1~n3 are also eliminated when Data is low. This function is done by Switch S in Fig. 3.4. If the position of S is P1, m1~m3 and n1~n3 are utilized, then PFD becomes both edge comparison. Likewise, if the switch S is in position P3, PFD becomes trailing only comparison. Fig. 3.2 also shows the both edge comparison and leading edge only comparison of the new PFD in relation to the false pulse generation on traditional 3-State PFD.

Fig. 3.5 also presents waveforms when Xck leads and lags the data. The waveforms show that the appropriate up and down pulses are generated for the charge pump to lock the loop. The middle waveforms in Fig. 3.5 shows the case that Xck leads in phase 0.2Tb from the data. Down pulses are generated on D1. The lower Wave forms in Fig. 3.5 shows the case that the Xck lags 0.2Tb from the data. The up plses are generated on U1.

Fig. 3.6 (A) presents the case of the frequency of Xck is twice (2.0X) of the original clock frequency of incoming data, and Fig. 3.6 (B) presents the case of half (0.5X) in frequency. As seen in Fig. 3.6 (A) down pulses in D are generated in higher frequency of Xck, and in Fig. 3.6 (B) up pulses are generated on Ubar (low level) in lower frequency of Xck. Thus, the proposed PFD has the function of the frequency detector.

As seen in Fig. 3.5, the output pulses of new PFD are very narrow at phase-matched state. This feature leads to another advantage. Even if there is some difference between charging and discharging currents, output becomes very small. It is because charging and discharging intervals are very small and their occurrence is the same time. Therefore, at phase matched state, very low

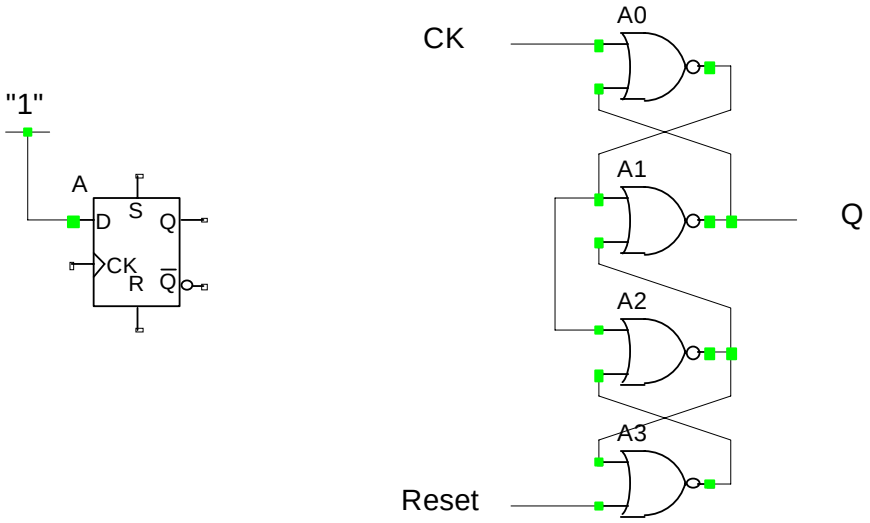



Fig. 3.7 Hidden “1” DFF
I. Shahanary etal IEEE GaAs IC Symp. Dig. October, 1985 [11]

ripple in output of charge pump (Vout) occurs as shown in Fig. 2.2b. This narrow pulse, which is generated by gate delay plus reset delay of DFF, is necessary for avoiding a non-linearity in phase difference output near phase matched state [11]. This scheme is very effective to maintain the low jitter. Moreover, T in equation (2.2) is very small. Therefore, the current difference between charging and discharging is not sensitive to the phase offset.

Since the data inputs of all of the DFFs are connected to a logical "1", a "Hidden 1" DFF [10, 11] can be used which offers advantages of simplicity and high speed operation. Fig. 3.7 shows Hidden 1 DFF.

Thus, clear and very narrow pulses, which are caused by the gate delay and the reset delay of DFF, only occur on U3 and D3 simultaneously at phase matched state. This new, effectively 4-state PFD, successfully extends the application of a traditional 3-state PFD to NRZ data. It inherits the desirable features of a 3-state PFD such as frequency detection and low jitter.

## 3.4 Verification on FPGA

The operation of new PFD was verified using FPGA and market available VCO. Test circuit is shown in Fig. 3.8. Verilog-verified circuit was written into FPGA of Altera EPF10K50VRC240-3, and VCO portion of TI TLC29321 was used as VCO. The charge pump circuit was made by discrete bipolar transistor, fT=2.4GHz, using a constant current switching as a differential charge pump circuit. It was confirmed that PFD written into FPGA works up to 40MHz, and VCO works the frequency range of 10 to 35MHz. Delay was taken by inverter delay, and delay time was adjusted by the serial resistor between the inverters. The test was made on data pattern of maximum density, a repetition of 1010…, and $2^7$ pseudorandom data, strictly speaking $2^7 - 1$ pseudorandom, at a bit clock rate of 20MHz( = 20Mbps).

Table 3.1 summarizes the frequency acquisition characteristics using the delay time as a parameter. In the table, Tb shows the interval time of one bit, 50ns at bit clock fb = 20MHz in this case, and “OK” means that there was no false lock. In case of new PFD, false lock was not observed in wide range of 0.4Tb to 0.7Tb in Delay1 if (Delay1 + Delay2) was maintained at 0.7Tb. This is very useful for practical applications where large margin should be required in fluctuation of delay time caused by wafer-fabrication process or operating conditions such as temperature or supply voltage. Without using Delay2 and XNOR2, the reset of DFF3 Rbar may be connected to the output of XNOR1[9].

In this case Delay1 should be 0.6Tb. However, the addition of Delay2 and XNOR2 contributes to extend the margin of the delay wider.

Fig. 3.9a to 3.9d show the frequency lock-in curve at Delay1 = 0.5Tb and Delay2 = 0.2Tb, low frequency 10MHz (-50%) to target frequency and high frequency 34MHz (+70%) to target frequency, under a data pattern of $2^7 - 1$ pseudorandom.

As shown in figures, in case of both edge compare, lock-in time is 100us, and in case of leading edge only comparing, the lock in time is 150us in pseudorandom data. The lock-in time can be decreased by decreasing the value of C1, C2 and increasing the value of R1. As shown in Fig. 3.9a to Fig. 3.9d the capture range on VCO frequency is proved to be –50 to +70% of target frequency by FPGA test. Other SPICE simulation showed that the capture range on VCO frequency is 1/10 to 10 times of target frequency, that is, there is theoretically no limitation in capture range so long as the logic works on that frequency. This feature is the same as 3-state PFD in continuous pulses.

As for capture range on input data bit rate, the new PFD has certain limitation due to the delay elements, Delay1 and Delay2. However, it was proved that the variation in input data bit rate of +15% and -20% is allowable at Delay1=0.6Tb, Delay2=0.1Tb, and in case of Leading Edge Only Compare. This means that input variation in data bit rate of 16Mbps to 23Mbps is allowable at designated bit rate of 20Mbps. This might be enough for most of the fixed bit rate applications.

Jitter characteristics were also measured, and results are tabulated in Table 3.2. Fig. 3.10a shows the jitter characteristics of Hogge's PD. Due to the lack of frequency acquisition this data was taken after manual lock-in. As assumed, the very large jitter of peak to peak 460ps was measured. Fig. 3.10b shows the New PFD both edges comparing on pseudorandom data pattern, and peak to peak jitter of 370ps was measured. Fig. 3.10c shows the jitter of leading edge only comparing type, and jitter of 350ps was measured. In practical application leading edge only comparing type is very useful to acquire the low jitter characteristics. The jitter of pattern generator itself was 240ps, and the jitter of VCO at DC input without PFD was 320ps. To decrease the jitter smaller, additional measures should be taken so as to decrease the jitter of VCO itself. The new PFD is described here in using conventional 3 DFFs.

However, all data input of DFFs are connected to logical "1". So simplified, hidden "1" DFFs can be applied [10]. This is another advantage of this PFD.

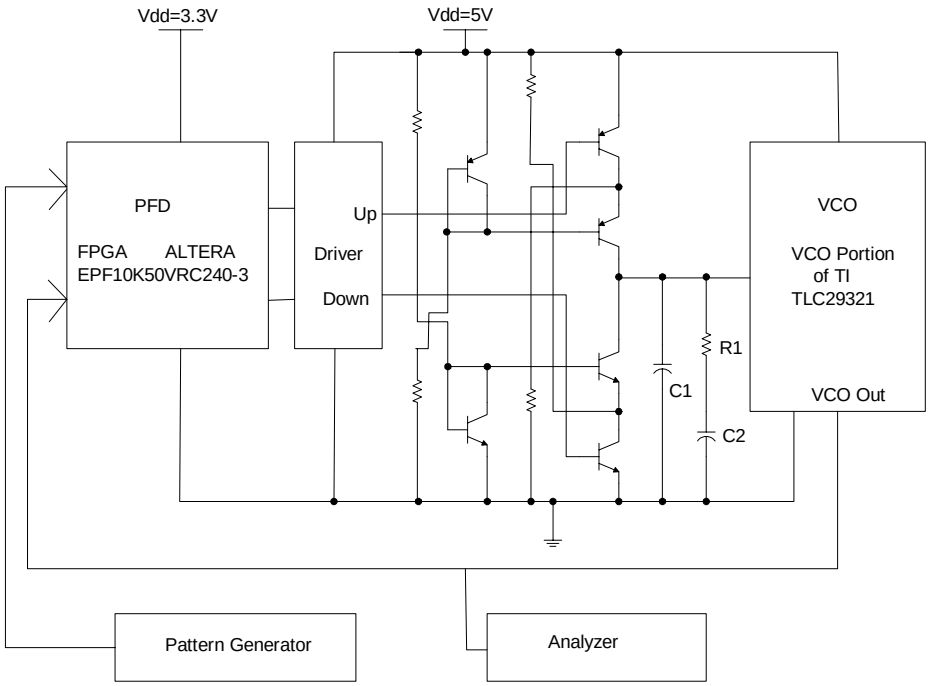



Fig. 3.8 Test circuit of PFD using FPGA

Table 3.1 Frequency Acquisition Characteristics
(Target Frequency = 20MHz)

| Lock-in Direction | | | Low(10MHz) up to Target(20MHz) | | High(34MHz) down to Target(20MHz) | |
|---|---|---|---|---|---|---|
| Data Pattern | Delay1 | Delay2 | Max. Density | $2^7$ Pseudorandom | Max. Density | $2^7$ Pseudorandom |
| New PFD | 0.4Tb | 0.3Tb | OK(6us) | OK(100us) | OK(6us) | OK(150us) |
| Both Edge | 0.5Tb | 0.2Tb | OK(6us) | OK(100us) | OK(6us) | OK(150us) |
| Compare | 0.6Tb | 0.1Tb | OK(6us) | OK(100us) | OK(6us) | OK(150us) |
| | 0.7Tb | 0.0Tb | OK(6us) | OK(150us) | OK(6us) | OK(150us) |
| New PFD | 0.4Tb | 0.3Tb | OK(14us) | OK(100us) | OK(14us) | OK(150us) |
| Leading Edge | 0.5Tb | 0.2Tb | OK(14us) | OK(100us) | OK(14us) | OK(150us) |
| Only Compare | 0.6Tb | 0.1Tb | OK(14us) | OK(150us) | OK(14us) | OK(150us) |
| | 0.7Tb | 0.0Tb | OK(14us) | OK(150us) | OK(14us) | OK(150us) |

Tb (Interval Time of 1bit) = 50ns, OK: Normal Lock(Lock-in Time)
Icharge = 1.5mA, R1 = 470Ω, C1 = 470pF, C2 = 0.047uF

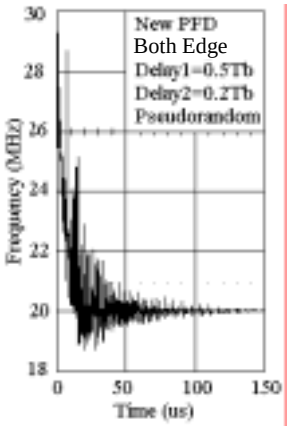



Fig. 3.9a
Downward lock-in
Both Edge
Compare

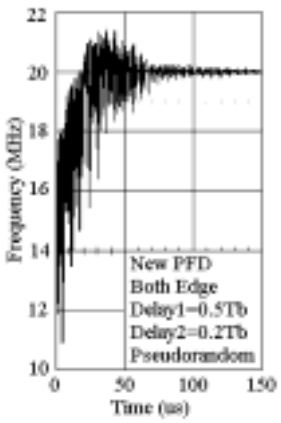



Fig. 3.9b
Upward lock-in
Both Edge
Compare

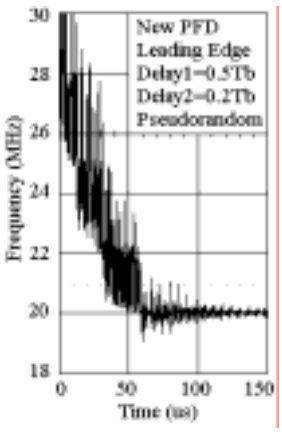



Fig. 3.9c
Downward lock-in
Leading Edge only
Compare

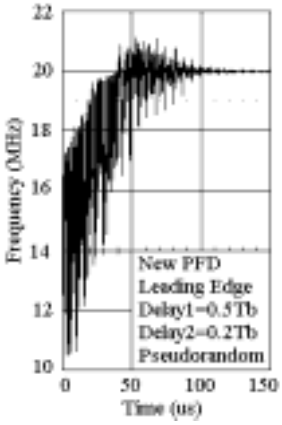



Fig. 3.9d
Upward lock-in
Leading Edge only
Compare

Table 3.2 Jitter Characteristics(Target Freqency = 20MHz, $2^7-1$ Pseudorandom Data)

| | Charge/Discharge Current(mA) | Delay1 | Delay2 | C1(pF) | R1(ohm) | C2(uF) | Peak to Peak Jitter(ps) |
|---|---|---|---|---|---|---|---|
| Hogge's PD | 0.5 | -- | -- | 470 | 470 | 0.1 | 460 |
| New PFD(Both Edge Compare) | 1.5 | 0.5Tb | 0.2Tb | 470 | 470 | 0.047 | 360 |
| New PFD(Leading Edge Only Compare) | 1.5 | 0.5Tb | 0.2Tb | 470 | 470 | 0.047 | 350 |
| Pattern Generator | Pattern Generator itself, Maximum Density Data | | | | | | 240 |
| VCO | VCO itself, at 20MHz | | | | | | 320 |

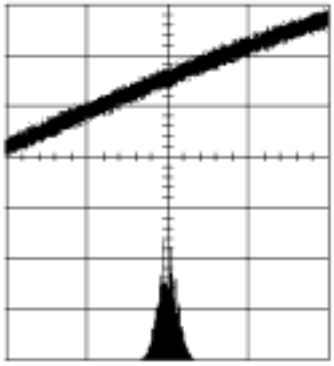


Fig. 3.10a Hogge's PD

Jitter = 460ps PP

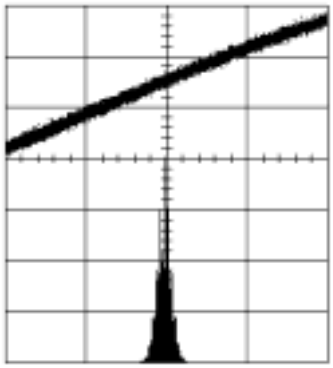


Fig. 3.10b New PFD
Both Edge Compare
Jitter = 370ps PP

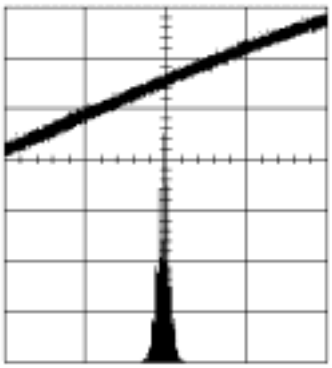


Fig. 3.10c New PFD
Leading Edge Only Compare
Jitter = 350ps PP

$2^7 - 1$ Pseudorandom NRZ Data, 20Mbps

## 3.5 Features of New PFD

The features of new PFD is summarized as follows;

1) Having function of frequency detector on NRZ data
2) Wide frequency capture Range
3) Large figure of merit – low output at phase locked state
4) Using only 3 DFFs
5) Hidden "1" DFF can be usable

# Chapter 4

# Circuit Block and Components

## 4.1 Summary

The delay element takes very important role in data delay and Current Controlled Oscillator (CCO). The linearity of oscillating frequency vs. control current or voltage is very important as well as its range of oscillating frequency.

To acquire the CCO with wide frequency range and good linearity in control a research work was made in analyzing the conventional delay element.

A new delay element utilizing relaxation delay scheme has been developed.

For wide bit rate application as a Clock and Data Recovery (CDR), charge pump control is necessary for stable operation.

Analysis on conventional delay element, new delay element, dimension improved charge pump circuit and charge pump current control are explained next.

## 4.2 Delay Element

### 4.2.1 Conventional Delay Element

Delay unit takes a very important role in this PLL. Differential amplifier type delay unit as shown in Fig. 4.1 has been widely used due to its robustness in common mode noise incurred by power supply line or ground or substrate noises, as well as applicability to higher frequency area.

As seen in Fig. 4.1, drains of differential pair M1 and M2 are connected to load MOS M3 and M4, and sources are commonly connected to current source I, and this current source is controlled by outside control voltage or current.

However, in low supply voltage application under 3.3V, the linearity of voltage or current to delay time or oscillation frequency is not so good, because the load MOS is saturated in high control current area because of narrow head space.

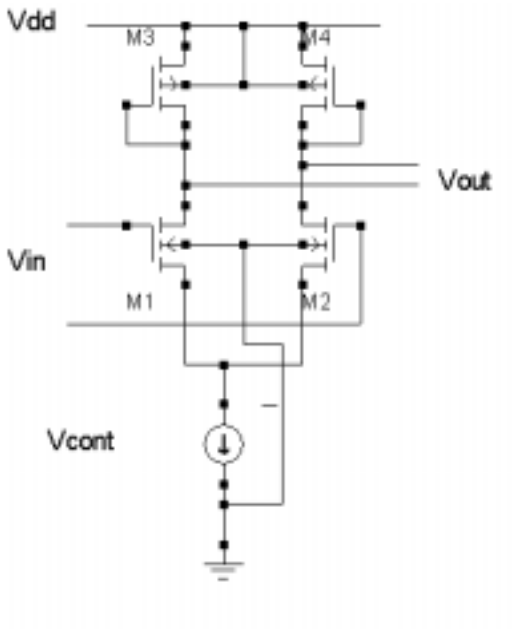



Fig. 4.1 Differential Amplifier Type Delay Element

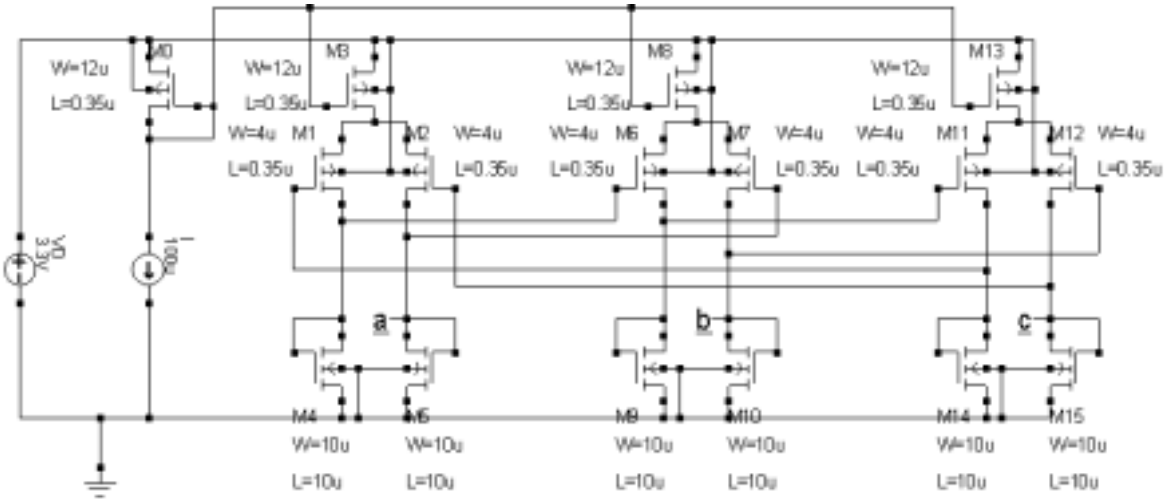



Fig. 4.2 3-Stage Current Controlled Oscillator for SPICE Simulation

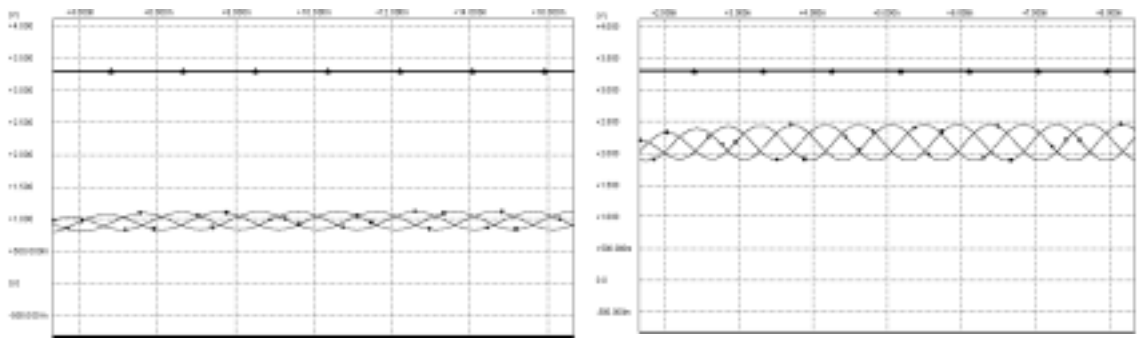


Fig. 4.3a Vdd = 3.3V, I = 20uA
fosc = 333MHz

Fig. 4.3b Vdd = 3.3V, I = 200uA
fosc = 809MHz

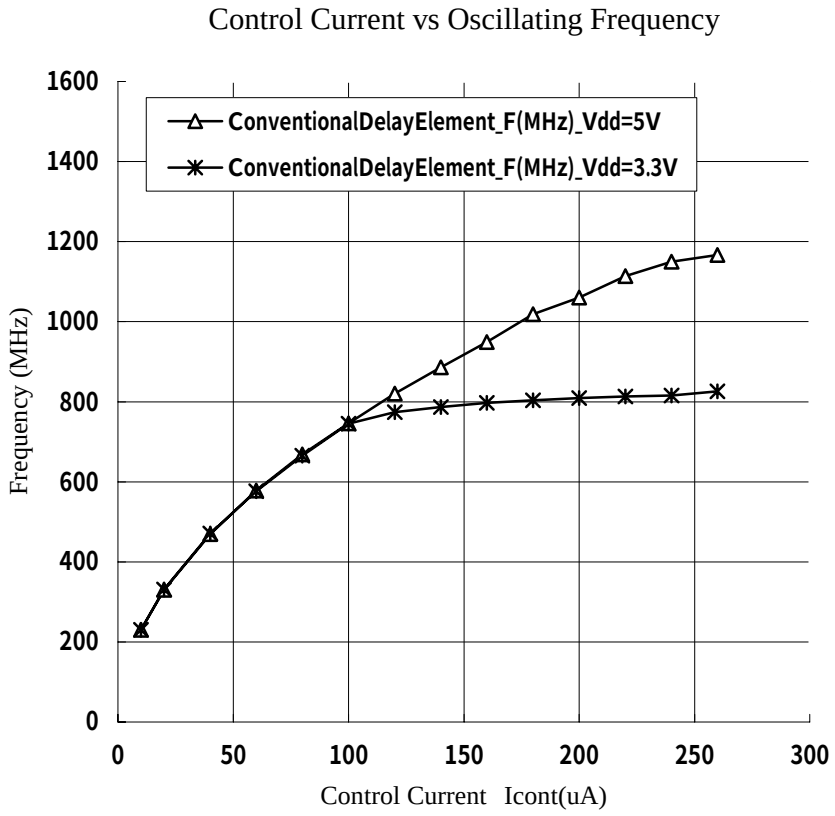



Fig. 4.4 Oscillation Frequency vs. Controlled Current

Another draw back of this circuit is the oscillation waveform is the sine wave. Therefore, to take out the digital signal from this delay element, some kind of comparator is required. Amplitude of the sine wave is very small. Therefore, the comparator should be designed carefully not to take noise or jitter coming from fluctuations in comparator threshold level.

For proposed PFD or CDR, a tapped delay line is required. Therefore, this type of delay element is not convenient.

SPICE simulation was made in 3-stage Current Controlled Circuit as shown in Fig. 4.2. As seen in Fig. 4.3a and Fig. 4.3b the oscillation waveforms are sine wave.

Fig. 4.4 shows characteristics of the oscillation frequency vs. control current. As seen in Fig. 4.4, the linearity is good in case of Vdd is 5V. However, in case of Vdd is 3.3V, the oscillation frequency is saturated in high control current area.

If the equivalent resistance of load MOS is decreased, the saturation in high current area may be improved. However, the oscillation frequency is saturated in low control current area, or oscillation itself is ceased.

Therefore the development of new type of delay element was required.

### 4.2.2 New Delay Element

In order to take more wider oscillation frequency range and more linear characteristics in current controlled oscillator, relaxation type delay element was developed.

Fig. 4.5 shows the new delay element. In Fig. 4.5, a differential pair MP01 and MP02 acts as a switch whose source current I1 is supplied by MP03. MP03, MP04 and MP06 are current mirrors, and width of the channel of MP04 is designed as half of MP03. Therefore current of MP04 I2 is designed a half of current of MP03 I1.

If the gate of MP01 IN is low level, MP01 conducts, and current I1 is flowing into the current mirror MN01 and MN02. Therefore, the charge stored on the gate capacitances of inverter MP05 and MN03 is discharged by the current,

$$I1 - I2 = I1/2. \qquad (4.1)$$

Next, if the gate of M01 IN is high level, MP01 becomes cutoff, then current of MN02 becomes zero. Therefore, the capacitances of inverter MP05 and MN03 are charged up by the current I2,

$$I2 = I1/2. \qquad (4.2)$$

Therefore, capacitances of the gate of inverter MP05 and MN03 are charged down and charged up by the same current I1/2 until ground level or Vdd, full swing. The currents I1, I2 and Icont are in relation of,

$$I2 = I1/2 = Icont/2. \qquad (4.3)$$

Therefore the linearity of the new delay unit is very good.

SPICE simulation was done as a 4-stage VCO. Circuit is shown in Fig. 4.6, and waveform of each stage is shown in Fig. 4.7, and characteristics as VCO is shown in Fig. 4.8.

As seen in Fig. 4.7, the waveform of each stage is rectangular, and delayed effectively. The linearity characteristics of frequency vs. control voltage is also good as shown in Fig. 4.8. MP03, MP04 and MP06 are current mirror, and width of the channel of MP04 is designed as half of MP03. Therefore current of MP04 I2 is designed a half of current of MP03 I1.

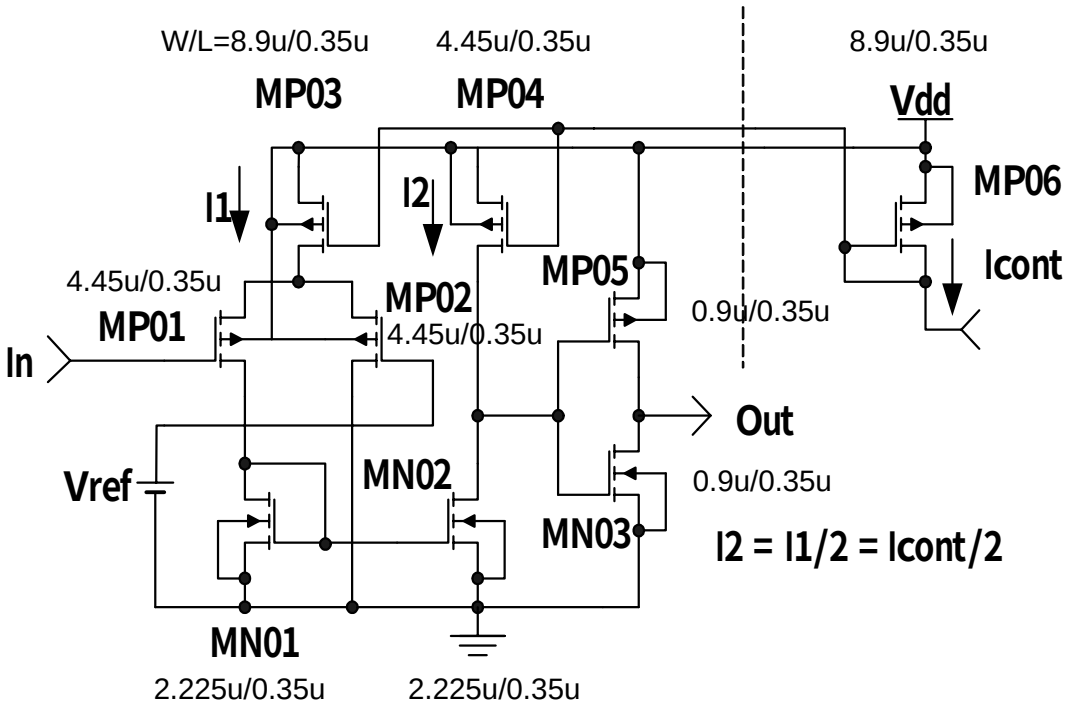



Fig. 4.5 New Delay element

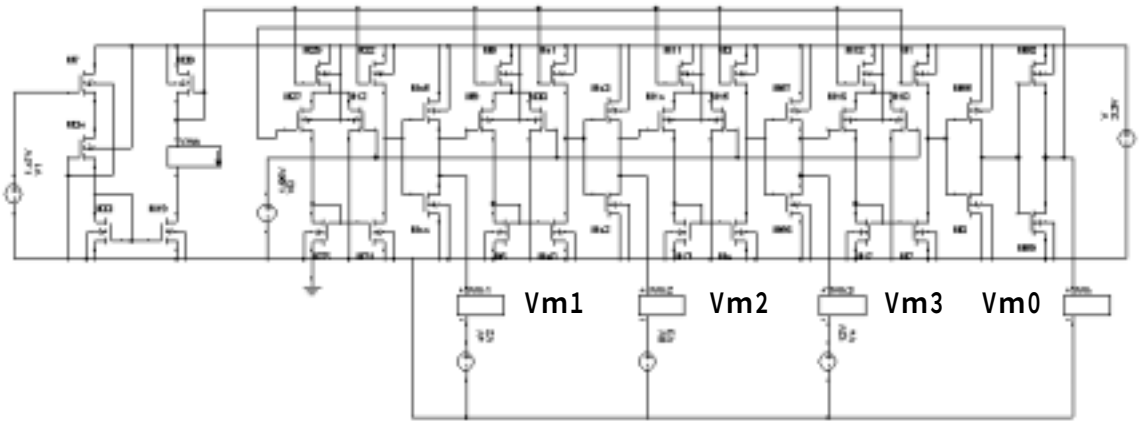



Fig. 4.6 Circuit for Simulation as a 4-Stages VCO

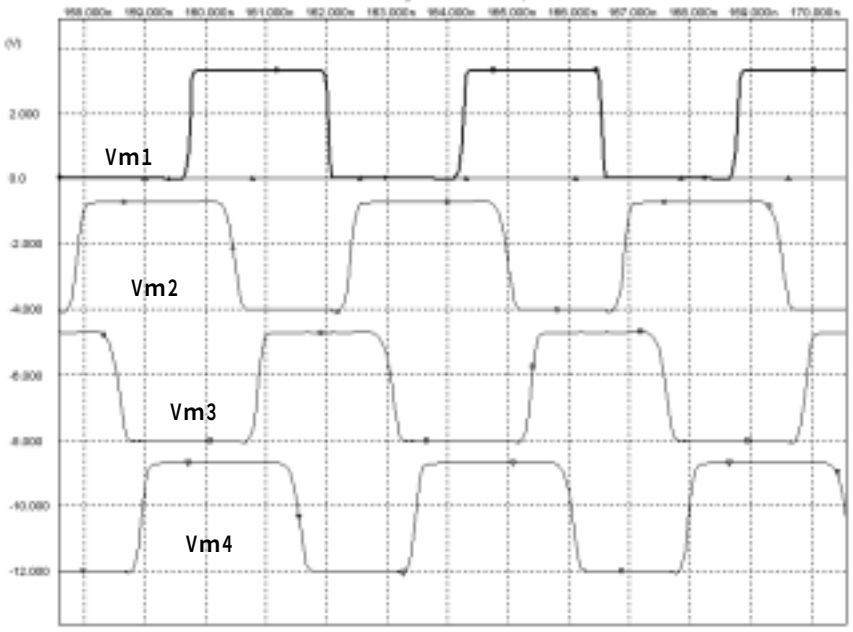



Fig. 4.7 Waveforms of each stage of delay element

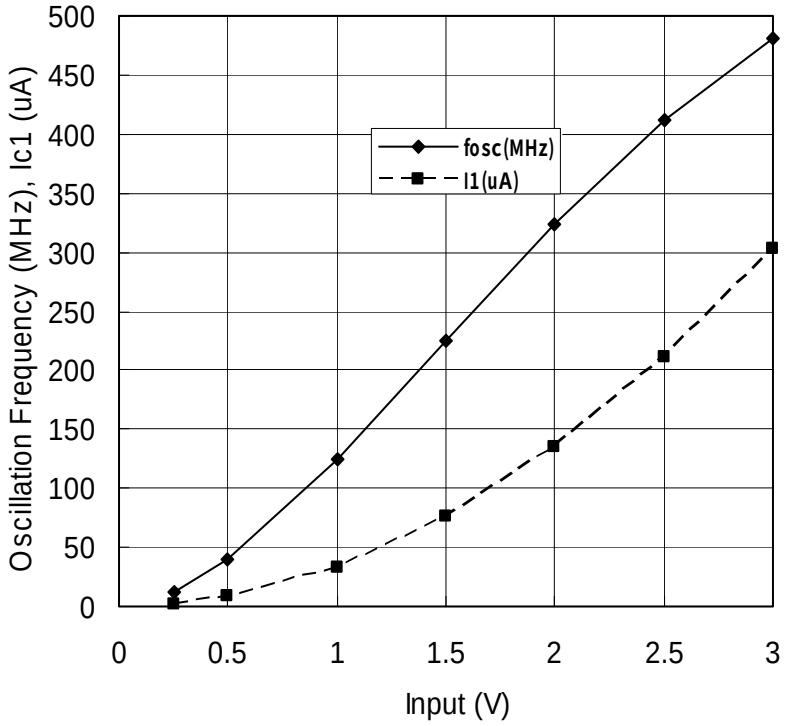



Fig. 4.8 Characteristics of new delay element as VCO

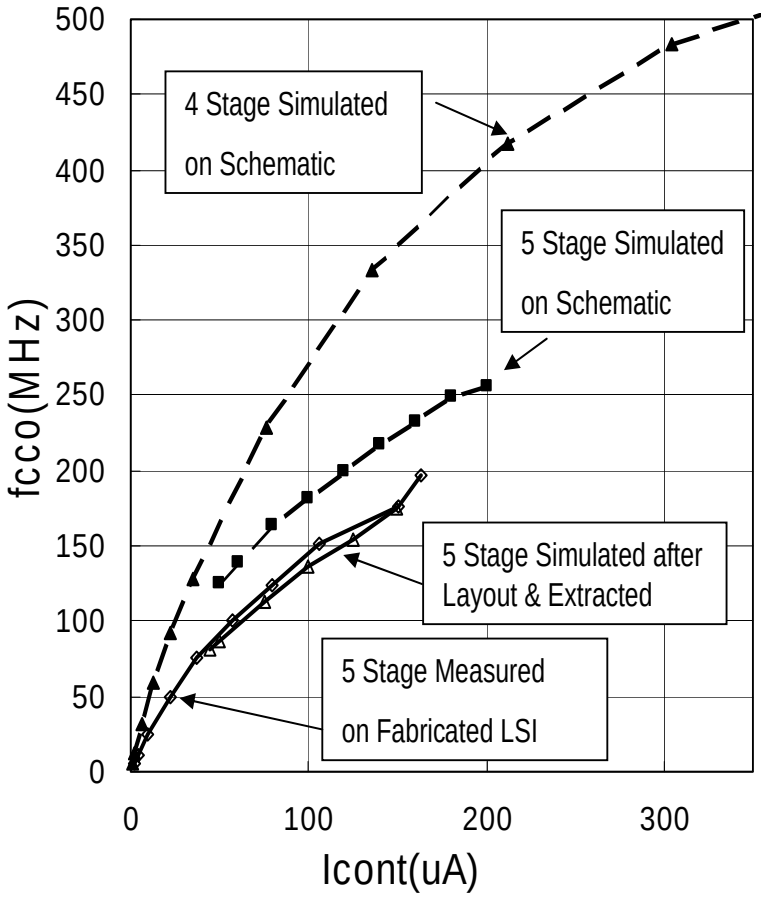



Fig. 4.9 Other characteristics of new delay element as CCO

The pattern layout design as 0.35u CMOS LSI was made as a current controlled oscillator using the delay elements, and was fabricated as a LSI.

Comparison among SPICE simulation on circuit schematic level, extracted net list level of pattern layout and measured result of fabricated LSI as shown in Fig, 4.9.

As a result, good correlation was acquired between SPICE simulation on extracted net list of pattern layout and actual measurement of fabricated LSI.
It means that if the SPICE simulation is down on extracted net list of pattern layout, good estimation can be attained on LSI to be fabricated.

In comparison between SPICE simulation on schematic level simulation and real LSI, the latter is around 80% in oscillation frequency. The difference is estimated to be the capacitances of the inter-connection.

## 4.3 Dimension Improved Charge Pump Circuit

The width of the out put pulses of new PFD are linear to the phase difference. The most effective way to convert the pulse width to the voltage is the charge pump which generates constant current pulse whose width is the same as the output pulse.

However, special precautions should be paid to keep constant current characteristics under wide varying output voltage in case of low supply voltage such as 3.3 Volts or lower. This will be explained next.

The charge pump circuit with current mirrors and differential pairs has been widely used. Due to the limited head space on low supply voltage, the constant current region of this type of charge pump is narrow, but has excellent characteristics as well as its simplicity. After repetition of SPICE simulation it became clear that a solution is to apply the large size of transistors in current mirrors and differential pairs to decrease the turn-on-voltage of transistors.

Fig. 4.10 shows the improved charge pump circuit with the description of channel width W and length L. MP1 and MP4 consist the current mirror whose W/L is 200um/0.35um for MP1, and 10um/0.35um for MP4. Therefore, charge pump current Icp is intended to be 10 times of setting current Ic. MP2 and MP3 consist the differential pair whose W/L is 50um/0.35um for MP2 and 10um/0.35um for MP3. As seen in Fig. 4.10, very large channel width transistors are introduced. N MOS transistors MN1 to MN4 are the same configuration. In common sense, differential pair should be designed in the same size of transistors to maintain the voltage at node P1 constant regardless of

switching of MP2 and MP3. This is intending to prevent the charge sharing between stray capacitance of node P1 and output filter circuit. However, this can be achieved if the drain voltage of MP3 is maintained at the same voltage that of MP2. This scheme may be necessary in the Bang Bang PD, because the value of charge pump current which is allowed for Bang Bang Pd is low value of 10 or 20uA due to its high gain and large width of output pulses. The new PFD allows 400uA to 1000uA due to its small width of pulses at matched state. Therefore, the effect of stray capacitance at node P1 is small.

The purpose of MP3 is to maintain the voltage at P1 to be less than VDD at turn-off state of MP2 to secure complete turn-off and prevent the effect of leakage current of MP2. Therefore the small size of MP3 is enough.

Fig. 4.11 shows the constant current characteristics of the circuit shown in Fig. 4.10. As seen in Fig. 4.11, the characteristics of constant current is very flat at 1000uA even though the output voltage Vo changes wide range of 0.5 to 2.8V.

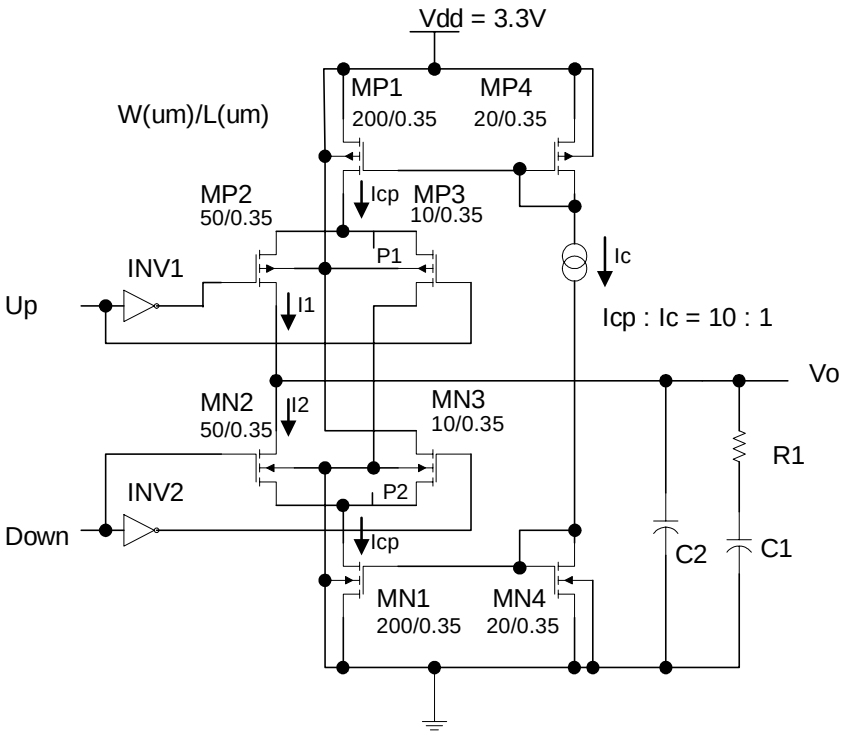



Fig. 4.10 Dimension improved charge pump circuit

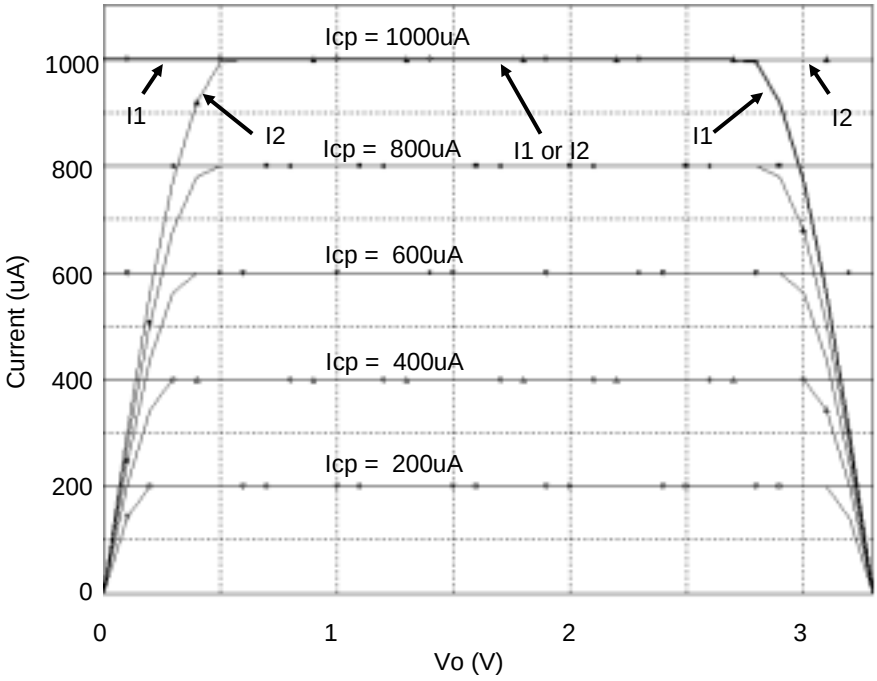



Fig. 4.11 Characteristics of charge pump circuit of Fig. 4.10

# 4.4 Charge Pump Current Control

To achieve wider variable bit rate under fixed filter time constant, a charge pump current control is introduced. To acquire smooth and rapid frequency capture in high bit rate range, higher charge pump current required; otherwise, CCO frequency is suspended in mid way. Conversely, if the charge pump current is too high in low bit rate range, system becomes unstable due to the high open loop gain.

Therefore, charge pump current should be controlled so that it should be proportional to the output voltage of charge pump.

Fig. 4.12 shows the circuit of charge pump current control. As shown in Fig. 4.12, MN32, MP32 is a voltage to current converter, and MN33, MN35 consist of a current mirror. MN34, MP33 and MP34 also consist of current mirror.

Constant current I0 is connected to diode connected MN33. By designing adequate channel width, it is easy to make the currents;

$$Ic2 = Ic3 = a\,(Ic1 + I0). \qquad (4.4)$$

a can be set 1 to 4. Currents Ic2 and Ic3 are connected to charge pump currents of charge-up and discharge-down.

In Fig. 4.12, charge pump portion is drawn in simplified circuit. However, in real SPICE simulation, differential charge pump portion was used as shown in Fig. 4.10.

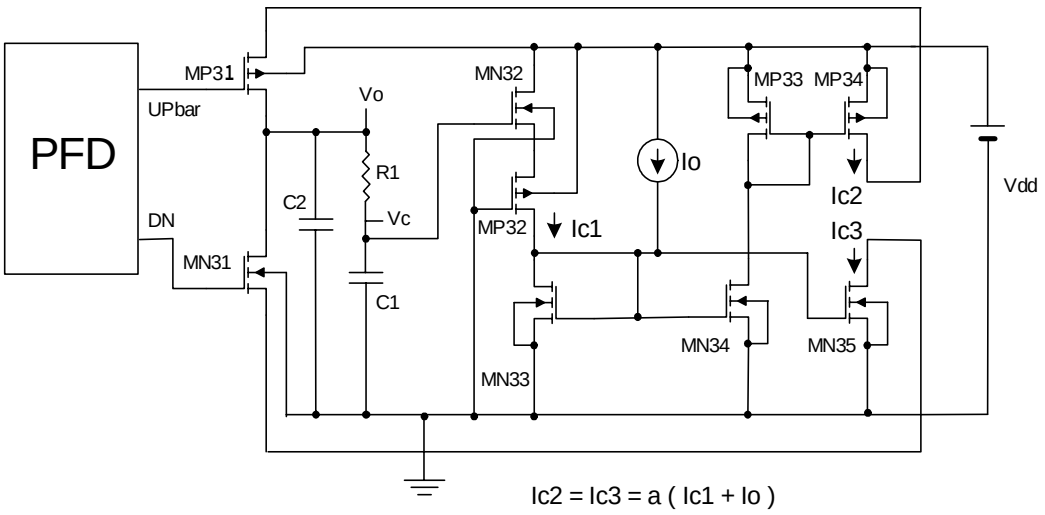



Fig. 4.12 Charge pump current control

# Chapter 5

# CDR for Fixed bit Rate

## 5.1 Summary

Data bit rate is pre-defined at a fixed value in most of the applications. In those applications, the most stable delay is that of physical entity such as coaxial cable or micro-strip line. For full integration, semiconductor delay element is used. To acquire more rapid frequency capture and false-lock-free operation, an adaptive PFD, utilizing a negative feedback to the data delay as well as time slot control, has been developed.

This will be discussed Next.

## 5.2 Data Delay for Differentiation

NRZ data does not have the explicit frequency component of original clock which generate NRZ data itself. To extract the frequency component of original clock, a data differentiation is mandatory. A combination of delay element and exclusive OR is effective for differentiation, so called, delay line differentiation. Therefore, the new 4-state PFD uses this scheme by tapped delay elements, delay time t1 for Data_dif and t2 for Vreset. To prevent false lock, t1 should be 0.6Tb (Tb is one bit time interval), and t2 should be t1 + 0.1Tb = 0.7tb. If t1 is taken less than 0.5Tb, false lock occurs at 2X of local clock Xck frequency. If t1 is set larger than 0.5Tb, false lock can be avoided because two leading edge of XCk are deployed during time interval of t1 at 2X of local clock frequency, then down pulse is generated on the output of the PFD.

For stable application for fixed bit rate, the best solution is that these delays should be taken by physical entity such as coaxial cable (Coax), twisted pair or micro-strip line on PCB, because the characteristics are predictable and it is power consumption-less. For example, Tb at data bit rate of 100Mbps is 10ns. In vacuum state, delay time in length of 3m is 10ns. However, the velocity factor of standard 50Ω Coax is 67%. So, the delay time of 2.01m Coax is 10ns. Therefore, t1(0.6Tb = 6ns) can be attained by 1.2m Coax. For 1Gbps the length becomes only 12cm.

However, the size is very important for most of the applications. In such a case the delay elements are integrated inside of semiconductor, and their delay time fluctuation by temperature or supply voltage change becomes the issue.

A solution of the issue is negative feedback to data delay. This will be explained next.

## 5.3 Negative Feedback to Data Delay

Fig. 5.1 presents the block diagram of proposed CDR system. The system consists of a current-controlled data delay (CCDD), New 4-State PFD, charge pump, Filter, voltage-to-current (V-I) converter-1, current controlled oscillator (CCO), and voltage-to-current (V-I) converter-1 with Current Subtraction.

The voltage out put of Filter Vo is converted to current Ic by V-I converter-1. Ic is provided to Current Controlled Oscillator (CCO), and the frequency of the CCO is controlled by the Ic. Other smoothed output of filter, Vc is provided to V-I Converter-II with Current Subtraction, then voltage Vc is converted to current Id in reverse direction, i.e. if the Vc increases, Id will decrease. The delay time of CCDD is controlled by this Id.

Detailed operation of this CDR system is described in two parts using detail circuit shown in Fig. 5.2 and Verilog simulated waveforms in Fig. 5.3.

First, the 4-state PFD that relies on the CCDD for data differentiation is described using waveforms under phase-locked and near phase-locked conditions illustrated in Fig. 5.3. Second, negative feedback control of the CCDD's delay required to prevent false lock and enable fast frequency capture is described. A time slot control method prevents false locking at 1.5 times the bit rate.

In Fig. 5.3, time points labeled from “a” through “g” illustrate the operation of the PFD in the absence of a data transition. DFF3 is reset during “a”-“c” due the data transition at “a”, but does not reset again until the next data transition at “g”. Hence, on the falling edge of Xck, the output of DFF3 (E) goes high, signifying a missing data transition state. E is used to swallow the error pulse out of DFF2 and prevent it from propagating to the charge pump. Furthermore, the high state of E causes both DFF1 and DFF2 to reset through AND2 on the subsequent rising edge of Xck and prepare them for the next set of edges.

In some applications, the delay times of leading and trailing edges of data may not be the same due to the characteristics of amplifiers or buffers included in the transmitter and receiver of the transceiver system. Therefore, phase detection on both rising and falling data edges can lead to higher jitter, and this jitter is data pattern dependent. So, single edge comparison is sometimes preferable. As a result, pulses corresponding to trailing edge comparison, m1~m3, n1~n3 are also eliminated when F is low.

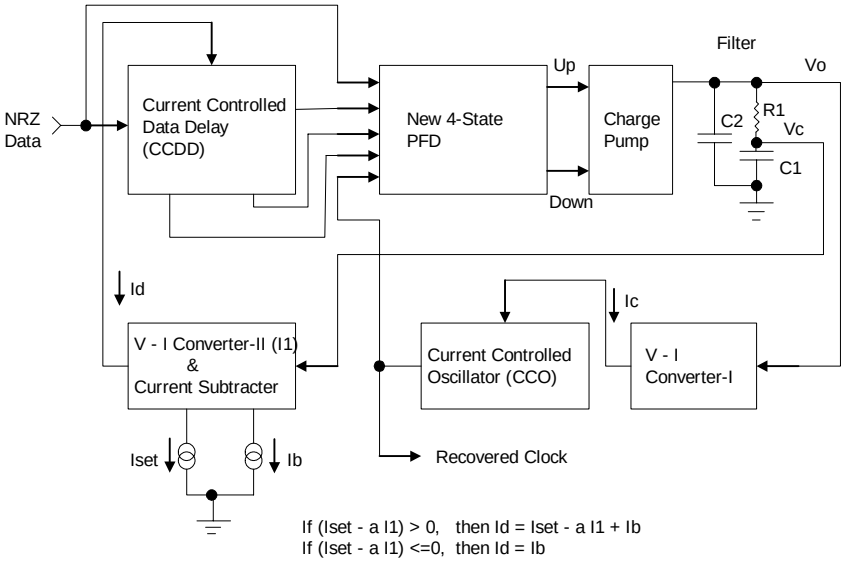



Fig. 5.1 Block Diagram of CDR for Fixed bit Rate with Negative Feedback to Data Delay

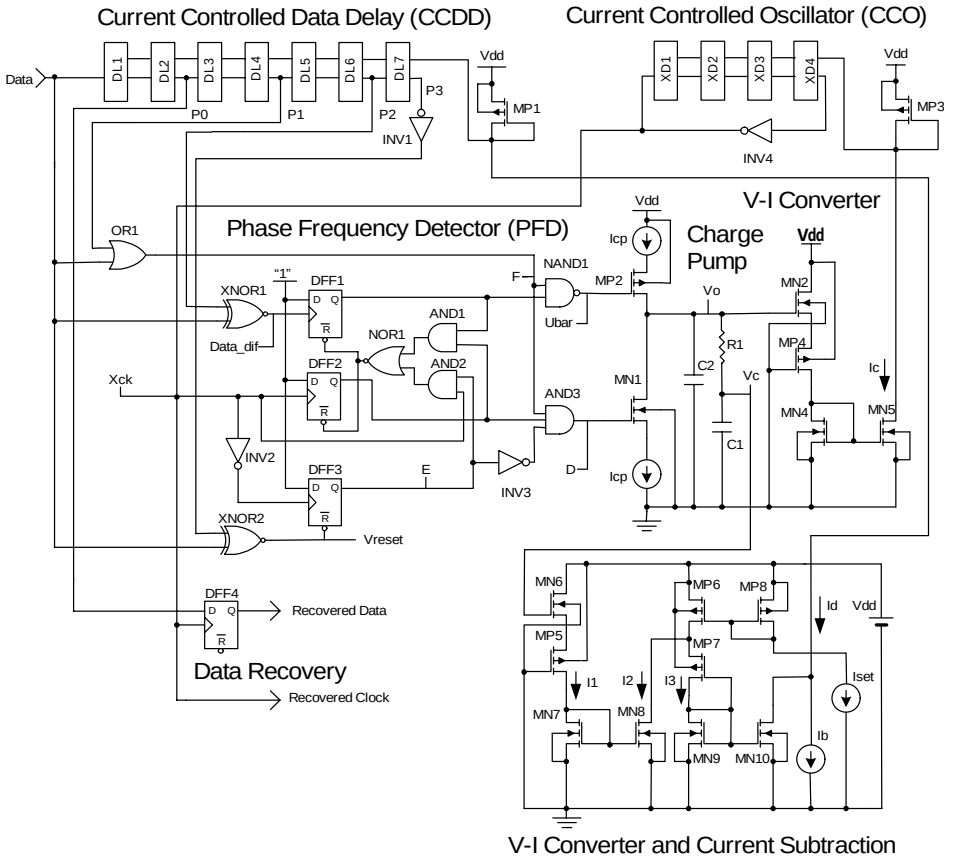



Fig. 5.2 Circuit of CDR for Fixed bit Rate with Negative Feedback to Data Delay

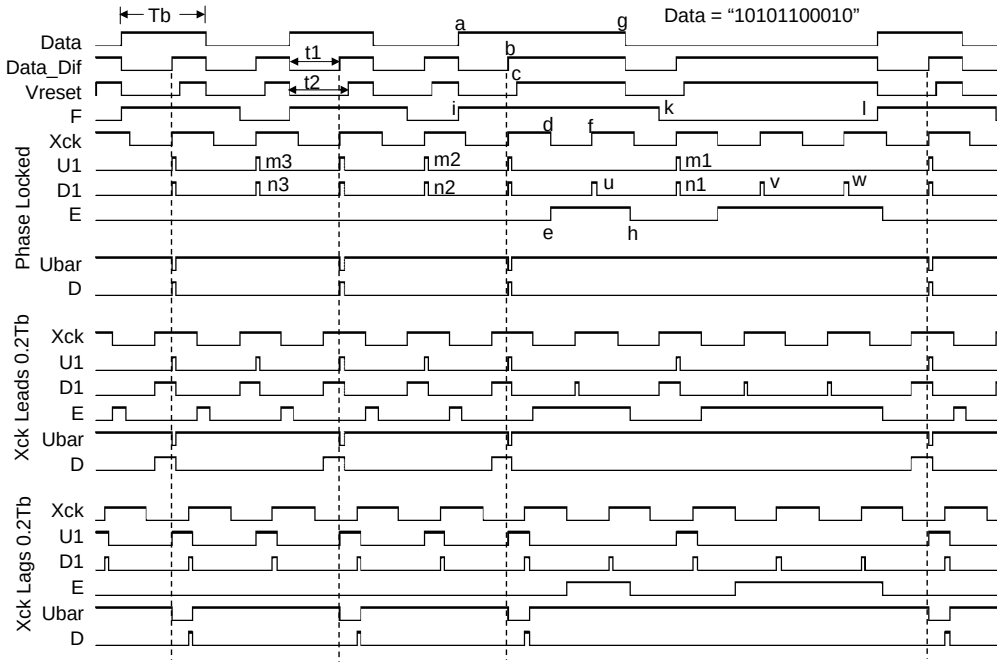



Fig. 5.3 Verilog Simulated waveforms, Xck Phase locked, lead and lag

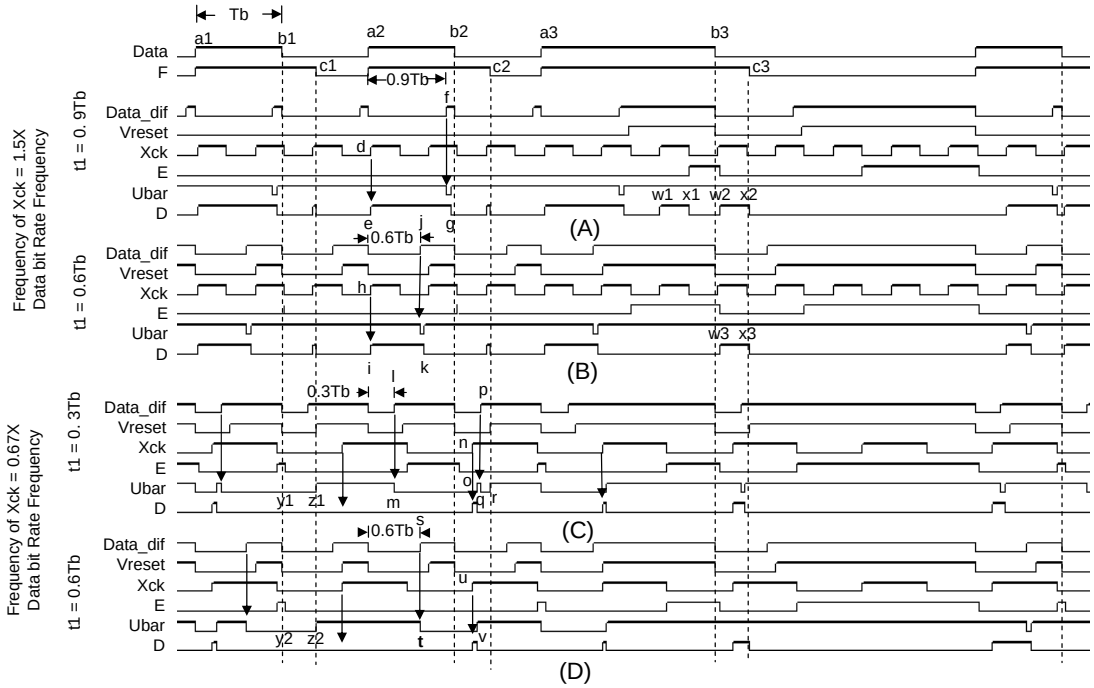



Fig. 5.4 Effect of Negative Feedback to Data Delay

(A), (C) with Negative Feedback (B), (D) Fixed Delay

(A), (B) High Frequency in Xck (C), (D) Low Frequency in Xck

Fig. 5.3 also presents waveforms when Xck leads and lags the data. The waveforms show that the appropriate up and down pulses are generated for the charge pump to lock the loop.

## 5.3.1 Rapid Frequency Capture and False Lock Prevention

### 5.3.1.1 Negative Feedback Method

The delay time for data differentiation t1 in Fig. 5.3 plays a very important role in the PFD's operation. If it is set lower than 0.5Tb (Tb = 1bit time interval), the CCO frequency may falsely lock to twice the bit rate (2.0X false lock). If t1 is set at a fixed value throughout operation, the settable range is very narrow --- 0.6 to 0.8Tb. If the delay time is set by the current flowing through a resistor, the range may not be enough for voltage fluctuation of power supply. Therefore, it is important to enlarge the settable range of t1. Even if t1 is set smaller than 0.5Tb at the same frequency (1.0X) of bit rate frequency of data in CCO, and if some measure is taken so that t1 becomes larger than 0.5Tb at 2.0X on CCO frequency, the 2.0X false lock can be avoided, and settable range can also be enlarged. To this end, negative feedback is used in order to adaptively control t1 to be larger for higher CCO frequency and vice versa.

Moreover, rapid frequency capture can be realized by this method, because it generates wider error pulses. A comparison of different t1 delays and CCO frequencies (fXck) is presented in Fig. 4: (A) is the case t1 = 0.9Tb and fXck = 1.5X; (B) t1 = 0.6Tb, fXck = 1.0X, (C) t1 = 0.3Tb, fXck = 0.67X; and (D) t1 = 0.6Tb, fXck = 0.67Tb. For higher Xck frequency, comparing (A) and (B) in Fig. 3, if t1 is the larger, the larger width of down pulse e-g occurs in D than the pulse width i-k. For lower Xck frequency, comparing (C) and (D), if t1 is the smaller, the larger width of up pulse m-r occurs in Ubar than the pulse width t-v. Therefore, t1 should be larger for higher fXck, and t1 should be smaller for lower fXck. As a result, negative feedback control of CCDD is applied for rapid frequency capture and false lock prevention. This negative feedback scheme is realized by a V-I Converter and Current Subtraction circuits shown in Fig. 5.2.

In Fig. 1, MN6, MP5, MN7 and MN8 comprise the V-I converter where MN6 is a source follower, MP5 is a resistor equivalent, and MN7 and MN8 implement a current mirror. The gate of MN6 is connected to Vc and sets I1. MP6 and MP8 constitute a current mirror which reflects the current Iset to the current flowing through MP6. MP7 is a PMOS whose source is connected to the drains of both MN8 and MP6, so that MP7 acts as a cascode (cascaded-triode)

with MN8 and MP6. Therefore, impedance conversion is done by MP7 from a low impedance source input to a high impedance drain output. The sum of I2 and I3 equals Iset. Thus, the current Id should be written as follows.

$$I2 = aI1 \quad (5.1)$$

$$Iset - aI1 > 0,\ Id = Iset - aI1 + Ib \quad (5.2)$$

$$Iset - aI1 <= 0,\ Id = Ib \quad (5.3)$$

When Vc is high, the frequency of CCO is also high, I1 is large, Id becomes small, and delay time of CCDD becomes large. In practical application, the maximum delay time of CCDD is set first by Ib at the highest CCO frequency. Then Iset should be set so that the delay time of Data_dif becomes 0.6Tb at phase locked state. Ib and Iset can be replaced by resistors. Thus, a very simple and high-speed combination of source follower and cascode functions well. The gate of MN6 may be connected to charge pump output, Vo. However, SPICE simulations verified that the connection to the filtered output, Vc, makes the CDR more stable.

## 5.3.1.2 Time Slot Control Method

In order to reduce jitter, leading-edge-only comparison of the Data is used, which detects only leading edge of input Data. In this case, mutual input F of AND3 and NAND1 as shown in Fig. 5.2 is driven by the input Data. If the delay time t1 is smaller than 0.67Tb, a “1.5X false lock" may occur. The 1.5X false lock here is defined as the lock condition when the CCO frequency is around 1.5 times the target data rate. It is a kind of run-time false lock, which occurs when the accumulated pulse width of up pulses becomes equal to the accumulated pulse width of down pulses in a plurality of data bits. Therefore, it is important to prevent this run-time false lock. Fig. 5.5 illustrates the phenomena with SPICE simulated waveforms. This is the case of t1=0.4Tb, and data pattern is a repeated "10101100" data pattern.

The Upper set of waveforms, "Time Slot=Data", are for the leading edge comparison case. The accumulated pulse width of a, b and c is equal to that of d, e and f, and false lock occurs. 13 cycles of Xck are deployed in 8 bit time intervals of Data, so this is a 1.625 times fXck false lock. This false lock can be avoided if F is driven by OR1 as shown in Fig. 5.2. The inputs of OR1 are connected to Data and tap P1 of the CCDD, therefore a longer interval of the high level than Data is supplied to AND3 and NAND1. As a result, a part of the trailing edge comparison outputs g and h are created on D, as shown by the lower set of waveforms "Time Slot = F" in Fig. 5.5.

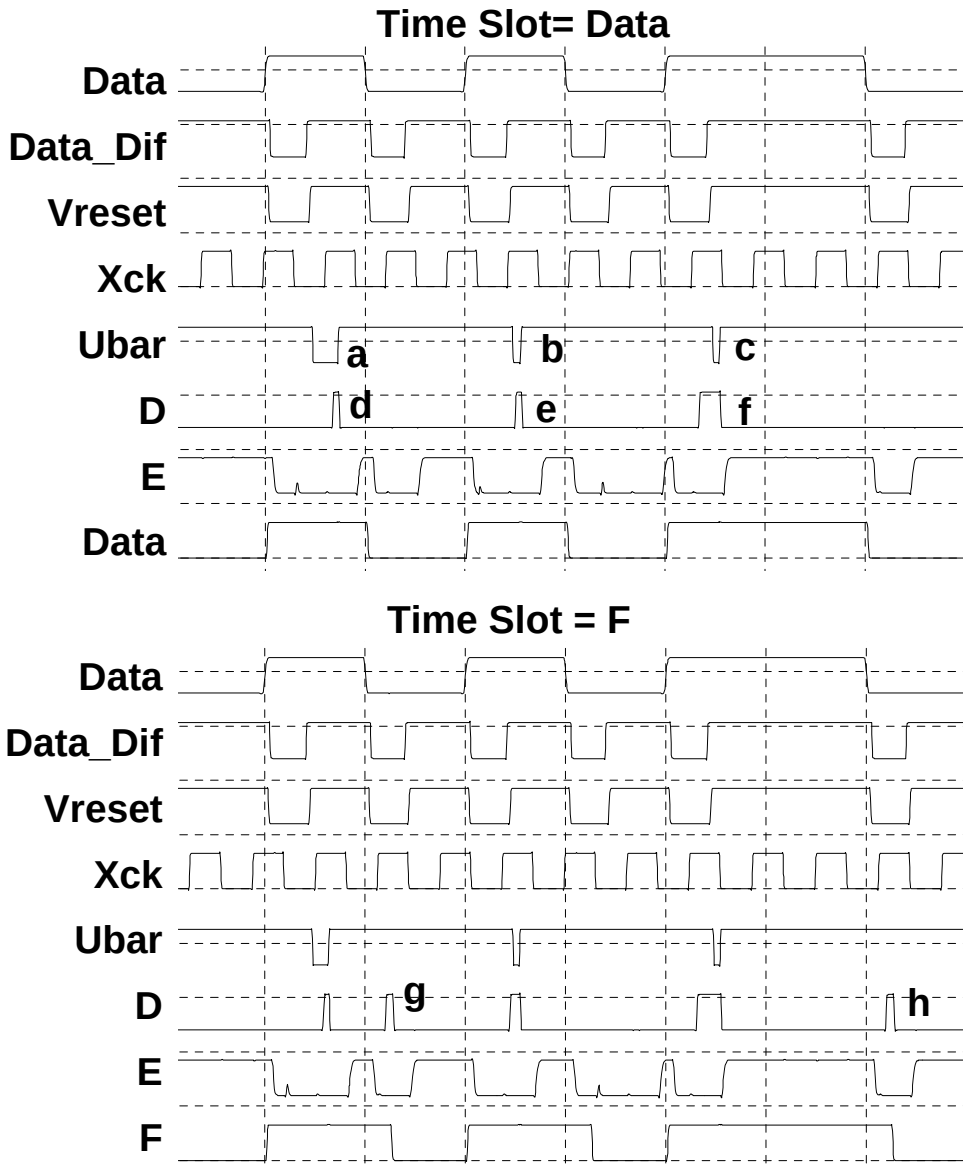



Fig. 5.5 1.5X False Lock (upper)
Counter measured (lower)

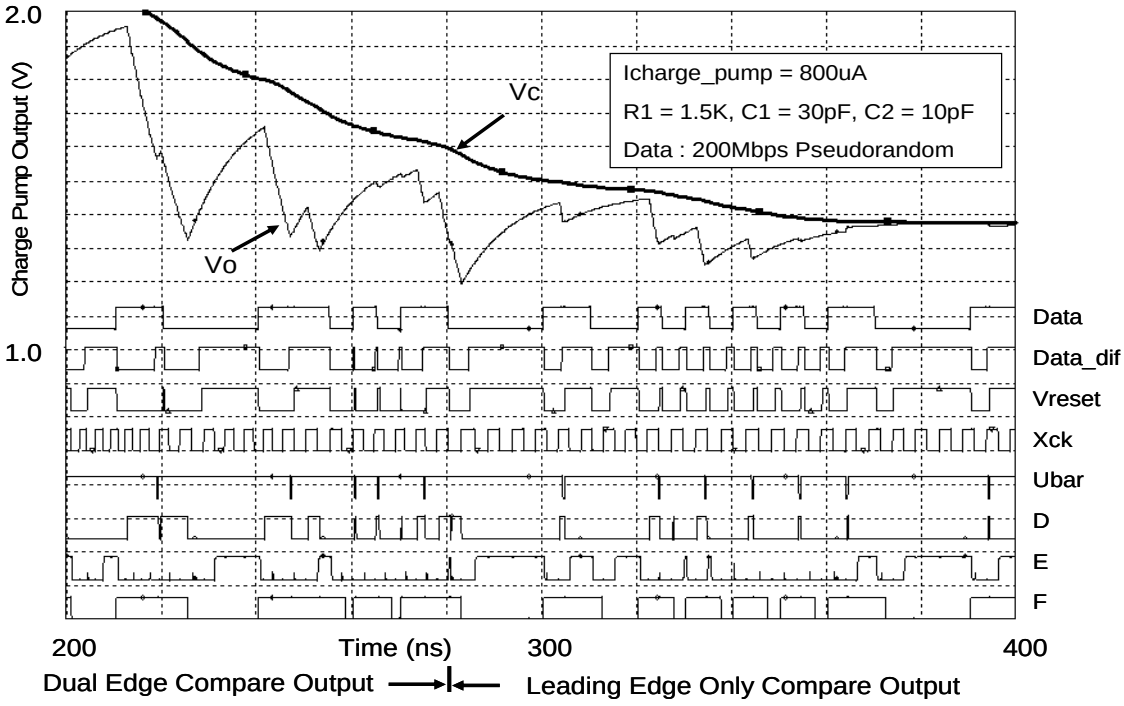



Fig. 5.6 Time Slot Control, Smooth Transition

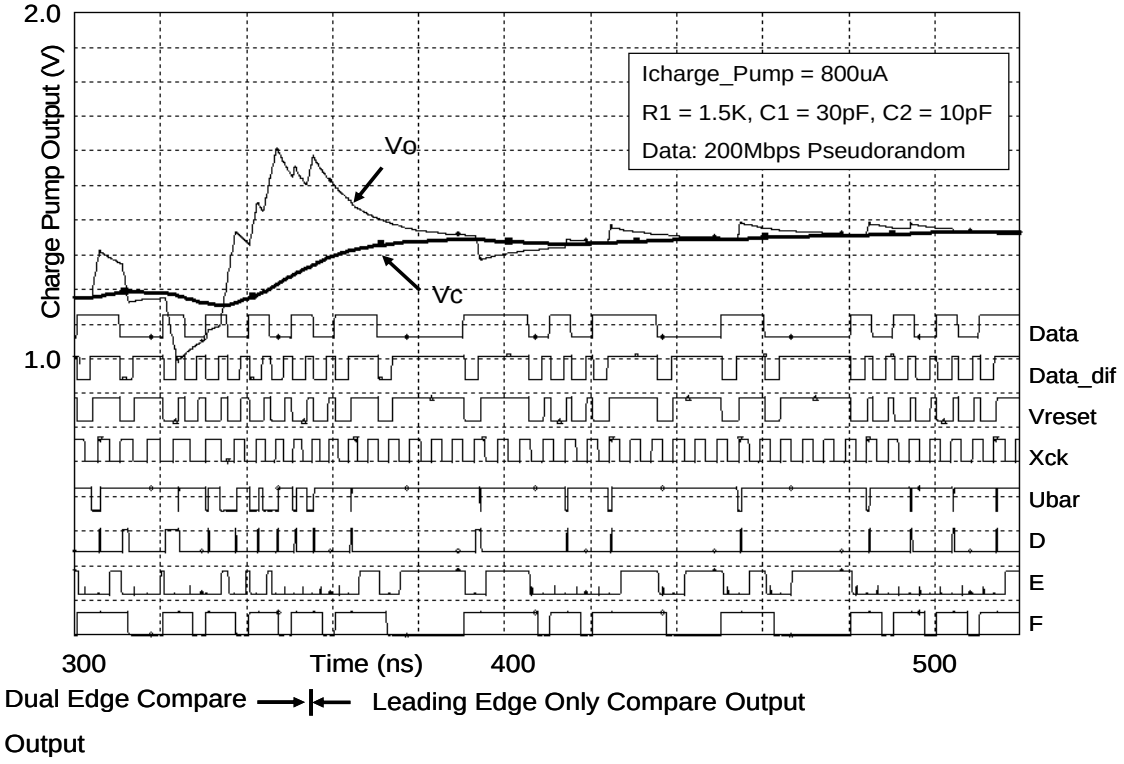



Fig. 5.7 Detail of lock-in stage, Upward frequency capture

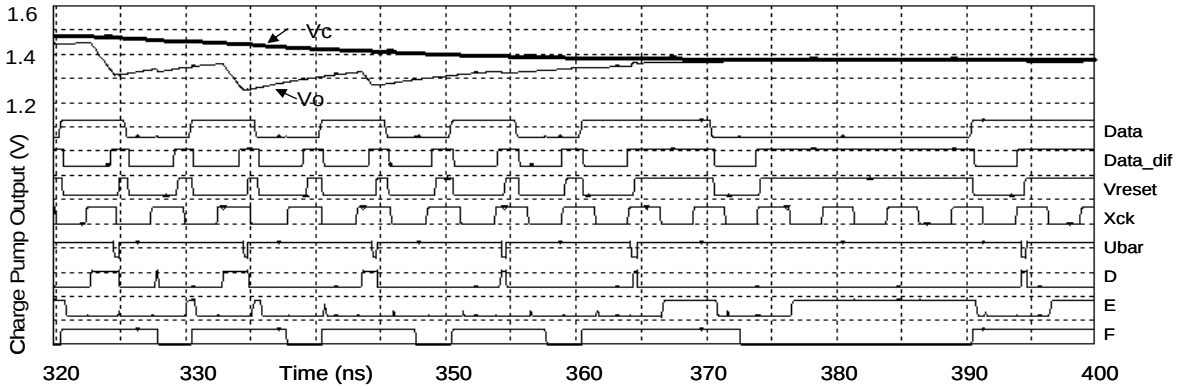



Fig. 5.8 More expanded detail of near matching,
Downward frequency capture

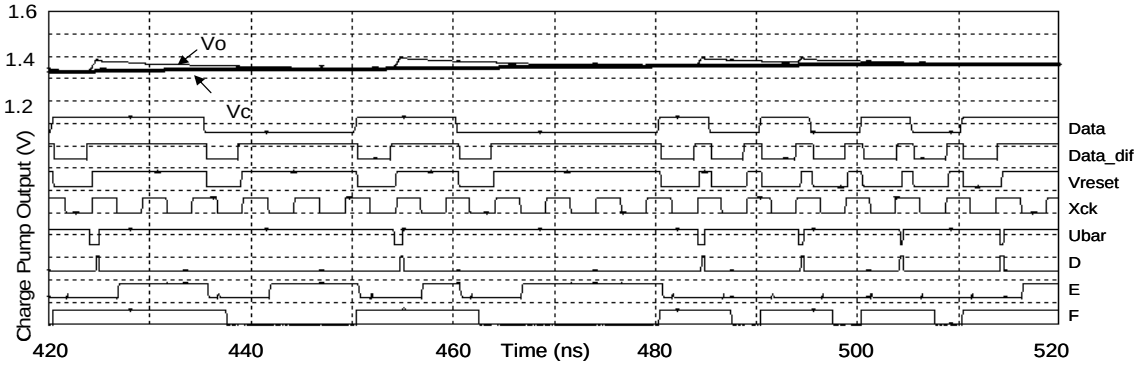



Fig. 5.9 More expanded detail of near matching,
Upward frequency capture

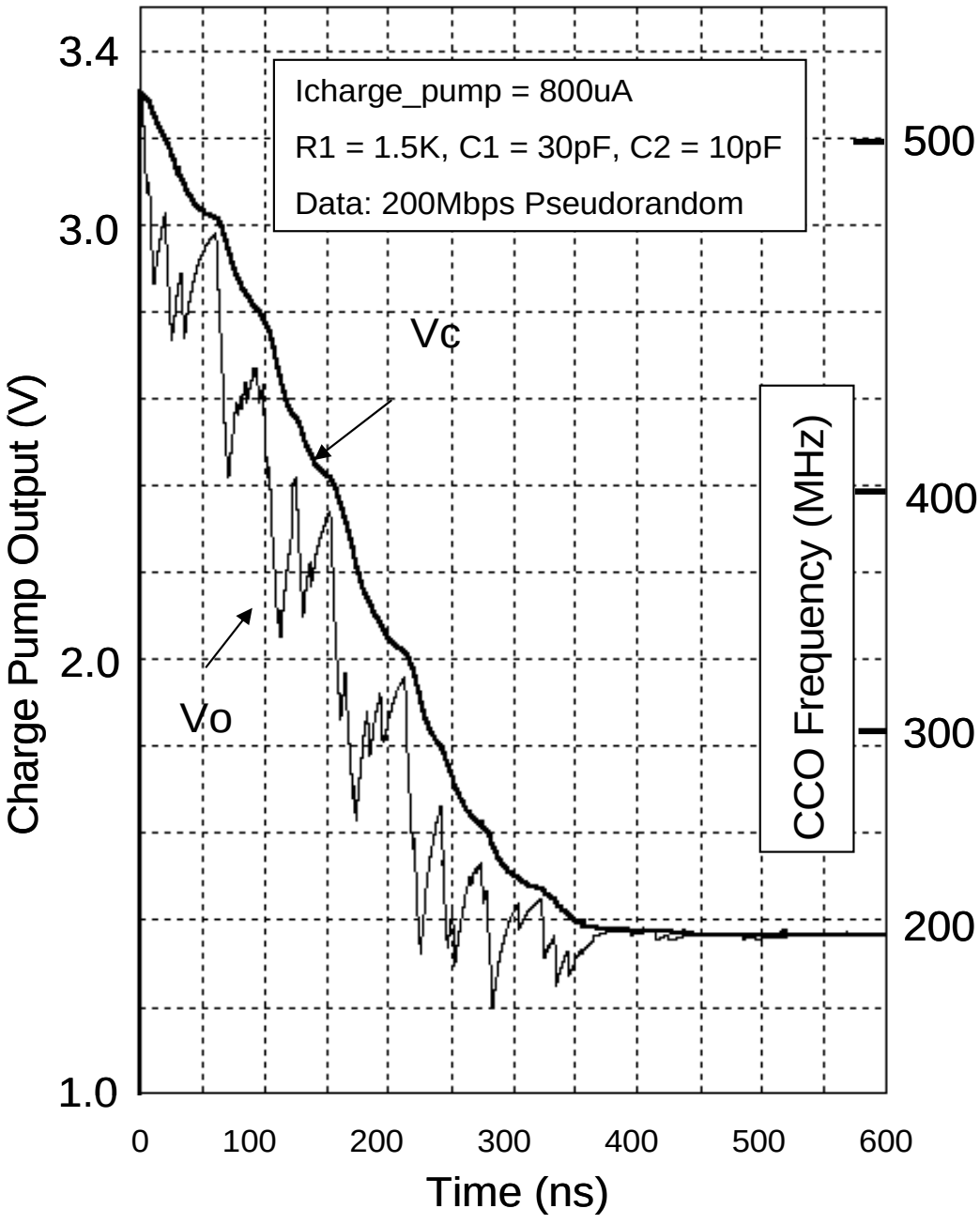



Fig. 5.10 Downward frequency capture

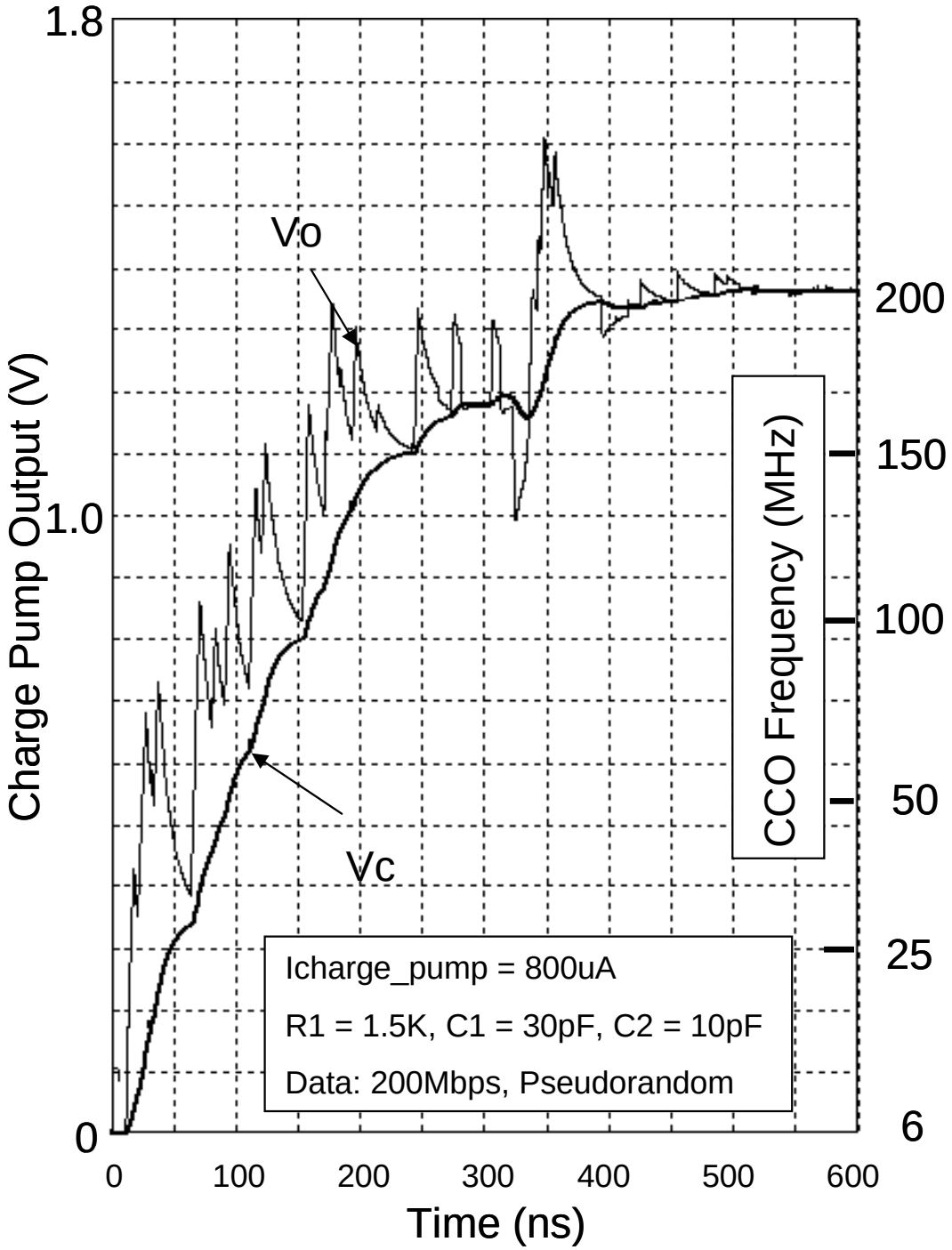



Fig. 5.11 Upward frequency capture

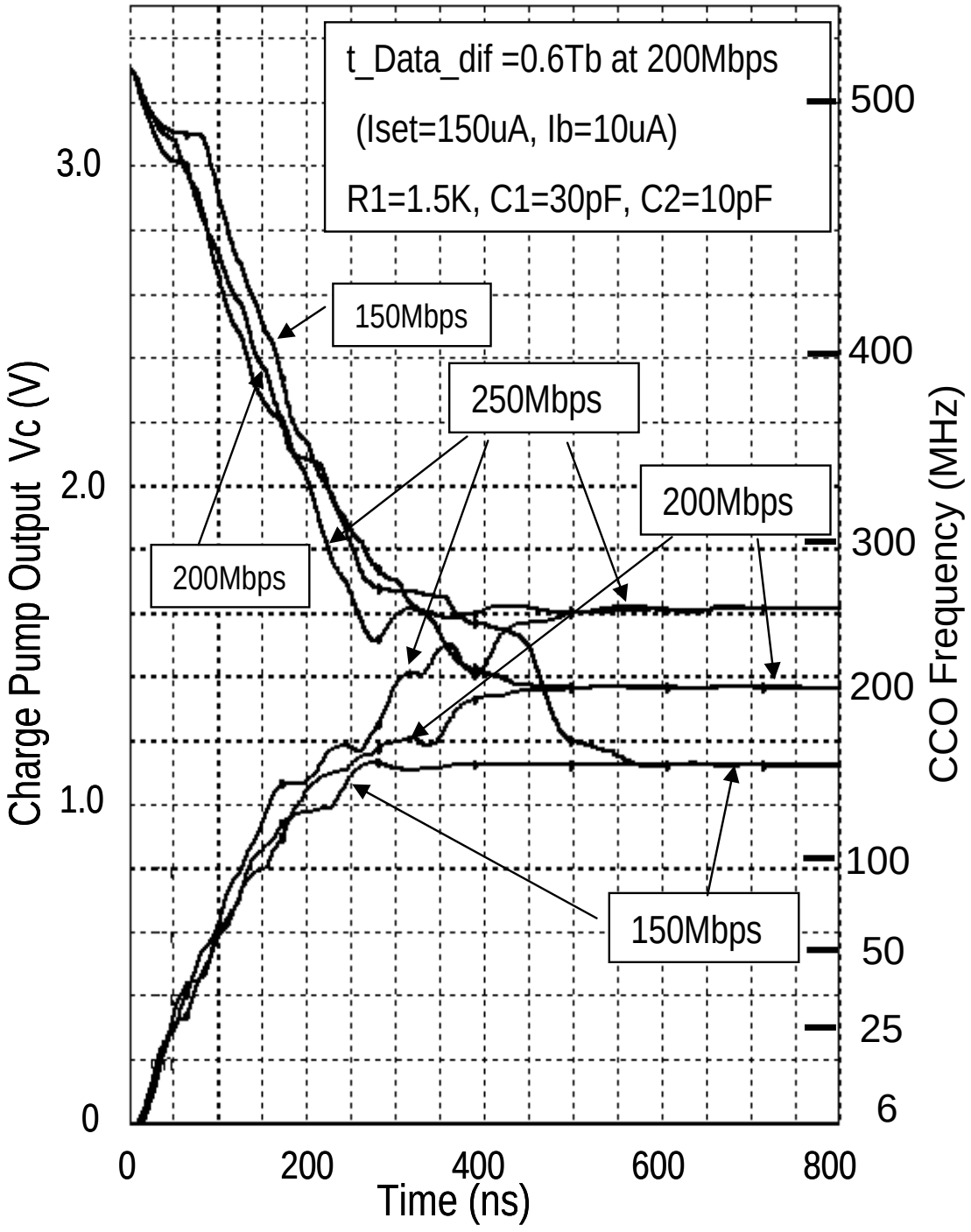



Fig. 5.12 Operable Data bit Rate

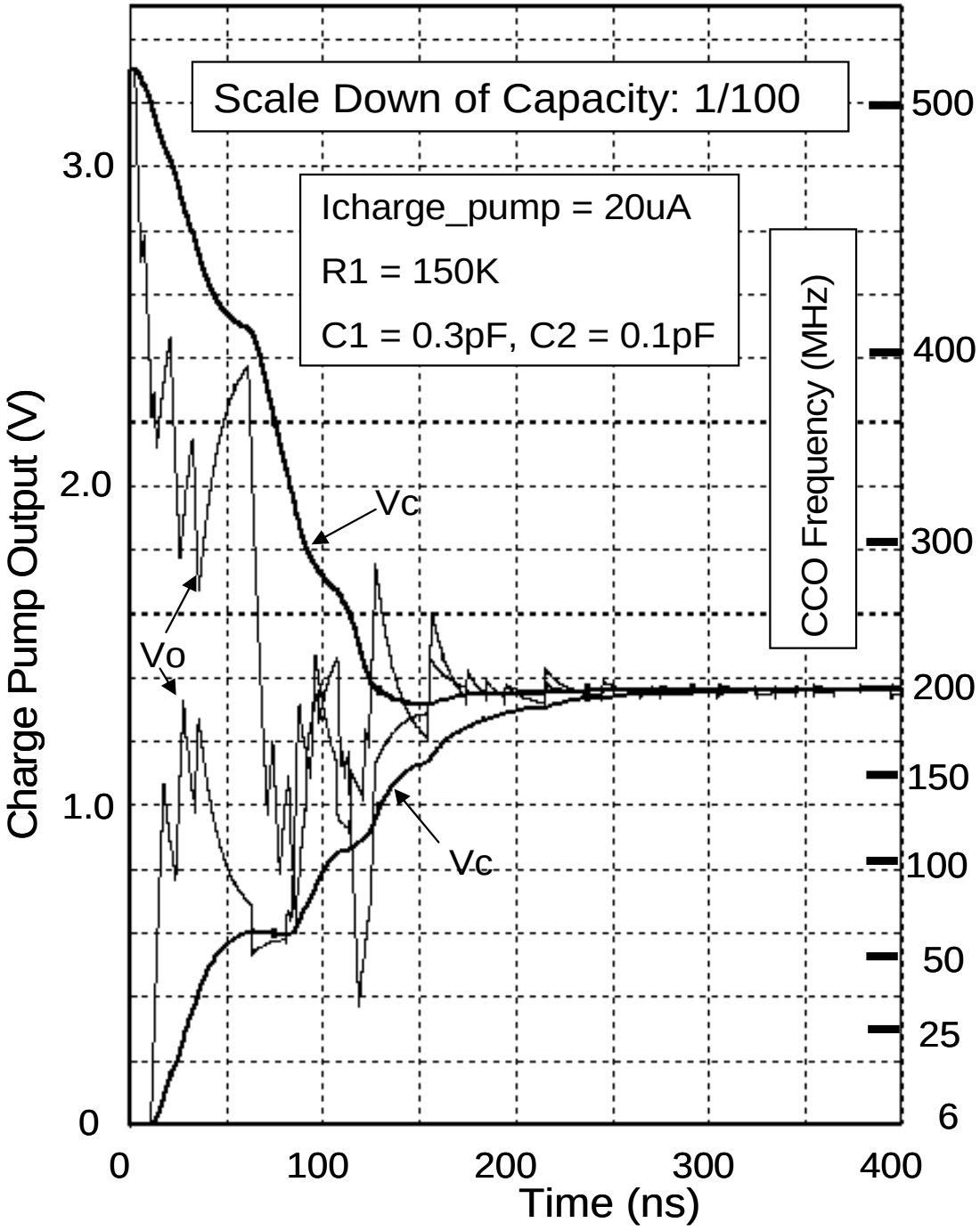



Fig. 5.13 Scale down of capacity by 1/100

With this simple modification, this false lock condition can be avoided. The time slot is designed so that the outputs of the PFD are prohibited only around the vicinity of Data_dif's leading edge corresponding to the low level of data.

This is also clear in Fig. 5.4. In Fig. 5.4, F is longer than data in b1-c1, b2-c2 and b3-c3. Therefore, pulses w1-x1, w2-x2 and w3-x3 are included as down pulses. This time slot control scheme also enables rapid frequency capture, dual edge comparison during frequency capture, and leading-edge-only comparison in phase matching stage under smooth transition as shown in Fig. 5.6 and Fig. 5.7 SPICE simulated waveforms.

Fig. 5.8 and Fig. 5.9 show more time-expanded detail of near phase match and lock-in stage. As seen in Fig. 5.8 and Fig. 5.9, very smooth and low ripple lock-in can be realized. Fig. 5.10 shows downward frequency capture. Very rapid and false lock free frequency capture and lock-in is verified from 500MHz to 200Mhz in CCO frequency. Fig. 5.11 also shows upward frequency capture from 6 MHz to 200MHz. Fig. 5.12 shows the input bit rate capture range. As seen in Fig. 5.12, 200Mbps +/- 50Mbps is verified.

In order to confirm the possibility to integrate the filter capacitor inside of the LSI, 1/100 scale down of capacitor was simulated as shown in Fig. 5.13. As seen in Fig. 5.13, good lock-in characteristics were verified under C1 = 0.3PF and C2 = 0.1pF. These values of capacitor may be integrated as LSI.

As a whole, negative feedback (inverse direction current feedback) CCDD control and time slot control are effective in achieving rapid and false-lock free frequency capture.

## 5.3.2 Conclusion of Negative Feedback to Data Delay for Fixed bit Rate Application

A new PFD with negative feedback data delay and timeslot control have been presented and the combination of schemes as an adaptive PFD have been demonstrated to be effective for achieving rapid and false-lock free frequency capture. Rapid lock-in time has been verified by SPICE simulation, 450ns in frequency capture from 500MHz down to 200MHz, and 550ns in frequency capture from 6MHz up to 200MHz for a 200Mbps pseudorandom data sequence.

Allowable bit rate is also confirmed to be 200Mbps plus minus 50Mbps (+/- 25%), and it might be sufficient for fixed bit rate application.

The new PFD is an effectively 4-state PFD, therefore it inherits the features of 3-state PFD such as frequency detection and low jitter characteristics even for NRZ data.

# Chapter 6

# CDR for Variable or Multiple bit Rate

## 6.1 Summary

Under the progress of information technology, paramount requirements are arising for the receiver to meet to the variable bit rate or multiple different bit rate transmitters in NRZ data. To meet those requirements, CDRs with the wider capture range of input bit rate have been developed using newly developed 4-state PFD.

In wide bit rate application, the stability issue became apparent especially in low bit rate area at fixed constants of charge pump circuit and succeeding filter. Therefore, z-Domain analysis were made, and it became clear that the z-Domain analysis was very powerful tool for evaluation of stability.

As the result of z-Domain analysis, it also became clear that the adaptive current control of charge pump was very effective as the countermeasure for this stability issue.

In such a wide input bit rate capture range, frequency capture aid is necessary. Analog- and digital-frequency capture aids are also presented.

Firstly, CDR comparatively narrow variable bit rate of 50Mbps to 200Mbps is presented. Secondly, more wider variable bit rate CDR of 1 decade, 40Mbps to 400Mbps, is presented.

## 6.2 CDR for Narrow Variable bit Rate

Fig. 6.1.1 presents the block diagram of proposed CDR system. The system consists of a current-controlled data delay (CCDD), New 4-State PFD, Charge Pump, V-I Converter with current feedback both to CCDD and current controlled oscillator (CCO) and Downward Frequency Capture Aid (DFCA).

Fig. 6.1.2 shows the circuit of the system. Details of operation of the system will be described in two parts. Firstly, the 4-state PFD that relies on the CCDD for data differentiation is described using Verilog simulated waveforms illustrated in Fig. 6.1.3. Secondly, adaptive delay control of the CCDD as well as DFCA to enable false lock free downward frequency capture is described.

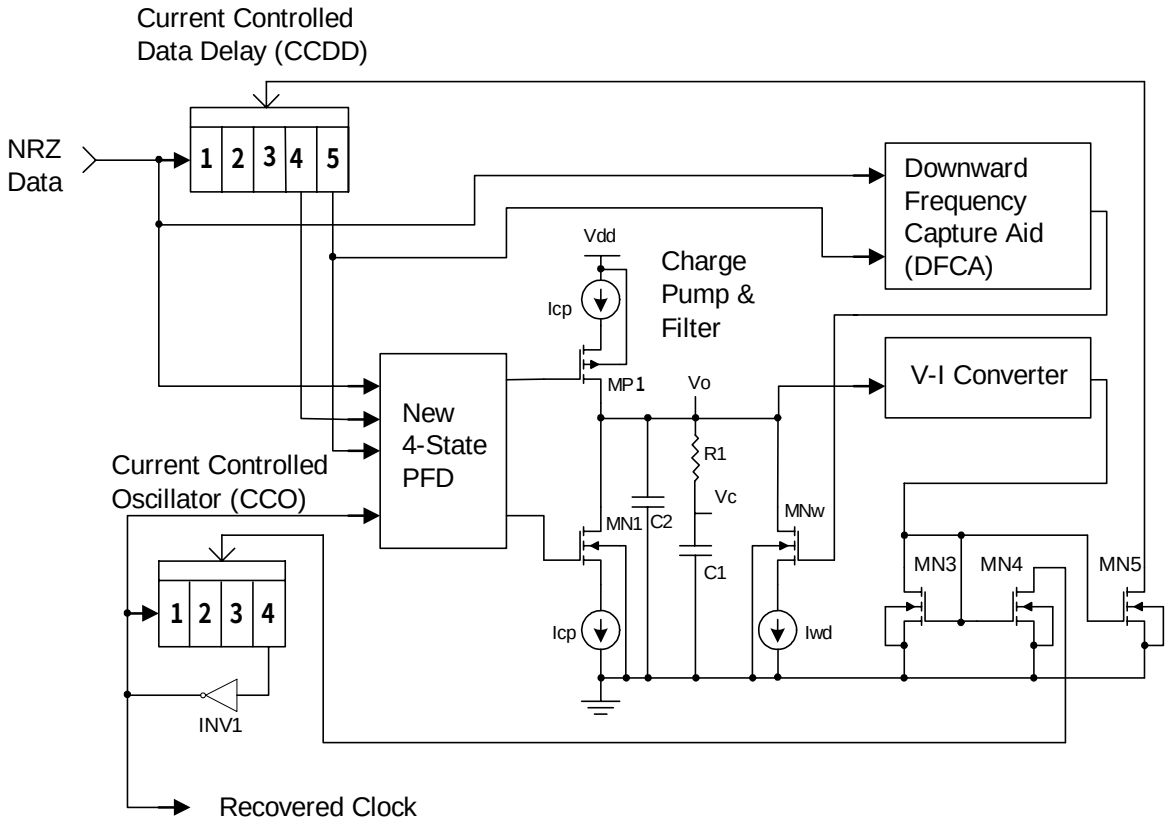



Fig. 6.1.1 Block Diagram of CDR for Narrow Variable bit Rate

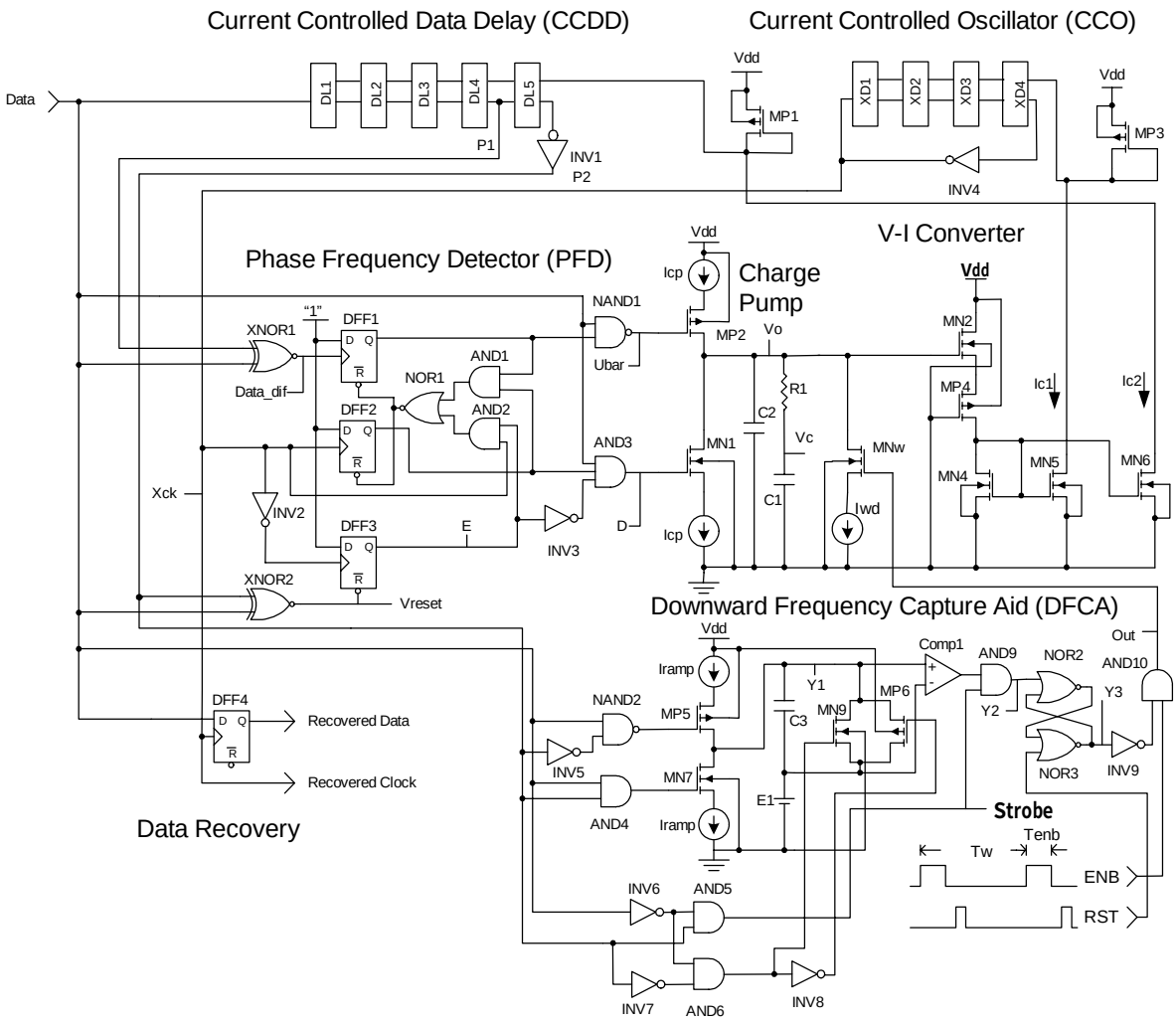



Fig. 6.1.2 Circuit of CDR for Narrow Variable bit Rate

### 6.2.1 Adaptive Data Delay and Downward Frequency Capture Aid

The delay time for data differentiation t1 in Fig. 3.5 plays a very important role in the PFD's operation. For fixed bit rate application, t1 should be set 0.8Tb >= t1 >= 0.5Tb. Considering the prevention for false lock, most optimum point for t1 is 0.6Tb. In case of variable bit rate application, it is very difficult to maintain the condition directly fit to the varying bit rate. One solution is the indirect setting in which the data delay and CCO consist of the same delay elements, and the delay time is controlled by the same value of current. Even in this scheme, false lock occurs in downward frequency capture. The detail and countermeasure for the false lock will be explained next.

As an example, if the PLL is locked at certain bit rate under data pattern of repetition of “10101110010”, then abruptly bit rate is changed to a half of bit rate.

In this condition CCO still maintains the same oscillation frequency, and t1 becomes smaller than half of new 1 bit interval time. Therefore PFD recognizes that there are other data transition missing, and maintains the lock as if the data were to be “11001100111111100001100”. To prevent this type of false lock, downward frequency capture aid is required. Using Fig. 6.1.2 and Fig. 6.1.3, the function of Downward Frequency Capture Aid (DFCA) will be explained next.

In Fig. 6.1.2, CCO and CCDD consist of same delay element, and controlled by the same current Ic1=Ic2 from V-I Converter. CCO consists of 4 stages of inverted type delay elements. At locked state, the delay time of each delay element is 0.125Tb, and the delay time of 4 stages is 0.5Tb in total.

CCDD consists of 5 stages of delay element in total, and is tapped at 4th stage P1 and 5th stage P2. Therefore, the delay time of P1(t1) and P2(t2) is t1 = 0.5Tb and t2 = 0.625Tb respectively at locked state.

In DFCA in Fig. 6.1.2, there is a charge pump circuit, Iramp, MP5, MN7, C3 and E1. C3 is charged up during t2 when Data is high and P2 is low by NAND2 and INV5, and discharged down during Tb - t2 when Data is high and P2 is high by AND4. Thus, C3 is charged up during interval time of,

$$t2 = 0.625Tb,$$

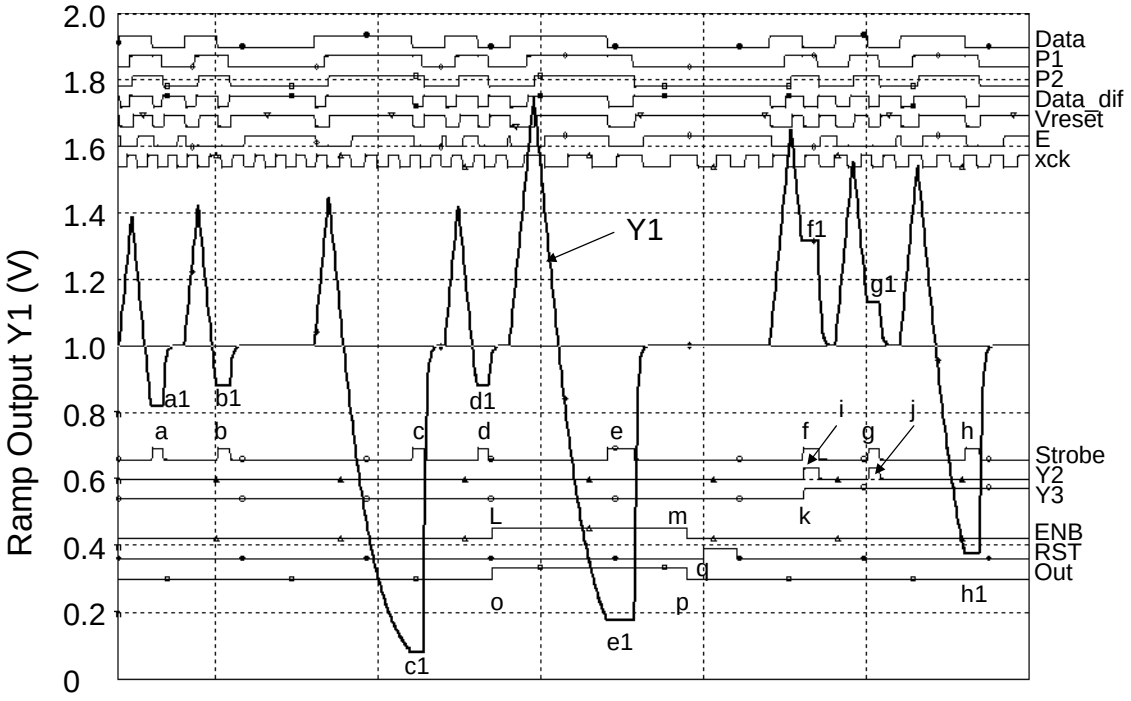



Fig. 6.1.3 Waveforms of Downward Frequency Capture Aid (DFCA)

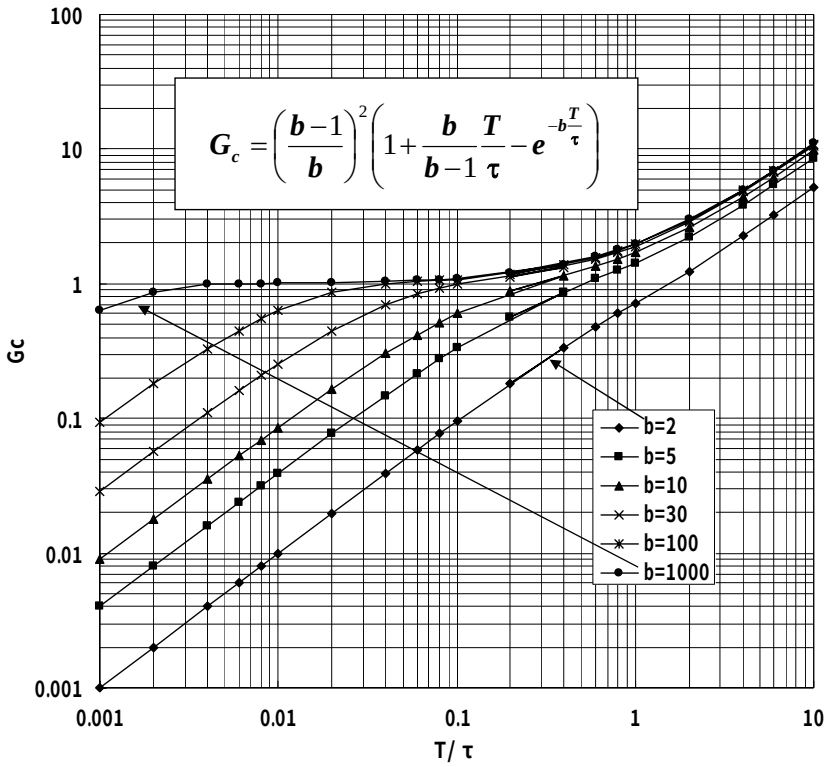



Fig. 6.1.4 Gain coefficient Gc

and discharged down during that of,

$$Tb - t2 = 0.375Tb.$$

Charge and discharge current are set in the same Iramp.

The circuit conducts very similar action to the dual throw A to D converter. Therefore, at the end of Data is high, final voltage of C3 over the ground level Y1, which is started from E1, is higher than E1 at locked state as shown in f1 and g1 in Fig. 6.1.3.

Conversely, if the CCO frequency is higher than locked state, Ic1 and Ic2 are high and t2 becomes small. Therefore the final voltage Y1 becomes smaller than E1 as shown a1 and b1 in Fig. 6.1.3. Level of Y1 is detected by comparator comp1. Thus, the voltage at the end of high level of Data indicates the frequency of CCO.

However, in NRZ data, single 1 bit such as “0100” does not always come. So, this state must be watched in certain interval time Tw like a watch dog. This function will be explained next.

During Data is low and P2 is high, strobe pulse Strobe is generated by INV6 and AND5. If the Y1 is higher than E1, R-S flip-flop (FF) NOR2 and NOR3 is set to “1” by the Strobe via AND9. Then Y1 is reset to E1 by INV5, AND6, INV8 and transmission gate MN9, MP6. If the output of R-S FF, Y3, is set to “1”, the output of AND10 is maintained low by INV9. Contrary, if Y3 is low, in another word, Y2 is low, which means CCO frequency is high, the Vo of Charge Pump circuit is discharged by MN7, Iwd, and AND10 while enable pulse ENB is high, after that, RS-FF is reset by RST. Thus, a kind of watch dog action is done by the DFCA during certain interval time Tw, which is 16 or 32 bit time.

In Fig. 6.1.3, a to h are waveform of Strobe. a, b, d, f and g are corresponding to Single “1” bit. Voltage of Y1, a1, b1 and d1 is lower than E1 1 volt. Therefore Y2 and Y3 is low. When ENB is high during l-m, Out becomes high during o-p, the Vo is discharged by MN7 and Iwd. RS-FF is reset by RST at q. Then next cycle Tw of watch dog begins. As the result of discharge, Vo becomes smaller, and t2 becomes larger, then f1, g1 becomes higher than E1, then Y3 becomes high at k. Thus, DFCA functions as a downward frequency capture aid.

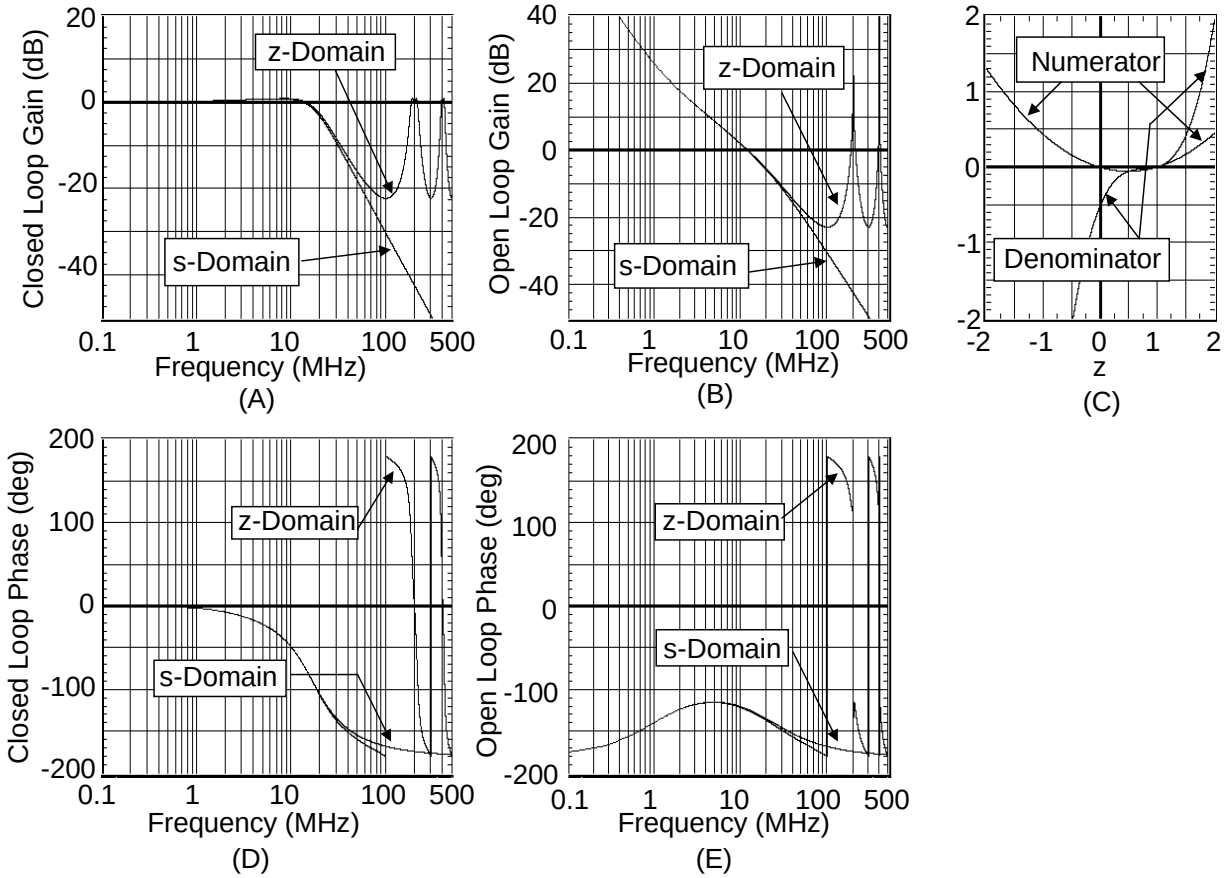



Fig. 6.1.5 z-Domain Analysis, System is stable.
T = 5ns (200Mbps), d = 1, Icp = 400uA,
R1 = 1.5K, C1 = 100pF, C2 = 5pF
(b = 21, $\tau$ = 150ns), K0=150MHz/V

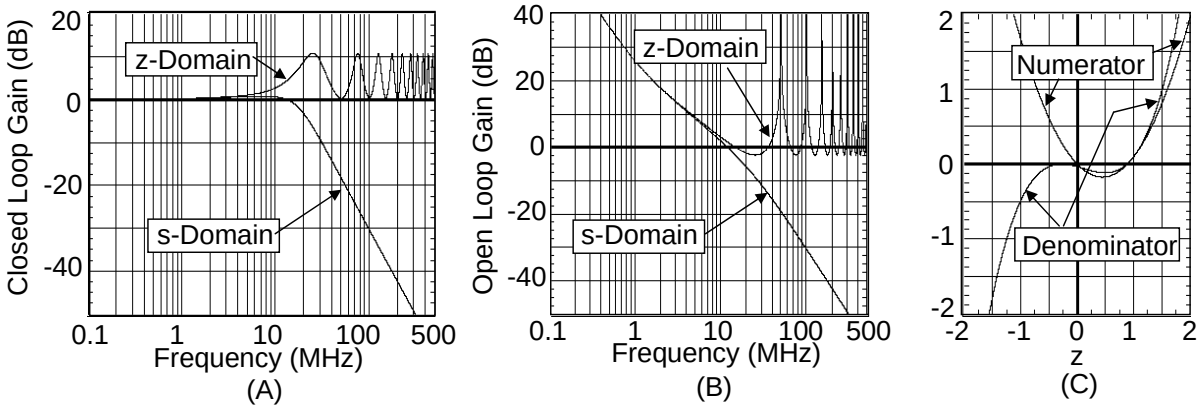



Fig. 6.1.6 z-Domain Analysis, System is stable.
T = 20ns (50Mbps), d = 1, Icp = 400uA,
R1 = 1.5K, C1 = 100pF, C2 = 5pF
(b = 21, $\tau$ = 150ns), K0=150MHz/V

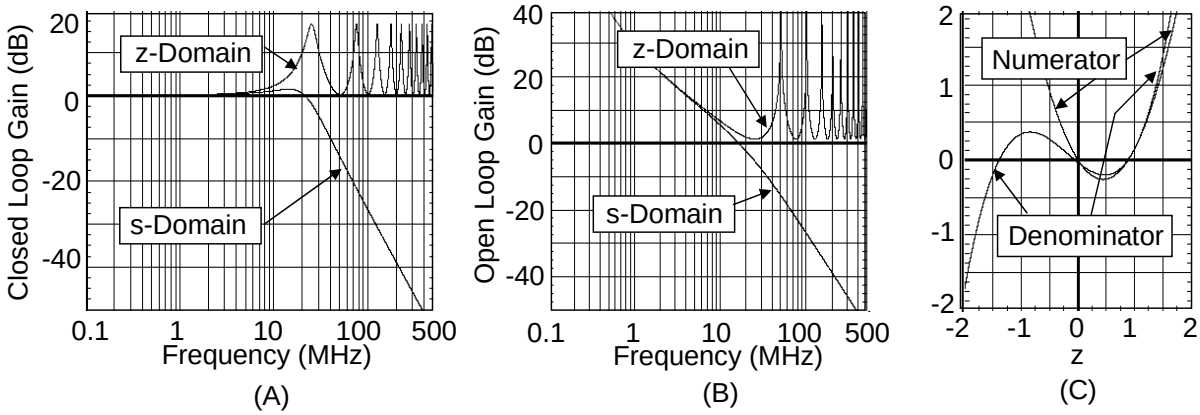



Fig. 6.1.7 z-Domain Analysis, System is unstable.
T=20ns (50Mbps), d = 1, Icp = 600uA,
R1 = 1.5K, C1 = 100pF, C2 = 5pF
(b = 21, $\tau$ = 150ns), K0=150MHz/V

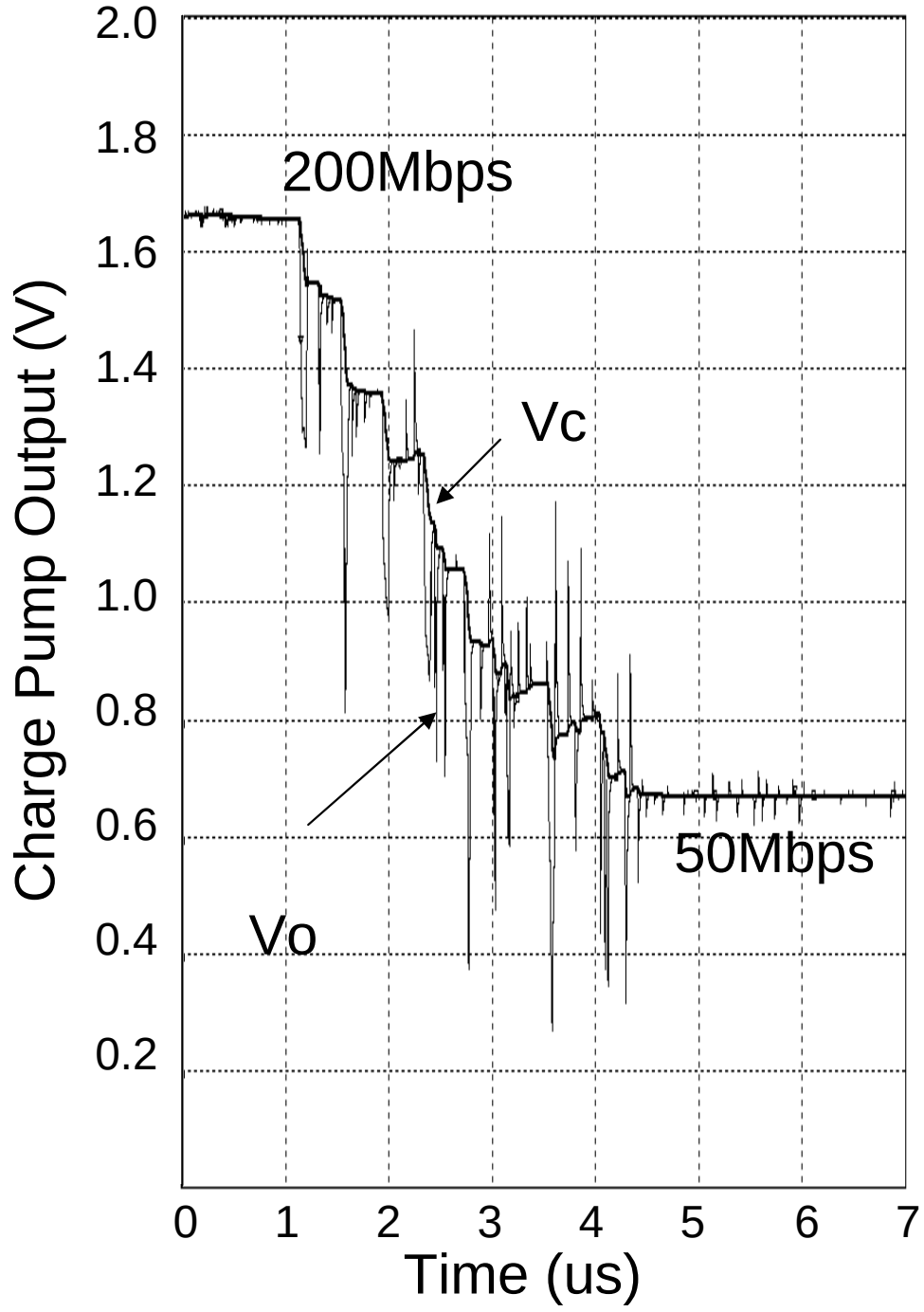



Fig. 6.1.8 bit Rate change from 200Mbps down to 50Mbps
Icp=400uA, R1=1.5K, C1=100pF, C2=5pF, Iw=300uA
Iramp=500uA, C3=5pF, E1=1V, Tw=400ns, Tenb=60ns

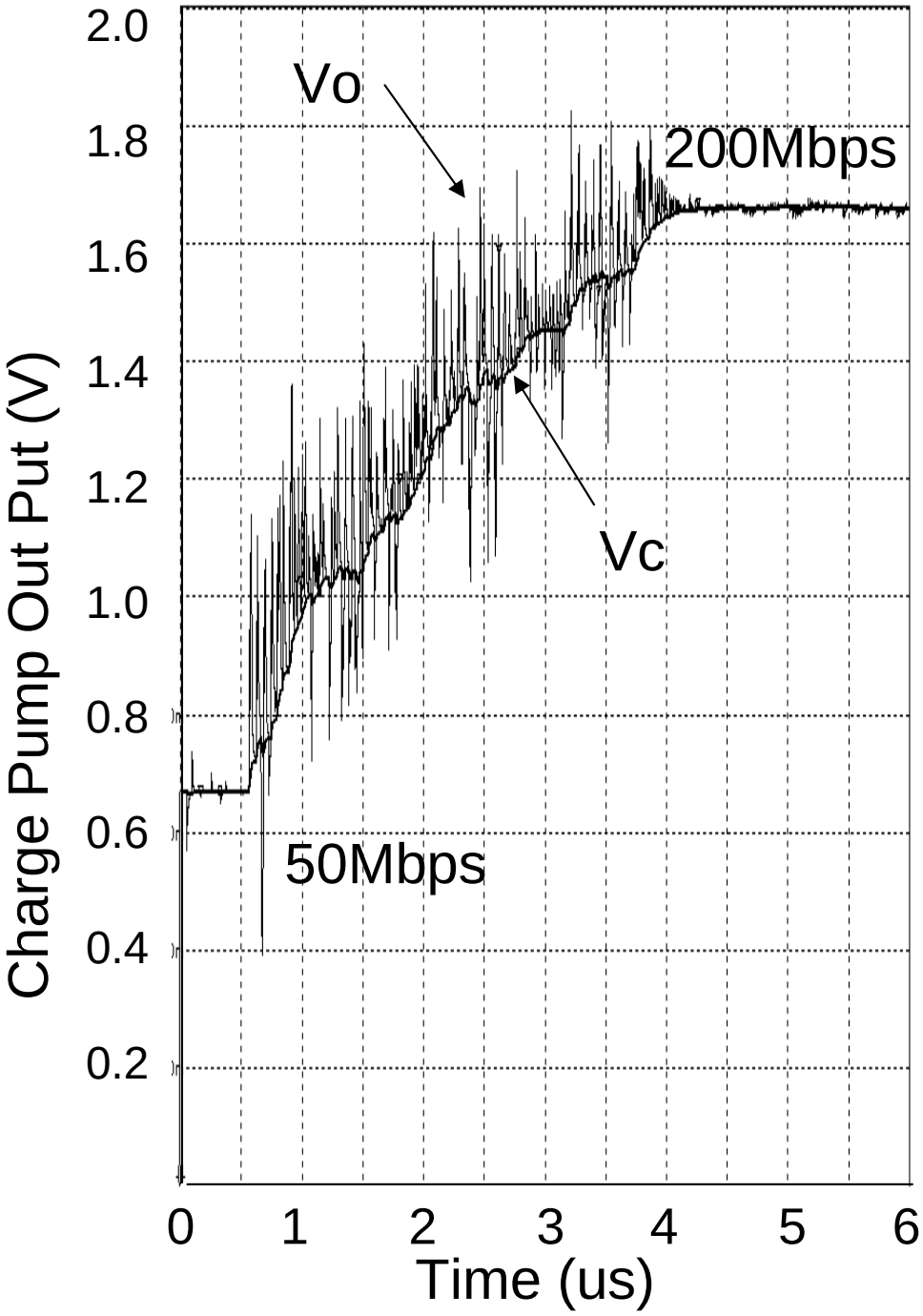



Fig. 6.1.9 bit Rate change from 50Mbps up to 200Mbps
Icp=400uA, R1=1.5K, C1=100pF, C2=5pF, Iw=300uA
Iramp=500uA, C3=5pF, E1=1V, Tw=400ns, Tenb=60ns

## 6.2.2 Results of SPICE Simulation

SPICE simulation was made on the circuit shown in Fig. 6.1.2 under flat level of 550 transistors, 0.35um CMOS and level 3 model. In repetition of SPICE simulation it becomes apparent that, in wide bit rate operation, the charge pump constant such as charge current Icp, filter constant R1, C1 and C2 are very important for smooth frequency capture and stable operation in locked state. Therefore, z-Domain analysis was made. The detail of z-Domain analysis is described in Chapter 7.

A simulator was also made for (7.8) to (7.11) of Chapter 7 in computing complex number. As a result it becomes apparent that the special attention should be paid to the gain coefficient Gc as shown in (7.9) as a part of open loop gain (7.8). Fig. 6.1.4 shows the Gc as a function of $T/\tau$ in parameter b. b and $\tau$ are defined as

$$b = \frac{C_1 + C_2}{C_2},$$
$$\tau = R_1 C_1 . \qquad (6.1)$$

To prevent overloading of CCO, and to reduce noise and jitter, C2 has a very effective filtering action in the charge pump circuit. However, the total PLL system becomes the third order loop by this scheme.

As seen in Fig. 6.1.4, if C2 is set in large value in order to make large filtering effect, b becomes small. In high bit rate, T is small. Therefore, in small b, if the $T/\tau$ is small, Gc becomes very small. Thus the open loop gain becomes very small, and the frequency capture becomes very hard. Therefore, $\tau$ should be set small as possible in trade off with jitter or noise. Conversely, in low bit rate area, if $\tau$ is small, stability issue will arise. This issue will be explained next.

Fig. 6.1.5, Fig. 6.1.6 and Fig. 6.1.7 show the result of z-Domain analysis. Fig. 6.1.5 (B) shows open loop gain of (7.7) at T = 5ns (200Mbps), d=1, Icp = 400uA, R1 = 1.5K, C1 = 100pF, C2 = 5pF, CCO gain as VCO Ko = 150MHz/V (b = 21, $\tau$ = 150ns), and (E) shows its phase. Phase less than -180 degree is shown by resetting to +180 degree only for display purposes to the graph. d is the transition density, so it is 0.5 because the circuit in Fig. 6.1.2 treats leading edge only comparison. However, the output of charge pump is fed back to data

delay, so open loop phase gain becomes double. Therefore d is set to 1.0 in maximum density of data, a repetition of “1010”, for stability criteria.

Thus, Fig. 6.1.5 (B) and (E) show Bode diagram in comparison with s-Domain analysis. Closed loop gain (10) is shown in Fig. 6.1.5 (A) and (D).

Fig. 6.1.5 (C) shows the zeros and pole(s) of the closed loop gain (7.10) by sweeping z in real axis from -2 to 2. The zero-cross points of numerator of (7.10), 2nd order curve in Fig. 6.1.5 (C), show the zeros of closed loop gain. The zero-cross point(s) of denominator of (7.10), 3rd order curve in Fig. 6.1.5 (C), show the pole(s) of closed loop gain. The system is stable if the pole(s) and zeros reside within the unit circle of z plane. As seen in Fig. 6.1.5 (C), the system is stable in T=5ns (200Mbps).

Fig. 6.1.6 shows the case of T = 20ns (50Mbps), d=1, Icp = 400uA, R1 = 1.5K, C1 = 100pF, C2 = 5pF, CCO gain as VCO Ko = 150MHz/V (b = 21, $\tau$ = 150ns). As seen in Fig. 6.1.6 the system is also stable in T=20ns, 50Mbps.

However, Fig. 6.1.7 show the case that charge pump current is increased from 400uA to 600uA comparing with Fig. 6.1.6. As seen in Fig. 6.1.7 (C), a pole, zero-cross point of denominator, is less than -1. Therefore the system becomes unstable. This may be also clear in Fig. 6.1.7 (B) and (A). However, no such information can be attained from the s-Domain curves of Fig. 6.1.5 to 6.1.7. Thus, the z-Domain analysis is very useful for selecting the filter constants and charge pump current, and estimation of stability.

Fig. 6.1.8 shows the results of SPICE simulation of bit rate change from 200Mbps to 50Mbps. Fig. 6.1.9 shows the bit rate change from 50Mbps to 200Mbps. As shown in the figures, false lock free robust operation was verified in 4 times wide bit rate change.

## 6.2.3 Conclusion of Narrow Variable bit Rate

A new PFD with adaptive delay time control for data delay and Downward Frequency Capture Aid have been presented, and the combination of schemes as an adaptive PFD have been demonstrated to be effective for achieving wide and false-lock-free frequency capture and phase lock for variable bit rate or multiple different bit rate transmitters.

Wide capture range on incoming data bit rate of 50Mbps to 200Mbps, low to high ratio of 4, has been verified by SPICE simulation. The new PFD is an effectively 4-state PFD, therefore it inherits the features of 3-state PFD such as frequency detection and low jitter characteristics even for NRZ data.

## 6.3 CDR for Wide Variable bit Rate

In wide variable bit rate application, it is very difficult to make a smooth frequency capture and stable lock-in under fixed constants of filter and charge pump current. High bit rate side, the loop gain decreases, and low bit rate side, stability issue occurs. To coupe with these issues, special care should be taken in selecting filter time constant and charge pump current. To make more rapid and false-lock-free frequency capture, full digital down- and upward frequency capture aid, and time slot control are also introduced.

Fig. 6.2.1 presents the block diagram of CDR for Wide Variable bit Rate.

The system consists of a current-controlled data delay (CCDD), New 4-State PFD, Charge Pump, V-I converter1, Current Controlled Oscillator (CCO), V-I ConverterI2, Downward Frequency Capture Aid (DFCA) and Upward Frequency Capture Aid (UFCA).

V_I Converter1 converts the output voltage Vo to the current, and this current controls the CCO, V-I Converter2 converts the voltage of smoothed voltage Vc to the current, and this current controls the CCDD. The input of V-I Converter2 may be connected to Vo. The difference will be discussed later.

In frequency capture stage, DFCA and UFCA provide additional charging current to the filter by MPw or MNw. Fig. 6.2.2 and Fig. 6.2.3 show the circuit of DFCA and UFCA.

Fig. 6.2.4 shows the circuit of CDR for Wide Variable bit Rate. In this case, inputs of V-I Converter1 and V-I Converter2 are unified and connected to Vo.

Detailed operation of this CDR system is described in three parts. Firstly, the 4-state PFD that relies on the CCDD for data differentiation is described using Verilog simulated waveforms under phase-locked and near phase-locked conditions illustrated in Fig. 6.2.5 and Fig. 6.2.6. Secondly, adaptive delay control of the CCDD as well as DFCA and UFCA as well as time slot control to enable false lock free and stable operation is described. Thirdly, a z-Domain analysis is described for stability issue.

Waveforms shown in Fig. 6.2.5 are different in small portion from Fig. 3.5 of Chapter 3, i.e. time slot control is added as waveform F. As seen in Fig. 6.2.5 there is no difference with Fig. 3.5 in near phase matched or phase matched state.

However, in frequency capture range, larger width down- or up-pulses are generated by the time slot control F as shown in Fig. 6.2.6.

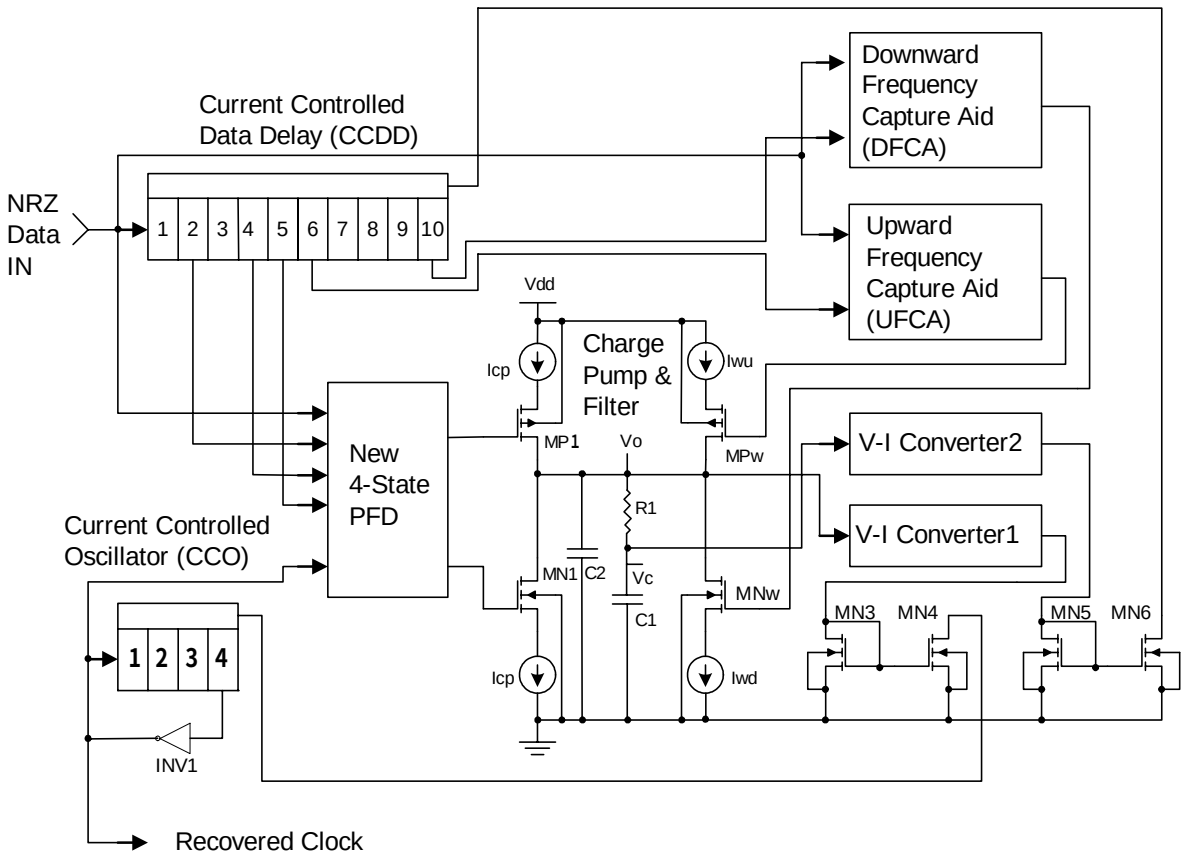



Fig. 6.2.1 Block Diagram of CDR for Wide Variable bit Rate

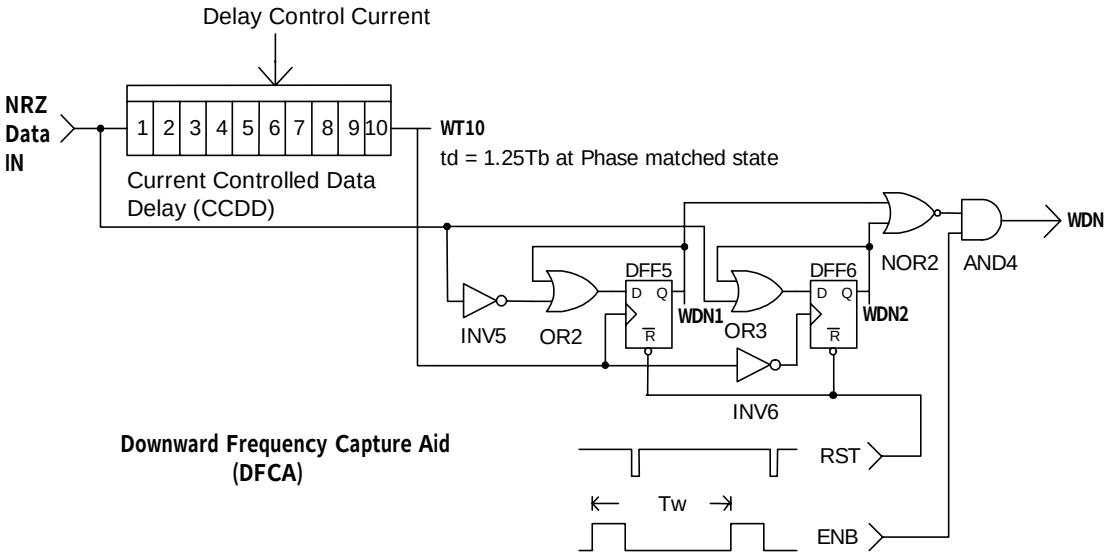



Fig. 6.2.2 Downward Frequency Capture Aid

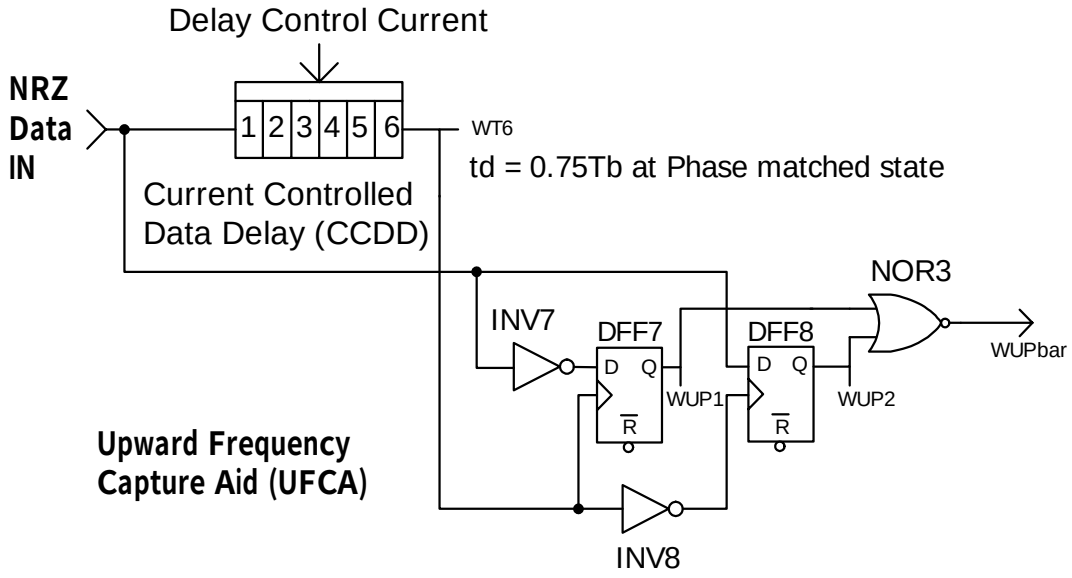



Fig. 6.2.3 Upward Frequency Capture Aid

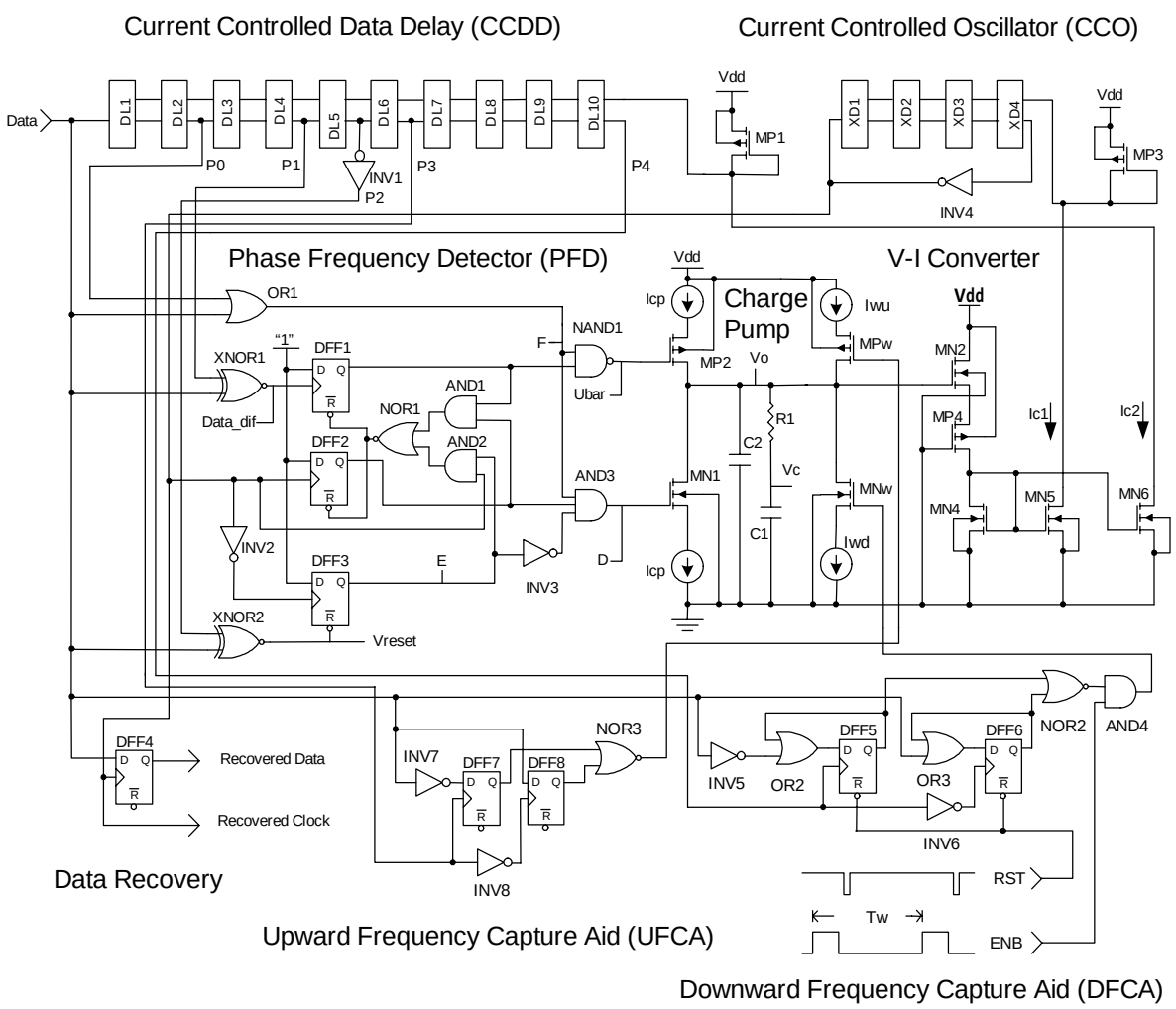



Fig. 6.2.4 CDR for Wide Variable bit Rate, Circuit Diagram

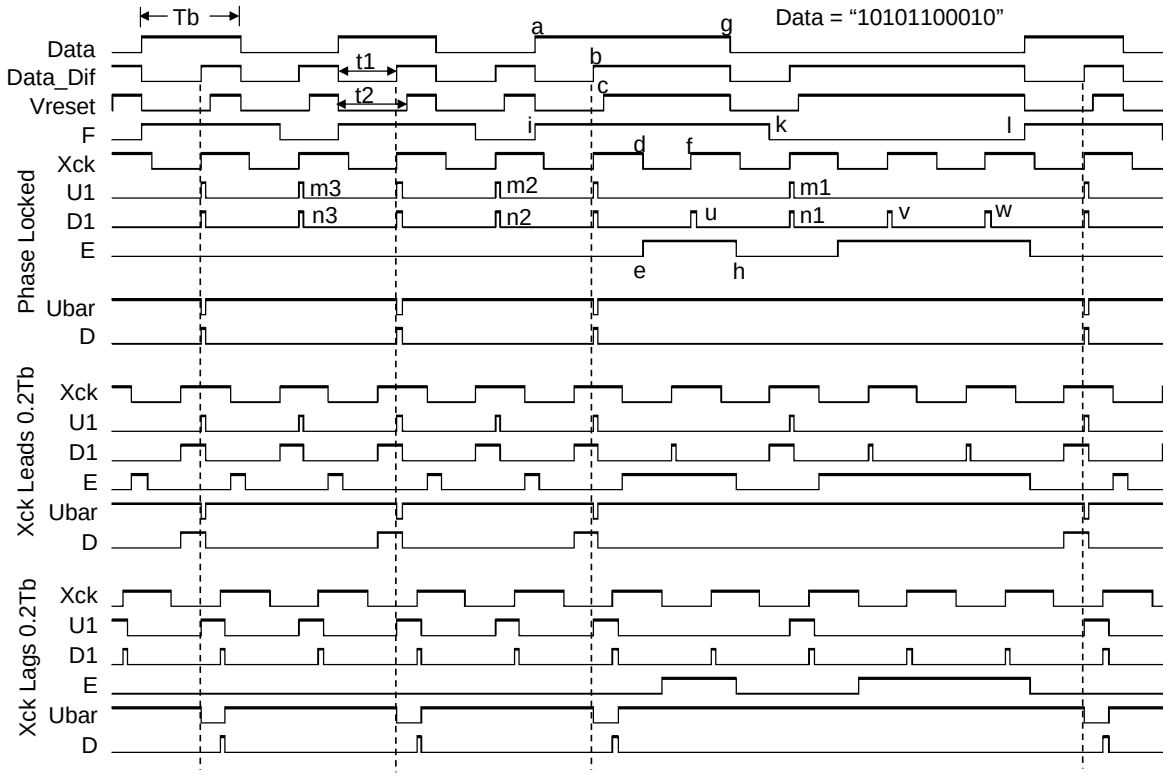



Fig. 6.2.5 Waveforms of PFD, t1 = 0.6Tb,
Phase locked, Xck leads 0.2Tb and lags 0.2Tb

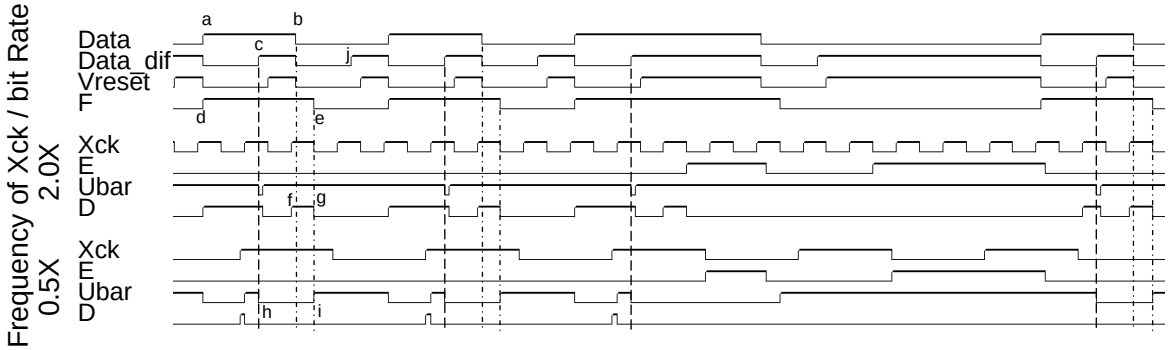



Fig. 6.2.6 Function of frequency detector-Effect of Time Slot Control “F”,
t1 = 0.6Tb
Upper; Frequency of Xck is twice (2.0X),
Lower; a half (0.5X) of data bit rate

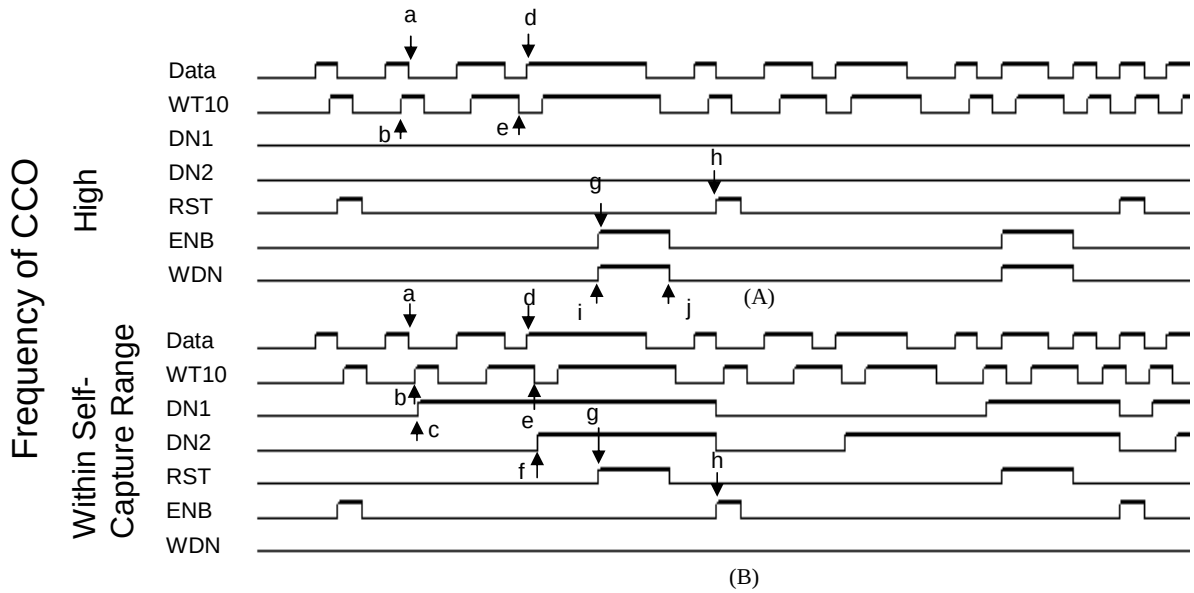



Fig. 6.2.7 Waveforms of Downward Frequency Capture Aid

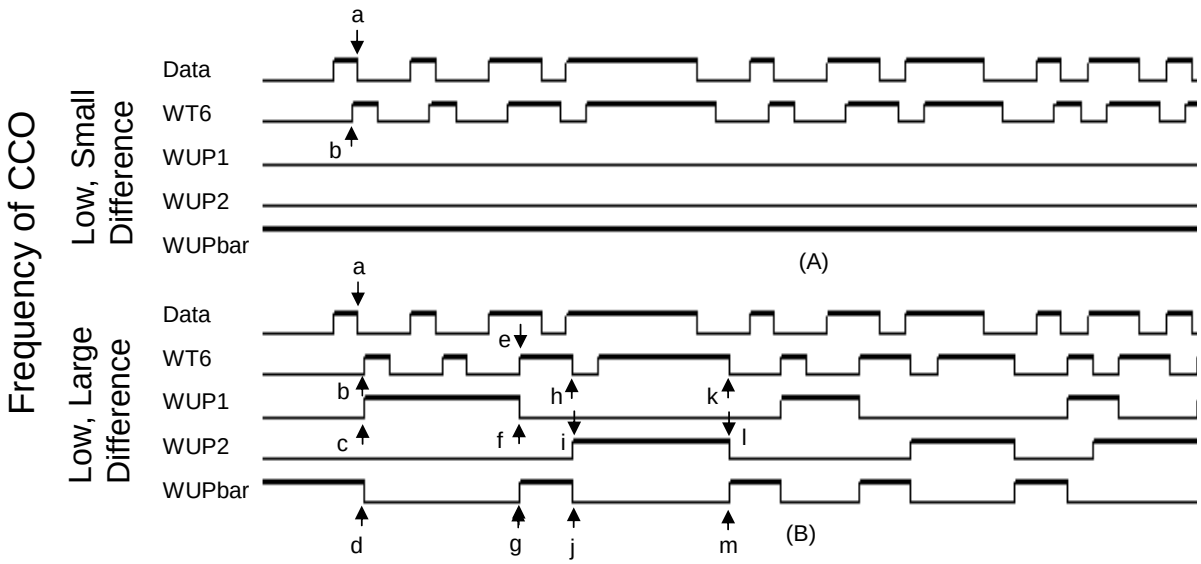



Fig. 6.2.8 Waveforms of Upward Frequency Capture Aid

## 6.3.1 Downward and Upward Frequency Capture Aid

In Fig. 6.2.4 full digital DFCA and UFCA are introduced.
In Fig. 6.2.4, CCO and CCDD consist of same delay element, and controlled by the same current Ic1=Ic2 from V-I Converter. CCO consists of 4 stages of inverted type delay elements. At locked state, the delay time of each delay element is 0.125Tb, and the delay time of 4 stages is 0.5Tb in total. CCDD consists of 10 stages of delay element in total, and is tapped at 2nd stage P0, 4th stage P1, 5th stage P2, 6th stage P3 and 10th stage P4. Therefore, the delay time of P0(t0), P1(t1), P2(t2), P3(t3) and P4(t4) is t0 = 0.25Tb, t1 = 0.5Tb, t2 = 0.625Tb, t3 = 0.75Tb and t4 = 1.25Tb respectively at locked state.

In order to clarify the DFCA and UFCA in relation to delay time of CCDD, Fig. 6.2.2 and Fig. 6.2.3 are extracted from Fig. 6.2.4.

In DFCA in Fig. 6.2.2 and Fig. 6.2.4, there are two DFFs, DFF5 and DFF6. DFF5 is triggered by P4(WT10) and DFF6 is triggered by inverted P4 by INV6. Logical OR is taken by OR2 on the signals of inverted Data by INV5 and output of DFF5 itself, and this signal is fed to D input of DFF5. Thus, if the output of DFF5 becomes high once, this state is self stored at next rising edge of Data until RST becomes low.

Conversely, logical OR is taken on Data and output of DFF6, then the signal is fed to data input D of DFF6. Likewise, if the output of DFF6 becomes high once, this state is self stored at next falling edge of Data until RST becomes low.

As seen in lower side of Fig. 6.2.7 (B), if the frequency of CCO is low, the delay time of CCDD is large, leading edge b of WT10, which is the waveform of P4, comes later than trailing edge a of Data. Therefore, DFF5 is triggered at b, and reads inverted low level of Data, “1” at D input, and output of DFF5 DN1 becomes high level at c. DFF6 is triggered at trailing edge of e, and the e comes later the leading edge of Data d, so the output of DFF6 DN2 becomes high at f.

Thus, if the frequency of CCO is low, the output of DFF5 or DFF6 becomes high, then output of NOR2 is low. Conversely, if the frequency of CCO is high, as seen in Fig. 6.2.7 (A), leading edge of WT10 b or trailing edge of WT10 e comes earlier than trailing edge of Data a or leading edge of Data d. So the output of DFF5 or DFF6 remains in low level, then the output of NOR2 is high.

Thus, this DFCA detects both side of single 1bit of “1” or “0”. Comparing with Fig. 6.1.2, DFCA in Fig. 6.1.2 detects single 1bit of “1” only. Therefore, DFCA in Fig. 6.2.4 takes more efficient function of watch dog.

In NRZ data stream, single 1 bit of “1” or “0” such as “001000” or “110111” is not always comes. Therefore, it must be watched in certain period, then decision should be made. This will be explained next.

In Fig. 6.2.2 and Fig. 6.2.4, enable pulse of watch dog ENB is supplied in interval of Tw. In case of frequency high in CCO, and if the ENB becomes high, output of AND4 becomes high, then output of Charge Pump Vo is discharged by MNw and Iwd, and frequency of CCO becomes lower.

Conversely, if the CCO frequency is low, the output of OR2 is low as explained, no discharge action is activated. After enable pulse ENB, the reset pulse RST is supplied, and DFF5 and DFF6 are reset.

In moderate capture range of bit rate such as two or four times of bit rate, upward frequency capture aid is not necessary for proposed new PFD, because it has a function of a frequency detector. However, in larger capture range under fixed time constant of charge pump and filter, upward frequency capture aid is necessary. Next, it will be explained.

In Upward Frequency Capture Aid (UFCA) in Fig. 6.2.3 and Fig. 6.2.4, there are two DFFs, DFF7 and DFF8, are used. DFF7 is triggered by P3 (WT6), and DFF8 is triggered by inverted P3 by INV8. Inverted Data by INV7 is fed to input D of DFF7, and Data is fed to input D of DFF8.

As seen in Fig. 6.2.8 (B), if the frequency of CCO is very low, the delay time of CCDD is large, so the leading edge of P3, waveform WT6 b comes after trailing edge of Data a. Hence, output of DFF7 WUP1 becomes high at c, and becomes low at f which is corresponding next Data high and leading edge of WT6 e.

Likewise, DFF8 becomes high at trailing edge of WT6 h while Data is high, and becomes low at trailing edge of WT6 k while Data is low. Charge pump output Vo is charged-up by NOR3, MPw and Iwu while output of DFF7 or DFF8 is high. Conversely, if the frequency of CCO is low but within self-capture range, as seen in Fig. 6.2.8 (A), nothing is occurred. Thus UFCA acts as an effective upward frequency capture aid.

Thus, DFCA and UFCA act as the frequency capture aid if the frequency of CCO exceed plus 25% or minus 25% of target original clock frequency of data.

Conversely, If the frequency of CCO is inside of +/- 25% of the target frequency, DFCA and UFCA make no action. Therefore, there is a dead zone of +/- 25%. This leads to free self-lock-in of the PFD, and prevents any exaggeration, which may be incurred by the frequency capture aids, in the vicinity of lock-in.

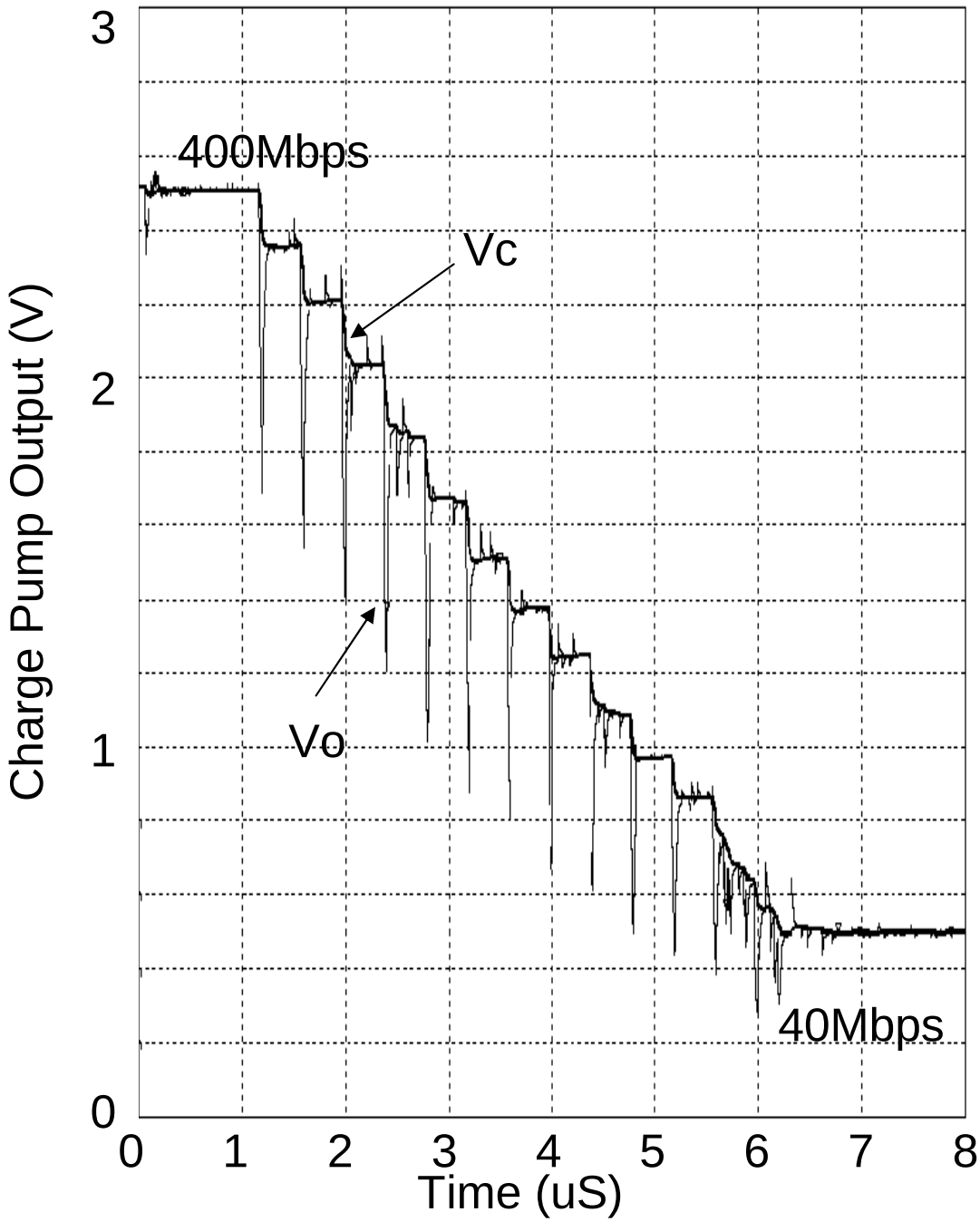



Fig. 6.2.9 bit Rate change from 400Mbps down to 40Mbps
Icp = 600uA, Iwd = 600uA
R1 = 1.5K, C1 = 100pF, C2 = 10pF
Tw = 400ns, Tenb = 60ns

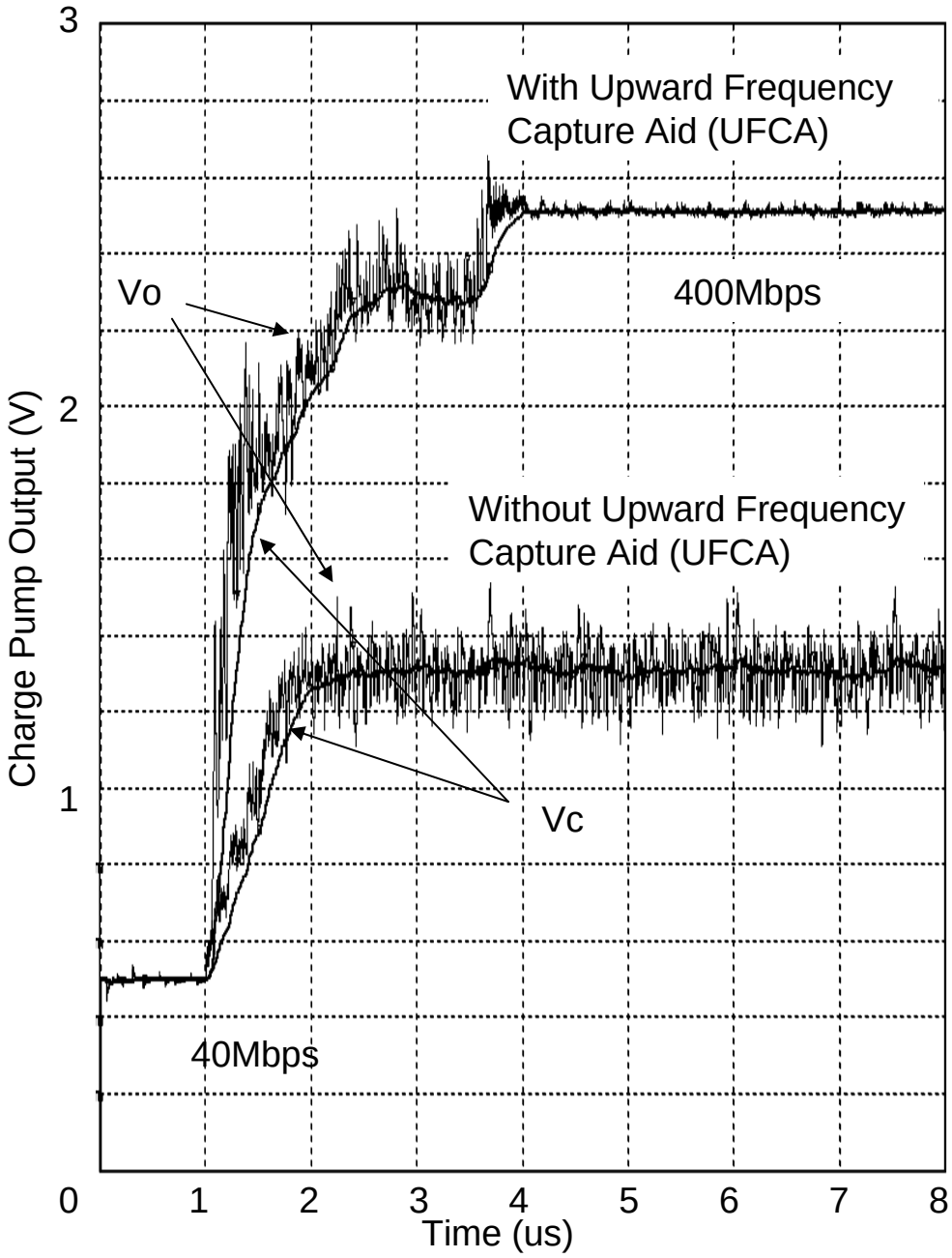



Fig. 6.2.10 bit Rate change from 40Mbps to 400Mbps
Icp = 600uA, Iwd = 600uA
R1 = 1.5K, C1 = 100pF, C2 = 10pF
Tw = 400ns, Tenb = 60ns

## 6.3.2 Results of SPICE Simulation

SPICE simulation was made on the circuit shown in Fig. 6.2.4 under flat level of 600 transistors, 0.35um CMOS and level-3 model, and Charge pump Current Icp = 600uA, R1 =1.5K, C1 = 100pF and c2 =10pF. Fig. 6.2.9 shows the bit rate change from 400Mbps to 40Mbps.
Fig. 6.2.10 shows the bit rate change from 40Mbps to 400Mbps.

As seen in Fig. 6.2.10, case of upward frequency capture, if the UFCA is not applied, system is suspended around 1.3V of charge pump output voltage.

This 1.3V is corresponding to the delay time of P1, 4 stages of CCDD, is nearly equal to the Tb, interval time of 1 bit of input data. This means that the frequency of CCO is half of target frequency. In this region, there is a case that the differentiated data Data_dif, as shown in Fig. 6.2.4, is not properly generated, and this region can not pass through if the charge pump current is low.

It is easier to pass through this region, if the input of V-I Converter2 is connected to Vo in place of Vc.

However, this issue has been overcome by applying UFCA.

As shown in the figures, false lock free robust operation was verified in 1 decade of bit rate change. However, the selection of charge pump current and filter time constants is very critical in wide bit rate application.

## 6.3.3 Charge Pump Current Control

In wide bit rate application, If the charge pump and filter constant are maintained in fixed value, the characteristics such as jitter may not be sufficient enough for the requirements. To cope with the drawbacks, an adaptive charge pump current control was introduced as explained in Chapter 4.4.

Fig. 6.2.9 and Fig. 6.2.10 were taken on the system as shown in Fig. 6.2.4 in fixed charge pump current Icp of 600uA, R1=1.5K, C1=100pF and C2=10pF.
At 400Mbps, jitter peaking curve is shown in Fig. 6.2.11. As seen in Fig. 6.2.11, jitter peaking curve, closed loop gain curve, is the same in s-Domain and z-Domain, and it is a peak of 2dB at 400Mbps.

Fig. 6.3.12 shows the case of 40Mbps. As seen in Fig. 6.2.12, s-Domain and z-Domain curve are different at 40Mbps. Jitter peaking of s-Domain is 2dB and z-Domain is 5dB.

As seen in the figures, jitter-peakings are large. Therefore, adequate loop damping is important. This will be discussed next.

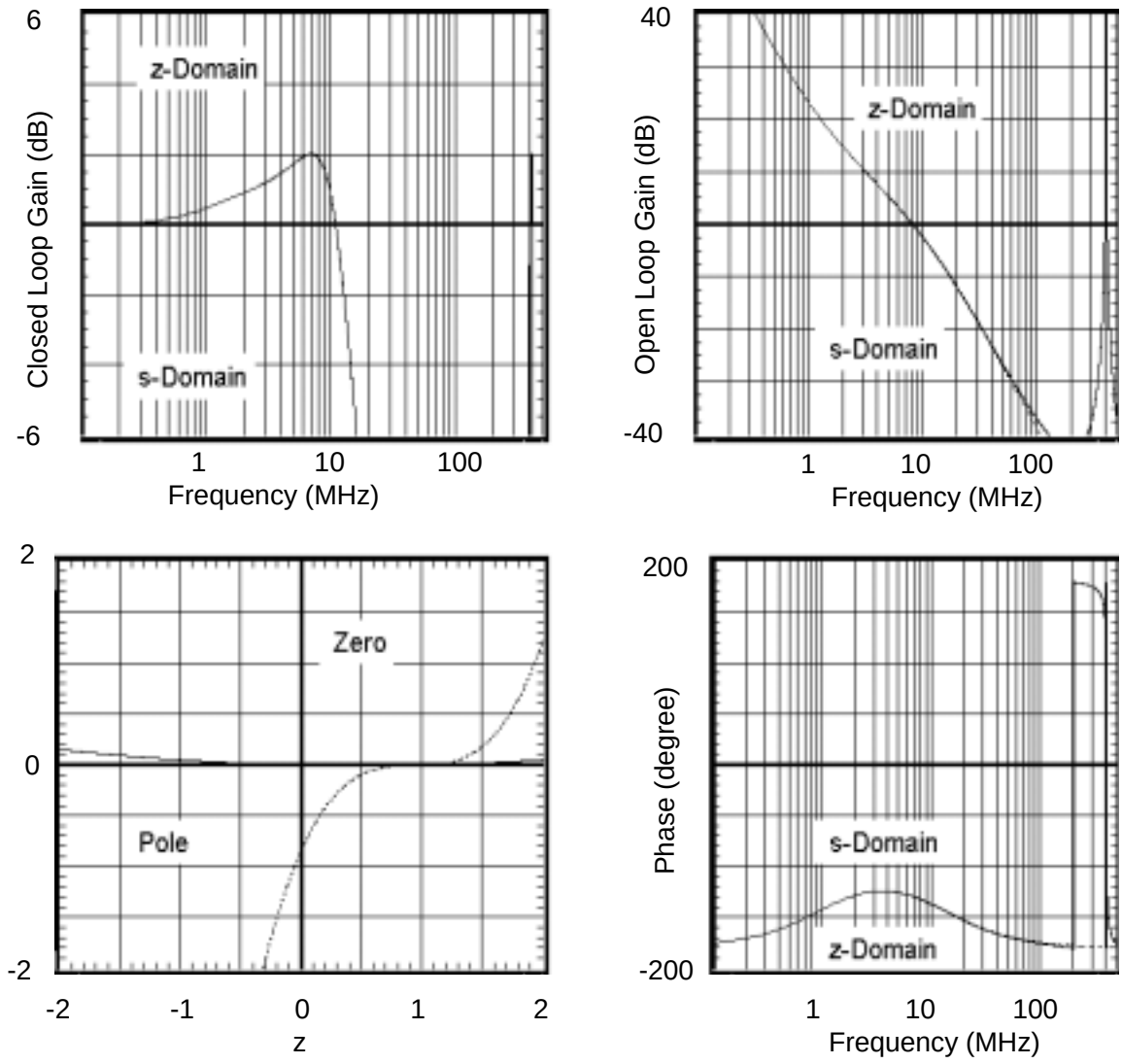



Fig. 6.2.11 z-Domain and s-Domain curve on fixed charge pump current
T = 2.5ns (400Mbps), Icp = 600uA,
R1 = 1.5K, C1 = 100pF, C2 = 10pF, K0=150MHz/V

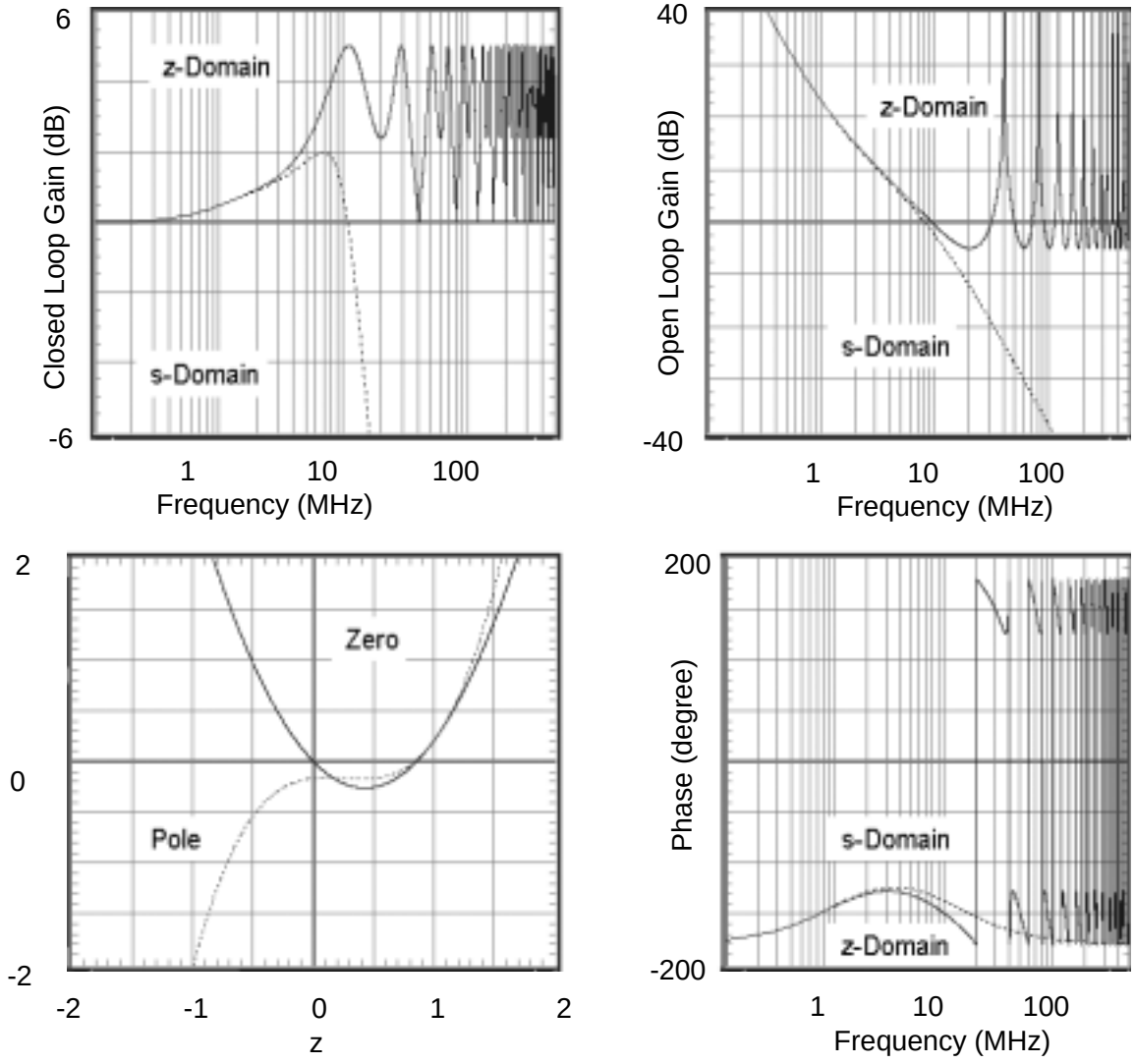



Fig. 6.2.12 z-Domain and s-Domain curve on fixed charge pump current
T = 25ns (40Mbps), Icp = 600uA,
R1 = 1.5K, C1 = 100pF, C2 = 10pF, K0=150MHz/V

## 6.3.4 Damping of PLL Loop

In 2nd order PLL loop, next equations are widely used [10].
In 2nd order loop, in which C2 is zero and b is infinity, the closed loop transfer function of charge pump circuit is written as (6.2).

$$H(s) = \frac{\frac{Icp}{2\pi C1}(R1C1+1)Kvco}{s^2 + \frac{Icp}{2\pi}KvcoR1s + \frac{Icp}{2\pi C1}Kvco} \tag{6.2}$$

Natural frequency and damping factor are also derived.

$$\omega_n = \sqrt{\frac{Icp}{2\pi C1}Kvco} \tag{6.3}$$

$$\xi = \frac{R1}{2}\sqrt{\frac{IcpC1}{2\pi}Kvco} \tag{6.4}$$

Here, Kvco is defined the gain of VCO as angular frequency, radian/V, and not the same as K0 defined in Chapter 7 as Hz/V.

$$Kvco = 2\pi K_0$$

In small C2, hence large b area, (6.4) gives the good insight about damping factor. If the charge pump current is fixed value, there are two ways to increase damping factor $\xi$, increase of C1 or increase of R1.

If C1 is increased in value of 4 times, $\xi$ becomes 2 times, and time constant becomes 4 times, and ripple on charge pump output is decreased. Conversely, if the R1 increased to 2 times, $\xi$ becomes 2 times, time constant becomes 2 times, and the ripple is increased.

Therefore, for application aiming fast lock-in, increase of R1 is effective, and for low jitter application, increase of C1 is effective in trade offs with jitter and lock-in time.

Fig. 6.2.13 shows a low damping case in which the charge pump current Icp is 1.08mA, R1=1K, C1=400pF, and C2=2pF at 400Mbps. As seen in Fig. 6.2.13, the lock-in curve has small hunting, and it does not cease quickly.

Fig. 6.2.14 shows a case of higher damping by increase of C1 4 times.

As seen in Fig. 6.2.14, the damping is in effect even though the lock-in time becomes longer. Fig. 6.2.15 shows the case of increase R1 2 times. As seen in Fig.2.15, damping is in effect in small lock-in time. However, it is clear in comparing Fig. 6.2.14 and 6.2.15 that the ripple becomes larger in case of Fig. 6.2.15.

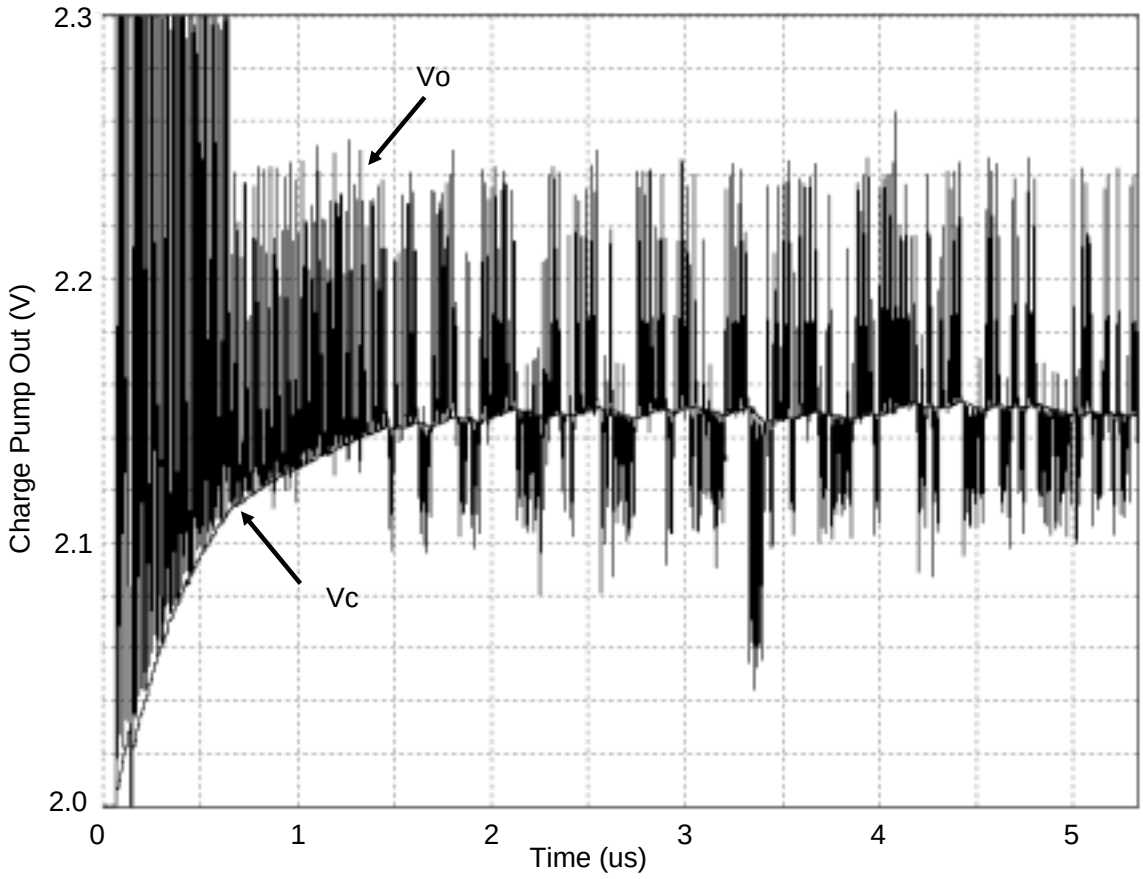



Fig. 6.2.13 Low Damping
R1=1K, C1=400pF, C2=2pF,
I1=200uA, 1:3, Iam=210uA, Iam1=1.08mA, CCDD=Vc

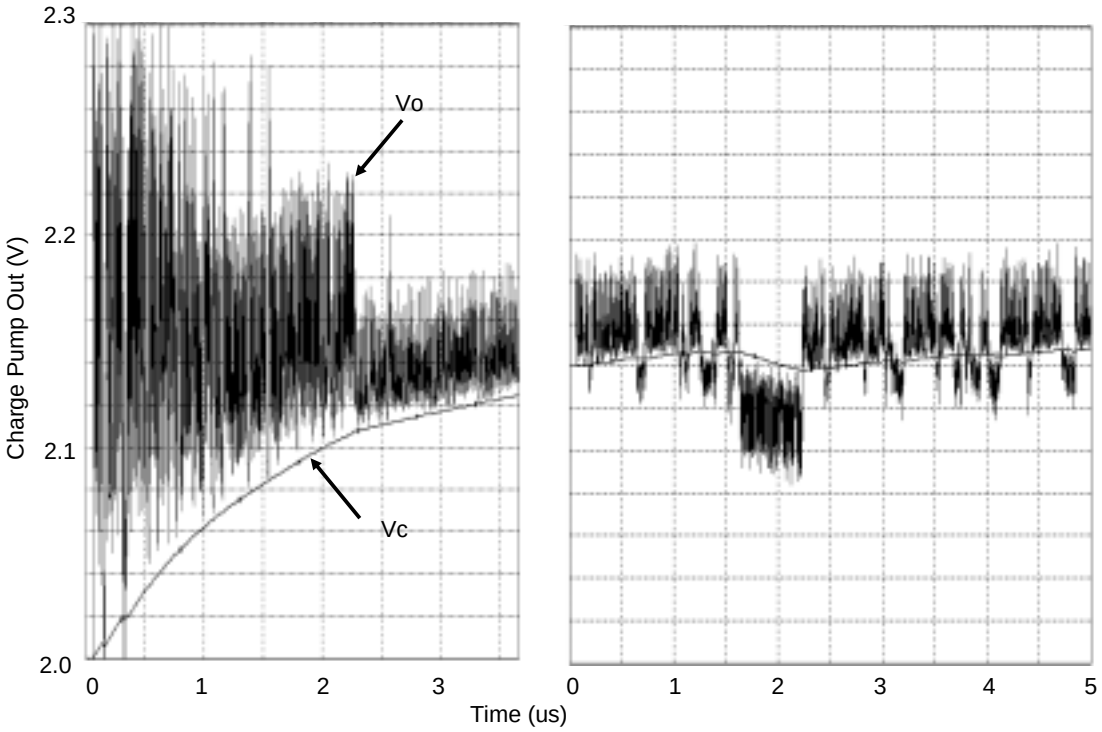



Fig. 6.2.14 Damping by increasing C1, 4 times
R1=1K, C1=1600pF, C2=4pF,
I1=200uA, 1:3, Iam=210uA, Iam1=1.08mA, CCDD=Vc

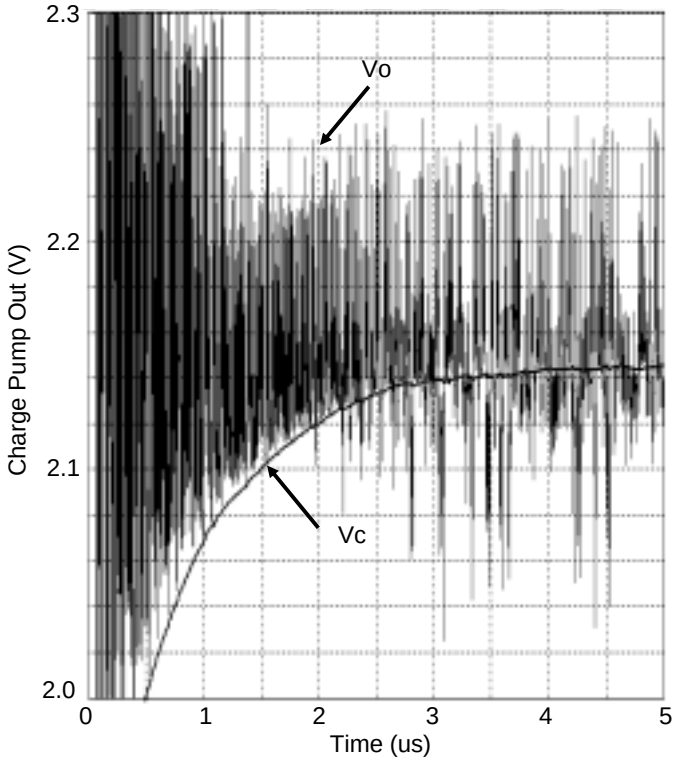



Fig. 6.2.15
Damping by increasing R1,
2 times
R1=2K, C1=400pF, C2=2pF,
I1=200uA, 1:3, Iam=210uA,
Iam1=1.08mA, CCDD=Vc

## 6.3.5 Adaptive Charge Pump Control

In application of low jitter requirement, charge pump circuit of small R1 and large C1 is preferable, because the ripple of charge pump out put is small. In this case, fixed value of charge pump current is usable even in wide variable bit rate application, even though the lock-in time is large.

If the characteristics of rapid lock-in and moderate jitter are required, filter circuit of large R1 and small C1 is mandatory. However, in such application, adaptive charge pump current control as discussed in Chapter 4 can provide more adequate damping and smooth lock-in preventing instability in low bit rate area.

Fig. 6.2.16 is the circuit of CDR for wide variable bit rate application with adaptive charge pump current control. In this circuit, input of V-I converter for CCDD, and Charge Pump Current Control is connected to Vc which is filtered and smoothed output of charge pump by R1 and C1. This makes more stable and robust operation comparing with the direct connection to Vo.

Characteristics of V-I converter and CCO are seen in Fig. 4.8. In Fig. 4.8, current of V-I converter at 400MHz is 220uA (= I1), and at 40MHz 6uA. In Fig. 6.2.16, if I0 is set 50uA and coefficient a is set 4, charge pump current Icp at 400MHz is 1080uA, and Icp at 40MHz is 224uA.

Fig. 6.2.17 and 6.2.18 show the upward bit rate change and downward bit rate change between 40Mbps and 400Mbps, 1 decade. As seen in the figures, rapid and smooth lock-in, adequate damping and small ripple at locked-state were verified. Due to the limitation of computer power, CPU clock of 1.73GHz and 512MB memory, SPICE simulations of 650 transistors were done in 3 parts in upward- or downward bit rate change. It takes 6 hours total in one way, upward bit rate change for example.

Fig. 6.2.19 and 6.2.20 show the z-Domain and s-Domain analysis curve. As seen in Fig. 6.2.20 at 40Mbps, jitter peaking in z-Domain analysis is larger than that of s-Domain, however it is small and stable as shown in Fig. 6.2.18. It takes 1 second for the s- and z Domain analysis.

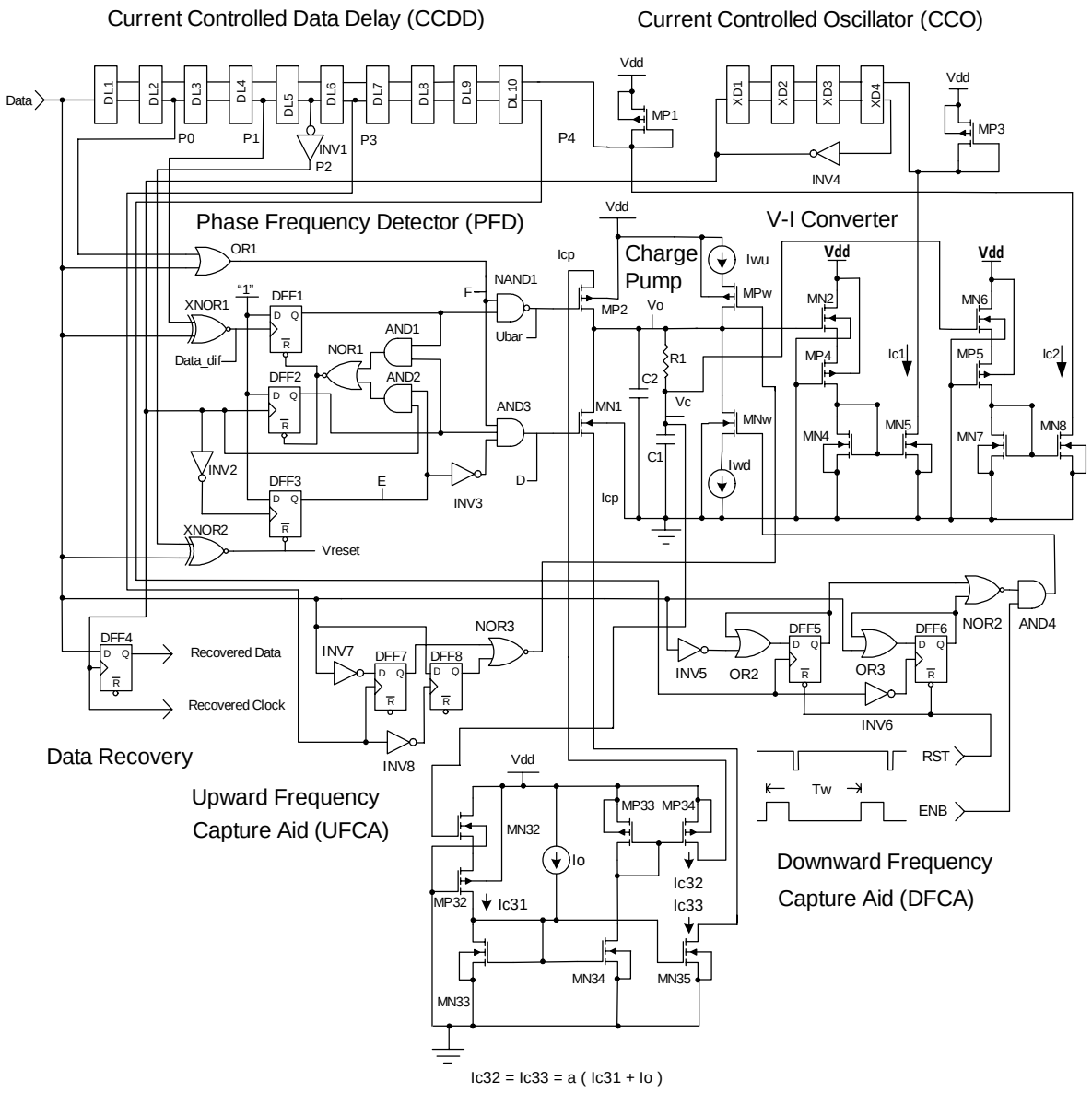



Fig. 6.2.16 Wide Variable bit Rate CDR with Adaptive- Data Delay and Charge Pump Current Control

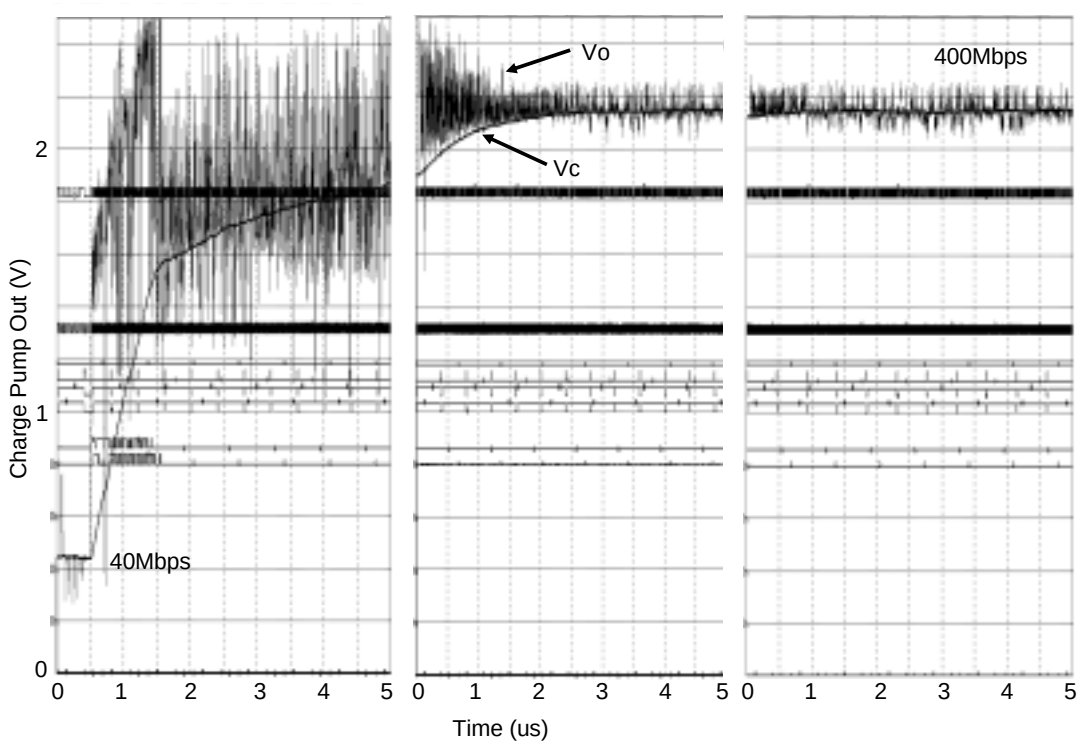



Fig. 6.2.17 CDR with Adaptive Charge Pump Current Control, High Damping R1=2K, C1=400pF, C2=2pF, I1=50uA, 1:4 (Icp=1.08mA at 400Mbps)

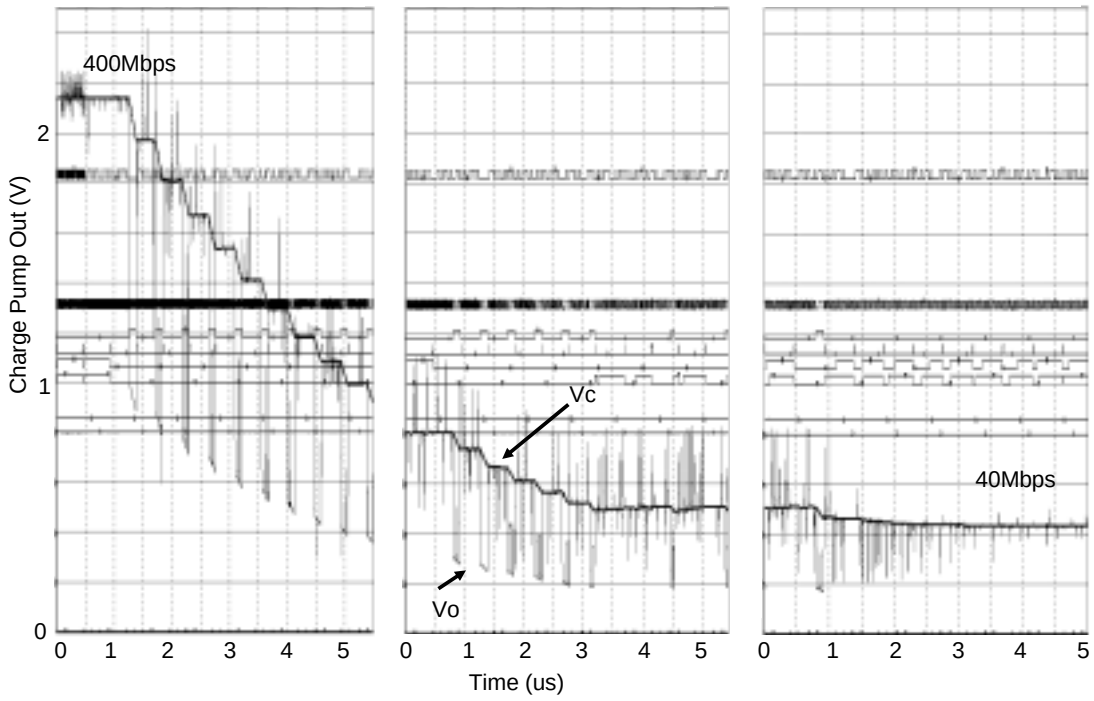



Fig. 6.2.18 CDR with Adaptive Charge Pump Current Control, High Damping R1=2K, C1=400pF, C2=2pF, I1=50uA, 1:4 (Icp=200uA at 40Mbps)

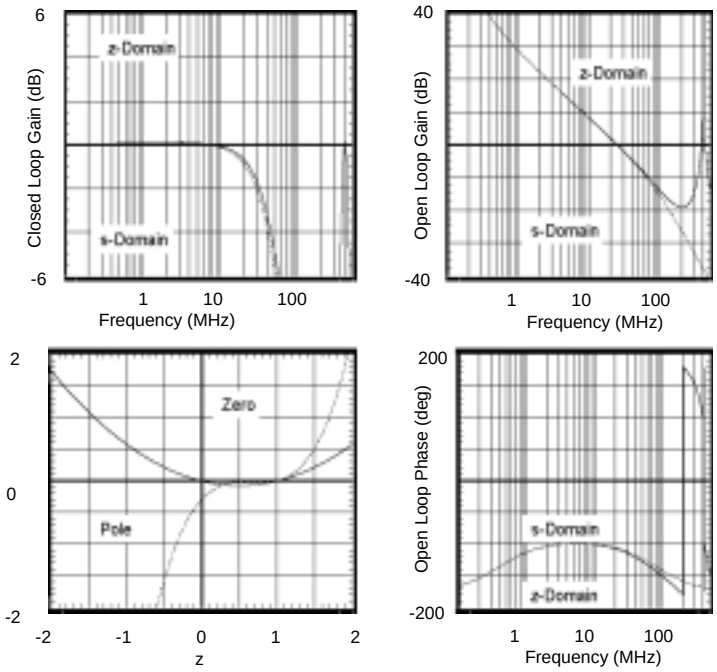



Fig. 6.2.19 CDR with Adaptive Charge Pump Current controlled
R1=2K, C1=400pF, C2=2pF,
I1=50uA, 1:4 (Icp=1.08mA at 400Mbps), K0=150MH/V

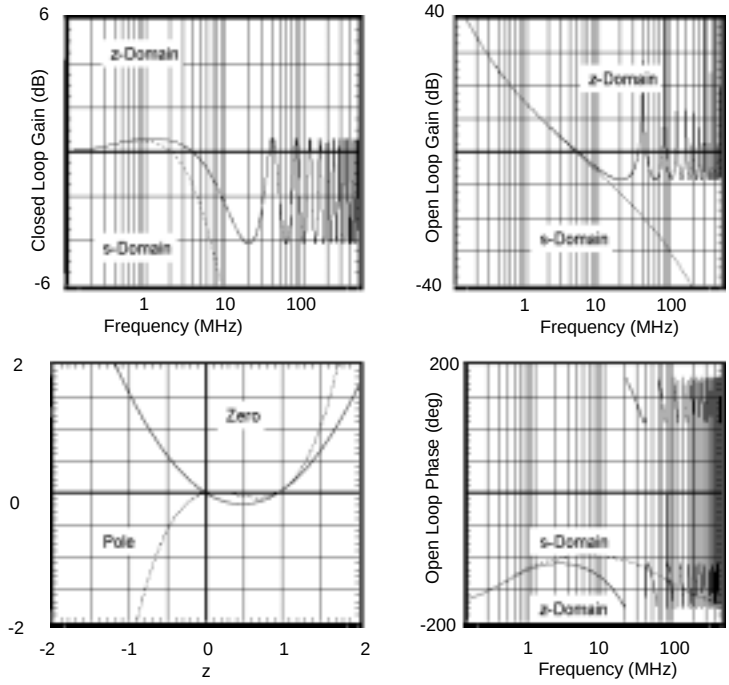



Fig. 6.2.20 CDR with Adaptive Charge Pump Current controlled
R1=2K, C1=400pF, C2=2pF,
I1=50uA, 1:4 (Icp=200uA at 40Mbps), K0=150MHz/V

## 6.3.6 Conclusion of Wide Variable bit Rate Application

For wide variable bit rate application, followings are concluded;

1) The charge pump current Icp and filter constant should be selected;

For low jitter application: smaller R1 and larger C1,

Icp should be small enough to upward frequency capture,

Charge pump current control may not be necessary in large $\tau(=\boldsymbol{R}_1\boldsymbol{C}_1)$,

$\boldsymbol{b}(=\frac{\boldsymbol{C}_1+\boldsymbol{C}_2}{\boldsymbol{C}_2})$ should be larger than 100.

For rapid lock-in: larger R1 and smaller C1,

Charge pump current control is mandatory,

Caution to stability in large $\frac{\boldsymbol{T}}{\tau}$ area,
( low bit rate side )

b should be larger than 20.

2) z-Domain analysis is very effective for;

Stability estimation: low bit rate area,

Jitter peaking estimation: all area of bit rate.

# Chapter 7.

# z-Domain Analysis for 3rd Order Loop

## 7.1 Summary

Usually, behavior of PLL is analyzed by s-Domain. However, in wide bit range application, if the time constant of filter approaches to the bit interval time (bit width), the stability issue arises especially in 3rd order loop. In such a circumstance, s-Domain analysis provides no valuable information. In order to make more precise analysis on that occasion, z-Domain analysis was made.

## 7.2 Fixed Delay 3 rd Order Loop

Gardner derived the z-Domain equations for 3rd order loop started from difference equation [13], however the final result was only presented. Hein derived the equations for 2nd order loop started from s-Domain filter impedance of the charge pump [14]. Followings are derived using the same scheme of Hein.

s and z are defined as follows. $T$ is defined as the 1 bit interval of data bit.

$$s = \sigma + j\omega \tag{7.2}$$

$$z = e^{sT} \tag{7.3}$$

Kps is defined as the s-Domain PFD-charge pump gain, and Kpz is that of z-Domain. Time averaging method [13,14] is applied, therefore,

$$K_{ps} = \frac{I_{cp} d}{2\pi} \tag{7.4}$$

$$K_{pz} = \frac{I_{cp} dT}{2\pi}. \tag{7.5}$$

Here, $I_{cp}$ is the charge pump current and $d$ is the transition density of data. Filter impedance of the charge pump circuit of R1, C1 and C2 can be written as s-Domain impedance Z(s),

$$Z(s)=\left(R_1+\frac{1}{sC_1}\right)\frac{\frac{1}{sC_2}}{R_1+\frac{1}{sC_1}+\frac{1}{sC_2}}=\left(\frac{b-1}{b}\right)\frac{s\tau+1}{sC_1\left(s\frac{\tau}{b}+1\right)} \tag{7.6}$$

Gain of CCO as VCO is defined as (MHz/V) and not in angular frequency. Laplace transformed open-loop-gain G(s) can be written,

$$G(s)=\frac{2\pi K_{ps}K_0}{s}Z(s)=\frac{2\pi KpsK_0}{C_1}\left(\frac{b-1}{b}\right)\frac{s\tau+1}{s^2\left(s\frac{\tau}{b}+1\right)}$$

$$=2\pi R_1K_{ps}K_0\left(\frac{b-1}{b}\right)^2\left[\frac{\left(\frac{b}{b-1}\right)\frac{1}{\tau}}{s^2}+\frac{1}{s}-\frac{1}{s+\frac{b}{\tau}}\right] \tag{7.7}$$

(7.7) is transformed to z-transformed-open-loop-gain G(z), and $K$ is defined as $K=2\pi R_1K_{pz}K_0$,

$$G(z)=2\pi R_1K_{pz}K_0\left(\frac{b-1}{b}\right)^2\left[\frac{\left(\frac{b}{b-1}\right)\frac{T}{\tau}z}{(z-1)^2}+\frac{z}{z-1}-\frac{z}{z-e^{-b\frac{T}{\tau}}}\right]$$

$$=K\left(\frac{b-1}{b}\right)^2\left(1+\frac{b}{b-1}\frac{T}{\tau}-e^{-b\frac{T}{\tau}}\right)\frac{z\left[z-\frac{1-\left(1-\frac{b}{b-1}\frac{T}{\tau}\right)e^{-b\frac{T}{\tau}}}{1+\frac{b}{b-1}\frac{T}{\tau}-e^{-b\frac{T}{\tau}}}\right]}{(z-1)^2\left(z-e^{-b\frac{T}{\tau}}\right)} \tag{7.8}$$

As seen in (7.8), open loop gain is proportional to certain coefficient. Here, this gain coefficient Gc is defined as follows.

$$G_c = \left(\frac{b-1}{b}\right)^2 \left(1 + \frac{b}{b-1}\frac{T}{\tau} - e^{-b\frac{T}{\tau}}\right) \tag{7.9}$$

Later, this coefficient is analyzed.

From (7.8) the closed loop gain H(z) is written as follows.

$$H(z) = \frac{G(z)}{1+G(z)} = \frac{B(z)}{A(z)} = \frac{K\left(\frac{b-1}{b}\right)^2 \left(1 + \frac{b}{b-1}\frac{T}{\tau} - e^{-b\frac{T}{\tau}}\right) z\left[z - \frac{1-\left(1-\frac{b}{b-1}\frac{T}{\tau}\right)e^{-b\frac{T}{\tau}}}{1+\frac{b}{b-1}\frac{T}{\tau}-e^{-b\frac{T}{\tau}}}\right]}{(z-1)^2\left(z-e^{-b\frac{T}{\tau}}\right) + K\left(\frac{b-1}{b}\right)^2 \left(1 + \frac{b}{b-1}\frac{T}{\tau} - e^{-b\frac{T}{\tau}}\right) z\left[z - \frac{1-\left(1-\frac{b}{b-1}\frac{T}{\tau}\right)e^{-b\frac{T}{\tau}}}{1+\frac{b}{b-1}\frac{T}{\tau}-e^{-b\frac{T}{\tau}}}\right]} \tag{7.10}$$

The numerator of (7.10) denote zeros, and the denominator of (7.10) denote pole(s) of H(z).

The denominator A(z) can be written as follows.

$$A(z) = z^3 - \left[3 - K\left(\frac{b-1}{b}\right)\frac{T}{\tau} - \left(1 + K\left(\frac{b-1}{b}\right)^2\right)\left(1 - e^{-b\frac{T}{\tau}}\right)\right] z^2$$

$$+ \left[1 - K\left(\frac{b-1}{b}\right)^2 + \left(2 + K\left(\frac{b-1}{b}\right)^2 \left(1 - \frac{b}{b-1}\frac{T}{\tau}\right)e^{-b\frac{T}{\tau}}\right)\right] z - e^{-b\frac{T}{\tau}} \tag{7.11}$$

## 7.3 Simulator of 3rd Order Loop

In order to visualize the equations, a simulator was made to calculate (7.8), (7.10) and (7.11) in complex number using Hewlett Packard VEE program so that the comparison between s-Domain and z-Domain analysis becomes clear.

Fig. 7.1 shows the display of the simulator. In Fig. 7.1, open loop gain in dB is shown in (B) and its phase is shown in (E) corresponding $G(z)$ (7.8). Phase beyond -180 degree is shown by resetting to +180 degree for just graph display purposes. Therefore, (B) and (E) show the Bode Diagram.

Closed loop gain in dB is shown in (A) and its phase is shown in (D) corresponding $H(z)$ (7.10). (C) shows the numerator of closed loop of $H(z)$ by sweeping z in real axis, whose crossing points of z axis denote zeros. (C) also shows the denominator of closed loop of $H(z)$, whose crossing point(s) of z axis denote pole(s). Due to the 3rd order equation, there is(are) one or three poles. If zeros and pole(s) reside inside of unit circle of z-plane, the system is stable, otherwise unstable.
These can be displayed on the panel of simulator as shown in Fig. 7.1.

Gain coefficient Gc is a function of $T/\tau$, and it is shown in Fig. 6.1.4 in parameter of b. As seen in Fig. 6.1.4, if b is small, and if $T/\tau$ is small, the gain factor Gc becomes abruptly small. This means that if C2 is large, and if bit rate is high, and if large $\tau$ (=R1C1) is used, open loop gain becomes abruptly small. Therefore, in high bit rate application, smaller $\tau$, i.e. smaller C1 should be used. Conversely, in low bit rate area, if small $\tau$ is used, stability issue may arise. Therefore, selection of these values is very important.

Other criteria is the jitter characteristics. Closed loop gain characteristics as shown in Fig. 7.1 (A) is called jitter characteristic curve or jitter peaking curve.
Fig. 7.2 shows the case of small $\tau$ and small b, $\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF), Icp = 400uA, d = 0.5, R1 = 1.5K, T = 5ns(200Mbps), K0 = 150MHz/V. As seen in Fig. 7.2, peak of closed loop gain is 1.1dB and bandwidth is 6MHz.

Therefore, if the transceiver systems are connected in tandem, jitter may be enlarged. If C1 is enlarged to 10 times, hence $\tau$ becomes 10 times, jitter peaking characteristics become better as shown in Fig. 7.3. As seen in Fig. 7.3, closed loop gain becomes small, 0.1 dB flat, and band width becomes 2MHz.

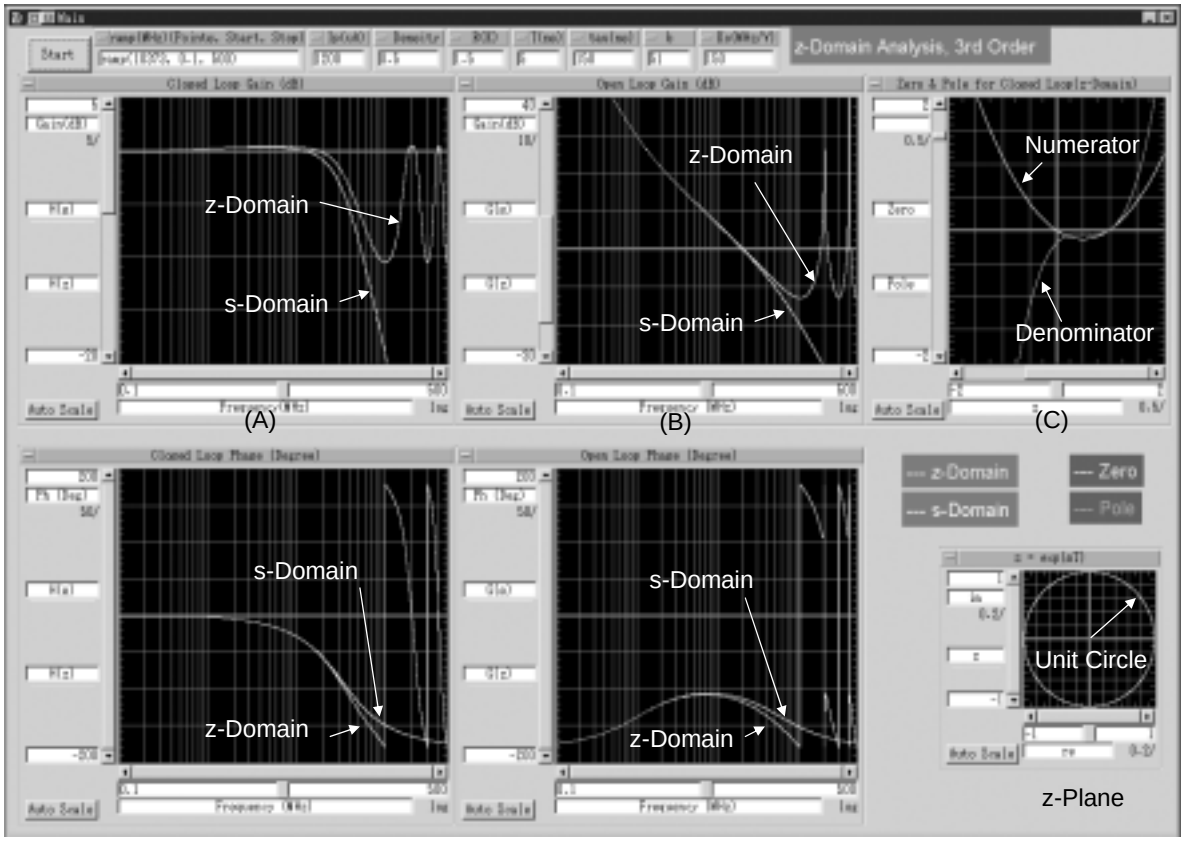



Fig. 7.1 z-Domain and s-Domain Simulator

Icp = 1200uA, d = 0.5, R1 = 1.5K, T = 5ns (200Mbps)

$\tau$ = 150ns (C1 = 100pF), b =51 (C2 = 2pF)

K0 = 150MHz/V

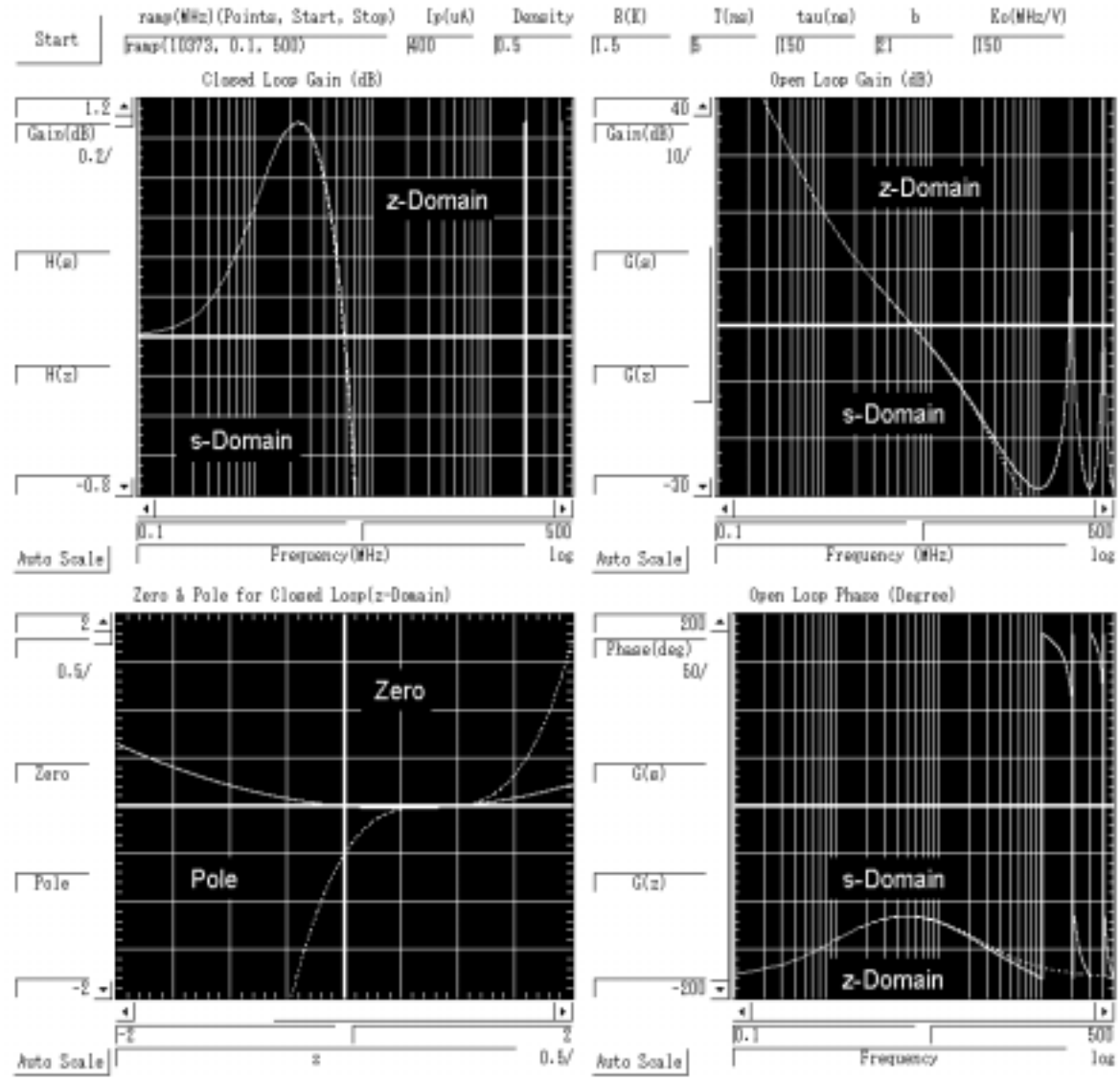



Fig. 7.2 z-Domain and s-Domain Simulator

$\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF)

Icp = 400uA, d = 0.5, R1 = 1.5K, T = 5ns(200Mbps)
K0 = 150MHz/V

For example, in the SONET OC-48, jitter peaking shoude be 0.1 dB and cutoff frequency should be 2MHz. In that sense, Fig. 7.3 meets the requirements.

However, in SPICE simulation, large $\tau$ requires prohibitively long time for computation. If $\tau$ = 1500ns and making full range of simulation about CCO, computation time becomes more than 24 hours even by 1.73GHz CPU clock and 512MB memory Windows PC. For SPICE Simulation software, B2 Spice AD2000 Version 4 by Beige Bug Software Inc. was used. In recent version, the simulation was crushed more than 3us. In version 4, the simulation can be made until 5us in 2 hours about the system of 650 transistors.
Therefore, the SPICE simulations presented earlier were done at $\tau$ = 150ns, until 3 to 6us.

As seen in Fig. 7.2 and 7.3, z-Domain curve shows a little bit higher jitter and wider band width than s-Domain curve, but not so much difference at these $\tau$ and b condition.

However, in low bit rate area, i.e. large T area, trace of the curve becomes different. Fig. 7.4 shows the case that T is 20ns (50Mbps), Icp is 1200uA, $\tau$ is 150ns and b is 21. As seen in Fig. 7.4, open loop gain in z-Domain analysis over the 0dB, and closed loop gain is extraordinarily high. One pole becomes less than -1. Therefore the system is unstable on this condition.

However, in open loop gain and phase curve of s-Domain, there is a phase margin of 50 degree or so. Therefore by s-Domain analysis, the system is stable. Fig. 7.5 shows the SPICE simulated waveforms under this condition. As seen in Fig. 7.5, it is apparent that the system is unstable.

Fig. 7.6 shows that Icp is decreased to 400uA. The poles reside inside of +/- 1. Therefore the system is stable. Fig. 7.7 shows the SPICE simulated wave forms under this condition. It is apparent that the system is stable.

As a conclusion, it was verified that the z-Domain analysis provides more powerful tool for stability criteria than conventionally used s-Domain analysis.

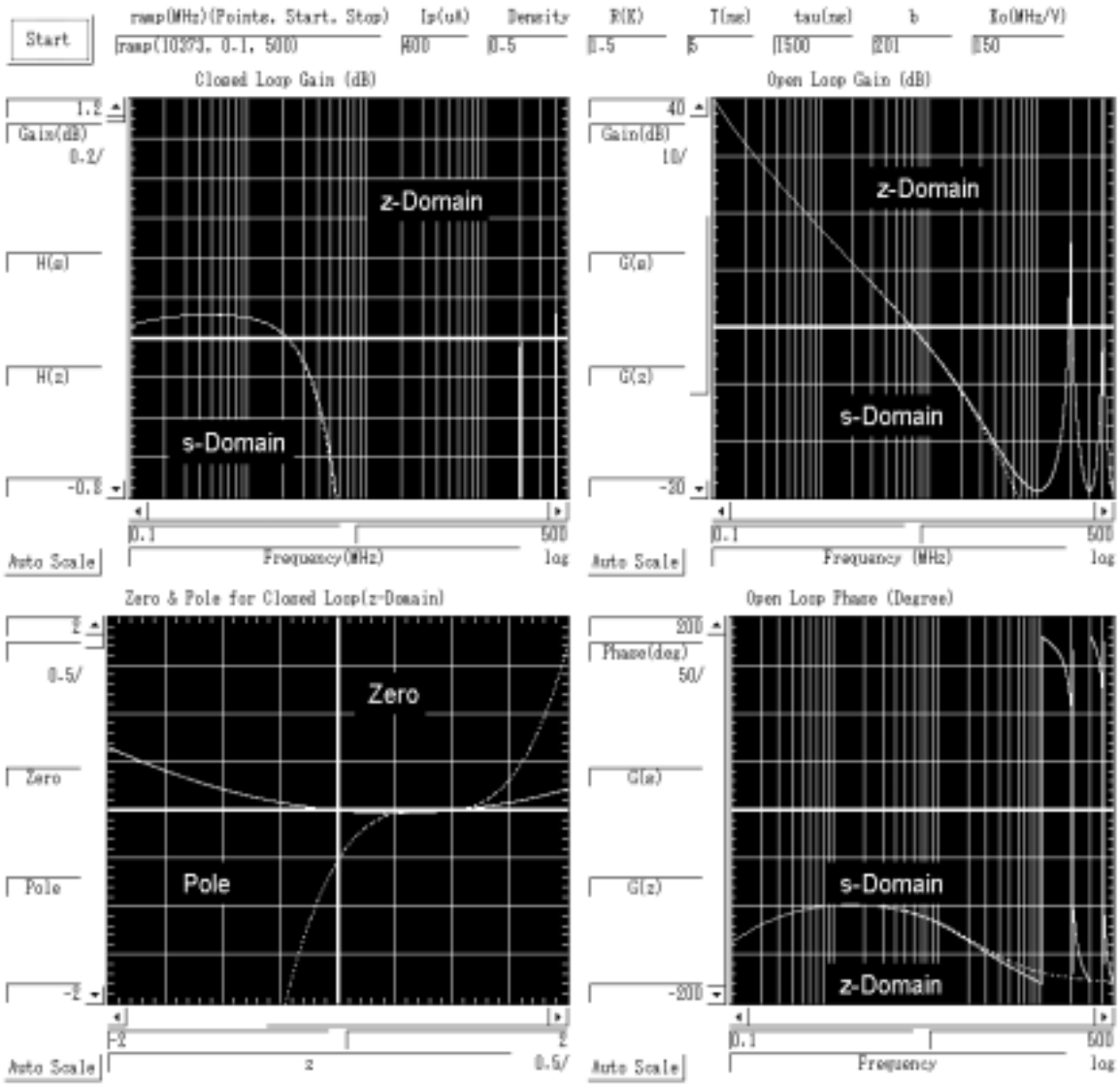



Fig. 7.3 z-Domain and s-Domain Simulator

$\tau$ = 1500ns (C1 = 1000pF), b =201 (C2 = 5pF)

Icp = 400uA, d = 0.5, R1 = 1.5K, T = 5ns(200Mbps)
K0 = 150MHz/V

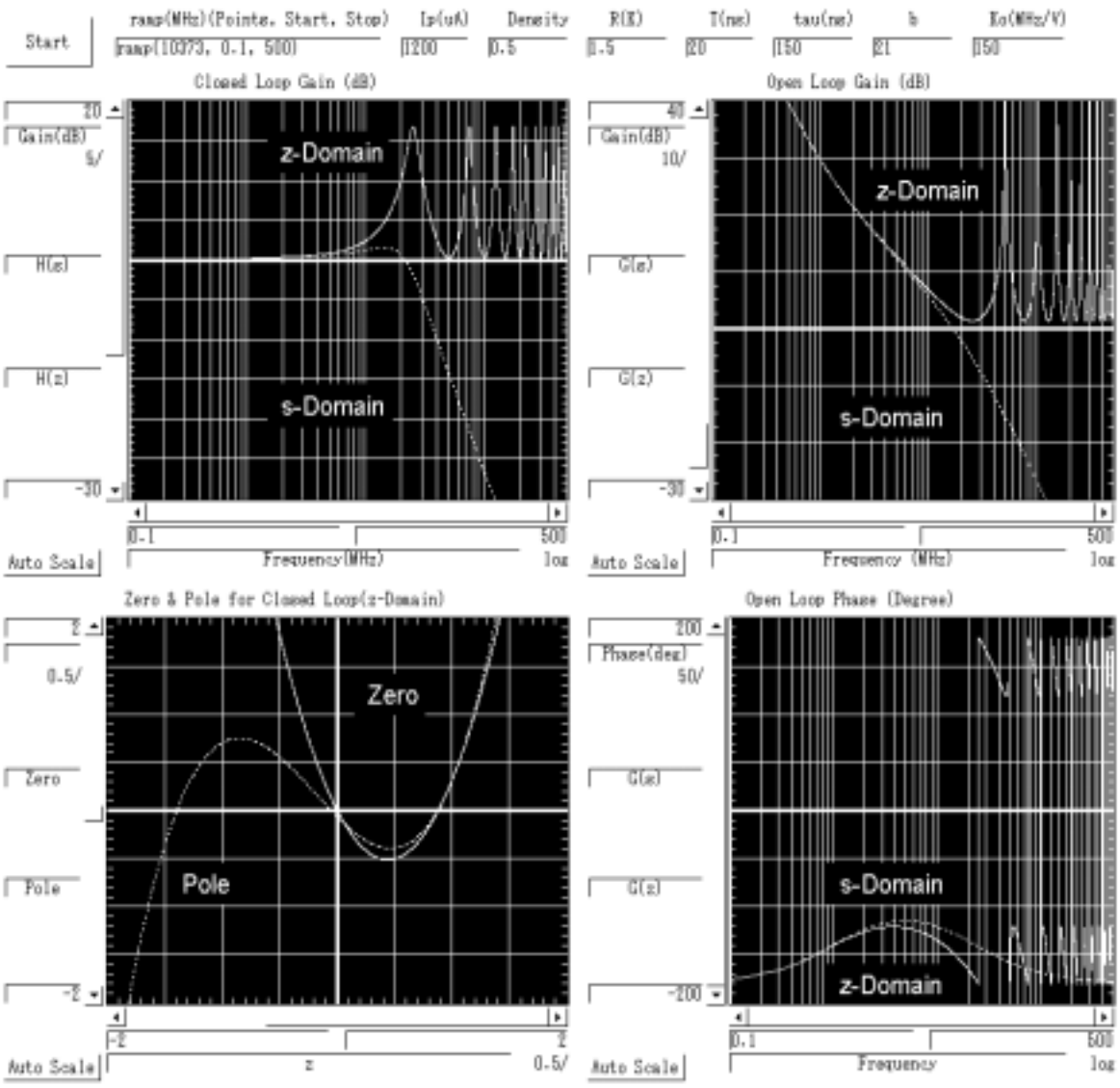



Fig. 7.4 z-Domain and s-Domain Simulator

Icp = 1200uA,

$\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF)
T = 20ns(50Mbps), d = 0.5, R1 = 1.5K
K0 = 150MHz/V

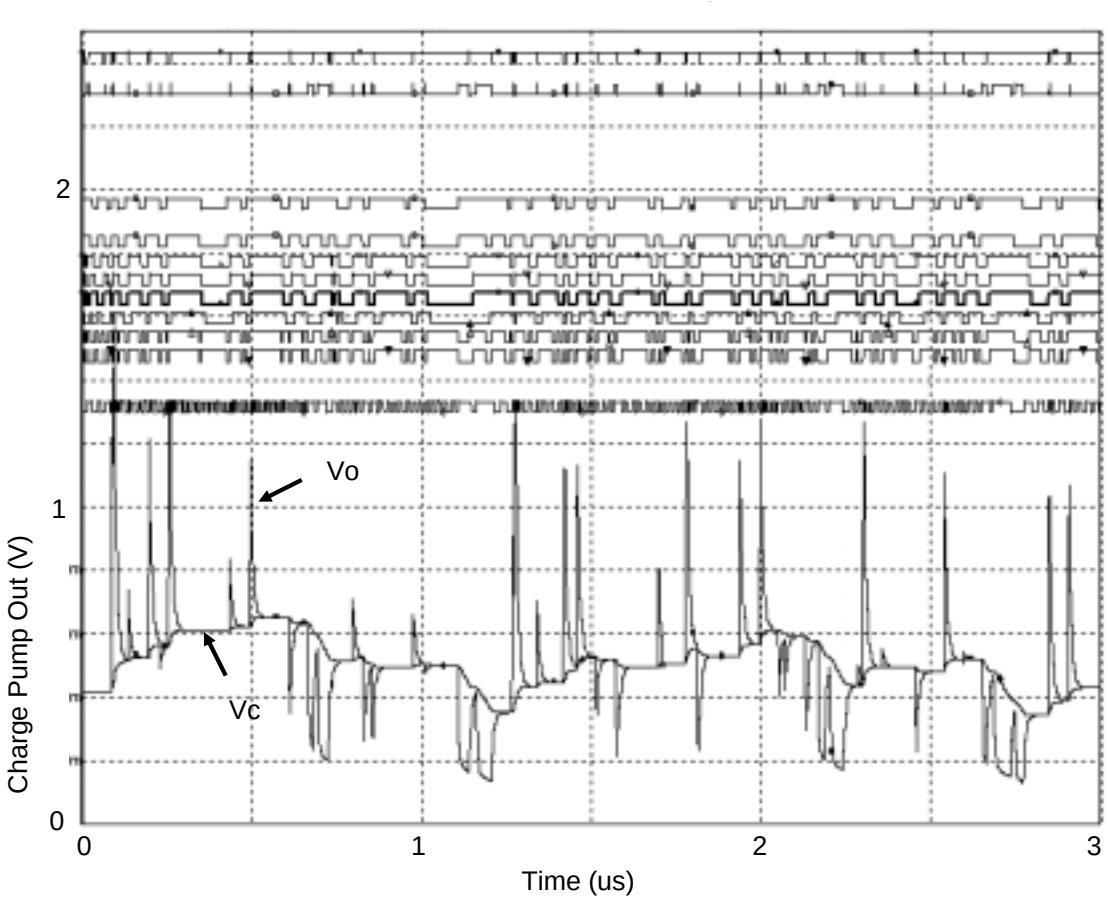



Fig. 7.5 SPICE Simulated Waveforms, System is unstable

Icp = 1200uA,

$\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF)
T = 20ns(50Mbps), d = 0.5, R1 = 1.5K
K0 = 150MHz/V

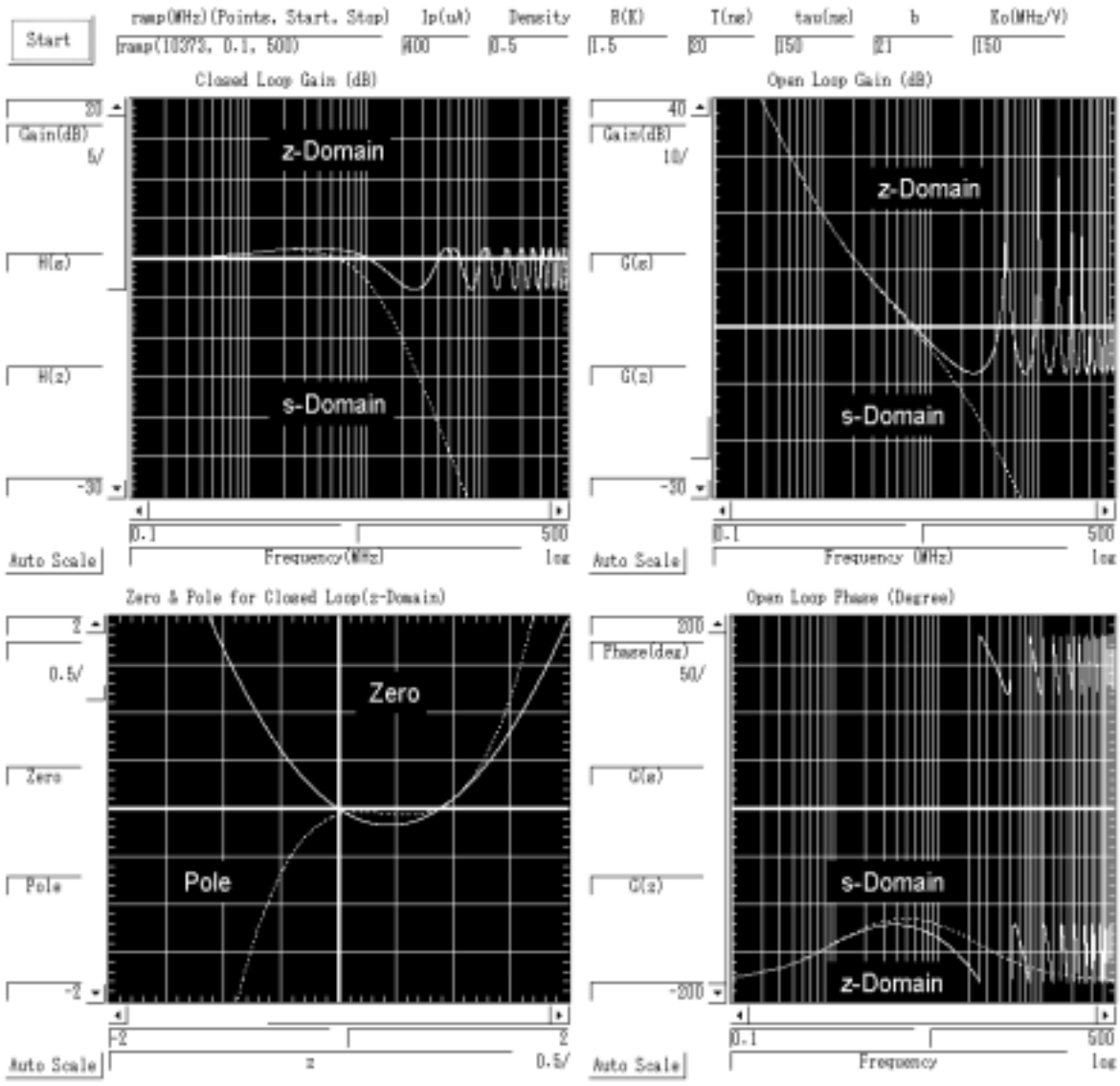



Fig. 7.6 z-Domain and s-Domain Simulator

Icp = 400uA,
$\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF)
T = 20ns(50Mbps), d = 0.5, R1 = 1.5K
K0 = 150MHz/V

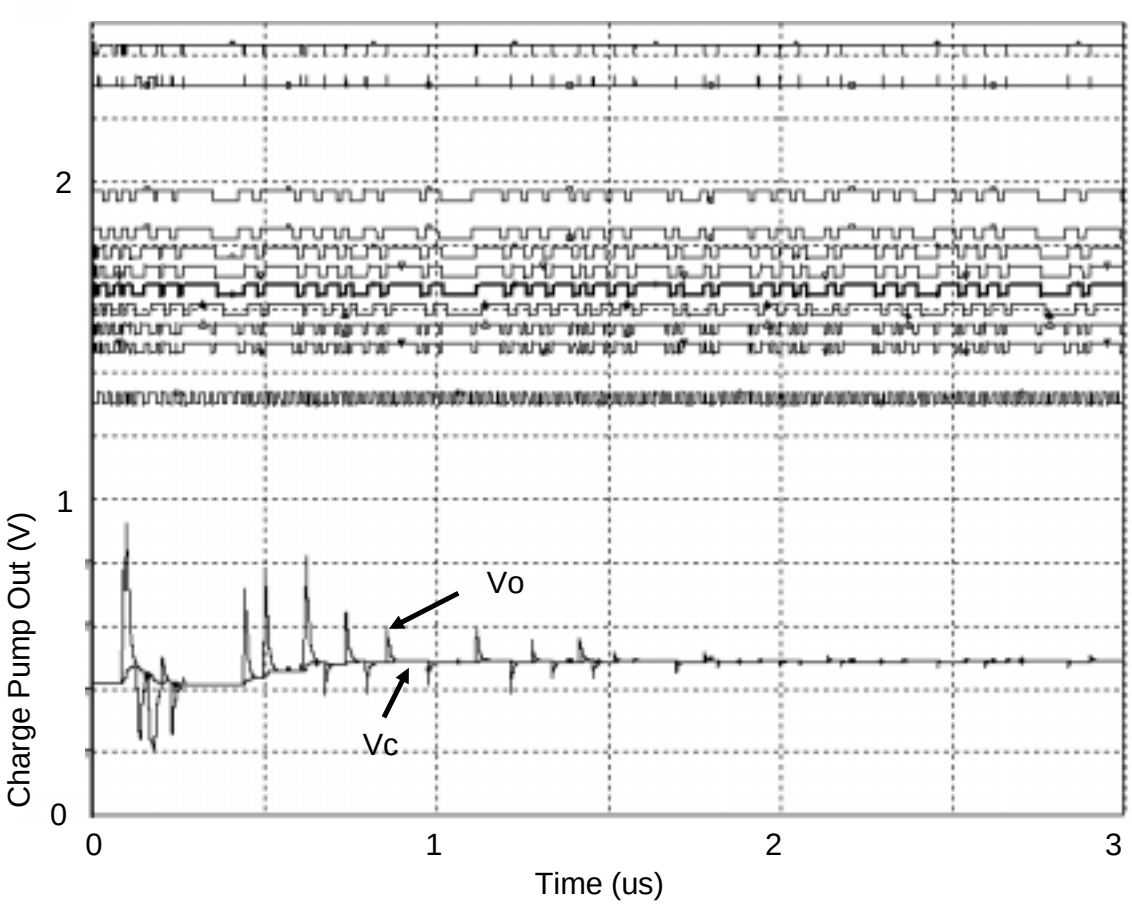



Fig. 7.7 SPICE Simulated Waveforms, System is stable

Icp = 400uA,
$\tau$ = 150ns (C1 = 100pF), b =21 (C2 = 5pF)
T = 20ns(50Mbps), d = 0.5, R1 = 1.5K
K0 = 150MHz/V

# Chapter 8.

# Fabrication as LSI

## 8.1 LSI Design

Pattern layout design of CDR for fixed bit rate application with negative feed back to data delay as shown in Fig. 5.2 was made in 0.35um CMOS, and its fabrication was ordered to ROHM Corporation via VDEC.

Fig. 8.1 shows the pattern layout. Digital PFD portion was written in Verilog, and the function was verified by Verilog. Then logic synthesis was made by Synopsis, and the automatic placement and interconnection were made by Apollo. Other blocks such as CCDD, CCO, Charge Pump, V-I converter, and Current Subtraction Circuit were written manually. Special care was taken to avoid noise and cross coupling. Each blocks were shielded or guarded by power ring or ground metal.

Fig. 8.2 shows pad layout and the inter-connection between blocks and pads.

## 8.2 Evaluation on Fabricated LSI

Evaluation was done in making a set in complete shielding in aluminum small box, cupper shielding and cupper ribbon interconnection in minimum inductance using UHF transceiver technology and practices.

Special care was taken in impedance matching on 50 ohm coaxial cable measuring system to eliminate the effect of reflection of pulses. To this end, “Fly-By” method and insertion of 3dB pad was applied as a basics of measurement. “Fly-By” method is described as follows. 50 ohm output of pattern generator, Agilent Technology (HP) 81110A, is connected to 50ohm coaxial cable 2m in length, and the coaxial cable is connected to 50 ohm input of Tektronix TDS3034B. At mid point of coaxial cable, 1m in length, the input of the CDR system is connected which is the high impedance of CMOS input pad buffer. However, there is an input capacitance on pad buffer, reflection of the pulse was occurred. To eliminate, or taking some isolation, this impedance miss-match, series resistor of 120ohm was inserted.

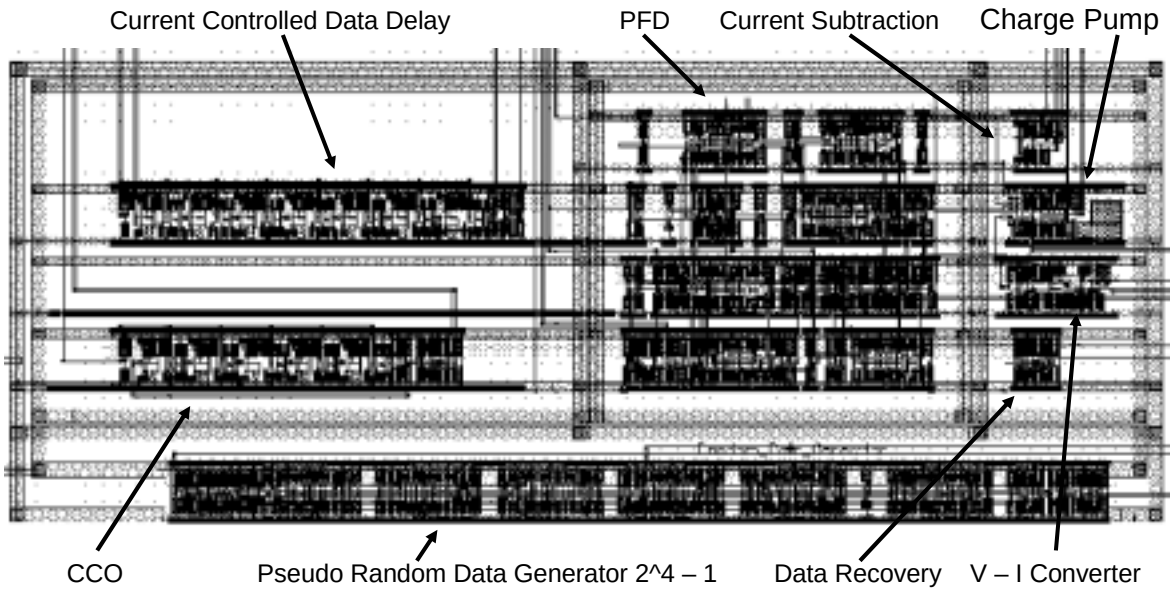



Fig. 8.1 LSI Pattern layout of Fixed bit Rate CDR

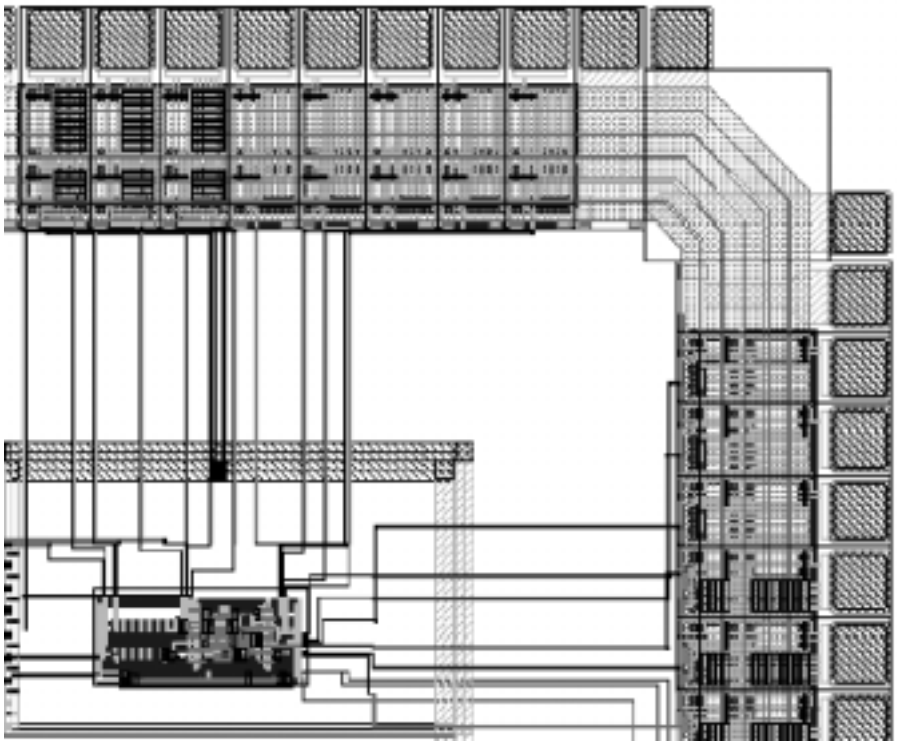


Fig. 8.2 Pad layout and interconnection

3 dB pad is also inserted on output of CCO. Out put impedance of pad buffer of the LSI was measured around 10 ohms. Therefore, 3 dB pad on 50 ohm system was made by resistor network and inserted.

Fig. 8.3 shows the out put waveform of PFD block of the fabricated LSI. In Fig. 8.3, Data and Xck are generated by the pattern generator, and Data_dif and Charge Pump Out are the output of the PFD. Delay of Data_dif was varied by the control current Id in Fig. 5.2. As seen in Fig. 8.3, the PFD is functioning as desired. There is no output at missing transition of data, and the charge pump output at phase matched state is very small. Therefore the PFD has large figure of merit even in NRZ data as the same as 3-state PFD in continuous pulses.

Fig. 8.4 and Fig. 8.5 show the waveforms as a PLL loop under 50Mbps $2^7-1$ pseudo-random data. These waveforms were taken as fixed delay current Id in Fig. 5.1, because there were many noises on current subtraction circuit as shown in Fig. 5.1.

As seen in Fig. 8.4, the PLL loop was duly locked at 50Mbps, measured value of 49.93MHz.

Fig. 8.5 shows the worst case of $2^7-1$ pseudo-random data pattern, “0111111110000001”. On this data, 14 bit time of center portion, the PFD generates only one output to the charge pump at first rise up of “1”, and other 13 bit times CCO oscillates in fly wheeling. In Fig. 8.5, lowest waveform is the original clock of pattern generator as a reference. Therefore, difference from this reference pulse means the jitter. As seen in Fig. 8.5, difference is very small during data is high level, however, the difference increases gradually during data is low. As the result of analysis, it became clear that some noise pulse was induced on input of V-I converter at falling edge of data, and not on out put of PFD. The Tektronix does not have the function of statistical measurement of jitter, but has the FFT function. So, the result of FFT is also shown in Fig. 8.5. The skirt of FFT is not narrow, that means the jitter is somewhat large.

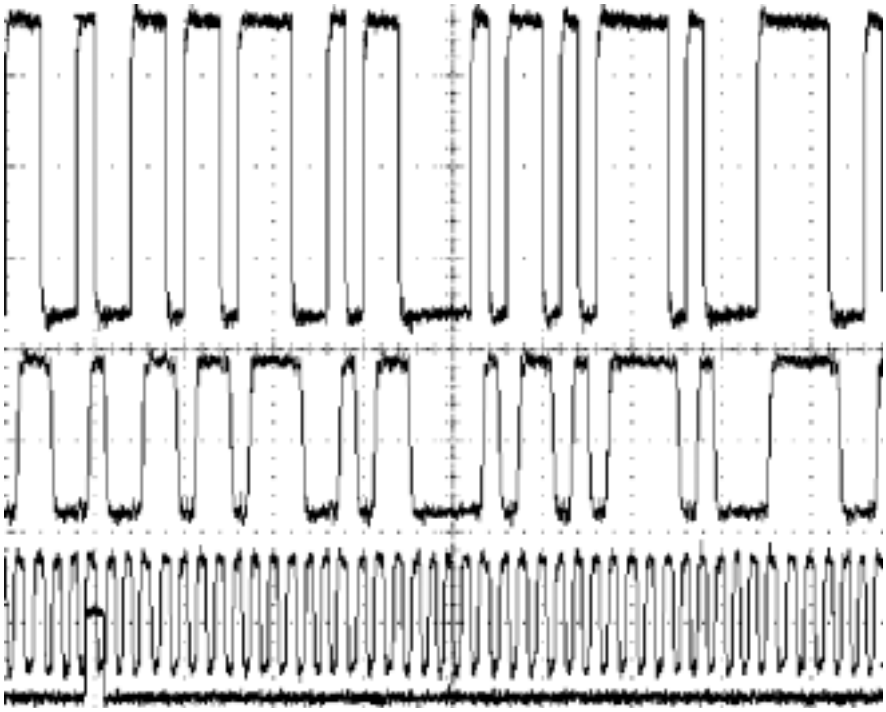



Fig. 8.3 Output of Phase Frequency Detector on Fabricated LSI, 50Mbps

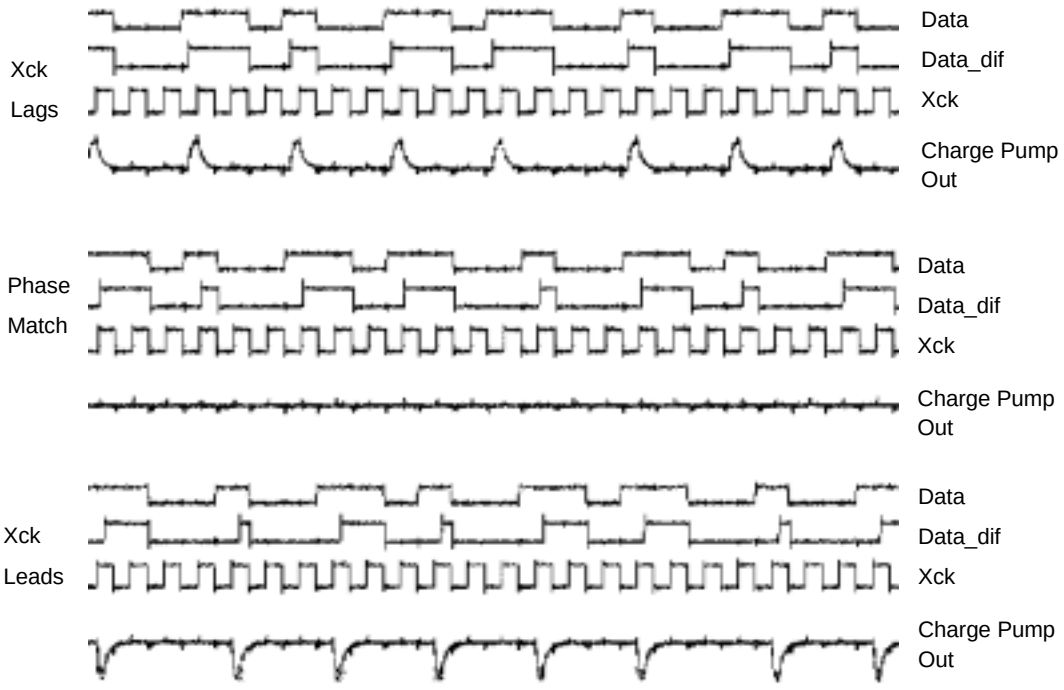



Fig. 8.4 Locked waveforms at 50Mbps

Icp = 500uA, R1 = 330ohm, C1 = 0.01uF, C2 = 470pF

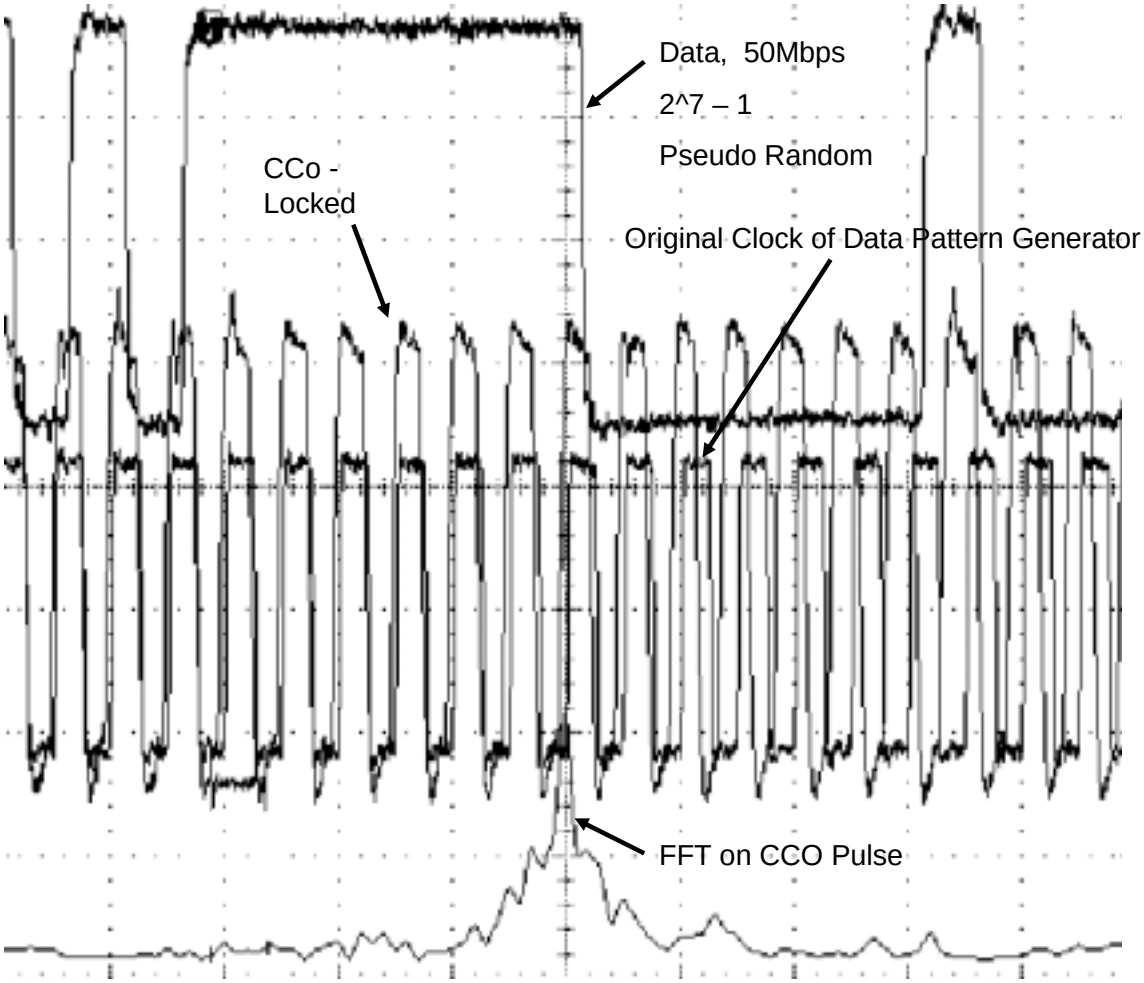



Fig. 8.5 Locked Waveforms, Worst Case of 2^7-1 Pseudo random Data

As the conclusion of trial product of the LSI;

1) The proposed 4-State PFD really works on LSI under NRZ data.
2) As proposed, the PFD has the function of frequency detector and large figure of merit.
3) In order to make the test of operability of blocks, this time trial design of the LSI was divided in each blocks and in- and output of each blocks were taken out of the LSI. This causes the many noise, especially loop coupling noise. Therefore, real integration inside of LSI should be done. Long and thin width inter connection to the pads as shown in Fig. 8.2 should be improved to short and thick one in future design.

# 9. Conclusion

A new 4-State PFD, which is an augmentation of traditional 3-State PFD, is presented and verified that it has the functions, characteristics and features; 1) having function of frequency detector on NRZ data, 2) wide frequency capture Range, 3) large figure of merit – low output at phase locked state, 4) using only 3 DFFs, in which Hidden “1” DFF can be usable. Therefore it inherits the features of 3-state PFD such as frequency detector and low jitter characteristics even for NRZ data stream. These have been verified by Verilog- and SPICE simulation, FPGA test and finally on fabricated 0.35um CMOS LSI.

The new PFD employs the data delay for extraction of frequency component of original clock and missing transition on NRZ data stream. By controlling the delay time of the data delay adaptively, rapid, false-lock-free and robust operation on application of fixed bit rate, variable- or multi-different-bit-rate NRZ data of transmitters. For wide bit rate application, the adaptive control of the charge pump current has been also verified that it can provide robust operation and rapid lock-in. Applying those schemes, the operation of 40 to 400Mbps, 1 decade in bit rate, has been verified by SPICE simulation.

z-Domain analysis has also verified that it provides the powerful tools for stability evaluation, lock-in- and jitter-peaking- characteristics through its software simulator.

As an application specific conclusion, followings will be wrapped up;

1. 4-State PFD
   Time slot control should be always included.

2. Fixed bit rate Application

   - Data delay by physical entity, such as coaxial cable or micro-strip line, is the best in the point of view of stability, high speed and power consumption-less.
   - If semiconductor delay element is used, a negative feedback to data delay by current mode (current subtraction) should be implemented due to stability, high speed and false- lock- free lock-in.

3. Variable bit rate - Narrow

   - Downward frequency capture aid is mandatory.
   - Upward frequency capture aid may be used.

4. Variable bit rate – Wide

   - Downward frequency capture aid is mandatory.
   - Charge pump current control is mandatory.
   - Upward frequency capture aid should be used.

# Chapter 10

# Acknowledgement

Author would like to express his sincere thanks to Professor Kunieda, Tokyo Institute of Technology, for his kind guidance and encouragements, and Messrs Kenichi Kawaguchi, Chikara Komata and Kazuyoshi Unno of Yazaki Corporation for their encouragement and cooperation for measurement, as well as to all the members of CAD21 Research body of Tokyo Institute of Technology for their suggestion and cooperation, and VDEC and ROHM Corporation for fabrication of LSI.

# References


[1] C.R. Hogge, “A self-correcting clock recovery circuit,” J. Light Wave Technol., vol. LT-3, no.6, pp.1312-1314, 1985.

[2] L. Devito et al., “A 52MHz and 155MHz clock recovery PLL,” 1991 ISSCC Dig. Tech. Papers, p.142.

[3] T. H. Lee et al, “A 155-MHz clock recovery delay- and phase-locked loop,” IEEE J. Solid State Circuits, vol. SC-27, pp. 1736-1746, December 1992.

[4] B. Razavi et al, “A 2.5-Gb/sec 15-mW BiCMOS Clock Recovery Circuit,” Symposium on VLSI Circ. Dig. of Tech. Papers, 1995, pp. 83.

[5] J. A. Bellisio, “A New Phase-Locked Timing Recovery Method for Digital Regenerators,” IEEE Int. Conf. Rec., vol.1,pp. 10-17 t0 10-20, June 1976.

[6] J. A. Afonso et al, “A Phase-Locked Loop with Digital Frequency Comparator for Timing Signal Recovery,” National Telecom. Conf. Rec. paper 14.4, 1979.

[7] C. A. Sharpe, “A 3-state phase detector can improve your next PLL design,” EDN, pp.55-59, September 20, 1976.

[8] W. D. Llewellyn, U. S. Patent 5,172,397, Date of Patented Dec.15, 1992.

[9] G. Idei et al, “A Clock Recovery PLL Applicable to Data Stream with Missing Pulses,” IEEE APCCAS-Tianjin, December 2000, pp509.

[10] B. Razavi, “Monolithic Phase-Locked Loops and Clock Recovery Circuits,” IEEE Press 1996, ISBN. 0-7803-1149-3, P26, Fig. 46.

[11] I. Shahriary et al, “GaAs Monolithic Digital Pulse/ Frequency Discriminator,” IEEE GaAs IC symp. Dig. of Tech. Papers, pp. 183-186, October 1985.

[12] G. Idei and H. Kunieda, “A False-Lock-Free Clock/Data Recovery PLL for NRZ Data Using Adaptive Phase Frequency Detector,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, Vol. 50, NO. 11, pp896, November 2003.

[13] F. Gardner, “Charge-Pump Phase-Locked Loops,” IEEE Trans. Comm, vol. COM-28, pp. 1849-1858, November 1980.

[14] J. P. Hein et al, “z-Domain Model for Discrete-Time PLL’s,” IEEE Trans. Circuit and Systems, vol. 35, pp. 1393-1400, November 1988.

[15] S. Yinshang, “An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance,” IEEE J. of Solid State Circuits, vol SC-24, pp325, April 1989.

[16] B. Kim, “A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-um CMOS,” IEEE J of Solid State Circuits, vol. SC-25,pp1385, December 1990.

[17] S. Miyazawa et al, “A BiCMOS PLL-Based Data Separator Circuit with High Stability and Accuracy,” IEEE J of Solid State Circuits, vol. SC-26,pp116, February 1991.
[18] N. Ishihara, “A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique,” IEEE J of Solid State Circuits, vol SC-29,pp1566, December 1994.
[19] T. Hu et al, “A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2um CMOS,” IEEE J of Solid State Circuits, vol SC-28, pp.1314, 1993.
[20] B. Lai et al, “A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit,” ISSCC Dig. Tech. Papers,pp.144, February 1991.
[21] M. Bann et al, “A 600 Mb/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission,” ISSCC Dig. Tech Papers, pp102, February 1993.
[22] M. Soyuer, “A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology,” IEEE J of Solid State Circuits, vol. SC-28, pp1310, December 1994.
[23] R. Cordell et al, “A 50 MHz Phase- and Frequency-Locked Loop,” IEEE J of Sold State Circuits, vol. SC-14, pp1003, December 1979.
[24] S. Enam et al, “NMOS IC’s for Clock and Data Regeneration in Gigabit-per-Second Optical-Fiber Receivers,” IEEE J of Solid State Circuits, vol. SC-27, pp1763, December 1992.
[25] H. Ransjin et al, ”A PLL-Bases 2.5-Gb/s GaAs Clock and Data Regenerator IC,” IEEE J of Solid State Circuits, vol. SC-26, pp1337, October 1991.
[26] A. Pottbacker et al, “An 8 GHz Silicon Bipolar Clock-Recovery and Data-Regenerator IC,” IEEE J of Solid State Circuits, vol. pp1572, 1994.
[27] M. Ramezani et al, “Analysis of Half-Rate Bang-Bang Phase-Locked-Loop,” IEEE Trans. Circuit and Systems-II Analog and Digital Signal Processing, vol. 49, pp505, July 2002.
[28] M. Rau et al, “Clock/Data Recovery PLL Using Half Frequency Clock,” IEEE J. Solid State Circuits, vol. 32, pp1156, July 1997.
[29] Y. Greshishchev et al, “A fully integrated SiGe receiver IC for 10 Gb/s data rate,” IEEE j. Solid State Circuits, vol. 35, pp1949, December 2000.
[30] R. Walker et al, “A two-chip 1.5GBd serial link interface,” IEEE J. Solid State Circuits, vol. 27, pp1805, December 1992.
[31] D. Messerschmitt, “Frequency detection PLL acquisition in timing and carrier recovery,” IEEE Trans. Commun., vol. Comm-27, pp1288, September 1979.

[32] Y. Choi et al, “Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery,” IEEE Trans. Circuit and Systems-II, Analog and Digital Signal Processing, vol.50, pp775, November 2003.
[33] J. Alexander, “Clock recovery from random binary signals,” Electron. Lett. Vol. 11, pp. 541-542, October 1975.
[34] J. Cao et al, “OC-192 transmitter and receiver in standard 0.18um CMOS,” IEEE J. Solid State Circuits, vol. 37, pp. 1768-1780, December 2002.
[35] J. Savoi et al, “A-10Gb/s CMOS clock and data recovery circuit with frequency detection,” ISSCC Dig. Tech. Papers, pp. 78-79, February 2001.
[36] K. Cheng et al, “A dual-slope phase frequency detector and charge pump architecture to achieve fast locking of phase-locked-loop,” IEEE Trans. Circuit and Systems-II: Analog and Digital Processing, vol. 50, pp. 892-896, November 2003.
[37] S. Kim et al, “A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL,” IEEE J. Solid-State Circuits, vol. 32, pp. 691-699, May 1997.
[38] J. Maneatic et al, “Low-jitter process-independent DLL and PLL based on self-biased techniques,” IEEE J. Solid-State Circuits, vol. 31, pp 1723, November 1996.
[39]B. Razavi, “A study of phase noise in CMOS oscillators,” IEEE J. Solid-State Circuits, vol. 31, pp.331-343, March 1996.
[40] J. Lee et al, “A low-noise fast-lock phase-locked loop with bandwidth control,” IEEE J. Solid-State Circuits, vol. 35, pp. 1137-1145, August 2000.
[41]P. Hanumolu et al, “Analysis of PLL clock jitter in high-speed serial links,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, vol. 50, pp. 879-886, November 2003.
[42] J. Kim et al, “Design of CMOS adaptive-bandwidth PLL/DLLs: a general approach,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, vol. 50, pp. 860-869, November 2003.
[43]M. Mansuri et al, “Methodology for on-chip adaptive jitter minimization in phase-locked loops,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, vol. 50, pp. 870-878, November 2003.
[44]G. Manganaro et al, “A Behavioral modeling approach to the design of a low jitter clock source,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, vol. 50, pp. 804-814, November 2003.
[45] B. Lee et al, “A 2.5-10Gb/s CMOS tranceiver with alternating edge-sampling phase detection for loop characteristic stabilization,” IEEE j. Solid-State Circuits, vol.38 pp.1821-1829, November 2003.

# Publications

## Papers, Published

1. G. Idei and H. Kunieda, “ A False-Lock-Free Clock/Data Recovery for NRZ Data Using Adaptive Phase Frequency Detector,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, vol. 50, pp. 896-900, November 2003.

## Papers, Accepted

1. G. Idei and H. Kunieda, “A Clock and Data Recovery PLL for Variable bitRate NRZ Data using Adaptive Phase Frequency Detector,” IEICE Trans. Fundament. Electron. Comm. Comp., To appear June, 2004.

## Conferences

1. G. Idei, H. Kunieda and K. Unno, “A Clock Recovery PLL Applicable to Data Stream with Missing Pulses,” Proc. IEEE APCCAS, Tianjin, China, p509, December 2000.

## Technical Meetings

1. G. Idei and H. Kunieda, “A Clock and Data Recovery PLL for Variable bit Rate NRZ Data using Adaptive Phase Frequency Detector,” IEE-J, Paper. Tech. Meeting, Electronic Circuits, ECT-03-84, November 13, 2003.

## Manuscripts Submitted, Under Review

1. G. Idei and H. Kunieda, “A Phase Frequency Detector Applicable to Clock and Data Recovery PLL for NRZ Data,” IEEE Trans. Circuit and Systems-II: Analog and Digital Signal Processing, Received on March 8, 2003.

# Patents Applied

## 1. Japan

1.1 名称：位相比較器および同期信号抽出装置
出願番号：2001-149888
出願日： 2001.05.18
公開番号：2002-246903
公開日： 2002.08.30

1.2 名称：遅延回路および発振回路
出願番号：2001-344521
出願日： 2001.11.09

1.3 名称：同期装置
出願番号：2003-370568
出願日： 2003.10.30

## 2. U.S.A.

2.1 名称：PHASE COMPARATOR AND SYNCHRONIZING SIGNAL EXTRACTING DEVICE
出願番号：859505
出願日： 2001.05.18
公開番号：0043086
公開日： 2001.11.22

## 3. Europe (EPO)

3.1 名称：Phase comparator and clock recovery circuit
出願番号：01111939.320
出願日： 2001.05.18
公開番号：1158680
公開日： 2001.11.28