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Doctor of Engineering Thesis

Study of the influence of crystal defects and interface traps on SiC power device characteristics

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Thesis Summary

Silicon carbide (SiC) is an attractive material for manufacturing low on-resistance, high-voltage power devices with less energy conversion loss. A full SiC inverter composed of a SiC metal oxide semiconductor field effect transistor (MOSFET) and SiC diode has already been put into practical use, and the performance of the SiC insulated-gate bipolar transistor (IGBT) and SiC thyristor has also been reported. However, because SiC is a compound and multiple polytypes exist, SiC power devices contain more high-density crystal defects and interface states/bulk traps than Si power devices. As an example, stacking faults (SFs) in the SiC epilayer exists on the order of 0.1–1 cm^{-2}, the density of SiO_2/SiC interface states is 10^{11}–10^{13} cm^{-2}, and the density of bulk traps in SiC is 10^{11}–10^{14} cm^{-3}. It is known that the performance of SiC power devices is determined by defects and states. To improve the characteristics of SiC power devices, it is necessary to evaluate the influence of crystal defects and interface states.

In this research, we aimed at quantitatively clarifying the influence of SiC crystal defects and interface states/bulk traps on device characteristics, including its mechanism, for the purpose of improving the performance of SiC power devices. We focused on SiC-junction barrier Schottky diode (JBS, a kind of Schottky diode in which the p-wells are fabricated at constant intervals in the Schottky barrier diode), MOSFETs, and optically triggered thyristors. The following common approach is used to clarify the degree and mechanisms of influence of defects/states on the device characteristics.

1. Evaluate defects/states in the device by optical or electrical measurement, and reflect the result in technology computer aided design (TCAD) simulation model.
2. Measure the device characteristics and compare them with the simulation results; then, make the simulation model more accurate.
3. Simulate the physical phenomena inside the device structure including defect/states behavior.

In Chapter 1, the backgrounds and objectives of this research are described.

In Chapter 2, we describe the basic theoretical background and review the previous literature. We also describe the basic approach of TCAD simulation here.

In Chapter 3, we clarified the relationship between the enhanced leakage current of SiC JBS and 3C-SiC inclusions that were a type of SF. The SF structure was identified by photoluminescence (PL) mapping and cross-sectional transmission electron microscopy (TEM). Numerical simulations of the I–V characteristics considering local lowering of Schottky barrier height at the Ti/3C-SiC contact area, which was 0.8 eV lower than that of Ti/4H-SiC Schottky barrier, explained the 4–6 orders of magnitude increase in reverse leakage current caused by SFs.

In Chapter 4, we investigated the mechanism of positive threshold voltage V_{th} shift by wet oxidation without a significant decrease in field effect mobility μ_{fe}, focusing on the variations in interface state density D_{it}. The μ_{fe} increased from 3.27 to 26.4 $cm^2/(V{\cdot}s)$ by nitridation. Then, V_{th} was shifted +0.52 and +0.71 V by wet oxidation at 700 and

800 °C, respectively, without significantly decreasing mobility. After wet oxidation at 900 °C, mobility became 60 % of the nitridation sample. By combining DLTS and ICTS, we obtained D_{it} measurements for a wide energy range without exceeding the upper temperature limit of the device (450 K). Compared to the nitridation-only sample, the relatively deep states at $E_c - E_t = 1.2$ eV were increased by an order of magnitude of 10^{11} $\mathrm{eV^{-1}cm^{-2}}$ due to wet oxidation at 700 and 800 °C without a significant increase in relatively shallow states. On the other hand, the relatively shallow states at $E_c - E_t = 0.2$ eV increased by an order of magnitude of 10^{12} $\mathrm{eV^{-1}cm^{-2}}$ after wet oxidation at 900 °C. The simulations of transfer characteristics using D_{it} measurement results were also conducted to quantitatively investigate the relationship between V_{th} and D_{it}. Considering the measured D_{it}, the simulated V_{th} accurately reproduced the actual value well. In this simulation, interface states deeper than $E_c - E_t = 0.2$ eV are affected V_{th}.

In chapter 5, we developed the simulation model for an optically triggered thyristor, focusing on the lifetime, which depends on the bulk traps, and response to incident light. The model accuracy, especially the minimum incident light intensity to turn-on $I_{0\mathrm{min}}$, was compared to experimental results. We estimated the lifetime from the holding current, and we considered the literature values of the refractive index, penetration depth, and quantum efficiency. The simulation results of $I_{0\mathrm{min}}$ accurately reproduced the actual values at $V_{\mathrm{ak}} = 300$ V. We also evaluated the influence of the drift-layer lifetime τ_{drift} and wavelength λ on the $I_{0\mathrm{min}}$. When the carrier lifetime of the drift layer τ_{drift} improved from 0.4 μs to 10 μs, $I_{0\mathrm{min}}$ was reduced by 1/30 times.

In Chapter 6, we summarize the outcomes, discuss the challenges for the future, and conclude this thesis.

With regards to the SiC JBS, SiC MOSFET, and SiC optical triggered thyristor, TCAD simulation models for predicting characteristics based on the information of crystal defects/interface states were constructed. Then, we quantitatively analyzed the influence of crystal defects/interface states on SiC power device characteristics to improve performance and reliability of SiC power devices.