

論文 / 著書情報
Article / Book Information

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種別(和文)	論文要旨
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論文要旨

THESIS SUMMARY

専攻 :
Department of Physical Electronics 専攻

申請学位 (専攻分 博士
野) : Doctor of (Philosophy)

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Academic Degree Requested
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要旨 (英文 800 語程度)
Thesis Summary (approx.800 English Words)

This dissertation presents a study of synthesizable phase-locked loop (PLL) for clock generation in CMOS technology.

Firstly, the basic theory of voltage controlled oscillator (VCO) is introduced and the VCO phase noise models are explained in details. In order to understand analog PLL more clearly, the PLL theory is illustrated step by step. After that the background of Digital PLL (DPLL) is given and time to digital converter (TDC) is explained in architecture and advantages or disadvantages.

Traditional analog circuits have moved towards digital-intensive or all-digital designs during the past few years. While taking advantage of digital circuits in scaled CMOS technology, digital-intensive or all-digital designs still cannot be absorbed in digital design flow. By using injection locking technique, a low-power, low-cost and high performance fully synthesizable PLL can be implemented using digital standard cells without any modification, and automatically place-and-routed by a digital design flow without any manual placement. Moreover, phase-interpolative coupled oscillator is proposed to reduce the phase mismatch and current output digital-to-analog converter (DAC) is utilized as the frequency coarse tuning without degrading the load balance. This design achieves a FoM of -236.5dB with the layout area of 0.0066mm². Thanks to the injection locked PLL (IL-PLL) advantages, this chip achieves super small area with comparable power, jitter.

Even though the above design can achieve good performance, however, the DAC can be improved by exploiting feedback technique. The proposed feedback current output DAC used in the synthesizable PLL reduces 30% power consumption and improves the frequency linearity largely. On the other hand, stochastic time-to-digital converter (STDC) is adopted to improve the resolution. By fully using the uncertainty of automatic place-and-route, the proposed STDC can achieve -10ps to 10ps detection range with a relatively linear gain. In the design of STDC, only D flip-flop (DFF) is used and is linear compared with conventional delay-line-based TDC when fully implemented with digital design flow.

In the IL-PLL design, the oscillator phase noise is very critical for the whole system performance such as phase noise, jitter and FoM. To further improve the phase noise performance, a low-jitter mostly synthesized phase-locked loop based on injection-locking technique, with LC-based digitally controlled oscillator (DCO), is proposed. Different from ring-based DCO used in the conventional synthesizable injection locked PLL with a high reference, LC-based DCO is firstly proposed based on 3-input NAND for a low-reference IL-PLL. It achieves a FoM of -250.3dB, the best one among synthesizable PLLs. The synthesizable PLLs can achieve comparable performance with low power and small area. In order to achieve a comparable performance with ring oscillator based IL-PLL, LC-DCO based IL-PLL can use a relatively low reference frequency.

Lastly, in order to satisfy the frequency resolution requirement, a Fractional-N IL-PLL is investigated. In order to relax the deteriorate spur level due to injection locking, and soft injection technique is employed to improve the spur performance. A 28 phase coupled ring oscillator is utilized to generate multi-phase, while the gating controller is used to control logic which determine the phase of the injection signal. With exploiting the fractional-controller, a fine time resolution around $TDCO/(28 \cdot 2^{16})$ can be achieved and fractional operation is achieved. This is the firstly synthesizable Fractional-N injection locked PLL implementation.