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Doctoral Thesis

A New Resistive Switching Based on Breakdown and Anodic Re-Oxidation of Thin SiO_2 at the Interface of CeO_x Buffer Layer and Silicon Related Bottom Electrodes

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Abstract

Rapid advances in information technology rely on the high performance computer system. As the manufacturing technology of semiconductor devices is moved to smaller and smaller geometries, so does the dimension of all components inside the computer system. Thanks to its smaller dimension of the semiconductor devices, the operation speed of the computer system becomes faster. But a significant performance gap between memory and storage in the recent computer system remains a big issue in the development of the computer system in the near future. Already poor speed performance of a flash memory, as a storage device in a computer system, is a bottleneck. This is because there is a tradeoff between access speed and endurance performance. Thus, finding a new type of memory, so called storage class memory (SCM), is indispensable to replace the role of flash memories in the computer system. The resistive random access memory (ReRAM) is one of the strong candidates as SCM among all emerging memory technologies, owing to its great potential of scaling, low programming voltage and fast speed operation with excellent retention properties. There are, however, some problems on the conventional ReRAM, such as the requirement of

forming process to apply a higher voltage than the normal operating voltage condition to initiate the switching and low on/off ratio.

In this thesis, a new type of ReRAM has been proposed in order to solve these problems of the conventional ReRAM technology. A bi-layer high-k and low-k dielectric structure is proposed as the resistive switching medium instead of single oxide layer such as in the conventional MIM structure ReRAM. Bipolar resistive switching characteristics of a CeO_x layer on Si-based bottom electrode (BE) were presented. Owing to the formation of a thin SiO_2 interfacial layer (SiO_2-IL) between the CeO_x layer and BE, the bi-layer structure was formed and the set process was triggered by a local breakdown at the thin SiO_2-IL due to large differences in dielectric constants. Reset process, on the other hand, was obtained by a local anodic oxidation of the breakdown spots due to the high oxygen ion conductivity of the CeO_x layer. Owing to high insulating properties of the SiO_2-IL, a large resistance ratio at high-resistive-state (HRS) to low-resistive-state (LRS) over 10^6 can be obtained. Moreover, a forming-free feature can be achieved by employing $NiSi_2$ as a silicon-based BE material.

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Chapter 1:

Introduction

1.1 Background of This Study

The computer system has been facing a problem of the access-time gap between memory and storage device. As the manufacturing technology of semiconductor devices is moved to smaller and smaller geometries, following the scaling rule, so does the dimension of all components inside the computer system. Thanks to the miniaturization of semiconductor device, the operation speed of CPU logic and access time of cache memory become faster. But a significant performance gap between memory and storage in the recent computer system still remains a big issue in the development of the computer system.

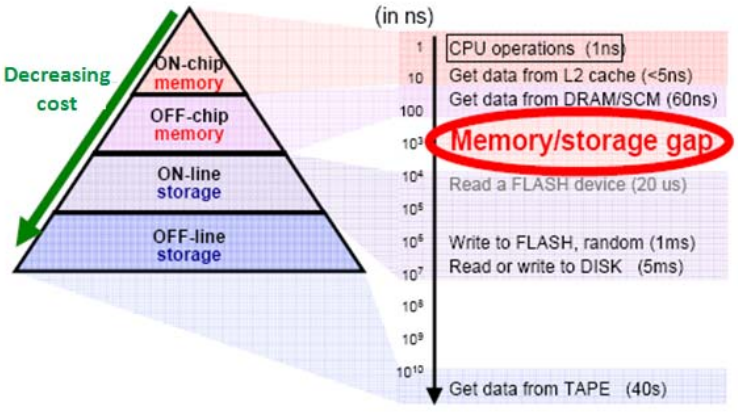


Figure 1.1 Memory hierarchy of conventional computer technology in the recent generations [1.1]

The poor speed performance of the flash memory, as a storage device in the computer system, limits the speed performance of the computer system. This is because there is a tradeoff between access speed and endurance performance. Thus, finding a new type of memory, so called storage class memory (SCM), is indispensable to mitigate the performance gap in the computer system. This idea of using SCM as a new type of memory in the computer system was proposed by IBM [1.1]. Then SONY also showed the same idea [1.2]. Applying the SCM in the computer system will change the memory hierarchy as shown in Figure 1.2.

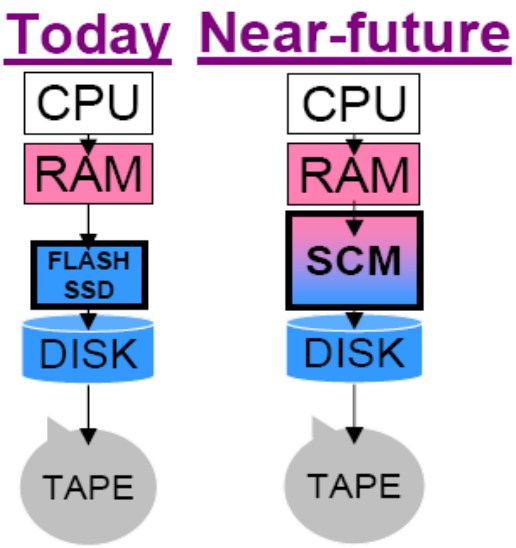


Figure 1.2 CPU and memory hierarchies, before and after using SCM [1.1]

The SCM application is not restricted to the computer system but also can be used for many other applications such as smart phone, digital music players, flash drive,

external hard drive, etc. For the embedded applications, this new type of memory must have high switching speed with low power consumption that is better than the performance of DRAM. For the storage application, it must have high device density at least the same level or higher than that of the flash memory. To fulfil these requirements, a new type non volatile memory is needed to be implemented.

A target memory capacity for SCM is from several GByte to hundreds GByte for the embedded memory application, and several TByte for the storage application. A key of large capacity SCM is shrinking the cell size as small as possible. ReRAM and the other alternatives thus have been getting particular attention to be used as SCM [1.1], owing to their great potential of scaling.

1.2 Current Memory Technologies

1.2.1 Static RAM

SRAM uses bistable latching circuitry to store each bit. Unlike dynamic RAM (DRAM), static RAM (SRAM) does not need to be periodically refreshed. SRAM exhibits data retention, but it is still volatile because the data are eventually lost when the memory is not powered.

A typical SRAM cell is made up of six MOSFETs, as shown in Figure 1.3.

Each bit of the single SRAM cell is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are representing the data 0 or 1. Two additional transistors (M5, and M6) are used to access a storage cell during read and write operations. SRAM is more costly and less dense than DRAM and is therefore not used as a high-capacity, memory block such as the main memory of the personal computer. The access time of SRAM is the fastest among various types of memories, typically less than several or one nano seconds, SRAM is used as a cache memory of the processor.

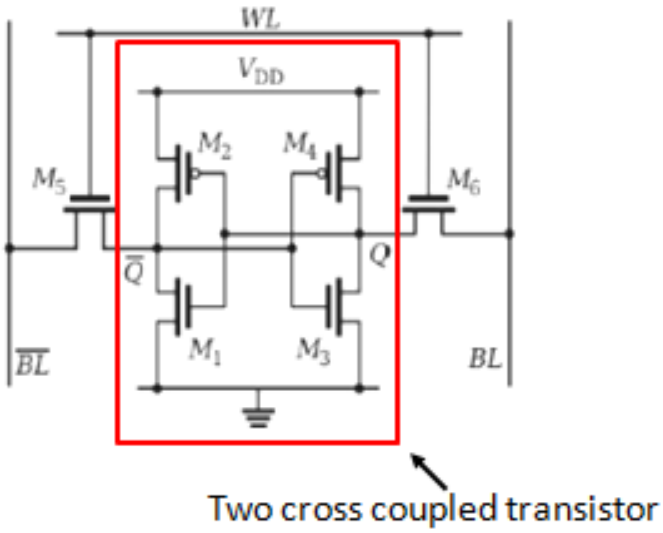


Figure 1.3 Schematic diagram of typical SRAM cell [1.21]

1.2.2 Dynamic RAM

DRAM stores each bit of data in a separate capacitor embedded nearby transistor within an integrated circuit. The capacitor has two states of either charged or

discharged. These two states represent the two values of a bit, known as 0 and 1. The advantage of DRAM is its simpler structure than SRAM. A cell of DRAM is consisted of only one transistor and one capacitor per bit. Figure 1.4 shows an example of a simple DRAM cell array with a four by four cell matrix.

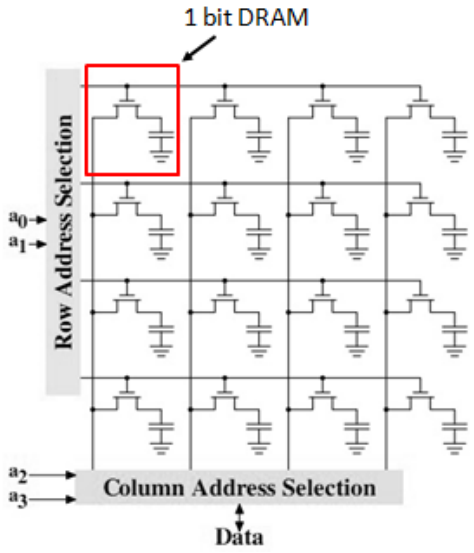


Figure 1.4Typical schematic of four-by-four DRAM matrices

DRAM must be refreshed periodically to prevent data from disappearing. This is because the capacitors will slowly discharge due to a small amount of leakage current of the transistors in the DRAM array. DRAM chip must equip a circuit to refresh all the cells approximately 20 times a second, depending on its capacitance value. Because of this refresh action, it is a dynamic memory as opposed to SRAM and other static memory. As DRAM cells decrease in size, the capacitor must shrink down. Lower capacitance means shorter retention (discharge) time. So it is necessary to refresh the

capacitor more often. Increase of capacitance density by either stacked or trench capacitor structure will increase the capacitance, but the power consumption will also increase.

1.2.3 Flash Memory

The flash memory stores information in an array of memory cells composed of floating-gate transistors. In the conventional single-level cell (SLC) memories, each cell stores only one bit of information. Modern flash memory technology has a variation of multi-level cell (MLC) devices, typically triple-level cell (TLC) devices.The devices can store more than one bit per cell by choosing multiple levels of electrical charge injected to the floating gate of each cell.

Figure 1.5 shows the typical structure of flash memory cell. By injecting different amount of electrons into the floating gate, the threshold voltage of MOSFET which can represent different state changes. The issues of the flash memory are trade-offs between high speed, with low power operation and long retention time: high speed with low power requires a smaller charge amount injected to the floating gate from the channel, whereas long retention time requires a large charge amount in the floating gate.

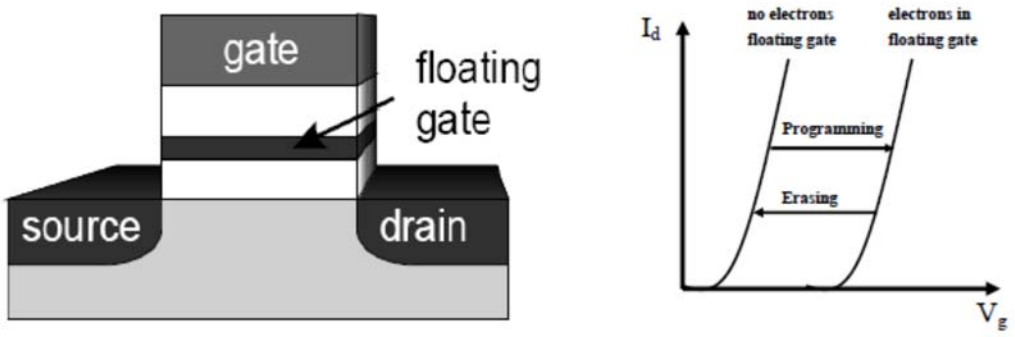


Figure 1.5 Flash memory and its floating gate structure[1.4]

As feature size of the flash memory cell shrinks, or the number of bits per cell increases, the number of electrons in a single bit should decrease. Eventually, the number of electrons will get too small to be reliably read or stored. Improved signal processing and error correction circuit (ECC) can help, but these carry their own overhead in chip size.

There are two main types of flash memory, NOR and NAND logic gates. In NOR gate type flash memory, each cell connected directly to ground at one end, and the other end connected directly to a bit line. NOR flash acts like a NOR gate: when one of the word lines is pulled up to high level, the corresponding storage transistor acts to pull down the output bit line to low level. On the other hand, NAND flash acts like a NAND gate: several transistors are connected in series, and the bit line is pulled low only if all word lines are pulled high, that is, all the series transistors are ON. Both NOR and NAND type flash memory has an issue of high power consumption because it requires a

higher programming voltage of about 12 V.

The NAND type flash memory also has a limitation in programming and erasing process. Although it can be read or programmed a byte or a word at a time, it can only be erased a "block" at a time. To do this, usually all bits in the block must be set to 1. Then on this freshly erased block, any location within that block can be programmed. But, once a bit has been set to 0, it cannot be changed back to 1 unless by erasing the entire block.

Table 1.1 shows a comparison of incumbent memory technologies. There is a significant performance gap between DRAM and flash memory giving a strong suggestion for the implementation of new technology to fill this gap.

Table 1.1 Comparison of DRAM, SRAM and Flash memory [1.4]

	SRAM	DRAM	Flash Memory
Write Time	0.2 ns	<10 ns	1 ms
Erase Time	0.2 ns	<10 ns	0.1 ms
Read Time	0.2 ns	<10 ns	0.1 ms
Retention Time	Voltage dependent	64 ms	10 years
Endurance	$>10^{16}$	$>10^{16}$	10^4
Write Operation Voltage (V)	1	2.5	12
Read Operation Voltage (V)	1	1.8	1.8

1.3 Emerging researches for Storage Class Memory

1.3.1 Magneto-resistive RAM

Data in the magneto-resistive RAM (MRAM) are not stored as an electric charge, but by electrical resistance variation due to magnetic property change. The memory elements are consisted of two ferromagnetic plates and an insulator layer in between, each plate can hold a magnetic field, separated by the thin insulating layer. This structure is called as magnetic tunnel junction (MTJ). One of the two plates is a permanent magnet set to a particular polarity, while the other plate's field can be changed by applying magnetic flux or electrical current to store data.

The reading process is established by measuring the electrical resistance of MTJ. A specific cell is selected by applying voltage to the associated transistor that switches current from a supply line through the cell to ground. If the two plates have the same polarity, the resistance of MTJ is lower that is called as a low resistance state (LRS), while if the two plates are of opposite polarity the resistance increase to high resistance state (HRS).

Due to its high current consumption during a write process, the conventional type writing by magnetic flux, of MRAM cell will have difficulty to be used at high

memory densities. For this reason, a new technique is introduced, the spin transfer torque (STT) MRAM as shown in Figure 1.6. STT-MRAM uses polarized electrons to directly torque the magnetic domains. In principle, if the electrons flowing into the ferromagnetic (storage) layer that has to change its spin polarity, this will develop a torque to align the polarity to parallel or anti-parallel of the nearby reference layer. This method lowers the current needed to write the cells, making it about the same level as the read process.

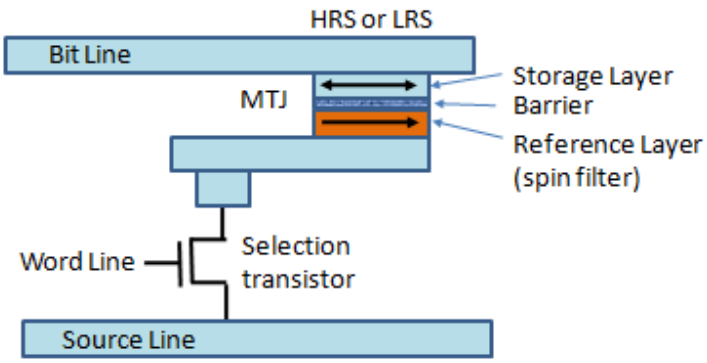


Figure 1.6 Typical STT-MRAM memory cell

However, in practical application achieving low switching current for STT-MRAM is difficult. Its resistance ratio between HRS and LRS, which is about 2 – 3 times is quite low for large memory system, so achieving tight distributions of magneto-resistive switching property is impossible. For the tiny size such as below 50nm, there is a serious problem with high-temperature retention. The conventional

MRAM and the STT-MRAM provides fast latency for switching their magnetic tunneling junction, however, it is difficult to be implemented for high memory capacity at present.

1.3.2 Ferroelectric RAM

Ferroelectric RAM (FeRAM) uses different dielectric polarization to differentiate on-off state. Dielectric polarization is done by applying voltage to the ferroelectric capacitor. After that, on-off state was detected by change of current caused by polarization inversion with applied pulse voltage. Structure of FeRAM is similar to that of DRAM whose paraelectrics capacitors are changed to ferroelectric capacitors [1.4]. Writing is done by applying an electric field across the ferroelectric layer by charging the plates on either side of it, forcing the dielectric polarity into the "up" or "down" orientation, that represent "1" or "0" state.

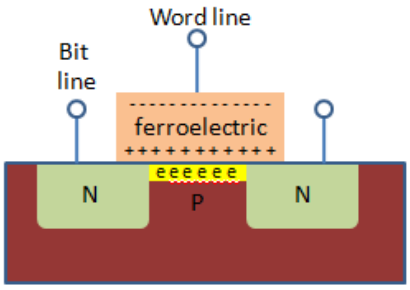


Figure 1.7 Typical FeRAM memory cell

The main disadvantages of FeRAM are that the storage density is considerably lower than that of other types of RAM. Since FeRAM cannot hold a great amount of data, it would be expensive to implement in the chip used for applications that require a lot of memory.

1.3.3 Phase Change RAM

Phase change RAM (PCRAM) uses the unique behavior of chalcogenide as a phase change matter. A heating element, generally made of TiN, would be used to heat the chalcogenide layer. When the layer is heated and quenched (quickly cooled), the chalcogenide layer will be amorphous and exhibit high resistance. On the other hand, the layer is heated and slowly cooled or held it in its crystallization temperature range for sometimes, the layer will be at a crystalline state and exhibit low resistance, see Figure 1.8. Switching between low-resistance crystalline, and high-resistance amorphous phases, is controlled through power & duration of electrical pulses. On-off state was detected by current through the bottom electrode to top electrode.

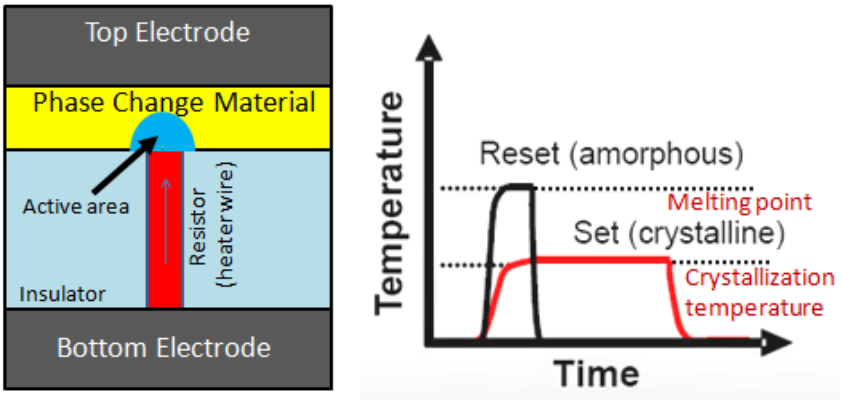


Figure 1.8 Typical PRAM structure and its switching mechanism.

The greatest challenge for the PCRAM is its high programming current density (>10^7 A/cm²) and the high density memory integration will be highly unlikely. This requires that the active cell area is much smaller than the driving transistor area to reduce the programming current. This discrepancy has forced the phase-change memory structures to package the heater and sometimes the phase-change material itself into sub-lithographic dimensions. Other challenges are its long-term resistance and threshold voltage drift. The resistance of the amorphous state slowly increases. This severely limits the ability for multi level cell (MLC) operation.

1.3.4 Resistive RAM

The basic structure of resistive RAM (ReRAM) is that a dielectric layer sandwiched between two electrodes, which is normally insulating, can be made to be conductive by applying a voltage. In other words, the resistance of the insulator layer

changes from high resistance state (HRS) conventionally known as “0” state to low resistance state (LRS) for “1”. ReRAM has a potential to be a front runner among other non-volatile memories. Compared to PRAM, ReRAM operates faster, while comparing to MRAM, it has a simpler, smaller cell structure. Compared to the flash memory, a programming voltage is lower, therefore it can be used in low power applications such as battery operated appliances. Details of ReRAM will be described in the next section.

Figure 1.9 shows a trend of emerging non volatile memories after [1.1], in terms of scaling limit. As mentioned earlier, high memory cell density is required for the SCM application. Based on this trend, only ReRAM and PRAM has a strong potential that can have a comparable memory density to NAND flash as a future storage class memory. Due to its strong potential as an SCM candidate, the number of research about ReRAM is growing year by year, as shown in Table 1.2.

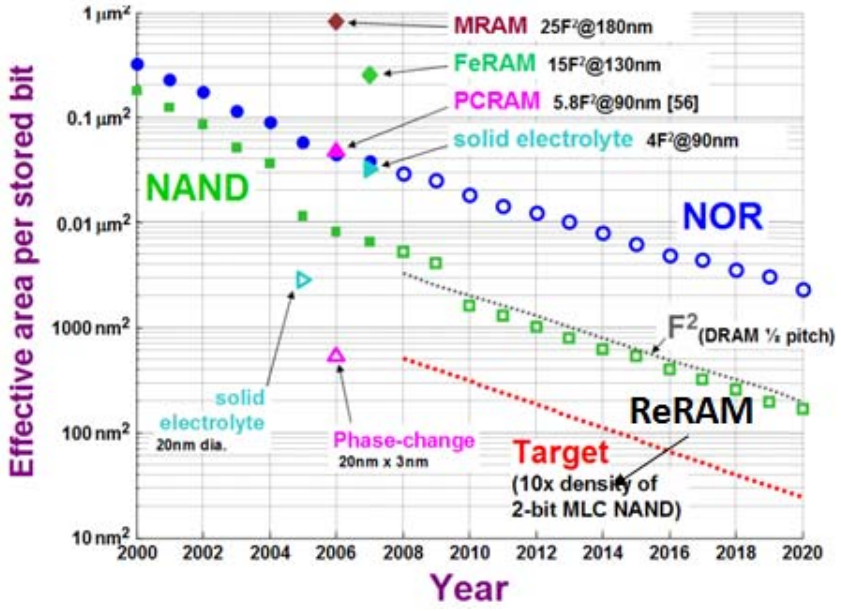


Figure 1.9. Scaling trend of emerging memory candidates for SCM[1.1]

Table 1.2. Trends of published article about ReRAM in IEEE journals and proceedings

Year	2006	2007	2008	2009	2010	2011	2012	2013
Published article	7	11	27	44	87	145	174	235

Table 1.3 Comparison of recently reported ReRAMs

	N:AlOx VLSI 2011	TaO_x/Ta_2O_3 VLSI 2011	Hf/HfOx IEDM 2011	TiO_xN_y/SiO_2 IEDM 2012	Ni/HfO_2 IEDM 2012	Parylene-C IEEE EDL 2013	HfO_x/LTO IEEE EDL 2013
Switching type	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar
structure	1T-1R	1R	1T-1R	1T-1R	1T-1R	1R	1R
Cell area (μm^2)	~1	~9000	0.0001 (10nm)	0.03	0.01 (100 nm)	~4	0.0004 (20nm)
Speed	N/A	~10 ns	~10 ns	500ns	N/A	N/A	1 μs
Peak voltage	<2V	<2.5V	<1.5V	<3V	<3V	3.7 V	<2.2V
Peak current	~50 nA	~30μA	~50 μA	~60 μA	20nA	150 nA	10μA
HRS/LRS ratio	>100	>100	>10	>30	>100	>10	100
endurance	10^5	10^{12}	$5x\ 10^7$	10^6	10^2	10^2	10^8

Besides its strong feature for high density storage class memory application, ReRAM faces some weak points that might be less competitive compared to other non-volatile memory. Most of the ReRAMs seem to operate based on conductive filament model, that exhibits low on/off resistance ratio, see Table 1.3. The low on/off ratio is not desirable in the SCM application. ReRAM cells with low on/off ratio cannot be used in a 3D ReRAM architecture that is suited for the ReRAM array with a large memory capacity required for the SCM application. The parasitic capacitance of the 3D structure comes from the diode, that is usually needed as a selector device, will significantly reduce the on/off ratio of cell arrays [1.3]. Another problem of ReRAM is the forming process to initiate the resistive switching, that is undesirable in a practical application. Memory chip using ReRAM, that requires large forming voltage, needs high voltage tolerable memory driver circuit. Only large device meets this requirement, total memory chip size thus becomes larger. Therefore, research in this area needs a new concept to enhance the performance of the device.

1.4 Introduction to Resistive Random Access Memory (ReRAM)

The first study related to ReRAM has been known for over 40 years ago [1.17]–[1.20]. Using oxide layer sandwiched between two metal electrodes, resistive change phenomena were observed. Those results, however, remain in the domain of

scientific studies, until Samsung presented a paper at the International Electron Devices Meeting (IEDM) 2004 [1.6]. They successfully demonstrated that NiO based memory cells can be integrated by using the conventional 0.18-μm complementary metal–oxide–semiconductor (CMOS) process in a one-transistor–one-resistor (1T1R) structure. A complete set of memory characteristics such as data retention, endurance, and programming characteristics was shown in the paper, and it suggested that ReRAM technology may be feasible. Moreover, its compatibility with back-end-of-the-line (BEOL) fabrication temperature envisioned that the ReRAM can be stacked in 3D in a crosspoint architecture [1.31].

Resistive switching devices with metal oxides have been attracting great attention as one of the non-volatile memories for next-generations, owing to low voltage and fast operation with excellent retention properties. The resistance of these oxides from high-resistance state (HRS) to low-resistance state (LRS) and vise versa is triggered by threshold voltage or current, and both states can be retained without applying power, see Figure 1.10.

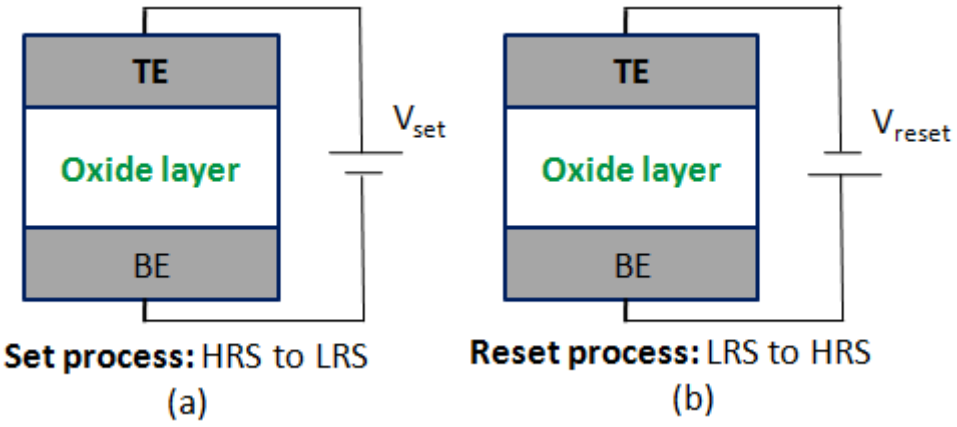


Figure 1.10 Basic concept of switching event in ReRAM: (a) Set process, (b) Reset process

ReRAM with a MIM structure is theoretically simple. However, the switching behavior itself is still unclear. With different combination of metal electrodes and oxide materials, the switching behavior may be different [1.5]. Soft breakdown ReRAM or so called the conductive-filament switching model ReRAM, as illustrated in Figure 1.11, where both states are determined by the annihilation and creation of the oxygen vacancies at the tip of filaments within the oxides [1.8] is very widely accepted as a model to explain the switching mechanism.

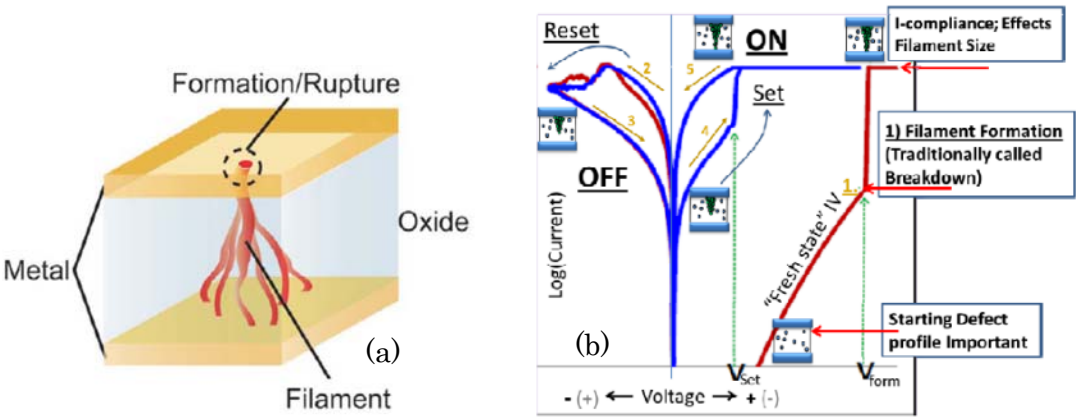


Figure 1.11 Conductive filament model of ReRAM (a) Schematic illustration[1.8]

(b) Typical I-V curve[1.1]

The on-state resistance of the conductive filament model of ReRAM is reported to depend on the maximum current during the set switching [1.22]. On the other hand, experimental results revealed that the power used for reset switching should exceed that for set switching, as the reset process is driven by power [1.23]. Although the dependence can be utilized as multilevel programming, precise current limit control to overcome the large variability in on state resistance still remains as an issue. Besides, creation of filaments using electroforming process is required before resistive switching, which involves high voltage application to create chains of oxygen vacancies. In addition to complicated circuit design and are overhead for electroforming process, the power consumption cannot be neglected for the large scale memory chip integration. A

recent study on defect-rich AlON resistive switching devices has shown the initial creation of the filament at a low voltage, which is comparable to the set voltage, achieving forming-free resistive switching [1.24]. However, the HRS/LRS ratio is still around 100 as the switching mechanism is still based on the conductive filament model.

1.4.1 Structure of ReRAM

The structure of a single ReRAM cell has a very simple capacitor-like structure as shown in Figure 1.11(a), in which an insulating or semiconducting oxide is sandwiched between two metal electrodes. The typical I-V curve is shown in Figure 1.11 (b), a forming voltage is needed to initiate the switching as indicated in the figure with a curve from the “fresh state”. Fig.1.12 shows simple memory matrices of ReRAM cell arrays. Word and bit lines are used for selecting a memory cell and writing or reading data, respectively. To prevent sneak current, ReRAM also need a selector device. In addition, the storage density is determined by the feature size of the fabricating process. Conventional ReRAM memory metrics use a transistor as an ReRAM selector device. Recent memory technologies use diode as selector device instead. A strong benefit of using diode as a selector device is the potential manufacturability of 3D ReRAM architecture.

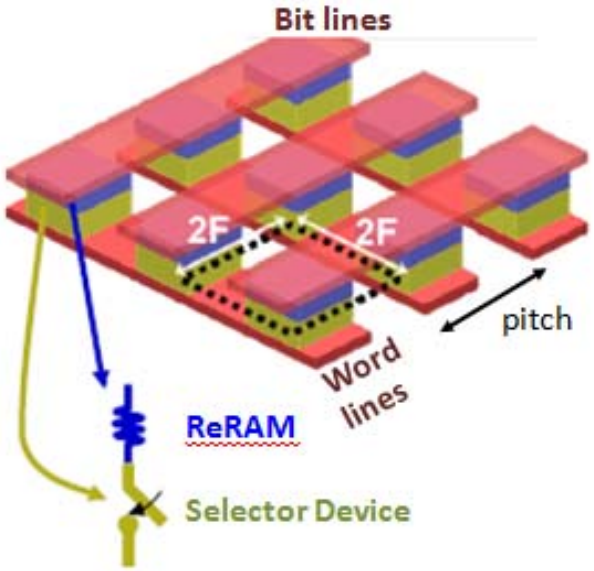
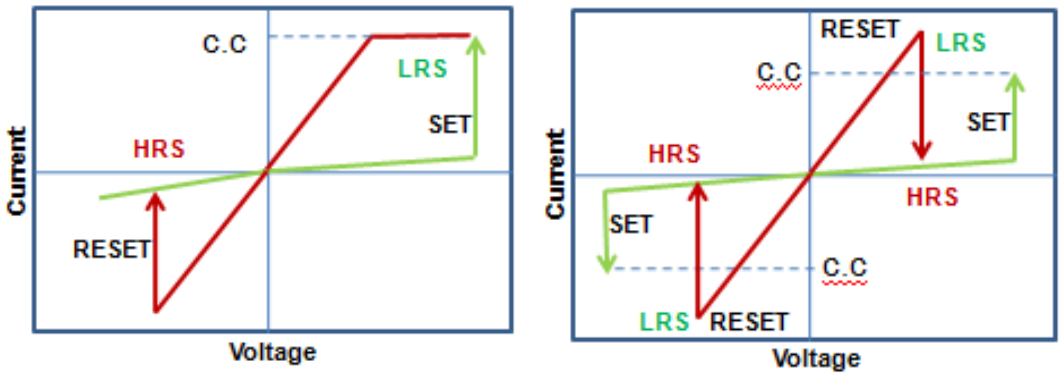


Figure 1.12 Structure of ReRAM and its selector device in memory matrices[1.1]

1.4.2 The Switching Modes of ReRAM

The switching modes of the metal–oxide ReRAM is classified into two switching modes: unipolar and bipolar, see figure 1.13.If the switching direction can be driven by one polarity of bias voltage, the device is called unipolar switching device. On the other hand, if the device has to be driven with different polarities of bias voltage, the device is called bipolar switching device. Therefore, in the bipolar switching mode, set process can only occur at one polarity and reset process can only occur at the reverse polarity.



(a) (b)

Figure 1.13 Two basic operation schemes of ReRAM: [1.3] (a) Bipolar, (b) Unipolar

The switching modes of the conductive filament model ReRAM is usually can be predicted by only based on the electrode materials selection [1.3]. Two ReRAMs with the same oxide material, but with different electrode materials have different switching modes. In most cases, the unipolar mode is obtained with noble metal electrodes both for top electrode (TE) and bottom electrode (BE). If one of the electrodes is replaced by an oxidizable material, the bipolar mode will be obtained, see Figure 1.14.

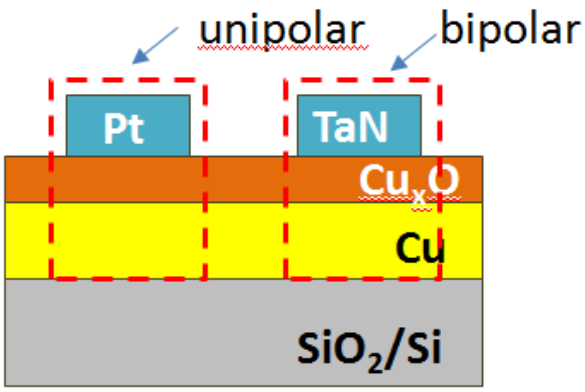


Figure 1.14 Top electrode selection and switching mode of ReRAM [1.7]

1.4.3 Current Conduction

Understanding current conduction behavior from TE to BE or vice versa in an ReRAM both for set and reset process is necessary in order to understand its I-V curve characteristic. Many reports discussed about current conduction in the conductive filament model ReRAM [1.25-1.30]. Most of the reports clearly clarify that the current conduction in reset process is just either ohmic or having a linear I-V relationship. On the other hand, the current conduction in set process is still unclear. During the set process usually TE voltage is higher than BE voltage. By applying a set voltage, electrons flows from BE to TE through the oxide.

There are many potential mechanisms for current conduction in the set process as illustrate in Figure 1.15. The explanation of each mechanism is described as follows: (1) Schottky emission: thermally activated electrons are injected over a barrier into conduction band oxide. (2) Fowler–Nordheim (F–N) tunneling: when the electric field

is high enough, electrons tunnel from the BE (cathode) into the conduction band via a thin notch near the interface. (3) Direct tunneling: when the oxide is thin enough, the electron tunnel from cathode to anode directly.

If there is a trap in the oxide such as oxygen vacancy, current conduction can change: (4) tunneling from cathode to traps, followed by schottky emission; or (5) tunneling from cathode to traps, followed by F-N like tunneling. If there are a number of traps in the oxide, current conduction occurs by (7) tunneling from cathode to a trap, followed by trap to trap hopping and tunneling from a trap to anode. Electrons would seek the easiest way among all the possibilities.

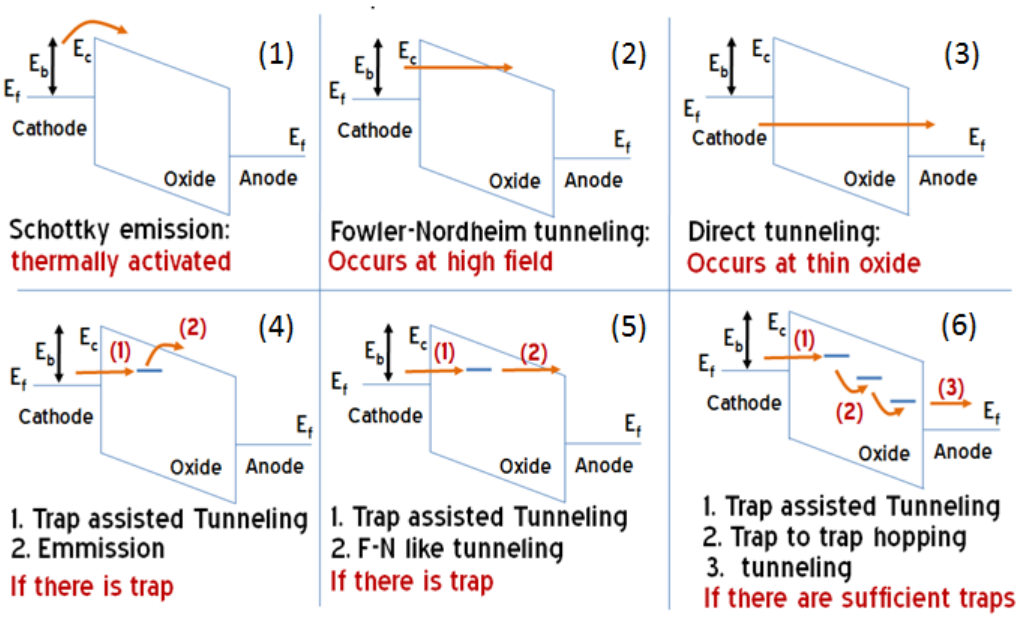


Figure 1.15 Schematic of possible electron conduction paths through a MIM stack during set process, adapted from [1.3]

1.4.4 Forming Process

Usually for the fresh samples with its initial resistance state, a voltage larger than the set voltage, so called forming process, is needed to initiate the switching process. The forming process in the fresh ReRAM is based on a dielectric soft breakdown process [1.9]. Under high electric field exceeding 10 MV/cm, oxygen atoms are knocked out of the lattice, and drift toward the anode. Instantly, defects in the bulk oxide are generated. The chain of either oxygen vacancies [1.10] or metal precipitates [1.11] leads to the formation of conductive filaments (CFs). The CFs are preferentially generated along the grain boundaries, which were confirmed by the conductive-AFM method [1.12].

Figure 1.16 shows an illustration of the forming and the set processes in the conductive filament model. As the number of intrinsic defects in fresh samples is few, a high forming voltage is needed to initiate the switching process. After the forming process, sufficient numbers of defects form in the oxide layer and the resistance changes from HRS to LRS. In the following switching cycles, the reset process recovers the defects, and it changes the resistance back to HRS. But a portion of the defects, which is the ones near one side of electrodeare, still remaining. This is why the resistance in HRS is much smaller than that in the fresh sample. In the set process, a lower positive bias

voltage than its initial one is required to change the resistance from HRS to LRS.

Apparently an ReRAM device, which requires the forming process, is not desirable in the practical applications, because the forming process requires complex memory control units. Thus, many efforts have been made to achieve the so-called forming-free ReRAM devices. Lee et al. [1.13] successfully eliminated the forming voltage by thinning the HfO_x oxide thickness down to 3 nm. Other ways can reduce the forming voltage are introducing defects by preparing the films under the condition to be oxygen deficient [1.14]–[1.16]. However, all of them need highly precise control of the fabrication process. If there are too many defects in the oxide the on/off ratio might drops.

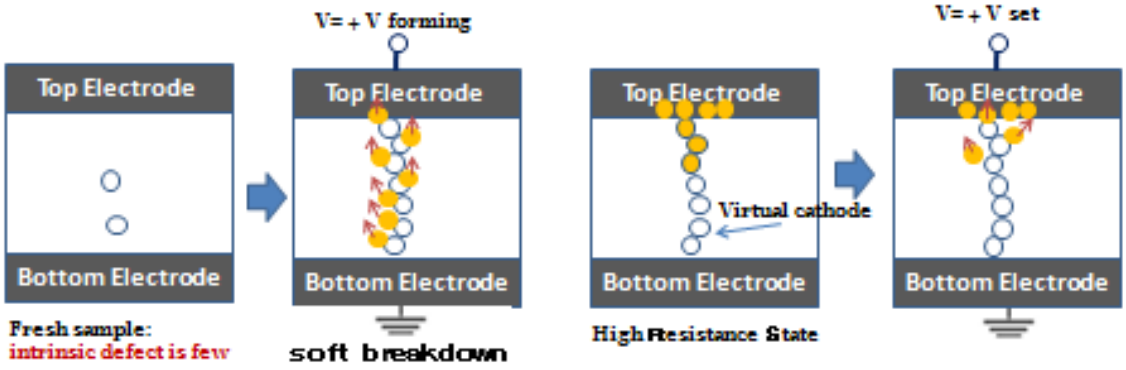


Figure 1.16 Forming process and set process in conductive filament model

1.4.5 Retention Time

The retention time characteristic of the resistive switching device is a key device performance that characterizes the possible utilization of ReRAM as a

non-volatile memory device. Retention time represents the period of time the stored data should be kept or retained. In practical applications, a data retention time longer than 10 years is required for nonvolatile memory [1.3]. This retention must be maintained at thermal stress up to 85ºC, 105ºC, 125ºC or even 150ºC, depending on the application. Understanding of the mechanism of the time relaxation process of stored bits may be essential to improve the retention performances.

1.5 Purpose and Organization of This Study

The purpose of this study is to introduce a new concept of resistive memory based on the breakdown and anodic re-oxidation phenomena, without the forming process that has been mandatory for the conventional resistive memory, while the on/off ratio of the device must be larger than 10^4. Thereby contributing to the realization of a high device density of storage class memory with programming voltage lower than 5V, which is more suitable for low power devices including battery driven appliances.

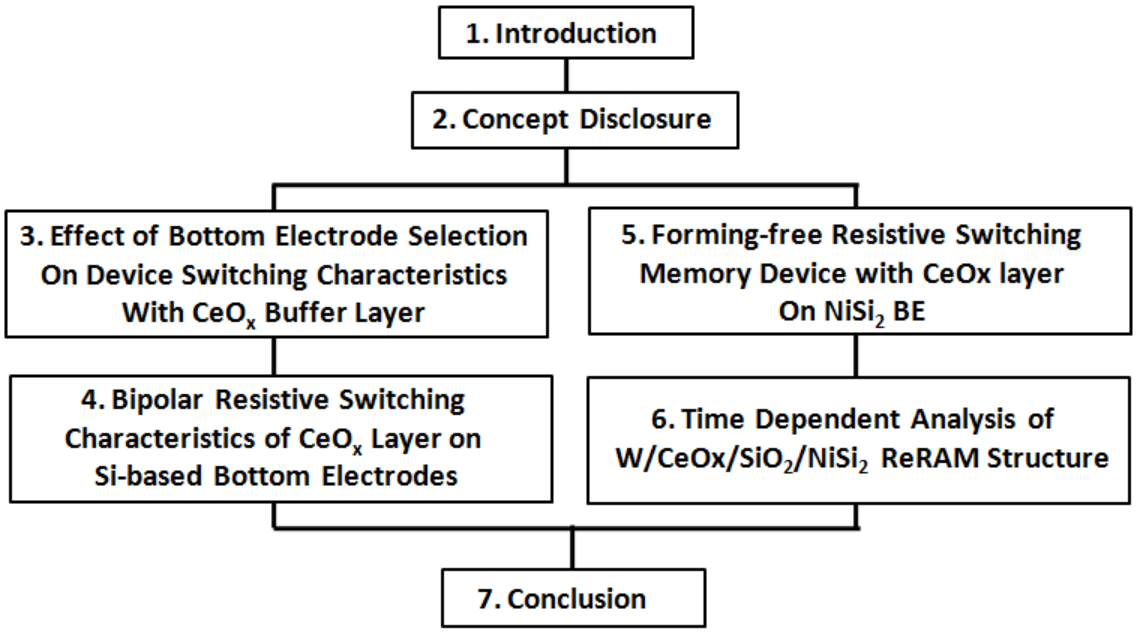


Figure 1.17 Outline of this thesis.

This thesis consists of seven chapters. The flow chart of the thesis is shown in Fig. 1.17. The contents of each chapter are briefly described as follows.

In Chapter 1, the necessities for realizing storage class memory with excellent features such as high capacity and fast switching operation is described. Then the details of incumbent memory and all emerging candidates for storage class memory are described. Next, an introduction of ReRAM which is one of the strongest candidates for storage class memory is explained. Lastly the motivation and the organization of this thesis are presented.

In Chapter 2, the concept of the new ReRAM in this study is disclosed. The

working principle of the proposed ReRAM model is described. ReRAM device key features such as switching speed, endurance, retention time, and device density are also discussed.

In Chapter 3, effect of bottom electrode (BE) selection on the switching properties of devices with a CeOx buffer layer is discussed. Using various BE material such as W, Ni, Ti and TiN, the resistance switching showed different switching behavior.

In Chapter 4, bipolar resistive switching characteristic for device with Si-based BE on CeO_x buffer layer is discussed. Effect of BE annealing is also described.

In Chapter 5, the switching behavior of devices with $NiSi_2$ BE is discussed. By taking the discussion in the previous chapters into account, a new resistive switching device with the bi-layer structure of CeO_x and SiO_2 is described. CeO_x thickness dependence on set voltage is also described. In addition, the effect of BE annealing on the compliance current is discussed.

In Chapter 6. Time dependent analysis of devices with $W/CeO_x/SiO_2/NiSi_2$ structure is discussed in order to check the validity of the proposed model. Then device endurance and operating speed are discussed.

Lastly, Chapter 7 summarizes the achievements of this thesis. Future research recommendations that are worthy of further development of ReRAM device is presented.

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Chapter 2:
Concept Disclosure

2.1 Introduction

Resistive switching devices with metal oxides have attracted great interests as one of the non-volatile memories for the next-generation, owing to low voltage and fast operation with excellent retention properties [2.1- 2.2]. The resistance change of these oxides from high-resistance state (HRS) to low-resistance state (LRS) or vice versa is triggered either by voltage or current larger than a threshold, and both states can be retained without power supply [2.3].

The change in the states has been explained based on the conductive-filament switching model, where both states are determined by the annihilation and the formation of the oxygen vacancies at the tip of filaments within the oxides [2.4], as illustrated in Figure 2.1. The resistance at LRS of resistive switching devices is reported to depend on the current compliance (CC) or current limit, during set switching [2.5]. On the other hand, experiments have revealed that the electrical power used for reset switching, from LRS to HRS, should exceed that consumed for set switching, as reset process is basically a Joule heating to annihilate the oxygen vacancies driven by power [2.6].

Although the switching with this mechanism can be utilized as multilevel programming, precise current limit control to overcome the large variability in resistances still remains as an issue [2.7]. Besides, the requirement to form filaments using an initial electroforming process before the resistive switching, which involves high voltage application to form chains of oxygen vacancies, is still another issue [2.1]. In addition to complicated circuit design for the electroforming process, the power consumption of this process cannot be neglected with a large scale memory chip.

A recent study on defect-rich AlON resistive switching devices showed the formation of a filament at low voltage, which is comparable to set voltage, achieving forming-free resistive switching [2.8]. However, the on/off ratio is still on the order of 10^2, because the switching mechanism is still based on conductive switching. Resistive Switching Memory discussed in this thesis is bipolar type ReRAM. Thus the current polarity is different polarity for set process and reset process [2.1].

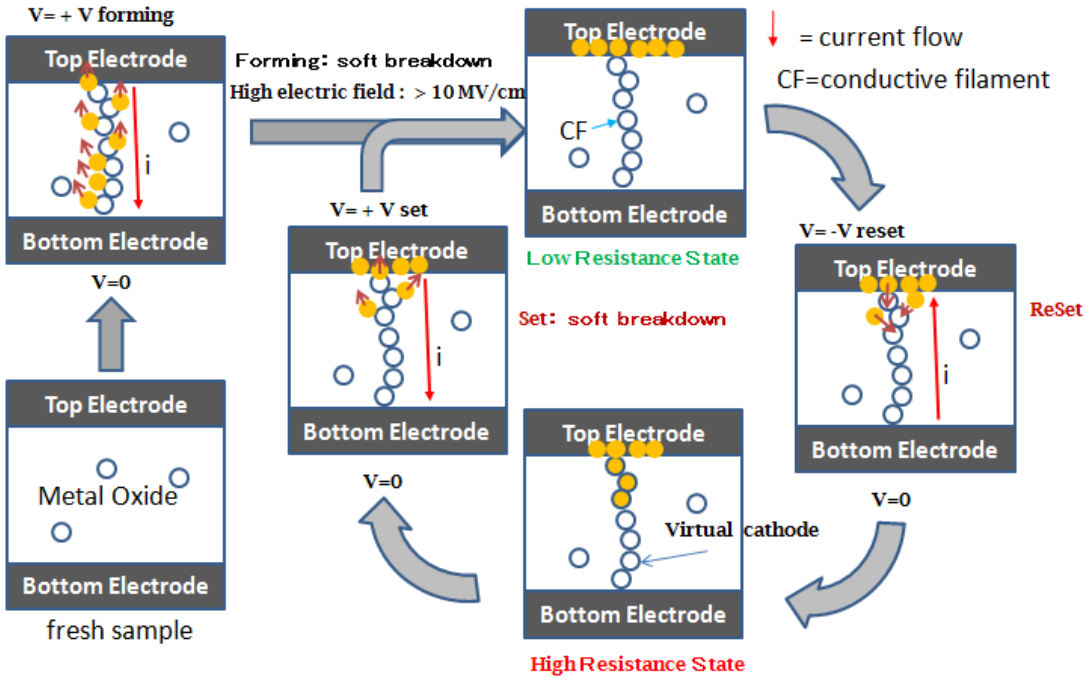

Figure 2.1 Switching process of conventional ReRAM, adapted from [2.1]

2.2 Proposed Model for New ReRAM

As mentioned in the previous chapter, the main purpose of this study is to get ReRAM with high on/off ratio higher than 10^4 without requiring the forming process to initiate the switching in a programming voltage less than 5V. Only ReRAMs with high on/off ratio can be used for application with large memory capacity that will have a 3D-ReRAM architecture. And it is typically known that ReRAM with high on/off ratio tends to have a good device endurance. Without a forming process, small memory chip size can be achieved. In addition, It is reported that a downscaling of ReRAM size may

cause an increase of the forming voltage [2.1], so achieving ReRAM without a forming process will give a strong contribution in terms of ReRAM scaling technology.

The structure of the proposed ReRAM model is shown in Figure 2.2. In this thesis, the new ReRAM has a bi-layer (high-k and thin low-k) structure instead of single oxide layer such as in the MIM structure ReRAM. It is reported that ReRAM with bi-layer structure can be achieved due to reaction of metal oxide and the electrodes [2.16-2.17]. The low-k layer acts as a switching layer, while the high-k layer acts as a buffer layer. During the set process (+V), the buffer high-k layer has relatively smaller electric field than the low-k layer electric field to initiate breakdown spot in the low-k layer. This high-k layer also enhances re-oxidation of the anodic side with the reverse voltage application during the reset process (-V). The buffer high-k layer plays an important role as an oxygen reservoir in the set and reset processes. By applying a set voltage, oxygen ion from the low-k layer drifts to the high-k layer, and the resistance of the memory cell becomes low. Conversely, by applying a reset voltage, oxygen ion from the high-k layer drifts back to the low-k layer to recover the breakdown spot, and the resistance of the memory cell becomes high.

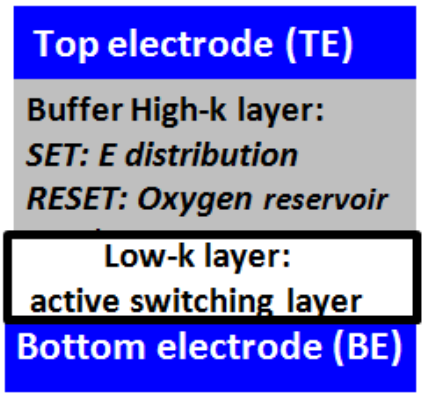

Figure 2.2 Proposed model of bi-layer structure with high-k and low-k layers

2.3 Oxide Material Selection

Material selection is an important factor to design the ReRAM. For the set process, buffer high-k layer is responsible for inducing a breakdown in the low-k layer so that the resistance state changes from HRS to LRS. In order to localize the breakdown spot only in the low-k layer, the breakdown electric field value of the buffer high-k layer must be a condition: $E_{BD}^{high-k} > (\epsilon^{low-k}/\epsilon^{high-k})E_{BD}^{low-k}$, where E_{BD}^{high-k}, E_{BD}^{low-k}, ϵ^{high-k}, and ϵ^{low-k} denote breakdown electric field of high-k layer, breakdown electric field of low-k layer, permittivity of high-k layer, and permittivity of low-k layer, respectively. For reset process, oxygen ions in the buffer high-k layer will re-oxidize BE, so the breakdown spot can be recovered. At the end of the reset process, the resistance state change from LRS to HRS. As set and reset process behavior is strongly depends on the oxygen ionic conductivity of buffer high-k layer,

selecting the best oxide material for the buffer layer is indispensable. The Guideline for buffer high-k layer and low-k layer oxide material selection is shown in Figure 2.3.

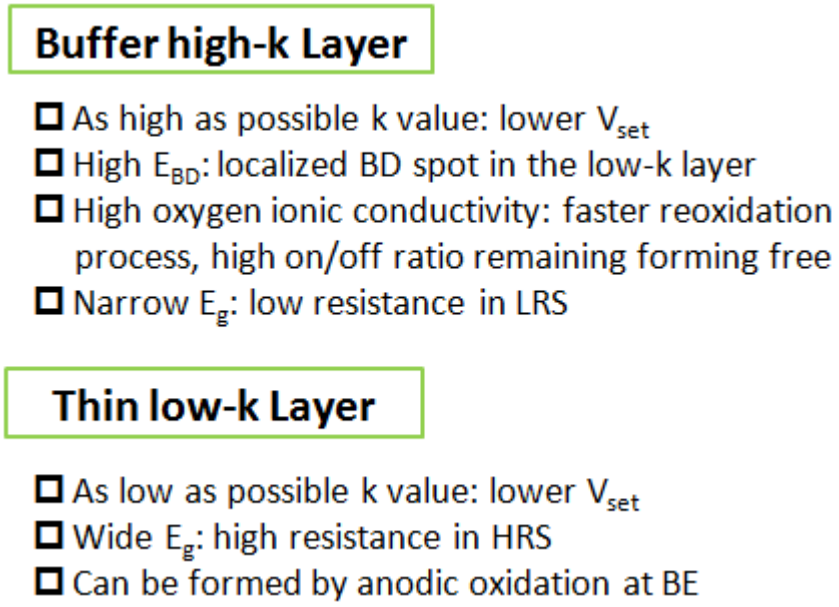

Figure 2.3 Guideline for the oxide material selection

Since current in LRS is mainly limited by the electron conduction in the buffer high-k layer, therefore a narrow band gap of high-k layer is preferable to get a lower resistance of LRS. While for buffer high-k layer there are numerous metal oxides as the candidates. Transition metal oxide are strong candidates, and the other candidates are lanthanide series metal oxides [2.1]. Figure 2.4 shows numbers of material candidates both for the high-k and the low-k layer. Based on the figure, buffer high-k layer strong candidate are CeO_x, TiO_2, BaO, YSZ, HfO_2, and Ta_2O_5, that are represent the high-k material with narrow band gap energy. While strong candidates for the switching layer

are low-k material with large band gap energy. SiO_2 is apparently the best oxide material for thin low-k layer. The electrode material selection is also an important factor, in this thesis bottom electrode material is selected based on its contribution on the formation of desired low-k layer. While for top electrode, metal that contribute as an oxygen reservoir are preferable. W is selected as top electrode, as it has good property for oxygen reservoir [2.15].

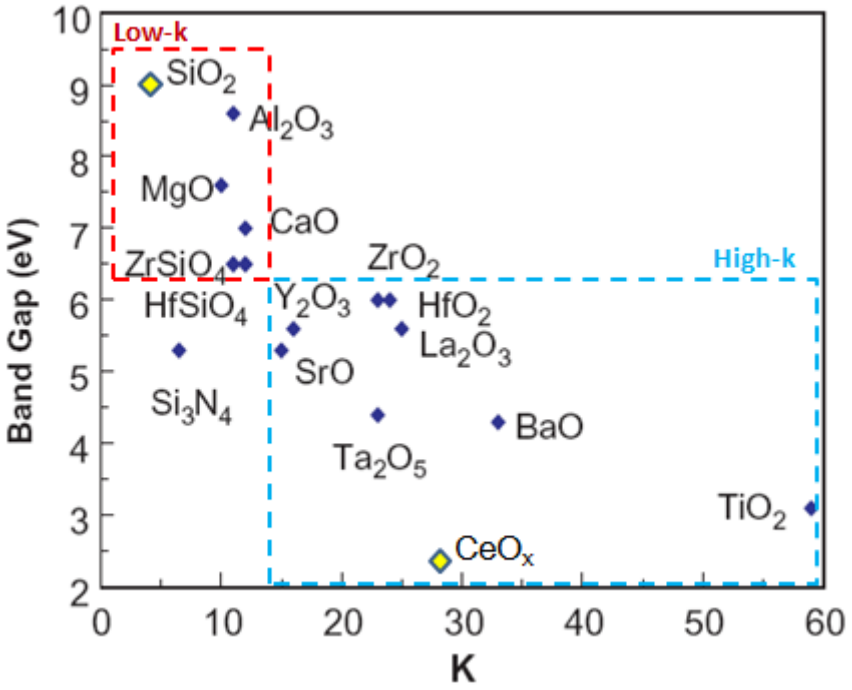

Figure 2.4 Band gap versus dielectric constants of oxide material candidates [2.9 - 2.10]

Poly yttria stabilized zirconia (YSZ) has reported to have high oxygen ionic conductivity in a wide range of temperature [2.11]. However, considering the operating

temperature for storage class memory applications: data server, computer memory, portable storage disk etc, maximum operating temperature of 105^0C will be in many cases is sufficient. Thus the search for buffer high-k material that has better oxygen ionic conductivity than that of poly-YSZ in the temperature range is necessary. Poly CeO_2 is reported to have higher oxygen ionic conductivity than that of poly YSZ in the temperature range of the SCM operation [2.12], as illustrated in Figure 2.3.

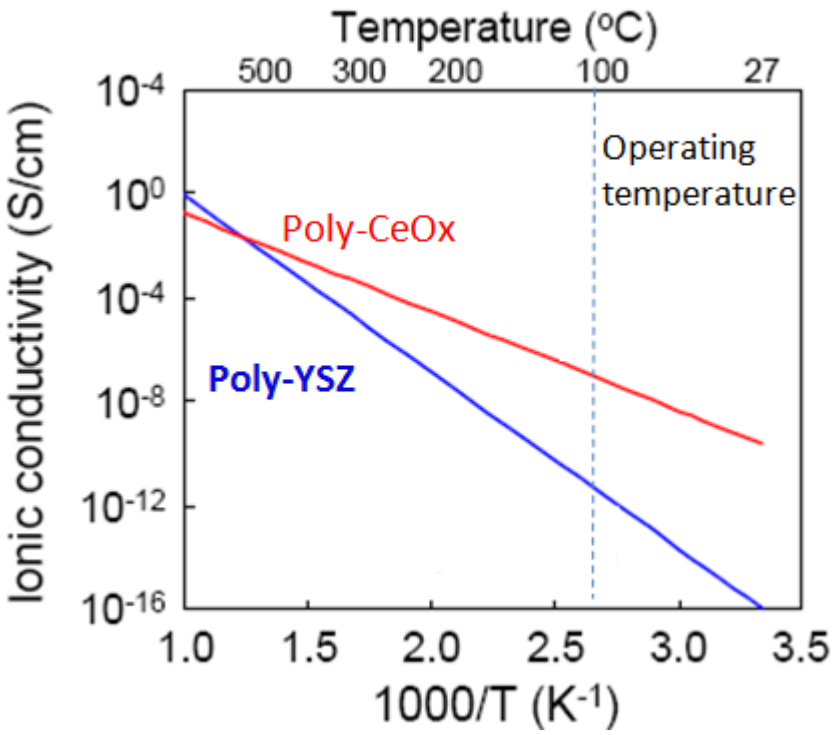

Figure 2.3 Oxygen ionic conductivity characteristic comparison between poly-YSZ and poly-CeO_x as buffer high-k layer strong candidate

2.4 Parameter for Set Process

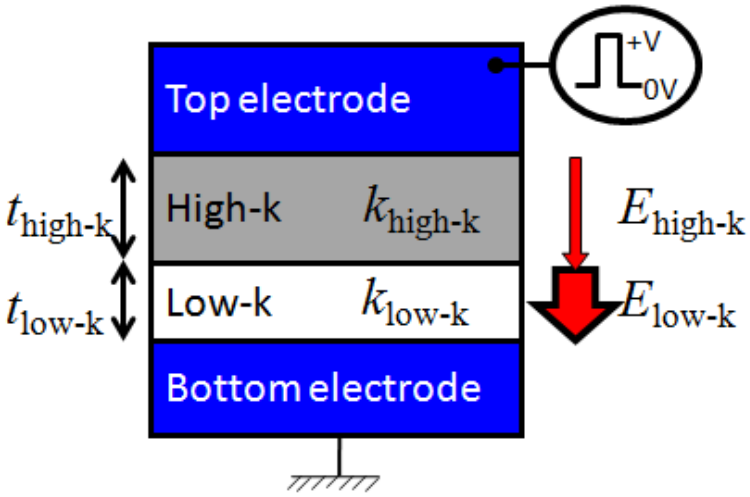

Figure 2.6 Model for set process mechanism

Based on a simple model for the set process as illustrated in Figure 2.6, the set voltage to form a break down spot in the low-k layer can be easily calculated. With a constant displacement throughout the bi-layer, the applied voltage V_{app}, can be expressed using equation 2.1

$$V_{app} = t_{low-k} E_{low-k} + t_{high-k} E_{high-k} \qquad 2.1$$

where, t_{low-k} as the physical thickness of the low-k layer, E_{low-k} as the electric field across the low-k layer, t_{high-k} as the physical thickness of the high-kand E_{high-k} as the electric field across the high-k. Since dielectric constants of low-k and high-k layer are different, the electric field in the high-k layer is proportionally smaller than that of the low-k layer.

Therefore, equation (2.1) can be expressed by only using the $E_{low\text{-}k}$ as:

$$V_{app} = t_{low-k} E_{low-k} + t_{high-k} \frac{k_{low\text{-}k}}{k_{high\text{-}k}} E_{low-k}$$

$$= \left(t_{low-k} + t_{high-k} \frac{k_{low-k}}{k_{high-k}} \right) E_{low-k} \qquad 2.2$$

Equation 2.2 indicates that the operating voltage depends on the thickness of the high-k layer. Therefore, it can be inferred that scaling the film thickness of the low-k layer can accomplish low operation voltage. Moreover, large contrast of dielectric constant value between low-k and high-k can also accomplish low operation voltage.

Assuming a certain breakdown field for low-k layer, the set voltage can be expressed.

$$V_{Set} = \left(t_{low-k} + t_{high-k} \frac{k_{low-k}}{k_{high-k}} \right) E_{BD.low-k} \qquad 2.3$$

In this study, SiO_2 was used as a low-k layer, as it has highest breakdown field value of 14 MV/cm among the candidates. Next, the effect of high-k layer thickness on the set voltage can be predicted, as shown in Figure 2.7. The black line represents the set voltage tendency of device,assuming relative permittivity of 28 for the buffer high-k layer, while the blue line represents the set voltage tendency assuming that the relative

permittivity is 16. The design guideline is: higher the dielectric constant ratio between high-k and low-k layer lower the set voltage.

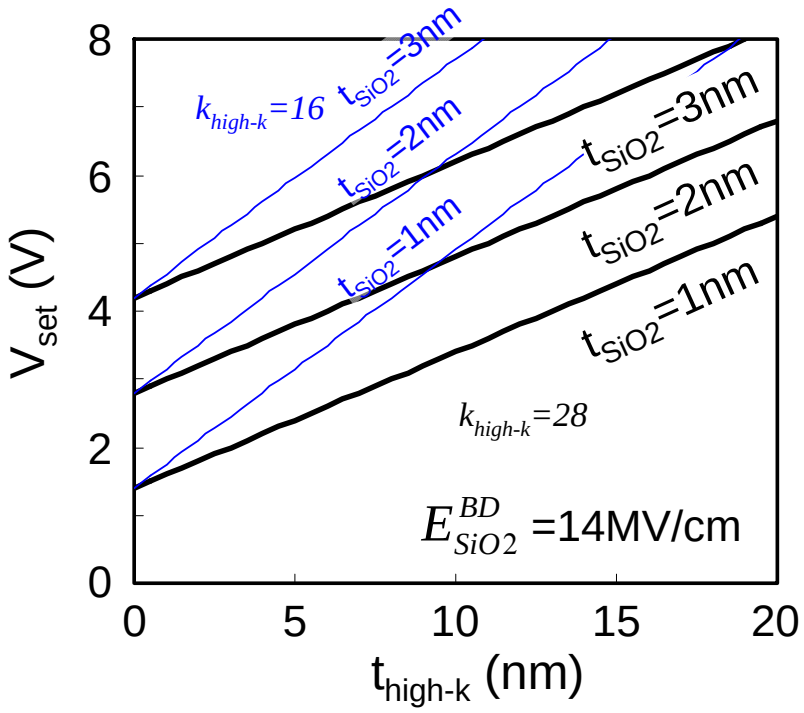

Figure 2.7 Model for set voltage on high-k layer thickness dependence

2.5 Parameter for Reset Process

Reset voltage application to the memory cell recovers the breakdown spot in the low-k layer. By applying negative voltage, oxygen ion in the high-k layer will drift back to the breakdown spot in the low-k layer, as illustrated in Figure 2.8. Resistance state therefore changes from LRS to HRS at the end of the reset process.

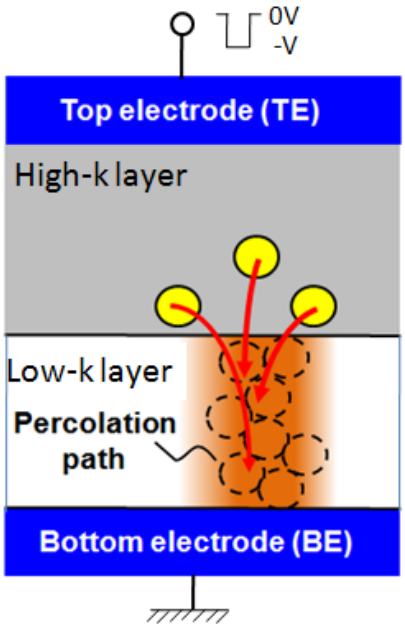

Figure 2.8 Model for reset process mechanism

In order to get a forming free behavior, the oxygen ionic conductivity of high-k buffer layer material must be high in order to perfectly recover the breakdown spot in the low-k layer. A simple method for achieving forming free ReRAM with high ON/OFF ratio, based on buffer layer material, oxygen ionic conductivity is illustrated in Figure 2.9.

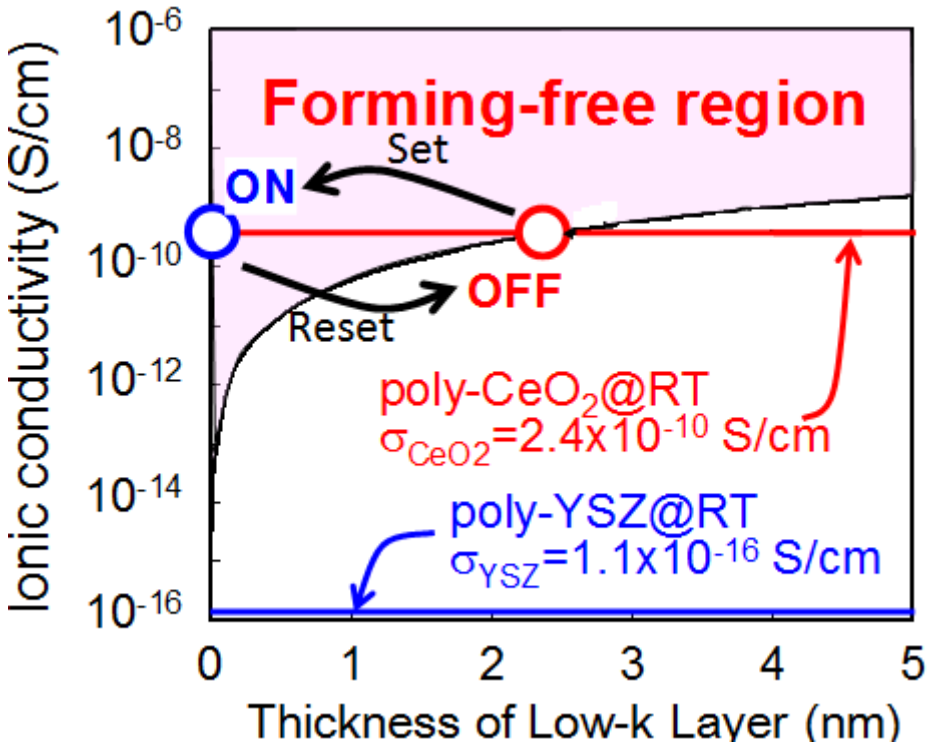

Figure 2.3 A method to achieve device with high on/off ratio without the forming process

2.6 Device Key Features

2.6.1 Switching Speed

The switching speed of ReRAM is determined by how fast the set process and reset process can complete. In the proposed device model, the set process time is considered to be determined by time to the breakdown process in the low-k layer. The breakdown process is initiated by oxygen ion drift from the low-k layer to the high-k layer when the electric field across the low-k layer reaches its breakdown electric field

value. Likewise, the speed of breakdown spot recovery will determine the reset process speed.

Selection of proper oxide material for the bi-layer ReRAM is important also to optimize the ReRAM switching speed. Selecting the high-k material with a high oxygen ionic conductivity of the buffer layer will increase the speed. In addition, the low-k layer thickness is also determines the switching speed. It is predicted that the thinner the low-k layer faster the switching speed.

2.6.2 Endurance

The ReRAM device endurance properties determine the maximum number of switching cycles until the switching failure. Usually, failure state of ReRAM is that stucking in LRS and being unable to reset back to HRS or vice versa [2.1]. In the proposed ReRAM device model, switching failure may occur when the high-k layer is unable to recover the breakdown spot in order to change the resistance state from LRS to HRS. A possible reason is due to either there is too large breakdown spot in the low-k layer or the oxygen ionic conductivity in high-k layer drop. Overshooting the set voltage may enlarge the breakdown spot, while temperature drop may cause the decrease in the oxygen ionic conductivity of the high-k layer.

2.6.3 Retention Time

Retention time represents the period of time the stored data should be kept or retained. Retention time longer than ten years is generally required for non-volatile memory. A comprehensive understanding of the physical switching mechanism of ReRAM device is needed in order to make reliable retention projections. Basically, there are two resistance states in ReRAM, HRS and LRS as illustrated in Figure 2.10. HRS represented by logic "0", while LRS is represented by logic "1".

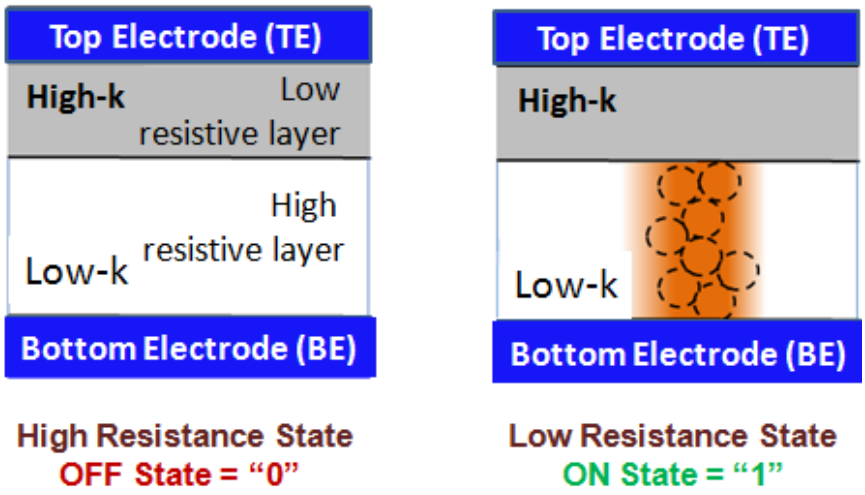

Figure 2.10 Representative states in ReRAM

The resistance in HRS can be expressed by equation 2.3

$$R_{HRS} = R_{\text{high-k}} + R_{low-k} \qquad 2.3$$

While the resistance in LRS is

$$R_{LRS} = R_{high-k} \quad 2.4$$

Retention time can also be described as how long time to failure, either in HRS or in LRS, without interference of applied voltage. There are three methods in the literature that are commonly used in order to predict the retention time behavior of ReRAM device [2.1]. The first one is to place the devices in a high temperature ambient, and monitor the device's resistance variation for a long duration by applying read pulses at certain time intervals, e.g., every 1 s, and extrapolate the resistance variation curve to ten-year point. While this method is easy to be implemented, however, it has a limitation, because the time dependence of resistance variation is not guaranteed to be steady. Abrupt resistance change or breakdown-like event might occur after a term of retention measurement [2.13].

Another alternative is to bake the device at elevated temperatures for an extended period and then read out the resistances at specific times (aftercooling down), e.g., after 1 day, 3 days, 1 week and so on. The third one is a temperature-accelerated method. Varying the temperature, record the time-to-failure for each temperature and draw the Arrhenius plot to extract the activation energy, and then extrapolate down to the operating temperature of the ReRAM device. By taking memory device to a high temperature, oxygen ion vacancy is generated due to oxygen ion drift to the electrode.

In this model, the retention time of the device is predicted by HRS error.

Since the proposed ReRAM device in this thesis has different switching mechanism compared to the conductive filament model ReRAM, the retention time behavior might be different. Generation of the oxygen vacancy in the buffer layer for devices with HRS will only slightly change the resistance of the device, because the resistance in the HRS is dominated by the resistance of the low-k layer. On the other hand, heating the ReRAM device at high temperature may trigger the oxygen ion drifted back from the high-k layer to recover the breakdown spot in a low-k layer that will change the resistance from LRS to HRS. This process is similar to the reset process. Even without applying voltage, oxygen ion may drift back to the breakdown spot at elevated temperatures.

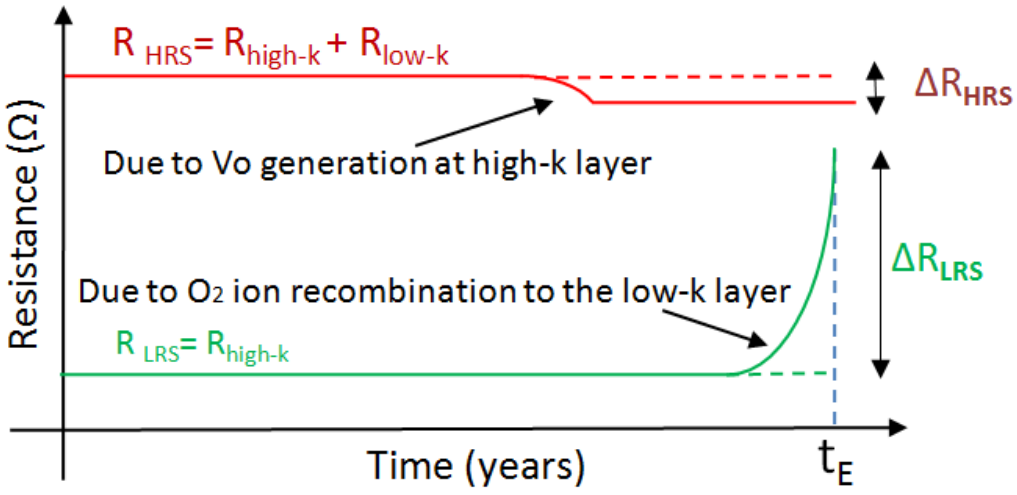

Figure 2.11 Proposed model for retention time extrapolation

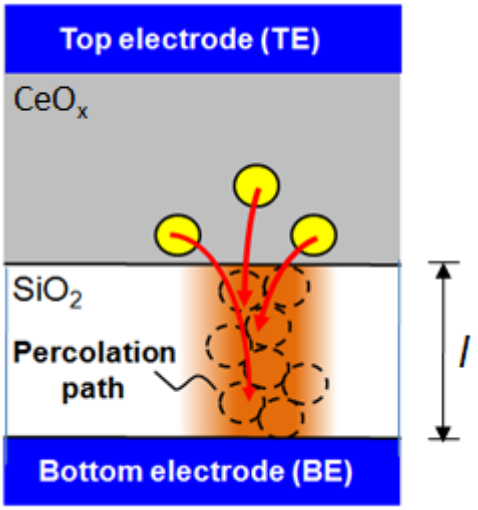

Figure 2.12 Illustration of reset process like phenomena in LRS failure model

By considering Figure 2.11 and 2.12, LRS failure will determine the retention time of the ReRAM device. To elucidate the reset like phenomena, the ion recombination model [2.14] as illustrated in Figure 2.13 is used.

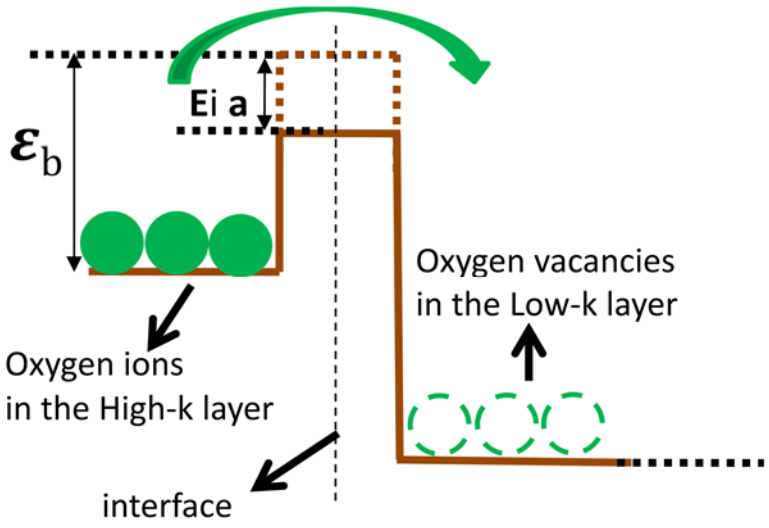

Figure 2.13 ion recombination model, adapted from [2.14]

The oxygen ion is accumulated near the interface of high-k and low-k layers. The mobile O^{2-} ions can jump over the interface barrier to recover the breakdown spot in the low-k layer under certain circumstance. Heating the memory device at high temperature may enhance the oxygen ion diffusion to recover the breakdown spot. Based on the diffusion and drift effect, the local O^{2-} concentration C_O(**r)** obeys the following equation [2.14]:

$$\frac{\partial C_0(x,t)}{\partial t} = D\left[ze\frac{\partial \varphi}{\partial x}\frac{\partial C_0(x,t)}{\partial x} + k_B T\frac{\partial^2 C_0(x,t)}{\partial x^2}\right] \quad 2.5$$

where $\boldsymbol{\varphi}$, D, T, kB, Ze, and l are electric potential in the oxide layer, diffusion coefficient, temperature, Boltzmann constant, electric quantity of O^{2-}, and oxide layer thickness, respectively. The drift effect appears only when there is a voltage applied in the system. In the retention time model, drift effect can be neglected, so equation 2.5 can be simplified as:

$$\frac{\partial C_0(x,t)}{\partial t} = Dk_B T\frac{\partial^2 C_0(x,t)}{\partial x^2} \quad 2.6$$

2.6.4 Device Density

Device density defines how large data can be stored for a certain memory die size. The requirement for the storage class memory is high device density and fast switching speed. So that it can fill the gap between flash memory and DRAM. There are

two general methods in order to increase the device density, by either exploiting the scaling limit or using multi bit operation so called multi level cell (MLC) operation.

Decreasing the device size is reported to alter the device property. For smaller device, higher on/off ratio can be achieved [2.1]. As mentioned in the previous chapter, that in memory chip contains memory cells and selector devices. Downsizing the selector device is an important factor to increase the device density. The selector device size is determined by its maximum current density. ON current is recognized as the peak current in memory cell [2.1]. Suppressing the ON current for scaled-down device, smaller current density flows throughout the selector device. And thus smaller selector device can be used.

MLC operation exploits the layout area of a memory device to realize more than one bit of digital data per cell [2.1]. In conventional ReRAM, MLC operation is performed by changing the resistance level, either in LRS or HRS, as illustrated in Figure 2.12. By applying different compliance current, different resistance level can be generated. Each resistance level represents a different bit state, which means that more data can be stored in one memory cell, that is the multiple number of resistance levels can be generated.

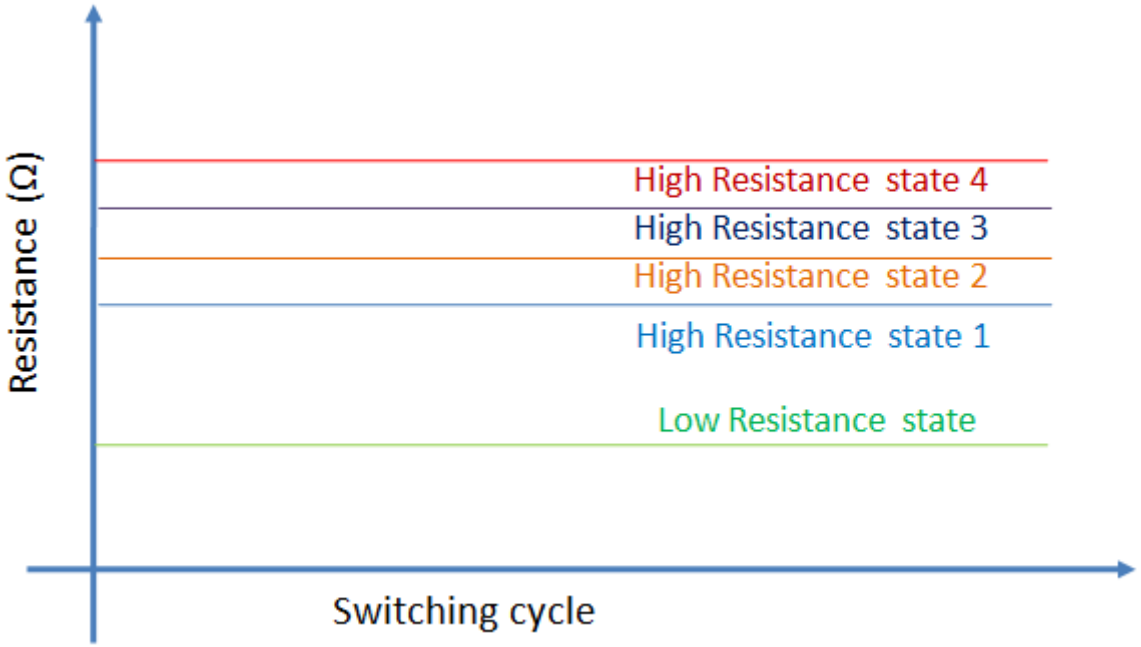

Figure 2.12 Resistance level in MLC operation

Basically, in bipolar type ReRAM, both positive and negative bias voltages can be used to trigger MLC operation. In the proposed ReRAM in this study, the set process is due to the breakdown process while the reset process is due to the re-oxidation process. Triggering the MLC operation using different set voltages is difficult in the practical application, on the other hand triggering MLC operation using different reset voltages will be much easier. The reset process in this study is almost similar to that in the conventional ReRAM. And basically these are the same redox reaction.

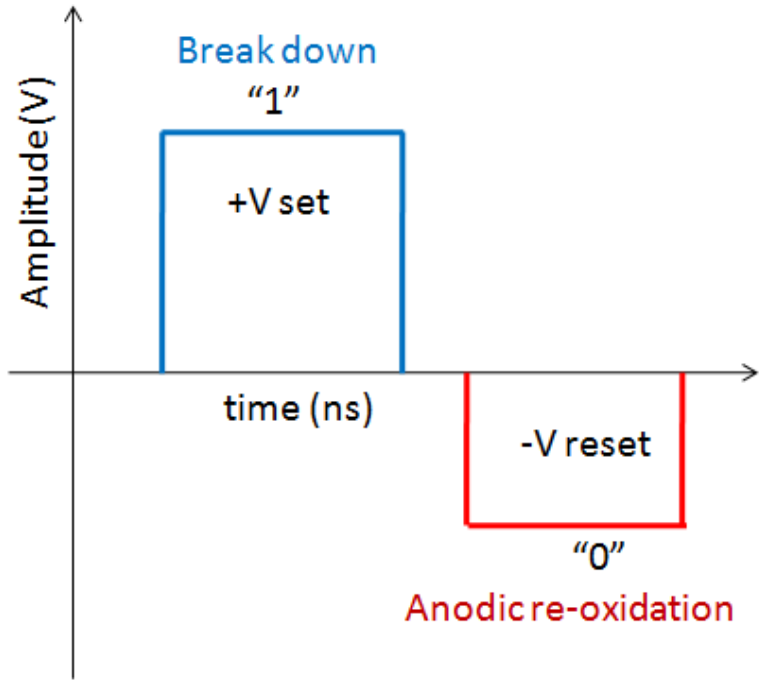

Figure 2.13 Switching voltage in SLC operation ReRAM

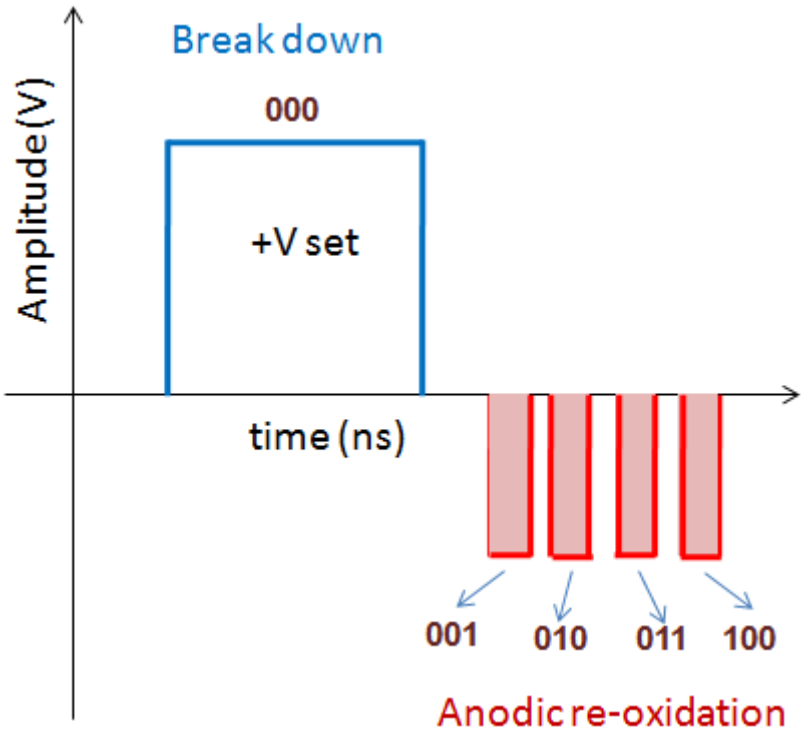

Figure 2.14 Switching voltage in MLC operation ReRAM

Figures 2.13 and 2.14 illustrate the switching voltage for single level cell (SLC) operation and multi level cell (MLC) operation of the ReRAM device of this study. The MLC operation is triggered by applying the reset voltages in order to generate different resistance levels. Assuming using the same reset voltage amplitude, applying a narrower pulse width than in SLC operation can generate different resistance level. The quantity of oxygen ion to recover the breakdown spot is controlled, as illustrated in Figure 2.15.

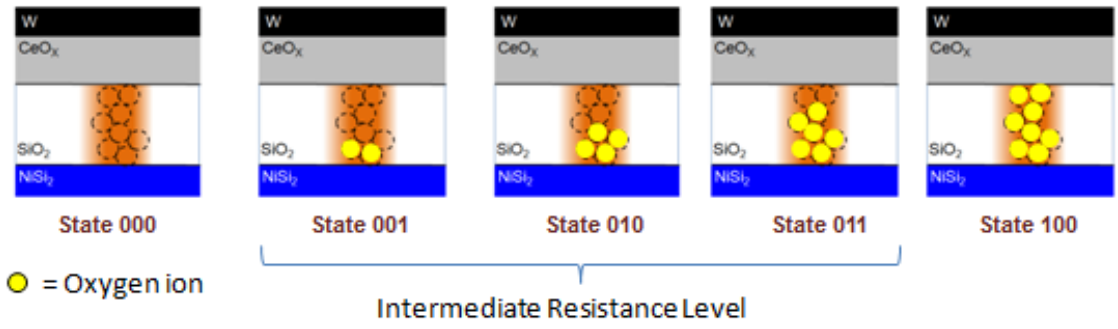

Figure 2.15 Physical illustration of different resistance levels of MLC operation

The switching cycle of the proposed ReRAM device in MLC operation mode is shown in Figure 2.16. In the initial state, the device is in the HRS state, by applying a set voltage the resistance changes from HRS to LRS, this state represents “000”. At the subsequent cycles, by applying reset voltages with narrow pulse width, resistance changes to different resistance levels, representing different bit values of “001”, “010”,

“011” and “100” respectively. A bit value of 100 in MLC operation mode is equal to HRS in SLC operation mode.

Figure 2.16 Switching cycle model of the proposed ReRAM device in MLC operation mode

2.7 References

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Chapter 3:

Effect of Bottom Electrode Selection On Device Switching Characteristics With CeO_x Buffer Layer

3.1 Introduction

In addition to its excellent feature for the ReRAM of this study, that is high oxygen ionic conductivity at room temperature [3.3] and narrow band gap energy [3.4], CeO_x is known to be composed of multivalent cations,which indicates to have a good property as an ReRAM buffer layer [3.1]. However, due to the self-compensating behavior to pin the oxygen chemical potential and hence the number of oxygen vacancies, the resistive switching is reported to be small for the ReRAM with Ce oxide [3.2]. Therefore, it is expected that there is a room for further improvement in the switching behavior if a proper reaction between the Ce oxide layers and electrodes occurs. Indeed, the electrode dependent resistive switching properties were reported for Hf oxide layer, suggesting the reactions between the dielectric layer and the bottom electrode is

influential to the ReRAM properties [3.5]. In this chapter, the effect of bottom electrode materials on resistive switching behavior with Ce oxide layer is discussed.

3.2 Device Fabrication Process

The basic device fabrication flow, used to process ReRAM devices with CeO_x buffer layer, is illustrated in Figure 3.1. A 200-nm SiO_2 layer was formed on *p* -Si substrate with an impurity concentration of $10^{18}cm^{-3}$ by thermal oxidation. The SiO_2 layer was lithographically patterned by a wet etching to form contacts between bottom electrode and substrate. Then bottom electrode layer (W, Ni, Ti, TiN) was deposited on the SiO_2 layer by RF sputtering. For depositing the TiN bottom electrode film, the reactive sputtering was used. N_2 gas was introduced into the chamber and then nitrogen reactive sputter deposition was done with Ti target to form nitride films. A 13-nm CeO_x film as a buffer layer, was deposited by electron-beam evaporation at 300ºC, followed by in-situ deposition of 50-nm-thick tungsten by rf sputtering as a top electrode. The top electrode was then patterned by a reactive ion etching (RIE) with SF_6 chemistry. Patterned W top electrodes (TE) with an area of (20×20) μm^2 were used to measure the electrical property of the device. Lastly, an Al layer was deposited as a backside contact.

For I-V curve characterization, a ramp voltage 0.05V/step ranging from -10V to + 10V were applied, using sweeping time of 640µs. I-V curve measurement setup is shown in Figure 3.2.

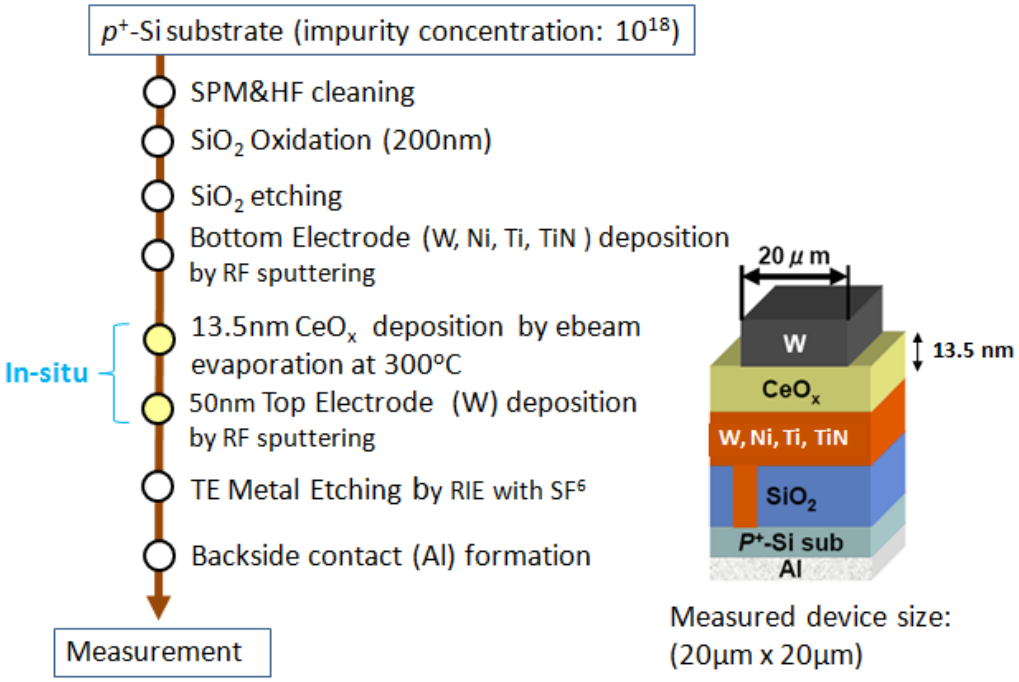

Figure 3.1Device fabrication processes of ReRAM with W, Ni, Ti and TiN BE

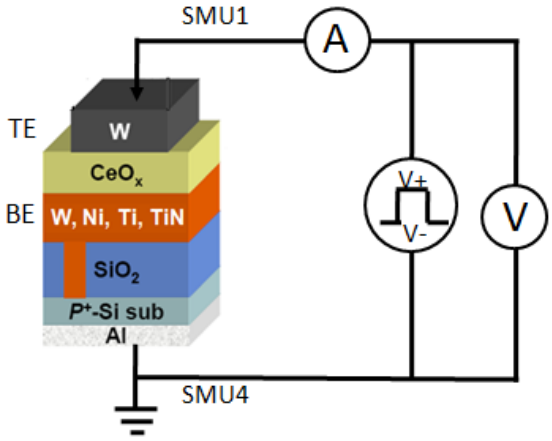

Figure 3.2 Measurement setup for I-V curve characterization

3.3 Switching Behavior of ReRAM with W BE

The resistive switching characteristics of ReRAM with W bottom electrodes is shown in Fig. 3.3. After the first voltage sweep, referred as initial, the voltage was swept to different polarity to achieve a reset process, then again the voltage was swept back to obtain set process. The switching behavior exhibited a bipolar type behavior, however, resistance change only could be observed in the reset process, while in set process was also essential. The I-V curve indicates no switching behavior between HRS and LRS.

A possible explanation for this behavior is that their switching properties weren't caused by changing the resistance in the CeO_x property itself [3.2]. But by changing the resistance of interfacial layer between CeO_x and BE, that is formed during the deposition of CeO_x. The interfacial layer at the initial state with fresh sample may either be too thin or have too many initial defects, once the current switches to LRS by applying the set voltage, it remains in this state indefinitely.

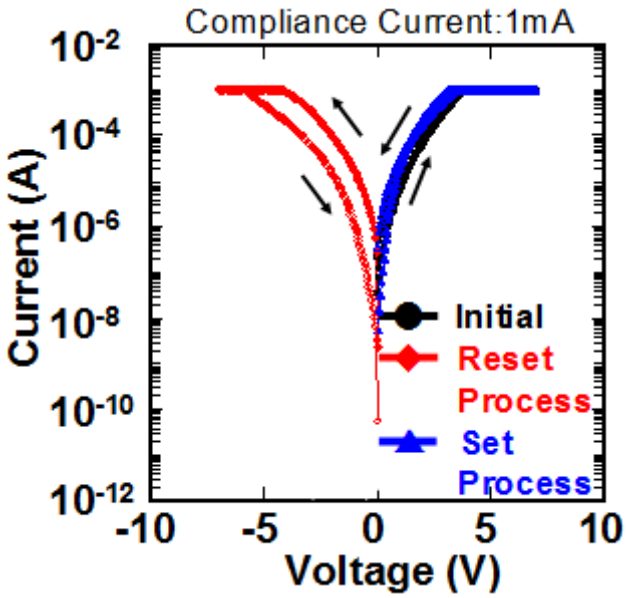

Figure 3.3 Bipolar resistance switching characteristics of W/CeO_x/W ReRAM

3.3 Switching Behavior of ReRAM with Ti BE

Figure 3.4 shows the switching behavior of ReRAM with Ti BE. After applying a voltage sweep to positive or negative directions the switching behavior shows almost the similar behavior to the ReRAM using W as BE. A small difference is that there is a little bit remarkable resistance change detected after set voltage applied. Possibly, there are many initial defects in the thin interface layer and the insulating property is low, applying reset voltage will repair some of them. On the subsequent cycle, applying set voltage will form an oxygen vacancy chain in the interface layer, but resistance change is small due to leakage current flow throughout the unrepaired defects site.

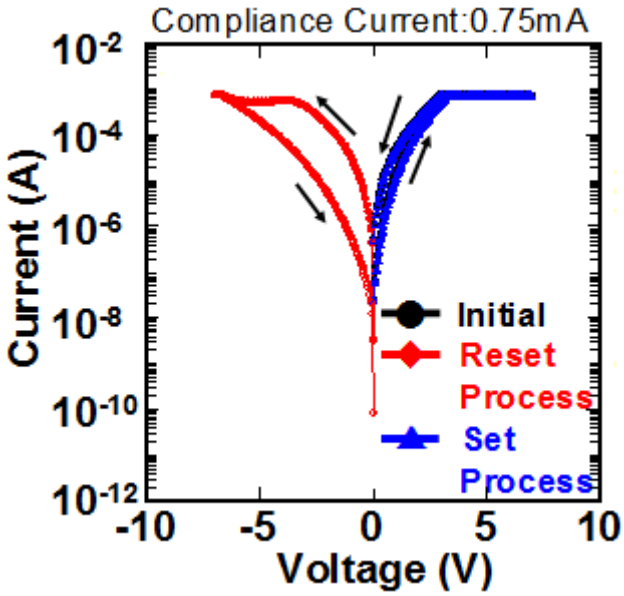

Figure 3.4Bipolar resistance switching characteristics of W/CeO_x/Ti ReRAM

3.4 Switching Behavior of ReRAM with Ni BE

The resistive switching characteristic for devices with Ni BE is shown in figure 3.5. Resistance switching characteristics with Ni bottom electrode showed a switching behavior with a symmetric shape and the current followed the initial characteristics, achieving a forming-free resistive switching behavior. The switching behavior was in good agreement with the proposed model in this study, as mentioned in Chapter 2. However, the on/off ratio is small, possibly due to the insulating property of the interfacial layer formed between the CeO_x layer and the Ni BE is low. High set and reset voltages of ~10V and ~ -10V, respectively, were detected, possibly due to small dielectric constant different between CeO_x and interface layers.

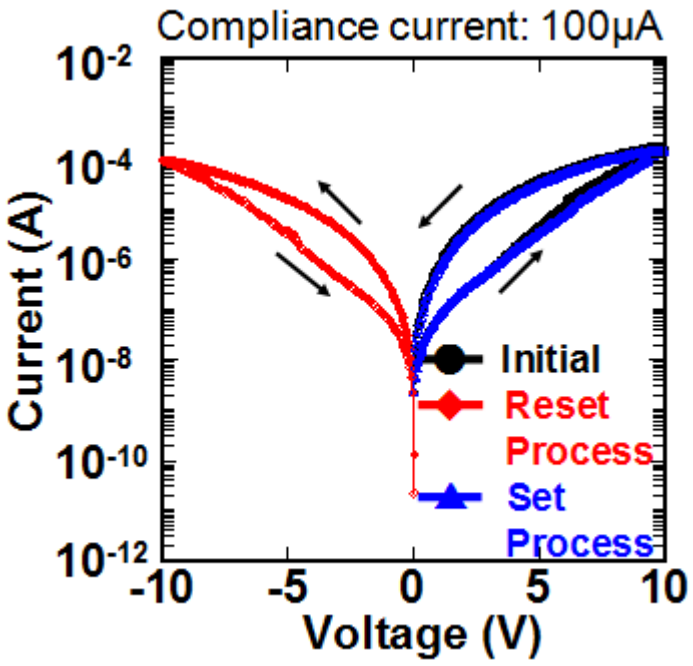

Figure 3.5 Bipolar resistance switching characteristics of W/CeO_x/Ni ReRAM

The results for the above three samples give a strong evidence that the proposed ReRAM device is works based on resistance change in the interface layer between CeO_x layer and BE. Figure 3.6 shows a model to explain the switching behavior of ReRAM with W, Ti and Ni BEs. Among all three BEs, Ni exhibit most suitable property as the interfacial layer. Low quality interfacial layer exhibits in both ReRAM with W and Ti BE leads to catastrophic dielectric breakdown in the interfacial layer after set voltage applied to ReRAM [3.8].

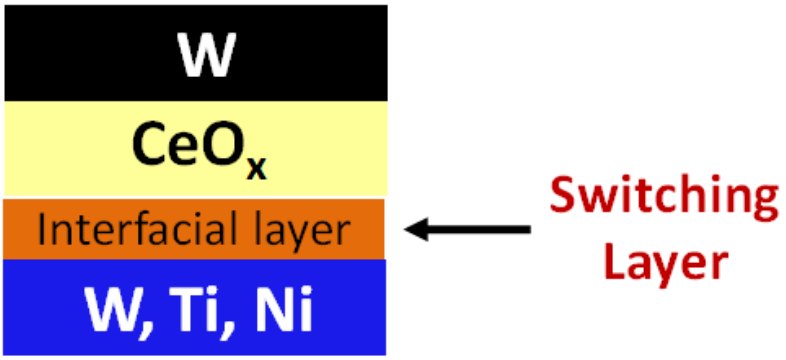

Figure 3.6 Illustration of switching layer for W/CeO_x/W, Ti, and Ni structure ReRAM[3.5-3.7]

3.5 Switching Behavior of ReRAM with TiN BE

To elucidate the proposed model, the resistive switching characteristics with TiN bottom electrode was also investigated.The CeO_x layer thickness was set to 13-nm, the same condition with ReRAM which using W, Ti and Ni as a BE.

The I-V characteristics of devices with TiN BE are shown in Figure 3.7. Only positive initial voltage sweep showed a resistive switching behavior. Also, a slight decrease in current only by one half was observed with a 2nd negative voltage sweep. The 3rd voltage application to positive direction did not follow the 1st sweep; higher current by two orders of magnitudes than the 1st sweep. Here, only a resistance ratio of 67 was obtained. A TEM image of the sample, shown in Figure 3.8 revealed a 1-nm-thick amorphous TiO_2 layer between TiN and CeOx layers. Due to the high

dielectric constant of TiO_2 more than 40, the electric field in TiO_2 layer is smaller than in CeO_x, and the breakdown spot exists in the CeOx layer not in the TiO_2 layer. Figure 3.9 shows an illustration of switching layer in the W/CeO_x/TiN structure ReRAM. Giving the fact that ReRAM device using this structure needs to apply forming voltage to initiate the switching process, while it exhibited small on/off ratio after a subsequent cycle, the switching behavior can be considered to follow the conductive filament model.

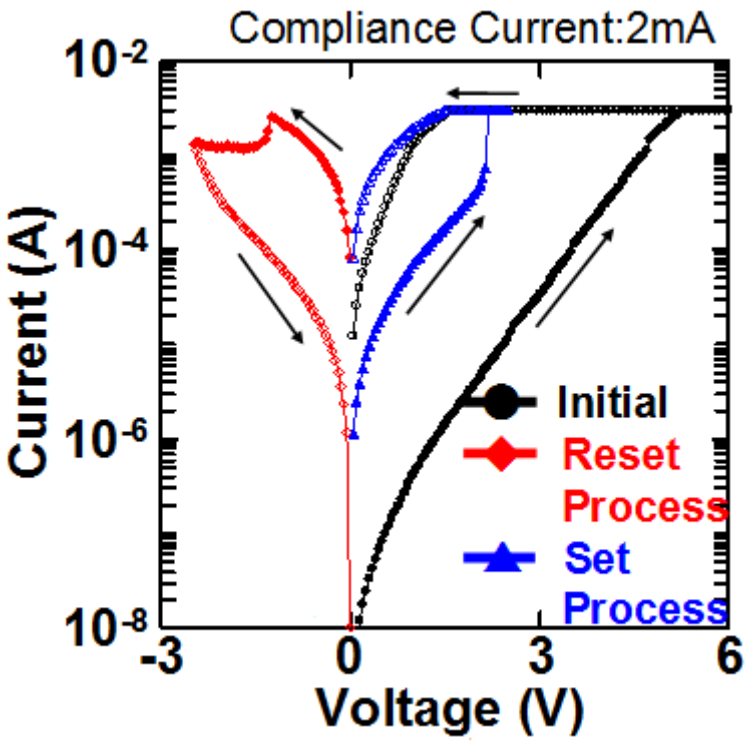

Figure 3.7 Bipolar resistance switching characteristics of W/CeO_x/TiN structure ReRAM

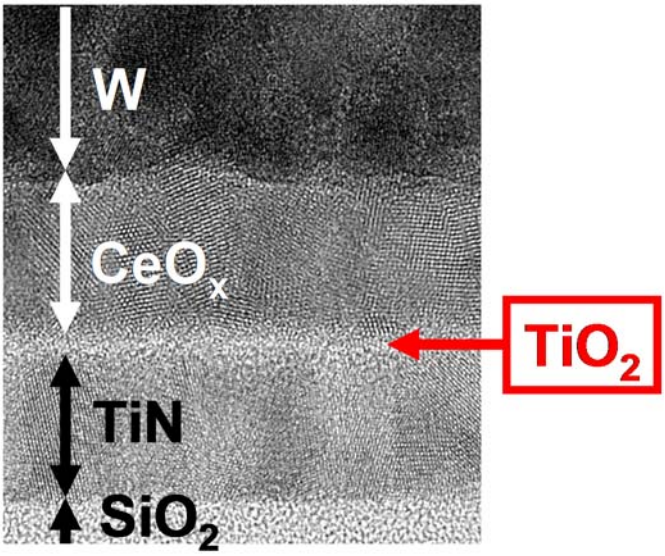

Figure 3.8 TEM image of W/CeO_x/TiN structure ReRAM

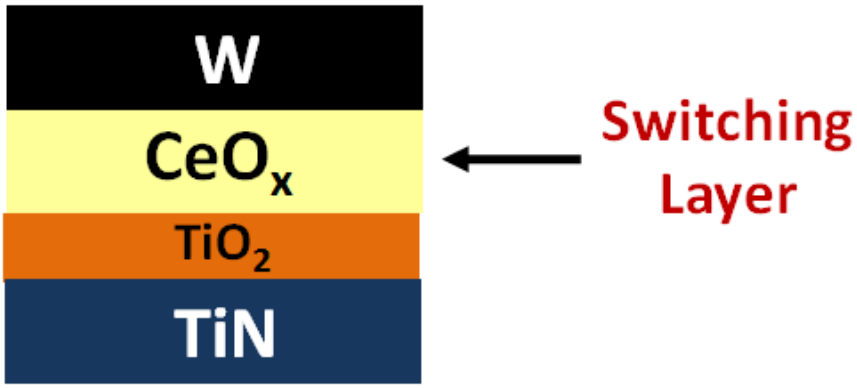

Figure 3.9 Illustration of switching layer for W/CeO_x/TiN structure ReRAM

3.6 Summary of this Chapter

The influence of the conventional metal BE selection on the resistive switching behavior of CeO_x films is investigated. Using the W, Ti, or Ni as BE exhibits forming free behavior, eventhough it has small on/off ratio. Change of resistance state depends

on resistance change of thin interfacial layer. While the device using TiN as BE material did not exhibit a forming free behavior, but it has relatively higher on/off ratio of ~67. Change of resistance state depended on resistance change of the CeO_x buffer layer. The bottom Electrode selection thus plays an important role in improving the entire switching characteristic of ReRAM device. The results give a strong suggestion that using a bottom electrode contains silicon, can form thin SiO_2 as the low-k interface layer. This will abruptly increase the on/off ratio of the device, and remaining forming free.

3.7 References

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Chapter 4:

Bipolar Resistive Switching Characteristics of CeO_x Layer on Si-based Bottom Electrodes

4.1. Introduction

In this chapter a structure to achieve a high HRS/LRS ratio by using a CeO_x layer on Si-based bottom electrodes (BEs) is proposed. This bottom electrode is chosen in order to generate the formation of SiO_2 as an interfacial layer (SiO_2-IL) between the CeO_x layer and the BE. The unique feature of SiO_2 is that it has both the widest band gap and the lowest dielectric value among the oxide material candidates [4.1]. As the resistance in HRS is strongly dependent on the insulating property of low-k layer and a large difference in dielectric constant of high-k and low-k layers can reduce the set voltage, the use of SiO_2 as a low-k layer will produce high on/off resistance ratio of the memory device.

4.2 Device Fabrication Process

The basic device fabrication flow, used to to process ReRAM devices with CeO_x buffer layer, is illustrated in Figure 4.1. A 200-nm SiO_2 was formed on p^+ -Si substrate with animpurity concentration of $10^{18}cm^{-3}$ by thermal oxidation. The SiO_2 layer was lithographically patterned by wet etching to form contacts between the bottom electrode and the substrate. Then BE layer was deposited on the SiO_2 layer by rf sputtering. A (100)-oriented p^+-Si single crystalline with doping density of 3×10^{18} cm^{-3} is used as BE.

For preparing the BE, either chemical cleaning with the HF dipping process or low temperature thermal oxidation in diluted oxygen ambient was used. Then, CeO_x films with different thicknesses were deposited at 10^{-6} Pa with a substrate temperature at 300^{o}C. A 50-nm-thick W layer was sputter deposited on the CeO_x layers and patterned by reactive ion etching with SF_6 chemistry to form top electrodes (TE). X-ray photoelectron measurements revealed that the deposited CeO_x layer contains 47%-Ce_2O_3 and 19%-CeO_2 with 34% of Ce-silicate at the bottom of the layer in molar concentration [4.2].

One of the prominent features of the CeO_x layer with multivalent properties is that the layer induces oxidation to form a thin SiO_2 for both BEs, owing to high oxygen ion conductivity [4.2]. Figure 4.2 shows a cross-sectional transmission electron microscope (TEM) image of the fabricated devices with p^+-Si BE. Thin layers with bright contrast, adjacent to the Bes, are clearly seen with thicknesses about 1 nm. An area of $20\times20\mu m^2$ for TE was used to measure the resistive switching behaviors. For I-V curve characterization, a ramp voltage 0.05V/step ranging from -10V to + 10V was applied, using sweeping time of 640μs. I-V curve measurement setup is shown in Figure 4.3.

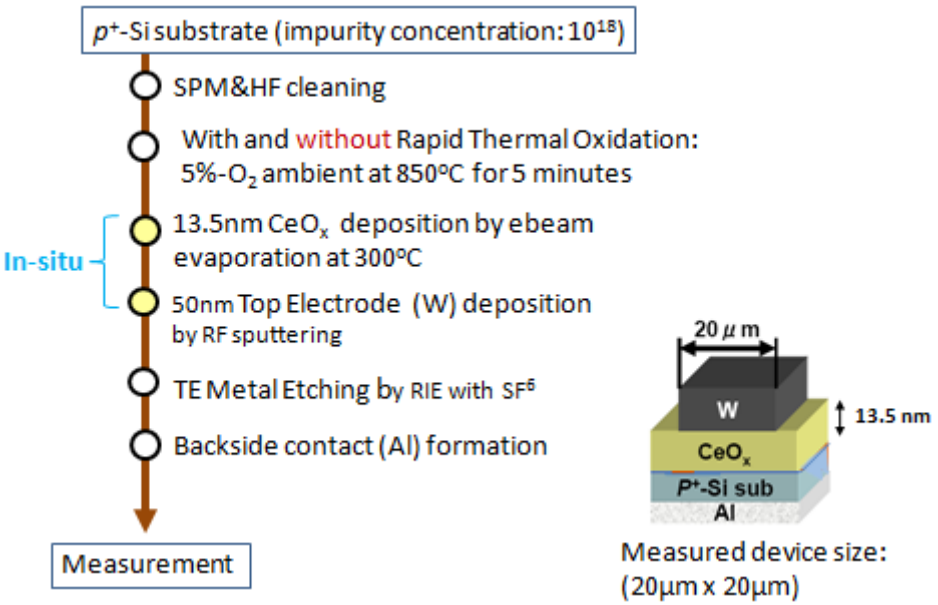

Figure 4.1 Fabrication process of ReRAM with p^+-SiBE

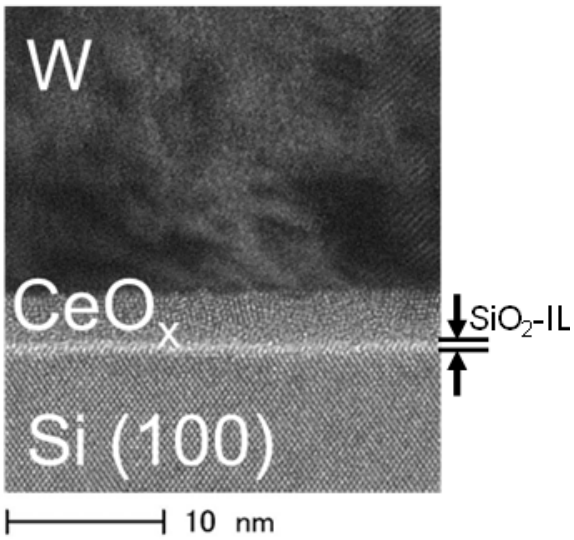

Figure 4.2 TEM images of fabricated devices for 4-nm-thick CeO_x layer

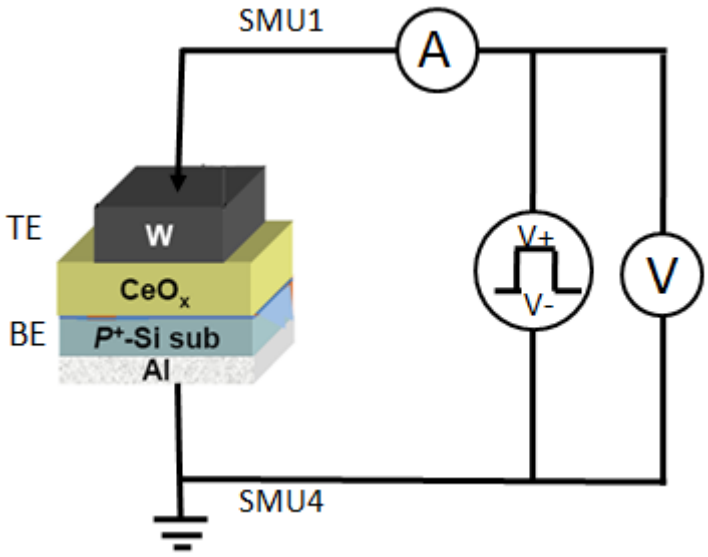

Figure 4.3 Measurement setup for I-V curve characterization

4.3 Resistive switching behavior of device with p^+-Si BE

Figure 4.4 shows the current-voltage (*I-V*) characteristics of the W/CeO_x(13nm)/SiO_2-IL/p^+-Si device. Here, the CC was set to 1 mA, which was

adjusted to give highest switching properties in terms of HRS to LRS ratio. Firstly, voltage to the TE was swept to positive direction and at a voltage of 8 V, the current was limited by CC. Sweeping back the voltage toward 0V revealed that the resistance of the device becomes three orders of magnitude smaller at a voltage of 0.1 V. When the second voltage sweep was conducted toward negative direction, a sudden drop in the current at a voltage of -3.5 V was observed and the resistance kept high during the voltage sweep back to 0 V. By applying the third voltage sweep toward positive direction, a sudden jump in the current, a breakdown-like behavior, was observed at a voltage of 3.7 V and reached to CC to clamp the applied voltage. Again, while sweeping back the voltage to 0 V, the current nearly followed the initial current characteristics. The obtained I-V curve is a typical bipolar type resistive switching behavior.

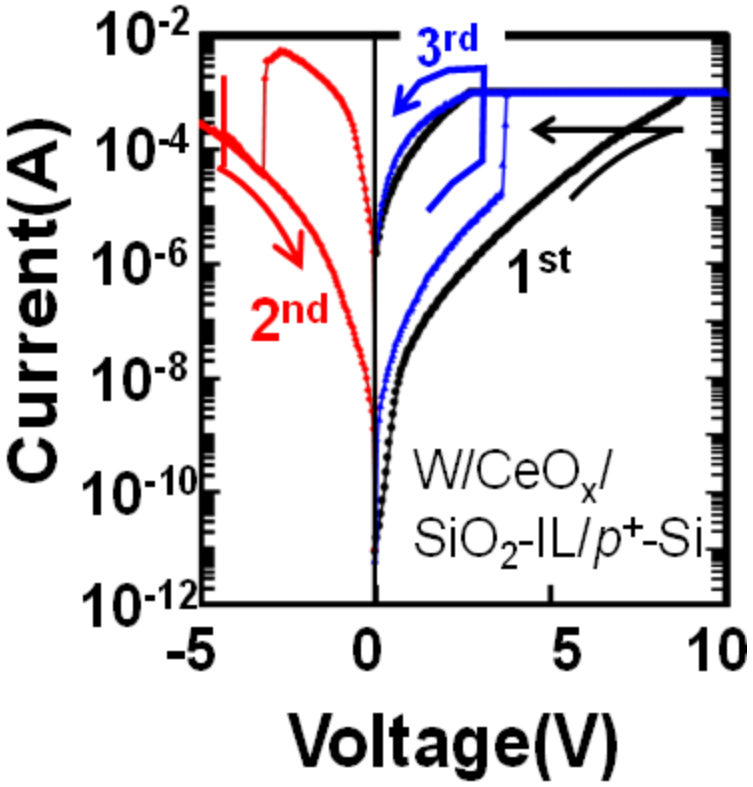

Figure 4.4 Resistive switching behavior of 13.5-nm-thick CeO_x layer on a p^+-Si BE with a thin SiO_2-IL with an initial voltage sweep to positive direction

Figure 4.5 shows the I-V curve with the initial voltage sweep to negative direction. No difference in the bipolar switching direction has been observed irrespective to the polarity of the initial voltage sweep direction, indicating that the device has polarity for resistive switching. Note that the I-V characteristics of a W/CeO_x/W MIM structure, as discussed in Chapter 3, showed little switching behavior, so that the obtained bipolar resistive switching with p^+-Si BE should originate from the interaction at the BE interface [4.3].

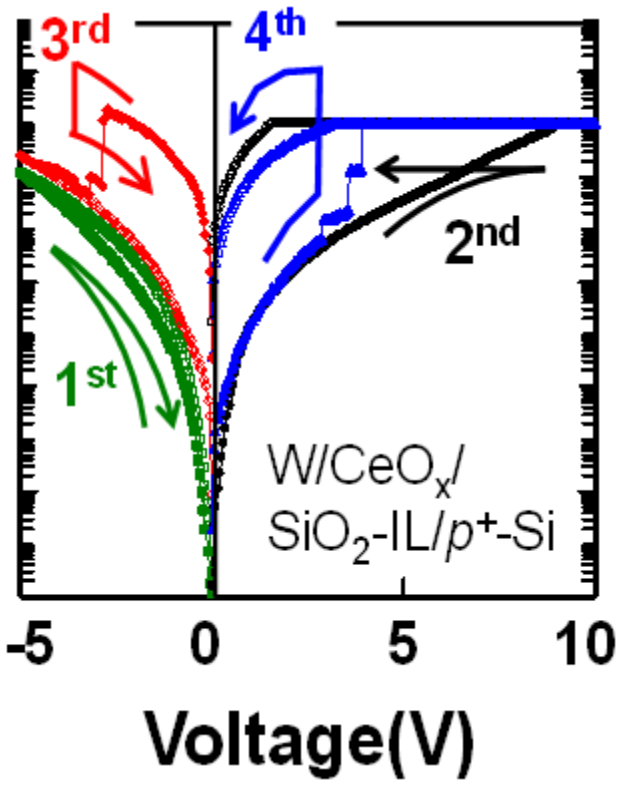

Figure 4.5 Resistive switching behavior of 13.5-nm-thick CeO_x layer on a p^+-Si BE with a thin SiO_2-IL with an initial voltage sweep to negative direction.

As the relative dielectric constant of CeO_x is 28, which is 7 times higher than that of SiO_2, the electric field in the thin SiO_2 layer becomes 7 times higher than that of CeO_x layer. Therefore, high electric field can easily induce local breakdown to the thin SiO_2 layer in the set process. As SiO_2 has good insulator properties, local breakdown in this layer dramatically reduces the resistance between TE and BE. In the reset process, the contribution of oxygen ions in the CeO_x layer can be the source to anodically reoxidize the breakdown spots (BD spots) in the thin SiO_2 layer, in the same way that

metals can be oxidized by scanning probe microscopy [4.4]. The above mechanism, shown schematically in Figure 4.6, can qualitatively explain the current jump behavior for the set and reset process.

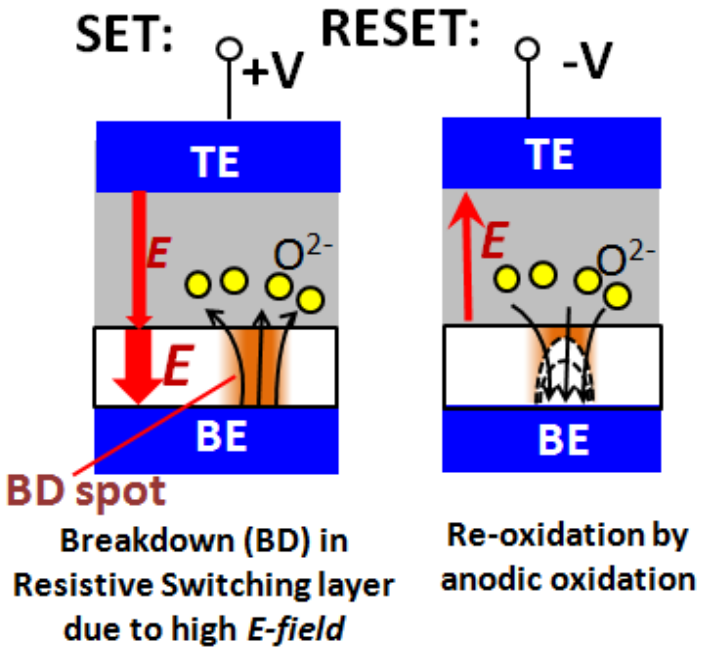

Figure 4.6 A schematic model to explain bipolar switching with a thin-SiO_2 IL

To elucidate the influence of the process to form thin SiO_2-ILs, a device with thermally grown SiO_2-IL was fabricated. The p^+-Si wafer was oxidized in 5%-O_2 ambient at 850°C for 5 minutes using rapid thermal oxidation (RTO) to form a thin SiO_2 layer with a thickness of nearly 1-nm [4.5]. Figure 4.7 shows *I-V* characteristics of the device with and without an RTO process of the initial substrate, where bipolar-type resistive switching behaviorsare observed for both devices. Smaller current was

obtained for the initial positive voltage sweep, indicating that the insulating properties of the thin-SiO_2 IL, for example, smaller number of traps or better thickness uniformity, were improved by the RTO process. It is reported that the RTO process can increase the regularity of atomic arrangement of the interface layer [4.11]. The CC of the device with RTO was optimized to 100 μA, which is smaller than the device without RTO. When the voltage is swept back to 0 V, same current characteristics were obtained for both samples, suggesting that electron conduction through the local breakdown spots were the same. Reset characteristics, a step-like drop in current, were observed in both samples with the second voltage sweep to negative direction, except that a large current drop over three orders of magnitude was obtained with the RTO-treated device around the same voltage of -2.7 V. As a result, the on/off ratio of the device, measured at -0.1 V, increased from 1.5×10^3 to 1.6×10^4 with the RTO process. The third voltage sweep to positive direction showed a jump in the current for both devices, with nearly the same voltage around 4 V.

Schematic models to explain the effect of the RTO process are shown in Figures 4.8 and 4.9. When a thinSiO_2-IL with large number of traps distributed in the film is formed between the CeO_x layer and the p^+-Si BE, relatively large leakage current can flow through leakage paths with a high density of localized states at energies

distributed over a wide range in the band gap[4.6]. While increasing the initial voltage applied to TE, new traps are generated and once it reaches to critical defect density, the layer breaks down to form breakdown spots and the forming process completes. Reset process to locally anodize the breakdown spot will take place by the drift of oxygen ions from the CeO_x layer, attracted by the electric field to the breakdown spot. Once the spot is re-oxidized, the current suddenly drops yet leaving the leakage current through initial traps as background. In the set process, the recovered part in the spot can be broken again with positive voltage application with a relatively low voltage, as a high density of defects can be considered to be located in the specific spots. For the RTO-treated device, on the other hand, owing to higher insulating properties of the thin SiO_2-IL with less number of initial traps, a higher voltage is needed to generate traps, building up the traps to configure the percolation path, and to reach the critical defect density [4.7 – 4.9].

To avoid catastrophic destruction of the film due to power dissipation to local spots, a smaller CC needs to be applied [4.6]. The reset process is considered to be performed in the same way as the trap-rich SiO_2 film case, except for low background leakage current, that is, high resistance in HRS. The proposed model suggests that the high resistance in the HRS can be achieved with small numbers of initial traps in the

SiO_2-IL in combination with smaller CC. And also the resistance at LRS is not affected by the value of CC. This fact is different from the conventional filament-model based resistive switching, where smaller CC results in higher resistance for LRS [4.10].

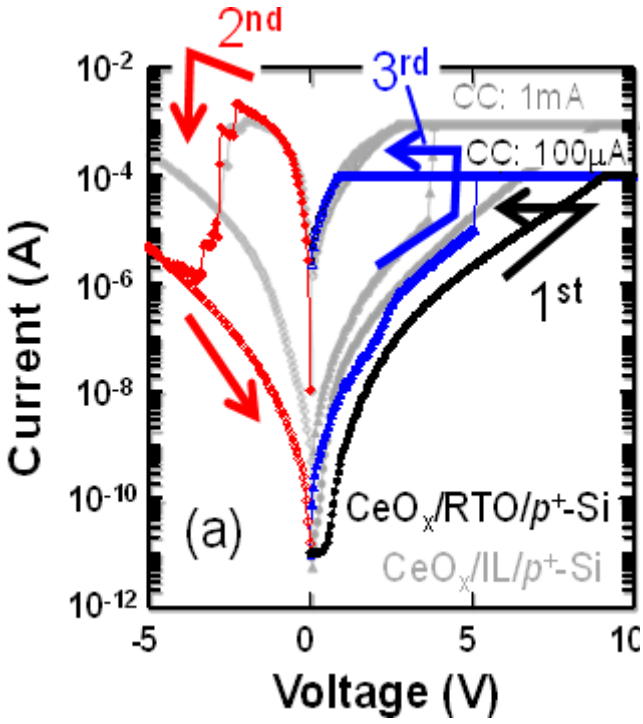

Figure 4.7 I-V characteristics of CeO_x layer on a low-temperature-oxidized p^+-Si BE. Gray lines show I-V characteristics without oxidation

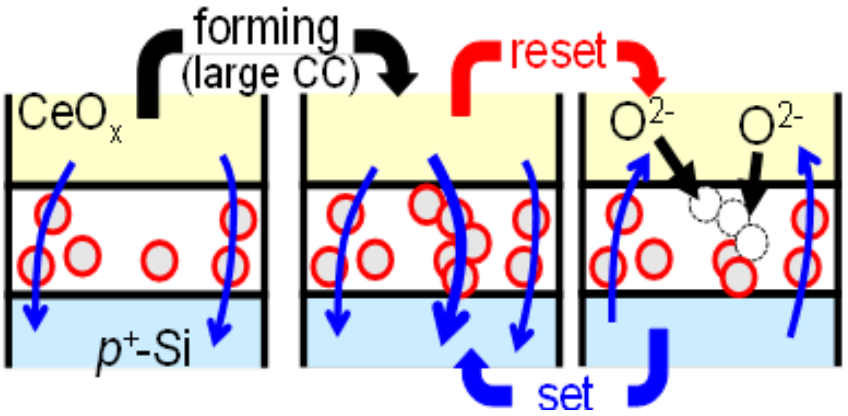

Figure 4.8 Schematic illustration of an SiO_2-IL with large numbers of initial traps

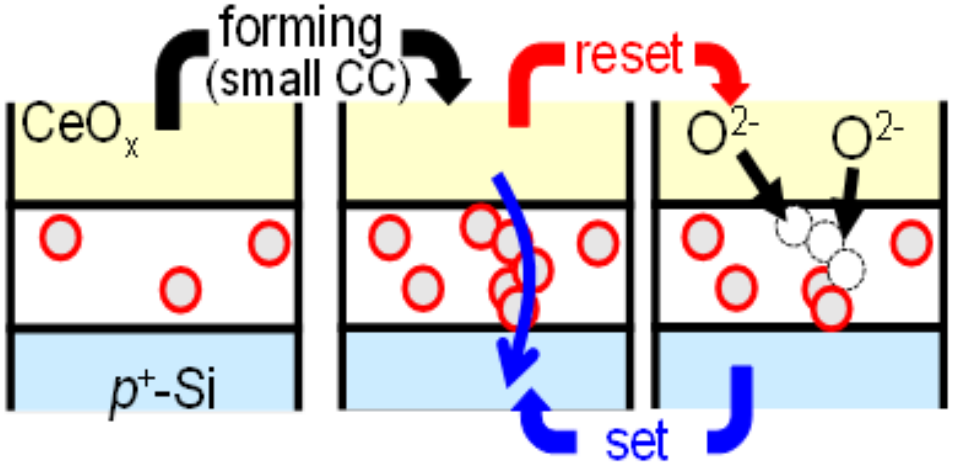

Figure 4.9 Schematic illustration of an SiO_2-IL with less initial traps

An SiO_2-IL with large number of traps relatively requires high CC to form breakdown spots for the forming process, and background leakage current limits the resistive change after the local anodic oxidation of the breakdown spots. With an SiO_2-IL with less initial traps, the breakdown spot should be carefully formed using

smaller CC. Owing to the suppressed background leakage current, higher resistance at HRS can be obtained.

4.4 Summary of This Chapter

A robust operation mechanism to increase the on/off ratio of ReRAM device was investigated. High on/off ratio > 10^3 was obtained by utilizing Si contains BE. For p^+-Si BE, the on/off ratio was modelled by the initial number of traps of the SiO_2 interfacial layer. The proposed model suggests that higher resistance in the HRS can be achieved with smaller numbers of initial traps in the SiO_2-IL in combination with smaller CC. Moreover, a new switching mechanism using breakdown and anodic re-oxidation phenomena is confirmed.

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Chapter 5

Forming-free Resistive Switching Memory Device with CeO_x Layer on $NiSi_2$ BE

5.1 Introduction

Resistive memory has attracted a great attention as a new generation of non-volatile memories, owing to low voltage and fast operation with excellent retention properties [5.1]. Based on the conductive-filament model, switching mechanism of ReRAM are determined by the annihilation and creation of the oxygen vacancies at the tip of filaments within the oxides, which is commonly created during the initial forming process [5.7]. The on/off ratio is strongly dependent on the forming process, and is sensitive to the compliance current as it determines the size of the filaments [5.3]. Forming-free devices have been presented using defect-rich AlON at the cost of on/off ratio [5.2].

Resistive memory utilizing CeO_x layer as a buffer layer and p^+-Si BE is confirmed to have high on/off ratio, as mentioned in Chapter 4. Despite its high on/off

ratio, the memory cell needs a forming voltage application to initiate the switching process. In this chapter, a proposal of forming free, high on/off ratio, and fast operation using a laminated structure of a thin SiO_2 layer with CeO_x buffer layer and silicide bottom electrode is discussed. $NiSi_2$ was selected as a bottom electrode (BE) as very thin-SiO_2layer can be easily created and out-diffusion of Ni atom is suppressed [5.4].

5.2 Device Fabrication Process

The basic device fabrication flow, used to to process ReRAM devices with CeO_x buffer layer, is illustrated in Figure 5.1. A 200-nm-thick SiO_2 layer was formed on p^+-Si substrate with an impurity concentration of 10^{18} cm^{-3} by thermal oxidation. The SiO_2 layer was lithographically patterned by wet etching to form contact between bottom electrode and substrate. Then bottom electrode layer was deposited on the SiO_2 layer by rf sputtering. To form 14.4-nm-thick $NiSi_2$ bottom electrode, six cycles of Ni/Si layer in-situ deposition consisting of Ni (0.5nm) and Si (1.9nm) each was annealed in nitrogen ambient for 1 minute at 500ºC to promote the reaction of Ni and Si atoms, see Figure 5.2. For a buffer layer, a CeO_x film was deposited by the electron-beam evaporation at 300ºC, followed by in-situ deposition of 50-nm-thick tungsten by rf sputtering as a device top electrode. The top electrode was then patterned by the reactive ion etching (RIE) with SF_6 chemistry. Patterned W top electrodes (TE) with an

area of (20×20) μm^2 were used to measure electrical properties of the device. Lastly, an Al film was deposited as a backside contact. For I-V curve characterization, a ramp voltage 0.05V/step ranging from -10V to + 10V was applied, using sweeping time of 640μs. I-V curve measurement setup is shown in Figure 5.3. The CC was set ranging from 100μA to 2mA, which was carefully adjusted to give the highest switching properties in terms of on/off ratio. As the switching layer is thin low-k layer, too large CC set must be avoided in order to avoid device damage due to catastrophic breakdown.

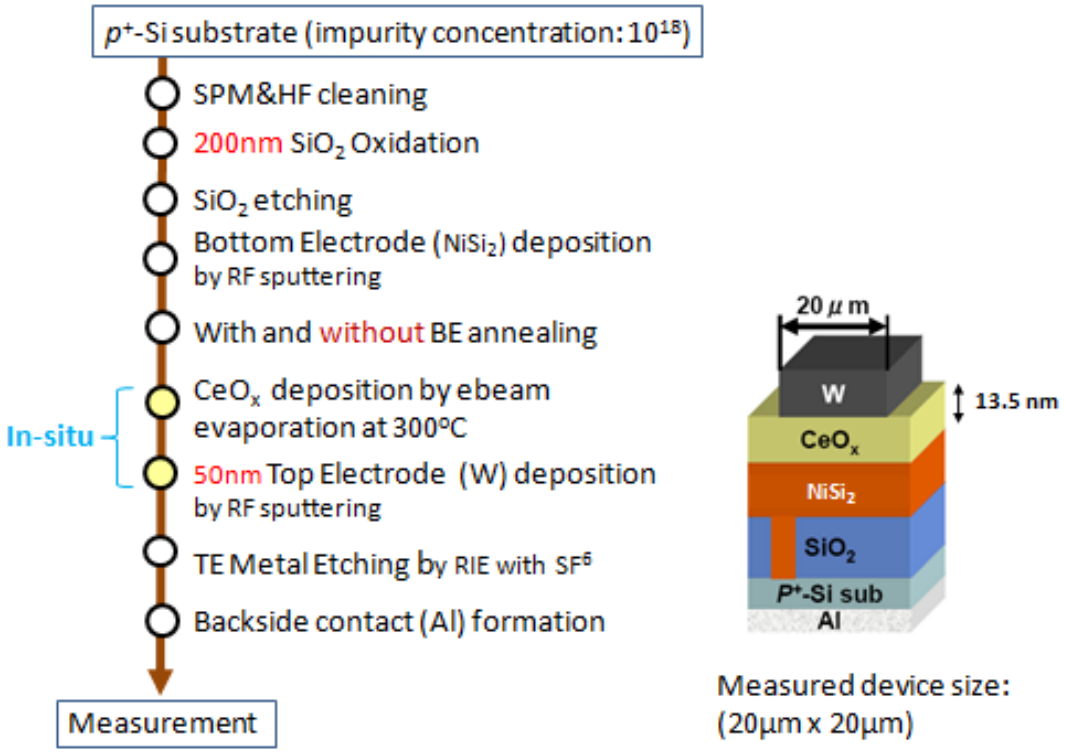

Figure 5.1 Fabrication process of W/CeO_x/SiO_2/$NiSi_2$ structure ReRAM

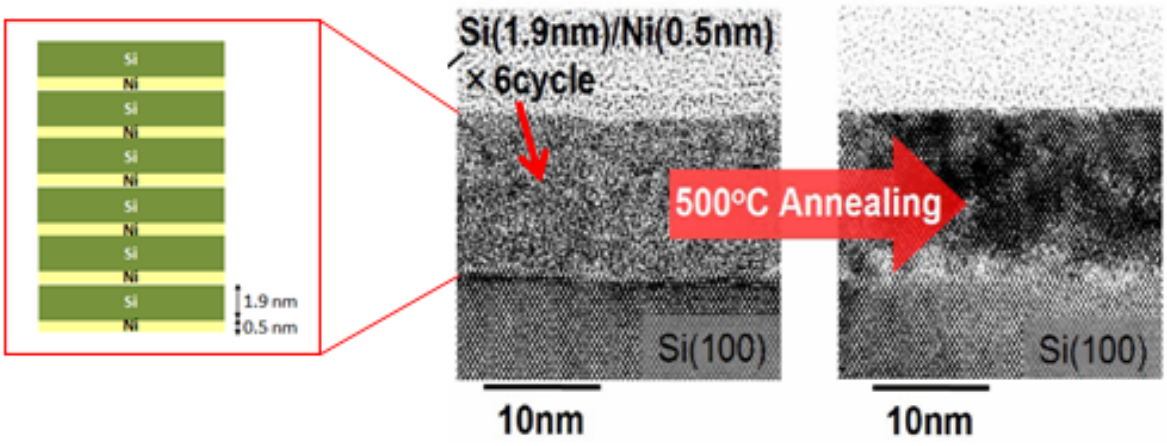

Figure 5.2 $NiSi_2$ bottom electrode formation by annealing process

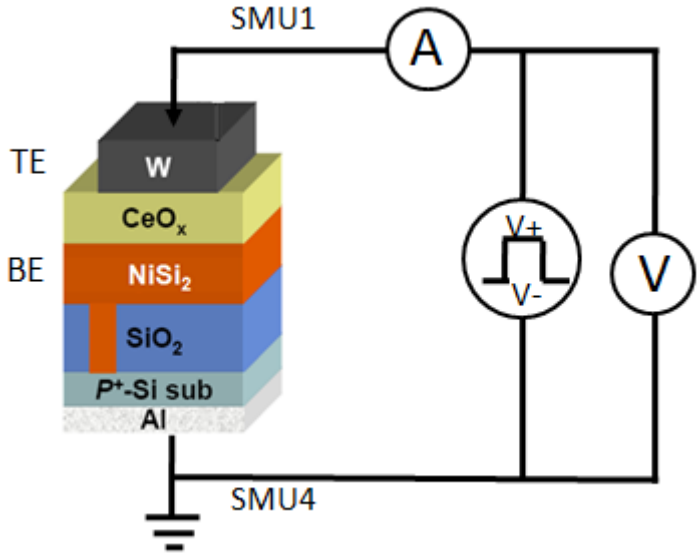

Figure 5.3 Measurement setup for I-V curve characterization

5.3 Resistive Switching Behavior

Figure 5.4 shows the current-voltage (I-V) characteristics of devices with 13.5-nm-thick CeO_x and $NiSi_2$ BE. Initial positive voltage sweep application to TE, indicated as 1st in the figure, showed a small breakdown behavior at 7.5 V and then the

current was limited by compliance current, set to 2 mA, until the voltage is swept back to 3.5 V. This strongly suggests that the device has changed the states from HRS to LRS. Second voltage sweep to negative direction without a current compliance showed a sudden decrease in current, indicating a bipolar switching type behavior from LRS to HRS. The current of the third positive voltage application showed identical current trace to the initial current behavior. This strongly suggests that a forming-free resistive switching was achieved. The extracted resistance ratio of 6×10^5 is considerably high compared to reported resistive switching devices.

The I-V characteristics of the device with initial voltage application swept to negative direction is shown in Figure 5.4(b). No jump in current was observed for the initial sweep. The 2nd sweep to positive direction showed a small jump in current at 6 V and after that the current was limited to compliance. The 3rd sweep to negative direction showed a drastic decrease in current at -3.5 V, and followed the current kept as small as the initial sweep. The 4th sweep to positive direction followed the same current track as the 2nd sweep, only with a slight difference in breakdown behavior to reach the current compliance. Therefore, it can be concluded that the device has a polarity; set process can only be obtained by positive bias and reset process by negative bias.

Transmission electron microscope (TEM) image of the device is shown in Figure 5.4(c), where a clear SiO_2 layer with a thickness of 1.5 nm can be observed between the CeO_x and $NiSi_2$ layers, reactively formed due to the catalytic effect of CeO_x [5.5]. As the dielectric constant of CeO_x is 28, 7 times higher than that of SiO_2, the electric field in the thin SiO_2 layer is 7 times higher than that of CeO_x layer. Therefore, high electric field can easily induce local breakdown to the thin SiO_2 layer. As SiO_2 has good insulator properties, local breakdown in this layer dramatically reduces the resistance between TE and BE. For reset process, the contribution of oxygen ions in the CeO_x layer can be the source to anodically re-oxidize the breakdown spot in the thin SiO_2 layer, in the same way that metals can be oxidized by scanning probe microscopy.

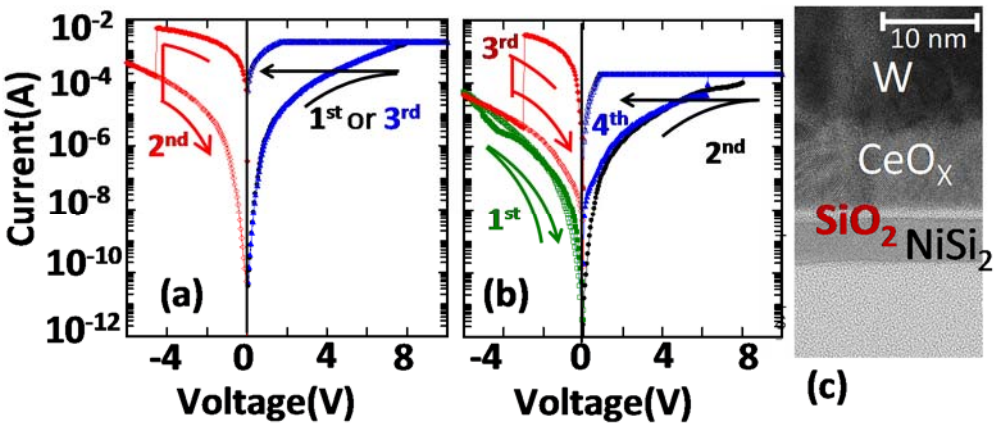

Figure 5.4 I-V curves of the device with $NiSi_2$ bottom electrode

The I-V characteristics of devices with TiN BE are shown in Fig.5.5 (a). Only a positive initial voltage sweep showed resistive switching behavior. Also, a slight decrease in current only by one half was observed with a 2nd negative voltage sweep, in contrast to the case for $NiSi_2$ and p^+-Si BEs. The 3rd voltage application to positive direction did not follow the 1st sweep; higher current by two orders of magnitudes. Here, only a resistance ratio of 67 was obtained. A TEM image of the sample, shown in Figure 5.5 (b), revealed a 1-nm-thick amorphous TiO_x layer between TiN and CeOx layers. Due to the high dielectric constant of TiO_x more than 40, the electric field in the layer, which is smaller than CeOx, cannot induce local breakdown. Therefore, together with forming process with a small resistance window, the switching behavior can be considered to follow the conductive filament model.

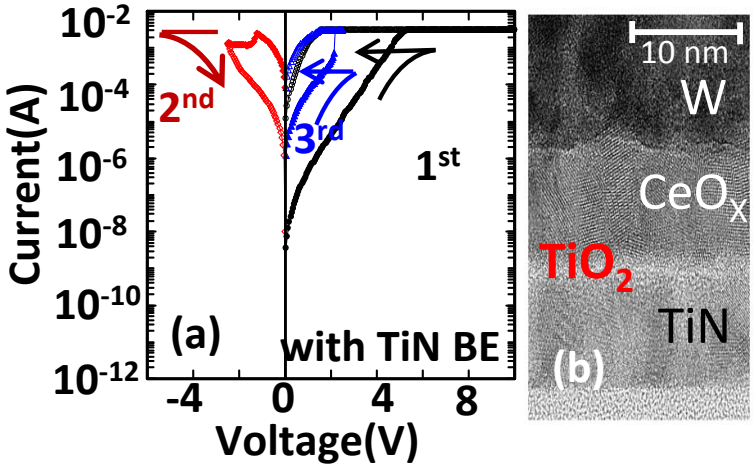

Figure 5.5 I-V curves of the device with TiN Bottom Electrode

5.4 Resistive Switching Mechanism

A model to explain the obtained switching behavior of W/CeO_x/SiO_2/$NiSi_2$ structure is shown in Figure 5.6. Owing to the buffer CeO_x layer, high electric field induces breakdown to the thin SiO_2 layer during the set process (+V). The layer also prompts the anodic re-oxidation by oxygen ion diffusion to the breakdown spot from CeO_x layer with a reverse voltage application (-V). The resistance of HRS is determined by the excellent insulating properties of SiO_2. For set-process, high electric field induces a breakdown to the thin SiO_2, due to the low dielectric constant (k~4), to change the state to LRS. For reset-process, oxygen ions from CeO_x layer induce local anodic oxidation of the breakdown spot to create SiO_2 and change the state to HRS.

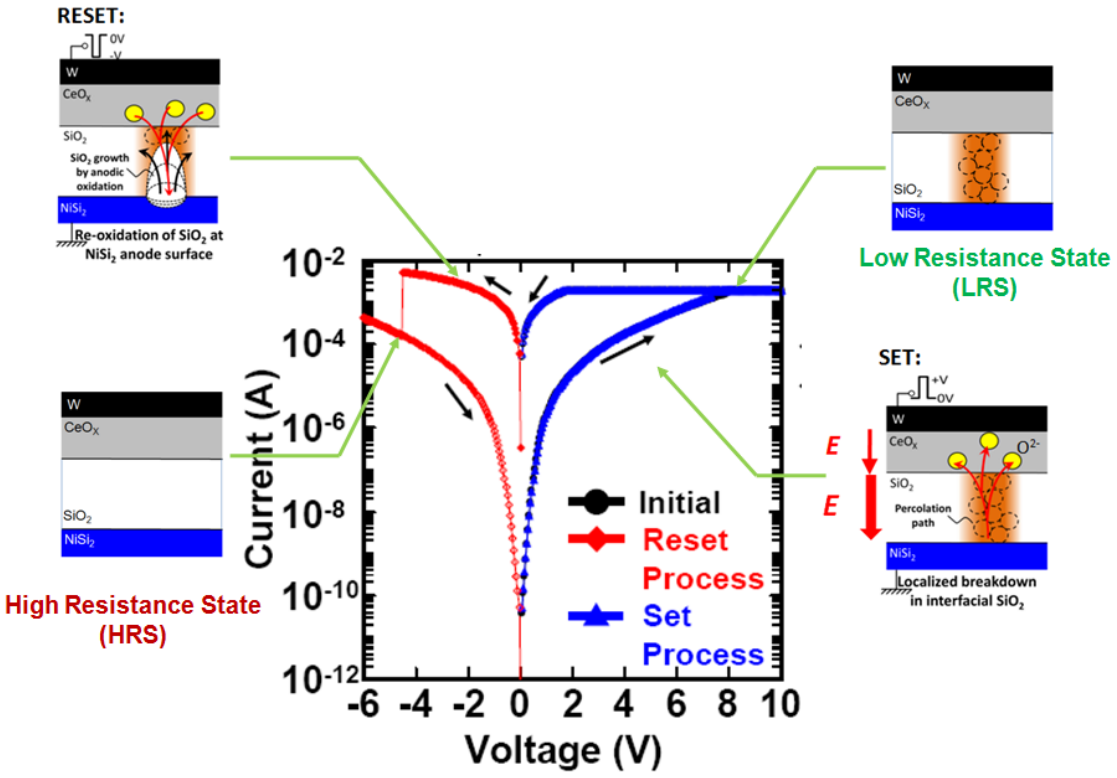

Figure 5.6 Resistive switching mechanism in W/CeO_x/SiO_2/$NiSi_2$ ReRAM

The forming free behavior remaining high on/off resistance ratio of ReRAM with $NiSi_2$ BE is possibly due to there is a Ni^+ contaminant in the CeO_x layer, as illustrated in Figure 5.7, that will simultaneously decrease the resistance in LRS on the other hand increase the oxygen ionic conductivity of CeO_x. Oxygen ion conducts fast in the lattice and conducts slow in grain boundary is reported [5.9]. This suggests that lowering grain boundary in an oxide material by adding trivalent dopants, higher oxygen ionic conductivity can be achieved [5.10-5.11]. Increase of the CeO_x buffer

layer oxygen ionic conductivity makes anodic re-oxidation process is able to perfectly recover the breakdown spot in the thin SiO_2 layer.

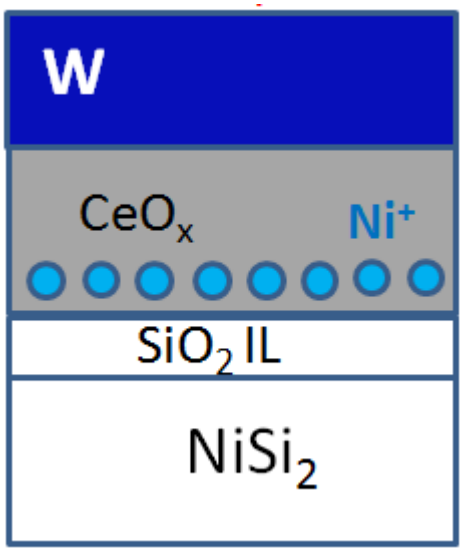

Figure 5.7. Fresh sample illustration for W/CeO_x/SiO_2/$NiSi_2$ structure ReRAM

5.5 CeOx Thickness Dependent on Set Voltage

In order to clarify the proposed model that set process is based on breakdown process, the high-k layer thickness dependence on set voltage is measured. Figure 5.9 shows the I-V characteristics of devices of $NiSi_2$ BE with different CeO_x layer thickness, where one can observe an increase in V_{set} with the thicker CeO_x layer. V_{set} dependency on t_{CeOx} can be well modeled, by a simple model of breakdown mechanism, as described in Chapter 2.

By thinning the thickness of the high-k layer, the applied voltage decrease. With constant displacement throughout the bi-layer:

$$k_{SiO2}E_{SiO2} = k_{CeOx}E_{CeOx} \quad 5.1$$

Where k_{SiO2} and k_{CeOx} is the dielectric constant of SiO_2 and CeO_x respectively. while E_{SiO2}, and E_{CeOx} is the electric field across each layer. The applied voltage can be expressed with equation:

$$V_{app} = E_{SiO2}t_{SiO2} + E_{CeOx}t_{CeOx} \quad 5.2$$

Using breakdown electric field of 16 MV/cm, the set voltage obey equation 5.3:

$$V_{set} = E_{BD}^{SiO2}\left(t_{SiO2} + \frac{k_{SiO2}}{k_{CeOx}}t_{CeOx}\right) \quad 5.3$$

The E_{BD} of SiO_2 is known to increase when the thickness is less than 10 nm and can exceed 15 MV/cm [5.8]. Here, the thickness of t_{SiO2} is fixed to 1.5 nm, obtained from TEM image shown in figure 5.4(c), so that V_{set} depends only on the thickness of t_{CeOx}.

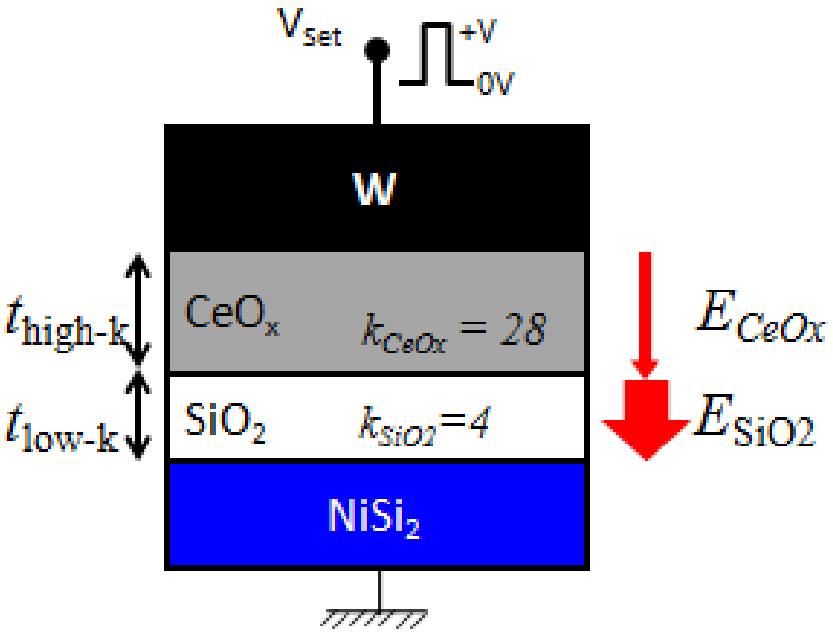

Figure 5.8 Parameter for set process in W/CeO_x/SiO_2/$NiSi_2$ ReRAM

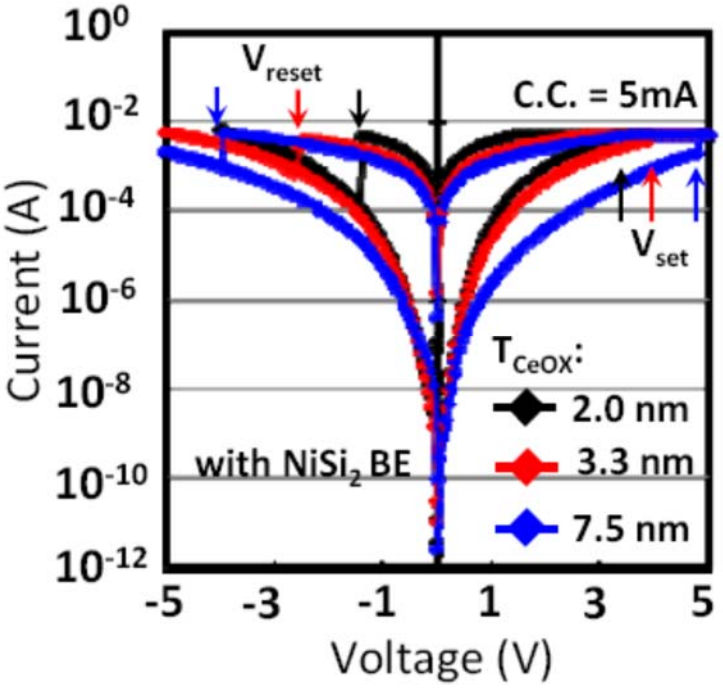

Figure 5.9 V_{set} dependent on CeO_x thickness

Using equation 5.1 – 5.3, CeO_x thickness dependency on set voltage can be plotted as shown in Figure 5.10. Assuming the breakdown field of SiO_2 layer is 16MV/cm, the experimental data can be well fitted the model. This indicates clear evidence that the set process is due the breakdown of the SiO_2 layer.

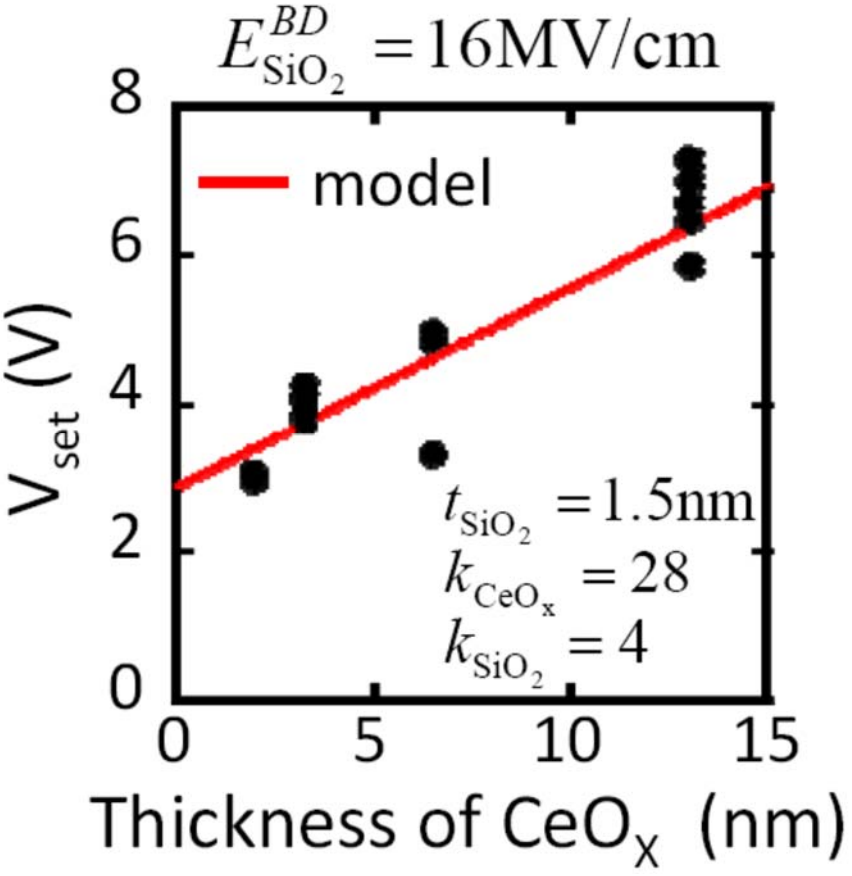

Figure 5.10 Model for set process on CeOx thickness dependence

5.6 Effect of The Thin SiO_2-IL Processes on Switching Characteristics

After sputter deposition of $NiSi_2$, annealing was conducted in 5%-O_2 ambient at either 500 or 650 ^oC for 1 minute to form a SiO_2 layer at the surface of BEs. No degradation in surface morphology was confirmed. The rest of the process, including the CeO_x deposition and the W TE formation went through identical processes. Here a device without annealing was also fabricated. Figure 5.11 shows *I-V* characteristics of the fabricated devices. The device with $NiSi_2$ BE without annealing, shown in Figure 5.11(a), showed almost the same switching behavior as those annealed at 500^oC in N_2. When annealed in oxygen ambient, as shown in Figure 5.11(b) and (c), a slight change in the current of the first voltage sweep to the third one (set process) was observed, which could be understood from the change in the physical properties of SiO_2-IL, as was discussed in the previous section. The CC that is required for exhibiting the switching behavior can be decreased by the improvement in the SiO_2 interface layer, and also smaller current can be obtained after reset process, resulting in higher on/off ratio. Figure 5.11(d) shows the relationship between CC and on/off ratio, showing that the smaller the CC is, the higher the on/off ratio becomes. Therefore, the same conclusion as the device with p^+-Si BE can be derived where an SiO_2-IL with low trap density can improve the on/off ratio.

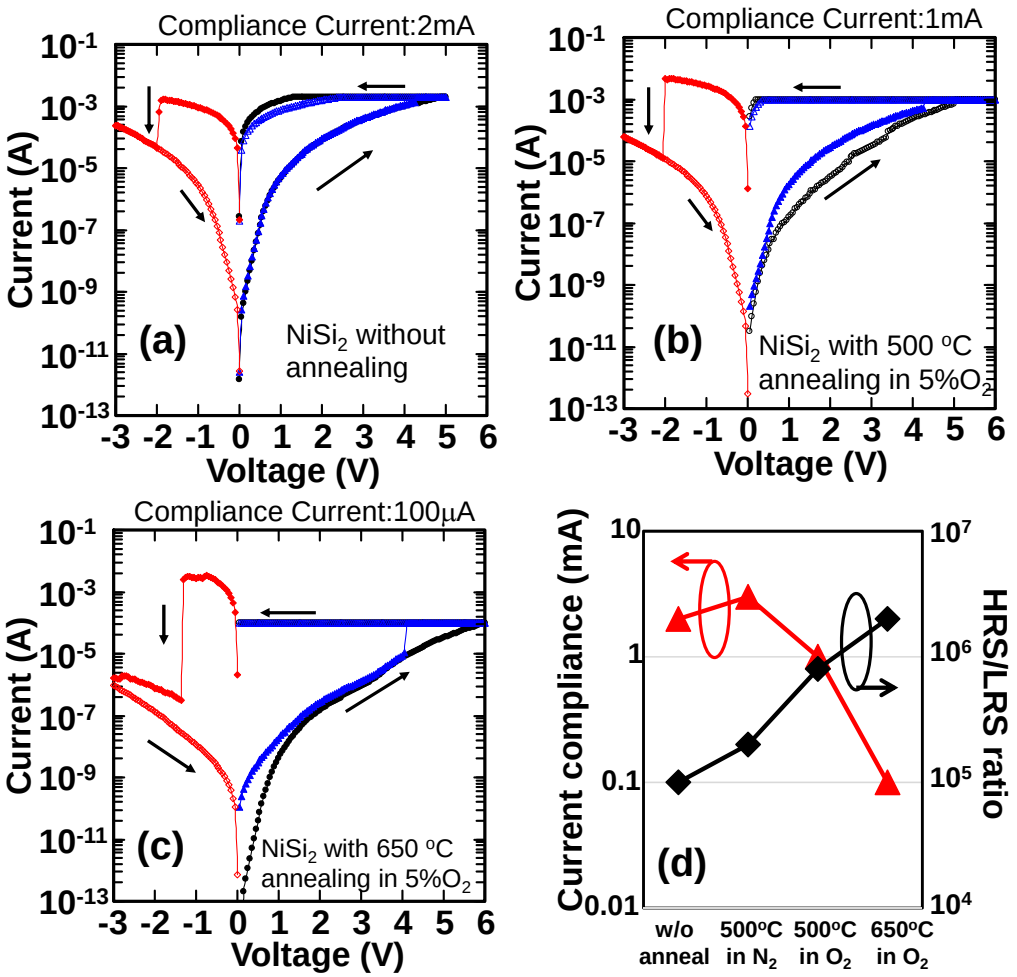

Figure 5.11 I-V characteristics of CeO_x layer on $NiSi_2$ BE. Different thermal treatments were performed for $NiSi_2$ formation; (a) without annealing, (b) 500°C in 5%-O_2, (c) 650°C in 5%-O_2. (d) Summary of CC and HRS/LRS ratio depending on annealing conditions.

5. 7 Summary of This Chapter

Resistive switching characteristics of CeO_x layer on Si-based BEs have been investigated. Owing to the presence of a thin SiO_2-IL between the CeO_x layer and BE,

the set process is considered to be triggered by a local breakdown at the thin SiO_2-IL due to large contrast in dielectric constants. Reset process, on the other hand, is obtained by a local anodic oxidation at the breakdown spots caused oxygen ion drift from the CeO_x layer. Moreover, with $NiSi_2$ BE, ReRAM device with forming-free feature was achieved. This means that BE selection is important for eliminating the forming process. Based on breakdown model, lower set voltage can be achieved by thinning the CeO_x layer.

5.8 References

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Chapter 6

Time Dependent Analysis of W/CeOx/SiO_2/$NiSi_2$ ReRAM Structure

6.1 Introduction

The switching mechanism of the proposed ReRAM structure with CeO_x buffer layer on $NiSi_2$ BE, that is discussed in Chapter 5, exhibits a different switching behavior with excellent device features such as high on/off resistance ratio without the need of he electroforming process to initiate the switching. For the set process, localized breakdown electric field in the SiO_2 layer is responsible for resistance change from HRS to LRS, while for the reset process anodic re-oxidation of $NiSi_2$ BE to recover the breakdown spot is responsible for resistance change from LRS to HRS. It was also confirmed that by thinning the CeOx layer, the set voltage can be suppressed <3V for a device with 2.5-nm-thick CeO_xbuffer layer. However, additional strong evidence to show the validity of the proposed model of this new ReRAM is necessary.

In this chapter, transient response current of both set and reset process is investigated to show the current behavior with different voltage levels that is applied

during the set and reset processes. Moreover, other device key features, that is, switching speed and endurance, are also discussed.

6.2 Transient Response Current at Set Process

Transient response current of the proposed ReRAM device with 7.5-nm-thick CeO_x buffer layer is shown in Figure 6.1. Various voltages with different amplitudes, which is lower than the device set voltage, are applied to the TE of memory device. Then current responses with time correspond to the applied voltage are plotted. It was found that lower applied voltage increases time to breakdown. When the voltage of +4.70V was applied, the currents abruptly increased due to the breakdown of the SiO_2 layer. Under the high electric field >10 MV/cm, the oxygen atoms are knocked out of the lattice [6.1], and drift toward the CeO_x buffer layer. The localized deficiency of oxygen leads to the formation of oxygen vacancies [6.2]. For higher applied voltage, defects in the bulk oxide are generated simultaneously. Figure 6.2 shows time to breakdown as a function of applied voltage. The time to breakdown decreased with increasing the applied voltage. In addition to the result in Chapter 5, the results indicate that the set process can be reasonably understood by the breakdown model.

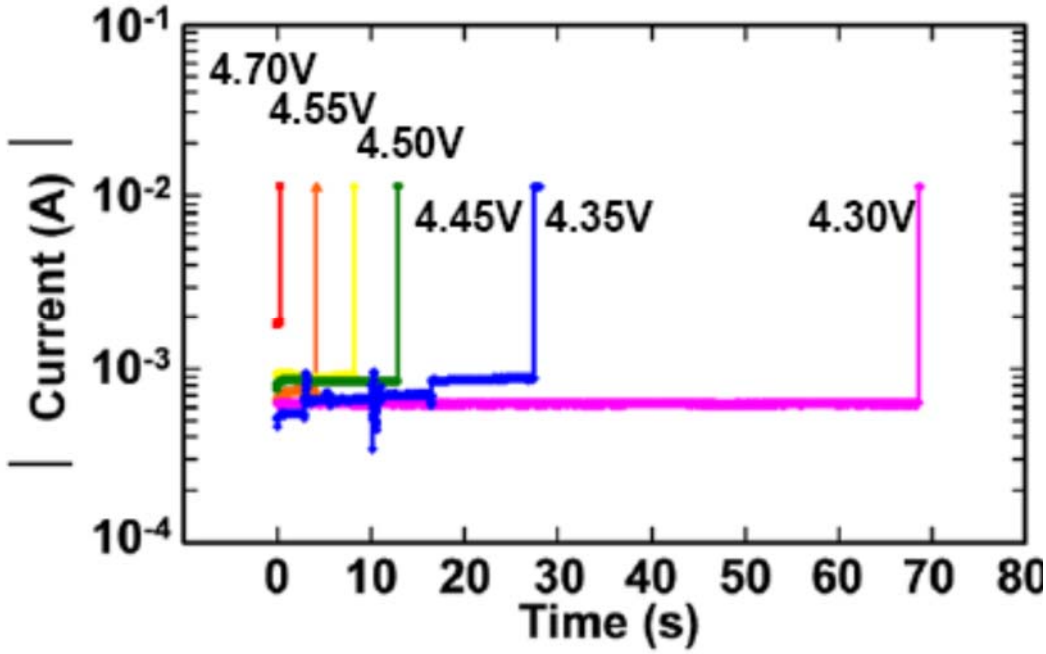

Figure 6.1 Transient response of current at set process with various voltages.

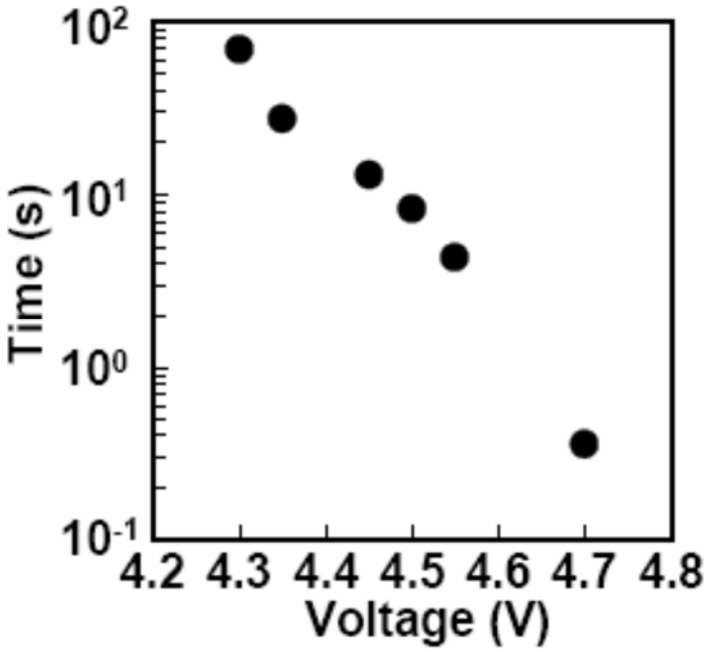

Figure 6.2 Time to breakdown dependent on applied voltage

6.3 Transient Response Current at Reset Process

Using the same sample with that in the previous section, transient response of current in the reset process was investigated to elucidate the proposed mechanisms. Figure 6.3 shows the transient response of current in the reset process with various voltages.The gradual decrease in current under constant voltage (V_{stress}) application indicates a gradual decrease in the size of the breakdown spot and once SiO_2 is grown enough the current drops to HRS.

Time to change in resistance was increased with decreasing the voltage. Applying high voltage can increase in the ionic conductivity and hence interfacial SiO_2 layer can be immediately re-oxidized, resulting in higher resistance. On the other hand, it takes long time for the reset process at a lower voltage because oxidation time becomes larger. It is worth noting that at V_{stress} of -1.8V, discrete current values were observed. Extended figure of V_{stress} set -1.8V is shown in Figure 6.4. It is considered that SiO_2 was re-oxidized each single layer at the breakdown spot by local anodic oxidation. This reflects that the current exhibited discrete values.

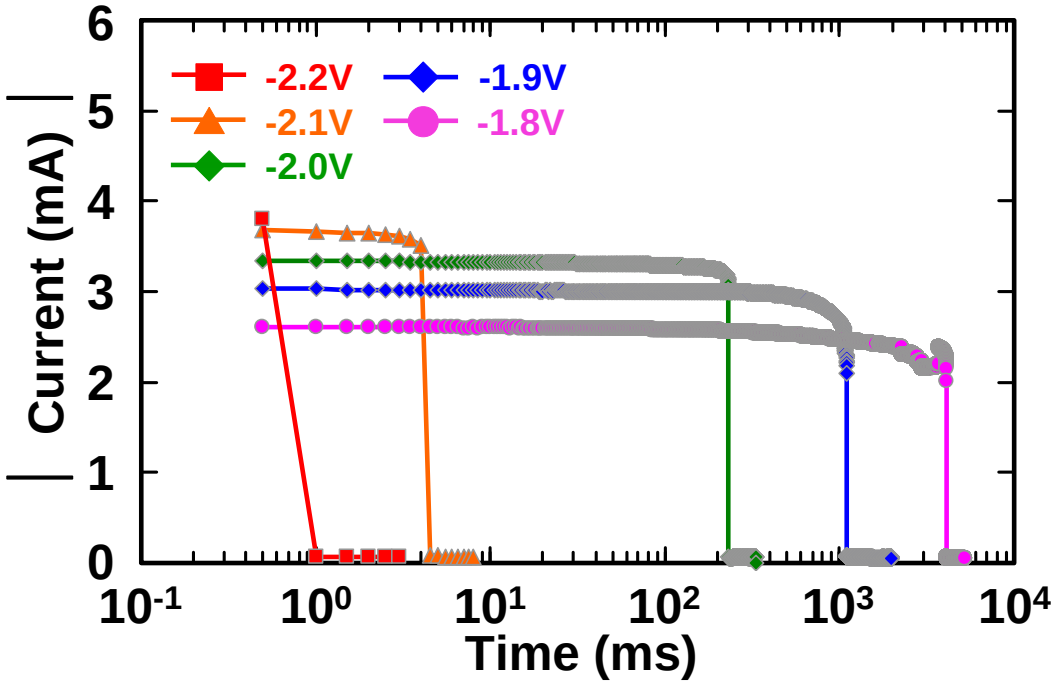

Figure 6.3 Time dependence of operation voltage in reset process

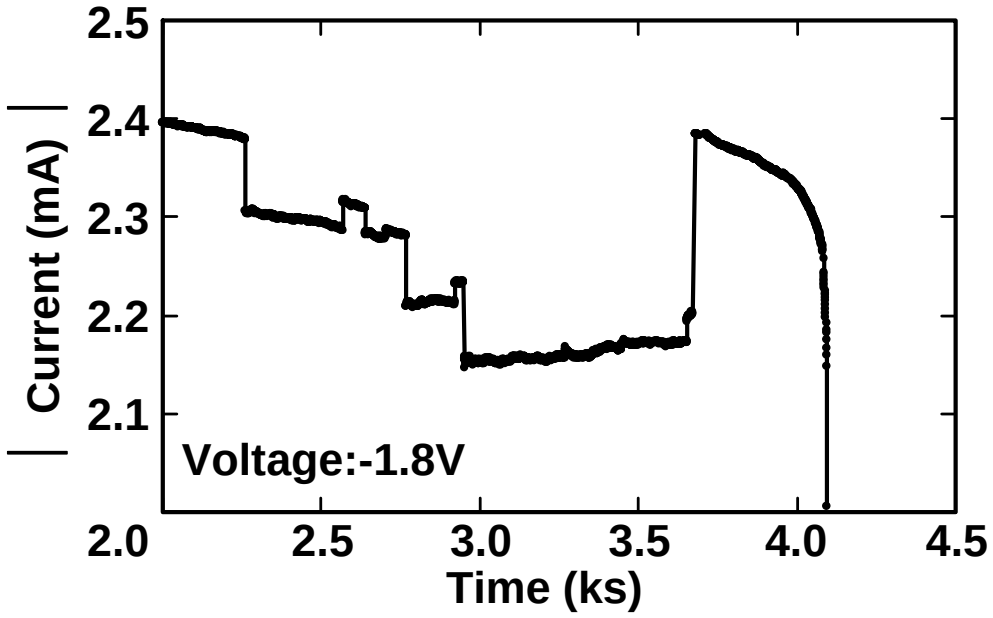

Figure 6.4 Extended figure of time dependence when reset voltage set -1.8V

Resistance steeply changes to the next resistance state when the SiO_2 single layer in breakdown spot was formed. Histogram of conductance when steady voltage was applied to the device is shown in Figure 6.5. Steady voltages were set at -1.65 ~ -1.2V. Four peaks are confirmed in the histogram. SiO_2 thickness is confirmed as 1.5 ~ 2.0-nm by TEM image. Therefore, four layers of SiO_2 exist at $CeO_x/NiSi_2$ interface. And this produces discrete values of current. Fluctuations of current exist in the local anodic re-oxidation in Figure 6.5. It is considered that fluctuations are due to the reparation and breaking of SiO_2 existing in the reset process.

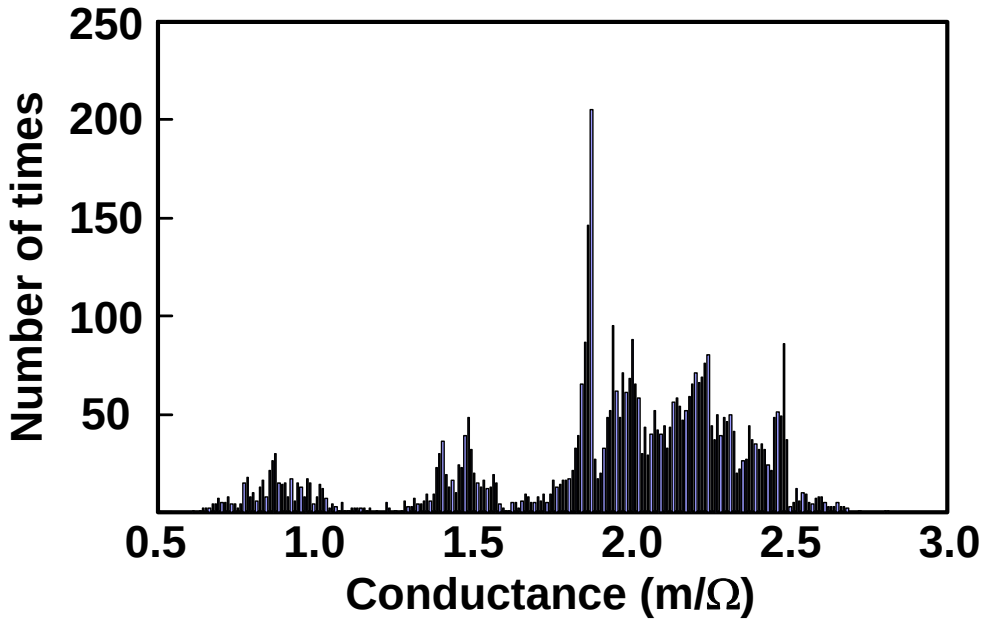

Figure 6.5 Histogram of conductance in re-oxidation process

Time of resistance back in the initial state is dependent on the balance of oxygen ion migration to oxidize Si atoms [6.3] and electron impacts to break the created Si-O bondings [6.4], which is advantageous for large read-out margin. The model of local anodic oxidation SiO_2 breakdown spot is shown in Fig. 6.6. Fluctuations of current exist in Fig. 6.5 are caused by the competition of SiO_2 formation by the anodic re-oxidation and dissociation by electron bombardment.

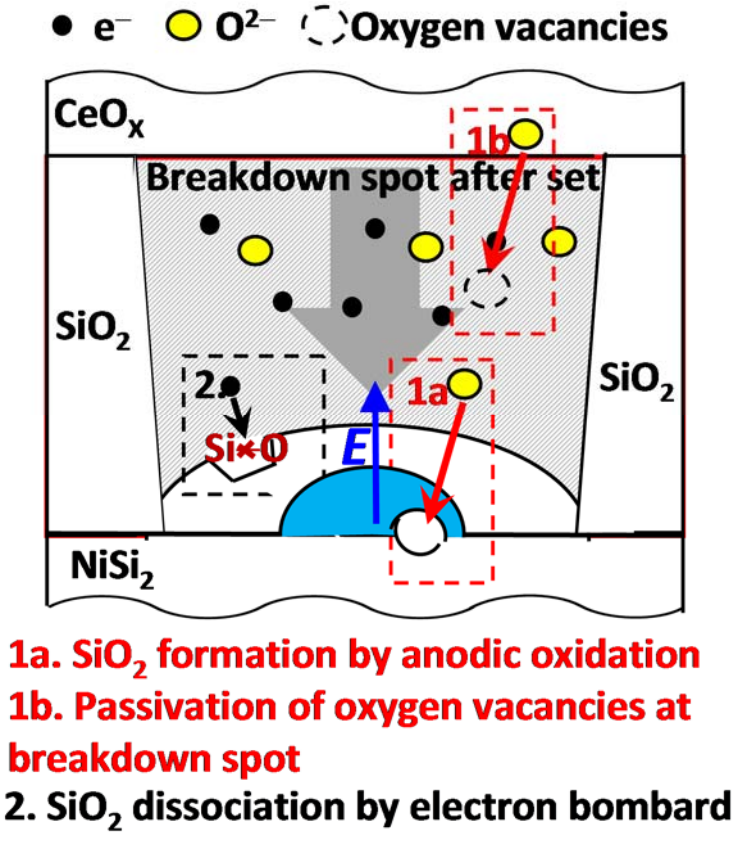

Figure 6.6 Model of local anodic oxidation SiO_2 breakdown spot

6.4 Device Operating Speed Characteristic

A memory device with 6.5-nm-thick CeO_x buffer layer on $NiSi_2$ BE was used to investigate the device operating speed. As the set and reset voltages, the applied voltage with an amplitude of +4.4V and -3.3V, respectively, were used. Resistive switching rate with different pulse width confirms no degradation in the on/off ratio of $>10^4$ at least 200nsec (limited by the measurement setup), as shown in Figure 6.7. This result indicates that the breakdown and re-oxidationcan be reliably processed in a short period and this delay time is an applicable level for the storage class memory.

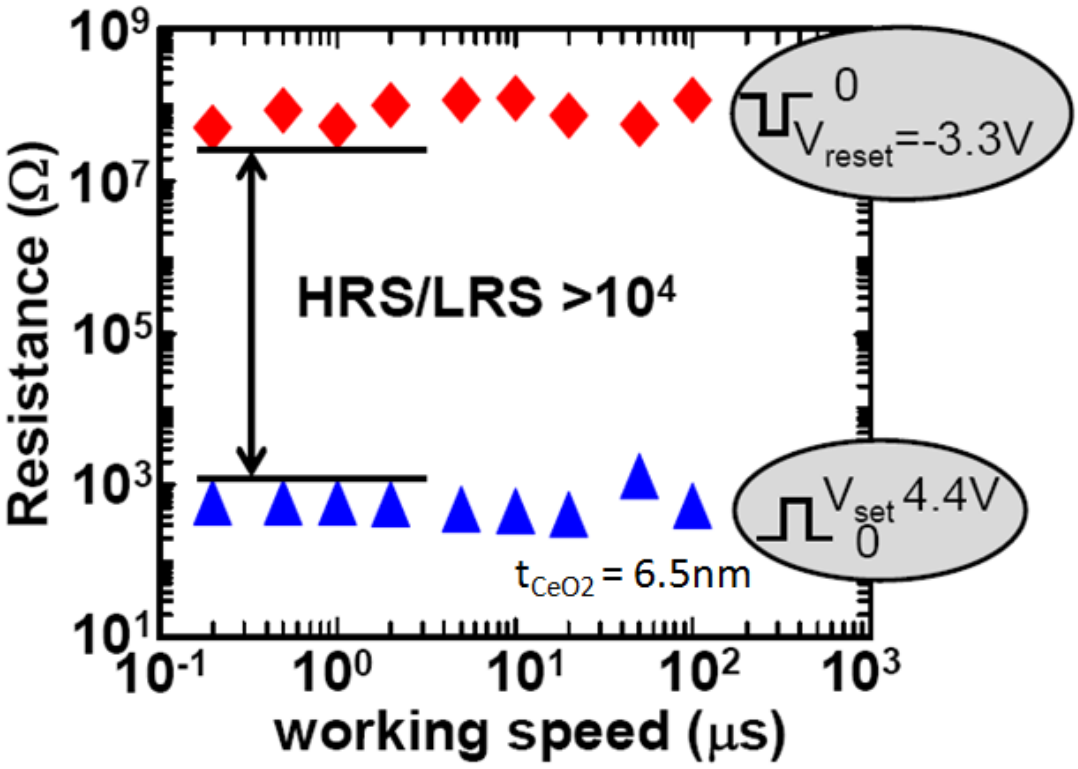

Figure 6.7 Device operating switching speed measurement

6.5 Device Endurance Characteristic

As mentioned in Chapter 2, the ReRAM device endurance properties indicate maximum number of switching cycle can be performed until the switching failure happen. By using the same sample as the operating speed measurement, device endurance was also investigated. Cyclic switching endurance showed a stable on/off ratio of ~10^3 with small spread for both HRS and LRS at least for 200 cycles (without verification voltage).

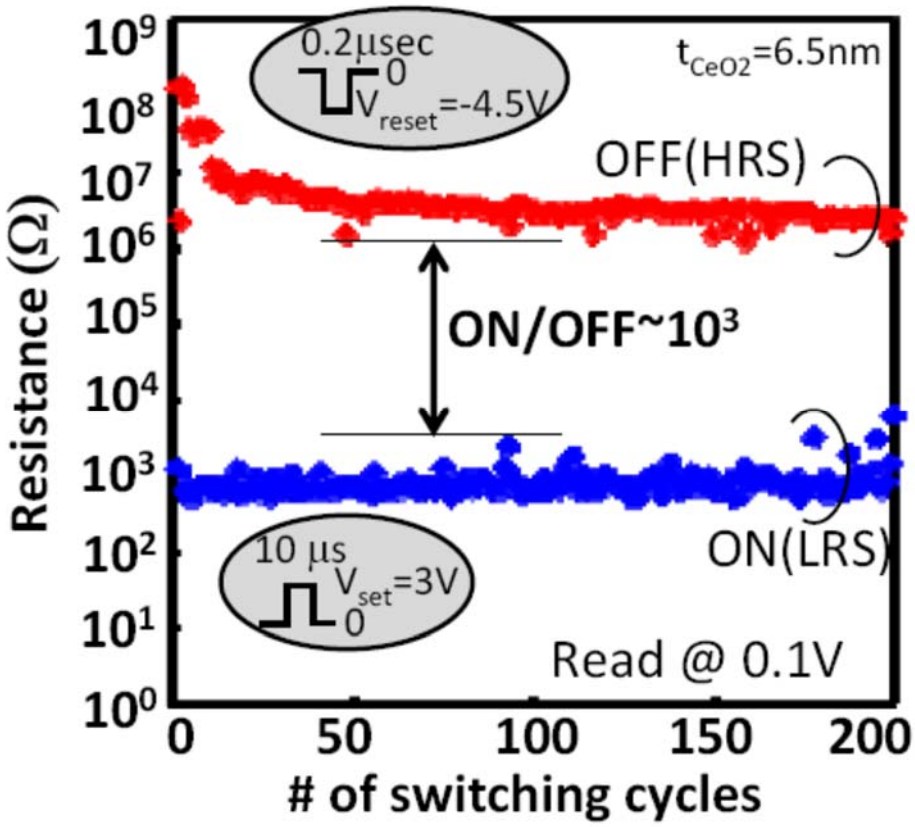

Figure 6.8 ReRAM device endurance characteristic

6.6 Summary of This Chapter

The proposed model of the set and reset switching has reconfirmed using the transient response current measurement both in the set and reset processes. The results indicate that the set and reset process can be reasonably understood by the breakdown and anodic re-oxidation model, respectively. Discrete value of current was observed in the case of low reset voltage. Fluctuations of current are caused by two simultaneous reactions, SiO_2 formation by anodic re-oxidation and dissociation by current bombardment. For the high reset voltage case, anodic re-oxidation is a dominant factor. Operating speed of <200 ns and device endurance characteristic at least stable for 200 cycles, even without verification voltage, indicates a good device property that is great potential to be used for SCM applications.

6.7 References

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Chapter 7
Conclusion

7.1 Summary of This Thesis

In this thesis, a systematic investigation is described on a new resistive switching memory by introducing a new switching concept in order to eliminate the forming process in a simple way. Unlike the conventional ReRAM model, that has a tradeoff between eliminating the forming process and small on/off resistance ratio,the proposed ReRAM exhibited forming free behavior while the on/off ratio is high ~10^6 for a device with 6.5-nm-thick CeO_x on $NiSi_2$ BE.

The bi-layer structure with high-k material as a buffer layer and thin low-k material as a switching layer is proposed in this study. The role of BE material is described as material that contributes to the formation of desired thin low-k layer. For the set process, high-k buffer layer is responsible for inducing localized breakdown in the thin low-k layer, based on its large difference in dielectric contrast between high-k layer and low-k layer. Higher the dielectric contrast lowers the set voltage. During the breakdown process in the low-k layer, oxygen ion drifts from the thin low-k layer to the buffer high-k layer and the resistance changes from HRS to LRS. In the reset process,

the buffer high-k layer is responsible as an oxygen reservoir. Oxygen ion in the buffer high-k layer drifts back to the low-k layer to trigger anodic re-oxidation, and the resistance state changes from LRS to HRS.

In chapter 3, the effect of BE material discussed. Using CeO_x as a buffer high-k layer material, the switching behavior exhibited differently depending on the BE material. The result revealed that the forming free property depends on the interfacial layer between the buffer layer and BE, and that higher on-state resistance owes to the CeO_x buffer layer property. Bottom electrode selection thus, plays an important role for the entire switching characteristic of the ReRAM device. The discussion strongly suggested that using the bottom electrode contains silicon is promising for high on/off ratio without the forming process because this structure can form thin SiO_2 as low-k interface layer. T

In Chapter 4, the structure of p^+-Si BE on CeO_x buffer layer is investigated. Rapid thermal oxidation improved the quality of the interfacial layer between the *p*+-Si BE and the CeO_x buffer layer,and high on/off exhibited with a low constant current set process. The on/off ratio of $>10^3$ was achieved due to the formation of high quality SiO_2 interfacial layer.

In Chapter 5, the structure with $NiSi_2$ BE on CeO_x buffer layer is investigated. Due to the very thin (1.5-nm-thick) SiO_2 formation and insulating property improvement by the rapid thermal annealing, the device exhibited very high on/off ratio of ~10^6 without a need of the forming process.

In Chapter 6, transient response current at the set and reset processes is discussed. The results were in good agreement with the proposed model of ReRAM operation in this study. Device switching speed of about 200 ns, and endurance characteristic longer than 200 cycles were confirmed. These results indicate that the proposed ReRAM structure and mechanism are suitable for the storage class memory application.

In Chapter 7, the results of this study are summarized and discussed on the items of the future research in order to further improve the device properties. For the embedded memory applications, thinner buffer high-k layer is more suitable while for the storage applications, thicker buffer high-k layer will be desirable.

7.2 Future Research Recommendation

The device performance of this study is compared to other reported results as shown in Fig. 7.1. The on/off ratio of this study is the best among the all reported

ReRAM data with forming free behavior. While the programming voltage of 5V, in this study, indicates that it will be suitable for the battery driven application. However, further improvement can be performed in order to optimize the device performance for wide variety applications of SCM.

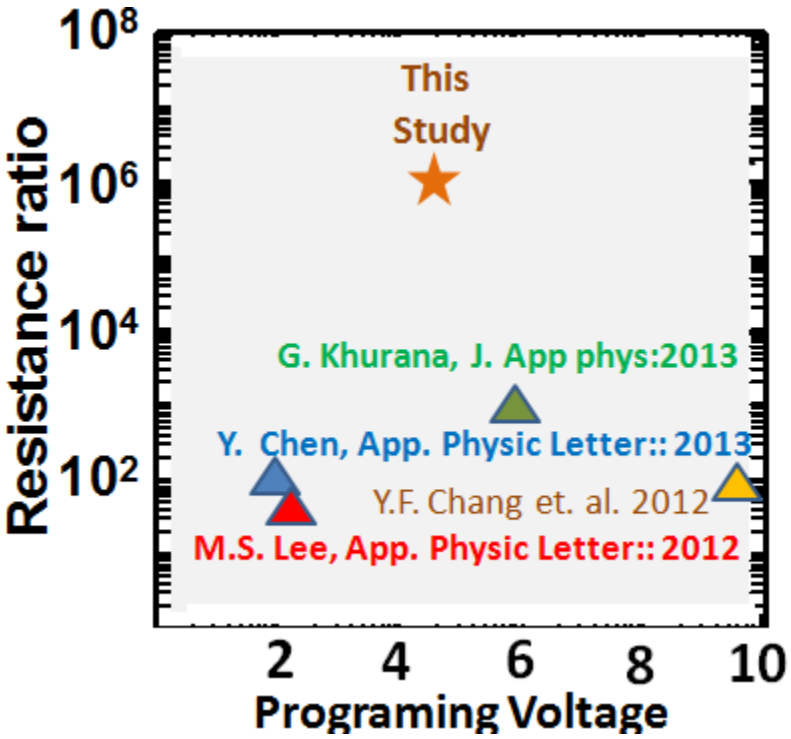

Figure 7.1 Position of this study, compared to other ReRAM with forming free

Suitable structures in terms of device optimization for various applications are summarized in Figure 7.2, based on the discussion in Chapter 5. By fabricating thin CeO_x layer the programming voltage can be suppressed. This is because the SiO_2 IL, which is formed due to the catalytic reaction during CeO_x deposition on $NiSi_2$ BE, is

dependent on the CeO_x layer thickness. Thinning CeOx buffer layer therefore will not only suppress the programming voltage but also reduce the on/off ratio.

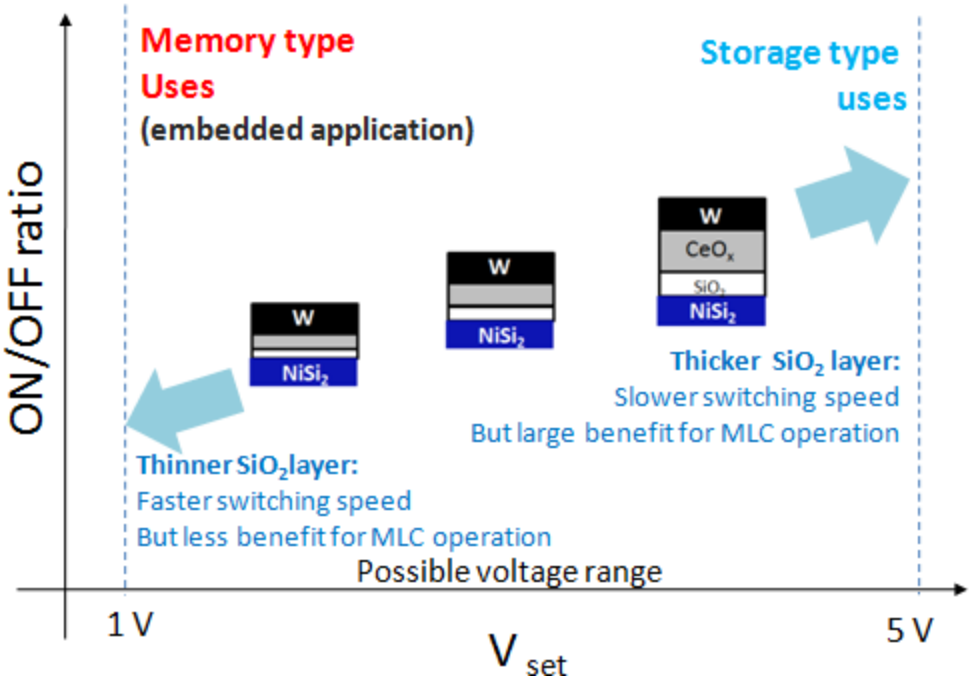

Figure 7.2 Model for device optimization recommendation

As described in Chapter 2, a thick interface layer will have a benefit for multi level cell (MLC) operation, where more bits can be applied in one memory cell. Thicker SiO_2 layer means, more resistance level can be generated, which also means the more bit number can be generated. Higher bit number in a single memory cell means higher

device density. The trade off between lower operation voltage and multi level function will be a tough issue, though.

In terms of increasing the device switching speed, preparing the buffer high-k layer material, that has higher oxygen ionic conductivity, higher k-value and narrower band gap energy than CeO_x, will be important. Both higher electron and oxygen ion conduction in the buffer layer will be desirable for lower on-state resistance and higher endurance (recovery of defects in the SiO_2 layer), respectively. Control of poly grain structure may increase the electron conductivity. Valence control of the CeO_x layer such as the addition of trivalent dopants will contribute to higher ion conductivity. In addition, as mentioned in Chapters 4 and 5 that the insulating property of low-k layer can be improved by BE annealing, which can increase the on/off ratio.

Further investigation of other device key characteristics such as retention time, and device scalability is necessary to be carried out. The scaling limit of this device is predicted to be the size of breakdown spot. For device of very small size, the breakdown spot can be localized in one location. Its scaling limit thus will be determined by the size of the breakdown spot in the low-k layer.

List of Publications and Presentations

Papers

- *Refereed:*

[1] M. Hadi, S. Kano, K. Kakushima, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, and H. Iwai, "A resistive switching device based on breakdown and anodic reoxidization of thin SiO_2 on Si-based electrodes using CeO_x buffer layer", Semiconductor Science and Technology, vol. 29, 115030, 2014.

[2] M. Hadi, N. Sugii, H. Wakabayashi, K. Tsutsui, H. Iwai, K. Kakushima, "Resistive switching properties of CeO_x buffer layer on n^+ and p^+Si bottom electrodes", Microelectronics Reliability, vol. 63, pp. 42-45, 2016.

- *Non-refereed:*

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International Conference

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