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INTEGRATION TECHNOLOGIES OF PEROVSKITE OXIDE THIN FILM CAPACITORS FOR LARGE SCALE INTEGRATED CIRCUITS

by

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Doctor of Engineering

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ABSTRACT

Capacitors play important roles in memory devices and power distribution networks for large-scale integrated circuits (LSIs). With the development of transistor integration, continuous increase in capacitance density for the integrated capacitors has been required. In addition, non-volatility in the memory capacitor and integration of μF-order capacitors into an LSI package have been also desired. Though perovskite-type ferroelectric oxides and related oxides with high dielectric constant (ε) have been promising dielectric materials for the integrated capacitors, processing for their integration into LSIs have not fully drawn out the material properties, and consequently limited practical implementation. Because the integrated capacitor's performance is determined by properties of the capacitor dielectric material, intra-connections, and interconnections, all of these factors have to be incorporated in the investigation of an integration process for ferroelectric thin film capacitors. In this study, integration technologies for major capacitor applications, including giga-bit (Gbit) dynamic random access memory (DRAM) cell capacitors, ferroelectric non-volatile memory (FeRAM) cell capacitors, and embedded decoupling capacitors, have been developed from the three viewpoints mentioned above. The validity of the developed technologies is discussed.

As the study on intra-connections for thin film capacitors, development of a RuO_2-based bottom electrode structure and their application to Gbit DRAM cell capacitors are described in Chapter 2. Because a high-temperature oxidizing atmosphere is necessary to obtain high ε perovskite-type oxide thin films, a decrease of effective capacitance caused by formation of a high-resistance or low ε oxide interfacial layer is a critical problem for high-density memory applications. Though Pt has been commonly used as a bottom electrode material for ferroelectric thin film capacitors, Pt cannot work as a barrier to

sufficiently prevent oxidation of a layer beneath it in the bottom electrode structure. Because stable conductive oxides are expected to be more effective in serving as such an oxygen diffusion barrier, RuO_2 was selected in this study as a storage electrode. The ε values for (Ba,Sr)TiO_3 (BST) thin films on RuO_2 were comparable to those on Pt, and RuO_2 was able to be chemically patterned by dry etching with $O_2 + Cl_2$ plasma, in contrast to the difficulty in patterning of Pt. To avoid Si diffusion from a Si-plug beneath the capacitor structure, a TiN-based Si barrier layer inserted between the RuO_2 layer and the poly-Si plug was also investigated. Contact resistance evaluation from *C-f* curves suggested that a RuO_2/Ru/TiN/Ti structure works well up to 550°C. The developed electrode was subsequently applied to the prototypes of 1G and 4G DRAM cell capacitors, and an equivalent oxide thickness as low as 0.4 nm was obtained.

Chapter 3 discusses improvement of the ferroelectric material properties. Composition control and crystal orientation control of ferroelectrics are effective ways to enhance the polarization density and reliability in FeRAM application. Though $SrBi_2Ta_2O_9$ (SBT) is recognized as a fatigue-free ferroelectrics, its relatively small remanent polarization (P_r) value has been one of the disadvantages in practical applications. In this study, P_r values for Sr deficient and Bi excess composition were found to be larger than those for the stoichiometric composition. Evaluation results on a dielectric anomaly of SBT thin films with various compositions revealed that Sr deficiency increases the Curie temperature. Measurements of X-ray absorption fine structure spectroscopy suggested a local structural change around Ta ions caused by the Sr deficiency. Therefore, the increase in P_r values for the Sr deficient SBT films is assumed to be an inherent aspect of the Sr deficient SBT crystal. Though Pb(Zr,Ti)O_3 (PZT) is also known as an FeRAM capacitor material, even as a major one rather than SBT, PZT thin film capacitors with Pt electrodes show polarization fatigue during

switching. Because the fatigue is recognized to be associated not with diminishing of spontaneous polarization but with pinning of domain walls, fatigue behavior is expected to depend on domain structures and switching processes. In this study, evaluation of fatigue behavior was performed on $Pb(Zn_{1/3}Nb_{2/3})TiO_3$-$PbTiO_3$ (PZN-PT) single crystals, which provided beneficial information. Rhombohedral $[001]_C$-oriented crystals did not show fatigue, whereas fatigue was observed in tetragonal phase and other orientations. The fatigue resistance is associated with an engineered domain configuration with 4 equivalent polar directions and a 71° switching process. The same fatigue anisotropy was observed in $Pb(Yb_{1/2}Nb_{1/2})O_3$-$PbTiO_3$ epitaxial films.

A heterogeneous integration process and demonstration of capacitor-embedded Si interposers for resolving power integrity issues are described in Chapter 4. Interconnection is the most important issue in this application because control of parasitic inductance and resistance has become critical with the LSI trends of lower power, higher integration density, and higher operating speed. In this study, it was found that a multi-contact 1-μF $SrTiO_3$ (STO) thin film capacitors showed an extremely lower equivalent series inductance compared to conventional multi-layer ceramic capacitors. Therefore, such a capacitor is assumed to be promising as an integrated decoupling capacitor. To minimize parasitic inductance due to wirings, a heterogeneous integration process based on a via-middle chip-to-wafer bonding process has been developed. The developed process enabled to contact the decoupling capacitor in the Si interposer directly with an LSI. In addition to the decoupling capacitor integration, an integration process of an *LC* filter with a Si interposer was also studied for a novel 3D-stacked buck converter application. To reduce the parasitic resistance of the inductor, a 15-μm-thick 3-layer wiring process over the STO thin film capacitor has been developed without degradation of the capacitor properties.

Integration technologies for ferroelectric thin film capacitors have been developed in terms of ferroelectric material properties, intra-connection, and interconnection. Application of STO thin dielectric films and Ru-based electrodes has been revisited for future DRAMs to alleviate process complexity. Though integration of SBT and PZT thin film capacitors appears to be pausing for the last decade, ferroelectric HfO_2 will boost highly-integrated FeRAM development. "More Moore" scaling of ferroelectric thin film capacitors will continue in these memory applications. On the other hand, "More than Moore" technologies for combining the ferroelectric technology with Si interposers will become more important in heterogeneous integration applications. The developed technologies and guidelines will be helpful for integration of ferroelectric thin film capacitors to enhance LSI performance.

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Chapter 1
INTRODUCTION

1-1 Background

1-1-1 Evolution of integrated circuits

Development of integrated circuit technologies has been bringing the evolution of computing systems. Not only have the technologies enhanced processing speed, they also have downsized, diversified, and popularized computing systems. Nowadays, we use many personalized computing systems, such as a personal computer, a smartphone, and a game console, and are also surrounded by computerized home appliances and computer-controlled infrastructures.

Large-scale integrated circuits (LSIs) are mainly used as the central processing unit (CPU) and the main memory in the organization of a computer hardware which is shown in Fig. 1-1-1. It is because processing speed and the number of functionalities of the

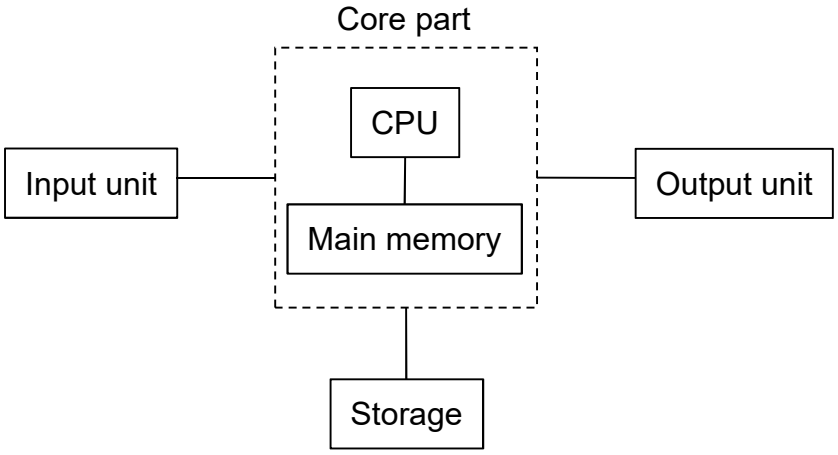

Fig. 1-1-1. Organization of typical computer hardware.

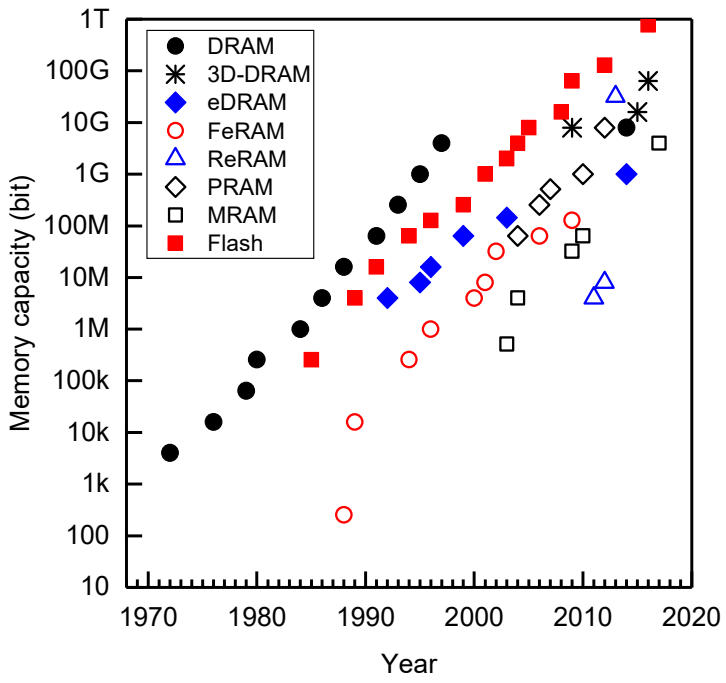

Fig. 1-1-2. Development trends for various memories as a function of the first presentation year at ISSCC.

processor and memory devices are directly associated with computing performance. Conveniently, processing speed and power consumption are improved by downsizing field-effective transistors (FETs). Great effort, therefore, has been made to miniaturize devices.

One of their typical integration trends appears in memory development, which can be seen in the presentations at International Solid-State Circuits Conference (ISSCC). Figure 1-1-2 shows a change in the memory capacity for various memories as a function of the first presentation year. The memory capacity for discrete dynamic random access memory (DRAM) monotonically increased until the 1990s. The DRAM has been commonly used as the main memory in various computing systems. Development of embedded DRAM (eDRAM) and ferroelectric random access memory (FeRAM) launched since the 1990s. This trend suggests the functionality enhancement for the LSIs.

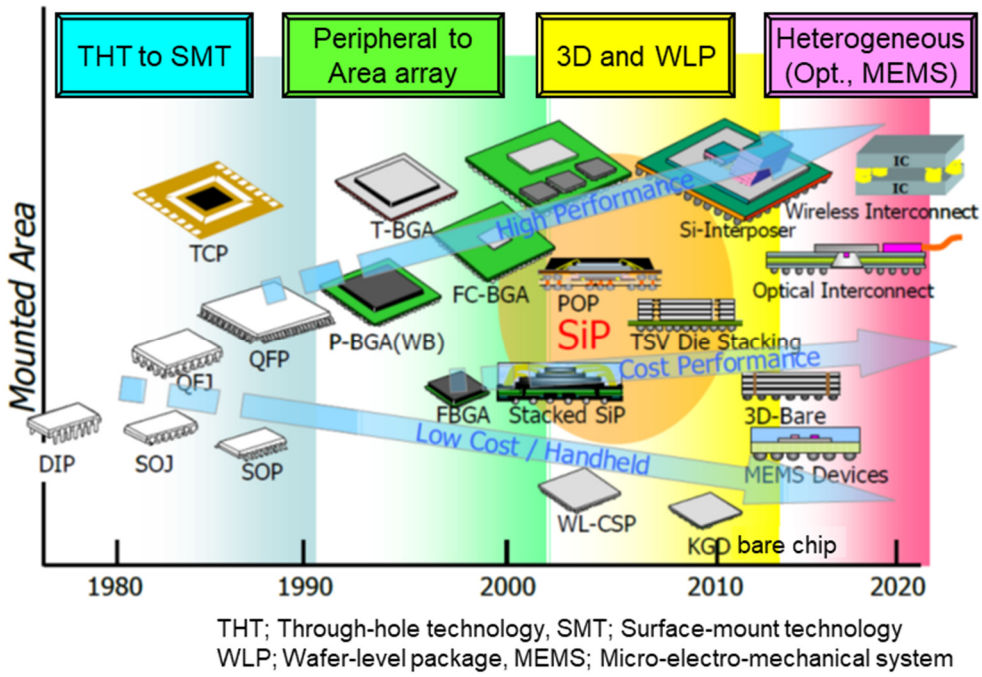

Fig. 1-1-3. LSI package development trend [1].

The eDRAM technology allowed logic LSIs to be integrated with high-performance DRAMs. The FeRAM added non-volatility to RAMs. In the 2000s, non-volatile random access memory (NVRAM) development diversified into resistive RAM (ReRAM), phase-change RAM (PRAM), and magnetic RAM (MRAM), and their memory capacity have been increasing steadily over the last decade. Heterogeneous integration, as well as conventional monolithic integration, has come to be recognized as a pragmatic approach to enhance functionality and performance for LSIs in the 2010s. Three-dimensionally-stacked DRAM is a typical example of this trend. As can be seen in Fig. 1-1-2, the development trends for integrated circuits are not only increasing density by miniaturization but also enhancing functionalities and heterogeneous integration.

Similar trends appear in the LSI package development as shown in Fig. 1-1-3. With increasing the number of I/O pins, area-array-type packages have been developed in the 1990s. Multi-chip package (MCP) as well as single chip package (SCP) has been widely used since the 2000s. In particular, a single package that contains multiple LSIs and

performs as a system or sub-system is called System-in-Package (SiP). Some of the LSIs in the SiP are stacked for further enhancement of integration density and performance.

These development trends reflect the evolution of computing systems. Mainframe computers drove the enhancement of memory capacity for the discrete DRAM at their golden age. In the 1990s, most electronic equipment went digital with the application of microprocessors or microcontrollers. Various computing systems were distributed in our life. Integration of main memories and storage with logic LSIs was desired in such systems so that NVRAMs and their embedding technologies were developed. Currently, computing systems have been more blended into society. Even non-electronic products are being equipped with computing devices and connected to the internet. In the Internet of Things (IoT) era, input and output devices are desired to be integrated with processors and memories at front-end computing systems, and further integration of processors and memories is required for processing huge amount of data at back-end computing systems. Heterogeneous and three-dimensional (3D) integration is a promising technique for these applications.

1-1-2 Role of capacitors in LSIs and requirements for capacitor integration

The LSI development is primarily driven by the FET scaling. Meanwhile, various devices other than the FETs are also integrated into an LSI. They have to be downsized with miniaturizing FETs. A capacitor is one of these devices and plays important role in electronic circuits.

The capacitor is a passive device that stores electronic charges. The representative application of the integrated capacitor in digital LSIs is data storage in DRAMs. Charged and discharged states correspond to binary digits. As well as the integrated capacitors, discrete capacitors also utilized in practical circuits. Because charging and discharging

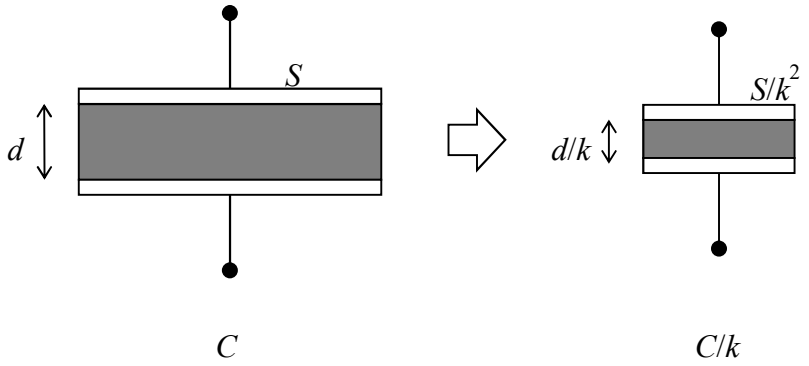

Fig. 1-1-4. Geometrical scaling of a capacitor.

behavior compensates instantaneous voltage fluctuation, the capacitors are needed to be placed between a power supply and an LSI. In particular, many capacitors are positioned very close to a microprocessor in current computers. The capacitors are indispensable for basic operations of the core part of current computing systems.

From the viewpoint of the evolution of LSIs described in the previous section, the demands for the capacitors in the core part of the computing systems are high capacitance density, non-volatility, and integration of discrete capacitors.

High capacitance density is the representative issue of the capacitors. The capacitance value (C) for capacitors is expressed by

$$C = \epsilon_0 \epsilon_r \frac{S}{d}, \tag{1-1}$$

where ε_0 is permittivity of vacuum, ε_r is relative dielectric constant, S is the electrode area, and d is the dielectric thickness. Though the performance of metal-oxide-semiconductor field effect transistors (MOSFETs) is enhanced by miniaturization, the capacitance value decreases by scale-down as shown in Fig. 1-1-4. Because a certain capacitance value, typically 20 to 30 fF for a DRAM cell capacitor, is necessary independently of the degree of integration, capacitance density has to be increased with miniaturization.

Non-volatility is required from the trend of the storage memory integration. Non-

semiconductor memories, such as hard disk drives (HDDs), optical disks, and magnetic tape, have been commonly used as the storage. Because integration of these memories into LSIs is not practical due to their storage mechanism, size, and speed, a rewritable non-volatile semiconductor memory is strongly desired to enhance the performance of computing systems. In contrast to the DRAM used as the main memory, the data in the storage memory is retained after power-off. Though read only memory (ROM) is a kind of non-volatile memory, the ROM is not rewritable and the memory capacity is generally small. Flash memory, which is a kind of rewritable non-volatile memory, has been used in microcontrollers. Read and write operations and endurance for the flash memory are different from those for the DRAM, so that DRAM-type non-volatile memory is preferable for various applications.

Integration of discrete capacitor is necessary for the further enhancement of integration. Heterogeneous and hybrid integration will further expand in both the front-end and back-end computing systems in the IoT era. A package with such integration architecture includes multiple Si chips. Because only a limited number of discrete components other than Si chips can be integrated into a package, most passive components working with the integrated chips, such as decoupling capacitors and filters, are left on a board. This limits the integration density and the performance of the computing systems.

1-1-3 Capacitors used in computing systems

The most commonly used capacitor dielectric material integrated into LSIs is SiO_2. The SiO_2 is a stable and good insulating oxide with a relative dielectric constant (ε_r) of 3.9. Because a SiO_2 layer can be formed by oxidation of Si substrate, it has been used as a capacitor dielectric since the beginning of integrated circuits [2, 3].

Regarding DRAM cell capacitor development, a simple planar structure came to an end with 1M (mega-bit) DRAM, and three-dimensional (3D) structure was employed since 4M DRAM to increase effective electrode area and consequently capacitance density [4-6]. In addition to the 3D cell capacitor structure development, Si_3N_4 and Ta_2O_5, as well as SiO_2, were studied for use as a dielectric material for the DRAM cell capacitors at the beginning of this study because the ε_r values for these materials are larger than that for SiO_2. However, even the ε_r value for Ta_2O_5 is about 20 that is only 5 times larger than that of SiO_2, so that a drastic solution was required for the realization of giga-bit-scale (Gbit-scale) DRAMs.

Among the discrete capacitors, multilayer ceramic capacitors (MLCCs) are placed right near LSIs owing to their small size, large capacitance, and impedance properties. The capacitor dielectrics generally consist of TiO_2 or $BaTiO_3$. The minimum case size for the prevalent MLCCs at the beginning of this study was 1608M, which stands for 1.6 mm × 0.8 mm × 0.8 mm. Though their capacitance values were much larger than that for integrated thin film capacitors, the capacitance density per footprint was consequently comparable to that for the integrated capacitors. Because MLCCs are fabricated by stacking micron-order-thick dielectric and electrode layers and co-firing them, it is difficult to integrate the MLCCs with LSIs. Even the current smallest MLCC, which is 01005M-size (0.1 mm × 0.05 mm × 0.05 mm), is too thick to be integrated into a Si chip.

Figure 1-1-5 summarizes the capacitance density and the dielectric thickness of DRAM capacitors and MLCCs at the beginning of this study. The capacitance per cell area for Mbit-scale DRAMs was less than 100 fF/μm^2. The maximum capacitance values for 1608M MLCC were less than 100 nF [7]. In order to integrate the MLCCs with Si chip, the dielectric layer thickness had to be reduced to less than 1 μm.

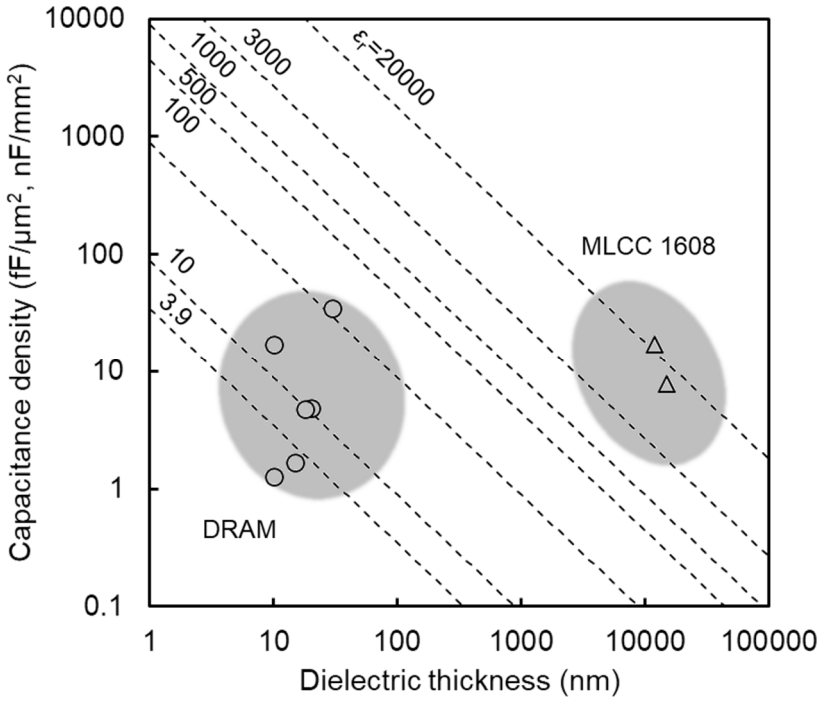

Fig. 1-1-5. Status of existing capacitors at the beginning of this research.

1-1-4 Advantages of ferroelectric capacitors

As explained in 1-1-3, the common and important issue for the capacitor integration into future LSIs is an increase of the capacitance density. One of the solutions for this issue is the application of ferroelectric thin film capacitors. It is known that the ε_r values for some ferroelectric thin films are several hundred, which is more than 10 times larger than the ε_r values for SiO_2 and Ta_2O_5. In addition to the high ε_r value, spontaneous polarization is available for the memory element. The spontaneous polarization maintains without an external electric field, and it can be reversed by the external field. These phenomena are usable for non-volatile memory operation. Therefore, application of ferroelectric thin films has been expected to make a contribution to the development of computing systems.

1-2 Prior Studies on Perovskite Oxides and Their Integration

1-2-1 Ferroelectric materials and their applications

Ferroelectric materials are a family of pyroelectric and piezoelectric materials and are characterized by spontaneous polarization which is reversible by applying external electrical field. Some of the ferroelectric and related materials also show very high permittivity which is mainly due to ionic polarization. Because these features of ferroelectrics provide a new mean for controlling electronic charges, the ferroelectric materials, especially oxides, have been utilized and played an important role in electronic circuits. Piezoelectricity converts mechanical energy and electricity mutually and is applied to ultrasonic transducers and actuators. Some infrared sensors use pyroelectricity, which senses temperature change as the change in the polarization. High permittivity of ferroelectrics has contributed to the development of ceramic capacitors. Ferroelectric non-volatile random access memories (FeRAMs) make use of ferroelectricity itself, namely polarization reversal, and it is the only application to integrated circuits (ICs) in contrast to other discrete device applications mentioned above.

The early history of ferroelectrics is reviewed in Refs. [8, 9]. Ferroelectricity was first found in 1921 on a single crystal Rochelle salt by J. Valasek. In the 1940s, dielectric anomaly and ferroelectricity of barium titanate ($BaTiO_3$) were discovered and it rapidly grew into useful ferroelectric materials for practical electronic device applications. The commercial barium titanate devices debuted about 1947. Another great advance for practical device applications was the discovery of very strong piezoelectricity on lead zirconate titanate, $Pb(Zr,Ti)O_3$, in the 1950s.

These useful ferroelectric oxides belong to the perovskite family. The unit cell of these oxides is characterized by oxygen octahedron and the simplest chemical formula is

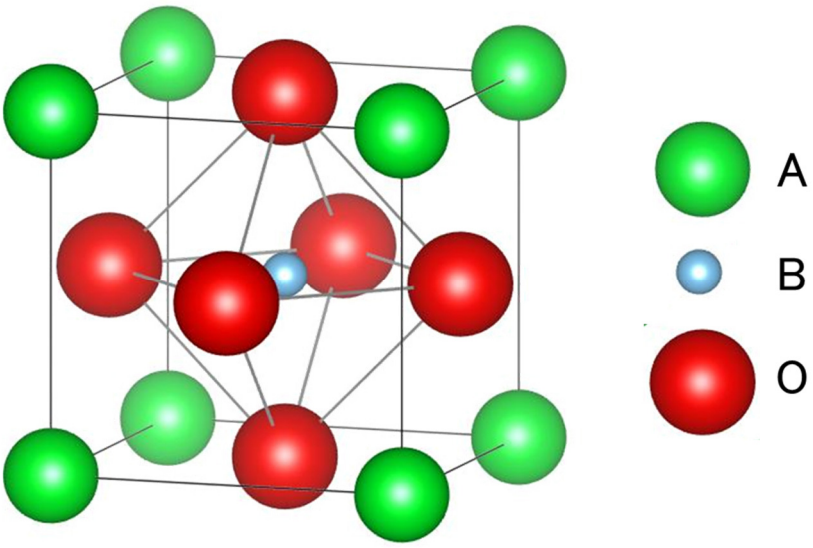

Fig. 1-2-1. Perovskite structure. The drawing was produced by VESTA [10].

expressed by ABO_3, where A and B is metallic ions, as shown in Fig. 1-2-1. In these oxides, the displacement of the positive-charged metallic ions and the negative-charged oxygen octahedron is the dominant origin of spontaneous polarization and high electrical permittivity.

The reasons why these oxides are important for practical applications are structural stability, ease of preparation and handling in polycrystalline ceramic form, and wide property variation by additives or compositional substitution, as well as outstanding ferroelectric and piezoelectric properties near room temperature. Because intensive efforts on electronic device applications since discovery have been made, the ferroelectric devices are extensively used in modern electronic equipment. Nevertheless, the practical use of the ferroelectric oxides has been mainly limited in discrete devices.

1-2-2 Integration of ferroelectric thin films into integrated circuits

The discovery of the ferroelectric oxides was contemporary with the invention of ICs. The ICs have been making progress in enhancing their functionalities and

performance as well as integration density and miniaturization. Producing many devices onto a die reduces fabrication and assembly costs and enhances reliability and usability. Another important driving force for the progress has been transistor scaling, which means geometric scaling leads to enhance transistor performance.

It is thought that integration of ferroelectric oxides into ICs started soon after the discovery. Though simple cross-point type cell memory was proposed in the 1950s, a disturbance was a fatal problem. Moll and Tarui [11] attempted to control the mobility of semiconductor CdS by the remanent polarization of ferroelectric triglycine sulfate, and non-volatile memories with ferroelectric gate were mainly studied in the 1970s. Practical non-volatile memories with cell selection transistors were presented by Eaton *et al*. [12], and Evans and Womack [13] in 1988. Their memory cell composed of 1 transistor and 1 capacitor, which is the same as that of the DRAM cell. Then, practical use of ferroelectricity has started with FeRAMs in 1992 [14]. Integration density of current commercial FeRAMs attains a mega-bit level, which is three orders of magnitude lower than that of DRAMs. Therefore, the FeRAM market is predicted to be limited in industrial and transportation applications.

1-2-3 Perovskite oxide thin films for DRAM cell capacitors

Because the increase of the required capacitance density was critical for the DRAM cell capacitor applications, various high ε_r thin films had been studied for the applications. Some of the ferroelectric oxides, which has extremely high ε_r values of hundreds to thousands in bulk form, were attractive candidates for storage capacitor dielectrics in Gbit-scale DRAMs. Because the DRAM capacitor application does not require the spontaneous polarization and the polarization switching, ferroelectric materials in paraelectric phase are suitable for the applications [15].

The first report on DRAM cell capacitors with ferroelectric-related oxides was given by Koyama *et al*. [16]. They developed 256M DRAM cell capacitors. The $(Ba_xSr_{1-x})TiO_3$ (BST) thin film was sputter-deposited onto Pt/Ta electrodes. Fujii *et al*. [17] also reported the cell capacitor with a BST dielectric layer and a Pt/TiN/Ti bottom electrode. The BST layer was fabricated by metal organic decomposition (MOD). Application of Pb-based ferroelectrics, such as $Pb(Zr,Ti)O_3$ and $(Pb,La)(Zr,Ti)O_3$, were reported by Moazzami *et al*. [18], Torii *et al*. [19], and Okudaira *et al*. [20]. Pt was also used as a bottom electrode material in their reports. Though they showed electrical properties for their capacitors, the cell structure with these materials was not reported.

1-2-4 Integration of discrete capacitors with Si

With regard to integration of discrete capacitors, GaAs microwave monolithic ICs (MMICs) preceded Si LSIs [21-23], discrete ferroelectric thin film decoupling capacitors on Si also started in the 1990s. Dimos *et al*. [21] and Imanaka *et al*. [22] reported discrete PZT and BST capacitors, respectively. These capacitors looked like LSI chips and were provided with solder balls for flip-chip bonding. Though these capacitors had low inductance values and were expected to be effective for decoupling in a high-frequency region, miniaturization of MLCCs have enhanced their usability, and consequently, MLCCs have occupied the vicinity of an LSI in current computing systems.

However, the layout for conventional decoupling capacitors has been becoming critical for high performance and low power LSIs [26, 27]. Figure 1-2-2 shows the prediction for the required capacitance (C_{req}) and the target impedance (Z_{target}) estimated from the data in Refs. [27] and [28] by the following equations.

$$C_{req} = \frac{P}{2f \times V_{dd}{}^2 \times n}, \qquad (1\text{-}2)$$

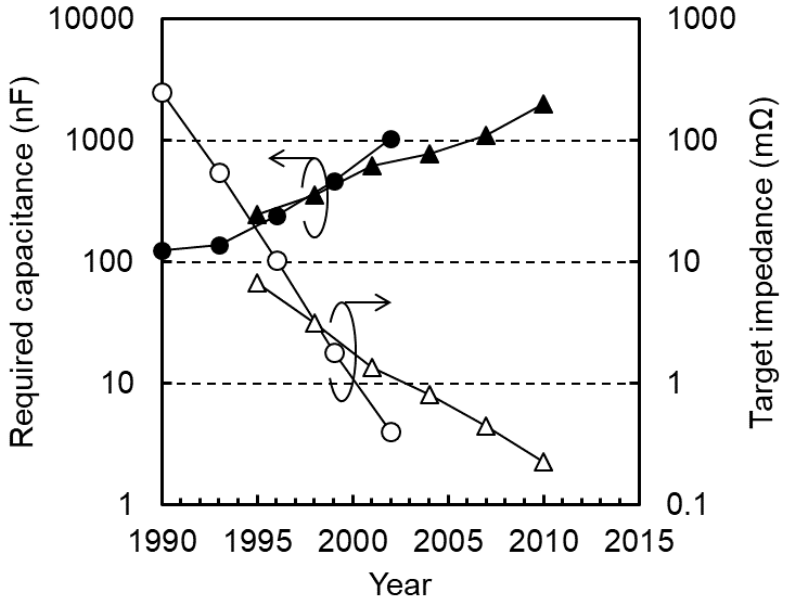

Fig. 1-2-2. Trends of the required capacitance for decoupling and the target impedance. Circles and triangles were estimated from the data in [27] and [28], respectively.

$$Z_{\text{target}} = \frac{V_{\text{dd}}{}^2 \times n}{P}, \tag{1-3}$$

where P is the power, f is the clock frequency, V_{dd} is the power supply voltage, and n is the allowed ripple (5%). The μF-order larger capacitance value and lower target impedance are required for highly integrated systems. It will be difficult for the MLCCs to reduce power distribution network (PDN) impedance at a GHz frequency range because inductance for wirings and pads between an LSI and the decoupling capacitors cannot be negligible. Direct connections between LSIs and the capacitors are suitable for minimizing the parasitic inductance. A Si interposer is a promising platform for the thin film capacitor integration. Because the total capacitance value per a DRAM chip exceeded 1 μF after 64M generation as shown in Fig. 1-2-3, it is reasonable to apply DRAM capacitor technologies to the decoupling capacitors on the Si interposers. Roozeboom *et al*. [29] developed trench metal-oxide-semiconductor (MOS) capacitors

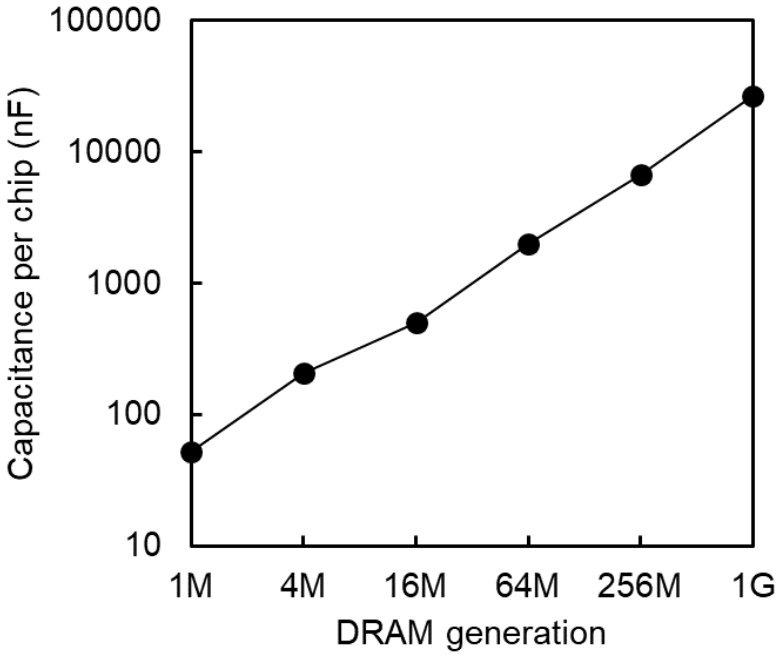

Fig. 1-2-3. Total capacitance value per a DRAM chip.

and demonstrated a Si-on-Si module with a capacitor-embedded passive die and an IC chip. The IC chip was flip-chipped onto the passive die. The passive die was bonded to a lead frame at the same side of the IC chip. Knickerbocker *et al*. [30] proposed a Si interposer with decoupling capacitor and through-Si-vias (TSVs). The developed capacitor was also a trench MOS capacitor. There are no reports on the integration of perovskite oxide thin film capacitors with TSVs in the beginning of the study.

1-3 Objectives

1-3-1 Issues in ferroelectric thin film integration

As described above in this chapter, applications of perovskite oxides to LSIs have been limited and their potential has not been fully drawn out although these materials have been regarded as useful to enhance LSI performance. The most important reason

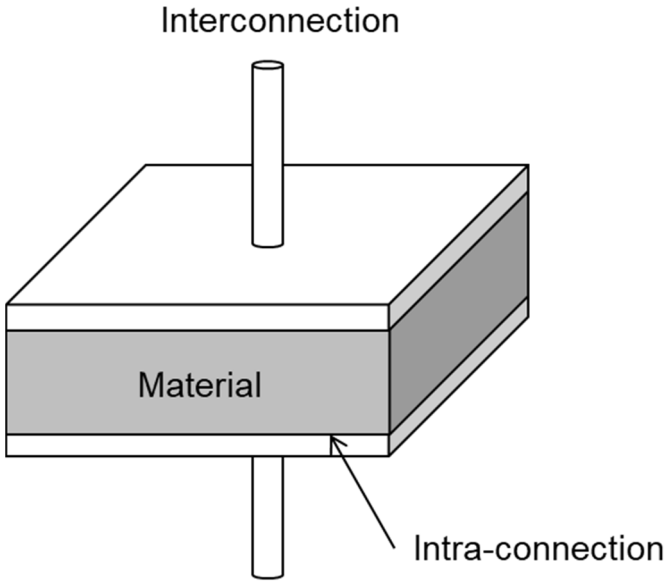

Fig. 1-3-1. Key factors for thin film capacitor integration.

why the applications of ferroelectric thin film capacitors to LSIs were limited was an insufficient performance for the integrated capacitors. The capacitor performance, such as charge storage capability, charging and discharging behavior, stability and so on, is determined by intrinsic dielectric material properties, intra-connection, and interconnection (Fig. 1-3-1). The intrinsic material properties include stability and reliability as well as capacitance. The intra-connection means electrode materials and their interfaces inside the capacitor. The interconnection is a state of the connection between the capacitor and the outside. Fabrication process and form factor are also included in the intra-connection and the interconnection. The intra-connection and the interconnection cause deterioration of effective performance for the integrated capacitors because the capacitor is a passive device.

In the DRAM capacitor application, the intra-connection, as well as the dielectrics, plays an important role in obtaining high capacitance density. Because the ferroelectric or high ε_r oxide film is generally deposited in an oxidizing atmosphere at a higher

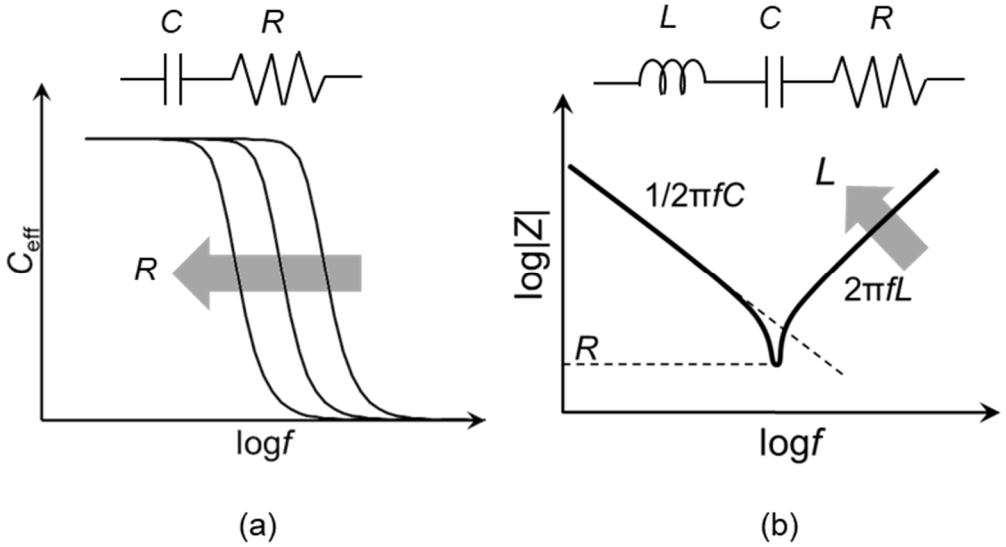

Fig. 1-3-2. Influence of parasitic resistance and inductance on (a) effective capacitance and (b) impedance.

temperature than 400°C, noble metals were used as an electrode. However, a low ε_r or high resistance layer was often formed at the interface between the dielectric layer and the electrode. It resulted in a decrease of effective capacitance as shown Fig. 1-3-2(a). In addition, reactive etching for noble metals is very difficult, so that their fine patterns cannot be obtained. A patternable and stable electrode, therefore, is needed for the DRAM application.

The FeRAM capacitor application requires ferroelectric polarization reversal. Difference between switching and non-switching charges, which roughly correspond to the polarization, should be as large as possible. However, the polarization decreases with increasing temperature and by repeated switching. Because these degradation phenomena arise from inherent material properties, deep understandings and improvement of the material properties are necessary for this application.

The ferroelectric capacitors in the heterogeneous integration application work in a coordinated manner with other devices. Not sensing electronic charges but charging and

Table 1-3-1. Key issues for perovskite oxide thin film capacitor applications.

Key factor	DRAM capacitor	FeRAM capacitor	Heterogeneous integration
Material	✓	✓✓	✓
Intra-connection	✓✓	✓	✓
Interconnection			✓✓

discharging processes for the capacitors are mainly used in this applications. The response of the capacitor is influenced by parasitic inductance and resistance as shown in Fig. 1-3-2(b), which are governed by packaging structure and configuration for the capacitor and connected devices. Therefore, interconnection is the most important.

The key issues for each application are summarized in Table 1-3-1.

1-3-2 Objectives and the structure of the thesis

In this study, integration technologies on the material, intra-connection, and interconnection for perovskite oxide thin film capacitors have been studied to expand the applications to LSIs which are used in the core part of computing systems. The problems and future directions for their integration are discussed. The structure of the thesis is shown in Fig. 1-3-3. The thesis consists of five chapters.

Chapter 1 introduced contribution of ferroelectric thin film capacitors to computing systems and prior studies on perovskite oxide thin films and their integration into LSIs. The objectives of the thesis were also defined.

Chapter 2 describes the development of Gbit-scale DRAM cell capacitors. $SrTiO_3$ and $(Ba,Sr)TiO_3$ are used as the capacitor dielectrics. As well as properties of a dielectric layer themselves, storage electrode materials and their interconnections are keys for monolithic integration. When a low ε_r or high resistivity layer is formed by interdiffusion,

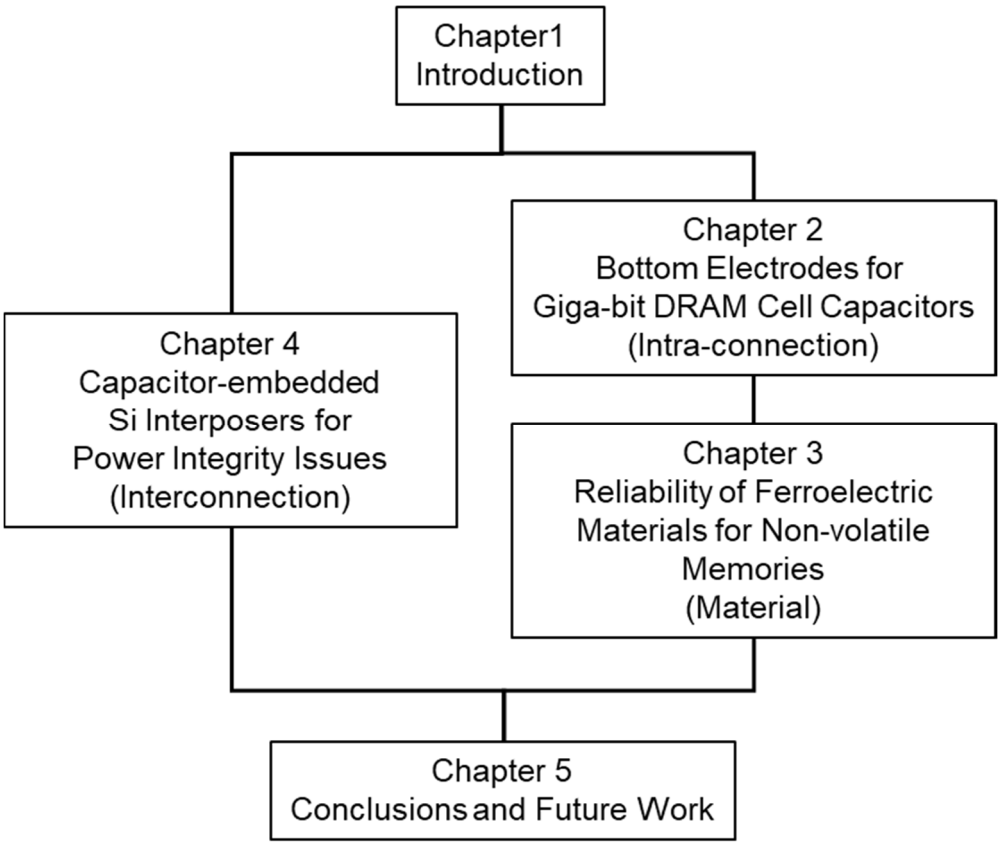

Fig. 1-3-3. Structure of this thesis.

an effective capacitance value for the cell capacitor reduces. Enhancement of thermal stability for the storage electrode is discussed, and the prototypes of 1G (giga-bit) and 4G DRAM cell capacitor structures are demonstrated.

Chapter 3 describes the development of ferroelectric materials for FeRAM capacitors. Bi-layered perovskites, such as $SrBi_2Ta_2O_9$, and $Pb(Zr,Ti)O_3$ have been generally recognized as candidates for FeRAM capacitor ferroelectrics. $SrBi_2Ta_2O_9$ have relative small remanent polarization though they show excellent ferroelectric fatigue endurance. The small remanent polarization degrades a readout signal. On the other hand, $Pb(Zr,Ti)O_3$ with a large spontaneous polarization value shows fatigue which limits

read/write cycles in the memory application. These phenomena reflect ferroelectric nature for these materials. Composition control of the remanent polarization for $SrBi_2Ta_2O_9$ and crystallographic orientation control of ferroelectric fatigue for Pb-based ferroelectric oxides are discussed.

Chapter 4 describes the development of capacitor-embedded Si interposers. The capacitor integration is required another important role in emerging 3D integration. Power integrity, such as suppression of simultaneous switching noise and proper power delivery, becomes critical when multiple LSIs are integrated into a package. Integration of $SrTiO_3$ thin film capacitors with through-Si-vias and other passive devices and control of parasitic inductance and parasitic resistance are discussed. Applications to a 3D-stacked decoupling capacitor directly connected to an LSI and a 3D-stacked buck converter have been proposed.

Chapter 5 summarizes the thesis, discusses its findings and contributions, and directions for future work.

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Chapter 2
BOTTOM ELECTRODES FOR GIGA-BIT DRAM CELL CAPACITORS

2-1 Introduction

2-1-1 Dynamic random access memory (DRAM) cell capacitor

DRAM is widely used as a main memory in current computing systems because of large memory capacity, low bit unit cost, and relatively fast read/write operation. Because miniaturization enhances these features, DRAM technology and market have been considered as a driving force for geometrical scaling of semiconductor devices.

A DRAM cell which stores binary data consists of a storage capacitor and a switching transistor as shown in Fig. 2-1-1. Binary digits are distinguished by sensing

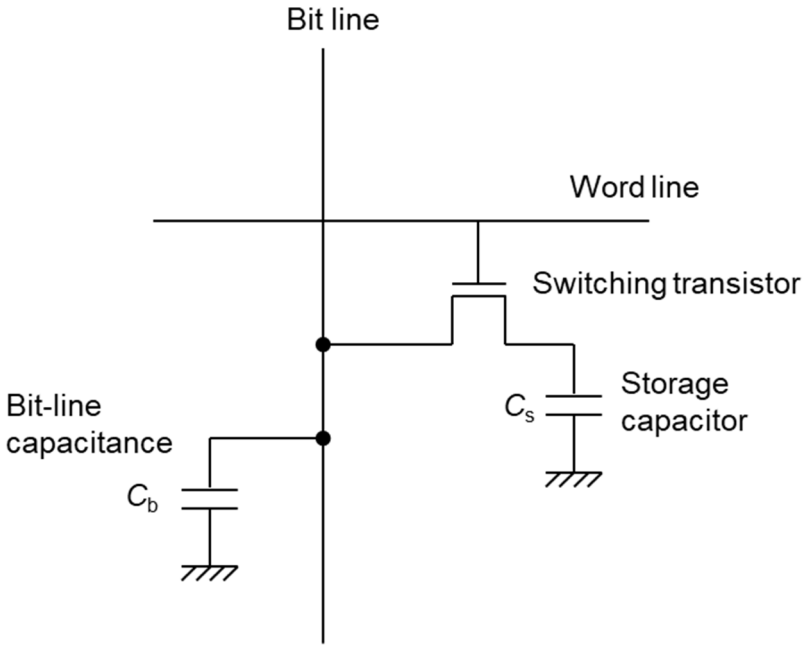

Fig. 2-1-1. DRAM cell.

stored charges in the capacitor. In a read operation, the stored charges are transferred to the bit line and the bit line is charged. The charged voltage called the bit-line voltage (ΔV_b) is given by

$$\Delta V_b = \frac{1}{2} V_{DD} \frac{1}{1 + C_b/C_s}, \tag{2-1}$$

where V_{DD} is the supply voltage, C_b is the bit-line capacitance, and C_s is the storage node capacitance. The C_s value is typically required to be around 30 fF to obtain a large enough ΔV_b value against the sense amplifier sensitivity. Because the required C_s value for discrete DRAMs is independent of the geometrical scaling, the storage capacitance density increases with miniaturization.

The electrostatic capacitance (C) of a capacitor is expressed by

$$C = \varepsilon_0 \varepsilon_r \frac{S}{d}, \tag{2-2}$$

where ε_0 is the permittivity of a vacuum, ε_r is the relative dielectric constant, S is the effective electrode area, and d is the dielectric thickness. When the S value decreases by downsizing, there are some approaches to maintain the required capacitance. These approaches are decreasing dielectric thickness, increasing effective area with 3-dimensional (3D) structure, and application of high ε_r dielectrics. In practice, 3D cell structures such as trench or stacked capacitors have been used since 4M (mega-bit) DRAMs.

Though complex 3D cell structures have been reported to enhance capacitor area, it is insufficient to apply giga-bit-scale (Gbit-scale) DRAMs as long as SiO_2 is used as a capacitor dielectric. Figure 2-1-2 shows the required equivalent oxide thickness (EOT) for various cell structures [1]. The EOT value is a kind of figure of merit for comparison of charge storage performance between different dielectric materials and defined by

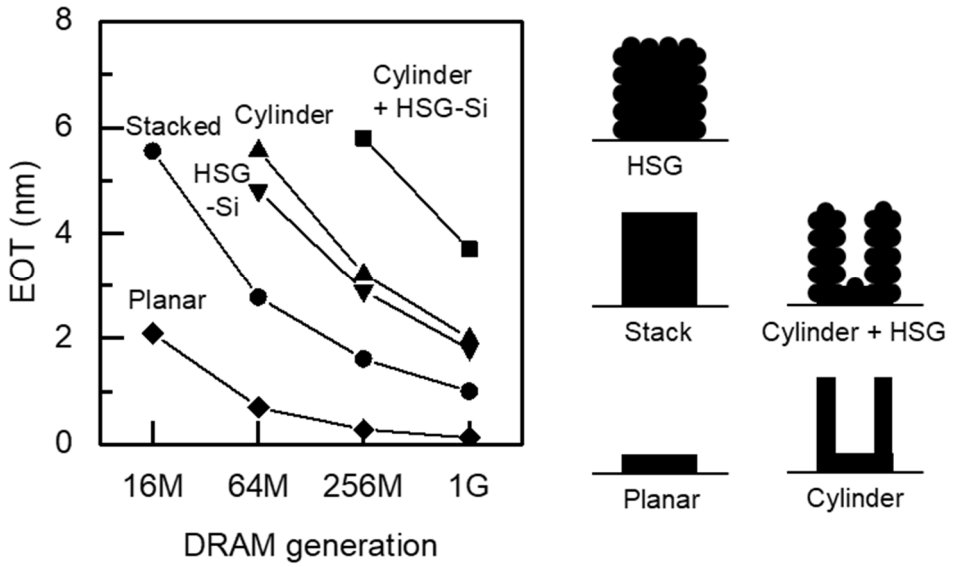

Fig. 2-1-2. Relationship between DRAM cell capacitor structures and equivalent oxide thickness [1].

$$\mathrm{EOT} = \frac{3.9}{\varepsilon_r} d \ , \tag{2-3}$$

where 3.9 is the relative dielectric constant of SiO_2. When the simple planar cell is applied to 1 Gbit DRAM, the EOT value has to be lower than 0.13 nm. Even though 3D cells of the stack, hemispherical grained-Si (HSG-Si) and cylinder structures, and their combination structures increase the capacitor effective area, the expected EOT value for 1 Gbit DRAMs is lower than 4 nm, which is too small to use SiO_2 or Si_3N_4. Therefore, integration of high ε_r materials is desired for Gbit-scale DRAMs. In order to achieve simple cell structures, the EOT value should be less than 1 nm for Gbit-scale DRAMs.

2-1-2 Prior studies on high dielectric constant oxides for DRAM capacitors

Tantalum oxide, Ta_2O_5, has the ε_r value of around 20 and was a candidate for use as a capacitor dielectric for Gbit DRAMs. Shibahara *et al.* [2] and Kaga *et al.* [3] developed

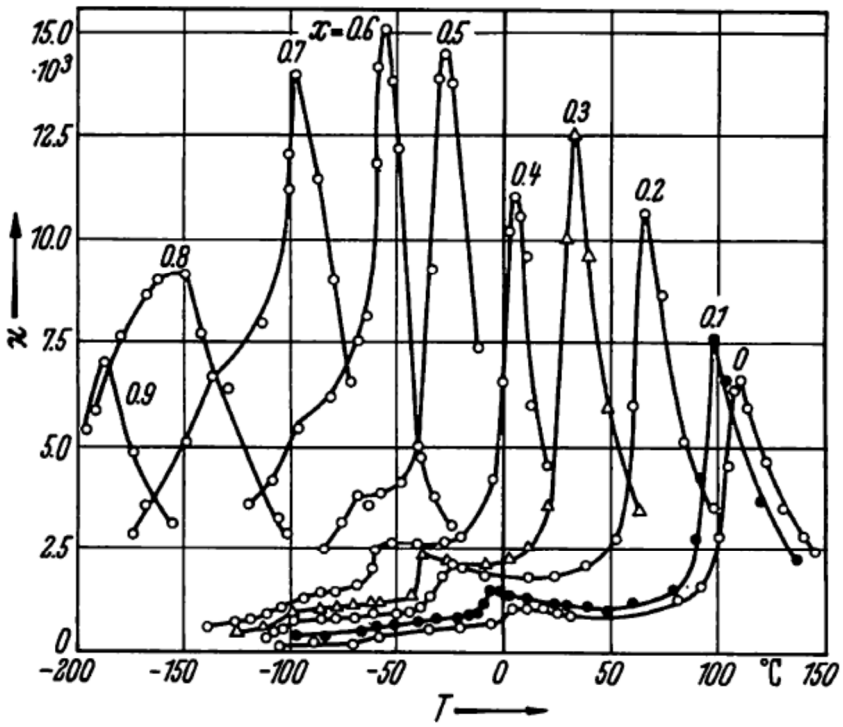

Fig. 2-1-3. Composition and temperature dependence for $(Ba_{1-x}Sr_x)TiO_3$ ceramic [5].

Ta_2O_5 storage capacitors with complex 3D structures for 1 Gbit DRAM. Their EOT values were 2.5 nm and 1.6 nm, respectively. Though the EOT values were applicable to 1 Gbit DRAMs, they were insufficient for 4 Gbit DRAM or beyond.

Some ferroelectric oxides, which has extremely high ε_r values of hundreds to thousands in bulk form, are attractive candidates for storage capacitor dielectrics in Gbit-scale DRAMs. Because the DRAM capacitor application does not require the spontaneous polarization and the polarization switching, ferroelectric materials in paraelectric phase are suitable for the application [4]. $(Ba_{1-x}Sr_x)TiO_3$ (BST) is the solid solution of $SrTiO_3$ (STO) and $BaTiO_3$ (BTO) and is paraelectric at room temperature when $x > 0.3$, as shown in Fig. 2-1-3 [5]. Miyasaka and Matsubara [6] reported that the maximum ε_r of 870 was obtained at $x = 0.5$ for sputtered BST thin films.

Table 2-1-1. Silicide formation temperature for various metals [9, 10].

Element	Temperature (°C)
Pt	200
Pd	100
Ru	375
Ir	400
Ph	350
Ti	500
Ta	650

2-1-3 Integration issues in DRAM cell capacitor application

From the integration point of view, intra-connections, as well as dielectric properties themselves, become important issues. Because these oxide thin films are generally deposited at a temperature higher than 400°C in an oxidizing ambient, interface reaction or diffusion between the oxide film and the electrode often forms a low ε_r or high resistance layer. For example, a SiO_2 layer is formed between the oxide and Si when STO or BST thin films are deposited directly onto silicon substrates [7, 8]. It causes reduction of the effective capacitance of the thin film capacitor. Therefore, the ferroelectric and high ε_r oxide films have to be deposited onto stable and metallic electrodes even in an oxidizing ambient. Refractory noble metals such as Pt were commonly used as the bottom electrodes for the ferroelectric and high ε_r oxide thin film capacitors to avoid reactions between the oxide and the electrode. The refractory metals, however, often react silicon to form silicides at a relatively lower temperature as shown in Table 2-1-1 and the silicide formation results in low ε_r SiO_2 layer formation during the ferroelectric oxide film deposition.

Therefore, development of storage electrodes, as well as ferroelectric thin film deposition, becomes essential to achieve Gbit-scale DRAM capacitors by using ferroelectric oxide thin films. This chapter describes the development of storage electrodes for Gbit-scale DRAMs as the intra-connection issue.

2-1-4 Objectives of this chapter

As described above, the effective capacitance value for high ε_r thin film capacitors is decreased by unintended reactions and interdiffusion in the capacitor electrodes. This is a fatal problem for the Gbit-scale DRAM cell capacitor application even though high ε_r thin films can be deposited. Therefore, development of thermally-stable, oxidation-resistant, and fine-patternable electrode and barrier layers is necessary for the applications.

Conductive oxides are attractive materials for use as the bottom electrodes because they are expected to maintain conductivity after exposure in an oxidizing atmosphere during perovskite oxide thin film deposition. In particular, ruthenium dioxide, RuO_2, has been considered to be a candidate for the electrode material because RuO_2 is metallic and stable.

This chapter describes the development of RuO_2-based storage electrodes for Gbit-scale DRAM cells and demonstrates that improvement of thermal stability for the electrodes achieves 1G and 4G DRAM cell prototypes. The target EOT values for the capacitors were 1 nm for 1G DRAM and 0.5 nm for 4G DRAM. The problems of Pt-based electrodes, advantages of RuO_2 for use as an electrode material, and thermal stability for RuO_2-based electrodes with various barrier layers are also discussed.

2-2 Issues in Pt-based Electrodes [11]

Because the features of perovskite oxides originate from crystallographic nature, perovskite oxide thin films are usually deposited in an oxidizing atmosphere to obtain high-quality oxide crystals. The oxidizing atmosphere often results in a low ε_r or high resistance oxide formation. When STO or BST thin films are deposited directly onto silicon substrates, an SiO_2 layer is formed between the oxide and Si, and then causes reduction of the effective capacitance for the thin film capacitor [7, 8]. Therefore, electrode materials for high ε_r thin film capacitors have to be stable in an oxidizing ambient.

Noble metals, particularly Pt, are the candidate for the electrode materials. It has been previously reported that high effective ε_r values of approximately 200 and 400 were obtained for 100-nm-thick STO films deposited at 400°C and BST films deposited at 600°C, respectively, on the Pt/Ta or Pt/Ti electrode [6, 8, 12, 13]. According to these previous studies, the Pt/Ta and Pt/Ti electrodes appear deceptively to be suitable for use as the bottom electrode from the viewpoint of material stability. In this section, the structural changes in Pt/Ta and Pt/Ti bilayers on Si with annealing in vacuum and in oxygen to simulate the practical thin film deposition process is described, and the problem of the Pt-based electrodes for integration into high-density DRAMs is defined.

2-2-1 Structural changes in Pt/Ta and Pt/Ti stacking structures by annealing

Because practical thin film deposition process environment is too complicated to be experimentally simulated, the influence of annealing in vacuum and in oxygen on the Pt/Ta and Pt/Ti bilayers on Si has been investigated. The sample preparation was as follows. The 0.01-0.05 Ω·cm *n*-type Si(100) wafers were cleaned using buffered HF

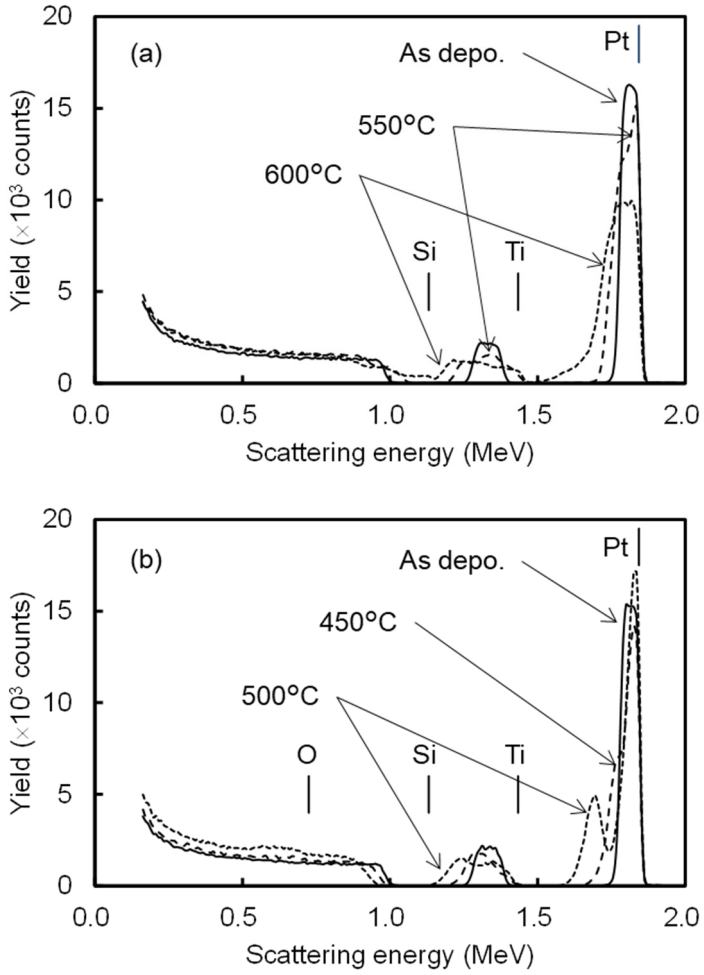

Fig. 2-2-1. RBS spectra for Pt(50 nm)/Ti(150nm)/Si stacking structures annealed (a) in vacuum and (b) in oxygen. Vertical lines indicate the surface scattering energies.

solution to remove native oxide. Then, the Pt/Ta or Pt/Ti layers were deposited on the cleaned wafer by DC magnetron sputtering. The Pt layer thickness was 50 nm and the Ta and Ti layer were 50 nm or 150 nm thick. These samples were annealed in vacuum (< 5 × 10^{-6} Torr) or in an oxygen atmosphere (760 Torr) at a temperature ranging from 450°C to 800°C, for 2 h. Structural changes after annealing were analyzed by X-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), and cross-sectional transmission electron microscopy (XTEM).

Figures 2-2-1(a) and 2-2-1(b) shows RBS spectra for the Pt(50 nm)/Ti(150 nm)

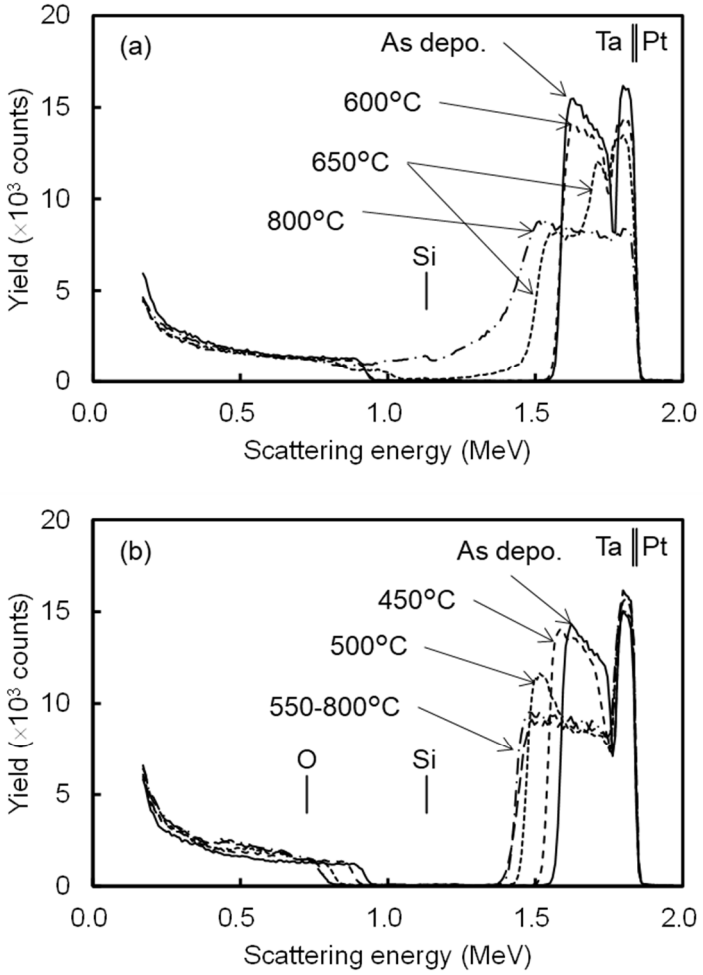

Fig. 2-2-2. RBS spectra for Pt(50 nm)/Ta(150nm)/Si stacking structures annealed (a) in vacuum and (b) in oxygen. Vertical lines indicate the surface scattering energies.

bilayers on Si annealed in vacuum and in oxygen. Incident ion beam was 10 μC of 2 MeV He^{2+}. Interdiffusion between Pt and Ti and between Ti and Si occurred simultaneously at a relatively low temperature. Si atoms reached to the surface after annealing at 550°C. With annealing in oxygen, Ti and Si oxidation occurred, as well as interdiffusion. In addition, the Pt signal for the sample annealed in oxygen at 500°C has two maxima. This implies that Pt content has two maxima in composition depth profile. The region between these maxima mainly consists of TiO_x ($1 \leq x \leq 2$), measured by Auger electron

spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS). This feature was also observed in the spectra of the samples annealed at a temperature between 500°C and 700°C.

RBS spectra for the Pt(50 nm)/Ta(150 nm)/Si stacking structures annealed in vacuum and in oxygen are shown in Fig. 2-2-2. In the case of vacuum annealing, the only interdiffusion between Pt and Ta is observed below 600°C and tantalum silicide was formed at higher than 600°C. Si was detected at the surface after vacuum annealing at 800°C. On the other hand, the Ta layer in the Pt(50 nm)/Ta(150 nm)/Si stacking structures is oxidized from the surface side with annealing in oxygen, and the stacking structure transformed to the Pt/TaO_x ($x \approx 2$)/Si at a temperature higher than 500°C. The resultant layered structure is stable even after annealing at 800°C. Because the silicidation temperature of Ta is higher than 600°C, the Ta layer is oxidized before silicide formation, which results in layered Ta oxide and Si diffusion barrier to the surface.

XRD and TEM analyses for these bilayers on Si were consistent with the RBS interpretation. These changes were independent of the Ti or Ta layer thickness. The structural changes in these structures are summarized in Fig. 2-2-3.

The above structural analysis indicated that thermal stability of the Pt/Ta bilayer was superior to that of the Pt/Ti bilayer. The Ta layer, however, is oxidized by annealing in oxygen in spite of being covered with the Pt layer. In order to clarify the conductivity of oxygen-deficient Ta oxides, their current-voltage characteristics were measured. After Pt(50nm)/Ta(150 nm)/Si was annealed in oxygen, the Pt layers were patterned into 0.3 mm × 0.3 mm squares, as upper electrodes, by etching with hot aqua regia. The rear surface electrode on Si consisted of sputtered Au(300 nm)/Ti(50 nm). Consequently, the Pt/TaO_x(300-400 nm)/Si/Ti/Au structure was obtained. The waiting time for each step was 2 s and measurements were carried out at room temperature. The results are shown

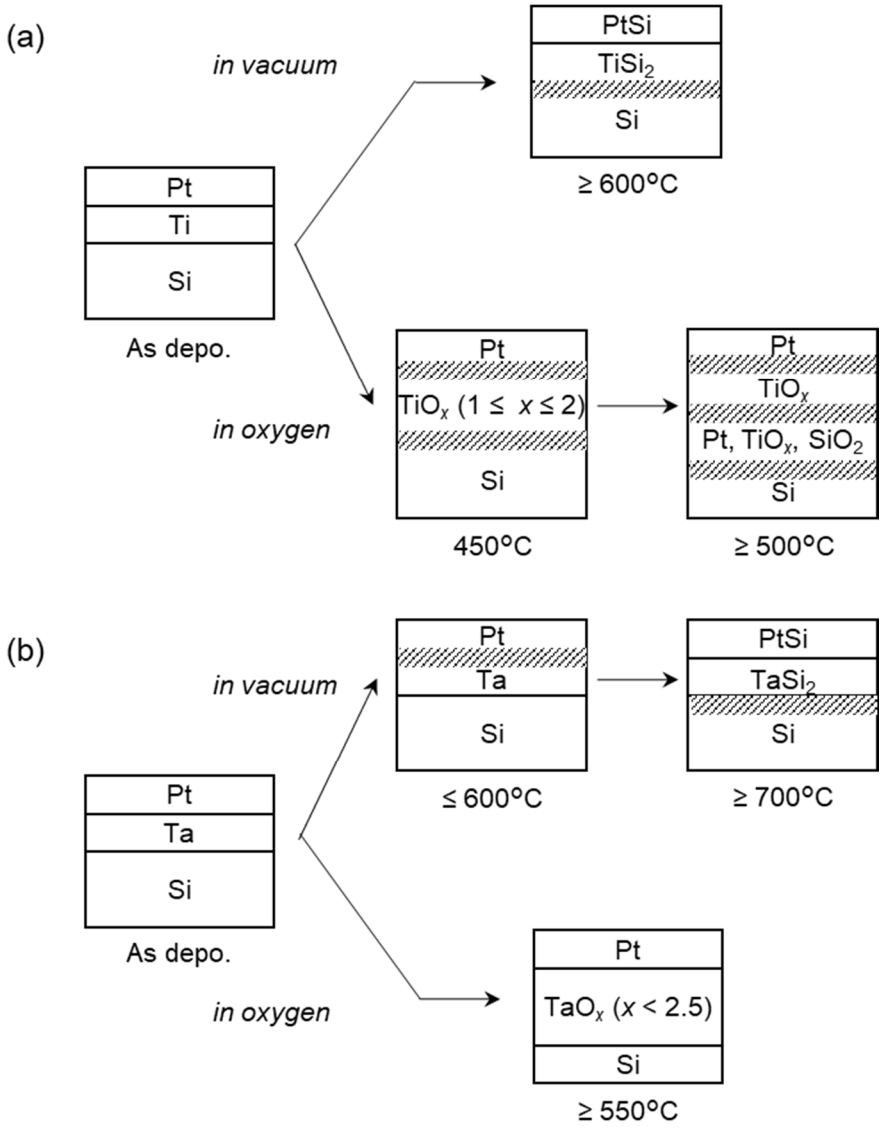

Fig. 2-2-3. Structural changes in (a) Pt/Ti/Si and (b) Pt/Ta/Si stacking structures by annealing in vacuum and in oxygen. Shaded parts mean interdiffusion. In the case of Pt/Ti annealed in vacuum, the PtSi layer contains Ti and the $TiSi_2$ layer contains Pt. In the case of Pt/Ti annealed in oxygen, Pt silicide was not detected by XRD and XPS measurements.

in Fig. 2-2-4. Resistivity for the TaO_x layer formed after oxygen annealing at 550°C was the order of 10^6 Ω·cm, and the TaO_x layer formed at higher temperatures was almost insulator. When a Ta/Si stack without a Pt layer was annealed in oxygen under the same conditions, an insulating Ta_2O_5 layer was formed. A current-voltage curve for the Ta_2O_5

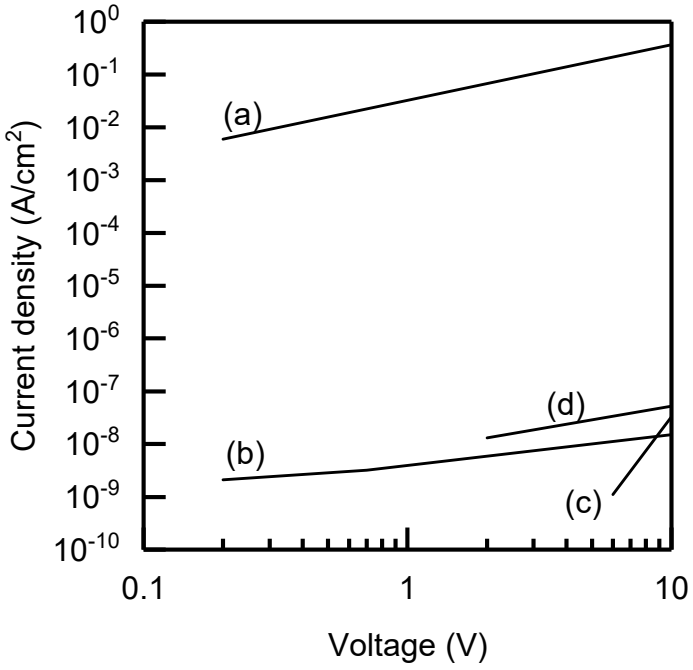

Fig. 2-2-4. Current-voltage characteristics for TaO_x layers in Pt/Ta/Si annealed in oxygen at (a) 550°C, (b) 600°C and (c) 800°C, and (d) for the Ta_2O_5 layer in Ta/Si annealed in oxygen at 500°C.

formed at 500°C is also shown in Fig. 2-2-4. The resistivity of a Ta oxide layer under Pt, formed at lower than 600°C, is much lower than that for Ta_2O_5. The Pt layer limits oxidation speed and composition although the Pt layer does not act as a complete oxygen barrier.

2-2-2 Structural changes in Pt/Ta and Pt/Ti electrodes by STO film deposition

The situation of oxide film deposition processes is different from that of simple annealing processes in vacuum and in oxygen. Therefore, structural changes and electrical properties of the Pt/Ti and Pt/Ta stacking structures after STO thin film deposition have been investigated.

The ε_r value for the STO thin films deposited on the Pt/Ti electrodes reduced with annealing at a higher temperature than 500°C and the barrier effect achieved by Pt/Ti

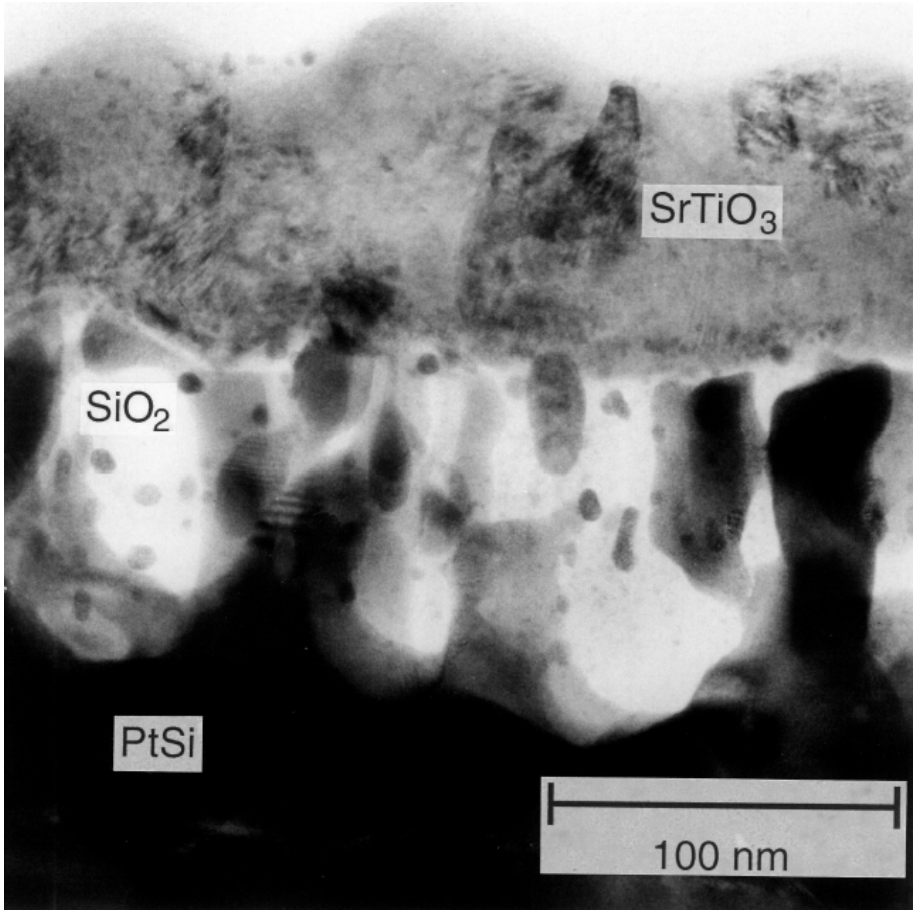

Fig. 2-2-5. Cross-sectional TEM image of a $SrTiO_3$/Pt/Ti/Si stacking structure after annealing at 600°C.

bilayers has been thought to be inferior to that for the Pt/Ta [8]. Therefore, changes in the STO/Pt/Ti/Si stack after annealing at 600°C was observed by XTEM. The sample preparation is detailed in Ref. [8].

An XTEM image of the stacking structure is shown in Fig. 2-2-5. A SiO_2 layer is observed just underneath the STO layer. As described in 2-2-1, Si atoms reach the surface and a PtSi layer is formed by annealing in vacuum at 600°C, and oxygen passes through the Pt layer by annealing in oxygen at 600°C. Because the STO layer is assumed to limit an external oxygen supply, structural change in the STO/Pt/Ti/Si annealed at 600°C is thought to be similar to that in the Pt/Ti/Si annealed in vacuum, that is, silicide formation occurs faster than oxygen diffusion. Therefore, the SiO_2 layer is formed just beneath the

Table 2-2-1. Sputtering conditions for STO thin films.

Target	Powder (3N purity)
Substrate temperature	400, 600°C
Sputtering gas	Ar
Sputtering gas pressure	4 mTorr (0.53 Pa)
Target-substrate distance	70 mm
Input power	1.37 W/cm^2
Deposition rate	4 nm/min

STO layer and reduce the effective ε_r value.

The Pt/Ta bilayer is more suitable than the Pt/Ti bilayer for use as a Si diffusion barrier and has been applied as a bottom electrode for STO or BST thin film capacitors [8, 13]. Therefore, the dielectric thin film deposition process effect on the Pt/Ta barrier has been investigated. The Pt/Ta barrier diffusion behavior, during the dielectric thin film deposition, is discussed in this section.

The 150-nm-thick STO films were sputter-deposited on Pt(50 nm)/Ta(50 nm)/Si under the conditions listed in Table 2-2-1. In order to evaluate resistivity of the oxidized tantalum layer, the deposited STO layer was removed by HF + HNO_3 solution after the STO deposition, and the Pt layer patterning and rear surface electrode deposition were carried out in the same manner as described in 2-2-1.

Though the Pt/Ta bilayer after STO deposition at 400°C was sufficiently conductive, its resistance after STO deposition at 600°C increased to around 200 μΩ as shown in Fig. 2-2-6. This result is quite different from that obtained for the Pt/Ta structures annealed in oxygen as shown in Fig. 2-2-4. Figure 2-2-7 shows an RBS spectrum for the Pt/Ta after STO deposition at 600°C, where the STO layer had already been removed by wet-etching. Ta layer oxidation and interdiffusion between Pt and Ta were observed.

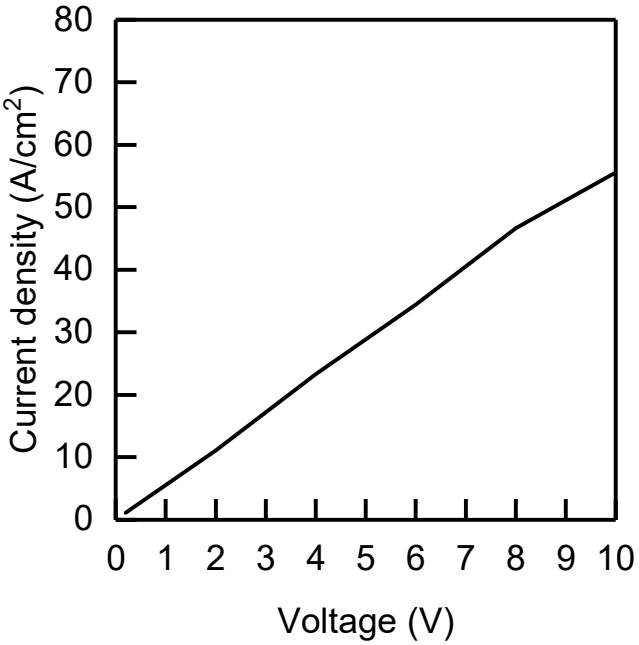

Fig. 2-2-6. Current-voltage characteristics of the Ta layer in Pt/Ta barrier after STO deposition at 600°C.

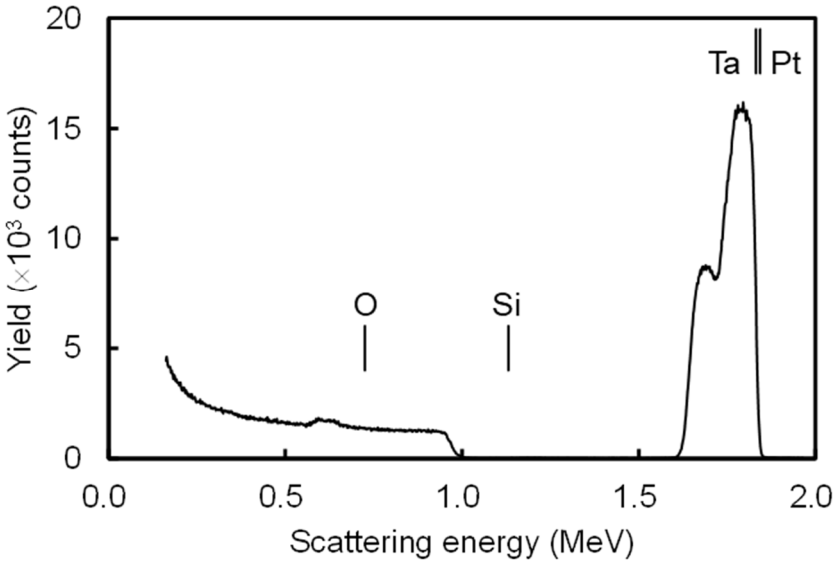

Fig. 2-2-7. RBS spectrum for Pt/Ta after STO thin film deposition at 600°C. The STO layer was removed before RBS measurement. Vertical lines indicate surface scattering energies.

The substrate temperature profile of the STO thin film deposition by RF sputtering is shown in Fig. 2-2-8. The profile can be divided into 2 stages, *i.e.* pre-heating and

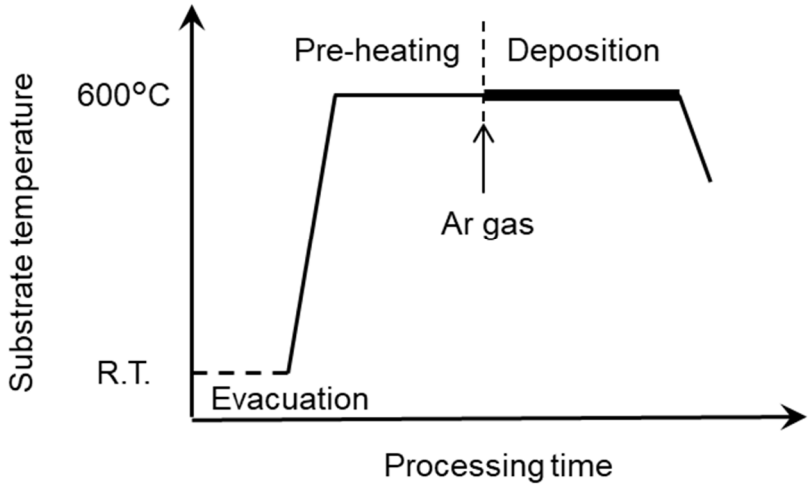

Fig. 2-2-8. Substrate temperature profile for STO deposition at 600°C.

deposition. At the pre-heating stage, the substrate is heated and kept at a deposition temperature in vacuum. Because the situation resembles vacuum annealing, interdiffusion between Pt and Ta proceeds during this period. During the successive deposition stage, sputtered particles, including oxygen, reach the substrate. The Ta layer is thought to be oxidized in this period. This tantalum oxide layer formed in the STO deposition process contains Pt, and consequently, the resistance of the resultant oxide layer is lower than that of the oxide obtained by the oxygen annealing.

2-2-3 Integration issues in Gbit-scale DRAM cell capacitors

However, the resistivity value for the Pt/Ta bilayer after STO deposition at 600°C is not low enough for use as a storage electrode in high-density DRAMs. When the storage electrode size is less than 1 μm^2, the resistance is estimated to reach MΩ order. Though a thicker Pt layer is expected to suppress the Ta layer oxidation, dry etching of the Pt layer becomes increasingly harder because reactive etching of Pt is difficult [14-16]. Therefore, it is imperative that other materials with high oxidation resistance and fine-patternability are applied to a storage electrode for Gbit DRAM capacitors.

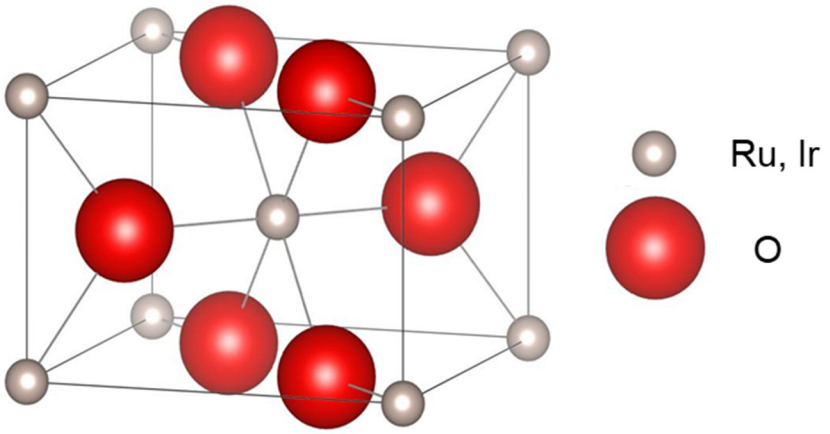

Fig. 2-3-1. Rutile structure. The drawing was produced by VESTA [17].

2-3 RuO_2 Storage Electrodes for Gbit DRAMs

As described in the previous section, Pt/Ta was not suitable for use as a storage electrode in Gbit DRAMs because of high resistance tantalum oxide formation though Ta acts as Si diffusion barrier. The bottom electrode structure, therefore, has to act as an oxygen diffusion barrier. Because Pt does not react with oxygen and consequently it does not act as an oxygen diffusion barrier, it is assumed that conductive oxides or refractory noble metals which form conductive oxides are expected to act as the oxygen diffusion barrier. Among refractory noble metals, Ru, Ir, Os, and Rh form a conductive oxide. From the viewpoints of availability and toxicity, Ru, Ir, and their oxides were considered to be the candidate for the bottom electrode of the high ε_r thin film capacitors.

Single crystalline RuO_2 and IrO_2 with rutile structure (Fig. 2-3-1) show metallic behavior in electrical and optical properties [18-20]. In particular, the RuO_2 thin film was regarded as attractive material for interconnects, contacts, gate electrodes and diffusion barriers in Si devices, because of relatively low resistivity (40 $\mu\Omega\cdot$cm at room temperature

for polycrystalline sputtered films) and a good diffusion barrier property [21, 22]. In addition to such properties, Saito and Kuramasu [23] reported RuO_2 dry-etching by O_2 + CF_4 plasma. In the ferroelectric thin film research field, Bernstein *et al*. [24] and Kwok *et al*. [25] reported that RuO_2 was effective in improving fatigue in PZT thin films. However, there were few reports about RuO_2 thin film application to bottom electrodes in BST thin film capacitors. Considering electrical properties and dry-etching, this study focused on Ru and RuO_2. This section describes their preparation and the development of barrier layers for the bottom electrodes of (Ba, Sr)TiO_3 thin film capacitors.

2-3-1 RuO_2 thin films for the bottom electrode of BST thin film capacitors [26]

RuO_x thin films were prepared by reactive DC magnetron sputtering. A mixture of Ar and O_2 gases was used as sputtering gas. O_2 content in the sputtering gas was varied from 0 to 1. Base pressure was less than 1.3×10^{-4} Pa (1×10^{-6} Torr). Total pressure during sputtering was 0.27 - 0.53 Pa (2 - 4 mTorr). The sputtering target was Ru metal (99.9 % purity). *R*-plane sapphire was used as the substrate in order to prevent the reaction between RuO_2 and the substrate, which would affect the growth and properties of BST films. The substrate temperature was monitored with a thermocouple attached to the substrate holder. Though substrates were not intentionally heated during sputtering, the measured temperature was around 40°C. The typical RuO_2 deposition rate was 7 nm/min. Crystal structures for RuO_x films were determined by X-ray diffraction (XRD). Film composition and thickness were measured by Rutherford backscattering spectrometry (RBS). Resistivity was measured by the four-probe method at room temperature.

$(Ba_{0.5}Sr_{0.5})TiO_3$ (BST) thin films were prepared with an RF magnetron sputtering apparatus. The sputtering conditions are detailed in [6]. In order to make metal-insulator-metal (MIM) capacitors, 300-nm-thick Au films were deposited by DC magnetron

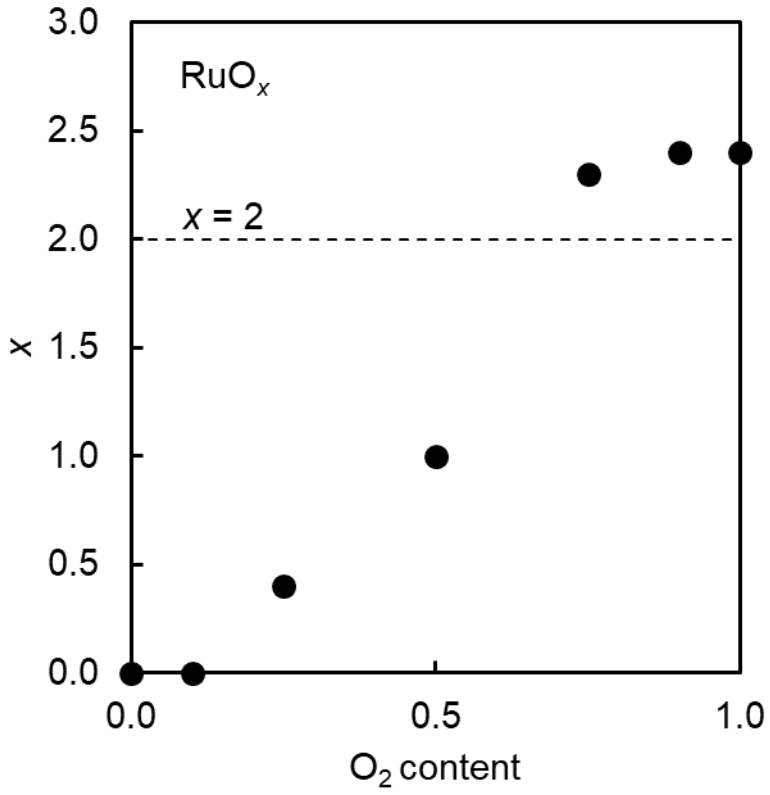

Fig. 2-3-2. RuO_x film composition as a function of O_2 content in sputtering gas.

sputtering and patterned in 300 μm × 300 μm squares by photolithography. The dielectric constants were calculated from the capacitances at 10 kHz measured with a Hewlett-Packard (currently Keysight) 4194A impedance/gain-phase analyzer. The current-voltage curves were measured with a Keithley 617 electrometer/source.

The sputtering gas composition affects the RuO_x film composition, as shown in Fig. 2-3-2. With increasing O_2 content in the sputtering gas in the range less than 0.7, x increases. When the O_2 content is greater than 0.7, x does not depend on the sputtering gas composition and maintains a constant value of approximately 2.4. Figure 2-3-3 shows XRD patterns for the RuO_x films. The film thicknesses are 200 - 400 nm. The diffraction peaks for the hcp phase were observed in the patterns of films with $x < 2$. On the other hand, broad rutile structure peaks were observed in the patterns of films with $x \sim 2.4$.

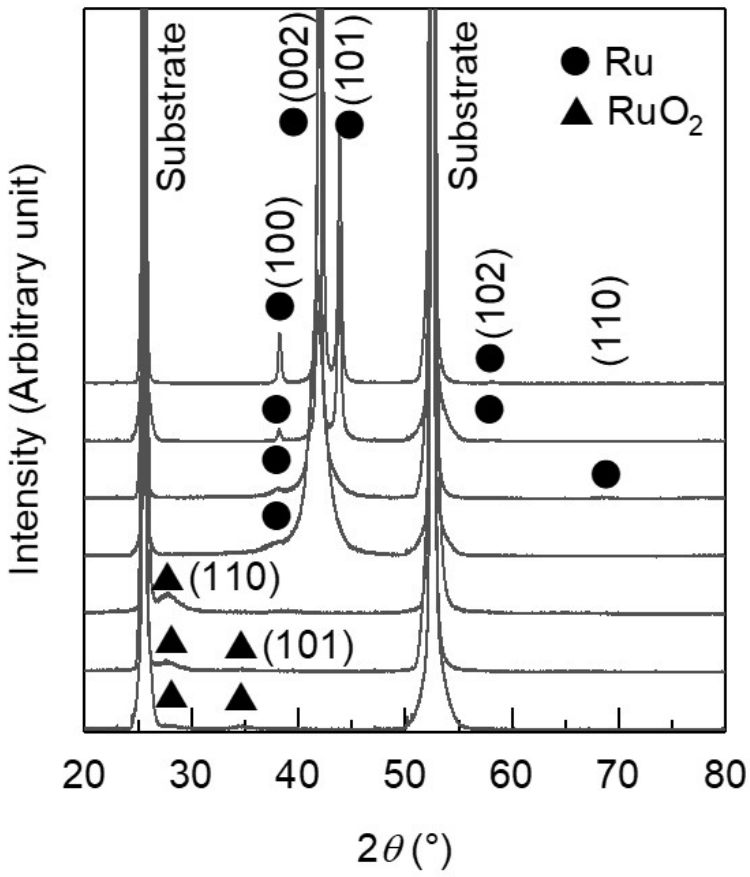

Fig. 2-3-3. X-ray diffraction patterns for reactive-sputtered RuO_2 thin films. O_2 contents for the sputtering gas are (a) 0, (b) 0.10, (c) 0.25, (d) 0.50, (e) 0.75, (f) 0.90, and (g) 1.00.

These results show that primary solid solutions with hcp structure are obtained by sputtering when the sputtering gas O_2 content was less than 0.7 and that rutile-type oxides which are so-called RuO_2 are obtained with O_2 content greater than 0.7. Resistivity values for the RuO_2 films were approximately 250 μΩ·cm at room temperature. These values are much larger than those for single crystalline RuO_2 [18, 19] and those for polycrystalline sputtered films [21, 22]. As indicated in Fig. 2-3-3, crystallinity for these films will not be good, which would cause high resistivity. These resistivity values could be reduced by annealing or deposition at a higher substrate temperature. However, 250

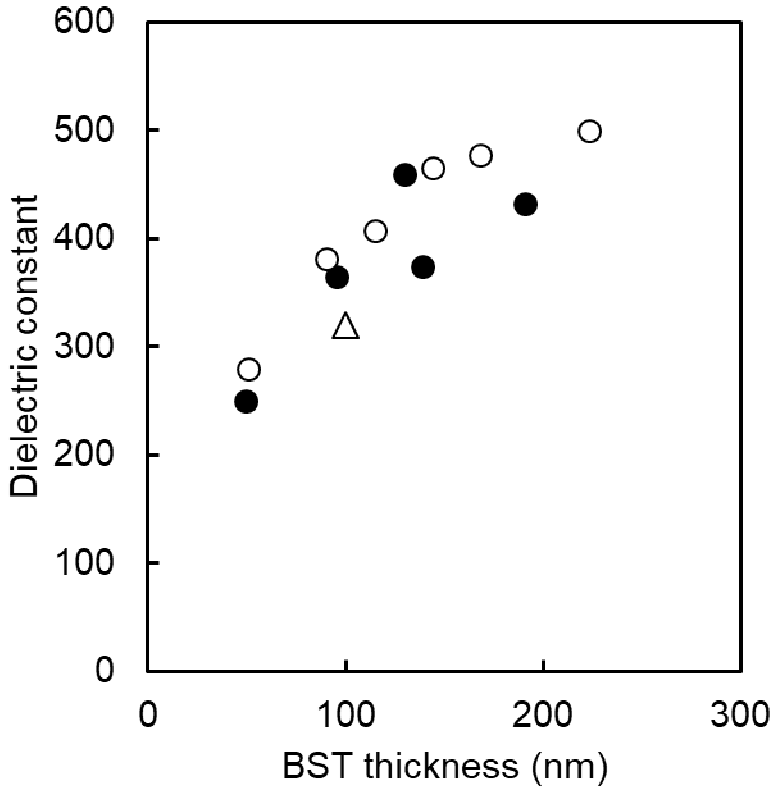

Fig. 2-3-4. Dielectric constant for sputtered BST films on RuO_2/sapphire depending on the thickness (solid circles). Open circles and triangle indicate those on Pt and Pd, respectively.

μΩ·cm will be acceptable for the bottom electrode of the high ε_r thin film capacitor, because it is comparable with the resistivity of doped poly-Si.

In Fig. 2-3-4, ε_r values for the sputtered BST films on RuO_2(150 nm)/sapphire substrate are shown by solid circles. Open circles indicate ε_r values for the sputtered BST films prepared on Pt under the same sputtering conditions. The triangle shows the ε_r value for the BST film prepared on Pd by ion beam sputtering [27]. The ε_r value on RuO_2 is as high as that on Pt or Pd electrode at each BST film thickness. Current-voltage curves are shown in Fig. 2-3-5. The leakage current density of the BST films is around 1×10^{-8} A/cm^2 up to 1 V for the 49 nm-thick film and 2 V for the 96 nm-thick film. This leakage current characteristics for the BST films on RuO_2 are also comparable with those on Pt and Pd.

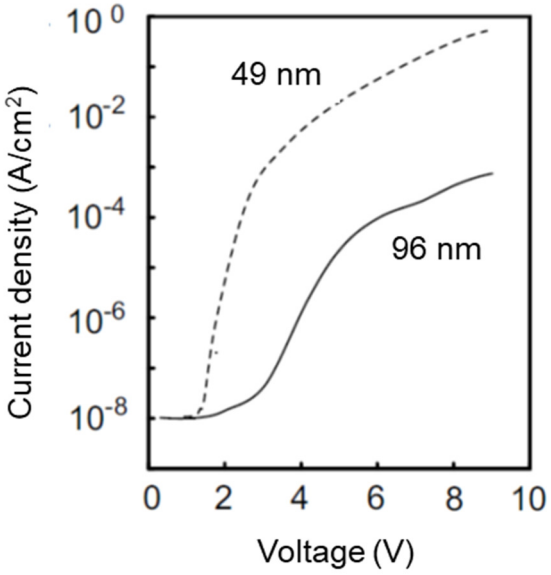

Fig. 2-3-5. Current-voltage characteristics for BST films on RuO_2/sapphire.

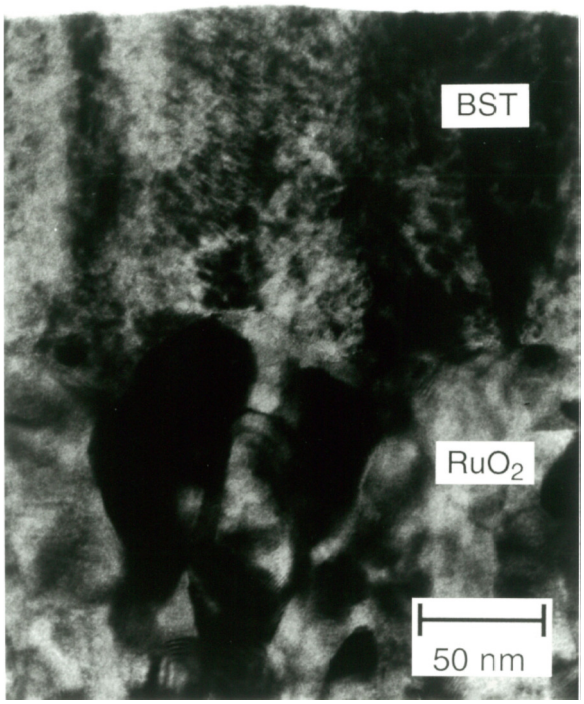

Fig. 2-3-6. Cross-sectional TEM micrograph for the BST/RuO_2 interface.

Figure 2-3-6 shows a cross-sectional transmission electron micrograph for the BST/RuO_2 interface. Composition depth profiles near the BST/RuO_2 interface region in

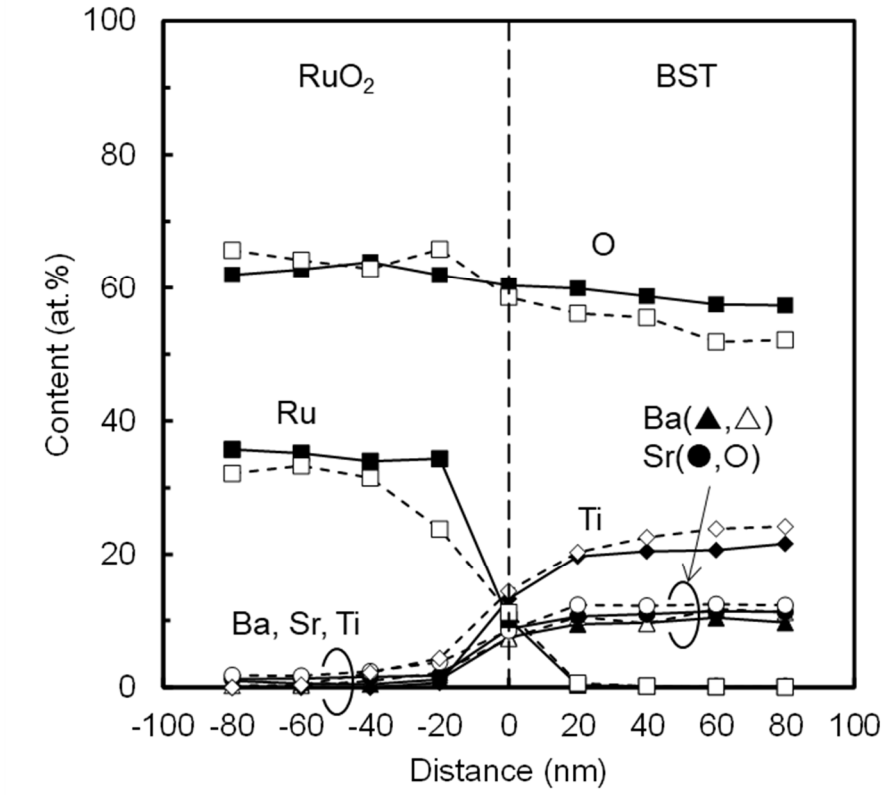

Fig. 2-3-7. Composition depth profiles near BST/RuO_2 interface.

Fig. 2-3-6 were measured by energy dispersive X-ray microanalysis and are shown in Fig. 2-3-7. Measurement points consist of two series; one is the region within a grain (solid markers) and the other is the region along a grain boundary (open markers). The electron microprobe was less than 1 nm in diameter. It can be said that there are no transition layers, such as an amorphous phase and perovskite (Ba,Sr)RuO_3 phase, and that the composition changes abruptly at the BST/RuO_2 interface. Figure 2-3-7 also shows that the BST film composition is almost stoichiometric and constant from the BST/RuO_2 interface.

Surface morphology of a RuO_2 film after the BST deposition is shown in Fig. 2-3-8. The RuO_2 surface was exposed by etching the BST film with HF + HNO_3 solution. The surface is smooth and has no hillocks, even after the BST deposition. Because hillocks often cause short-circuited capacitors, this morphology will be of great advantage to device applications, compared to using Pt.

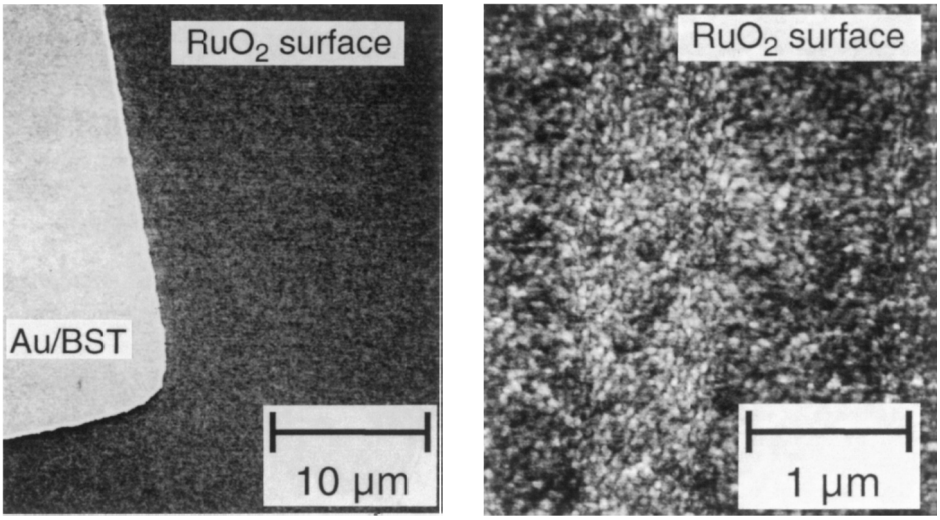

Fig. 2-3-8. SEM micrographs for the RuO_2 thin film surface after BST film deposition.

2-3-2 Barrier layer development for Gbit DRAM capacitors [28]

As described in the previous section, sputtered BST/RuO_2 interface was stable and no hillocks were observed on the RuO_2 surface even after BST deposition at 650°C, and consequently high ε_r BST thin film capacitors with low leakage current have been obtained. In addition, a thick RuO_2 layer can be easily patterned into a 0.15 μm line-and-space structure by dry etching with O_2-Cl_2 plasma [29]. However, RuO_2 cannot be deposited directly onto poly-Si plug because the interface between RuO_2 and the plug will be oxidized and act as a low ε_r layer. A Si diffusion barrier layer, therefore, is necessary between RuO_2 and the contact plug. Titanium nitride, TiN, is known as conductive and oxidation-resistive nitride and widely used as a Si diffusion barrier in LSIs [30]. Combination of RuO_2 and TiN is assumed to be appropriate for a basic electrode/barrier structure.

Grill *et al*., [31] and Yoshikawa *et al*. [32] have studied structural changes occurring in several RuO_2-based stacked structures on Si during annealing and high ε_r thin film

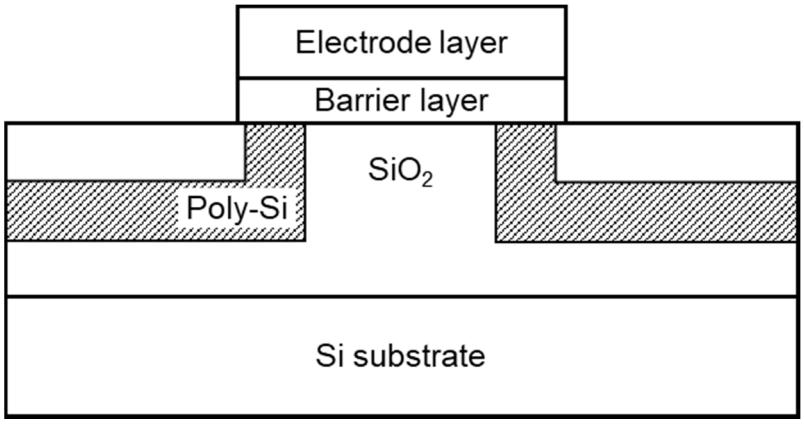

Fig. 2-3-9. Cross-section of the interconnection structure in a contact chain for the case of a multilayered electrode.

deposition. They have focused only structural stability and have not characterized the electrical properties of the RuO_2-based structures. Because even a slight degradation of the electrode/barrier or barrier/Si-plug interface affects the electrical properties of the capacitors used for Gbit-scale DRAM application, it is necessary to evaluate the electrical properties of fine-patterned electrodes.

For multilayered electrode structures such as RuO_2/TiN, it is difficult to evaluate the electrode resistance adequately with a conventional contact chain or a Kelvin pattern, when a high resistance region exists at the electrode/barrier interface. In this section, the evaluation of the electrical properties of fine-patterned storage electrodes from capacitance-frequency (*C-f*) measurements is presented for various RuO_2/TiN-based structures formed over poly-Si contact plugs.

Contact resistance in LSI devices is usually measured using a contact chain or a Kelvin pattern. Figure 2-3-9 shows a schematic cross-section of the interconnection structure in a contact chain for the case of a multilayered electrode. In the case of RuO_2/TiN electrodes, RuO_2 and TiN correspond to electrode and barrier layers, respectively. In such a test pattern, current flows through a barrier layer even when a high

resistance region exists at the electrode/barrier interface, and the measured resistance is consequently dominated by the barrier layer/Si contact resistance. In addition, the electrode/barrier interface area is considerably larger than the barrier/Si contact area at probing pads. These structures can only be used to evaluate the contact resistance of the barrier layer/Si interface, and cannot detect a resistance increase at the electrode/barrier interface. Therefore, these test patterns are not applicable for electrode resistance evaluation.

When an electrode resistance placed in series with dielectric capacitance is large enough, the dielectric dispersion can be observed in the kHz-MHz range (See Appendix). The dispersion frequency (ω_0) of the measured capacitance (C_s) is approximated as

$$\omega_0 = \frac{1}{R_e\sqrt{3C_e(C_e + C_d)}}, \tag{2-4}$$

where R_e is the resistance of the overall electrode including contact plugs, and C_d and C_e are the respective capacitance of the dielectric and the electrode. C_d and C_e can be obtained from the frequency (ω) dependence of C_s, which is approximated as follows:

$$C_s \approx C_d \quad (\omega \ll \omega_0), \tag{2-5}$$

$$C_s \approx \frac{1}{\frac{1}{C_e} + \frac{1}{C_d}} \quad (\omega \gg \omega_0). \tag{2-6}$$

These equations show that if the dispersion is only due to the existence of C_e and R_e, the electrode resistance can be estimated from *C-f* measurements.

Figure 2-3-10 shows a cross-sectional SEM image of a sample used for electrical evaluation and having a RuO_2/TiN storage electrode covered with a BST layer. The different types of RuO_2/TiN-based electrodes evaluated in this study are as follows.

A. RuO_2(500 nm)/TiN(50 nm)

B. RuO_2(500 nm)/TiN(50 nm) + RTA

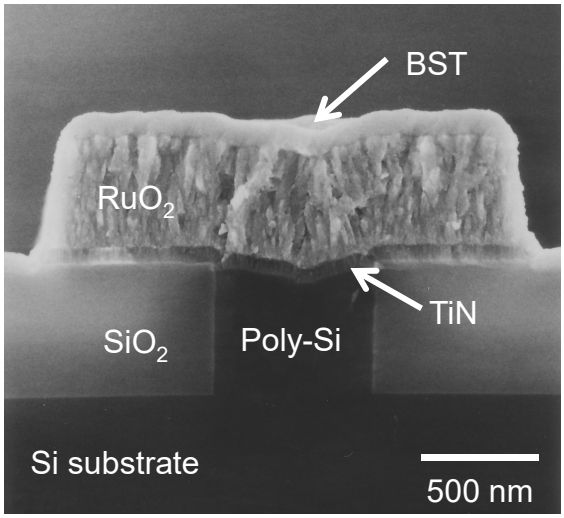

Fig. 2-3-10. Cross-sectional SEM photograph of the RuO_2/TiN storage node covered with a sputtered BST layer.

C. RuO_2(500 nm)/Ru(50 nm)/TiN(50 nm)

D. RuO_2(500 nm)/TiN(50 nm)/Ti(50 nm) + RTA

E. RuO_2(500 nm)/Ru(50 nm)/TiN(50 nm)/Ti(50 nm) + RTA

Rapid thermal annealing (RTA) in N_2 ambient is expected to improve the oxidation endurance of a TiN layer, and the Ti/Si structure can be changed into $TiSi_2$/Si by RTA. Ti is commonly used as a contact layer consuming the native oxide to form a low resistance $TiSi_2$/Si junction in metallization for LSI devices. A Ru layer between RuO_2 and TiN layers is expected to suppress TiN oxidation occurring during BST deposition.

First, *n*-type poly-Si plugs were fabricated by an etch-back technique in a thermal SiO_2 layer grown on *n*-type Si(100) (0.05 ~ 0.01 Ω·cm) wafers. The size of the contact plugs was 0.8 × 0.8 μm^2. Each layer of the RuO_2/TiN-based electrode structures was deposited by DC sputtering on substrates with poly-Si plugs. TiN thin films were sputtered using an Ar-N_2 plasma at 200°C. RuO_2 thin films were sputtered using an Ar-O_2 plasma at room temperature. In the case of electrodes B, D and E, RTA was carried

out at 700°C for 30 s in N_2 ambient between the TiN deposition and the RuO_2 deposition. In the case of electrodes D and E, the Ti layer consequently silicided during the RTA treatment. These different RuO_2/barrier structures were patterned by reactive ion etching (RIE). RuO_2 etching was carried out using an electron cyclotron generated O_2-Cl_2 plasma and a spin-on-glass hard mask [29, 33, 34]. Using different patterns, the electrode area was varied from 1.0 × 1.0 to 2.0 × 2.0 μm^2. Next, 100-nm-thick $(Ba_{0.5}Sr_{0.5})TiO_3$ films were deposited by RF magnetron sputtering at various deposition temperatures (T_d) ranging from 450°C to 600°C.

Al(700 nm)/TiN(50 nm) plate electrodes were finally deposited by DC sputtering and patterned by RIE. The plate electrode covered 2025 or 2500 small capacitors connected in parallel. *C-f* characteristics were measured in the 100 Hz to 10 MHz frequency range with a YHP (currently Keysight) 4194A impedance/gain phase analyzer, by contacting the plate electrode and the rear surface of the substrates.

In order to investigate structural changes occurring in the storage electrode during BST deposition, the flat BST/RuO_2/TiN/Si structures, corresponding to electrode A, were analyzed by Auger electron spectroscopy (AES) and X-ray diffraction (XRD). For AES depth profile measurements, Ba MNN, Sr MNN, Ti LMM, Ru MNN, O KLL and Si LVV peaks were used to calculate the atomic concentration of each element. Because N KLL peaks overlap with Ti LMM peaks, the N content was not estimated in these measurements. XRD patterns were measured by the θ-2θ scan method using the Cu $K\alpha$ radiation (50 kV, 180 mA).

C-f characteristics of the capacitors with RuO_2/TiN electrodes (A) are shown in Fig. 2-3-11. The capacitance measured for T_d = 450°C is independent of frequency. However, frequency dispersion is observed for $T_d \geq$ 500°C. Because BST thin film capacitors with a flat electrode structure do not show such dispersion, it is reasonable to consider that the

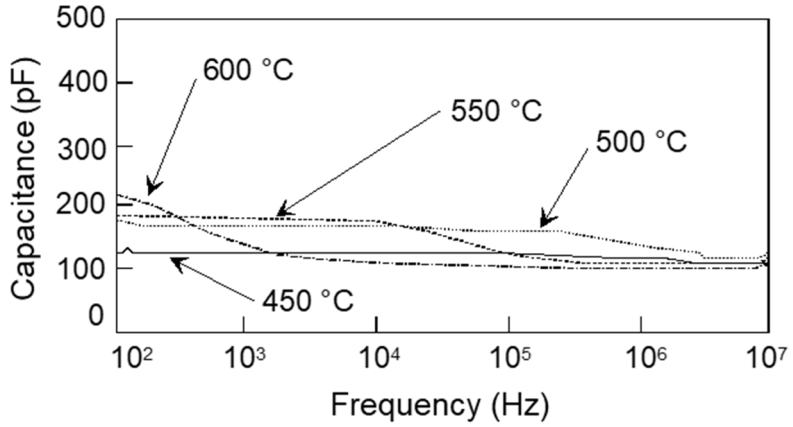

Fig. 2-3-11. BST deposition temperature dependence of *C-f* characteristics for BST capacitors with RuO_2/TiN bottom electrodes.

measured dispersion is due to C_e and R_e of the electrode structure as described above. With increasing T_d, the capacitance at lower frequency increases and the dispersion frequency decreases. The former is probably due to an increase in ε_r for the BST thin films with T_d, as is usually reported [6]. Although capacitance of the BST layer increases with increasing T_d, C_e and R_e cancel the capacitance increase in the higher frequency range.

AES depth profiles for flat BST(100 nm)/RuO_2(500 nm)/TiN(50 nm)/Si samples are shown in Fig. 2-3-12. The dashed line corresponds to the measured Sr concentration in the electrode and the Si substrate. It is not the correct Sr concentration. This is due to a background level change around the energy corresponding to the Sr MNN peak caused by the Ru NVV or Si LVV peaks. As shown in Fig. 2-3-12, the oxygen concentration and thickness of the oxidized TiN layer increase with increasing T_d. For T_d = 550°C and 600°C, RuO_2 reduction and TiO_2 formation are observed at the RuO_2/TiN interface. However, the TiN layer is not entirely oxidized even after BST deposition at 600°C. The TiN/Si interface is stable and no interdiffusion is observed up to T_d = 600°C.

Figure 2-3-13 shows the T_d dependence of XRD patterns for the same samples. No significant changes in peak intensity and width are observed for BST, RuO_2 and Si peaks

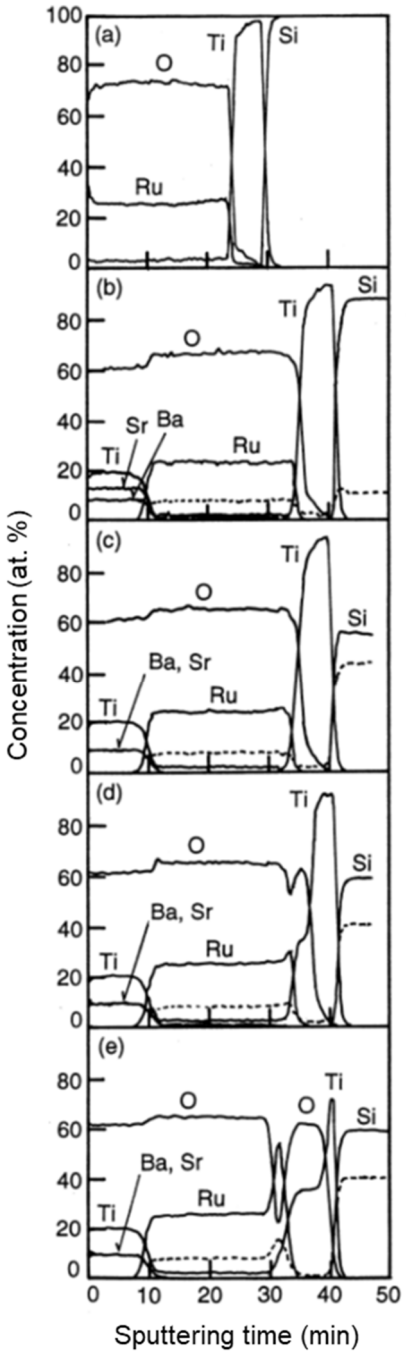

Fig. 2-3-12. AES spectra for RuO_2(500 nm)/TiN(50 nm)/Si before BST deposition (a) and after BST(100 nm) deposition at (b) 450°C, (c) 500°C, (d) 550°C, and (e) 600°C. The dashed lines show the incorrectly measured Sr concentration in the electrode and the substrate.

in the entire temperature range. Ru peaks are detected for T_d = 600°C. This suggests that the RuO_2 layer is partially reduced, which is consistent with the results of AES analysis

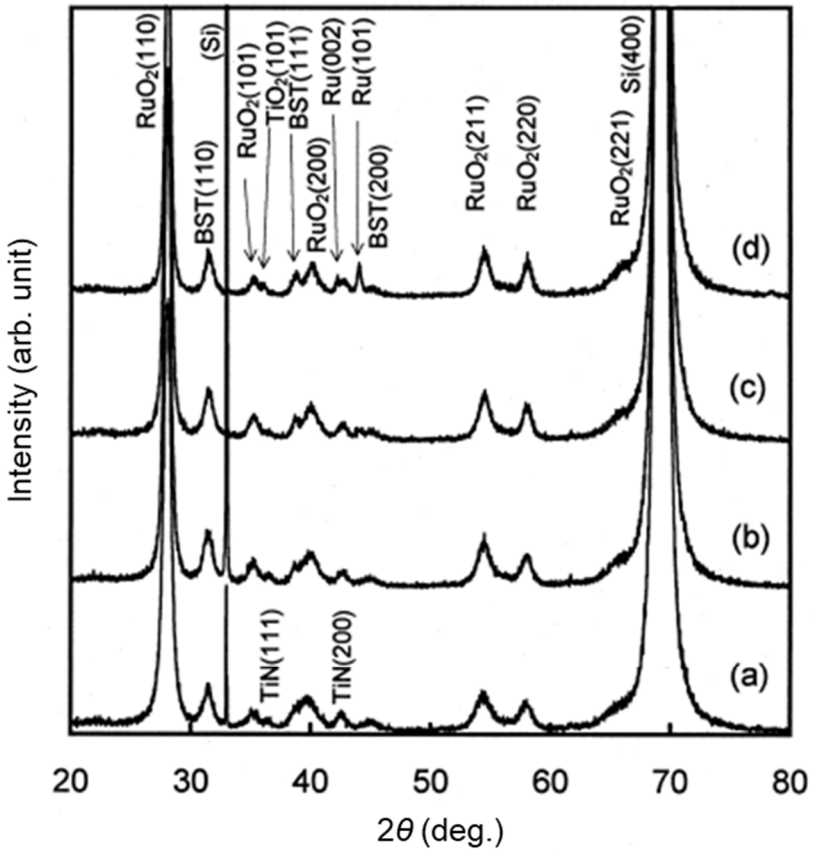

Fig. 2-3-13. BST deposition temperature dependence of XRD patterns for BST(100 nm)/RuO_2(500 nm)/TiN(50 nm)/Si. The BST deposition temperatures are (a) 450°C, (b) 500°C, (c) 550°C, and (d) 600°C.

described above.

As indicated by the results of AES analysis, TiN oxidation at the RuO_2/TiN interface progresses with increasing T_d. This oxidation of TiN explains the dispersion frequency shift observed with increasing T_d, as shown in Fig. 2-3-11. It is thought that TiN oxidation increases the resistance of the RuO_2/TiN electrode.

Figures 2-3-14 and 2-3-15 show *C-f* characteristics of the capacitors with the RuO_2(500 nm)/TiN(50 nm)/Ti(50 nm) (D) and RuO_2(500 nm)/Ru(50 nm)/TiN(50 nm)/Ti(50 nm) (E) electrodes, respectively. As described above, both structures were annealed between the TiN deposition and RuO_2 deposition, and the Ti layers consequently silicided. For example, the RuO_2/TiN/Ti electrode changed to RuO_2/TiN/$TiSi_2$ on Si plugs.

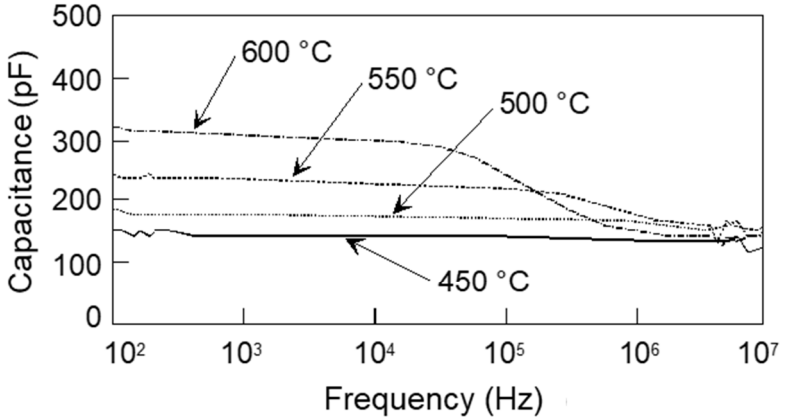

Fig. 2-3-14. BST deposition temperature dependence of *C-f* characteristics for the BST capacitors with RuO_2/TiN/Ti bottom electrodes. The RTA treatment was carried out after TiN deposition.

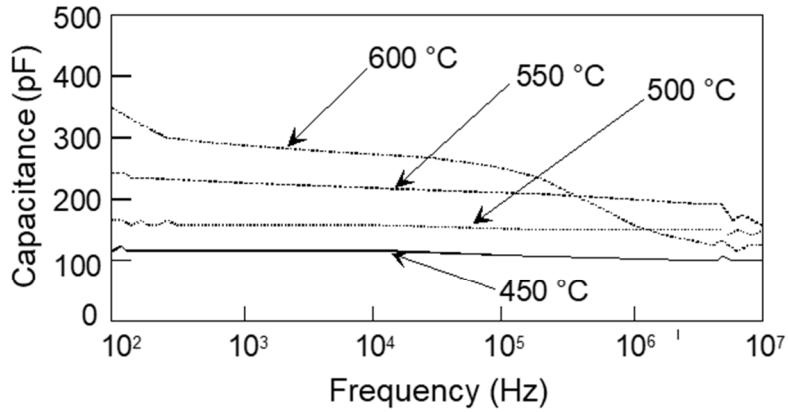

Fig. 2-3-15. BST deposition temperature dependence of *C-f* characteristics for the BST capacitors with RuO_2/Ru/TiN/Ti bottom electrodes. The RTA treatment was carried out after TiN deposition.

No capacitance dispersion is observed for $T_d \leq 500$°C in Fig. 2-3-14 and for $T_d \leq 550$°C in Fig. 2-3-15. The dispersion frequencies for $T_d \geq 550$°C in Fig. 2-3-14 and that for $T_d =$ 600°C in Fig. 2-3-15 are obviously higher than those shown in Fig. 2-3-11. This last result indicates that a higher oxidation resistance is observed for the RuO_2/TiN/$TiSi_2$ and the RuO_2/Ru/TiN/$TiSi_2$ structures than for the simple RuO_2/TiN structure.

Figure 2-3-16 shows the BST deposition temperature dependence of the R_e values

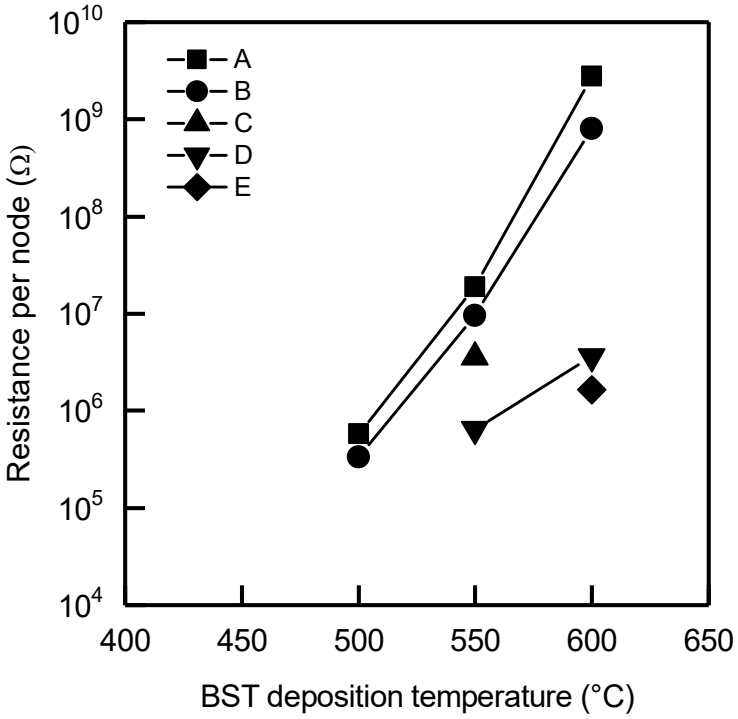

Fig. 2-3-16. BST deposition temperature dependence of the electrode resistance for various RuO_2/TiN-based electrodes used in BST thin film capacitors. The electrode structures are (A) RuO_2/TiN, (B) RuO_2/TiN + RTA, (C) RuO_2/Ru/TiN, (D) RuO_2/TiN/Ti + RTA, and (E) RuO_2/Ru/TiN/Ti + RTA.

estimated using Eqs. (2-4) ~ (2-6). R_e values less than 100 kΩ cannot be evaluated in this study because no dispersion is observed below 10 MHz with such R_e values. Comparison of A and B shows that the RTA treatment reduces R_e. Comparison of A and C shows that the Ru layer inserted between RuO_2 and TiN also reduces R_e. The effect of the Ru layer insertion on the R_e reduction is also shown in the comparison between D and E. The RTA treatment and the Ru layer insertion are thought to suppress TiN oxidation. The RTA treatment in N_2 ambient is expected to improve stoichiometry and crystallinity of a TiN layer. The Ru layer insertion is thought to act as an oxygen diffusion barrier, and it is more effective than the RTA treatment. The effects of Ti layer insertion at the TiN/Si interface and silicide formation by RTA on the reduction of R_e are clearly recognized when comparing B and D or C and E. The RTA treatment is effective in both suppressing

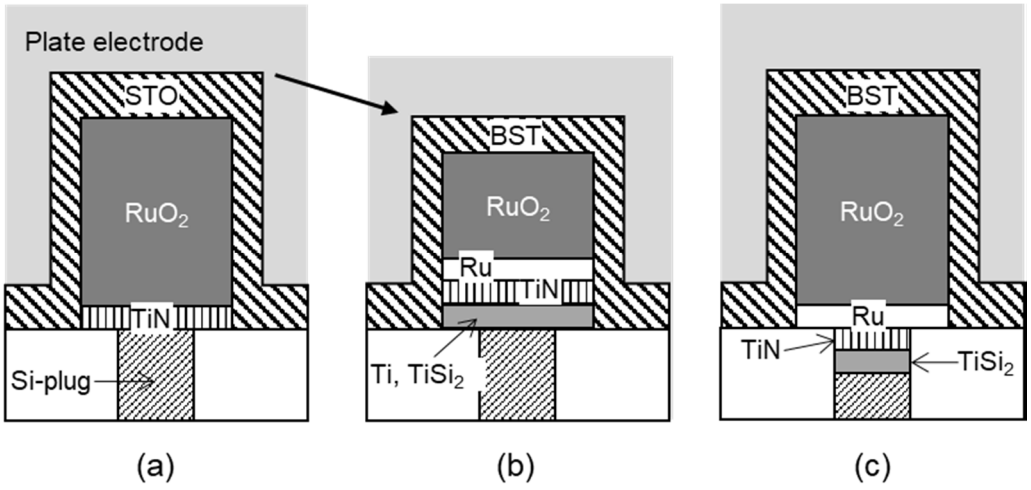

Fig. 2-3-17. Developed Gbit-scale DRAM cell capacitor structures. (a) 1G DRAM capacitor with STO (EOT = 1 nm), (b) 1G DRAM capacitor with BST (EOT = 0.65 nm), and (c) 4G DRAM capacitor with BST (EOT = 0.4 nm).

TiN oxidation and forming a low resistance TiN/$TiSi_2$/Si junction. The RuO_2/Ru/TiN/$TiSi_2$ electrode (E) is a total combination of the positive effects of the RTA treatment and the Ru and Ti layer insertion and shows the lowest R_e value among the electrodes studied.

2-3-3 Gbit DRAM cell capacitor prototypes

1G and 4G DRAM cell capacitor prototypes with RuO_2/TiN-based bottom electrodes have been developed. BST was used as a capacitor dielectric and was deposited by electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECRCVD). The ECRCVD uses oxygen radicals produced by ECR plasma to promote source gas decomposition and oxidization, so that high-quality oxide films are obtained at relatively low temperature. The developed capacitor structures are summarized in Fig. 2-3-17. Figure 2-3-17(a) shows a 1G DRAM capacitor prototype with a RuO_2/TiN bottom electrode. The dielectric layer was STO deposited at 450°C. The EOT value was approximately 1 nm [35]. An improved 1G DRAM capacitor is shown in Fig. 2-3-17(b).

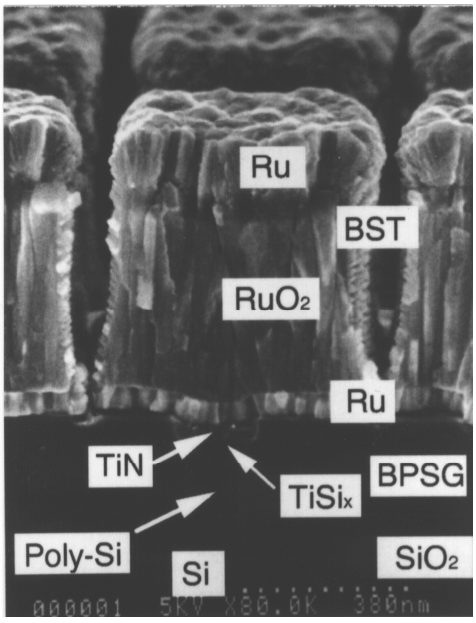

Fig. 2-3-18. SEM photograph of 4G DRAM cell capacitor prototype corresponding to Fig. 2-3-17(c).

Because heat resistance for the bottom electrode was superior to that for RuO_2/TiN, BST thin film deposited at 500°C was applicable. The EOT value was 0.65 nm [36, 37]. Further improvement of heat resistance was achieved by preventing from oxidation from the side of the electrode [38]. The BST was deposited at 550°C and the obtained EOT value was 0.4 nm, which corresponds to a 4G DRAM capacitor [39]. The photograph of the developed 4G DRAM cell capacitor prototype is shown in Fig. 2-3-18.

2-4 Conclusion

The RuO_2-based storage electrodes for Gbit-scale DRAM cell capacitors have been developed. The following results were obtained:

(1) Pt does not act as an oxygen diffusion barrier, and consequently, a low ε_r or high resistance layer is formed underneath the Pt layer. Therefore, Pt is not applicable to

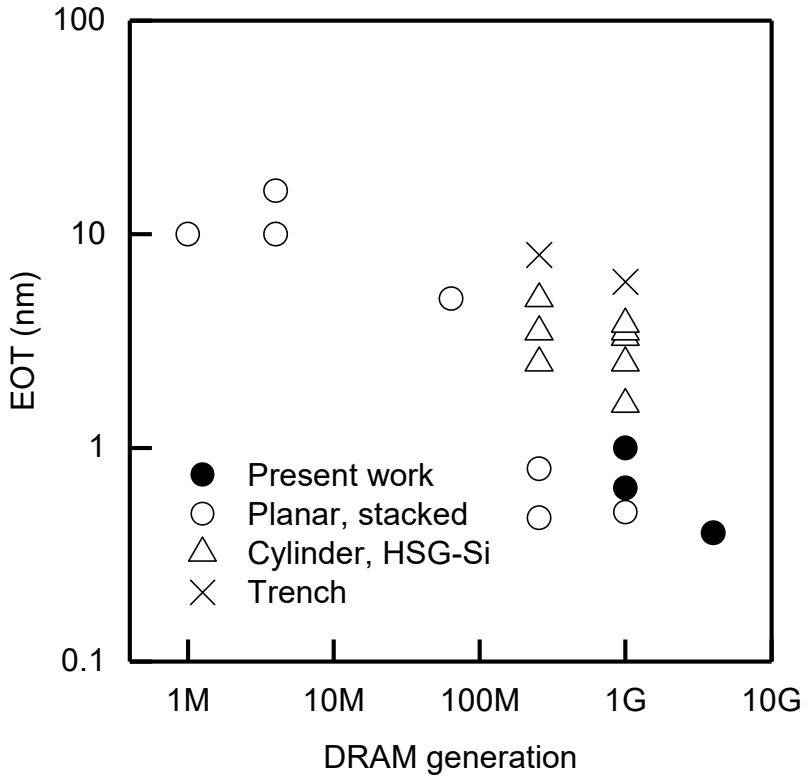

Fig. 2-4-1. Trend of the EOT values obtained by the previous and the present studies.

the storage electrode for Gbit-scale DRAMs.

(2) RuO_2 is stable for ferroelectric thin film deposition at a higher temperature, and thick RuO_2 can be patterned by dry etching to make sub-micron patterns.

(3) Resistance evaluation method for layered structures by capacitance measurement has been demonstrated and applied to the evaluation of properties for various RuO_2/TiN-based structures.

(4) Improvement of thermal stability for the RuO_2/TiN-based electrodes allows the rise of ferroelectric thin film deposition temperature to obtain higher ε_r thin films. As a result, the minimum EOT value of 0.4 nm was obtained for the capacitors with a RuO_2/Ru/TiN/$TiSi_2$ storage electrode.

Figure 2-4-1 summarizes the EOT values obtained by the previous studies and the present

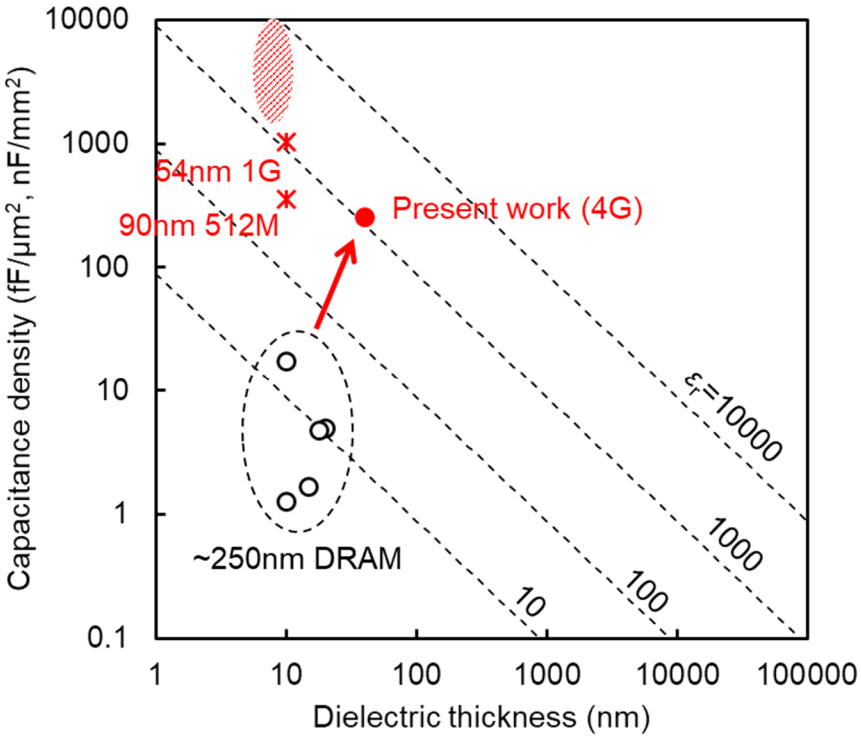

Fig. 2-4-2. Progress in increasing capacitance density by the present study and commercial DRAMs developed after this study. The capacitance density was obtained from the capacitance value per cell area.

study. The development of RuO_2/TiN-based storage electrodes has contributed to achieving 1G and 4G DRAM cell capacitors.

Figure 2-4-2 summarizes the result of this work and recent DRAM capacitors from the viewpoint of the relationship between capacitance density and dielectric thickness. Though this study succeeded in increasing the capacitance density by using high ε_r thin film capacitors, scaling of commercial DRAMs has made progress and the capacitance per cell area is larger than 1000 nF/μm^2. Currently, ferroelectric thin film capacitors are not implemented into commercial DRAMs. Other oxides, such as HfO_2, ZrO_2, and Al_2O_3, are used as the capacitor dielectrics [40]. Because the ε_r values for these oxides are much lower than that for perovskite ferroelectric oxides, the aspect ratio of the capacitor exceeds 50 to enlarge effective storage area. The current required EOT value is 0.4-0.3

nm [41], which was already obtained in this work. Therefore, implementation of perovskite oxide thin film capacitors, particularly the combination of STO and Ru or ruthenium oxide electrode, into DRAMs are drawing an attention again [42-46].

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Chapter 3
RELIABILITY OF FERROELECTRIC MATERIALS FOR NON-VOLATILE MEMORIES

3-1 Introduction

3-1-1 Ferroelectric random access memory

Non-volatile random access memory (NVRAM) is believed to be a so-called universal memory, which is combining features of main memory and storage memory. One of the candidates for the universal memory is ferroelectric random access memory (FeRAM). There are two types of the memory cell structures for the FeRAM, as shown in Fig. 3-1-1. The 1T1C-type cell is similar to the DRAM cell shown in Fig. 2-1-1. A ferroelectric capacitor is used as a storage capacitor. The 1T-type cell has a transistor with a ferroelectric gate. Because it is quite difficult to fabricate high quality ferroelectric thin films directly on Si, the 1T1C-type FeRAM has been considered to be more suitable for practical applications.

Ferroelectricity is defined by the presence of reversible spontaneous polarization (P_s). When the ferroelectric material is used as a capacitor dielectric, there are two stable macroscopic polarization states in the ferroelectric capacitor. The macroscopic polarization states can be switched to the other state by applying an electric field between the capacitor electrodes. The FeRAM utilizes these two polarization states for binary digits, as shown in Fig. 3-1-2. Because the bit line is charged with switching or non-switching current in a read operation, the remanent polarization (P_r) value has to be large to distinguish the two states. The coercive field (E_c) value has to be smaller than the

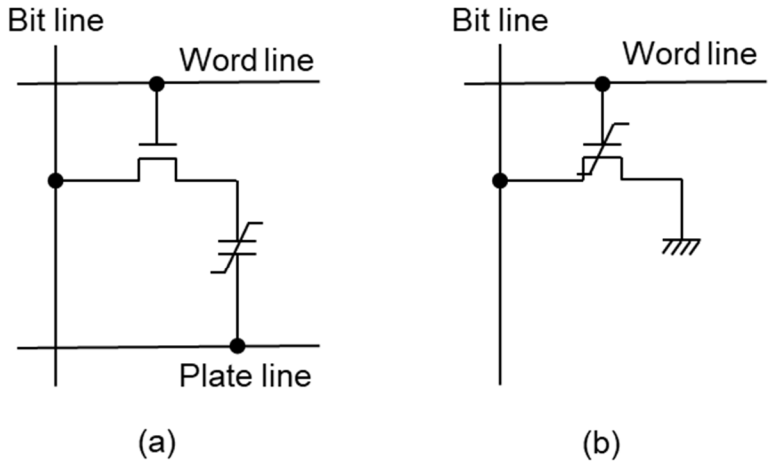

Fig. 3-1-1. Two types of FeRAM cells. (a) 1T1C-type and (b) 1T-type.

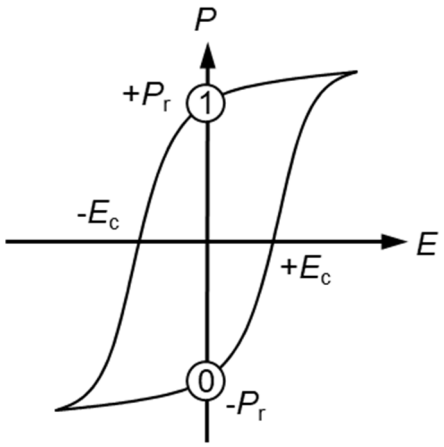

Fig. 3-1-2. Ferroelectric hysteresis loop.

applied voltage to switch polarization completely.

Ferroelectric materials lost ferroelectricity at Curie temperature (T_c) when the temperature increases. In other words, the P_s decreases with temperature and becomes 0 at T_c. The P_r value decreases more rapidly than the P_s value because of depolarization effect. This leads to instability in operation at high temperature and limits operation temperature. Fatigue is the typical degradation phenomenon in ferroelectrics. The fatigue

is a gradual decrease in polarization by switching. It limits read/write endurance. In this manner, the reliability of FeRAM operation is strongly related to nature of ferroelectric materials.

3-1-2 FeRAM capacitor materials

Lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT) are generally considered as the representative candidates for capacitor dielectrics in FeRAMs.

PZT thin films have large P_r values and are applied to commercial FeRAMs. The PZT, however, shows ferroelectric fatigue by repetition of polarization switching [1, 2]. This phenomenon limits read/write endurance for memory devices. One of the solution to overcome the problem of fatigue in perovskite films is the utilization of top and bottom conductive oxide electrodes, such as RuO_2 [3], IrO_2 [4], $SrRuO_3$ [5], and (La, Sr)CoO_3 [6, 7]. It is assumed that such oxide electrodes can act as oxygen sources and so help limit pinning of the domain walls associated with point defects. However, the mechanism responsible for the improved fatigue resistance with oxide electrodes is not fully elucidated. Because the oxide electrodes are not necessarily suitable for use in CMOS process, other solutions have been strongly desired.

The SBT thin films have drawn a great deal of attention, because of their excellent fatigue endurance and low switching voltage [8, 9]. SBT is known as a member of the bismuth-layered perovskite oxide family in oxygen-octahedral type ferroelectrics. The crystal structure for the SBT is shown in Fig. 3-1-3. Smolenskii *et al.* [11] and Subbarao [12] investigated the dielectric properties of this group. The SBT has the spontaneous polarization lying in the *a-b* plane of the orthorhombic unit cell. There are only four possible polarization states with SBT [13]. In their polycrystalline thin films, the remanent polarization is small, unless care is taken to control the crystallization

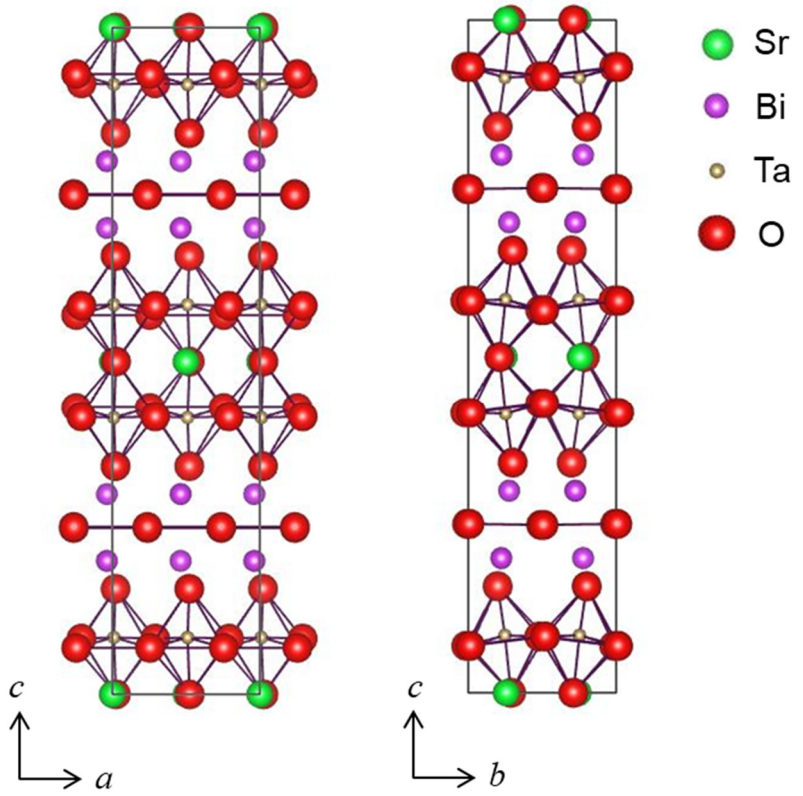

Fig. 3-1-3. Crystal structure of SBT. The drawing was produced by VESTA [10].

Table 3-1-1. Advantages and disadvantages of PZT and SBT.

Materials	Advantages	Disadvantages
PZT	Large remanent polarization Low processing temperature	Fatigue
SBT	Fatigue-free Low switching voltage	Low remanent polarization High processing temperature

orientation. The smaller P_r value is a drawback compared to PZT. Since polarization switching is utilized for read/write operation, capacitor materials are required to have stable switching characteristics over the device operating temperature range.

Advantages and disadvantages of these materials are summarized in Table 3-1-1. The drawback of the PZT thin films is ferroelectric fatigue, whereas the P_r values for the fatigue-free SBT thin films have to be improved.

3-1-3 Objectives of this chapter

As described in the previous section, both SBT and PZT have disadvantages for practical memory applications. Because the P_r values and ferroelectric fatigue are related to ferroelectricity, essential improvement by optimizing ferroelectric materials is necessary. This chapter discusses the relationship between ferroelectric degradation and material properties and demonstrates thin film capacitor improvement by materials.

3-2 Remanent Polarization Enhancement in $SrBi_2(Ta,Nb)_2O_9$ Thin Films [14, 15]

3-2-1 Off-stoichiometric $SrBi_2Ta_2O_9$ (SBT) thin films

It is well-known that electrical properties of ceramics are often affected by composition and impurities. Noguchi *et al*. [16, 17] reported on the composition dependence of the P_r and E_c values for SBT films in the temperature range from 25°C to 150°C. The P_r and E_c values decreased with increasing temperature, and the degree of the change depended on the SBT film composition. It was noteworthy that Sr-deficient and Bi-excess composition increased the P_r values, decreased their temperature dependence, as shown in Fig. 3-2-1 [17]. Figure 3-2-2 shows XRD patterns for the SBT thin films [16]. Though off-stoichiometric composition slightly improved crystallinity, preferred orientation did not depend on composition. These results suggest that Curie temperature (T_c) for these SBT films varies with the film composition. Therefore, measuring dielectric anomaly, that is, capacitance measurement at higher temperatures, in these SBT films is important as a means of understanding their ferroelectric properties. However, only a few reports on T_c for SBT have been published to date. Smolenskii *et al*. [11] and Subbarao

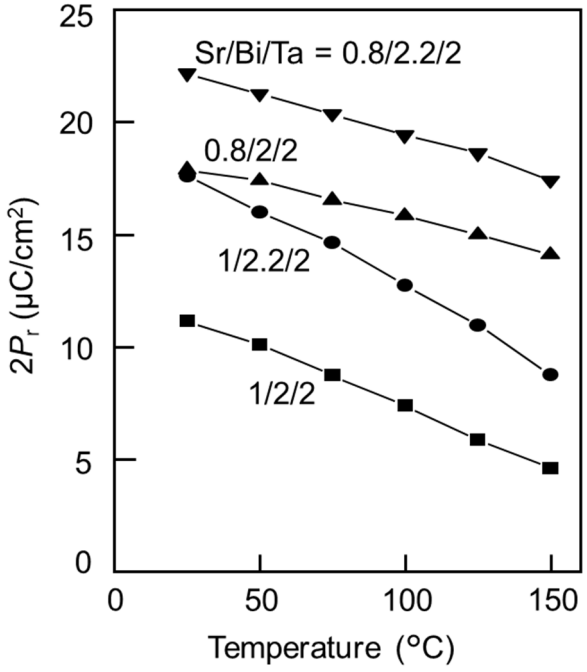

Fig. 3-2-1. Temperature dependence of remanent polarization for SBT thin films of varying composition [17].

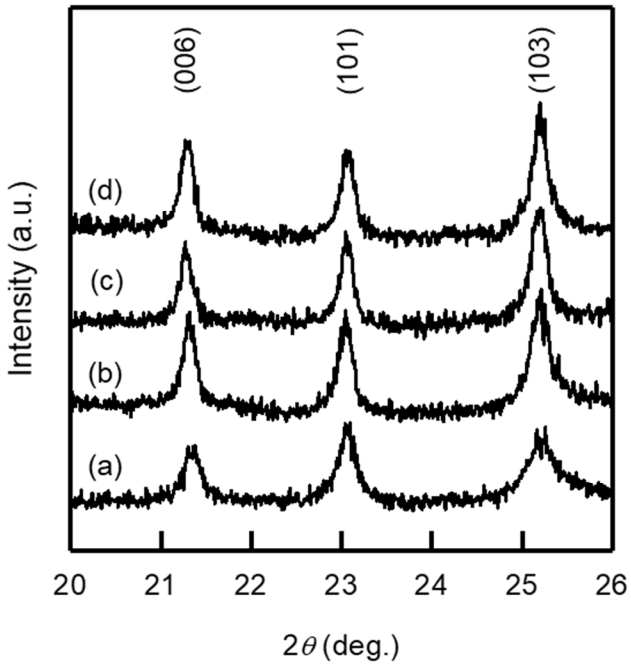

Fig. 3-2-2. XRD pattern for SBT thin films produced by MOD method. Sr/Bi/Ta = (a) 1/2/2, (b) 1/2.2/2, (c) 0.8/2/2, and (d) 0.8/2.2/2 [16].

[12] reported on the temperature dependence of dielectric constant (ε_r) for SBT ceramics, specifically that maximum ε_r was obtained at T_c values of 310°C or 335°C. Newnham *et*

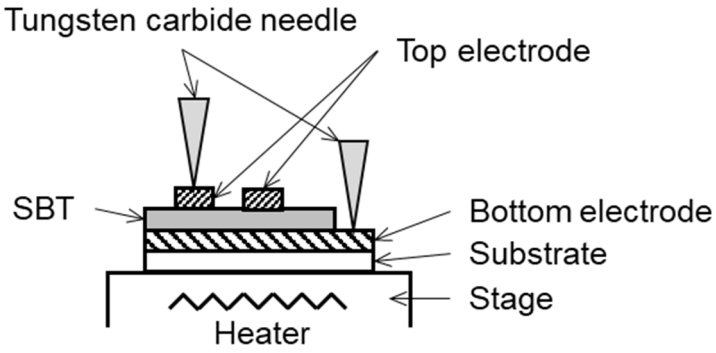

Fig. 3-2-3. Configuration of the probing system for capacitance measurement at high temperature.

al. [13] reported that the T_c value for $(Sr_{0.9}Ba_{0.1})Bi_2Ta_2O_9$ ceramic was approximately 210°C. For thin films, Taylor *et al*. [18] measured ε_r for 200 nm-thick stoichiometric SBT films and found that it increased monotonically up to 300°C. They were not able to observe any dielectric anomaly in the SBT films.

In the present experiments, SBT thin films were prepared on Pt(200 nm)/Ti(20 nm)/SiO_2/Si substrates by metal-organic decomposition (MOD) method [9, 16, 17]. Spin-coating, drying, and decomposition processes were repeated two or three times in order to obtain 200 or 300 nm-thick films, respectively. The films with stoichiometric atomic ratio (Sr/Bi/Ta = 1/2/2), Bi-excess and/or Sr-deficient composition (Sr/Bi/Ta = 1/2.2/2, 0.8/2/2, 0.8/2.2/2) were studied.

For electrical measurement, Pt top electrodes of 300 μm × 300 μm were fabricated by dc sputtering and ion-milling. After the Pt patterning, samples were annealed at 800°C for 30 min in oxygen. Capacitance and dissipation factor (tanδ) for the SBT films were measured with Hewlett-Packard (currently Keysight) 4284A precision LCR meter in an atmospheric nitrogen ambient at temperatures ranging from 20°C to 500°C. The temperature increasing rate was controlled at 5°C/min. The measurement frequency (f) ranged from 30 Hz to 1 MHz, and the oscillation voltage was 10 mV. The capacitor

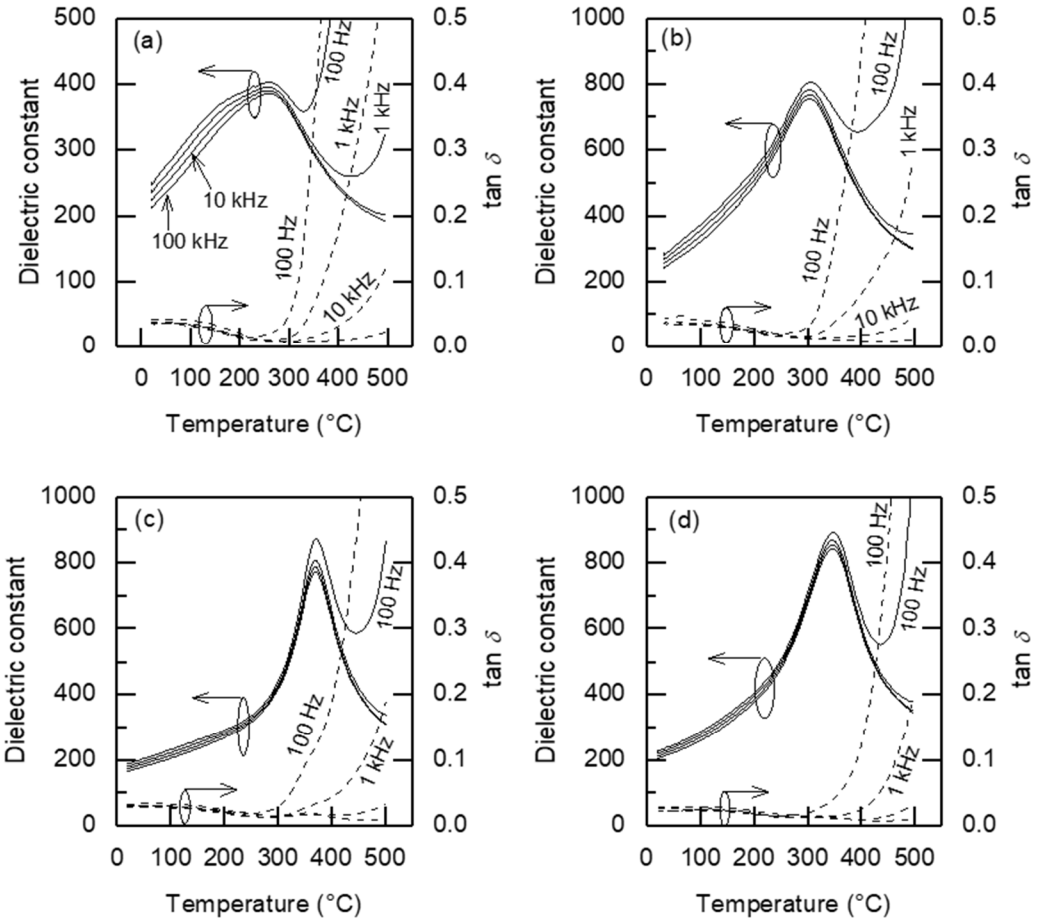

Fig. 3-2-4. Temperature dependence of ε_r and tanδ for the SBT films of varying composition. Sr/Bi/Ta = (a) 1/2/2, (b) 1/2.2/2, (c) 0.8/2/2, and (d) 0.8/2.2/2. The film thickness for (a), (b) and (c) is 200 nm, and that for (d) is 300 nm. Each figure shows that the ε_r values decrease as the measurement frequency increases.

electrodes were directly probed with tungsten carbide needles as shown in Fig. 3-2-3. The measured capacitors were not subjected to any other electrical measurements before the present capacitance measurement.

Figures 3-2-4(a) - (d) show temperature dependence of the ε_r and tanδ values for SBT films of varying composition. The results for f = 100 Hz, 1 kHz, 10 kHz and 100 kHz are indicated in each figure. The following features are observed in all SBT films; (1) The ε_r values show maxima at temperatures between 200°C and 400°C. (2) For lower

frequencies, ε_r and tanδ values abruptly increase in a high-temperature region. This increase is thought to be caused by increasing conductivity in the SBT films. (3) Below the temperatures of maximum ε_r value, the frequency dispersion of the ε_r values decreases with increasing temperature and the tanδ values also decrease. This is probably due to ferroelectric domain wall motion. Considering these results and that the SBT films examined show ferroelectricity at room temperature [16, 17], the dielectric anomaly observed in Figs. 3-2-4(a)-(d) surely corresponds to a ferroelectric-paraelectric phase transition.

The results obtained also imply composition dependence of the dielectric anomaly. The ε_r value for the stoichiometric SBT film exhibits a broad peak and a shoulder at around 170°C. This suggests that the stoichiometric SBT film consists of grains with various T_c values. The anomalies in the off-stoichiometric SBT films are stronger and the maxima for the ε_r values shift to the temperature range almost identical to or higher than that reported for the ceramics [11, 12]. From X-ray diffraction and scanning electron microscopy, the stoichiometric SBT film has less crystallinity, smaller grain size, and lower density compared to those for the Bi-excess or Sr-deficient composition [16]. Therefore, the distribution of the T_c values in the stoichiometric SBT grains is thought to be caused by defects and poor microstructure. In other words, the Sr deficiency and the excessive Bi very likely promote crystallization and grain growth in the MOD process.

Figure 3-2-5 shows the ε_r values at 10 kHz for varying SBT composition. Dielectric parameters are listed in Table 3-2-1. The T_c values were defined as the temperature at which the ε_r value is maximum. Curie-Weiss constant (C_{CW}) and Curie-Weiss temperature (θ) were evaluated assuming that ε_r obeys the Curie-Weiss law,

$$\varepsilon_r = \frac{C_{CW}}{(T-\theta)}, \tag{3-1}$$

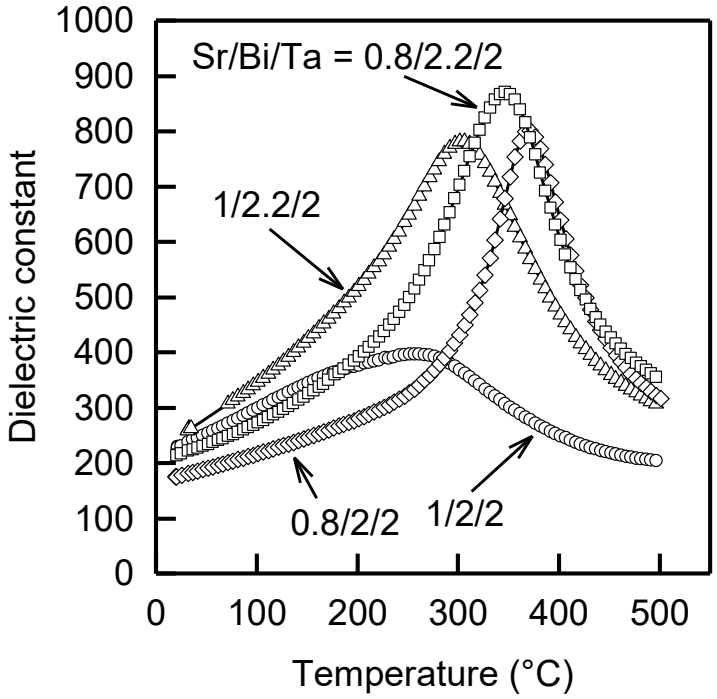

Fig. 3-2-5. Temperature dependence of ε_r at 10 kHz for the off-stoichiometric SBT films.

Table 3-2-1. Dielectric parameters for the off-stoichiometric SBT films.

Sr/Bi/Ta	ε_r (@RT)	ε_r (@Tc)	T_c (°C)	C_{CW} (10^5°C)	θ (°C)
1/2/2	228	397	257	0.72	111
1/2.2/2	259	781	302	0.81	228
0.8/2/2	175	801	371	0.58	311
0.8/8.2/2	214	871	347	0.7	286

The C_{CW} values for the SBT films are in the 10^4 K order, a typical value for displacive-type ferroelectrics. The T_c value for the stoichiometric SBT film is approximately 260°C, which is significantly lower than the T_c values reported for SBT ceramics [11, 12]. The T_c value for the Bi-excess composition (Sr/Bi/Ta = 1/2.2/2) is approximately 300°C, and those for the Sr-deficient SBT films (Sr/Bi/Ta = 0.8/2/2, 0.8/2.2/2) are higher than 340°C.

Noguchi *et al*. [17] reported that the P_r values below 150°C for the stoichiometric Sr content films (Sr/Bi/Ta = 1/2/2, 1/2.2/2) were smaller than those for the Sr-deficient SBT films (Sr/Bi/Ta = 0.8/2/2, 0.8/2.2/2), and that the P_r values for the former films decreased rapidly with increasing temperature. They also observed that the E_c values below 150°C for the stoichiometric Sr content films were smaller than those for the Sr deficient SBT films, and hypothesized that this would be due to comparatively lower T_c of the stoichiometric Sr content films and cause fast polarization relaxation or depolarization of the films [17]. The composition dependence of the T_c values obtained in the present work is consistent with these results on P_r and E_c of the films and supports this hypothesis. Therefore, the lower T_c and/or diffused dielectric anomaly in the stoichiometric Sr content SBT films increase fast relaxation or depolarization with increasing temperature and consequently aggravate the temperature dependence of P_r compared to the Sr deficient SBT films.

As described above, the T_c values of the Sr deficient SBT films, 371°C for Sr/Bi/Ta = 0.8/2.2/2 and 347°C for Sr/Bi/Ta = 0.8/2.2/2, are obviously higher than those for the ceramics. This suggests that local atomic configuration for the Sr deficient SBT films is different from the stoichiometric SBT structure such as that it shifts the T_c values higher than that for the stoichiometric crystal.

The T_c value for the stoichiometric SBT film was found to be approximately 260°C, which is lower than that for the ceramic. Bi-excess and/or Sr-deficient SBT films showed stronger dielectric anomaly at T_c values higher than 300°C. In particular, the T_c values for the Sr-deficient SBT films were higher than that for the ceramic. The Sr deficiency and excessive Bi are thought to improve crystallinity and promote grain growth in the SBT films. The composition dependence of remanent polarization and a coercive field near room temperature for the SBT films reflects the composition dependence of the T_c values.

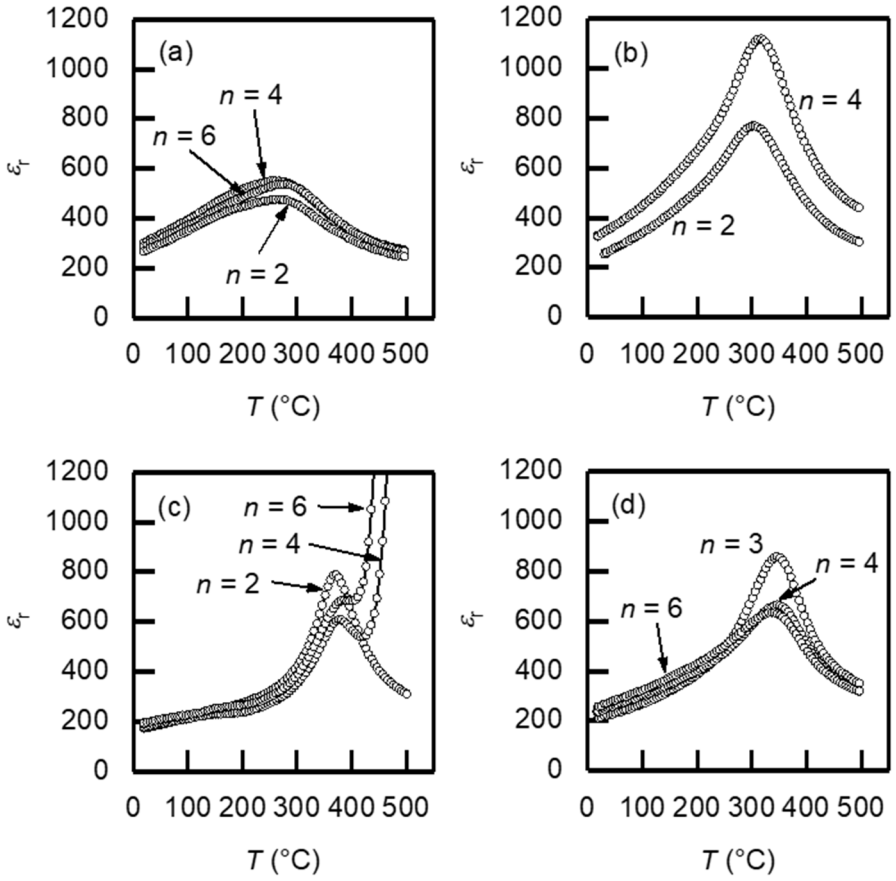

Fig. 3-2-6. Thickness dependence of dielectric anomaly in SBT thin films. Sr/Bi/Ta = (a) 1/2/2, (b) 1/2.2/2, (c) 0.8/2/2, and (d) 0.8/2.2/2.

These features of the T_c and P_r values does not depend on the SBT film thickness. Figure 3-2-6 shows the SBT film thickness dependence of the ε_r values for the SBT films as a function of temperature. The n value is the number of spin-coating (approximately 100 nm/coating). Figure 3-2-7 shows the thickness dependence of the T_c values obtained from Fig. 3-2-6. The strength of the dielectric anomaly and the T_c values are independent of the film thickness, and a diffuse anomaly was observed even for the thicker stoichiometric SBT films with n = 4 and 6.

The spontaneous polarization (P_s) values for the SBT films are shown in Fig. 3-2-8. The P_s values were extrapolated from a saturated-polarization region in a hysteresis

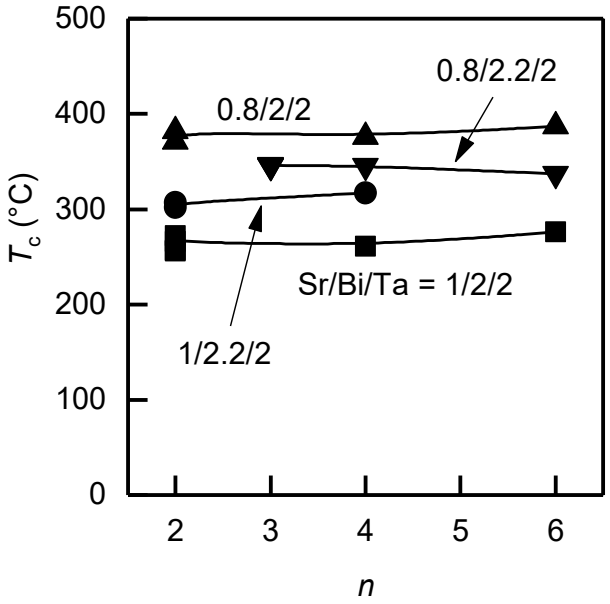

Fig. 3-2-7. Thickness dependence of the T_c values for SBT films.

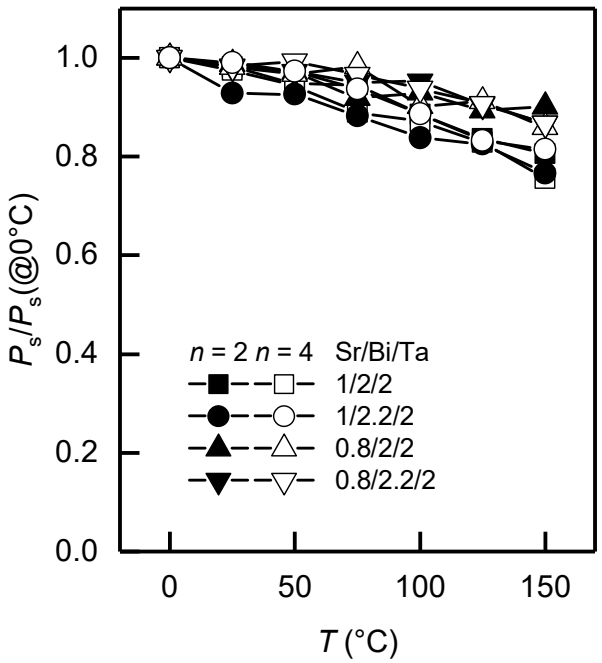

Fig. 3-2-8. Temperature dependence of the normalized P_s values for SBT films.

loop and were normalized to that at 0°C. The dependence of the normalized P_s values on temperature is also independent of the film thickness. Therefore, it is assumed that the

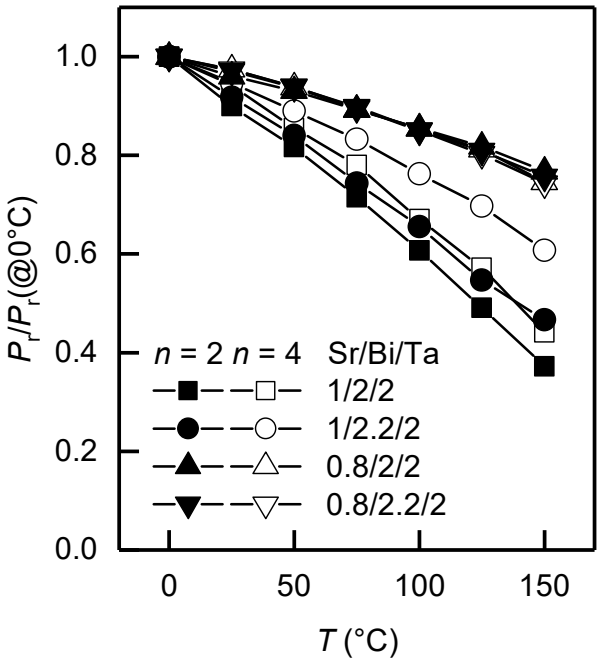

Fig. 3-2-9. Temperature dependence of the normalized P_r values for SBT films.

composition dependence of the dielectric anomaly, the T_c values, and the P_s values observed in the present experiment are governed by the nature of the crystal and that a Sr-deficient crystal has an inherently higher T_c. Shimakawa *et al*. [19] examined precise crystal structures for well-sintered stoichiometric and Sr-deficient and Bi-excess SBT ceramics and reported that the calculated polarization of $Sr_{0.8}Bi_{2.2}Ta_2O_9$ was larger than that of the stoichiometric SBT. Their result supports the findings of this study.

On the other hand, the P_r values show thickness dependence different from that for the T_c and P_s values. As shown in Fig. 3-2-9, the temperature dependence of the P_r values for the stoichiometric Sr content SBT films decreases with increasing film thickness, whereas those for the Sr-deficient films are independent of the thickness. Figures 3-2-10(a) and 3-2-10(b) show the cross-sectional transmission electron microscope (XTEM) images for the 400-nm-thick SBT films. Compared with the grain size of the 200-nm-thick films reported in Ref. [16], the grain size of the film with Sr/Bi/Ta = 1/2.2/2

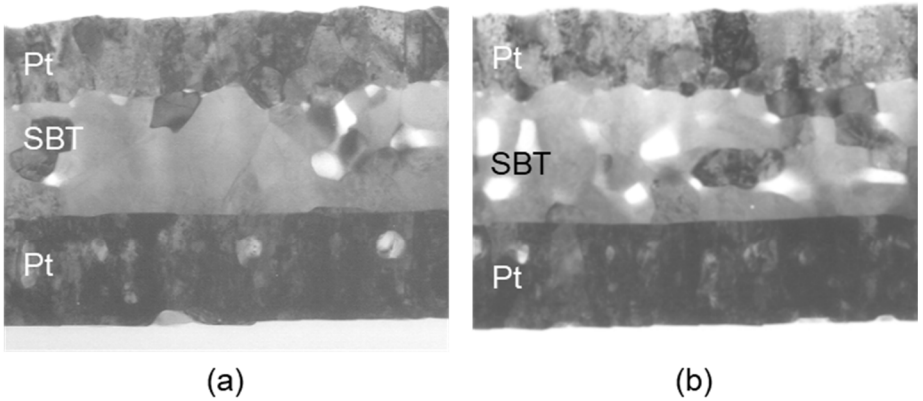

Fig. 3-2-10. XTEM images for SBT thin films with n = 4. Sr/Bi/Ta = (a) 1/2.2/2, and (b) 0.8/2.2/2.

increases with film thickness, whereas that for the Sr deficient films is independent of the thickness. The P_r is determined by the amount of polarization relaxation ($\Delta P = P_s - P_r$). Hence, the film morphology affects the relaxation, and consequently, the P_r depends on the morphology.

3-2-2 Local atomic configuration in off-stoichiometric SBT thin films

As described above, Sr-deficient SBT films have higher T_c than ceramics, and it seems to result from nature of the material. X-ray diffraction patterns for these SBT films were almost independent of the film composition as shown in Fig. 3-2-2 [16]. Short-range atomic configuration, as well as long-range order, affects dielectric properties. X-ray absorption fine structure (XAFS) spectroscopy is useful for investigating short-range pair-distribution functions in solids.

Local atomic configuration around Ta ions for 200-nm-thick SBT films was evaluated by XAFS spectroscopy. The XAFS measurement was carried out with a Si(111) double crystal monochrometer at BL-9C of the Photon Factory in the National Laboratory for High Energy Physics (KEK, Tsukuba, Japan). The Ta L_3-edge was measured at room

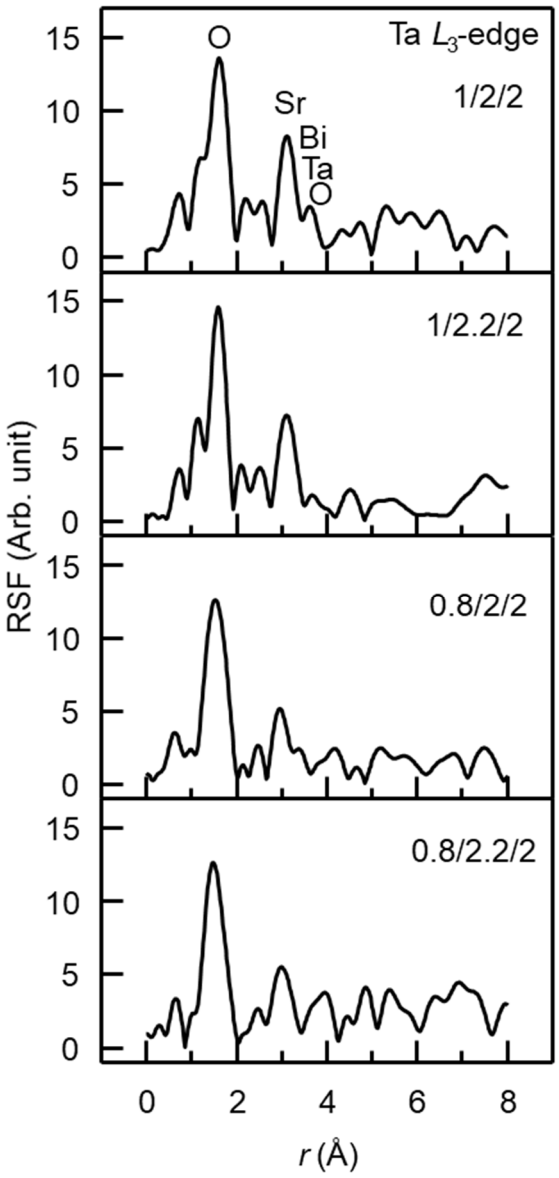

Fig. 3-2-11. RSFs for the off-stoichiometric SBT films.

temperature in the fluorescent mode using an ion chamber with nitrogen fill gas and a Lytle detector with argon fill gas. The photon energy was calibrated with a copper foil by assigning 8.9788 keV to the pre-edge peak of absorption. Details of analyzing procedures were described in Ref. [20].

Figure 3-2-11 shows the radial structure functions (RSF) around Ta atoms for the SBT films. The horizontal axis (r) corresponds to the distance from Ta. Phase shift

correlation was not taken into account in this figure. The main peaks for all curves appear between 1 and 2 Å and are related to the nearest neighbor oxygen atoms. The peaks observed between 3 and 4 Å represent metal and further oxygen neighbors. These peaks show similar features of RSF for the Aurivillius phase SBT that reported by Hartmann *et al*. [21].

The peak at approximately 3 Å corresponds to the nearest Sr. This peak for Sr-deficient SBT films is smaller than that for stoichiometric Sr content films. This means that part of the Sr-site for the Sr-deficient SBT films remains vacant. Even for the SBT thin films with Sr-deficient and Bi-excess composition (Sr/Bi/Ta = 0.8/2.2/2), excessive Bi does not completely compensate for Sr deficiency because of charge neutrality, though part of the Sr vacancies would be occupied by excess Bi. The films of Sr/Bi/Ta = 0.8/2/2 have the higher T_c than that of Sr/Bi/Ta = 0.8/2.2/2. Therefore, the Sr-deficient lattice structure is related to the rise in T_c. The main peak for the stoichiometric Sr content SBT films (Sr/Bi/Ta = 1/2/2 and 1/2.2/2) have a shoulder at approximately 1.2 Å and a sub-peak at approximately 2.2 Å. Newnham *et al*. [13] and Rae *et al*. [22] have reported asymmetry of the Ta-centered oxygen octahedron for SBT. The nearest oxygen atom is the apex oxygen of the perovskite-like layer bonding with Bi and produces the shoulder. The sub-peak appears when oxygen atoms forming the octahedron coordinate symmetrically as referred above. The shoulder and sub-peak disappear and the broader main peak is observed in the RSF for the Sr deficient SBT films. This suggests that the octahedron distortion along *c*-axis is reduced in the Sr deficient structure.

3-2-3 Effect of Nb substitution

For Bi-layered ferroelectric oxides, the niobates have a higher T_c value than the

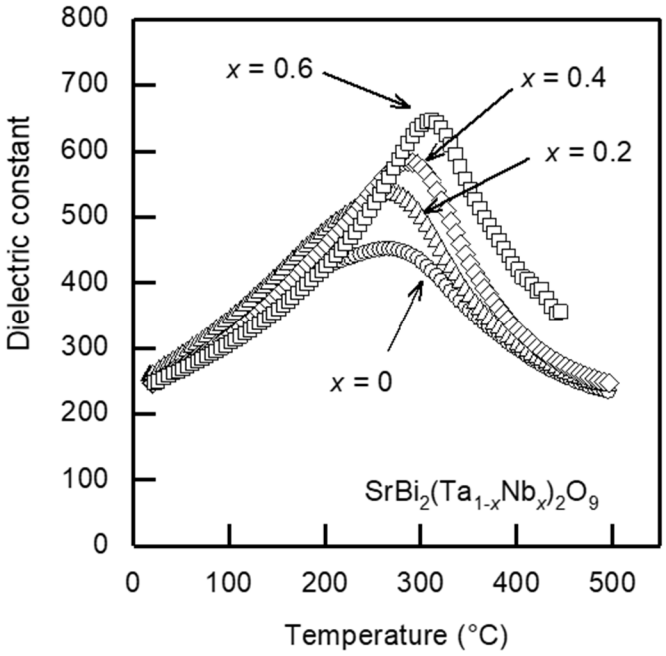

Fig. 3-2-12. Dielectric anomaly in SBTN thin films.

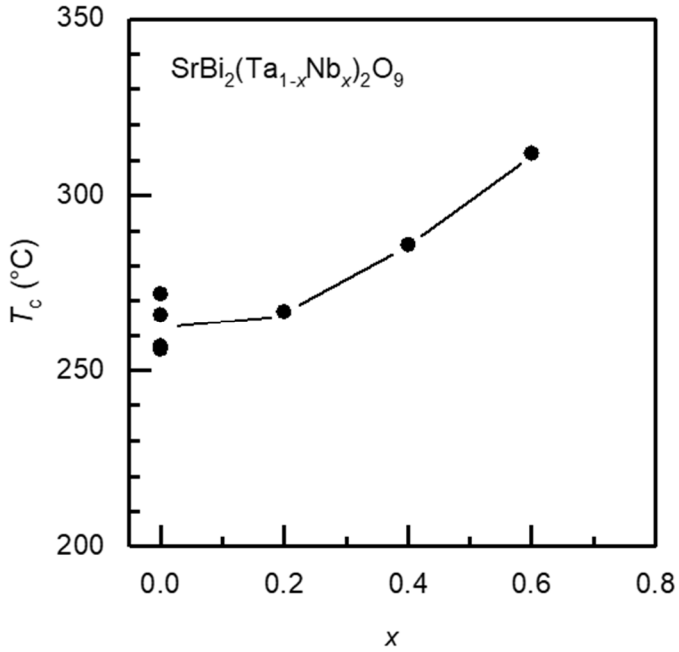

Fig. 3-2-13. Nb content dependence of T_c.

corresponding tantalates. The T_c value for $SrBi_2Nb_2O_9$ ceramics has reported 400 ~ 440°C [11, 12]. Therefore, $SrBi_2(Ta,Nb)_2O_9$ (SBTN) thin films, where Ta is partially substituted by Nb, are expected to have higher T_c values than SBT films with increasing Nb content.

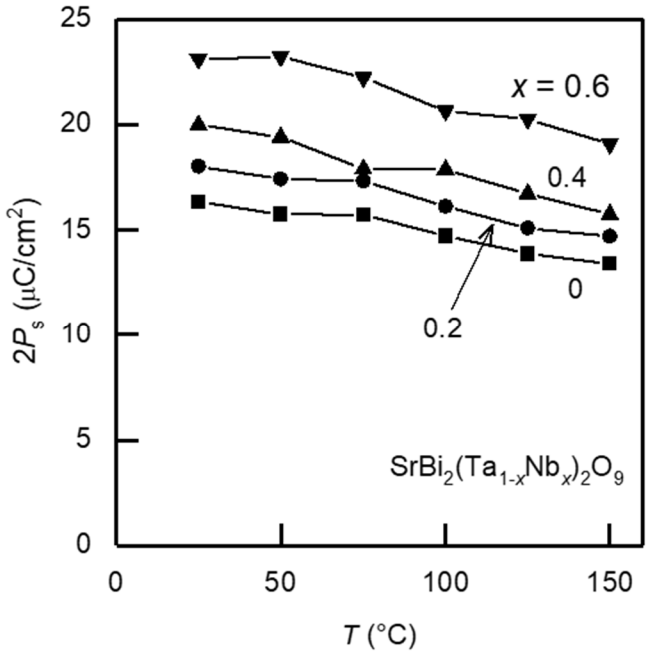

Fig. 3-2-14. Temperature dependence of P_s for the SBTN films.

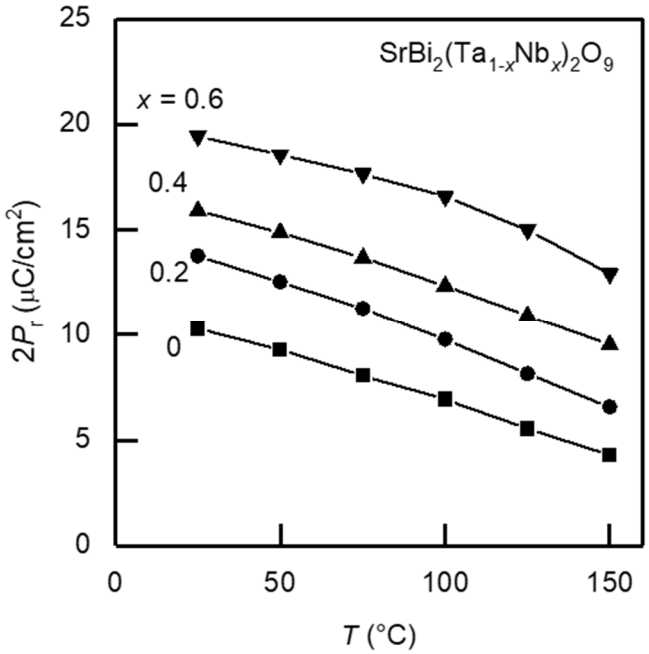

Fig. 3-2-15. Temperature dependence of P_r for the SBTN films.

The dielectric anomaly and the T_c values for the SBTN thin films are shown in Figs. 3-2-12 and 3-2-13, respectively. The film thickness was approximately 200 nm. With

increasing Nb content (x), the dielectric anomaly becomes stronger and the T_c value becomes higher. Nb substitution for Ta as well as Sr deficiency raises T_c.

The temperature dependence of the P_s and P_r values for the SBTN thin films are shown in Figs. 3-2-14 and 3-2-15. With increasing x, the P_s and P_r values increase. The results also show that higher T_c decreases ΔP, and consequently reduces the temperature dependence of P_r.

3-3 Ferroelectric Fatigue Anisotropy in $Pb(Zn_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ [23]

3-3-1 Single crystal study on fatigue of Pb-based ferroelectrics

Ferroelectric fatigue is the gradual decrease of switchable charge with polarization reversal under bipolar drive. Early studies of fatigue were mostly confined to $BaTiO_3$ single crystals, and fatigue was observed to be a general phenomenon in ferroelectrics. In general, freezing of the switchable polarization is believed to occur through the pinning of domain walls with point defects and space charge [24-31].

In ferroelectric thin film studies, fatigue, as well as imprint and retention, are widely recognized as major problems to overcome with ferroelectric non-volatile random access memories (FeRAMs). In FeRAM devices, polarization reversal is utilized for read/write operations and the two remanent polarization states correspond to “0” or “1” in the binary memory. Ferroelectric fatigue makes it difficult to distinguish between the two states and consequently limits the lifetime of the memories [32-34].

One of the solutions for the fatigue is the application of “fatigue-free” SBT. Though the previous section describes the P_r enhancement by composition control, the high crystallization temperature is still a drawback from a viewpoint of production process.

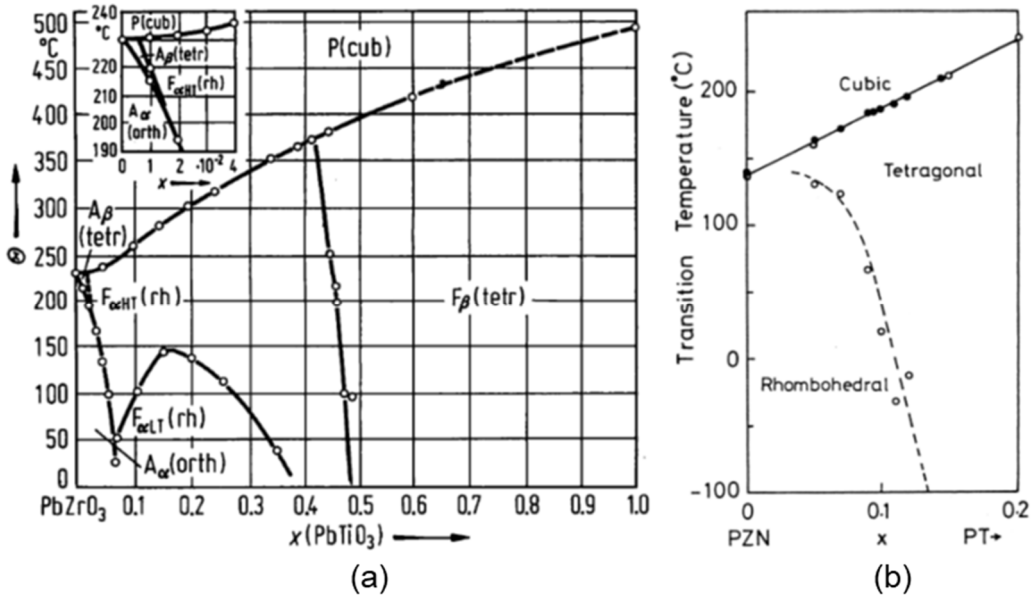

Fig. 3-3-1. Phase diagrams of (a) PZT [35] and (b) PZN-PT [36] systems.

Though degradation by Fatigue in PZT is improved by using conductive oxide electrode, the introduction of the oxide electrodes to CMOS process line is limited. Therefore, exploration of other solutions to overcome fatigue and deeper understandings of fatigue mechanisms are required. Single crystal study is expected to reveal better understandings of the material as compared to studying polycrystalline thin films. The growth of PZT single crystals, however, is difficult because of decomposition of $PbZrO_3$ at a high temperature.

The objective of this section is to revisit fatigue in Pb-based perovskite single crystals based on $Pb(Zn_{1/3}Nb_{2/3})O_3$–$PbTiO_3$, (PZN-PT) system. Because PZN-PT single crystals can be grown and their crystal structures and phase diagrams are similar to those for PZT as shown in Fig. 3-3-1, these materials are considered to be a good model for PZT crystals. In addition, these material systems have become important owing to the excellent electromechanical performance obtained with engineered domain structures [37, 38].

3-3-2 Sample preparation and measurement method

PZN-PT crystals were grown by a high-temperature flux technique [39]. The ferroelectric crystal compositions studied include 100% PZN (PZN), 95.5% PZN - 4.5% PT (PZN-4.5PT), 92% PZN - 8% PT (PZN-8 PT), and 88% PZN - 12% PT (PZN-12PT). At room temperature, PZN and PZN-4.5PT crystals are rhombohedral (pseudocubic), PZN-8PT is near the morphotropic phase boundary (MPB) (still rhombohedral), and PZT-12PT is tetragonal. For the sake of consistency, all of the orientations given throughout the remainder of the paper will be given in terms of the prototype cubic perovskite axes. This will be denoted by the subscript C when orientations are given. All the crystals were oriented within ± 2° along the $[111]_C$ or $[001]_C$ axes by the back-reflection Laue method. Plate-shaped samples were obtained by cutting off the oriented crystals, which were then polished with 3 μm alumina powder to obtain flat and parallel surfaces. 100-nm-thick Pt was sputtered as an electrode. The thickness of the samples ranged from 200 μm to 600 μm, and the electrode area ranged from 0.7 mm^2 to 7 mm^2. The samples were annealed at 250°C in air for 16 h in order to remove residual strain and defects that were introduced during crystal growth and polishing.

Polarization hysteresis loops were measured at room temperature using a modified Sawyer-Tower circuit. In particular, the electric field (E) was applied as a triangular bipolar waveform using a high voltage dc amplifier (Trek Model 609C-6 or Kepco Model BOM 1000M). The frequency of the alternating field was 10 Hz for polarization measurements as well as the switching in fatigue measurements. During measurement, the samples were immersed in Fluorinert to prevent arcing. The remanent polarization (P_r) and the coercive fields (E_c) were computed from the hysteresis loops obtained. On a limited number of samples, the strain-field hysteresis loop was monitored with a linear valuable differential transducer (LVDT) to ensure complete switching under the bipolar

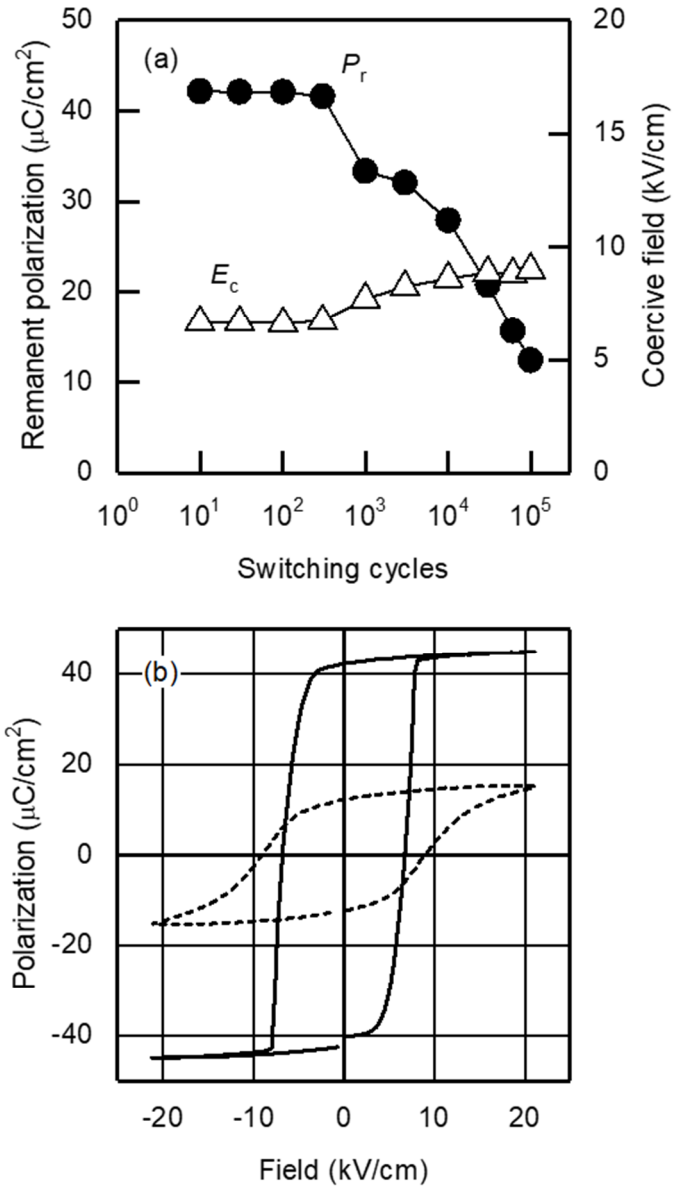

Fig. 3-3-2. Switching cycle dependence of (a) the P_r (solid circles) and the E_c (open triangles), and (b) hysteresis loops after 10 cycles (solid line) and 1×10^5 cycles (broken line) for $[111]_C$-oriented PZN-4.5PT single crystals.

drive at each driving field frequency and amplitude.

3-3-3 Composition and orientation dependence of fatigue

Figures 3-3-2 and 3-3-3 show P_r, E_c, and hysteresis loops for $[111]_C$- and $[001]_C$-oriented PZN-4.5PT crystals as a function of the number of switching cycles. The

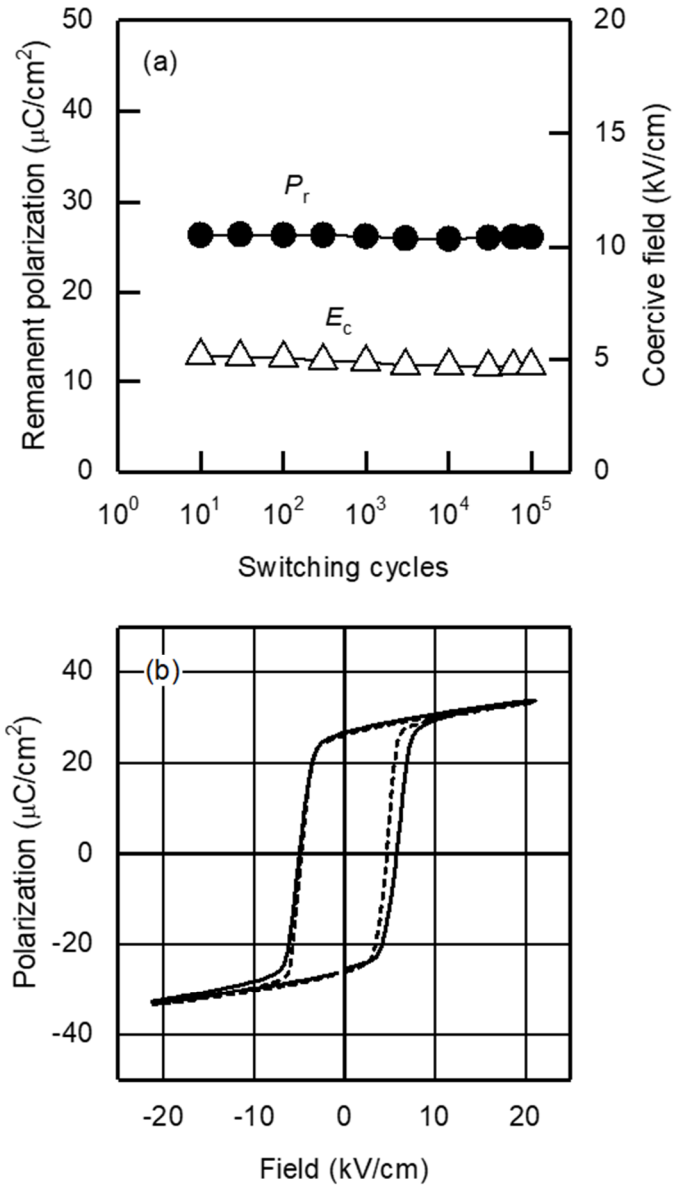

Fig. 3-3-3. Switching cycle dependence of (a) the P_r (solid circles) and the E_c (open triangles), and (b) hysteresis loops after 10 cycles (solid line) and 1×10^5 cycles (broken line) for $[001]_C$-oriented PZN-4.5PT single crystals.

amplitude of the alternating triangular electric field (E_{max}) was 20 kV/cm, and the frequency of the field was 10 Hz. The initial P_r value for the $[001]_C$-oriented crystal ($P_{r,[001]}$) is approximately equal to $1/\sqrt{3}$ of $P_{r,[111]}$. In $[111]_C$-oriented crystals, the

remanent polarization during cycling is along $[111]_C$ for E // [111], or $[\bar{1}\bar{1}\bar{1}]_C$ for E // $[\bar{1}\bar{1}\bar{1}]_C$. Thus, the domains switch between [111] and $[\bar{1}\bar{1}\bar{1}]$ states. In $[001]_C$-oriented crystals, the spontaneous polarization lies along one of four possible polar directions, for example $[111]_C$, $[\bar{1}\bar{1}\bar{1}]_C$, $[1\bar{1}\bar{1}]_C$, or $[\bar{1}\bar{1}\bar{1}]_C$ for E // [001]. With a reverse electric field, then these domains switch to $[\bar{1}\bar{1}\bar{1}]_C$, $[1\bar{1}\bar{1}]_C$, $[\bar{1}1\bar{1}]_C$, or $[11\bar{1}]_C$, and this can be done via 180°, 71°, or 109° switching processes, assuming rhombohedral symmetry.

As shown in Fig. 3-3-2, the P_r values for $[111]_C$-oriented crystals are almost constant up to 10^3 cycles and then decreases rapidly with further switching cycles. $[111]_C$-oriented crystals obviously fatigue. The E_c values increase after the onset of fatigue. In contrast, the P_r and E_c values for $[001]_C$-oriented crystals are almost constant up to 10^5 switching cycles as shown in Fig. 3-3-3(a). The shape of the hysteresis loop does not change even after 10^5 cycles as shown in Fig. 3-3-3(b). The E_c value slightly decreases with switching cycles. As will be discussed below, this decrease in E_c as a function of cycling was observed for $[001]_C$-oriented crystals measured with a wide variation in field amplitudes. It suggests that some domain walls are weakly pinned in the initial state, causing some resistance to switching, but during cycling, these domain walls are detached from the original pinning sites. Possible origins for the pinning include impurities, oxygen or lead vacancies, or damage produced during crystal growth, polishing, or electroding.

The same orientation dependence of fatigue is also observed in pure PZN single crystals, as shown in Figs. 3-3-4 and 3-3-5. Fatigue in rhombohedral PZN(-PT) single crystals, therefore, is not dominated by the nature of the ferroelectricity, that is to say, relaxor or normal behavior [40, 41].

Unlike the rhombohedral phase, fatigue is observed in $[001]_C$-oriented PZN-12 PT tetragonal crystals as shown in Fig. 3-3-6. In tetragonal PZN-12 PT, the polar direction is along $[001]_C$. Thus, domain switching involves polarization directions normal to the

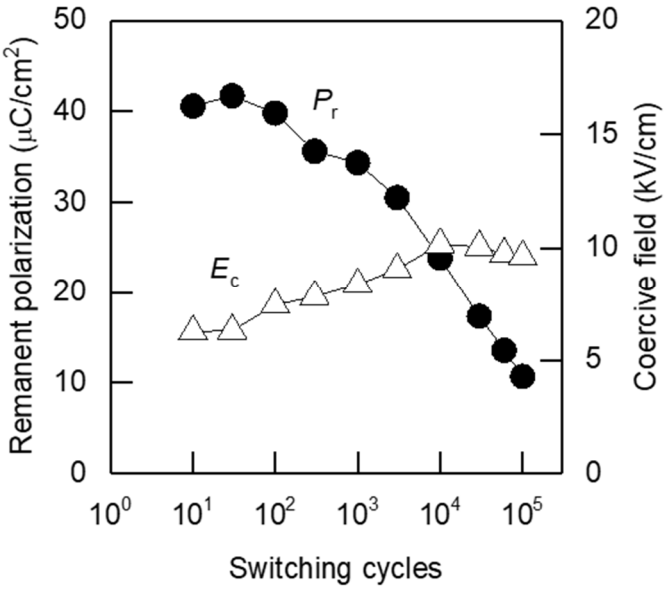

Fig. 3-3-4. Switching cycle dependence of the P_r (solid circles) and the E_c (open triangles) for $[111]_C$-oriented PZN single crystals.

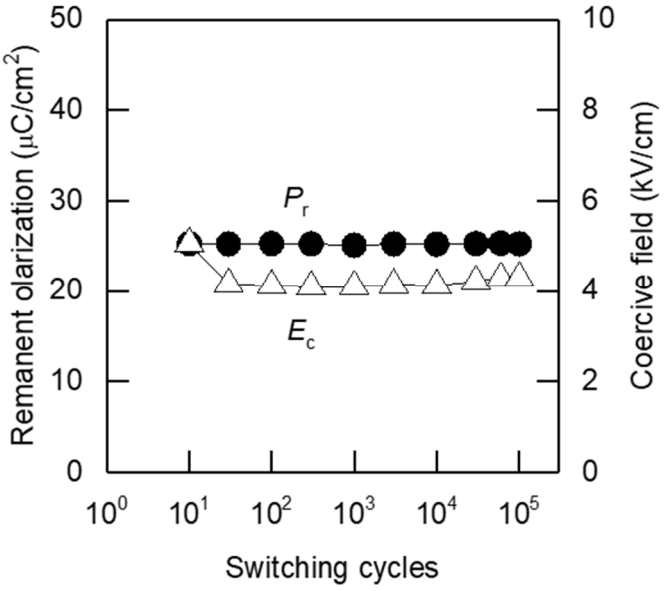

Fig. 3-3-5. Switching cycle dependence of the P_r (solid circles) and the E_c (open triangles) for $[001]_C$-oriented PZN single crystals.

electrode-crystal interface and presumably is accomplished predominantly through 180° domain wall motion. The origin of fatigue in tetragonal PZN-PT crystals is believed to be similar to that found in tetragonal $BaTiO_3$ single crystals.

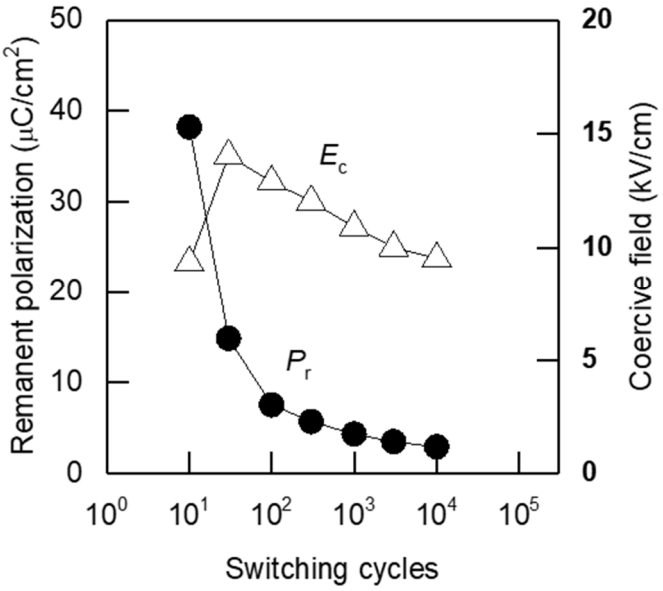

Fig. 3-3-6. Switching cycle dependence of the P_r (solid circles) and the E_c (open triangles) for $[001]_C$-oriented PZN-12PT single crystals.

The switching behavior of P_r and Ec in a $[001]_C$-oriented PZN-8 PT crystal (near the MPB composition) is shown in Fig. 3-3-7(a). Whereas the P_r values are almost constant up to 10^5 cycles, the hysteresis loop changes as shown in Fig. 3-3-7(b). There is some indication of the development of a pinning phenomenon, as is evidenced by the narrowing of the waist of the hysteresis loop.

The above results indicate again that rate of fatigue is strongly dependent on both the ferroelectric phase and the crystal orientation in relaxor-PT single crystals. The $[001]_C$-oriented rhombohedral phase showing no notable fatigue up to 10^5 cycles for the slow alternating field required to switch the polarization in the crystal capacitors.

3-3-4 Switching condition dependence of fatigue

In ferroelectric thin films, the magnitude of the applied fields can influence the fatigue rates [42, 43]. Figure 3-3-8 shows that the $[111]_C$-oriented PZN-4.5 PT single crystals fatigue for a wider range of E_{max} values. $[001]_C$-oriented PZN-4.5PT crystals, in

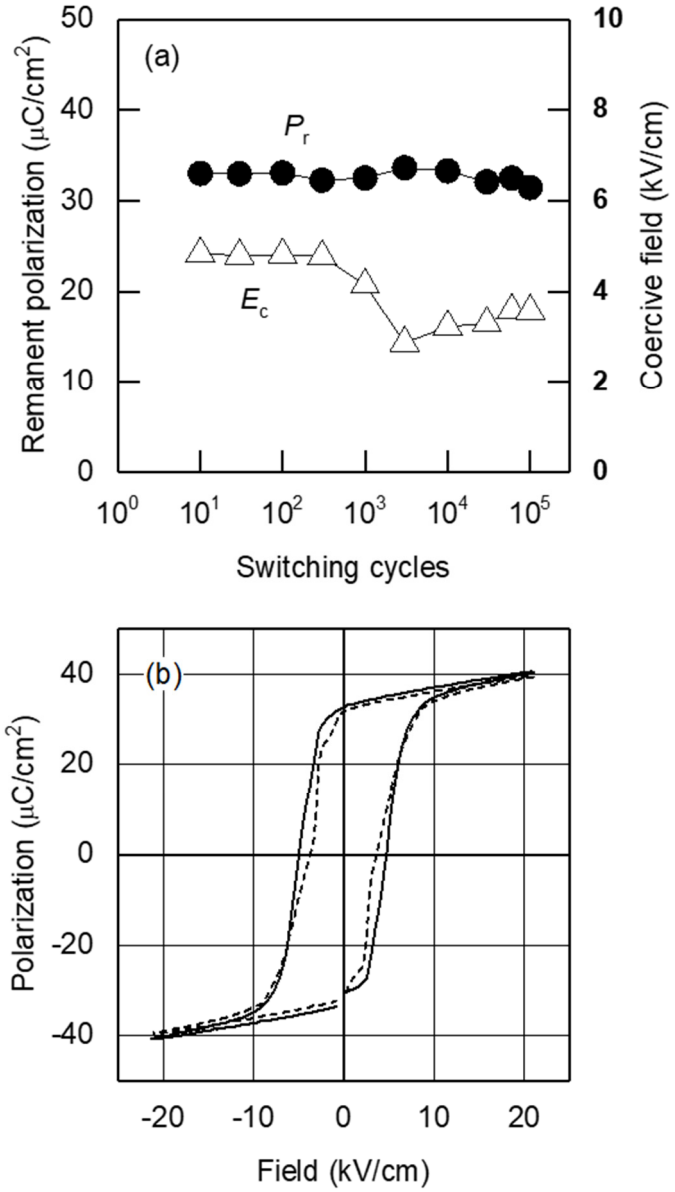

Fig. 3-3-7. Switching cycle dependence of (a) the P_r (solid circles) and the E_c (open triangles), and (b) hysteresis loops after 10 cycles (solid line) and 1×10^5 cycles (broken line) for $[001]_C$-oriented PZN-8PT single crystals.

contrast, do not fatigue under various E_{max} levels, as shown in Fig. 3-3-9. It is inferred that the crystal orientation, rather than E_{max}, governs the fatigue resistance for these PZN-PT crystals. Figures 3-3-10 and 3-3-11 show the switching cycle dependence of P_r and E_c values for $[111]_C$- and $[001]_C$-oriented PZN-4.5PT single crystals measured at various switching frequencies between 0.1 Hz and 10 Hz. In the present study, fatigue lifetime

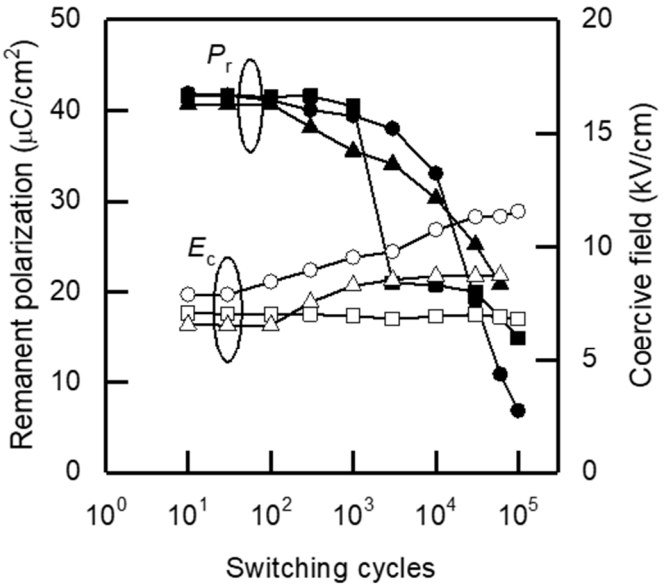

Fig. 3-3-8. Switching cycle dependence of P_r (solid symbols) and E_c (open symbols) for $[111]_C$-oriented PZN-4.5PT single crystals under various switching field strengths (■, □; 10 kV/cm, ●, ○; 20 kV/cm, ▲, △; 30 kV/cm).

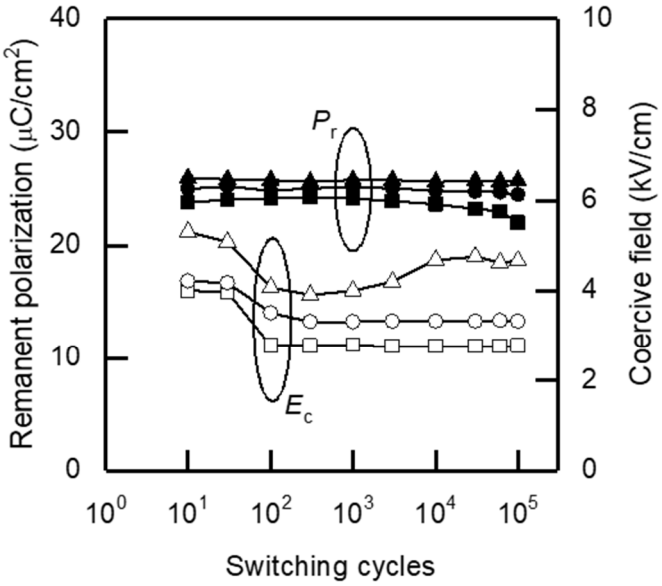

Fig. 3-3-9. Switching cycle dependence of P_r (solid symbols) and E_c (open symbols) for $[001]_C$-oriented PZN-4.5PT single crystals under various switching field strengths (■, □; 5 kV/cm, ●, ○; 10 kV/cm, ▲, △; 20 kV/cm).

does not depend on the switching frequency for $[111]_C$-oriented crystals.

It has been shown previously that large strain changes of 0.1% accompany polarization reversal in $[111]_C$-oriented crystals [37]. Strain sometimes results in

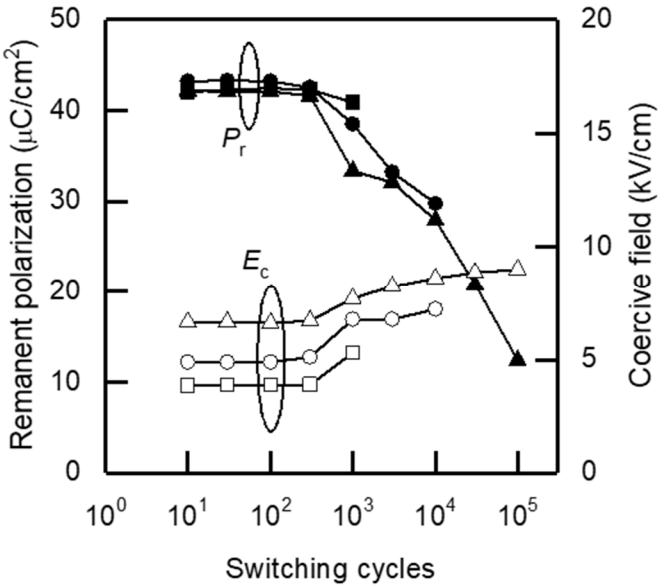

Fig. 3-3-10. Switching cycle dependence of P_r (solid symbols) and E_c (open symbols) for $[111]_C$-oriented PZN-4.5PT single crystals under various switching frequencies (■, □; 0.1 Hz, ●, ○; 1 Hz, ▲, △; 10 Hz).

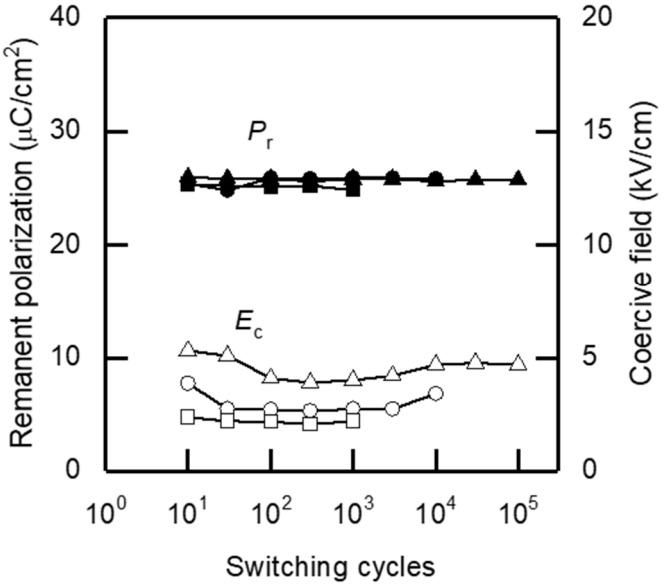

Fig. 3-3-11. Switching cycle dependence of P_r (solid symbols) and E_c (open symbols) for $[001]_C$-oriented PZN-4.5PT single crystals under various switching field strengths (■, □; 0.1 Hz, ●, ○; 1 Hz, ▲, △; 10 Hz).

microcracking, and microcracks have often been associated with fatigue in bulk ceramics [44]. Figure 3-3-12 shows that annealing improves the P_r value of a fatigued $[111]_C$-oriented PZN-4.5PT crystal. When a fatigued crystal was annealed at 450°C for 16 h in

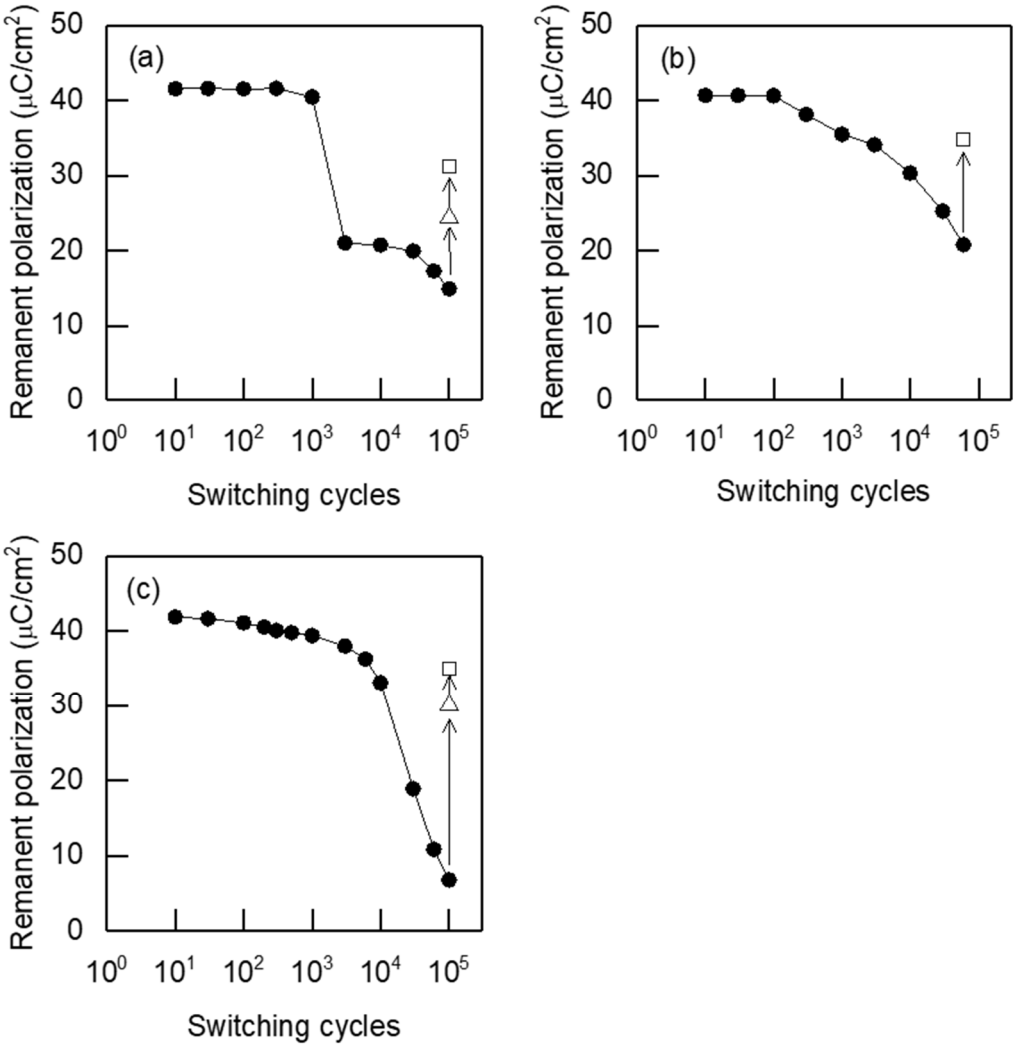

Fig. 3-3-12. Recovery of the P_r for $[111]_C$-oriented PZN-4.5PT single crystals fatigued under different E_{max} conditions; (a) 10 kV/cm, (b) 20 kV/cm, and (c) 30 kV/cm. After fatigue, the crystal was annealed at 250°C (△), and then 450°C (□) for 16 h in air.

air, P_r increased to more than 80% of the initial P_r value. This result proves that the fatigue observed in the present study is recoverable, and rules out fatigue by microcracking. Therefore, fatigue in the $[111]_C$-oriented PZN-4.5PT single crystals is believed to result from domain wall pinning via defects during polarization reversal, as has been reported in earlier single crystal studies.

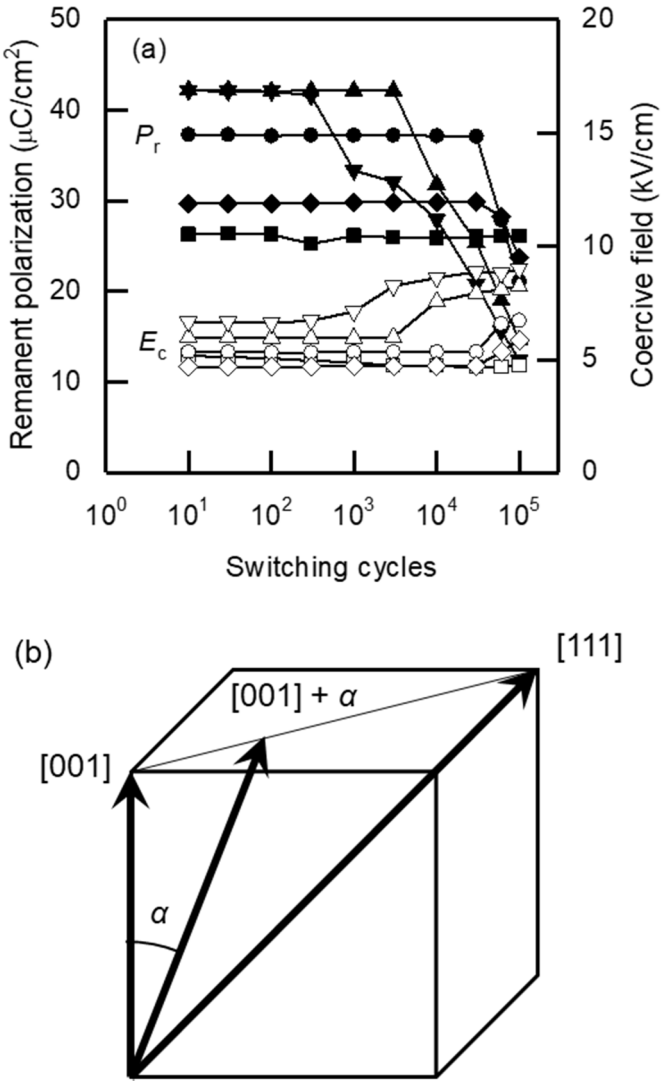

Fig. 3-3-13. (a) Effect of deviation from $[001]_C$ direction on fatigue for PZN-4.5PT single crystals. (b) The direction angle from $[001]_C$ toward $[111]_C$ (α) is defined. Solid markers show P_r, and open markers show E_c (■, □; $\alpha = 0°$ [001], ◆, ◇; $\alpha = 15°$, ●, ○; $\alpha = 30°$, ▲, △; $\alpha = 45°$, ▼, ▽; $\alpha = 54.7°$ [111]).

3-3-5 Optimum orientation of crystals

Figure 3-3-13(a) shows the fatigue behavior for PZN-4.5PT single crystals oriented along $[001]_C + \alpha$, where α is the degree of deviation from $[001]_C$ ($\alpha = 0°$) toward $[111]_C$ ($\alpha = 54.7°$), as shown in Fig. 3-3-13(b). The initial P_r and E_c values increase with α, and the initial P_r magnitude is consistent with a projection of the $P_{r,[111]}$, *i.e.* $P_{r,[111]}\cos(54.7°$

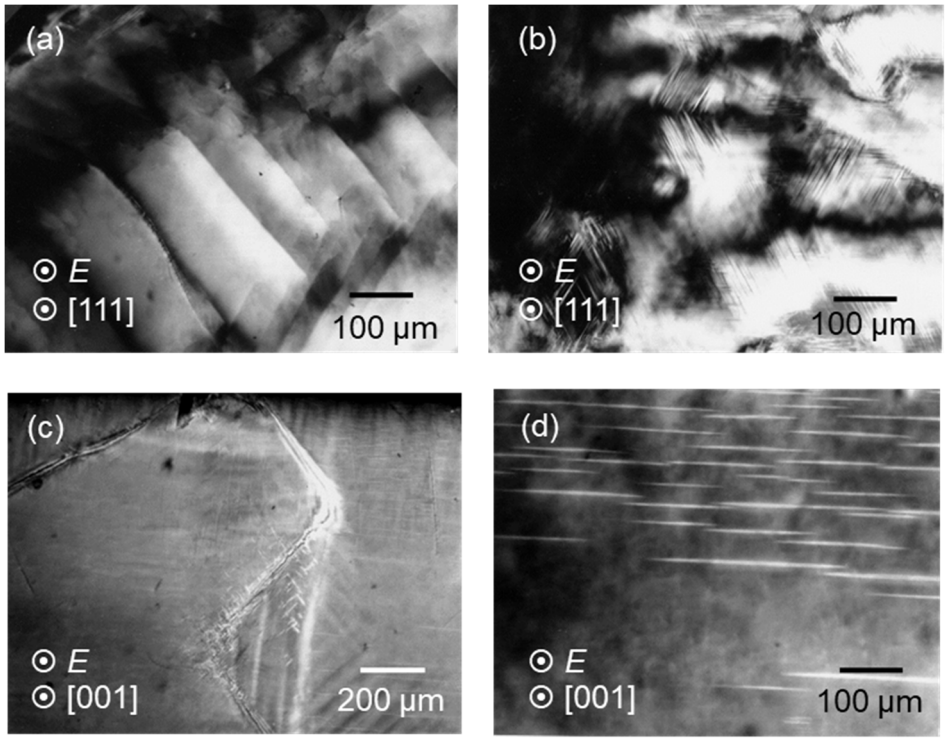

Fig. 3-3-14. Optical micrographs for $[111]_C$-oriented PZN-4.5PT single crystals (a) before cycling and (b) after 1×10^5 cycles, and $[001]_C$-oriented crystals (c) before cycling and (d) after 1×10^5 cycles.

– α). The fatigue rate is enhanced when crystals are oriented with $\alpha \geq 15°$. The induction period before fatigue onset gradually decreases with increasing α. Fatigue in the rhombohedral PZN-PT single crystals is systematically dependent on crystallographic orientation, with $[001]_C$-oriented rhombohedral ferroelectric single crystals believed to have the lowest fatigue rate.

3-3-6 Domain structure in field cycled PZN-PT crystals

Optical microscopy has shown in the $[111]_C$-oriented PZN-4.5PT crystal the domain density increases with cycling and fatigue, whereas in the $[001]_C$-oriented PZN-4.5PT crystal, the density of domain walls decreases, as shown in Fig. 3-3-14. In the case of $[111]_C$-oriented crystals, it is anticipated that as domain walls are pinned by the fatigue process, new domains are activated from pre-existing nuclei, initially enabling the

maximum polarization to be reversed for each cycle. As cycling continues the process of pinning, activation of new domains, and then ultimately freezing, the result is a high density of frozen-in domain walls in fatigued crystals. Switching analysis of $[111]_C$- and $[001]_C$-oriented PZN-PT crystals has shown that the mobility of domain walls in $[001]_C$ cuts is much higher [45]. This results in the ferroelectric being able to lower its total energy by systematically having the fastest domain walls control the switching and the domains can grow to define the largest volumes in the crystal and reduce the total domain wall density. This is consistent with observations made with optical microscopy, where only a few domains are observed in $[001]_C$-oriented crystals driven under bipolar fields to 10^3 to 10^5 cycles. Clearly, more work needs to be conducted to establish the orientation and nature (*i.e.* charged or uncharged) of the residual domain walls in both fatigued and unfatigued crystals of both orientations. Higher resolution techniques which can verify the local domain structures will also be necessary.

Fatigue in PZN-PT single crystals was studied at room temperature for a variety of crystallographic orientations, electric field strengths, frequencies, and compositions. It is observed that the rhombohedral PZN-PT crystals oriented with the field along $[001]_C$ have no fatigue. At room temperature, $[111]_C$-oriented rhombohedral PZN-PT fatigues as does tetragonal PZN-PT in $[001]_C$ and $[111]_C$ directions. Close to the morphotropic phase boundary the presence of tetragonal phase will dominant and complex the fatigue process.

The fatigue-free nature of the rhombohedral phase in the $[001]_C$ orientation is suggested to be related to the engineered domain configuration, and to the observation that the $[001]_C$ direction has a high domain mobility. Following these studies, epitaxial ferroelectric thin films of $Pb(Yb_{1/2}Nb_{1/2})O_3$–$PbTiO_3$ (PYbN-PT) have been fabricated and tested to verify fatigue at higher switching frequencies and thinner crystals. As shown in Fig. 3-3-15, the results are consistent with the fundamental observations made here [46].

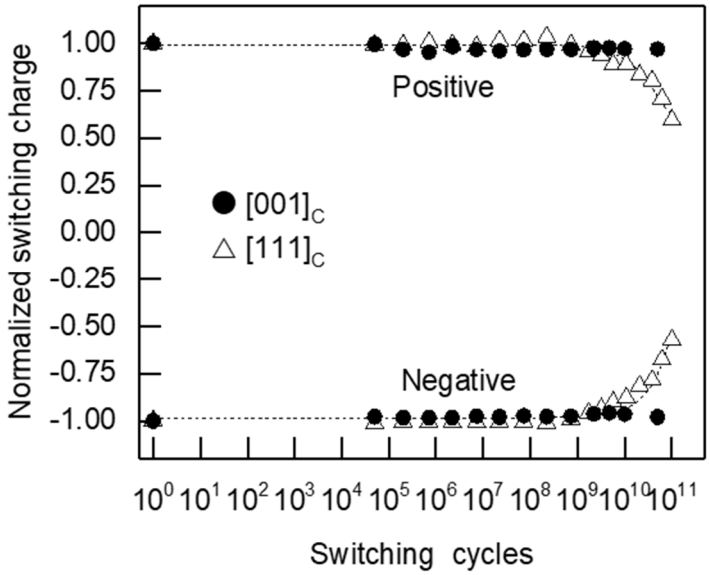

Fig. 3-3-15. Anisotropic fatigue characteristics for heteroepitaxial PYbN-PT thin films [46].

3-4 Conclusion

Reliability of FeRAM operation reflects stability in ferroelectricity which is associated with ferroelectric crystal properties. In this chapter, improvement of reliability for ferroelectric thin film capacitors has been studied from the viewpoint of ferroelectricity.

Though small P_r value of stoichiometric SBT thin films was a disadvantage for the memory applications, off-stoichiometric Sr-deficient and Bi-excess composition increased the P_r value. The T_c values for the Sr-deficient SBT films were higher than those of stoichiometric SBT films and ceramics, which results in suppressing temperature dependence of the P_r. Nb substitution for Ta also increased the T_c and the P_r values. It is assumed that these stoichiometry control inherently changes ferroelectricity in the

crystals. The Sr-deficient and Bi-excess composition and the Nb substitution have been exploited for FeRAM development [47-50].

A gradual decrease in switchable polarization called fatigue is a major issue for PZT thin film capacitor with commonly-used Pt electrodes. Fatigue anisotropy was discovered in this study. Fatigue behavior for PZN-PT single crystals obviously depends on crystal orientation. $[001]_C$-oriented rhombohedral PZN-PT showed no fatigue, whereas $[111]_C$-orientation, which corresponds to polarization axis, was not fatigue-free. This fatigue anisotropy is associated with engineered domain structure and was also observed in epitaxial PYbN-PT thin films. These results suggest that crystal orientation control becomes a new material solution for improving read/write endurance in FeRAM. After this study, the fatigue anisotropy has also been found in $Pb(In_{0.5}Nb_{0.5})O_3$-$Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ single crystals [51], epitaxial $BiFeO_3$ films [52], $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ ceramics [53], and $Bi_{3.15}Nb_{0.85}Ti_3O_{12}$ thin films [54].

Figure 3-4-1 shows the remanent polarization per unit area for the results of SBT film in this study and FeRAM capacitors developed after this study. Optimization of the composition increases the P_r value for SBT films, which is comparable to that for PZT thin films. FeRAMs with PZT or SBT thin film capacitors have been put into practical use after this study. Though scaling made progress, the remanent polarization has been staying at several ten to a few hundred nC/mm^2 [47, 48, 55-57]. Consequently, current technology node and the maximum capacity for the commercial FeRAMs is 130 nm and 4 Mbit, and there has been no remarkable progress in FeRAM integration. Reduction of the ferroelectric thickness and three-dimensional capacitor structure are necessary for further integration. Recently, some of doped HfO_2 was found to show ferroelectricity [58-60]. Because HfO_2 is compatible with CMOS process and its ferroelectric phase has sufficiently large P_r values, the doped HfO_2 will be a new promising candidate.

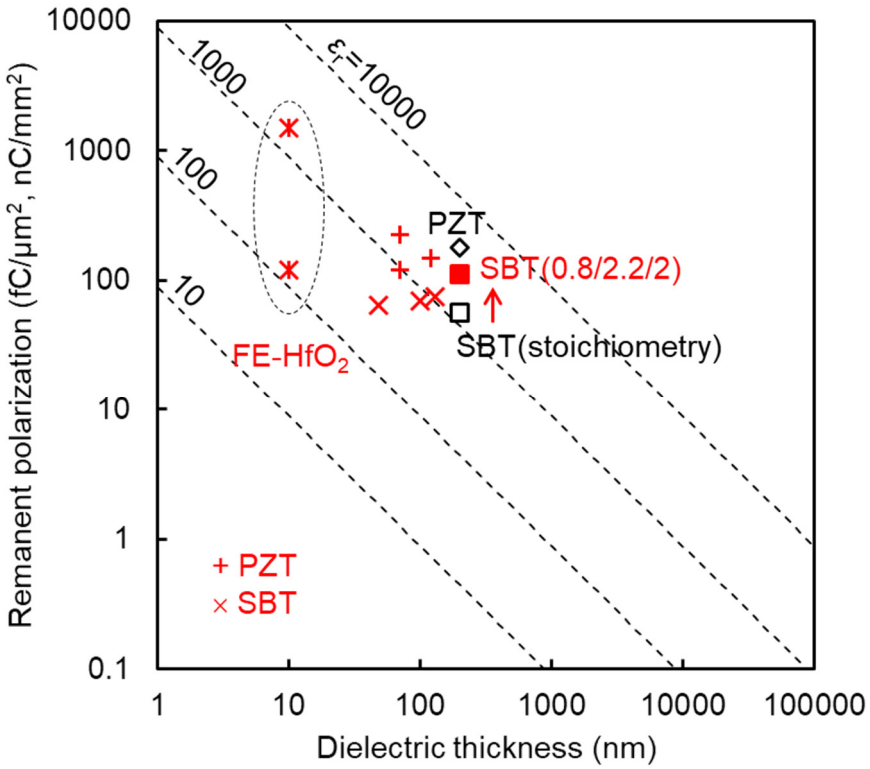

Fig. 3-4-1. Progress in increasing remanent polarization, *i.e.* storage charge density, by the present study and FeRAM capacitors developed after this study.

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Chapter 4
CAPACITOR-EMBEDDED SILICON INTERPOSERS FOR POWER INTEGRITY ISSUES

4-1 Introduction

4-1-1 Power integrity issues and 3-dimensional (3D) integration

Dynamic charging and discharging behavior of capacitors can be used for stabilizing and smoothing power supply voltage fluctuations. This is another important role of the capacitor in digital computing systems. Power integrity has been a crucial issue for high-performance and low-power integrated systems. In particular, the power integrity for 3D integrated systems (Fig. 4-1-1) becomes even more critical because of increasing integrated transistors and complexity of power distribution network (PDN).

Decoupling capacitors are the typical countermeasure for suppressing simultaneous switching noise. Because switching of transistors fluctuates the power supply voltage, the decoupling capacitors act as local power supplies and instantaneously

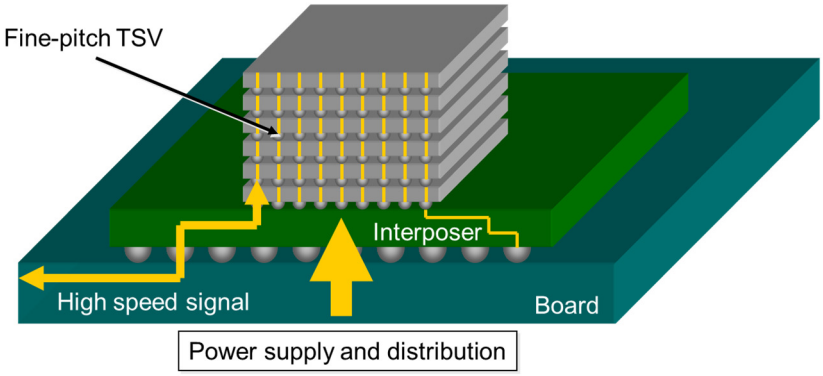

Fig. 4-1-1. 3D-integrated system.

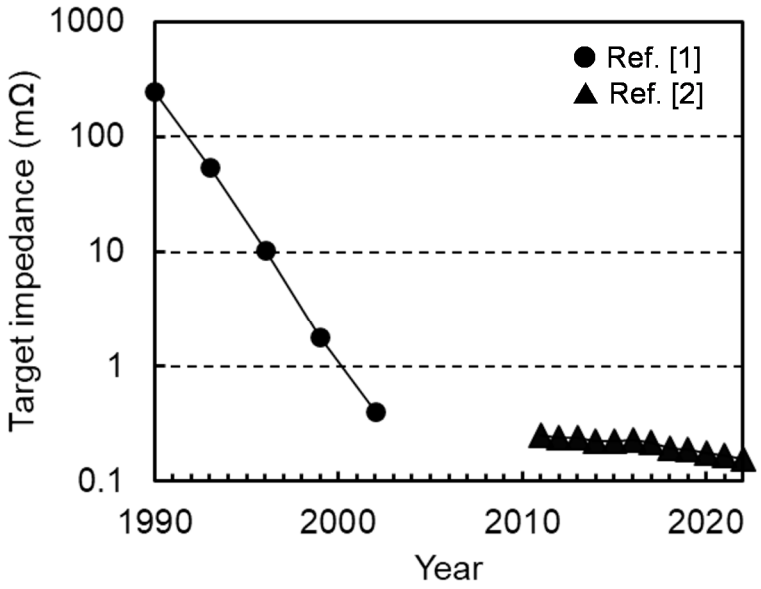

Fig. 4-1-2. Trends of the target impedance [1, 2].

compensate electronic charges to suppress the voltage fluctuation. From a viewpoint of designing methodology, the PDN system has to be maintained an appropriate impedance value in a broad frequency range. This impedance value is known as a target impedance (Z_{target}) and expressed by

$$Z_{target} = \frac{V_{dd} \bullet n}{i}, \tag{4-1}$$

where V_{dd} is a power supply voltage, n is an allowed ripple voltage, and i is current. To meet the Z_{target} value, various types of discrete capacitors are hierarchically configured in current electronic systems. Small and high capacitance multilayer ceramic capacitors (MLCCs) are placed near a processor to reduce PDN impedance in a high-frequency region. Continuous performance improvement for large scale integrated circuits (LSIs), however, has been depressing the target impedance and requires wider-band decoupling. Figure 4-1-2 shows the Z_{target} value trend based on the data by Smith *et al*. [1] and ITRS [2]. The Z_{target} value is required to be less than 1 mΩ up to a GHz region. The inductance of a straight rectangular wiring (L_w) in nH is expressed by

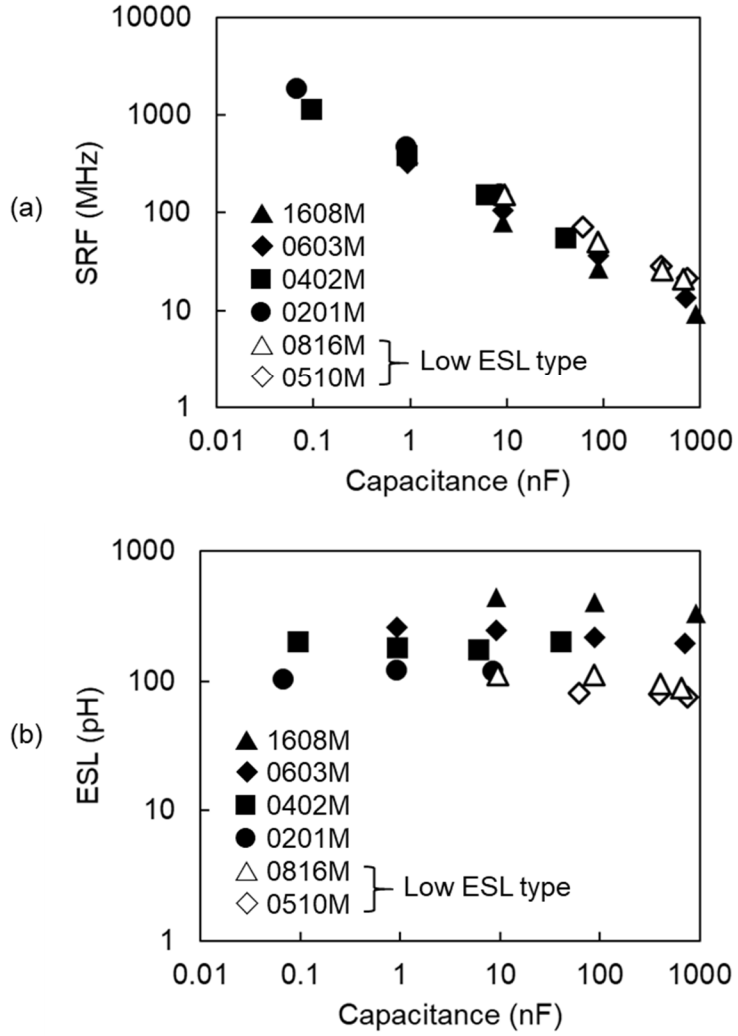

Fig. 4-1-3. (a) Self-resonant frequency and (b) equivalent series inductance for commercial MLCCs.

$$L_{\mathrm{w}} = 0.2l(\ln\frac{2l}{w+d} + 0.2235\frac{w+d}{l} + 0.5)\,, \qquad (4\text{-}2)$$

where l is the length in mm, w is the width in mm, and d is the thickness in mm [3]. According to Eq. 4-2, the inductance value for wirings in printed circuit boards is several hundred pH/mm, *e.g.* 645 pH for w = 0.1 and d = 0.035, and 278 pH for w = 1.0 and d =0.035. Because these values correspond to larger than 100 mΩ at 100 MHz, it is difficult to meet the Z_{target} value by capacitors on the board. Figures 4-1-3(a) and 4-1-3(b) show self-resonant frequency (SRF) and equivalent series inductance (ESL) for various

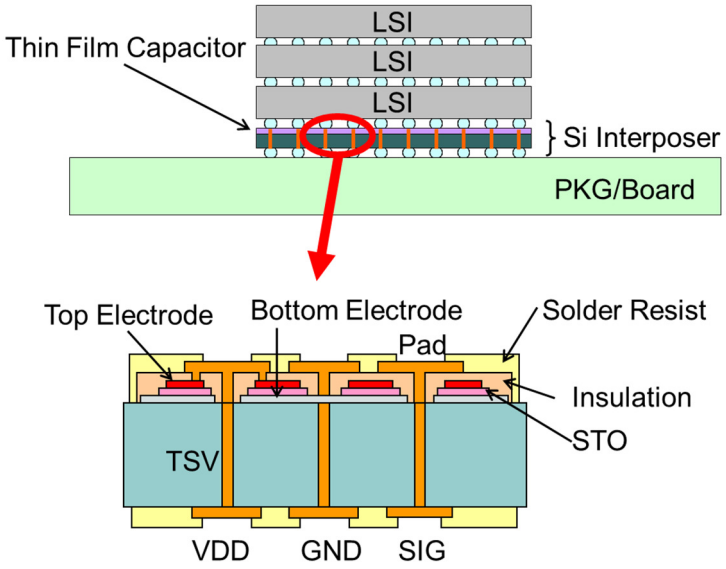

Fig. 4-1-4. Concept of a Si interposer with high ε_r thin film capacitor.

commercial MLCCs. The SRF values for the MLCCs with the capacitance value of larger than 47 nF are lower than 100 MHz, and the ESL values for the MLCCs are several hundred pH. It suggests that further reduction of parasitic inductance is necessary for wideband decoupling in 3D integrated systems although current LSI packages have decoupling capacitors at the rear surface of the package substrate to reduce the parasitic inductance of wirings.

From the viewpoint of proximity to transistors, on-chip decoupling capacitors are one of the solutions for decoupling in a higher frequency range. However, dielectric materials, fabrication process, and layout for on-chip capacitors are highly restricted in order to be compatible with the complementary metal-oxide-semiconductor (CMOS) process. Despite many efforts to increase capacitance for on-chip capacitors, the obtained capacitance density for simple planar metal-insulator-metal (MIM) capacitors was less than 1 $\mu F/cm^2$ [4-6].

Therefore, a Si interposer integrated with high dielectric constant (ε_r) thin film capacitors as illustrated in Fig. 4-1-4 can be a promising solution. A Si interposer, instead

of an LSI itself, is considered to be an integration platform for thin film capacitor and other passive devices. The Si interposer is a silicon-based chip carrier that bridges electrically and mechanically between LSIs and a conventional organic substrate. In addition to creating connections by using high-density wirings and relaxing the thermal stress, thin film passive components can be integrated into the Si interposer. The size of the interposer is almost the same as or larger than that of the stacked LSI. The whole area can be used for thin film capacitors, and the capacitor fabrication process is independent of the CMOS process. The Si interposer has another advantage in fine-patterning. Fine through-Si-vias (TSVs) can be fabricated using reactive ion etching, so that the Si interposer can receive a high-pin-count LSI. Because the capacitors in the Si interposer are directly connected and stacked with an LSI, the capacitors are expected to exhibit an extremely low parasitic inductance.

The distribution and integration of various types of power supplies are also a critical issue for 3D integrated systems because these stacked LSI chips require their own power supplies to provide proper voltage and current. On-chip power supplies are expected to reduce the power losses due to the parasitic impedance of the power lines and to save on footprint when compared with discrete voltage regulators. In Addition to the multiplicity of the power supplies, distributed on-chip power supply circuits with buck converters are crucial in recent low-power LSI designs based on space-domain fine-grain voltage engineering because hundreds of domains in future LSIs will be controlled by different clock frequencies along with adequate power supply voltages, which is called dynamic voltage and frequency scaling (DVFS) [7]. The buck converter is a kind of step-down voltage regulator that has higher power efficiency than other kinds of DC-DC converters.

Usually, the output filter which consists of a capacitor and an inductor for conventional on-chip buck converters is not monolithically integrated with an LSI but

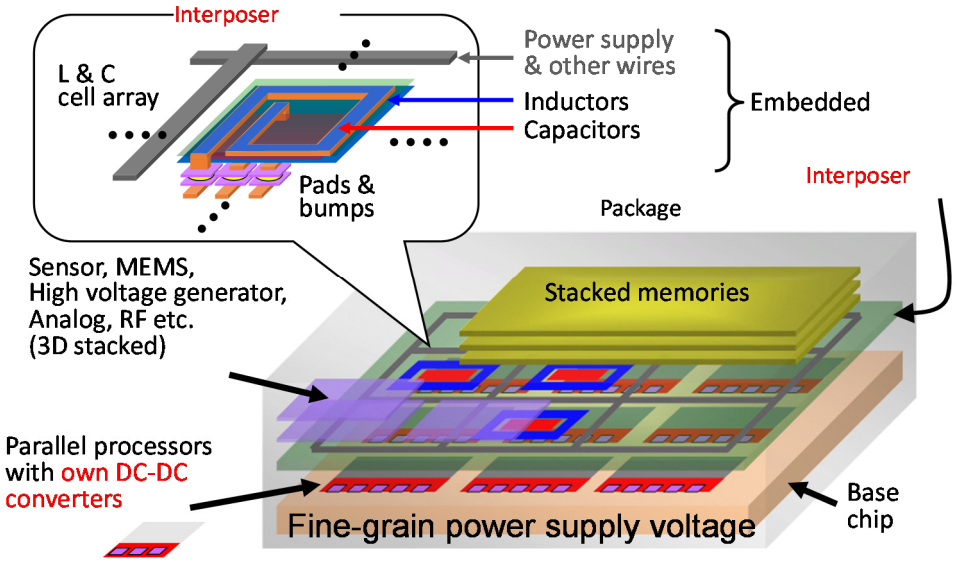

Fig. 4-1-5. Concept of distributed power supplies using a Si interposer [7].

configured with external discrete components on a printed circuit board. It is difficult to layout many *LC* filters around the LSI when the number of buck converter increases. Though fully-integrated on-chip buck converters were reported, they had a drawback of the large occupying area [8] or very high switching frequency [9]. Separating the output filter from the active components is feasible solution based on 3D integration technology, and the concept of a distributed power supply for high-performance 3D integrated systems has been proposed and demonstrated [7]. Integration scheme for the distributed on-chip power supplies is also utilization of a Si interposer as a platform for passive device integration, as shown in Fig. 4-1-5 [7].

4-1-2 Previous studies

The form of the thin film can reduce the internal inductance of the capacitor [10, 11], and inductance for wiring between an LSI and a capacitor can be minimized by direct connection to the LSI. Therefore, Si interposers equipped with high ε_r thin film capacitors

will have large capacitance and extremely low parasitic inductance, and consequently, reduce impedance in a higher frequency range as compared to the capacitor-embedded organic interposers in which commercial chip capacitors are embedded. Some research groups reported Si interposers integrated with thin film capacitors. Rooseboom *et al*. [12] and Knickerbocker *et al*. [13] developed Si interposers with deep-trench MOS capacitor for RF transceivers. The dielectric layer was oxide-nitride-oxide (ONO) films. Kamehara *et al*. [14] proposed (Ba,Sr)TiO_3 (BST) thin film capacitors for this application. Mori *et al*. [15] developed Ta_2O_5 capacitors for RF circuits. However, there was no report on the integration process of high dielectric constant perovskite oxide thin film capacitor and TSVs into Si interposers.

The on-chip power supply application needs to integrate both an inductor and a capacitor into a Si interposer. Only Takamiya *et al*. [7] reported *LC*-filter-embedded Si interposer fabricated in 0.35-μm CMOS process. The embedded capacitor and inductor were a 1-nF MOS capacitor and a 22-nH Al spiral inductor. The switching frequency was 200 MHz. The maximum power efficiency with the input voltage of 3.3 V and the output voltage of 2.3 V was 62% at an output current of 70 mA. Figure 4-1-6 summarizes the switching frequency and the inductance value for the on-chip buck converters presented at the International Solid-State Circuits Conference (ISSCC). There is a frequency gap between the buck converters employing an on-chip inductor and an external inductor around 10 MHz. The lower switching frequency is generally favorable to higher power efficiency and lower power consumption. The 3D-stacked buck converter with the *LC*-filter-embedded Si interposer is expected to have lower switching frequency than the reported converters with an on-chip inductor by non-CMOS process increasing capacitance and inductance and reducing parasitic resistance.

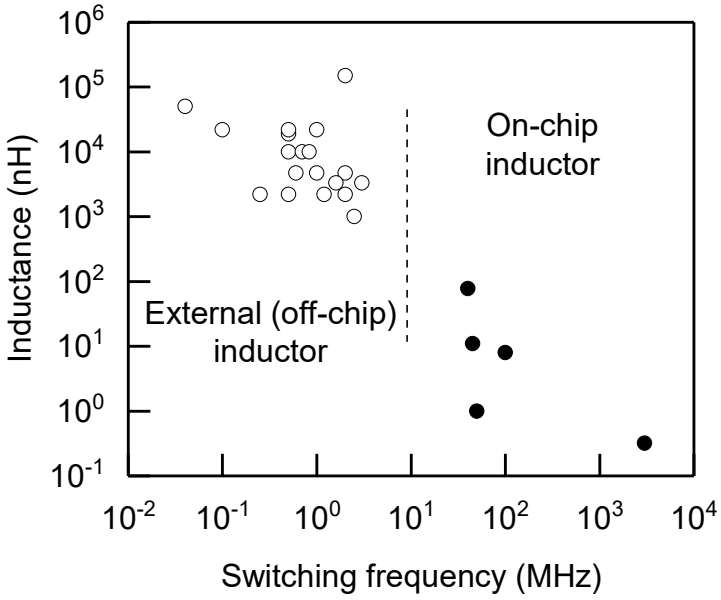

Fig. 4-1-6. Trends of the switching frequency and the inductance value for on-chip buck converters reported at ISSCC.

4-1-3 Objectives of this chapter

As described above, hybrid integration of high ε_r thin film capacitors using 3D stacking technologies is a key for power integrity applications, in contrast to monolithic integration for the memory application discussed in chapters 2 and 3. The requirements for thin film capacitors from power integrity applications are summarized in Table 4-1-1. Interconnection, such as the shape of the capacitors, bonding, and impedance characteristics, is the main issue. The objectives of this chapter are a clarification of the structure-properties relationship for thin film capacitors, the development of integration process for high ε_r thin film capacitor into Si interposers, and demonstration of the capacitor-embedded Si interposers.

Two applications have been studied. One is a 3D-integrated decoupling capacitor directly connected to an LSI. The target capacitance density was 1 $\mu F/cm^2$, which was larger than the capacitance density for on-chip capacitors reported at the beginning of this

Table 4-1-1. Requirements for thin film capacitors from power integrity applications.

Requirements		Solutions
Impedance	Lower impedance than MLCC (ESL <10 pH)	Multi-contact capacitor
Area, size	Chip-scale size (>1 cm^2) for connecting multiple pads to a capacitor electrode	Optimizing electrode material and deposition conditions
Capacitance	Higher capacitance density than on-chip MIM capacitor (> 1 $\mu F/cm^2$)	STO thin films and via-middle process
Stacking process	Direct connection with an LSI	Chip-to-wafer bonding

study. The other application is a 3D-stacked buck converter. An *LC*-filter was integrated into a Si interposer. The target switching frequency was less than 40 MHz, which was the lowest switching frequency for on-chip power supplies with on-chip inductors.

4-2 $SrTiO_3$-Thin-Film-Capacitor-Embedded Si Interposer [16-18]

4-2-1 Large-area $SrTiO_3$ (STO) thin film capacitors

Because an LSI have generally multiple power and ground pads, a thin film decoupling capacitor directly connected with LSI pads have to be as large as the LSI, which is typically larger than 1 cm^2. Such large capacitors tend to include defects which cause short failure. Therefore, the relationship between yield, the ε_r value, and STO deposition conditions has been studied.

The STO thin film capacitors were fabricated using sputter-deposition, photolithography, and etching. The bottom electrode materials were Pt or Ru. The STO deposition conditions are summarized in Table 4-2-1. Figures 4-2-1 and 4-2-2 show the ε_r values for the 100-nm-thick STO thin film capacitors depending on the deposition temperature and leakage current for the STO films at 400°C. The capacitor was simple planar metal-insulator-metal (MIM) structure and the electrode area was 100 μm × 100 μm. The ε_r values of higher than 200 were obtained for the 100-nm-thick STO thin films at 600°C for both on Pt and on Ru. The leakage current did not depend on the bottom electrode and the breakdown voltage was higher than 20 V, indicating that 100-nm-thick STO film was a good insulator.

However, the defect density in the STO thin film capacitors, which leads to initial

Table 4-2-1. STO thin film deposition conditions.

Target	5 mol.% Mn-doped $SrTiO_3$ ceramics
Sputtering gas	80% Ar - 20 % O_2
Deposition temperature	400 - 600°C
Bottom electrode	Pt/Ta, Ru/Ta
Top electrode	Pt, Ru, TiN

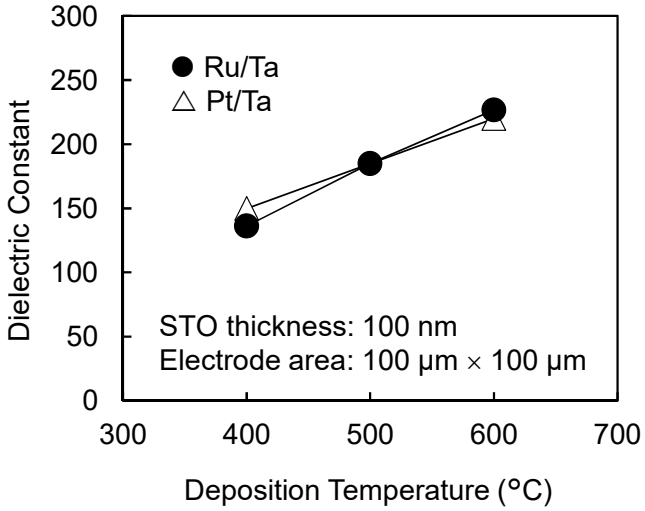

Fig. 4-2-1. Deposition temperature dependence of ε_r values for sputter-deposited STO thin films on Ru/Ta and Pt/Ta bottom electrodes.

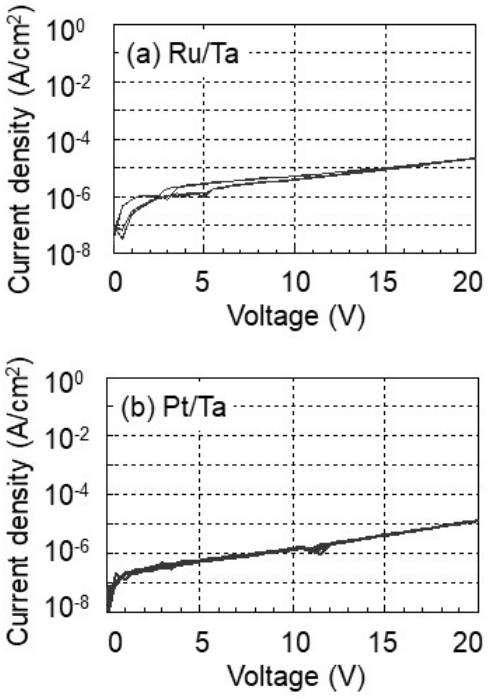

Fig. 4-2-2. Leakage current for sputter-deposited STO thin films at 400°C on (a) Ru/Ta and (b) Pt/Ta bottom electrodes.

short failure, depends on the STO deposition temperature and the bottom electrode materials, as shown in Fig. 4-2-3. The initial failure was defined by the breakdown voltage

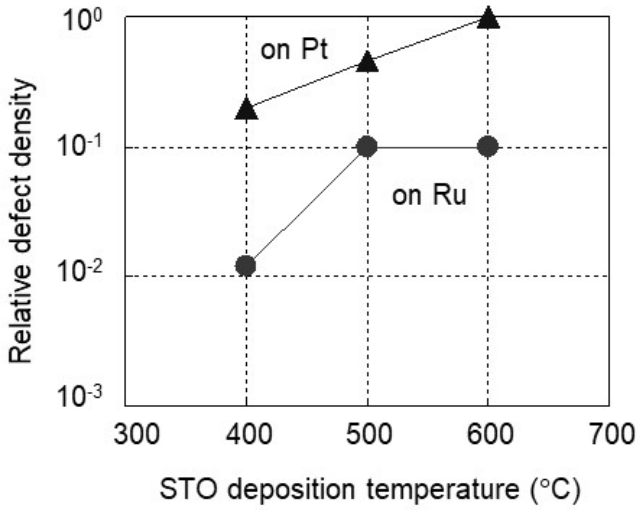

Fig. 4-2-3. Relative defect density for the STO thin film capacitors on Ru and Pt. Initial failure was defined by the breakdown voltage less than 5 V.

of less than 5 V. The defect density was calculated from the electrode area dependence of the yield for each deposition condition. On the assumption that the defects are randomly distributed over a wafer, probability ($P(n)$) that n defects are included in the capacitor obeys the Poisson distribution and is expressed by

$$P(n) = \frac{DS^n}{n!}\exp(-DS)\,, \tag{4-3}$$

where D is the defect density and S is the electrode area. The relative defect density increases with the deposition temperature. The defect density also depends on the bottom electrode materials, and the estimated defect density for the Ru bottom electrode is much smaller than that for the Pt bottom electrode. The defect density depending on the STO deposition temperature and the bottom electrode materials can be explained by surface morphology [18]. As a result, the 100-nm-thick STO thin films deposited at 400°C on Ru were used as capacitor dielectrics for the embedded capacitors in Si interposers because of their adequate ε_r values of approximately 140, sufficient breakdown strength of more than 20 V, and the lowest defect density in the present study.

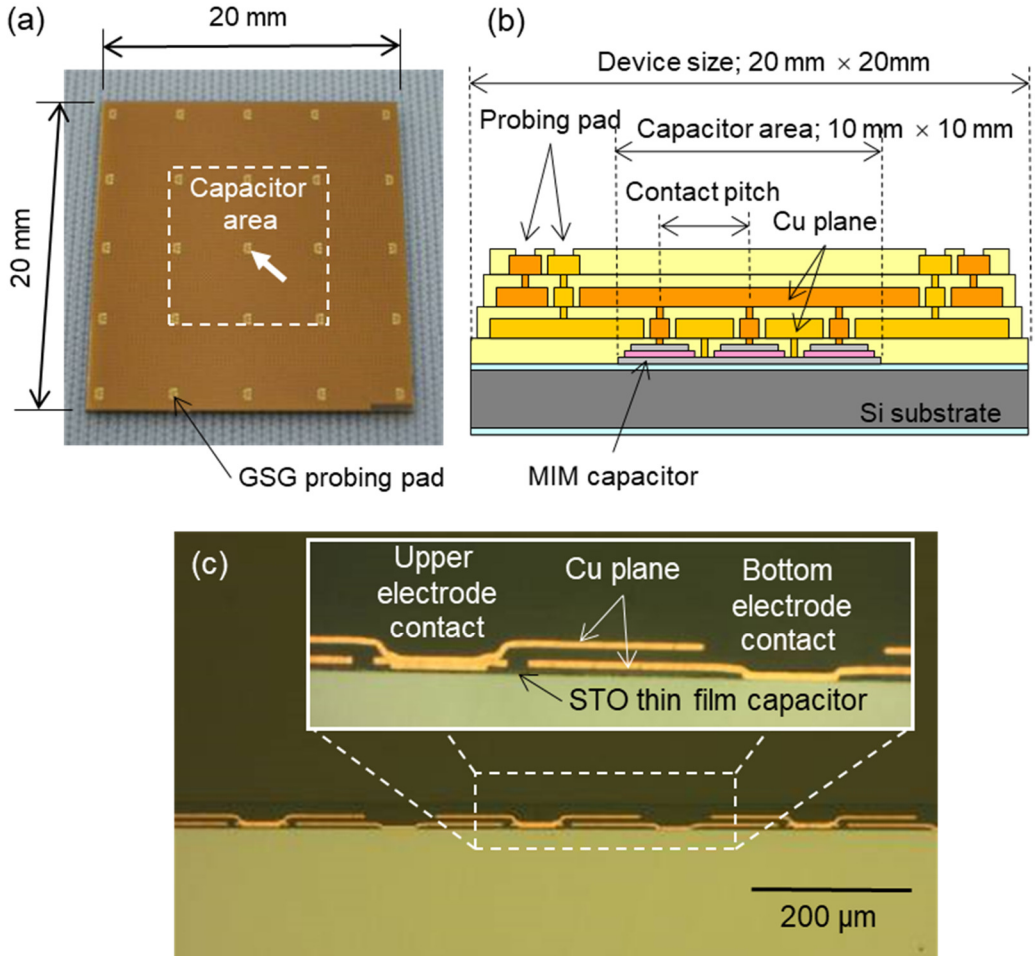

Fig. 4-2-4. (a) Top-view image, (b) schematic cross-section, and (c) cross-sectional photograph of the impedance measurement device.

4-2-2 Impedance characteristics of multi-contact STO thin film capacitors

There was little data on impedance characteristics depending on the configuration of the thin film capacitors and interconnects for Si interposer applications though parasitic components of capacitors strongly affect the overall performance of the capacitors. Therefore, the relationships between capacitor structure and impedance in a high-frequency range have been studied. MIM capacitors on Si substrates using high ε_r STO thin film dielectrics were fabricated, and their *Z*-parameters were evaluated.

Three types of test devices with STO thin film capacitors on Si substrates were

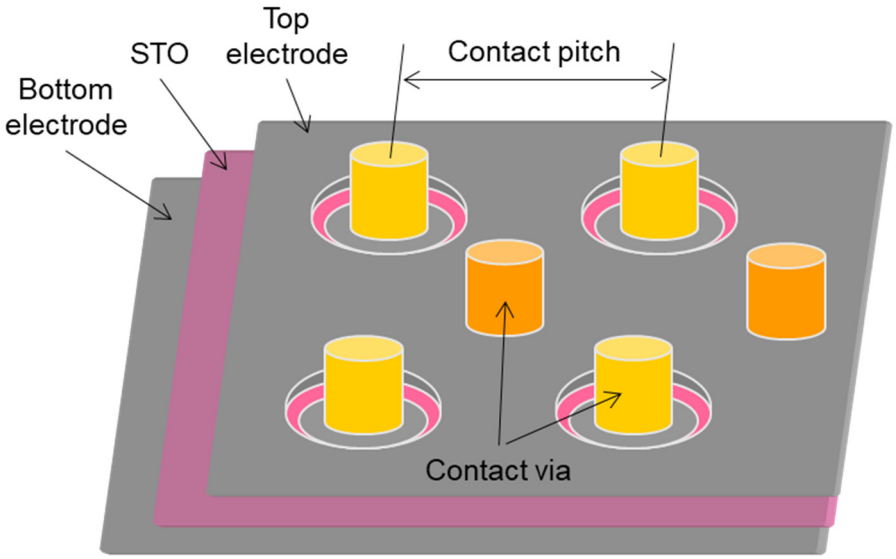

Fig. 4-2-5. Configuration of the capacitor electrodes and contacts.

Table 4-2-2. The number of contacts for the top and bottom electrodes of the tested devices.

Contact pitch (μm)	250	750	2250
# of contacts			
Top electrode	1396	144	16
Bottom electrode	1440	160	16

prepared. The size of the test devices was 20 × 20 mm. The thin film capacitors were 10 mm × 10 mm and placed at the center of the devices. The capacitance value was about 1 μF. Figures 4-2-4(a), 4-2-4(b), and 4-2-4(c) show the top-view image and schematic cross-section, and the cross-sectional photograph of the test device, respectively. Two Cu planes were placed over the capacitor. The MIM capacitors had multiple contacts, and the bottom and top electrodes connected to the lower and upper Cu planes, respectively. As shown in Fig. 4-2-5, these two types of interconnections were staggered, and the pitch for the contacts was varied from 250 to 2250 μm. The capacitor configuration is summarized in Table 4-2-2. GSG-configured probing pads were prepared in a 5 × 5 configuration at

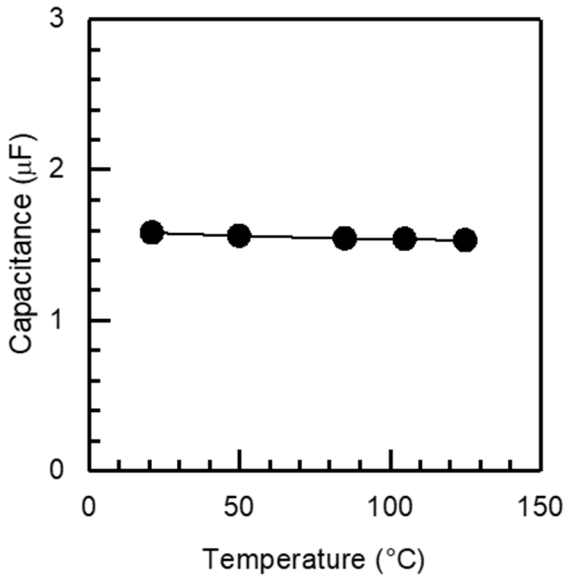

Fig. 4-2-6. Temperature dependence for the capacitance values of the tested devices.

the surface of each test device to measure the impedance. Arrowed probing pads were used for the following measurements.

The preparation process for the test devices is as follows. The substrates were thermally-oxidized Si wafers with a resistivity higher than 5000 Ω·cm. The bottom electrode, STO, and the top electrode layers were successively deposited by sputtering. The bottom and top electrode materials were Ru. The thickness and the deposition temperature for the STO thin films were 100 nm and 400°C. More detail deposition conditions and the basic properties are described in the previous section. After MIM capacitor fabrication, interlayer dielectrics with photosensitive polyimide and 5-μm-thick Cu planes by electroplating were formed alternately, then multilayer interconnections were obtained. The probing pads at the surface were finished with electroless-plated Ni/Au to reduce contact resistance. The capacitance values for the test devices were 1.2 ~ 1.6 μF, which were measured at 100 kHz using the HP (currently Keysight) 4194A impedance/gain-phase analyzer. The temperature dependence for the capacitance values of a test device is shown in Fig. 4-2-6. The capacitance was almost constant from 20 to

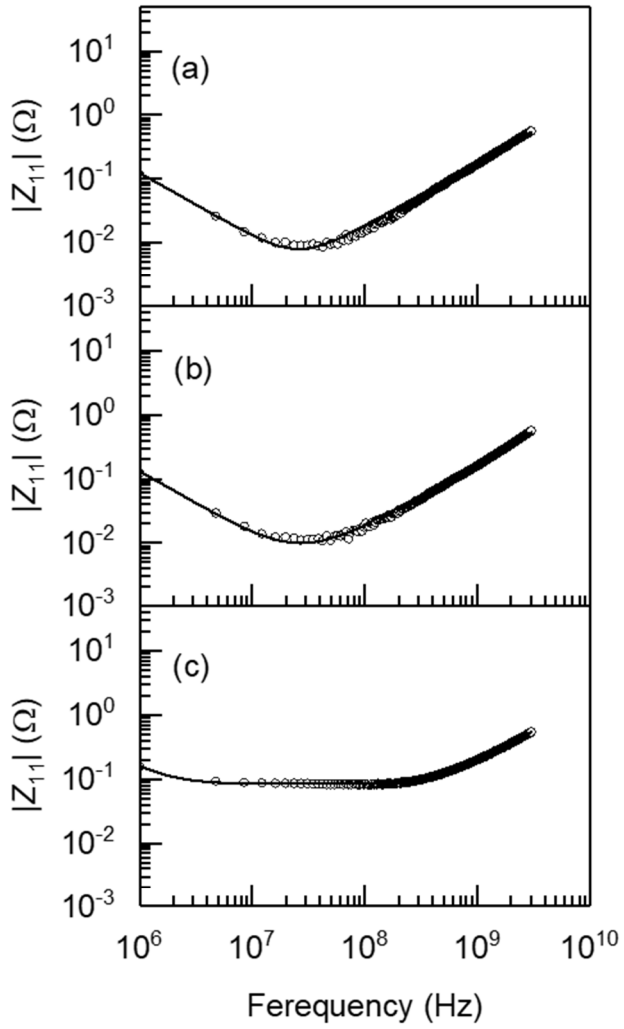

Fig. 4-2-7. Measured (open circle) and simulated (solid line) Z_{11} curves for the STO thin film capacitors. The contact pitch was (a) 250 μm, (b) 750 μm, and (c) 2250 μm.

125°C.

Input impedance (Z_{11}) values for the test devices were measured with the Agilent (currently Keysight) E4991A RF impedance/material analyzer between 1 MHz to 3 GHz with a 1-port configuration. The obtained Z_{11} values are shown in Fig. 4-2-7. The measured Z_{11} values exhibit capacitor-like behavior and were less than 1 Ω in the entire measurement frequency range. Assuming a simple series equivalent circuit as shown in

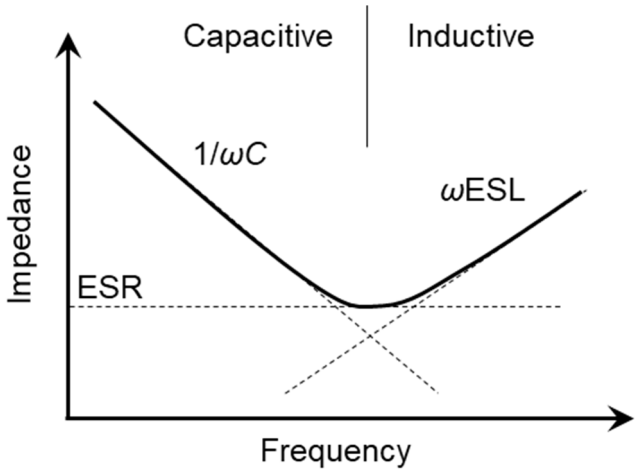

Fig. 4-2-8. Impedance curve for practical capacitors.

Table 4-2-3. Apparent ESR and ESL values.

Contact pitch (μm)	C (μF)	ESR (Ω)	ESL (pH)
250	1.28	0.008	28.9
750	1.22	0.01	28.1
2250	1.16	0.085	28.3

Fig. 4-2-8, frequency dependence of the Z_{11} value is expressed by

$$|Z_{11}| = \sqrt{{R_S}^2 + (\omega L_S - \frac{1}{\omega C})^2}\ , \tag{4-4}$$

where ω is angular frequency, R_s and L_s are equivalent series resistance (ESR) and equivalent series inductance (ESL), respectively. The fitted curves are also shown in Fig. 4-2-7. The fitting parameters including ESR and ESL values are listed in Table 4-2-3.

Though the ESR and ESL values for the MIM capacitors are assumed to depend on the number of contacts, the differences for the estimated ESR and ESL values between the test devices are small. In other words, the parasitic resistance seems to be dominant for the test devices with the 250- and 750-μm-pitch contacts and the ESR for the capacitor is larger than the parasitic resistance for the devices with the 2250-μm-pitch contacts

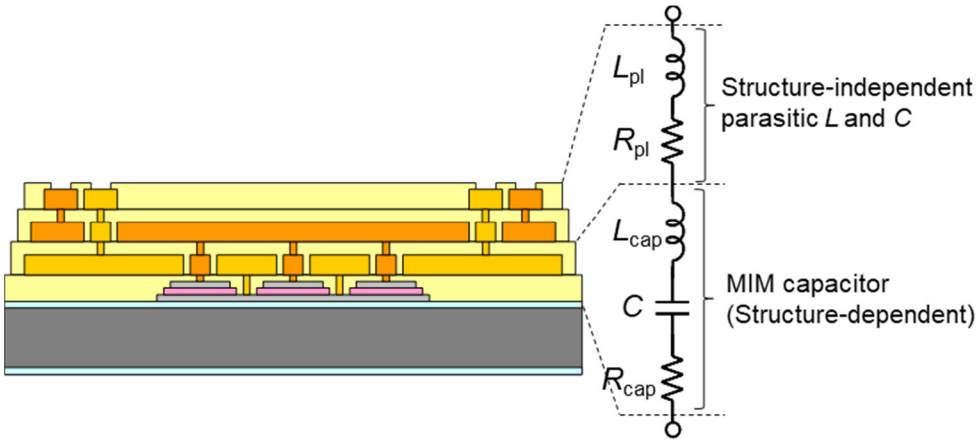

Fig. 4-2-9. Structure-independent parasitic resistance and inductance in the measured devices.

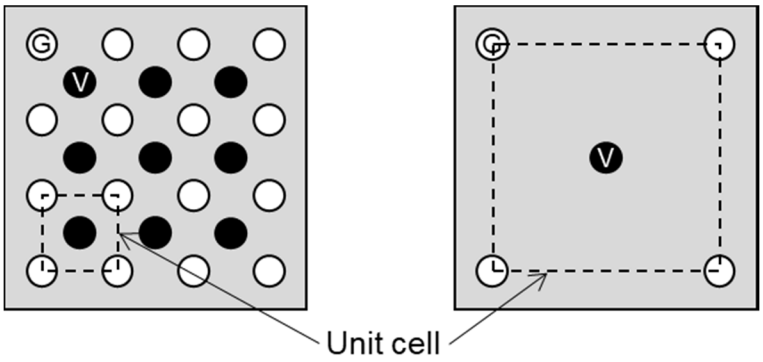

Fig. 4-2-10. Unit cell for multi-contact MIM capacitors.

because of the small number of the contact. Similarly, the parasitic inductance is thought to be larger than the true ESL values for the thin film MIM capacitors. Therefore, the structure-independent parasitic series resistance and inductance have to be taken into account in a measured system, as shown in Fig. 4-2-9.

Considering the unit cell for the multi-terminal MIM capacitors as shown in Fig. 4-2-10, the intrinsic ESR values (R_{cap}) is in inverse proportion to the number of the unit cell,

$$R_{cap} = \frac{r}{N} \approx \frac{rd^2}{S}, \tag{4-5}$$

where r is the resistance value of the unit cell, N is the number of the unit cell, d is the

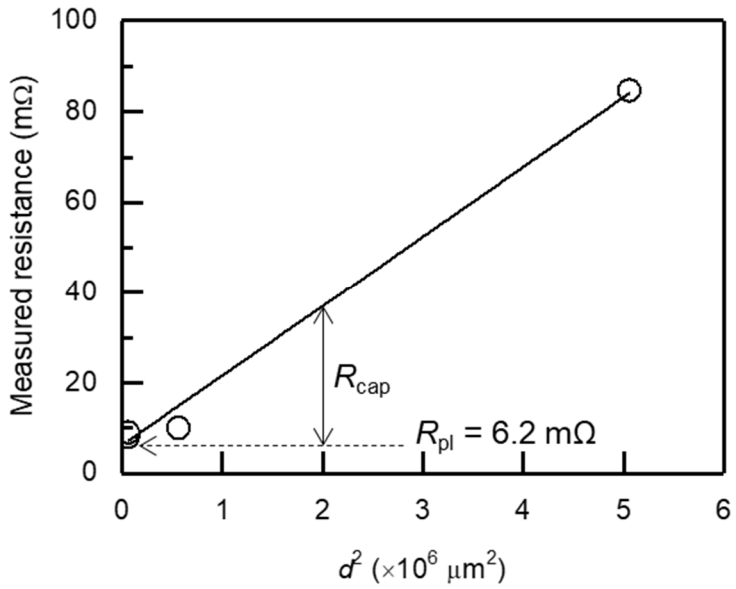

Fig. 4-2-11. Estimation of the R_{cap} values from the measured resistance values.

Table 4-2-4. Obtained R_{cap} values.

Contact pitch (μm)	R_{cap} (Ω)
250	0.002
750	0.004
2250	0.079

contact pitch, and S is the total electrode area. Figure 4-2-11 shows the apparent ESR values depending on the square of the d value. The intercept corresponds to the parasitic resistance (R_{pl}), which is evaluated to be 6.2 mΩ. The R_{cap} values can be obtained by subtracting the R_{pl} values from the apparent ESR values, and are listed in Table 4-2-4. The multi-terminal thin film MIM capacitor with the 250-μm-pitch contacts has very small ESR values of a few mΩ.

The apparent ESL values for the test devices are also regarded to consist of structure-dependent intrinsic ESL (L_{cap}) and structure-independent parasitic inductance (L_{pl}). The apparent ESL values, however, does not indicate the structural dependence of

the MIM capacitors. This suggests that the apparent ESL values are dominated by the L_{pl} values. The L_{pl} value was evaluated from the impedance measurement for the samples without the MIM capacitor. The evaluated L_{pl} value was 22.5 pH, which is comparable to the apparent ESL values. The L_{cap} value for the test device with the 250-μm-pitch contacts is estimated to be 6.4 pH. The ESR and ESL values for commercial MLCCs are several hundred mΩ and several hundred pH, respectively. Therefore, the multi-terminal STO MIM capacitors are assumed to have extremely small ESR and ESL values. In practical use as decoupling capacitors for 3D LSIs, the effective ESR and ESL will be dominated by the parasitic resistance and inductance, which are due to interconnections, such as solder bumps, vias, and wiring. Direct connection to the LSI pads without redistribution wirings is favorable for minimizing the parasitic resistance and inductance.

4-2-3 Comparison with discrete capacitors

Because the ESL and ESR values for the multi-contact high ε_r thin film capacitor are much smaller those for conventional discrete capacitors as described in the previous section, transfer impedance (Z_{21}) values for the multi-contact STO thin film decoupling capacitor have been compared with those for conventional decoupling capacitors in a wide frequency range to evaluate advantage in reducing PDN impedance.

As shown in Fig. 4-2-12, impedance measurement system was composed of Ultimetrix P4800K impedance analyzer (IMA) and Agilent (currently Keysight) N5245A vector network analyzer (VNA). Because a VNA is generally used to measure the impedance value larger than 0.01 Ω in a GHz range, the IMA performs a complementary role in measuring lower impedance value in a lower frequency range. This system enables seamless impedance measurement using two types of instruments by connecting the IMA and the VNA with a coaxial switch in a wide frequency range from 10 Hz to 40 GHz. The

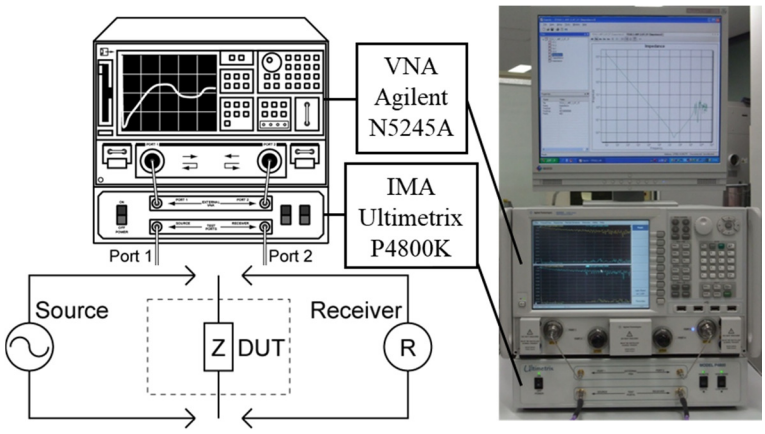

Fig. 4-2-12. Transfer impedance measurement system [19].

measurement system is detailed in Ref. [19].

Three types of capacitor-mounted or capacitor-embedded interposer test devices, *i.e.* chip-capacitor-surface-mounted and chip-capacitor-embedded organic interposers, and an STO-thin-film-capacitor-embedded silicon interposer, were prepared for evaluation. The schematic cross-sectional views and photographs for the interposer test devices are shown in Figs. 4-2-13 and 4-2-14. The outline of the test devices was 20 mm × 20 mm and the 1.1 - 2.4 μF capacitors were mounted or embedded in the center region of 10 mm × 10 mm in the test devices. The surface-mount-type test device has 24 LW-reverse-type chip capacitors on the rear side of an organic interposer. The case size and the capacitance value for surface-mounted capacitors were 0816M (length × width = 0.8 mm × 1.6 mm) and 47 nF. The total capacitance value was 1.175 μF. Twenty-four 0603M (length × width = 0.6 mm × 0.3 mm) case-sized chip capacitors were buried in the embedded-capacitor-type test device with B^2it technology [20]. The capacitance value for the embedded chip capacitor was 100 nF, resulting in the total capacitance value of 2.4 μF. The 1.2 μF STO thin film capacitor was integrated into the Si interposer, which was the same sample described in the previous section. The distance from the measures pad to the capacitors were 1090 μm for the surface-mount-type, 150 μm for the embedded-

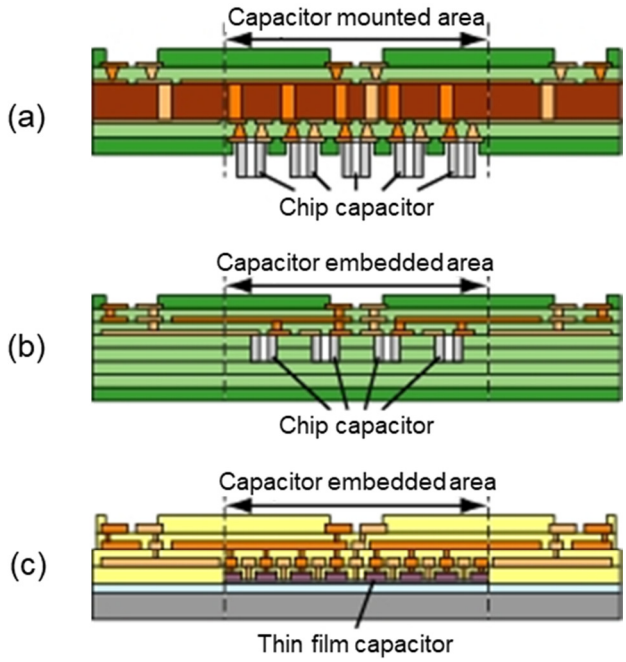

Fig. 4-2-13. Schematic cross-sectional views of the test interposer devices: (a) chip-capacitor-surface-mounted organic interposer, (b) chip-capacitor-embedded organic interposer, and (c) STO-thin-film-capacitor-embedded Si interposer.

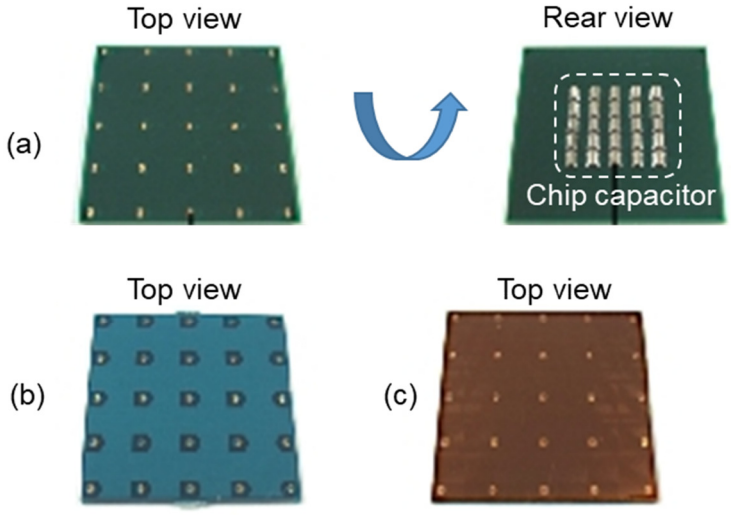

Fig. 4-2-14. Photographs of the measured test interposer devices: (a) chip-capacitor-surface-mounted organic interposer, (b) chip-capacitor-embedded organic interposer, and (c) STO-thin-film-capacitor-embedded Si interposer.

capacitor-type, and 32 μm for the Si interposer.

Transfer impedance (Z_{21}) values for the interposer test devices from the 3rd terminal

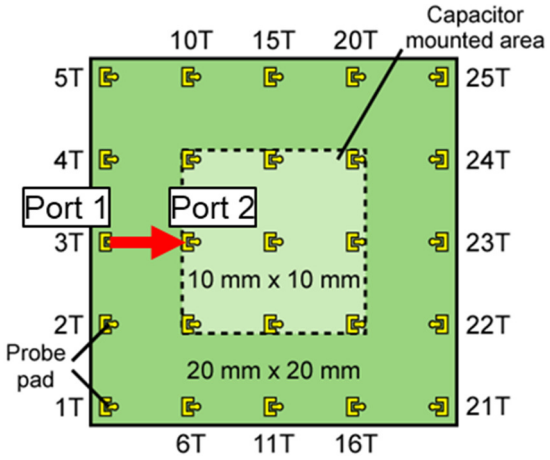

Fig. 4-2-15. Transfer impedance measurement ports.

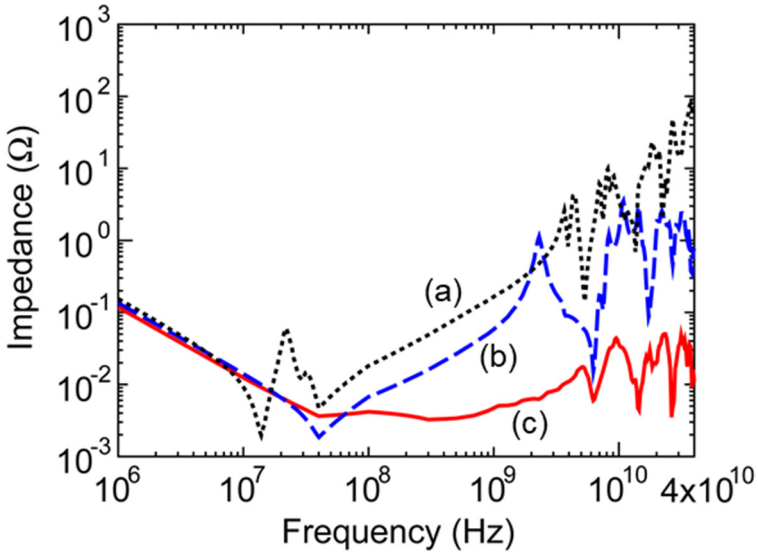

Fig. 4-2-16. Transfer impedance for (a) chip-capacitor-surface-mounted organic interposer (dashed line), (b) chip-capacitor-embedded organic interposer (broken line), and (c) STO-thin-film-capacitor-embedded Si interposer (solid line).

to the 8th terminal were measured as shown in Fig. 4-2-15. The obtained results are shown in Fig. 4-2-16. Wide frequency range measurements up to 40 GHz were successfully carried out by using the developed measurement system described above. The Z_{21} value for the STO-thin-film-capacitor-embedded Si interposer is less than 0.1 Ω in a wide frequency range from 1 MHz to 40 GHz. It is notable that the Z_{21} value for the STO-thin-

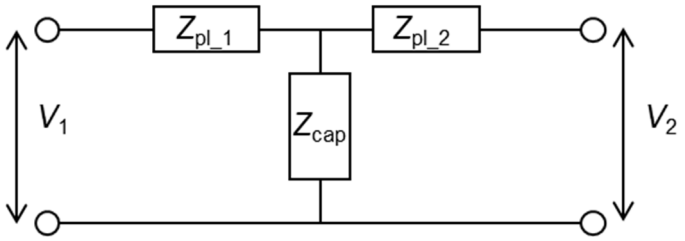

Fig. 4-2-17. T-network.

film-capacitor-embedded Si interposer is smaller than that for the chip-capacitor-surface-mounted and chip-capacitor-embedded organic interposers in a frequency range higher than 100 MHz.

Considering impedance of the capacitor structure (Z_{cap}) and impedance from probing pad to the capacitor (Z_{pl_1}, Z_{pl_2}), the Z_{21} measurement circuit can be regarded as a T-network as shown in Fig. 4-2-17. The Z_{11} and Z_{21} values are given by

$$Z_{11} = Z_{pl\_1} + Z_{cap} , \tag{4-6}$$

$$Z_{21} = Z_{cap} . \tag{4-7}$$

The minimum Z_{21} value for the STO-thin-film-capacitor-embedded Si interposer is approximately 3 mΩ, which is consistent with the ESR value for the MIM capacitor structure estimated from the Z_{11} measurements. The ESL values at 1 GHz for the chip-capacitor-surface-mounted and chip-capacitor-embedded organic interposers and the Si interposer were estimated to be 32 pH, 9.5 pH, and 0.62 pH, respectively. Though parallel connection of chip capacitors reduces effective ESL values for the organic interposers, the multi-contact STO thin film capacitor appears more effective to reduce impedance, particularly in a frequency range higher than 100 MHz. The Si interposer with the multi-contact STO thin film capacitor is a promising solution to reduce the PDN impedance in a GHz range for 3D integrated systems.

Table 4-2-5. Comparison of TSV integration process.

	TSV formation	Dielectric material	TSV connection
Via-first	Before capacitor	Low deposition temperature	TSV oxidation, Thermal expansion
Via-middle	Between capacitor and wiring	OK	OK
Via-last	After wiring	OK	Etching, Pad area penalty

4-2-4 Integration process with through-Si-vias (TSVs)

The impedance measurements reveal that the multi-terminal STO thin film capacitor has enormously low ESL as discussed in earlier sections. The features will be of great advantage for reducing PDN impedance in a GHz frequency range when the thin film capacitor is directly connected with an LSI to minimize parasitic inductance and resistance between the thin film capacitor and the LSI. This section describes integration process of the multi-terminal STO thin film capacitor and TSVs into a Si interposer between an LSI and an organic package substrate.

Table 4-2-5 summarizes comparison of TSV integration process. Because TSVs are fabricated before capacitors in the via-first process, the STO deposition temperature is limited due to oxidation and thermal expansion of TSVs. The via-last process has disadvantages of connection between TSV and wiring. Control of over-etching is very difficult, so that the TSV etching process damages wirings. Connecting pads between TSVs and wirings are necessary to avoid misalignment. It causes an increase in area penalty. Therefore, the via-middle process is thought to be the optimum process for integration of thin film decoupling capacitors. The stacking process for the Si interposer is based on a chip-to-wafer bonding technique because the size of a Si interposer is not

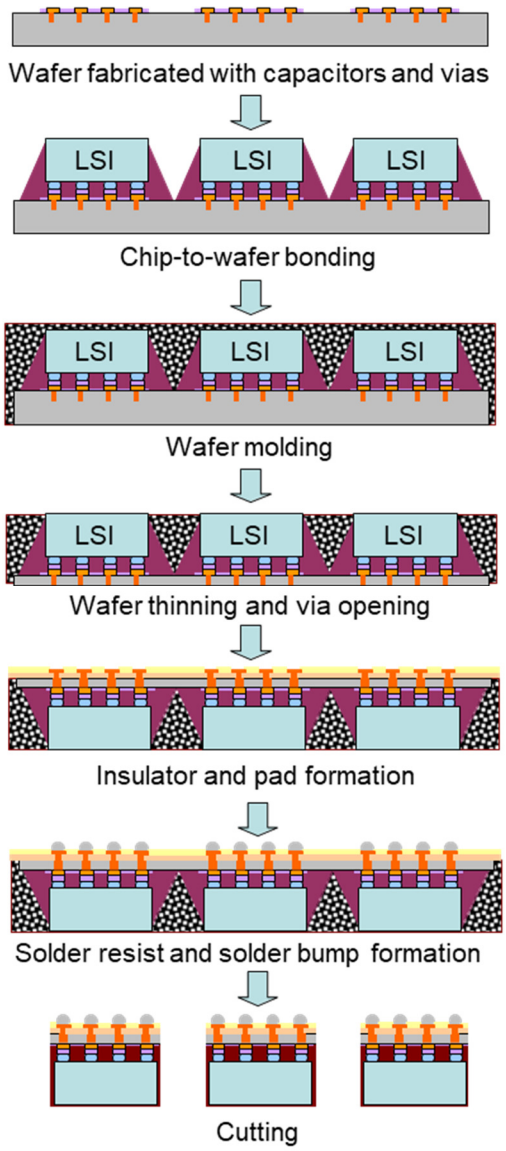

Fig. 4-2-18. Si interposer fabrication and stacking process based on via-middle chip-to-wafer bonding.

always the same as that of an LSI. The process flow is shown in Fig. 4-2-18.

First, STO thin film capacitors and Cu-filled cavities are integrated with a Si wafer, and flip-chip bonding pads are prepared. After the MIM capacitor fabrication, 50-μm-deep and 50-μm-diameter cavities are formed on the wafers using reactive ion etching, and the sample surface is insulated with SiO_2. Then the cavities are filled with electroplated Cu, which become TSVs. Figures 4-2-19(a) and 4-2-19(b) show top-view

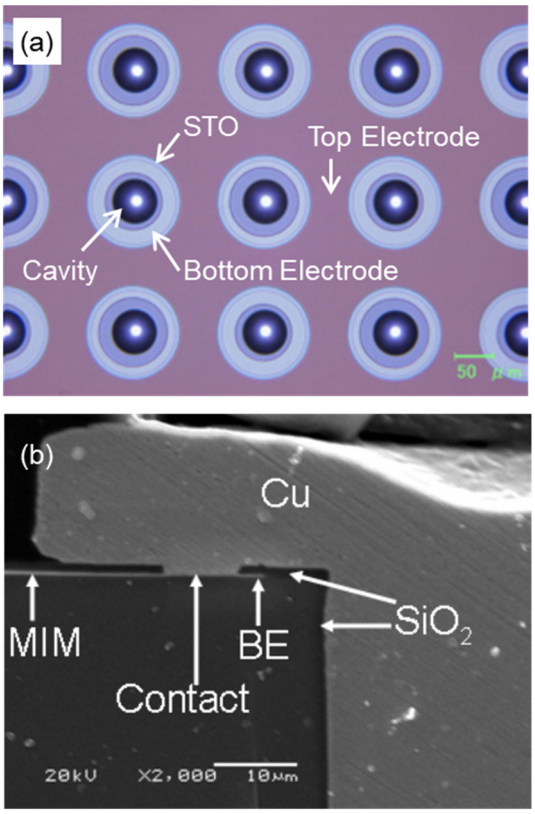

Fig. 4-2-19. (a) Top-view and (b) cross-sectional images of the interposer with STO thin film capacitor deposited at 400°C on Ru.

and cross-sectional images of the interposer integrated with an STO thin film capacitor deposited at 400°C on Ru, respectively. Consequently, a maximum capacitance of approximately 7 μF was obtained for 60-nm-thick STO capacitors in an area of 20 mm × 20 mm with 9000 TSVs, which corresponds to 2.5 μF/cm^2.

Then, LSIs are bonded onto the wafer with lead-free solder bumps and under-filled with resin, as shown in Fig. 4-2-20. After chip-to-wafer bonding, the LSIs are molded with resin and the wafer is thinned to 50 μm, and consequently, the bottom of Cu-filled cavities appears at the rear surface of the wafer. Finally, Cu pads are patterned on the back of the wafer, lead-free solder bumps are formed, and each LSI/Si interposer stack is obtained by dicing the wafer, as shown in Fig. 4-2-21. This process enables a 50-μm-

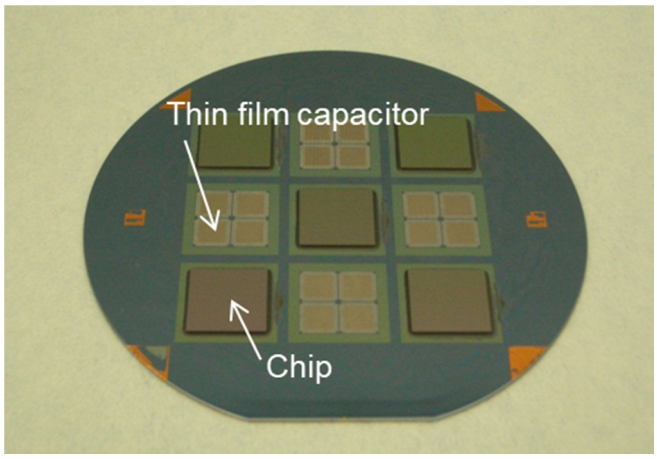

Fig. 4-2-20. Chip-to-wafer bonding.

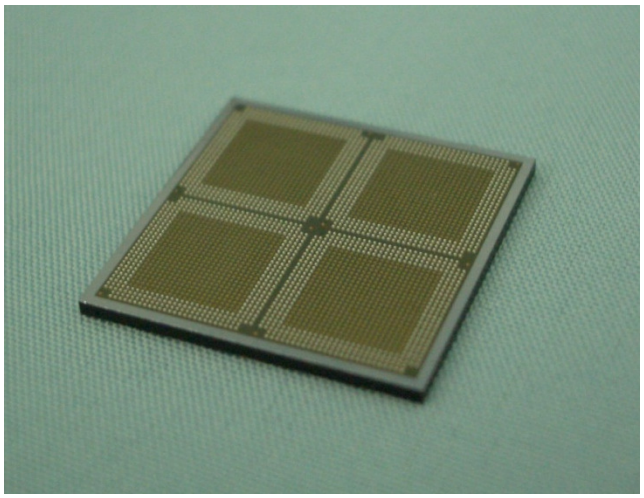

Fig. 4-2-21. Si interposer directly connected to a chip.

thick interposer stacked with an LSI because the molding resin acts as a support during wafer thinning. A short via length of 50 µm will contribute to the reduction in signal propagation delays in the interposer. The LSI/Si interposer stacking structures can be handled as well as bare LSI chips.

Figure 4-2-22 shows bird's-eye and cross-sectional images of an LSI/Si interposer stacking structure on a PCB. The stacking structure was integrated with a 1-µF capacitor. A 50-µm-thick Si interposer was observed between the chip and the board, in other words, a direct connection of the thin film decoupling capacitor to the chip was obtained.

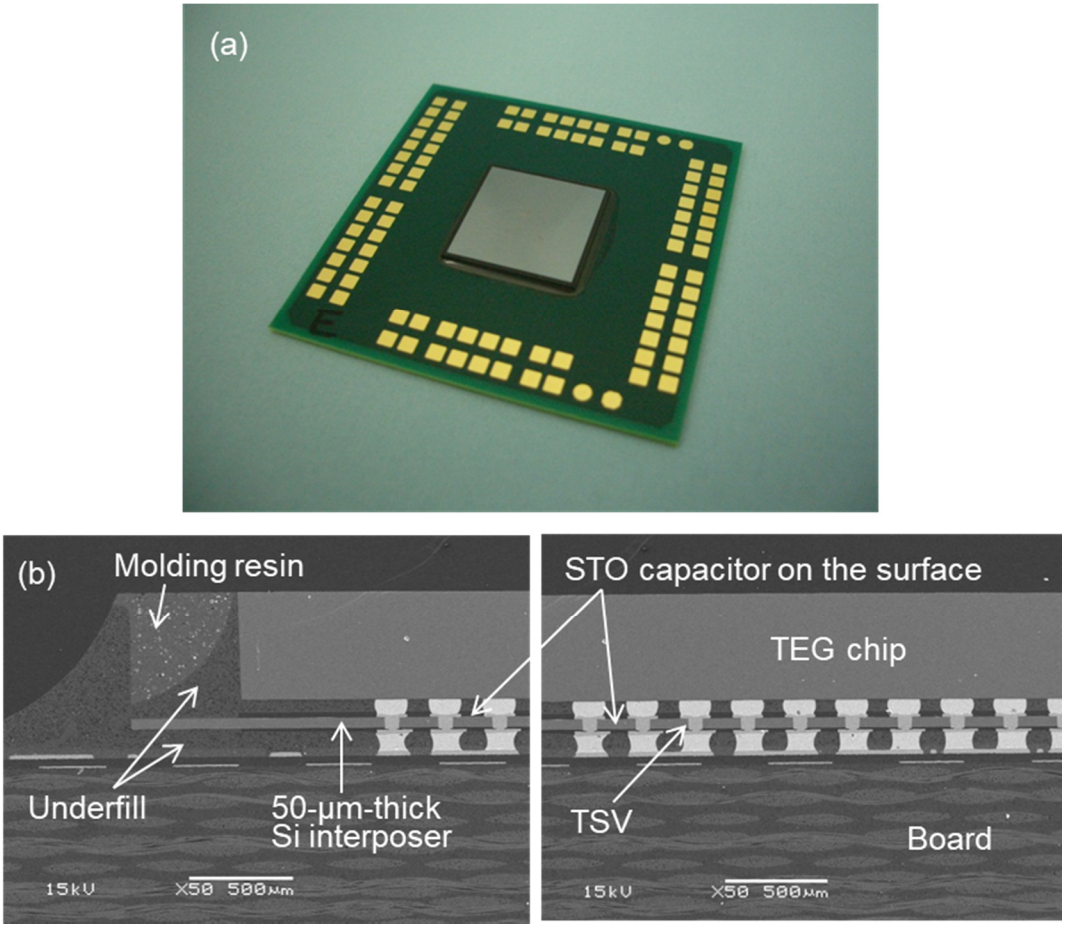

Fig. 4-2-22. (a) Bird's-eye and (b) cross-sectional images of LSI/Si interposer stacking structure on printed circuit board.

Capacitance change during assembly and a thermal cycle test from -40 to 125°C for the LSI/Si interposer stacks are shown in Fig. 4-2-23. The capacitance values were almost constant and did not change even after 1000 cycles of the thermal cycle test. Thus, the Si interposer exhibits sufficient reliability.

Si interposers with high-ε_r STO thin-film capacitors and their stacking process based on chip-to-wafer bonding have been developed. From the viewpoints of dielectric constant, leakage current density and defect density, the STO thin films were sputter-deposited at 400°C on Ru. The stacking process enables the 50-μm-thick Si interposers to be inserted between an LSI and a printed circuit board (an organic interposer).

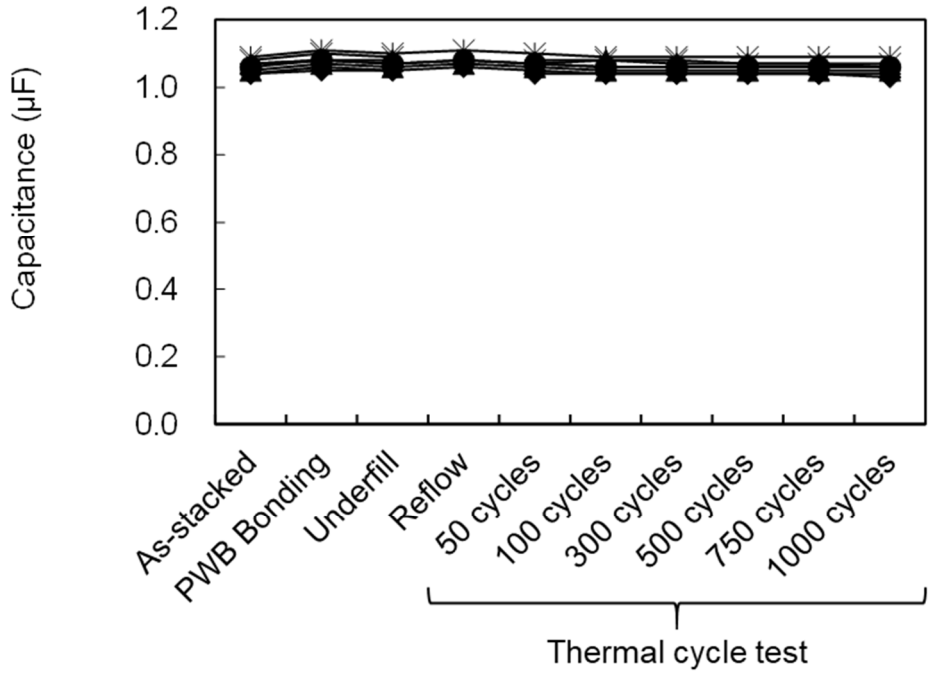

Fig. 4-2-23. Capacitance change during assembly and thermal cycle test for the STO capacitors in the LSI/Si interposer stacking structures.

Maximum capacitance density of 2.5 μF/cm^2 was obtained for 60-nm-thick STO capacitors in an area of 20 mm × 20 mm with 9000 TSVs. Capacitance for the LSI/Si interposer stacks did not change during thermal cycle test up to 1000 cycles.

4-3 Si Interposer for 3D-Stacked Buck Converters [21]

4-3-1 Concept of 3D-stacked buck converter

In addition to the thin film decoupling capacitor, a 3D-stacked buck converter is another part that can help to deal with the power integrity problems in heterogeneously integrated systems. The 3D-stacked buck converter consists of a CMOS LSI that includes

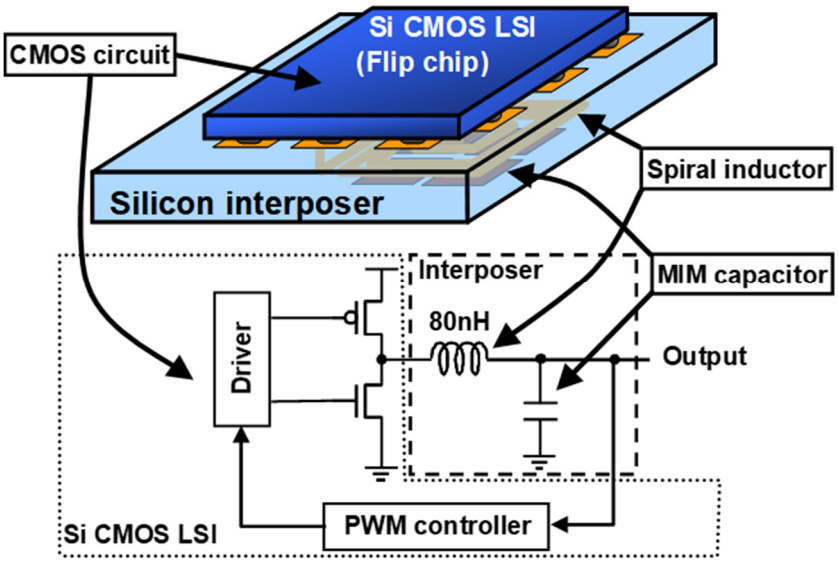

Fig. 4-3-1. Concept of the 3D-stacked buck converter [22].

active components and an output-filter-embedded Si interposer. The conceptual diagram for the 3D-stacked buck converter is shown in Fig. 4-3-1 [22]. The Si LSI has a driver, a pulse width modulation (PWM) controller, and a CMOS switch. The passive components of the buck converter, namely the output filter, composed of a spiral inductor and a metal-insulator-metal (MIM) capacitor, are embedded in the Si interposer. The LSI is mounted on the Si interposer by flip-chip bonding.

High ε_r materials are most suitable for obtaining a large capacitance in a small area because the MIM capacitor must be small and stacked with the inductor to minimize form factor. In this study, $SrTiO_3$ (STO) thin films were used as the capacitor dielectrics. High-density wiring with fine design rules, particularly small spacing, is required to ensure there is a large level of inductance per unit area to minimize the area penalty.

The power efficiency of on-chip buck converters is influenced by inductor properties. Inductor power loss (P_i) is one of the major factors of the power efficiency. The P_i value is given by

$$P_{\mathrm{i}} = \frac{V_{\mathrm{in}} D(1-D)}{2f\left(\frac{L_{\mathrm{i}}}{R_{\mathrm{i}}}\right) I_{\mathrm{R}}}\left({I_{\mathrm{L}}}^2 + \frac{{I_{\mathrm{R}}}^2}{3}\right), \tag{4-8}$$

where V_{in} is the input voltage, D is the duty ratio, f is the switching frequency, I_{R} is the ripple current, and I_{L} is the load current [23]. The ratio of the inductance and parasitic resistance ($L_{\mathrm{i}}/R_{\mathrm{i}}$) is an important parameter of the inductor performance and is determined by the thickness and design rules for the wiring layers. The calculated power efficiency of a buck converter increases with an increase in the $L_{\mathrm{i}}/R_{\mathrm{i}}$ values and metal layer thickness, and the typical wiring layer parameters for improving the power efficiency are 15-μm-thick Cu with a line/space (L/S) value of 20 μm/20 μm [22].

This design rule corresponds to that for printed circuit boards, and the Cu wiring thickness is larger than that for commonly used Si interposers, which is smaller than 5 μm. Therefore, development of thick Cu wiring process on Si wafers and integration of STO thin film capacitors with thick Cu wirings are essential for ensuring there is an improved level of power efficiency and compactness in a 3D stacked buck converter.

4-3-2 Si interposer fabrication with multilayer 15-μm-thick Cu wiring

A multi-layer 15-μm-thick Cu wiring process for obtaining a higher $L_{\mathrm{i}}/R_{\mathrm{i}}$ ratio was developed based on a semi-additive process. A Ti/Cu seed layer, typically Ti(50 nm)/Cu(300nm), is deposited to a substrate by sputtering. A spin-coated photoresist layer is formed by photolithography into a reverse pattern of the wiring pattern. After photolithography, Cu is grown in spaces between photoresist patterns by electroplating. The Cu wiring formation is finished by removing photoresist and etching Cu and Ti layers by NH_3 + H_2O_2 and HNO_3 solutions, respectively. The insulating layer is made of a photosensitive resin. The resin is spin-coated over the Cu wiring layer. Via holes

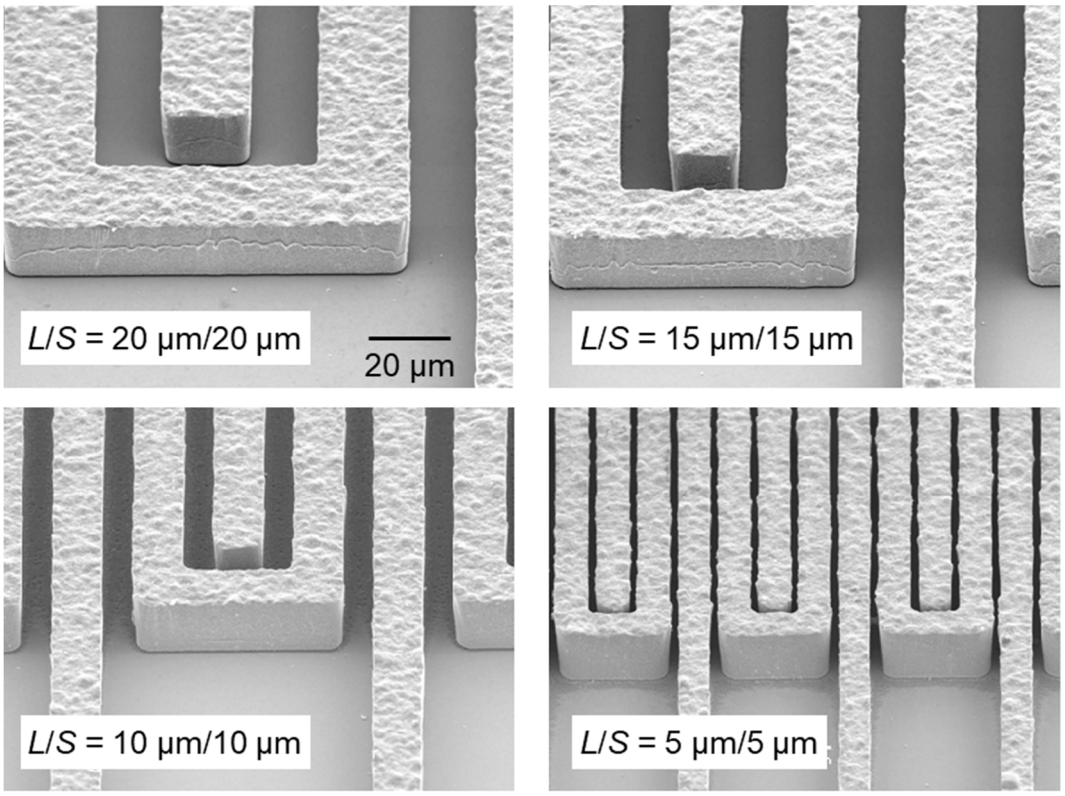

Fig. 4-3-2. Photographs of 20-μm-thick electroplated Cu patterns with various *L*/*S* values.

connecting upper and lower Cu layers are patterned by photolithography. The thickness of a Cu wiring layer fabricated on a Si wafer is usually not more than 5μm because it becomes more difficult to cover the wiring layer with resin.

Thick and fine electroplated Cu patterns were created by optimizing both the exposure and development conditions. Photographs of 20-μm-thick electroplated Cu patterns are shown in Fig. 4-3-2. The *L*/*S* values indicated in the figures are designed values which correspond to the *L*/*S* values of mask patterns. The observed spaces between the line patterns tend to be smaller than the line width. The difference between the observed and designed patterns is estimated from 2 μm to 3 μm, and it does not depend on the *L*/*S* values. These results suggest that photoresist patterns for electroplating were overexposed and/or overdeveloped. The observed space for an *L*/*S* value of 5 μm/5 μm is

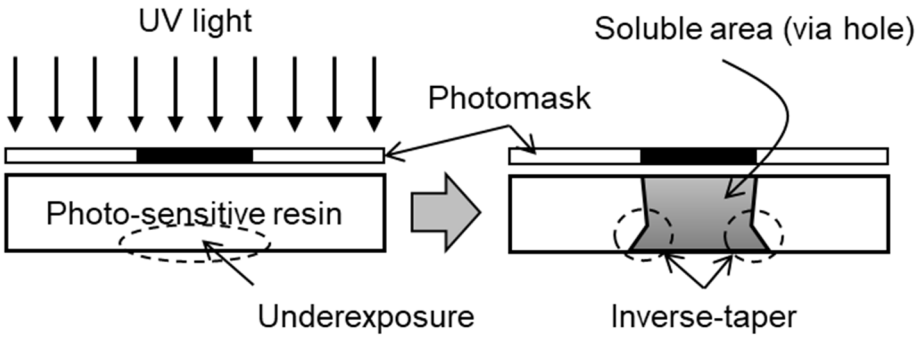

Fig. 4-3-3. Inverse-tapered shape formation in negative-tone resins.

smaller than 3 μm, which seems to be too small to fill the space with interlayer dielectric resin. On the other hand, the obtained patterns for a designed space value of 10 μm or larger will be applicable to multilayer wiring. The designed *L*/*S* value of 20 μm/ 20 μm resulted in about 23 μm/17 μm. Though the difference is believed to be slightly larger than that for 5-μm-thick Cu patterns, the fluctuation of the obtained *L*/*S* values is thought not to have a significant impact on the following analysis. The result is acceptable for the target design rule described above.

Proper patterning of the interlayer dielectrics is another issue for ensuring thick and fine multilayer wiring. The dielectric layer must be thicker than the metal layer, and a high level of sensitivity and high resolution for patterning fine via holes are also required. Photo-sensitive resins are preferable for use as the thick interlayer dielectrics. The bottoms of thick photo-sensitive resins, however, tend to be underexposed, and thus, this often causes open failures. For example, a negative-tone resin can easily be used to form inverse-tapered shapes at the bottom of via holes, as shown in Fig. 4-3-3. This results in open failures because a seed layer in the following electroplating process cannot be deposited onto the side wall at the bottom.

Because there were few commercial positive-tone resins for thick dielectric layers, a chemically-amplified positive-tone resin for covering thick wiring layers was newly

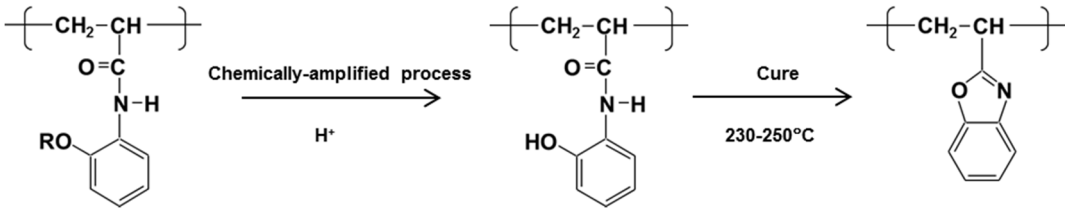

Fig. 4-3-4. Molecular structure and changes by chemically-amplified process and curing for developed photosensitive resin.

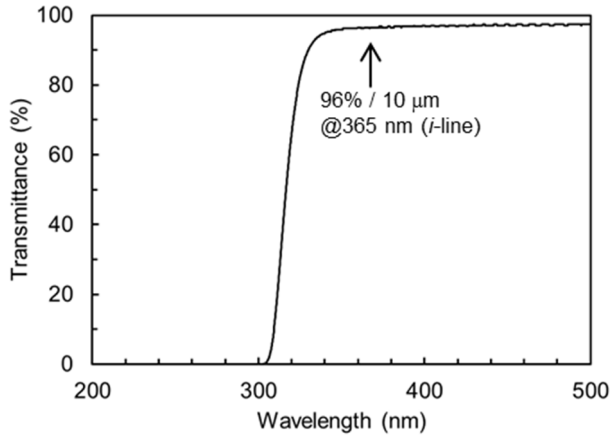

Fig. 4-3-5. Transmittance spectra of the developed resin.

developed to solve this problem. The developed resin is a kind of acrylamide polymer. The molecular structure and reactions of the developed resin are summarized in Fig. 4-3-4. The base resin is sufficiently transparent for the *i*-line, as shown in Fig. 4-3-5. High transparency, chemically-amplified processing during exposure, and positive-tone materials are favorable for avoiding the underexposure at the bottom of the resin and to obtain a higher resolution. The intermediate is alkaline-developable and changes to form a benzoxazole structure at 250°C or lower. This molecular design is suitable for obtaining good insulating properties as well as low curing temperature. Figure 4-3-6 shows that the cured resin is an excellent insulator and high resistance values are maintained even after 2000 h of high temperature and high humidity benchmark test (HHBT). Figures 4-3-7(a) and (b) show a cross-sectional view of the developed resin patterns. The intended

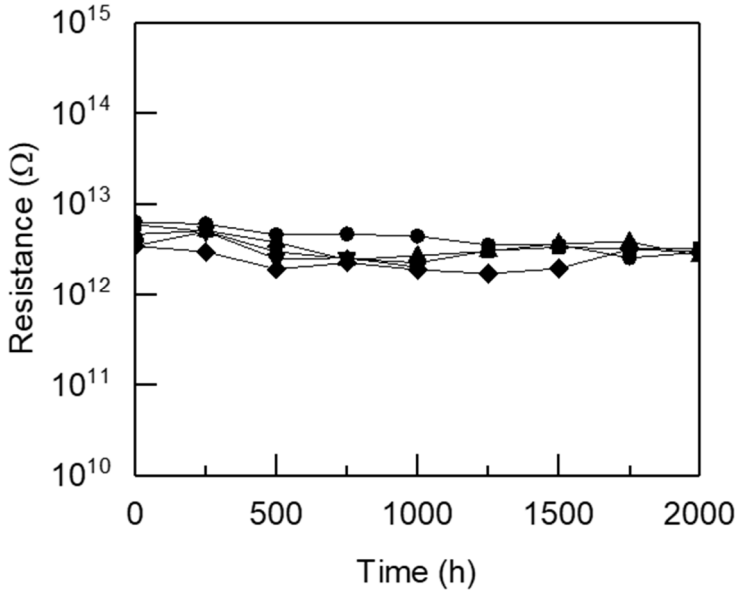

Fig. 4-3-6. Resistance changes in HHBT at 85°C, 85% RH, and 10 V.

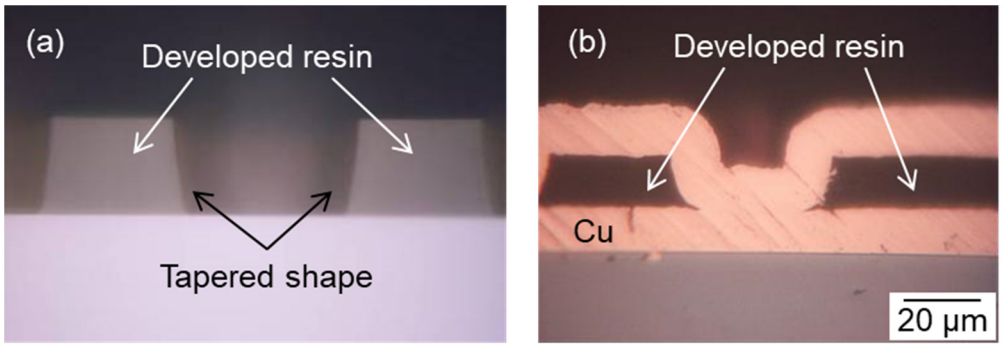

Fig. 4-3-7. Cross-sectional views for improved resin patterns (a) after development and (b) after Cu metallization.

forward-tapered shape and a good interconnection are observed. The minimum via-hole diameter was designed to be 30 μm in the following Si interposer fabrication.

The developed Si interposers for the 3D stacked buck converters have 3 wiring layers and an MIM thin film capacitor. A schematic cross-section of the *LC*-filter-embedded Si interposer is shown in Fig. 4-3-8. The wiring layers use electroplated Cu and are 15-μm thick. Figure 4-3-9 shows the build-up wiring process for the Si interposer. MIM capacitors with 100-nm-thick STO thin film dielectrics and Ru electrodes were formed on a thermally-oxidized Si wafer. The capacitor fabrication process is the same as

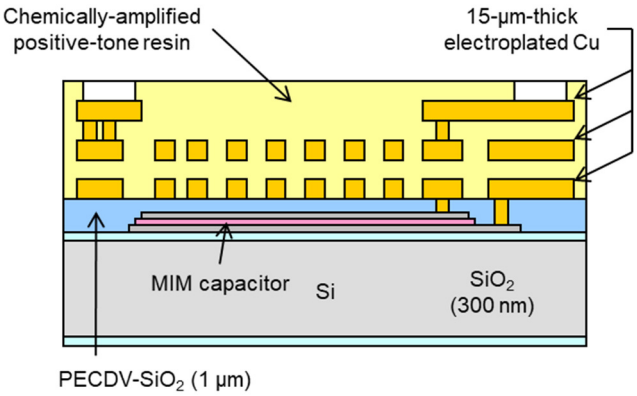

Fig. 4-3-8. Schematic cross-section for *LC*-filter-embedded Si interposer.

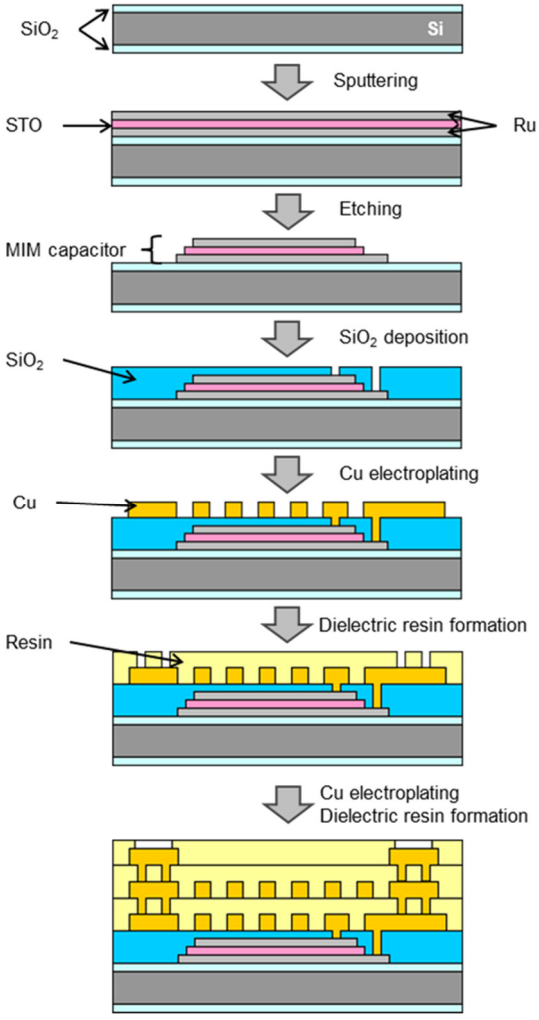

Fig. 4-3-9. Build-up process for Si interposer with MIM capacitor and multi-layer Cu wirings.

that mentioned in Section 4-2. Reactive RF sputtering at 400°C was used to deposit the STO thin films, and DC sputtering was used to deposit the top and bottom electrode layers.

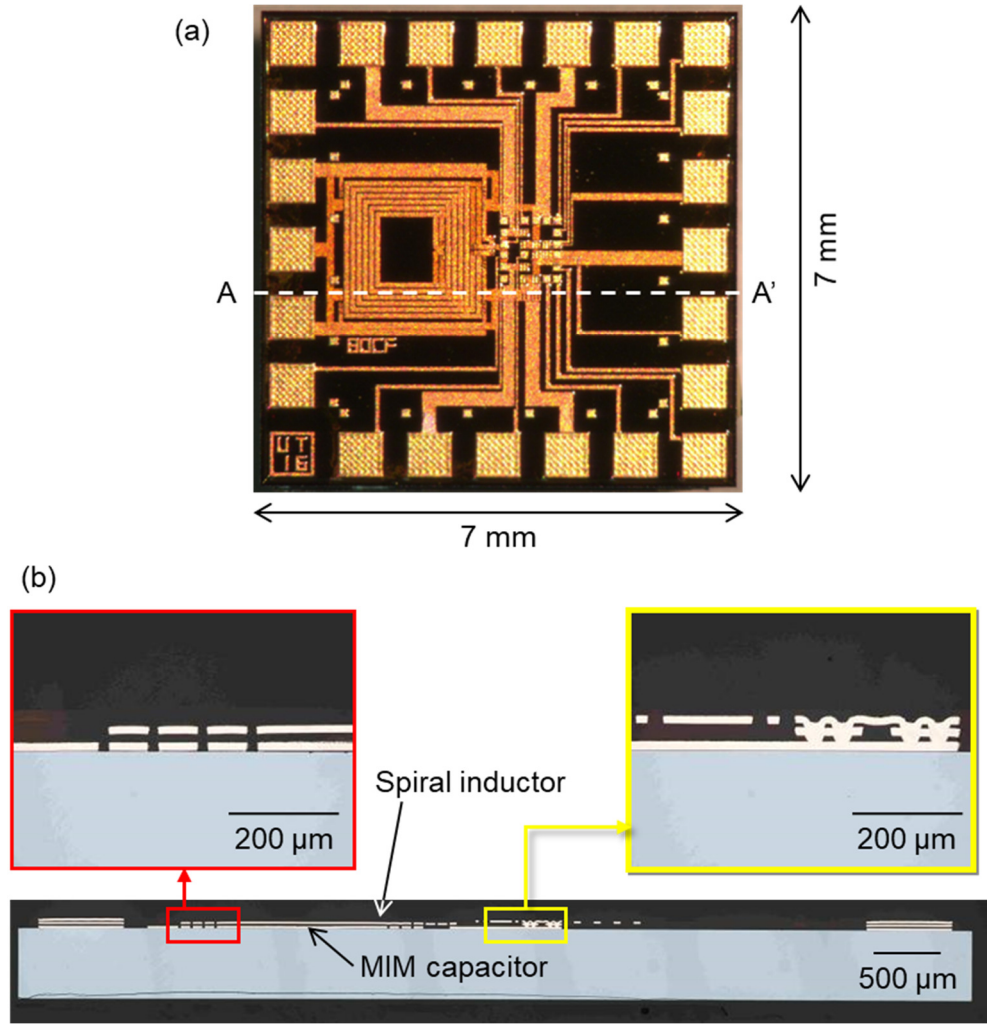

Fig. 4-3-10. Photographs of (a) top view and (b) cross-sectional view at A-A' line for fabricated Si interposer with 15-μm-thick Cu layers.

Each layer in the MIM capacitor was patterned from to down by using ion milling. The capacitance density was higher than 12 nF/mm^2. After covering the MIM capacitor with SiO_2 deposited by using plasma enhanced chemical vapor deposition (PECVD), 15-μm-thick electroplated Cu patterns were formed over the capacitor by using a semi-additive method. The interlayer dielectric resin was spin-coated and then cured at 250°C for 1 h. The dielectric layer thickness was designed to be 20 μm.

The fabricated Si interposers were 7 mm × 7 mm. The minimum *L*/*S* value was 20 μm/20 μm and the via-hole diameter was 30 μm, which is the same as that for

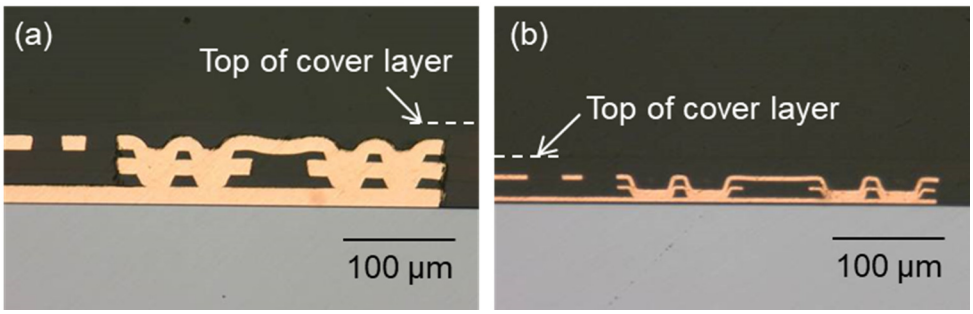

Fig. 4-3-11. Comparison of cross-sectional views for Si interposers with (a) 15- and (b) 5-μm-thick Cu wiring layers.

conventional Si interposers with 5-μm-thick metal layers. Figure 4-3-10(a) shows an example of the top view of the fabricated Si interposer with 15-μm-thick Cu layers. The cross-sectional view at the A-A' line in Fig. 4-3-10(a) is shown in Fig. 4-3-10(b). Cu wiring was used for the spiral inductor in the output filter, and the MIM capacitor was placed right below the spiral inductor. Si interposers with 5-μm-thick wiring layers as well as those with 15-μm-thick wiring layers were also fabricated by using the same photomasks. A comparison of the cross-sectional views for both Si interposers is shown in Fig. 4-3-11. The difference in Cu layer thicknesses is clearly observed.

Figure 4-3-12 shows a comparison of the measured sheet resistance for two kinds of Cu wiring layers. This figure shows that the sheet resistance for the 15-μm-thick Cu layer decreases based on the Cu thickness. The designed sheet resistance values of the 5- and 15-μm-thick Cu are 3.36 mΩ/□ and 1.12 mΩ/□, respectively. The measured values are slightly larger than the designed values due to the film thickness and quality. Distribution of sheet resistance for the 5-μm-thick Cu is larger than that for the 15-μm-thick Cu. The Cu thickness fluctuation is also thought to be causally related to the distribution of the sheet resistance because the thickness fluctuation was controlled within ±1 μm and has more influence to the 5-μm-thick Cu as compared to the 15-μm-thick Cu. The inductance values do not depend on the wiring thickness and are in good agreement

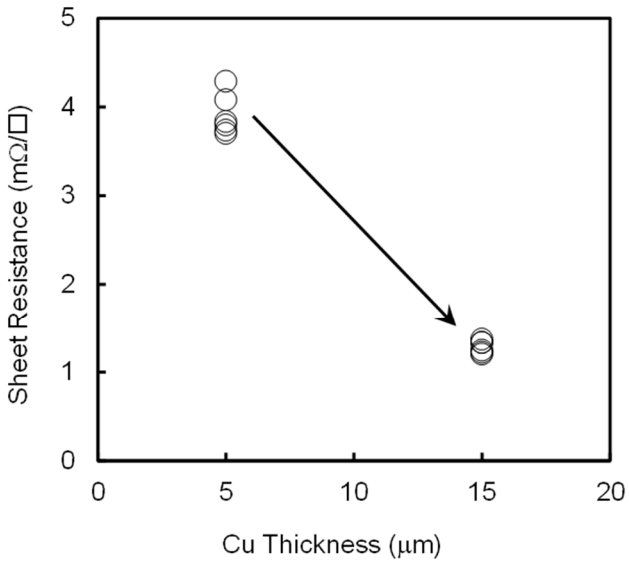

Fig. 4-3-12. Measured sheet resistance for 15- and 5-μm-thick Cu wiring layers.

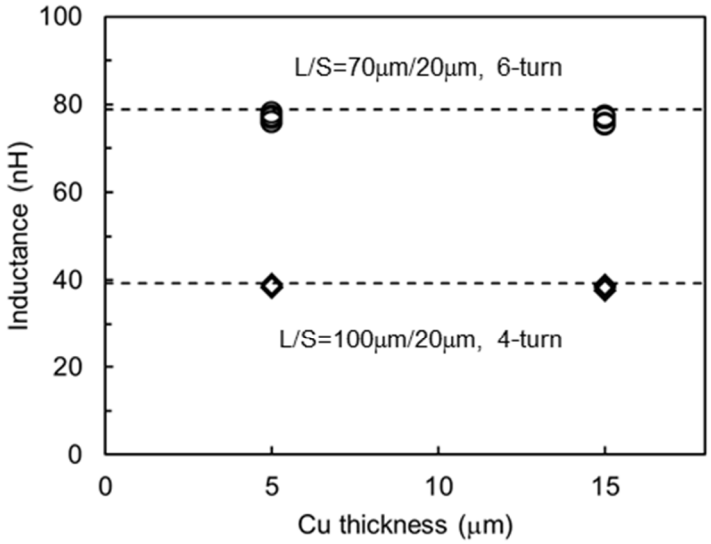

Fig. 4-3-13. Measured and calculated inductance values for various embedded spiral inductors. The dashed lines indicate the calculated inductance by the formulas in Ref. [24]. The outline of the inductors was 2 mm × 2 mm.

with the estimation formula [24], as shown in Fig. 4-3-13.

Figure 4-3-14 shows that the capacitance values for the embedded MIM capacitors under the 5- or 15-μm-thick Cu wiring layers. The measured capacitance values are larger than 22 nF for 1.62 mm^2 and are also independent of the build-up Cu wiring layer

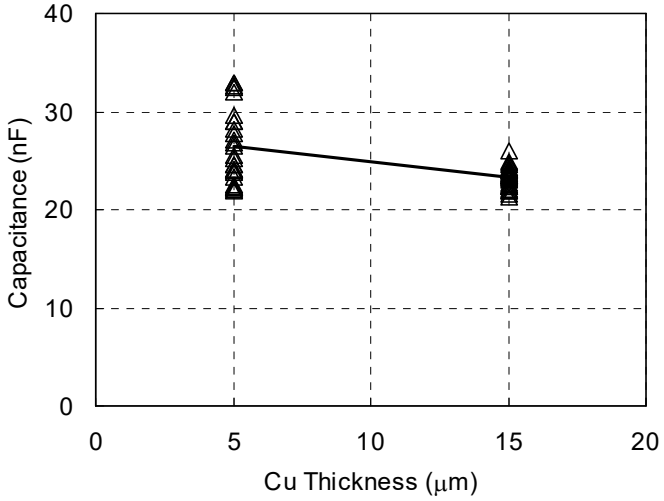

Fig. 4-3-14. Measured capacitance values for embedded STO thin film capacitors beneath 15- or 5-μm-thick wiring layers in fabricated Si interposers. The electrode area was 1.62 mm^2, and the STO thickness was 100 nm.

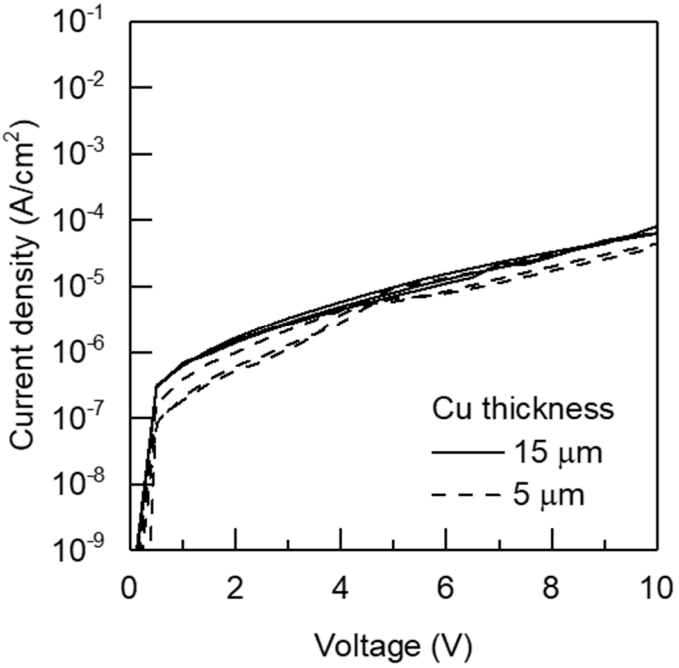

Fig. 4-3-15. Current-voltage curves for embedded STO thin film capacitors after 15- or 5-μm-thick wiring process. The electrode area was 1 mm × 1 mm and the STO thickness was 100 nm.

thickness. Distribution of the capacitance values for the 5-μm-thick Cu is larger than those for the 15-μm-thick Cu though average capacitance values are almost the same. It is mainly due to STO sputtering apparatus applied to each fabrication process. Some

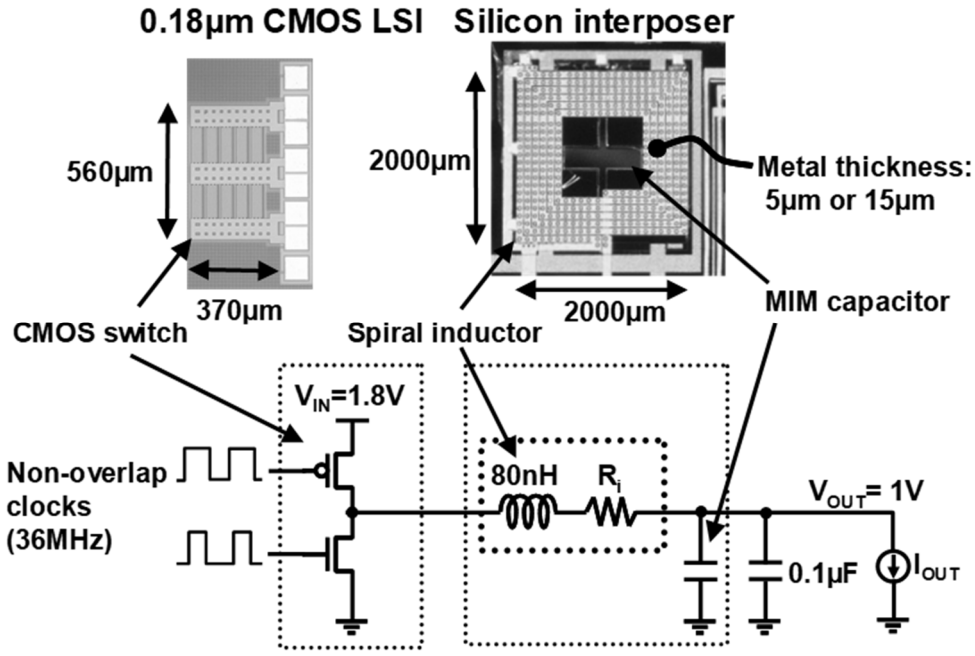

Fig. 4-3-16. Photographs of measured LSI chip and Si interposer, and measurement circuit.

typical current-voltage curves of the STO thin film capacitors after 5- or 15-μm-thick wiring process are shown in Fig. 4-3-15. The leakage current is sufficiently low at the output voltage range for the buck converter. Both the capacitance and leakage current are independent of the Cu thickness suggesting that the Cu wiring fabrication process did not affect the properties of the STO thin film capacitors. Thus, the only difference between the two types of Si interposers is the sheet resistance of the spiral inductors.

4-3-3 Power efficiency evaluation for the 3D-stacked buck converter

The Cu thickness dependence for the power efficiency of the buck converters was evaluated. Photographs of the measured LSI chip and the Si interposer and the measurement circuit are shown in Fig. 4-3-16. The CMOS switch of the buck converter was implemented using a 0.18-μm CMOS process. Si interposers containing both 5- and 15-μm-thick Cu wiring layers were examined in order to compare the performance

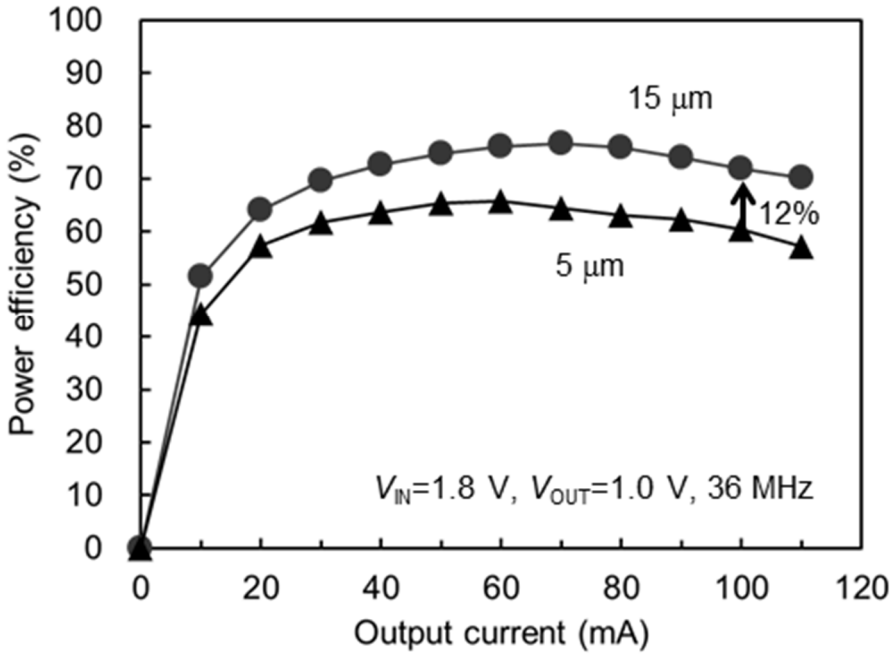

Fig. 4-3-17. Measured power efficiency depending on I_{OUT} for 3D-stacked buck converters.

degradation due to the parasitic resistance of the spiral inductor. A 6-turn square spiral inductor with *L*/*S* values of 70 μm/20 μm in a 2 mm × 2 mm area and an STO thin film capacitor were integrated into the tested Si interposer. The STO thin film capacitor was placed just beneath the spiral inductor. The inductance and parasitic resistance values for the inductor were around 80 nH and 0.6 Ω for 15-μm-thick Cu. 36-MHz non-overlap clocks were applied to the switch for the measurements, and the input voltage was 1.8 V and the output voltage was 1.0 V.

Figure 4-3-17 shows the measured power efficiency depending on the output current (I_{OUT}) of the buck converters. The maximum power efficiency for the buck converter with the 15-μm-thick inductor was 77 % at an I_{OUT} of 70 mA, whereas that with the 5-μm-thick inductor was 66 % at an I_{OUT} of 60 mA. The power efficiency degradation in a low output current range is dominated by parasitic capacitance. In this region, the

difference between the two curves is small. On the other hand, when the I_{OUT} is increased, the difference in the power efficiency tends to increase because the power consumption due to the parasitic resistance becomes dominant. As a result, the 15-μm-thick inductor improves the power efficiency by 12% at an I_{OUT} of 100 mA compared with that of the 5-μm-thick inductor. The power efficiency of the buck converters is not determined by only the parasitic resistance of the inductor but also the parasitic resistance and capacitance of switching transistors. In this study, variation in power efficiency due to the parasitic resistance fluctuation is supposed to be limited within a few percent. Therefore, creating 15-μm-thick Cu wiring makes a significant impact on improving power efficiency.

4-4 Conclusion

Interconnection technology for the perovskite oxide thin film capacitors have been discussed and Si interposers with STO thin film capacitors for power integrity issues have been demonstrated.

A 1.2-μF STO capacitor with 250-μm-pitch multiple contacts showed the ESR values of a few mΩ and the ESL values of less than 10 pH. These values are extremely lower than those for conventional MLCCs. Impedance for the STO-thin-film-capacitor-embedded Si interposer is lower than that for chip-capacitor-surface-mounted and chip-capacitor-embedded organic interposers in a frequency range higher than 100 MHz. Integration process for STO thin film capacitors and TSVs into a Si interposer and stacking process based on via-middle chip-to-wafer bonding have been successfully developed. The developed STO-capacitor-embedded Si interposer passed thermal cycle test.

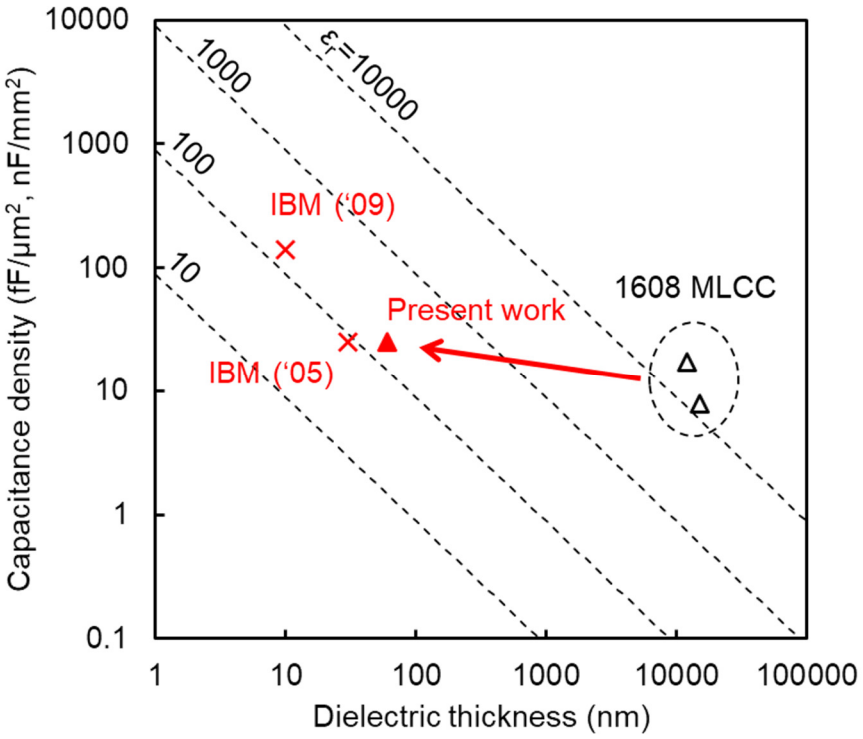

Fig. 4-4-1. Progress in increasing capacitance density by the present study and other decoupling capacitors embedded in a Si interposer.

For the 3D-stacked buck converter application, a Si interposer with a stacked *LC* filter and 15-μm-thick Cu wiring process has been developed. The capacitance value and leakage current for the STO capacitors covered with thick Cu wiring layers did not deteriorate after the wiring process. The 3D-stacked buck converters with the stacked *LC* filter have also been developed. The developed buck converters demonstrated that the 15-μm-thick inductor improved the power efficiency by 12% as compared with that for the 5-μm-thick inductor.

Fig. 4-4-1 summarizes capacitance density for decoupling capacitors embedded in a Si interposer and 1608M MLCCs at the beginning of this study. Thin film capacitors with the capacitance value of larger than 1 μF can be heterogeneously integrated with an LSI by the developed process. In contrast to planar ferroelectric MIM capacitors in this

study, integration of trench-type capacitors into Si interposers has been also developed [13, 25]. It is easy for the trench capacitor to increase effective electrode area, so that the capacitance density for the trench decoupling capacitor is larger than that for the developed STO capacitors. As described in this chapter, control of the ESL and ESR is predominant for the decoupling capacitor applications. The electrical and mechanical design will play a more important part in exploiting capacitor performance.

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Chapter 5
CONCLUSIONS AND FUTURE WORK

5-1 Conclusion

Capacitors play important roles in memory devices and power distribution networks for large-scale integrated circuits (LSIs). Though perovskite-type ferroelectric oxides and related oxides with high dielectric constant (ε) have been promising dielectric materials for the integrated capacitors, processing for their integration into LSIs have not fully drawn out the material properties, and consequently limited practical implementation. In this study, integration technologies for major capacitor applications, including giga-bit (Gbit) dynamic random access memory (DRAM) cell capacitors, ferroelectric non-volatile memory (FeRAM) cell capacitors, and embedded decoupling capacitors, have been developed from the viewpoints of properties of the capacitor dielectric material, intra-connections, and interconnections. The following results were obtained.

Chapter 2 described RuO_2-based storage electrode development. In addition to the difficulty of fine-patterning, Pt does not act as an oxygen diffusion barrier, and consequently, a low ε_r or high resistance layer is formed underneath the Pt layer. Therefore, Pt is not applicable to the storage electrode for Gbit-scale DRAMs. This study found out that RuO_2 was a candidate for the storage electrode material because it was stable for ferroelectric thin film deposition and thick RuO_2 could be patterned by dry etching to make sub-micron patterns. A resistance evaluation method for layered structures by capacitance measurement was demonstrated and applied to the evaluation of properties for various RuO_2/TiN-based structures. Improvement of thermal stability for the

RuO_2/TiN-based electrodes allows the rise of ferroelectric thin film deposition temperature to obtain higher ε_r thin films. As a result, a minimum EOT (equivalent oxide thickness) value of 0.4 nm was obtained for (Ba,Sr)TiO_3 stacked capacitors with a RuO_2/Ru/TiN/$TiSi_2$ storage electrode. The results contributed to the development of 1G and world's first 4G DRAMs [1-5].

Chapter 3 discussed enhancement of reliability for $SrBi_2Ta_2O_9$ (SBT) and Pb-based ferroelectric thin film capacitors from the viewpoint of materials development. Relatively low remanent polarization (P_r) values are regarded as a disadvantage of fatigue-free SBT thin film capacitors for the memory applications. Off-stoichiometric composition, such as with Sr deficiency, excess Bi, and Nb substitution, results in improving crystallinity and consolidation of ferroelectricity and consequently increases the P_r. These off-stoichiometric compositions have been utilized for advanced FeRAM developments [6, 7]. Ferroelectric fatigue, which is the serious ferroelectric degradation phenomena for the FeRAM application, has been revisited with $Pb(Zn_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PZN-PT) single crystals. In this study, the anisotropy of fatigue degradation has been discovered. More specifically, fatigue behavior for PZN-PT single crystals obviously depends on crystal orientation. $[001]_C$-oriented rhombohedral PZN-PT showed no fatigue, whereas $[111]_C$-orientation corresponding to the polarization axis was not fatigue-free. This fatigue anisotropy is associated with an engineered domain structure and is also observed in epitaxial $Pb(Yb_{1/2}Nb_{1/2})O_3$-$PbTiO_3$ thin films. These results suggest that crystal orientation control becomes a new material solution for improving read/write endurance in FeRAM. The fatigue anisotropy has also been found in $Pb(In_{0.5}Nb_{0.5})O_3$-$Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ single crystals [8], epitaxial $BiFeO_3$ films [9], $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ ceramics [10], and $Bi_{3.15}Nb_{0.85}Ti_3O_{12}$ thin films [11].

Chapter 4 described integration process development for Si interposers with $SrTiO_3$

(STO) thin film capacitors for power integrity issues. It was clarified that multi-contact STO thin film capacitors exhibited much smaller ESR (equivalent series resistance) and ESL (equivalent series inductance) values than conventional multi-layer ceramic capacitors. To utilize these properties, an integration process for STO thin film capacitors and TSVs into a Si interposer and a stacking process based on chip-to-wafer bonding were developed. In addition to the capacitor, an *LC*-filter-embedded Si interposer was also developed for novel 3-dimensionally-stacked (3D-stacked) buck converter application. For this application, an integration process of the STO thin film capacitor with a 15-μm-thick Cu wiring was developed to reduce parasitic resistance. The capacitance value and leakage current for the STO capacitors covered with thick Cu wiring layers did not deteriorate after the wiring process. The developed 3D-stacked buck converters demonstrated that the 15-μm-thick inductor improved the power efficiency by 12% as compared with that for a 5-μm-thick inductor.

Integration technologies developed in this study have enabled to enhance the performance of the perovskite oxide thin film capacitors integrated into LSIs. Furthermore, the findings from this study have contributed the subsequent device development. Therefore, it is concluded that three viewpoints are essential for the perovskite oxide thin film capacitor integration.

5-2 Future work

As mentioned in Chapter 1, heterogeneous and 3D integrated systems become common in the Internet of Things (IoT) era. Figure 5-2-1 shows an example of a fully-integrated processing system. Highly-integrated processors and memories are integrated

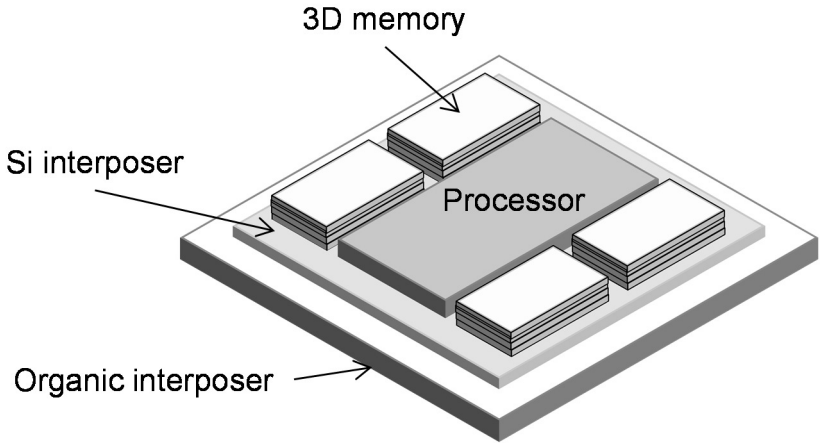

Fig. 5-2-1. Example of a fully-integrated processing system.

on a Si interposer and an organic interposer. Considering such integrated system, the applicability of perovskite oxide thin film capacitors is discussed below.

"More Moore" scaling will continue in the memory applications. Current DRAM design rule is 20 nm or beyond, so that the physical thickness of a dielectric layer has to be less than 10 nm. Because the cell size is 0.0016 μm^2 or smaller, the capacitance per cell area becomes larger than 10000 $fF/\mu m^2$. A ε_r value higher than 10000 is needed when a simple stacked capacitor structure is applied. In practice, ZrO_2, Al_2O_3, and HfO_2 are used as capacitor dielectrics and a high-aspect-ratio cylindrical electrode is used in the current DRAM cells. Recently, application of STO thin dielectric films and Ru-based electrodes has been revisited for DRAM cell capacitors to alleviate process complexity [12-16]. Development of a process for conformal deposition of a very thin STO layer, such as atomic layer deposition, is necessary. However, the application of thin STO films to a DRAM cell will be challenging because the ε_r values of thin STO films will be smaller than 200. Despite great efforts on developing higher density FeRAMs, other non-volatile memories, such as resistive RAM, phase-change RAM, and magnetic RAM, overtook FeRAM from a viewpoint of integration density, as shown in Fig. 1-1-2. Even in a

development phase, the memory capacity and technology node of the FeRAM remain 128M and 130 nm node. Because the cell structure of a 1T1C FeRAM is similar to that of a DRAM, ferroelectric materials used in the FeRAM cell capacitors have to be thinner than 10 nm to achieve the same integration density as the DRAM. Because the minimum thickness for high-quality PZT and SBT thin films is considered to be sub 100 nm, the perovskite oxide thin films are presumed not to be capacitor dielectrics for Gbit-scale FeRAMs. Recently, it has been reported that a doped HfO_2, which has a fluorite structure, shows ferroelectricity [17-19]. Because HfO_2 is compatible with the CMOS process and its ferroelectric phase has a sufficiently large P_r value even when the thickness is 10 nm, HfO_2 has become the most promising candidate for high-density FeRAM cell capacitor material. This material is applicable to a gate oxide. Development of 1T-type cell, therefore, is also expected to enhance integration density. However, the relationship between ferroelectricity and crystal structures and reliability are still unknown though prototype development has already started. Therefore, further studies on ferroelectric properties of HfO_2 will be necessary.

As mentioned above, application of the perovskite oxide thin film capacitor to the future high-density memory cell will be restricted because it seems to be difficult to obtain high-quality 10-nm thick or thinner perovskite oxide thin films. The perovskite oxides consist of at least 3 elements. Precise composition control is generally more difficult than binary compounds. Local composition fluctuation and defects will make more impact on overall properties of thinner films. Sr deficiency in SBT thin films changes inherent ferroelectric properties as described in Chapter 3. This is another aspect of difficulty in composition control. In practice, materials used in CMOS LSI fabrication line are limited to pure metals and semiconductors, and binary oxides and nitrides.

"More than Moore" technologies for heterogeneous integration will become more

suitable for perovskite oxide thin film capacitor applications. Because the perovskite oxide is not deposited onto an LSI in this applications, limitations of processing conditions will be relaxed. Applications do not require thin or fine-patterned shape but properties of perovskite oxides.

Power integrity described in Chapter 4 is becoming more critical. Latest commercial high-end microprocessors are mounted onto decoupling-capacitor-embedded organic interposers [20, 21]. The capacitor dielectric material is $BaTiO_3$ which is sputter-deposited on Ni foil. Because interposer development will proceed further integration and functionalization, a Si interposer is more suitable for use as an integration platform. Though a disadvantage of the Si interposer is production cost, commercial applications of the Si interposer is expanding, particularly in high-end field programmable gate array (FPGA) and graphics processing unit (GPU). Both applications utilize only fine and dense wiring on Si. The next step is thought to be the integration of passive devices. Considering the power integrity applications enabling further integration of the transistors and functionalities into a package, it can be regarded that the perovskite oxide thin film capacitors will contribute to “More Moore” scaling in a broad sense.

Applications of perovskite oxide thin films with metal-oxide-metal (MIM) capacitor structure is not limited to a “capacitor.” Ferroelectric perovskite oxides also have potential applications in piezoelectricity and pyroelectricity. Because these phenomena are also associated with polarization, an MIM structure is necessary for detecting signals and controlling devices. Possible applications of these materials are sensors and actuators for energy saving or energy harvesting, which will be more important in the IoT era. The fabrication process for these oxides is similar to that for capacitors studied, so that findings and guidelines obtained in this study will be applicable.

In order to achieve these “More than Moore” applications, capacitor design will be

an issue for practical development. An integrated capacitor on a Si interposer is not a part of an LSI and discrete capacitors. Design flow and methodology for the capacitor-embedded Si interposer has not been fully established yet. More work on detail analysis of electrical properties for capacitor-embedded Si interposers will be necessary to develop design environment and libraries for the Si interposer.

The MIM capacitor structure is independent of a substrate. Therefore, the MIM capacitor can be formed on glass, polymer or other materials. The recent development of printed transistors enables to realize high performance printed electronics. FeRAM will be suitable for non-volatile memory in printed electronics because ferroelectricity is a bulk phenomenon. From a viewpoint of processing temperature, the conventional deposition techniques, such as sputtering, chemical vapor deposition, and metal-organic decomposition, will not be suitable. Though printed electronics requires low-temperature processing, the deposition temperature for these techniques is generally higher than 400°C. This is because synthesis of a perovskite structure and deposition simultaneously occur in their deposition process. In order to reduce the deposition temperature for a perovskite oxide dielectric layer, the deposition process has to be separate from the synthesis of the oxide. Synthesis of nanocrystalline perovskite oxide particles will expand applications in this field.

Further development of the deposition technique and the capacitor design environment will be necessary for future perovskite oxide thin film capacitor applications. The developed technologies and guidelines obtained from this study will be helpful for integration of perovskite oxide thin film capacitors to enhance LSI performance and expanding their applications to a wide variety of integrated systems.

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APPENDIX

A-1 Evaluation of Parasitic Resistance from *C-f* Measurement

In *C-f* measurement, the measured series capacitance (C_s) and dissipation factor (D) are obtained from the measured complex impedance (Z) by the following equations,

$$C_s = \frac{1}{\omega |X|}, \tag{A-1}$$

$$D = \frac{R}{|X|}, \tag{A-2}$$

where R and X are the series resistance and reactance, *i.e.*, the real and imaginary parts of Z, respectively, and ω is the angular frequency. In a practical capacitor, when an electrode structure with contact plug includes a high resistance region, the device can be regarded as a combination of two capacitors and the equivalent circuit is shown in Fig. A-1. In this case, C_s and D are expressed as follows.

$$C_s = \frac{(1+\omega^2 {C_d}^2 {R_d}^2)(1+\omega^2 {C_e}^2 {R_e}^2)}{\omega^2 \{C_d {R_d}^2 (1+\omega^2 {C_e}^2 {R_e}^2) + C_e {R_e}^2 (1+\omega^2 {C_d}^2 {R_d}^2)\}}, \tag{A-3}$$

$$D = \frac{R_d (1+\omega^2 {C_e}^2 {R_e}^2) + R_e (1+\omega^2 {C_d}^2 {R_d}^2)}{\omega^2 \{C_d {R_d}^2 (1+\omega^2 {C_e}^2 {R_e}^2) + C_e {R_e}^2 (1+\omega^2 {C_d}^2 {R_d}^2)\}}, \tag{A-4}$$

Assuming that a dielectric layer is an ideal insulator, C_s and D are simplified to

$$C_s = \frac{C_d (1+\omega^2 {C_e}^2 {R_e}^2)}{1+\omega^2 C_e {R_e}^2 (C_d + C_e)}, \tag{A-5}$$

$$D = \frac{\omega C_d R_e}{1+\omega^2 C_e {R_e}^2 (C_d + C_e)}, \tag{A-6}$$

and they show the Debye-type dispersion. The frequency dependence of C_s and D is shown in Fig. A-2. The dispersion frequency (ω_0) in C_s ($\omega_{0,C}$) is

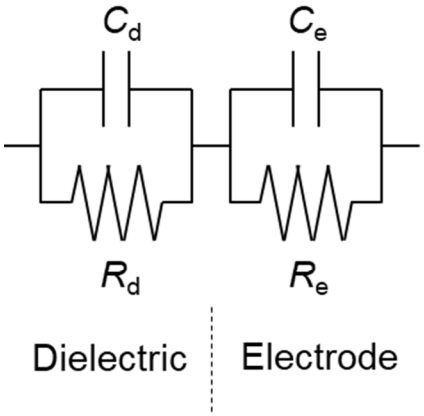

Fig. A-1. Equivalent circuit for a capacitor in series with a high resistance electrode. C_d, R_d, C_e, and R_e stand for the capacitance and resistance of the dielectric and those of the electrode, respectively.

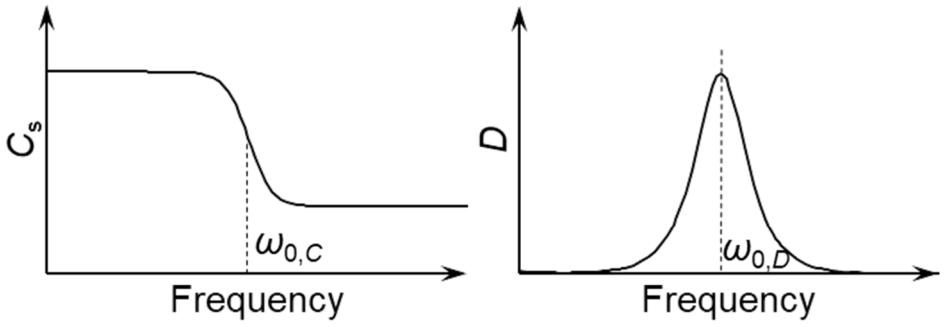

Fig. A-2. Schematic graphs of the frequency dependence of the C_s and D. C_s and D show the Debye-type dispersion. The dispersion frequency decreases with increasing R_e.

$$\omega_{0,C} = \frac{1}{R_e\sqrt{3C_e(C_e + C_d)}}, \tag{A-7}$$

and ω_0 in $D(\omega_{0,D})$ is also

$$\omega_{0,D} = \frac{1}{R_e\sqrt{C_e(C_e + C_d)}}, \tag{A-8}$$

Equations (A-7) and (A-8) show that both $\omega_{0,C}$ and $\omega_{0,D}$ decrease with increasing R_e. With regard to $\omega_{0,C}$, C_s changes as follows.

$$C_s \approx C_d \ (\omega \ll \omega_{0,C}) , \tag{A-9}$$

$$C_s = \frac{1}{\frac{1}{C_d} + \frac{1}{C_e}} \ \left(\omega \gg \omega_{0,C}\right) , \tag{A-10}$$

When a high resistance component is included in the electrode structure, measured C_s and D show dielectric dispersion and absorption in the kHz-MHz range, even though the dielectric layer itself is homogeneous and does not show dielectric dispersion and absorption.

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LIST OF PUBLICATIONS

Refereed papers

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