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博士学位論文

3次元積層チップに向けた超薄Si基板上のCMOSのミックスシグナル及びRF特性の研究

Study of RF and mixed signal performance of CMOS on ultra-thin Si substrate for 3D stacked chips

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Abstract

This thesis describes RF characteristics of CMOS and inductor on ultra-thin Si substrate. 3D stacked integration has been important in order to realize both high-density system in package (SIP) and high functionality with heterogeneous integration of materials and devices. Circuits on thin Si substrate are effective for realizing the SIP with many stacked chips. In this thesis, 0.11 μm CMOS on 1.7 μm Si substrate are examined. I obtained the results of the larger reduction of substrate noise and the minimum of noise figure ($N.F._{min}$) because the penetration of the noise propagating along Psub from Nwell can be reduced. No degradation of 1/*f* noise is observed because of no degradation of D_{it} during thinning process. Additionally, I found g_m and f_T of CMOS have layout dependence because compressive stress occurs in the thin chip. The Q value degradation of inductor caused by the metal under thin chip can be suppressed by 10 nm permalloy film (FeNi) deposition on backside of Si substrate because the film can suppress the penetration of magnetic field into the metal and occurrence of eddy-current.

Any other technologies for high performance of mixed-signal and RF circuits are described. First technology is self-aligned silicide (silicide) process to reduce some parasitic resistance such as gate, source and drain described in chapter 2. This technology has been used since 250 nm technology node. In CMOS on the ultra-thin Si substrate, Co silicide was used because the material was suitable for 130 nm technology because of no degradation of silicide sheet resistance on gate electrode and junction leakage current of drain of CMOS for the technology node. But, I found that Ni silicide is the best material beyond 90 nm technology node because no those degradations occur with scaling of gate electrode and active area. In $TiSi_2$, sheet resistance degradation is observed when gate length is below 1.0 μm. I proposed new test structure to analyze the sheet resistance degradation and I found that an area ratio occupied by C49 phase with higher resistivity than C54 phase with lower resistivity has increased and the thickness of $TiSi_2$ has become thinner with reducing of width of gate line. On the contrary, the slicide thickness has become thicker in $CoSi_2$ and NiSi because moving species is Ti in $TiSi_2$ formation process but that is Co and Ni in $CoSi_2$ and NiSi formation process, respectively. NiSi has merit regarding to junction leakage current because Si consumption is lower comparing with any other silicide.

This merit is significant important as junction depth decreases especially in below 90nm technology node.

In this thesis, characteristics of power amplifier of NMOS with $CoSi_2$ is also described. In general, metal gate is used in order to obtain a higher gain of a power device because a power loss at gate electrode becomes reduced. However, it is difficult to fabricate a short gate length due to the difficulty of the metal gate etching. On the other hand, the short gate length is easily achieved by poly Si RIE etching. Thus, $CoSi_2$ polycide gate with short finger length is suitable for power amplifier with a short gate length and lower gate resistance. In the section 2-3, the results of power gain, output power and power-added efficiency are indicated. In the section 2-4, the combination of $CoSi_2$ and epitaxial Si technology is described. Thanks to T-shape gate electrode formed by selective epitaxial layer on poly Si gate, the gate resistance becomes lower than that $CoSi_2$ polycide gate without epitaxial layer. As a result, higher f_{MAX} is obtained.

Second technology is oxynitride film used as gate insulator to suppress boron penetration from gate electrode into Si substrate in PMOS. NO gas annealing process had been used because this process had been popular to form the oxynitride film in 130 nm technology node. But, I cleared that plasma nitridation process is suitable for mixed signal and RF circuits than the NO gas annealing because of lower flicker noise. In chapter 3, not only the process dependence to fabricate oxynitride film but also the distance dependence between STI edge and gate electrode, gate width dependence and deuterium annealing effect regarding to $1/f$ noise are exhibited.

Next technology is that high resistivity substrate with beyond 500 ohm-cm is used to obtain higher Q Inductor and lower substrate noise. This substrate has, however some issues to be solved for integration with CMOS. Those are slip generation during shallow trench isolation (STI) process, larger leakage current between Nwells, lower snap-back voltage and the larger minimum of noise figure. In order to suppress the slip generation, fully oxygen precipitated wafer is a solution. In order to suppress the larger leakage current and the lower snap-back voltage, additional boron ion implantation under n-well is needed. Additionally, in order to suppress the degradation of the minimum of noise figure, metal shield layer is necessary under pad for input and output signal. In chapter 4, the solution to solve and the measurement results of CMOS on the high resistivity substrate are described in detail.

I believe planar CMOS will been used for mixed-signal and RF circuits because supply voltage of around 1.5-2.5V are suitable for those circuits design and the planar CMOS production cost is lower. On the other hand, aggressive technique have been developed for digital circuit performance. Recently, FinFET has been used for LSI chip production when the gate length is below 30nm because this structure can suppress short channel effect by double gate effect. In chapter 5, RF and mixed-signal characteristics of FinFET are described in order to discuss future mixed signal and RF CMOS. The flicker noise decreases when fin width is below 50 nm with fully depletion mode operation. This result indicates FinFET is suitable for mixed signal circuits with high performance digital circuits. However, RF performance is poor comparing with planar MOSFET because the FinFET has larger parasitic capacitance than planar MOSFET.

In chapter 6, I concluded the results obtained and discussed in this thesis and I described feature of high density 3D stacked chip with many functions. I think the best technology node CMOS depends on the required performance and the production cost. In order to realize some systems with many functions by low production cost, System in Package (SIP) is suitable rather than System on Chip (SOC). Thus 3D stacked chip with ultra-thin substrate has been important and it is necessary to develop the thinner technology and study device performance on the thin Si substrate.

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Chapter 1 Introduction

In RF and analog circuits, CMOS has replace Si and SiGe bipolar device by the gate length scaling. And 3D stacked structure composed of some chips with using thin Si has been proposed in order to realize various functions on a lower height. But the study of RF and mixed signal performance on ultra-thin Si substrate and 3D stacked structure is not sufficient. In this thesis, the detail of the study are described. In this chapter, RF CMOS application and the potential, requirements to RF CMOS and passive elements, purpose and outline of this thesis are described.

1-1. RF CMOS application

Application and market of CMOS has been grown rapidly and widely for these 30 years. At first, the desk-top type personal computer (PC) had been widespread and chips with high speed operation had been technology driver till 1980s. In order to realize the high speed operation of the chip, the scaling of MOSFETs has progressed aggressively. Then, the progress in the semiconductor technology made it possible to offer the note-type mobile PC and the mobile phone instead of the desk-top type at the end of 1980s. In order to satisfy the requirements for the mobile PCs and phones, not only the high-speed operation but also the low-power consumption, the small size of the chip have been required. To satisfy these requirements, the introduction of additional technologies with simple scaling of the MOSFETs were necessary. For example, the salicide technology has been used for the reduction of parasitic resistances of the MOSFET and the lower-k materials than SiO_2 have been introduced to the inter-layer of some interconnects to reduce the wiring capacitances. Recently, high-k materials as the gate insulator have been used for the reduction of the gate leakage current.

Regarding the RF front-end circuits for the mobile phones and PCs, traditionally, compound semiconductor devices such as III-V and Si or SiGe bipolar junction devices (BJT) have been used because of its superiority in high frequency (RF) operation. However, high frequency performance of the CMOS transistors cached up that of compound and bipolar devices by scaling of the gate length of the MOSFETs [1-6]. Moreover CMOS has advantages in production cost and integration with base-band and

logic CMOS circuits. RF CMOS has already used for Bluetooth (2.4 GHz operation [7-23]) and WLAN (2.4 and 5 GHz operation [24-39]) for mobile communications with micro-wave. And these are used in various system such as smartphone, PC, CAR and so on. In future, it will be possible to design millimeter-wave application chips by using scaled CMOS device [40-43].

For the mixed-signal and RF operation of CMOS transistors, there are additional requirements about the electrical characteristics more than those required to the digital circuit applications. Especially, RF circuits are sensitive to the various kinds of the noise such as thermal, shot and flicker noise. Furthermore, RF circuits desiners require high accuracy modeling and high performance operation of not only transistor but also passive elements such as resistors, capacitors and inductors. For example, inductor with high Q is extremely important for voltage controlled oscillator (VCO) with low power and low phase noise [49-53].

1-2. Potential of RF CMOS

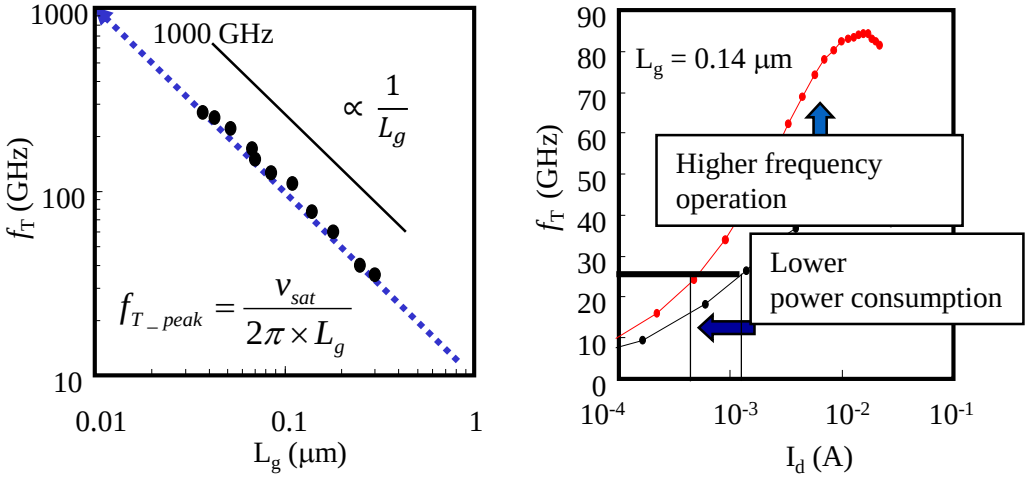


Figure 1-1. Gate length dependence of f_T for NMOS.

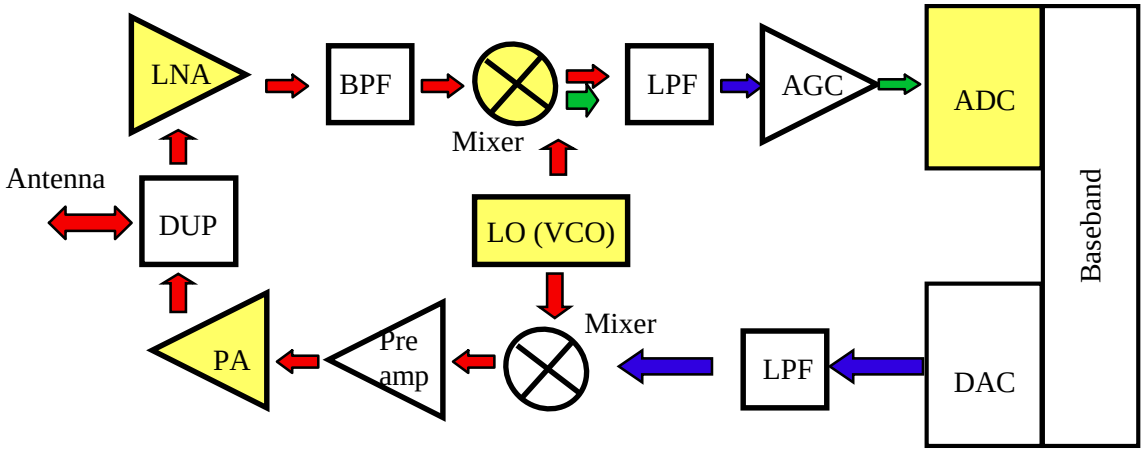


Figure 1-2. Block diagram of telecommunication system.

Figure 1-1 shows the relationship between the maximum value of f_T and the gate length. The f_T value increases with almost inverse proportional to the gate length and the f_T value will reach almost 1.0 THz when the gate length of 10 nm. As a result, application of CMOS is not only micro-wave but also millimeter-wave systems. The radar system with the wave of 77 GHz is useful for safety system of automobile and WLAN with the wave of 60GHz can realize higher translation rate. RF CMOS are necessary in this system because the cost of millimeter wave system must be reduced in order to go into actual use. In ISSCC 2004, Intel reported 64 GHz and 100 GHz VCO circuits by using 90 nm technology CMOS. This report shows CMOS has a great potential for RF circuits in operation in millimeter wave region.

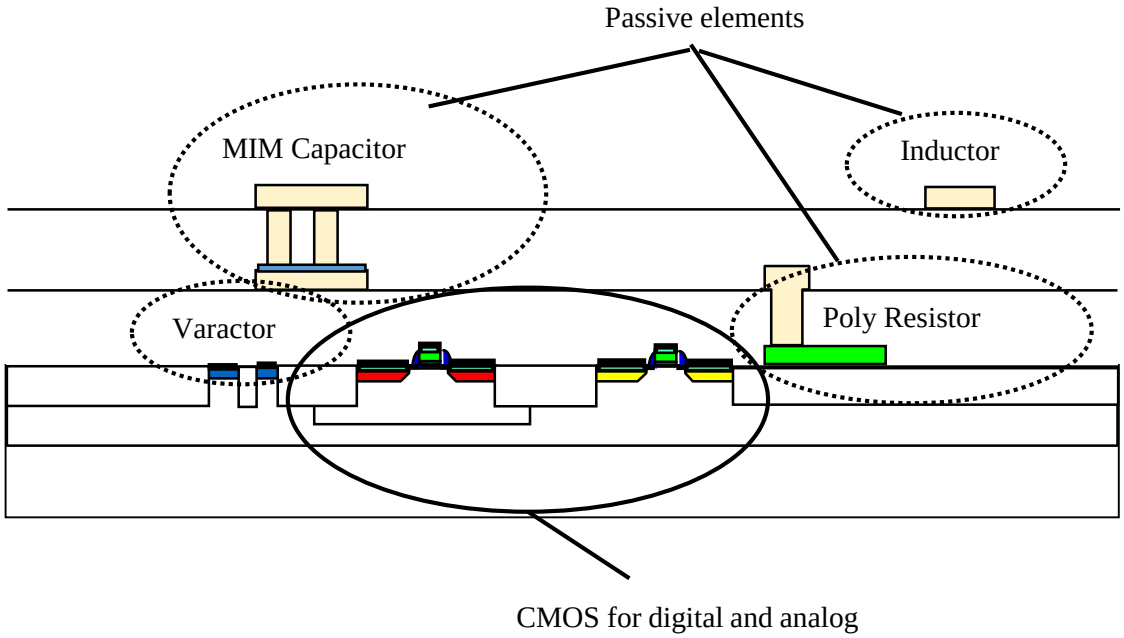


Figure 1-3. Cross sectional view of RF CMOS device.

The other merit of scaling RF CMOS is realization of low power consumption of RF circuit. For example, Operation current at L_g = 0.14 μm NMOS is 70 % lower than that at L_g = 0.25 μm when the f_T is 25 GHz as shown in Fig. 1-1. Figure 1-2 shows block diagrams of telecommunication. Basically this system consists of RF block -- such as low noise amplifier (LNA), Mixer, voltage controlled oscillator (VCO) and power amplifier (PA) -- and low frequency block -- such as analog-digital converter (ADC). In circuit block of receiving the signal, LNA amplifies the signal received from the antenna, and down-conversion from the high frequency (GHz) to an intermediate frequency (a few MHz) or a low frequency (a few KHz) is carried out by the mixer circuit. The down converted signal is changed from analog to digital by analog – digital converter (ADC). After that, digital signal can be processed in baseband circuits. In circuit block of sending the signal, the digital signal in the base-band block is changed to the analog signal by the digital – analog converter (DAC). Then, the signal is up converted to the high frequency and is amplified by the power amplifier (PA). Finally, the signal is transmitted from the antenna.

Since 2000, the PA has been integrated with front-end circuits because digital circuit can control signal distortion whose characteristics of MOSFET is poorer than bipolar and III-V compound semiconductor devices [54-60].

Figure 1-3 shows cross-sectional view of RF CMOS. Basically, CMOS has developed for not mixed-signal and RF but digital circuit because digital market has been huge compared with mixed-signal and RF market. Thus because the production cost has decreases, it is possible to realize mixed-signal and RF embedded digital function with lower cost when older generation CMOS technology are used. Because the depreciation for new equipment to product the mixed-signal and RF CMOS is not needed. Basically, low cost mixed-signal and RF CMOS circuits are realizing by adding some passive elements to older generation. For example poly Si resistor and MIM capacitor are added for mixed-signal circuit design. Additionally, some variable capacitor (varactor) and inductor are added for RF circuit design.

Higher g_m is the most important for mixed-signal and RF circuits. As the operation frequency increases, the gain is determined not only by g_m but also by the input capacitance such as intrinsic and overlap capacitances of the gate electrode. Any blocks of analog circuit are sensitive to noise, which is different from the digital circuit cases. In the digital circuits, "0" and "1" discrete signals are used in logic operation. Unless there is large noise, the "0" can not be changed to "1". On the other hand, in the analog circuits, the phase, frequency and amplitude of the signal themselves are the key elements of the analog signal and these are affected by the noise easily. For example, the $1/f$ noise degrades ADC and VCO circuits. The thermal and RF noise degrades LNA circuit. Therefore, MOSFETs with higher g_m, low input capacitance and low noise are necessary in order to obtain mixed-signal and RF circuits with high performance.

1-3. History of RF CMOS

$$I_d = \frac{\mu\, C_{ox}}{2}\frac{W_g}{L_g}\left(V_g - V_{th}\right)^2 \quad \Rightarrow \quad \frac{g_m}{I_d} = \frac{2}{V_g - V_{th}} = 10 \quad (@\ V_g - V_{th} = 0.2\ V)$$

$$g_m = \frac{\partial I_d}{\partial V_g} = \mu\, C_{ox}\frac{W_g}{L_g}\left(V_g - V_{th}\right)$$

$$I_c = I_s\left(\exp\left(\frac{qV_{BE}}{nkT}\right) - 1\right) \quad \Rightarrow \quad \frac{g_m}{I_c} = \frac{q}{nkT} = 39$$

$$g_m = \frac{\partial I_c}{\partial V_{BE}} = \frac{q}{nkT} I_s\left(\exp\left(\frac{qV_{BE}}{nkT}\right) - 1\right)$$

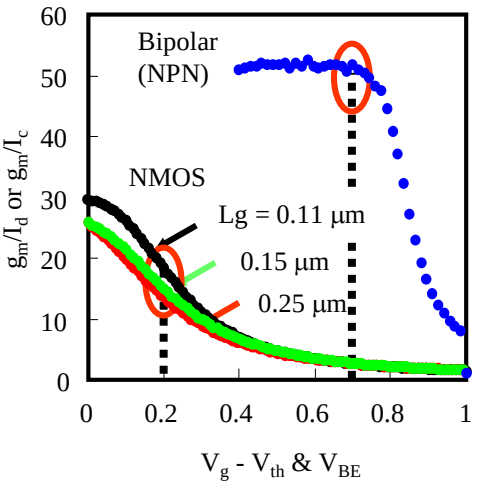


Figure 1-4. g_m/I_c of NPN bipolar device and g_m/I_d of NMOSFET.

Table 1-1. Mixed-signal and RF performances in advanced technology for digital CMOS. ↑ and ↓ represent improvement and degradation of characteristics of MOSFET.

	Small L_g	Halo I/I	Thin EOT	High K	stress	Metal gate
V_d	↓	-	↓	-	-	-
g_m	↑	↑	↑	↑	↑	↑
g_m/I_d	-	-	-	-	-	-
R_{out}	↓	↓	-	-	-	-
$g_m \times R_{out}$	↓	↓	-	-	-	-
V_{th} matching	↓	↓	↑	↑	-	↑
1/*f* noise	↓	↓	↑	↓	-	↑
f_T	↑	↑	-	↑	↑	↑
f_{MAX}	↑	↑	-	↑	↑	↑
RF noise	↑	↑	↑	↑	↑	↑

Figure 1-1-4 shows g_m/I_c of NPN bipolar device and g_m/I_d of NMOSFET. In order to realize low power consumption mixed-signal circuit, higher g_m/I_c or g_m/I_d is necessary. As shown in this figure, bipolar device is suitable for lower power consumption and the g_m/I_d of MOSFET is not improved by gate length scaling. On the other hand, scaling MOSFET is useful to realize low power RF circuits because f_T/Id becomes higher by the gate length Table 1-1 shows mixed-signal and RF performances in advanced technology for digital CMOS. In order to realize advanced CMOS with scaled gate length, halo ion implantation, thinner effective gate oxide thickness (EOT), high K gate insulator to reduce gate leakage current, stress engineering to increase carrier mobility and metal gate to suppress depletion of gate electrode are introduced to advanced CMOS.

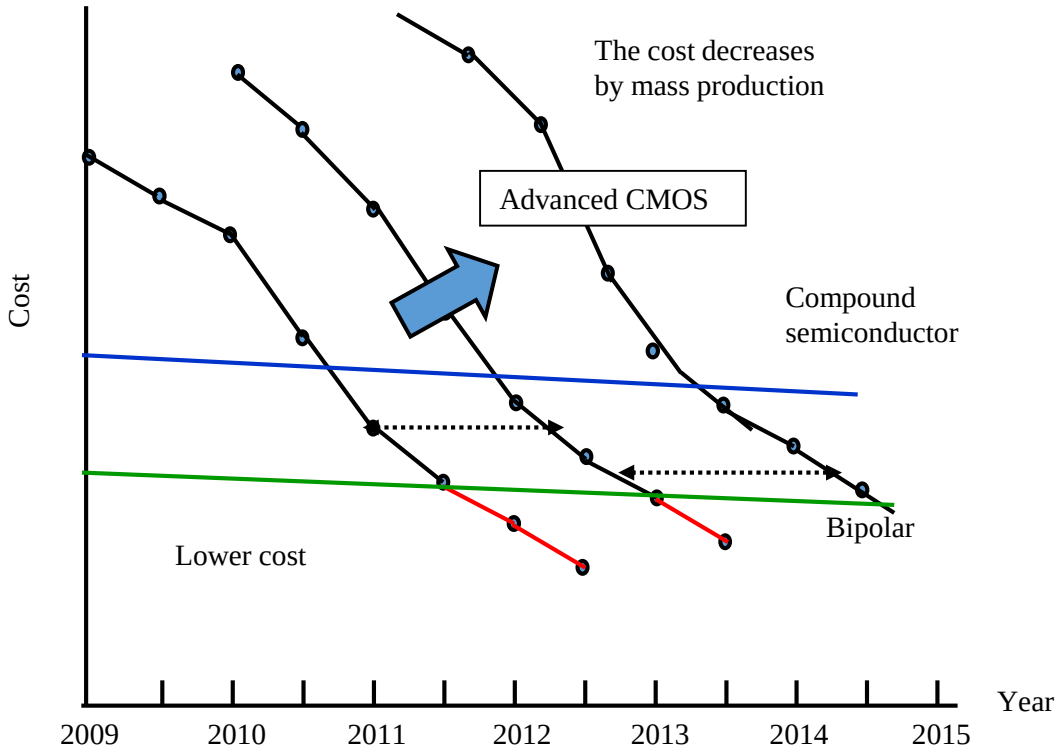


Figure 1-5. Change of production cost of advanced CMOS

As show in Table 1-1, gm, f_T, f_{MAX} and RF noise improve while supply voltage decreases and R_{out} degrades. These mean advanced CMOS is attractive for RF circuit but is not for mixed-signal circuit. However, the production cost of CMOS abruptly decreases in a few years because the advanced CMOS application has spread. As a result, CMOS has attractive for mixed-signal and RF circuits fabricated in a same chip. Thus, mixed-signal and RF circuits by CMOS continue to develop for long time.

In 1998, Bluetooth SIG was established by Ericson, Intel, IBM, Nokia and Toshiba to design Bluetooth for short-range communication (about 10-100 m). That can be realized by 0.25 μm gate length NMOS because the NMOS has f_T of 40 GHz and the f_T is sufficient to design the Bluetooth with operation frequency of 2.4 GHz. (In general, at least f_T of 10 times operation frequency is needed.) So far, RF circuits mainly had been designed by compound semiconductor and bipolar device because f_T of MOSFET is lower compared with those devices. But by scaling of gate length, f_T has been increased and became 40 GHz at L_g = 0.25 μm as shown in Fig.1-1. Additionally, system on chip with RF, mixed-signal and digital function can be realized. This was attractive for lower cost system and smaller chip size.

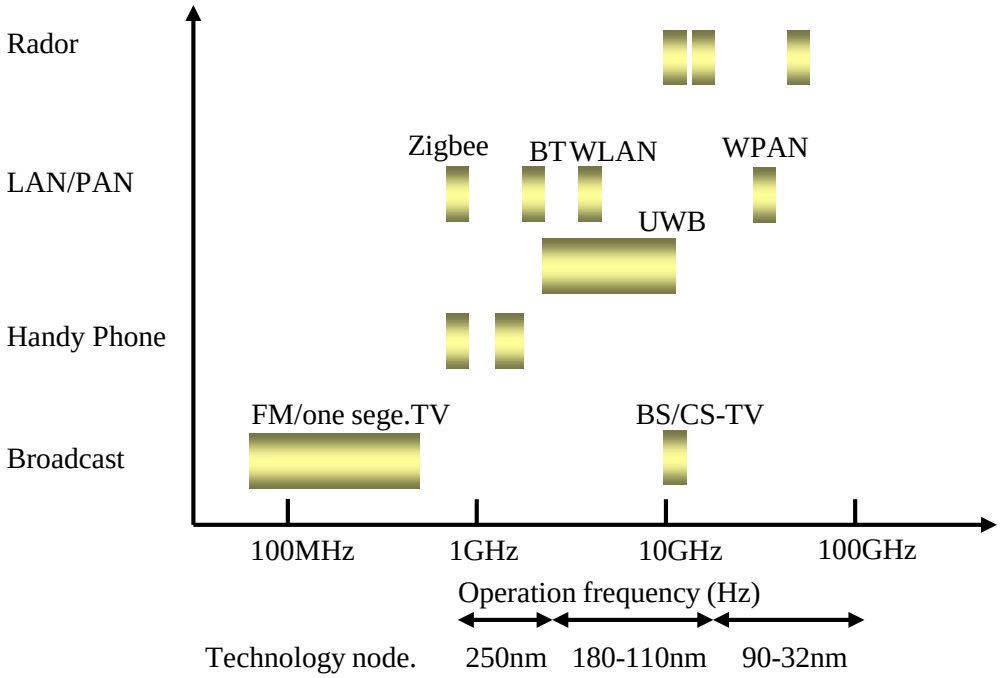


Figure 1-6. Relationship between RF system and technology node of CMOS.

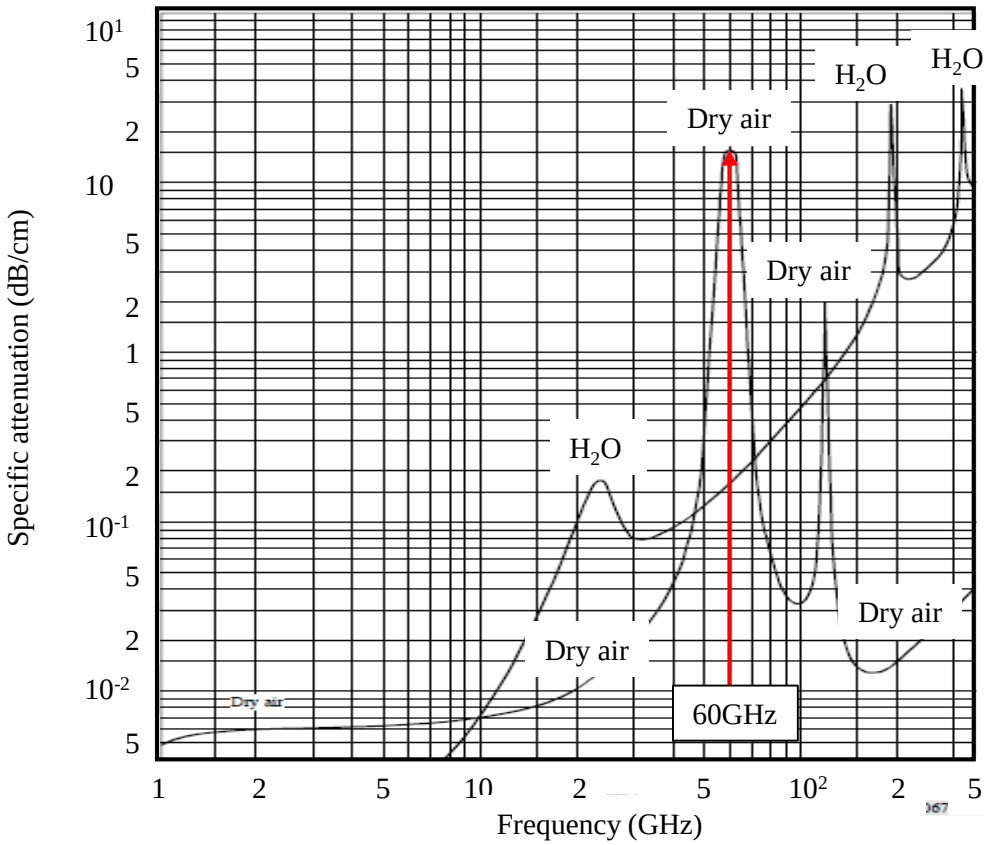


Figure 1-7. Dependence of Attenuation coefficient on operation frequency.

The Bluetooth has been used for various system such as WLAN, Car navigation, Digital audio player, Wireless headphone, printer, keyboard and mouse and so on. In 2001, Atheros Communications announced a production chip for 5 GHz WLAN designed by CMOS. I was surprised at the news because the discussion about "which CMOS and bipolar is better" was continued in those days in Japan. The one of issues of RF circuit design by CMOS is supply voltage. In CMOS, not only gate length but also supply voltage must be scaled in order to obtain higher f_T and f_{MAX}. On the contrary, it is difficult to design under low supply voltage because cascade connection is used in RF circuit. Thus, it was considered the scaling MOSFET was not suitable for higher frequency operation such as 5 GHz operation. By many designer efforts, scaled MOSFET has been used for RF circuits. Figure 1-6 shows relationship between RF system and technology node of CMOS. Transmission speed depends on the system and the operation frequency. In order to realize the higher speed, higher operation frequency is useful because that has wider band width. With progress of technology node, operation frequency has increased by increasing the f_T and fmax. Beyond 90 nm technology node, mm-wave application has been examined. However, the attenuation coefficient increases with the operation frequency as shown in Figure 1-7 [61]. Especially, that at 60 GHz is extreme higher. This result meanss long distance transmission is difficult even if higher speed transmission. Thus near field transmission is suitable for millimeter wave application with 60 GHz.

1-1-4. Requirements to RF CMOS and passive elements

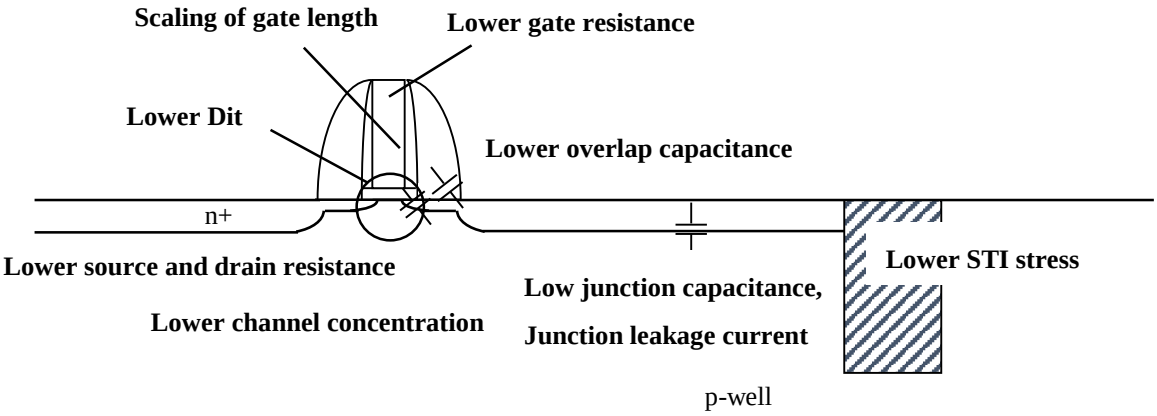


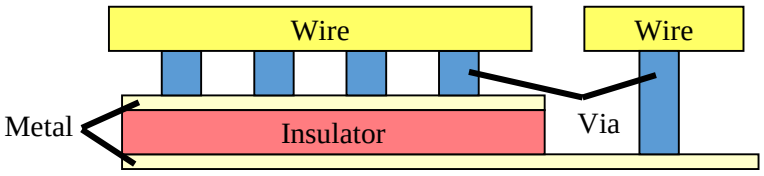
Figure 1-8. Requirements to RF CMOS for high performance RF circuits.

Table 1-2. Dependence of mixed-signal and RF performances on device parameter and characteristics of MOSFET. ↑ and ↓ represent improvement and degradation with device parameter and characteristics of MOSFET.

Device parameter and characteristics of MOSFET	f_T	f_{MAX}	1/f noise	RF noise	V_{th} matching	Low power
Scaling of gate length	↑	↑	↑	↑	↓	↑
Lower gate resistance		↑		↑		↑
Lower source and drain resistance	↑	↑		↑		↑
Lower channel concentration	↑	↑	↑	↑	↑	↑
Lower D_{it}	↑	↑	↑			
Lower overlap capacitance	↑	↑				↑
Low junction capacitance		↑				↑
Low gate and sub. capacitance						↑
Low junction leakage current						↑
Lower STI stress			↑			

Figure 1-8 shows parasitic components of CMOS device. These components degrade CMOS performance for digital and mixed-signal and RF circuits. Influence of the parasitic elements on digital and analog circuits operation is described below.

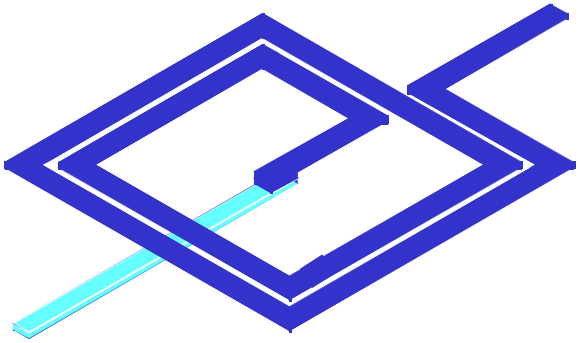
In digital devices, the gate length has to be smaller in order to achieve high drivability. However, when reducing the gate length, the drivability of the MOSFET deviates from the trend due to increases the parasitic resistance of shallower source and drain. Higher channel concentration and interface state density also degrade the carrier mobility because that degrade due to the impurity and surface scatterings. In order to achieve high-speed operation, parasitic capacitances have to be also reduced. The parasitic capacitances of MOSFETs indicate junction capacitance of source and drain, overlap capacitance between gate and drain, fringe capacitance between gate and drain and between gate and Si substrate. The gate resistance also degrades the operation speed. In mixed-signal and RF device, the gate length has to be smaller in order to achieve high transconductance (g_m), high cut-off frequency (f_T), high power gain and low noise figure.



1) High capacitance per unit area
2) Low leakage current
3) Good matching
4) Low voltage coefficient
5) Low temperature coefficient

Figure 1-9. Requirements to MIM capacitor.

However, these RF performances also degrade by the parasitic resistance of source and drain, higher channel concentration and interface state density as well as digital devices. Additionally, the higher channel concentration also degrades the uniformity of the pair transistor characteristics. Matching of the pair transistor characteristics is very important in mixed-signal and RF circuits. In order to achieve high frequency operation, parasitic capacitances must be reduced. The gate resistance also degrades f_{MAX} and noise figure because the input power is consumed and the thermal noise is generated due to the gate resistance. The lower interface state density at the gate insulator and Si substrate is important for reducing of low frequency noise (1/f noise). Thus, basically, the parasitic elements on the digital also degrade performance of mixed-signal and RF circuits . Moreover because mixed-signal and RF circuits are much more sensitive to noise such as flicker noise compared with the digital circuits, lower interface-state density than that digital circuits is required. Digital circuits with low power consumption are sensitive to leakage current at off state. For the sake of lower off leakage current, the threshold voltage, V_{th}, of the MOSFETs can not be decreased too much in the digital case. However, in mixed-signal and RF circuits, off leakage current is not serious problem for many cases because other MOSFET with higher V_{th} is cut the off leakage current when the system is not operated. The lower V_{th} has good advantage for achieving the larger dynamic range in mixed-signal and RF circuits under lower supply voltage operation. For digital circuits, the passive elements are not important except capacitor or resistor used in a memory or resistor and ESD circuit at I/O part. On the other hand, these elements are quite important for mixed-signal and RF circuits.



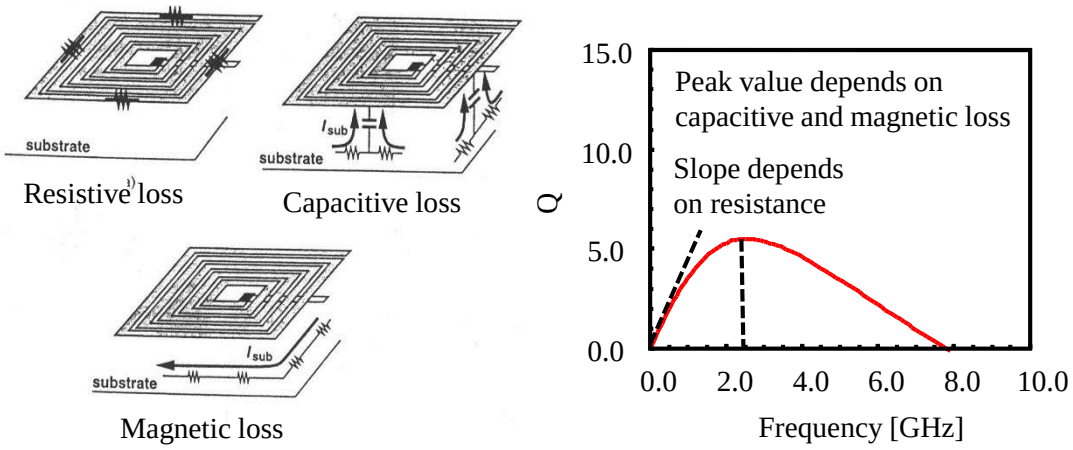
1. Inductor value is determined by outer length and number of turns.
2. Resonance frequency is determined by capacitance between inductor and Si substrate.

: High Q value at operation frequency

: High oscillation frequency

: Larger inductance value per unit area

Figure. 1-10. Requirements to Inductor.



1. Resistive loss → Thicker metal, low resistivity metal
2. Capacitive loss → Low e interlayer, air wire
3. Magnetic loss → High resistivity substrate, poly shield

Figure 1-11. Frequency dependence of Q value of inductor.

Figure 1-9 shows schematic cross sectional view of metal-insulator-metal (MIM) capacitor. The requirements to the MIM capacitor are high capacitance value per unit area, low leakage current, good matching, low voltage coefficient and low temperature coefficient. The component is introduced between M3 and M4 which is called as metal on metal (MOM) capacitor. Recently, the capacitor between wires has been used due to requirement of lower cost.

Figure 1-10 shows schematic cross sectional view of inductor. The requirements to the inductor are higher Q value at the operation frequency, high oscillation frequency and larger inductance value per unit area. Stacked structure by any layers of wire or bonding wire for packaging are used in order to reduce parasitic resistance of inductor. .

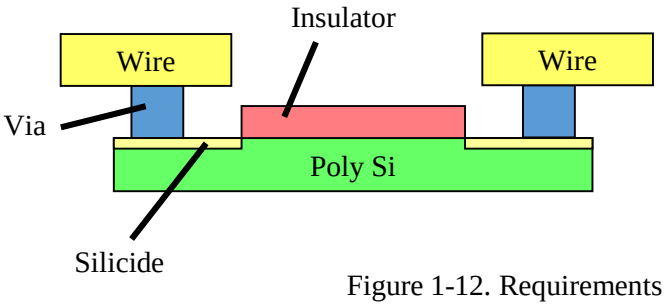


Figure 1-12. Requirements to resistor.

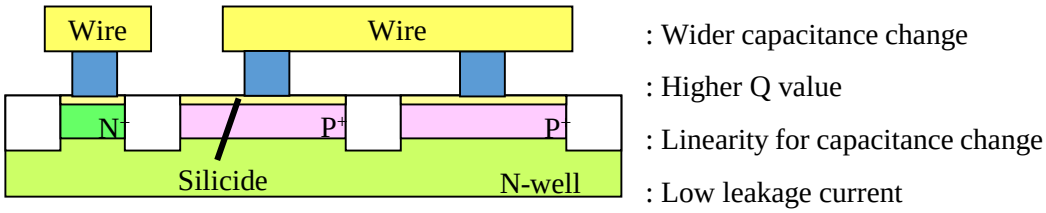


Figure 1-13. Requirements to variable capacitor (varactor) by PN junction.

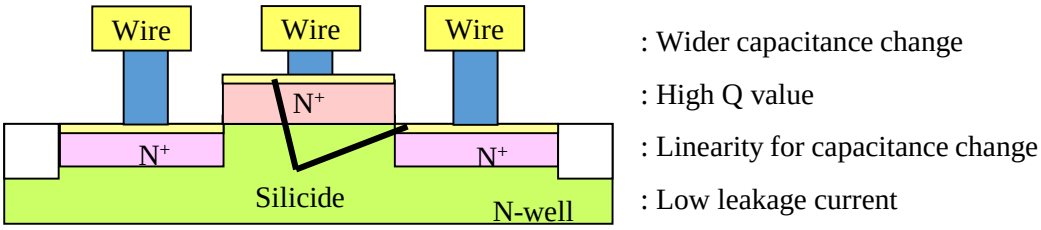


Figure 1-14. Requirements to varactor by MOS capacitor.

Figure 1-11 shows frequency dependence of Q value for an inductor. Lower wire resistance of the inductor is needed in order to achieve high Q value. The Q value decreases under higher frequency. This is caused by capacitance loss and magnetic loss between inductor and Si substrate. Thus, not only reducing of wire resistance but also reducing capacitance loss and magnetic loss are necessary in order to realize high Q value.

Figure 1-12 shows cross sectional view of resistor. The requirements to the resistor are optimum value of the resistance, good matching of pair resistors, lower temperature coefficient and low voltage coefficient of the resistances. The temperature coefficient depends on the impurity concentration. In lower concentration, the coefficient is negative which is characteristics of semiconductor, namely the resistivity decreases with increasing temperature. On the other hand, in higher concentration, that is positive which is characteristics of metal, namely the resistivity increases with increasing temperature. Thus, the very small coefficient can be realized by optimization of the impurity concentration.

Figure 1-13 shows cross sectional view of vaiable capacitor (varactor) formed with PN junction. The capacitance value can be controlled by changing the thickness of the depletion layer by applying bias. The requirements to the varactor are wider change in capacitance value, high Q value, low distortion and low leakage current. Figure 1-14 shows cross sectional view of varacter formed by MOS capacitor. The capacitance value can be controlled by a gate bias. This structure has wider capacitance change than the PN junction varactor. This result indicates the MOS varactor is useful for low voltage design of RF circuits because wider capacitance change is obtained even if applied bias is small. Thus, recently this varactor has been used than PN junction varactor for RF circuits design.

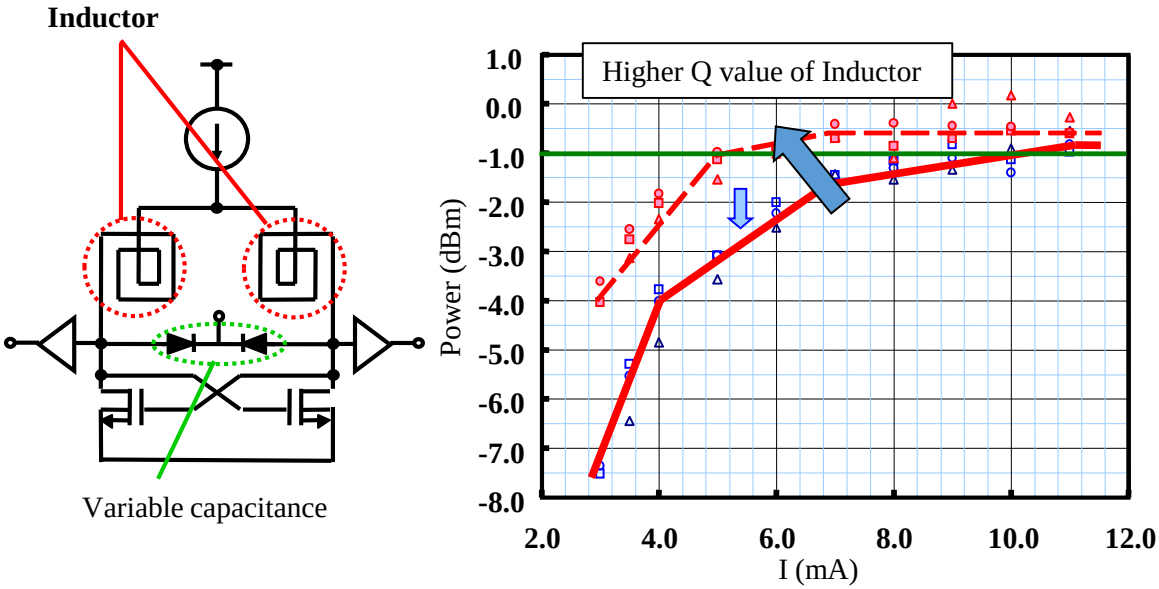
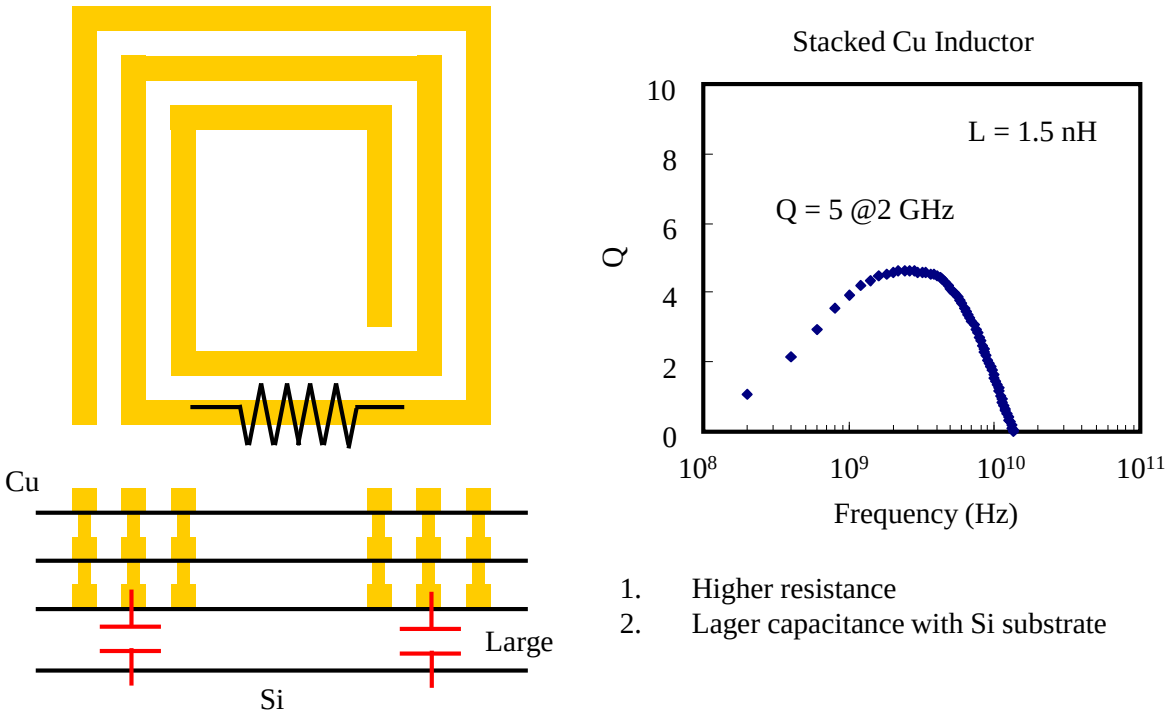


Figure 1-15. Power of VCO circuit at required output signal with difference Q value of inductor.



1. Higher resistance
2. Lager capacitance with Si substrate

Figure 1-16. Cu stacked inductor (Total wire thickness is 1μm). Low Q value is observed because of higher resistance and larger capacitance with Si substrate.

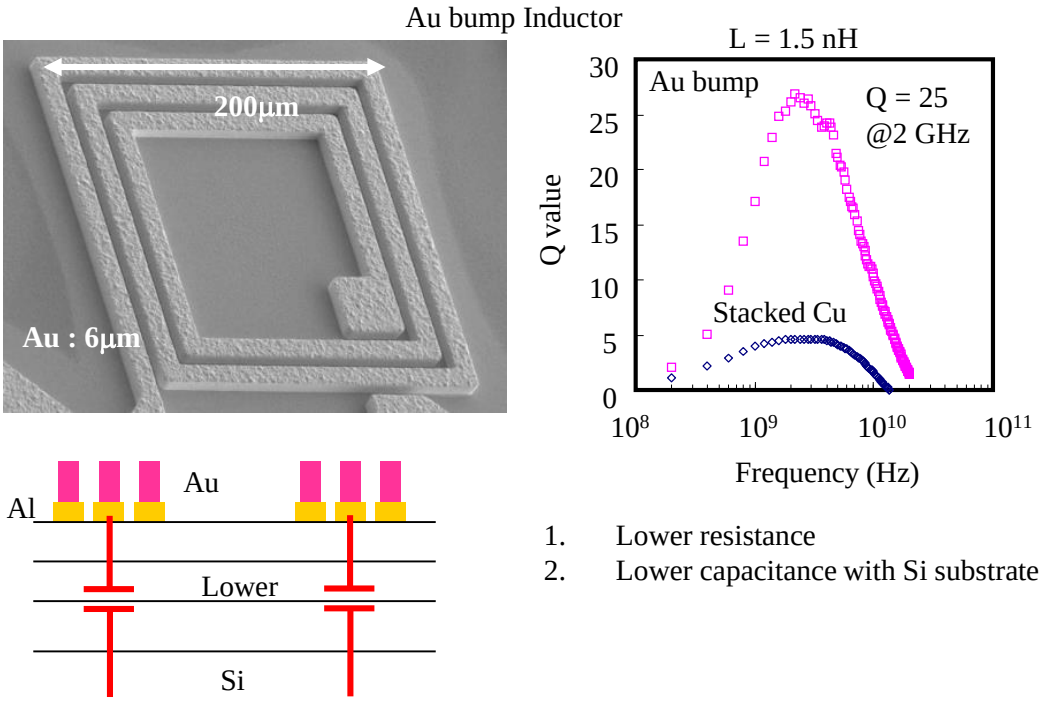


Figure 1-17. Au bump inductor (The Au wire thickness is 6μm). High Q inductor with Q of 25 is realized.

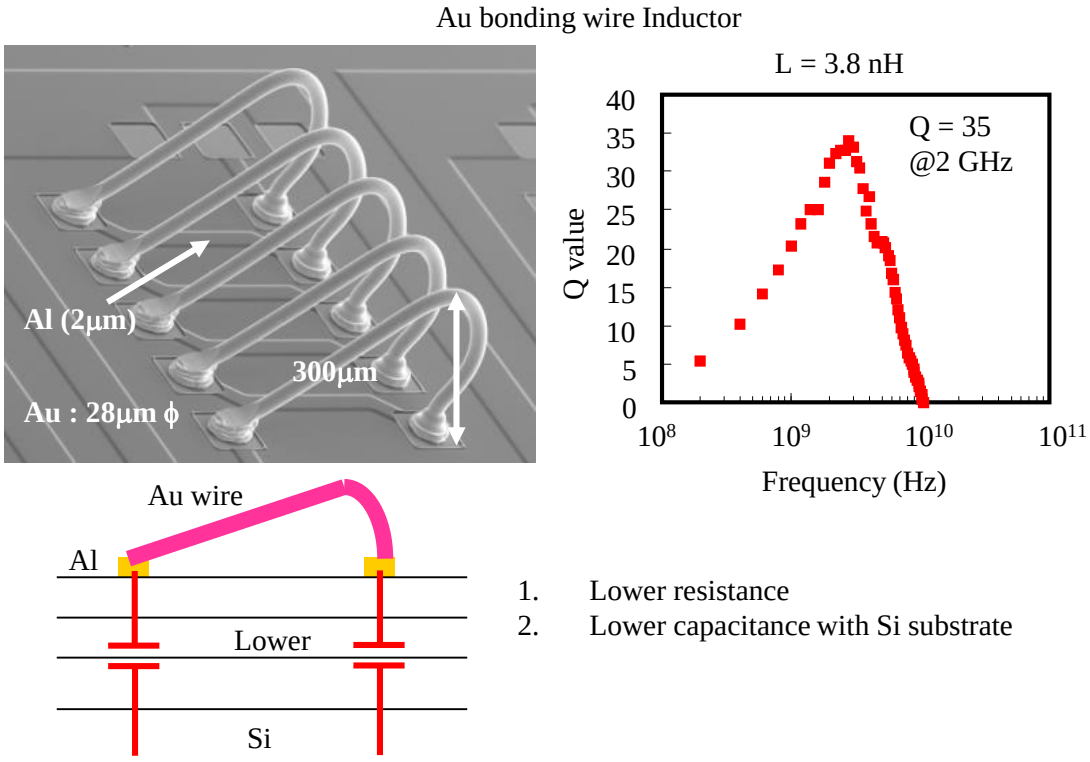


Figure 1-18. Inductor by Au bonding wire (The Au wire thickness is 28 μm). High Q inductor with Q of 35 is realized.

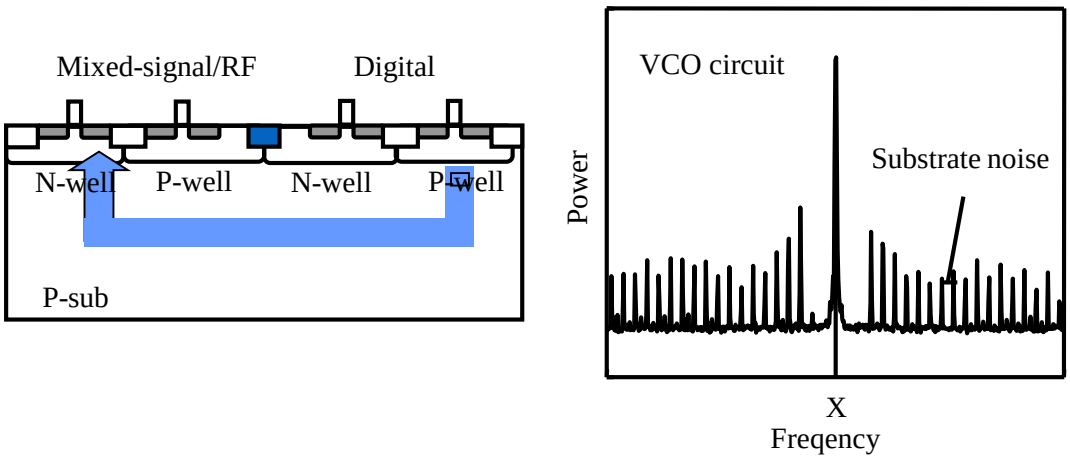


Figure 1-19. The substrate noise from digital to VCO circuit.

High frequency application by MOSFET has been spread because f_T and f_{MAX} have increased be scaling of MOSFET. At the same time, the improvement of Q value inductor is required for high performance RF circuit because the high Q can reduce not only phase noise but also power consumption of VCO circuits as shown in Fig. 1-15. In order to realize high Q inductor, low resistance of wire, low parasitic capacitance and high resistivity substrate are needed. But it is difficult to improve the Q value of on chip inductor because Cu thickness used for digital circuits are about the maximum 4 μm.

Figure 1-16 shows Cu stacked inductor. Each Cu thickness is about 300 nm, which is sufficient for digital circuits. In this case, Q value is lower because of higher resistance and larger capacitance with Si substrate. In order to improve Q value on chip inductor, we have some method. Those are fabrication of inductor on top Cu wire by using plating technology or bonding wire because both inductor has lower wire resistance and lower parasitic capacitance with Si substrate. Figure 1-17 shows high Q inductor by Au bump, whose Q value is 25 at 2 GHz. The improvement caused by lower wire resistance and lower parasitic capacitance with Si substrate. Additionally, inductor by Au bonding wire are attractive because wire is thicker than Au bump process. Figure 1-18 shows high Q inductor by Au bonding wire, whose Q value is 35 at 2 GHz.

CMOS devices are commonly used when digital, RF and analog circuits are embedded in a same Si substrate in order to reduce the system cost. However, suppression of substrate noise as shown 1-19 from digital circuit to mixed-signal and RF circuits through Si substrate during digital circuits operation is required.

1-5. Purpose of the study and outline of the thesis

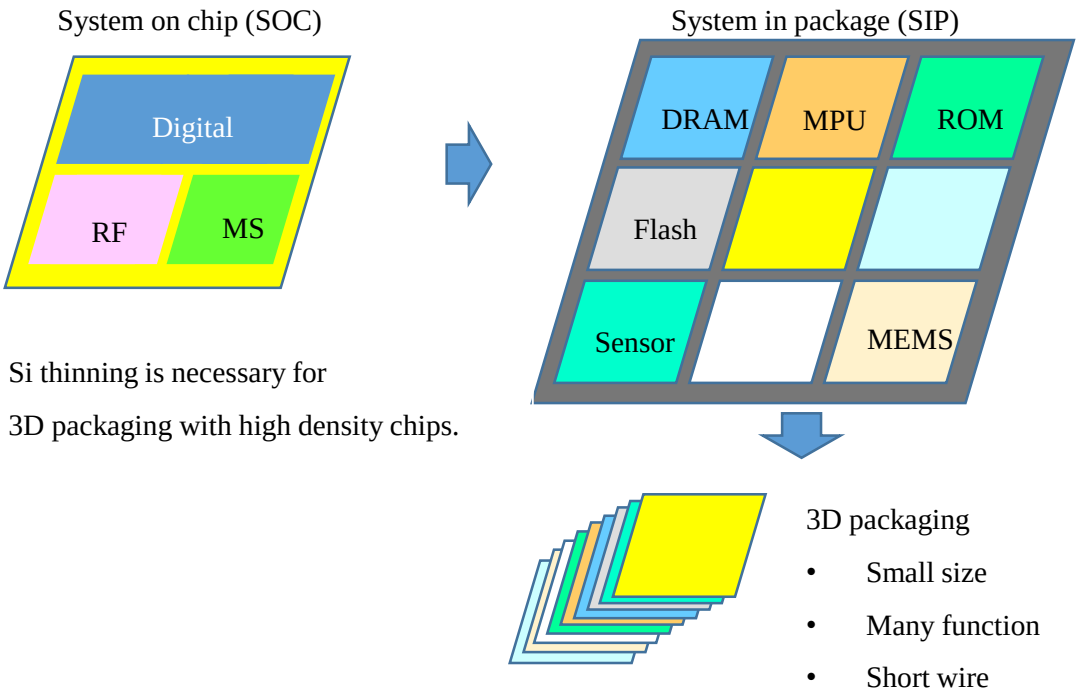


Figure 1-20. Change from SOC to SIP with high density chips.

Recently, 3D stacked integration has been important in order to realize both high-density system in package (SIP) and high functionality with heterogeneous integration of materials and devices. Because it has been significantly difficult to fabricate many circuits on a same chip due to complex process and very expensive to realize the chip. Thus SOC has not been attractive because especially the cost of digital chip fabricated by advanced CMOS process has become higher. While in SIP, the process of each chip can be optimized for each circuit. The issues of SIP are larger packaging area and height, and degradation of signal translation speed. Thus, recently, 3D packaging technology has been developed by using (Trough Silicon Via) TSV technology. Additionally ultra-thin Si substrate is necessary to realize packaging with high density chips because circuits on thin Si substrate are effective for realizing SIP with many stacked chips within limitation of height of packaging as show in Fig. 1-20. For example, when 5 chips are stacked, the height is 505μm in the Si substrate thickness of 100 μm, while the height is only 15 μm for the thickness of 2 μm according to our estimation. (5 μm is needed for TSV process except chip thickness.)

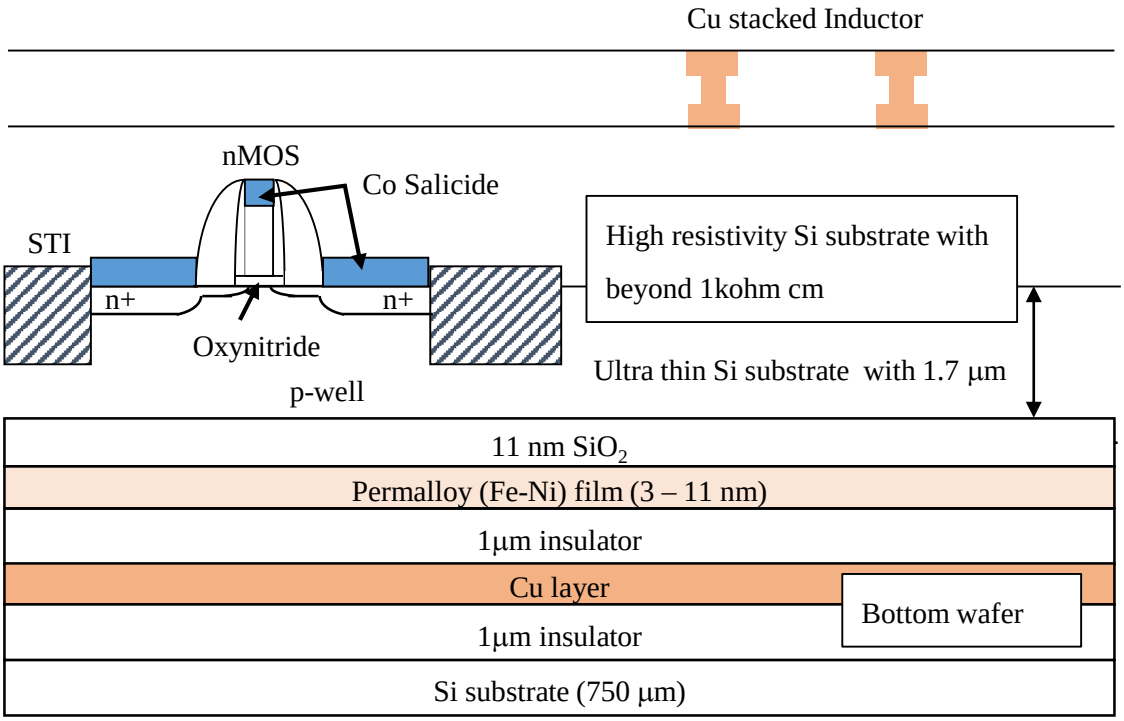


Figure 1-21. Schematic cross sectional view of ultra-thin chip.

In this thesis, firstly, device and process technologies for high performance mixed and signal and RF device are described. After that, study of mixed and RF device on ultra-thin Si substrate is described. Figure 1-21 shows the chip structure for my experiment. The thickness of Si substrate is 1.7 μm which is thinner than Pwell depth. The substrate resistance is beyond 500 ohm cm. A permalloy film is deposited on back side of the ultra-thin chip. I obtained the results of the larger reduction of substrate noise and the minimum of noise figure ($N.F._{min}$) because the penetration of the noise, which passes along Psub from Nwell can be suppressed. No degradation of 1/f noise is observed due to no degradation of D_{it} during thinning process. Additionally, we found gm and f_T in PMOS have layout dependence because compressive stress occurs in the thin chip. The Q value degradation of Inductor caused by the metal under thin chip can be suppressed by 10 nm permalloy film deposition on backside of Si substrate because the film can suppress the penetration of magnetic field into the metal.

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Chapter 2
Reduction of resistive component for higher gain of CMOS

2-1. Salicide technology for higher f_T, f_{MAX} and lower thermal noise

2-1-1. History of introduce of Salicide to CMOS

Table 2-1-1. Material constants of various metal for slicide used in MOSFET.

Silicide	Resistivity (μΩ cm)	Moving species	Silicidation Temp. (°C)	Film stress (dyne/cm)	Si consumption
$TiSi_2$	10 - 15	Si	750 - 900	1.5×10^{10}	0.904
$CoSi_2$	18	Co	550 - 900	1.2×10^{10}	1.03
NiSi	20	Ni	350 - 500	6.0×10^{9}	0.82

Silicide	Diffusion in Si (cm^2/sec)	Barrier height for electron (eV)	Barrier height for hole (eV)
$TiSi_2$	Ti : 2.0×10^{-5}	0.61	0.49
$CoSi_2$	Co : 9.2×10^{-4}	0.65	0.45
NiSi	Ni : 2.0×10^{-3}	0.67	0.43

Self –aligned silicide (Salicide) enables source, drain, and gate layers of low resistivity to be formed. Table 2-1-1 shows material constants of various silicide. $TiSi_2$, $CoSi_2$ and NiSi have been used to logic CMOS. In $TiSi_2$, moving specie is metal (Ti) while in both $CoSi_2$ and NiSi, those are Si during silicidation process. The specie difference causes narrow line effect difference. Regarding to the silicidation temperature, In $TiSi_2$, that is highest and in NiSi, that is lowest. The temperature depends on the diffusion coefficient of each metal in Si. The lower silicidation temperature corresponds to the lager coefficient.

As the temperature decreases, the agglomeration during silicidation process can be suppressed when gate length becomes shorter. From point of the view, NiSi is the most suitable for scaled CMOS. Additionally, NiSi is important for higher drivability of PMOS because barrier height for hole is lowest.

As silicide material, for the first time, $TiSi_2$ had been used for CMOS production since 250 nm technology node because Ti is easy to react Si due to high reducibility and $TiSi_2$ has lower barrier height for N-type, which is advantage for higher drivability of NMOS [1]-[7]. However, it had been discovered that the sheet resistance of a Ti-salicided polysilicon gate electrode increases significantly as the line width reaches the lower sub-micron range [8-10]. This became a significant problem in deep submicron high-speed CMOS devices. Because the degradation causes delay of operation speed due to RC delay. In order to suppress the increases of sheet resistance of Ti-salicided polysilicon gate, pre-amorphization was suggested by arsenic ion implantation because the amorphization is easier by heavier arsenic. However, no effect was when the gate length was below 180nm. Thus, the other silicide materials had been proposed to overcome this shortcoming. The aim of section 2-1-2 is to clarify the mechanism by which this increase in $TiSi_2$-polycide resistance arises as the line width is reduced. Using a combination of electrical measurements and analysis by TEM and EDX (energy-dispersive X-ray spectroscopy), the complex mechanism of the resistance increase has been successfully explained. And sheet resistance and top view and cross sectional view of Ni-salicided and Co-salicided polysilicon was also observed. Clearly difference points were found by comparing among $TiSi_2$, $CoSi_2$ and NiSi. Particularly noteworthy is a new test structure I have designed with six voltage terminals at various spacing for the detection of high resistance and non-ohmic regions to a resolution of 0.2 μm. Following our analysis, I consider the possibility of replacing $TiSi_2$ with another material, namely $CoSi_2$ and NiSi [11]. I demonstrate that NiSi and $CoSi_2$ do not suffer from resistance degradation when the lines are very narrow [12], [13], and the reason for this is also explained.

The NiSi has been used beyond 90 nm technology node. But the NiSi had serious problem, that is abnormal oxidation of NiSi formed on As doped Si substrate. By this problem, the NiSi was not used to CMOS. In section 2-1-2, the analysis and method to resolve that are described.

2-1-2. Analysis of narrow line effect

i) Salicidation process

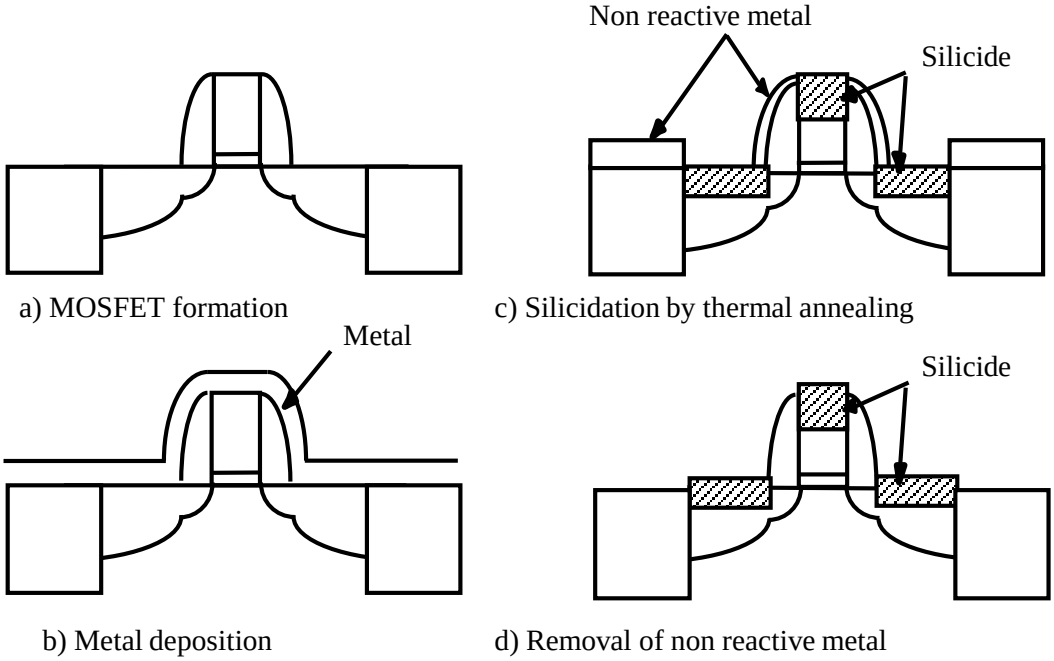


Figure 2-1-1. Self-aligned silicidation (Salicide) process.

Figure 2-1-1 shows explanation of self-aligned silicidation process. After fabrication of MOSFET and removal oxide film on Si substrate and poly Si by wet treatment (dilute HF), a metal is deposited by sputtering process. In order to silicidation between Si and a metal, thermal annealing is carried out in N_2 gas. Then, non-reactive metal is removed by wet treatment (mixture of H_20_2 and H_2S0_4 in my experiments). In final case, silicide material remains on gate, source and drain regions. This process is named as self-aligned silicideation (Salicide).

ii) Sample fabrication for analysis of narrow line effect

In order to analysis of narrow line effect, just gate line are fabricated (In this experiments, MOSFET are not fabricated). After Growing 100 nm oxide films by thermal oxidation on a p-type (100) silicon wafer, 350 nm polysilicon films were deposited. After polysilicon line patterning, films of Ti (20 nm), Co (20 nm) or Ni (20 nm) were deposited and silicided. In the Ti case, the silicidation conditions were 750 ℃ for 30 s in N_2 as the first stage in $TiSi_2$ formation. After selective etching of the unsilicided portion of Ti using $H_20_2 + H_2S0_4$, a second silicidation was camed out at 900 ℃ for 20 s in N_2.

iii) Dependence of Sheet Resistance on Line Width

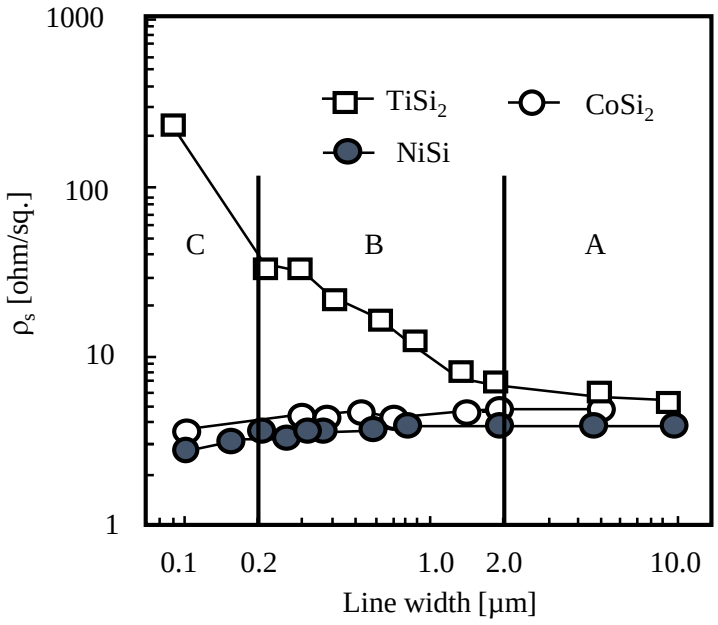


Figure 2-1-2. the line-width dependence of sheet resistance for silicided polysilicon.

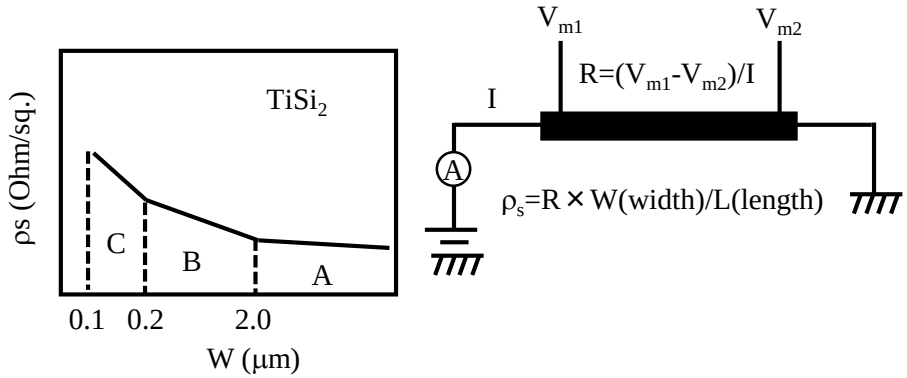


Figure 2-1-3. the TEG layout to analyze silicide line effect of $TiSi_2$.

Figure 2-1-2 the line-width dependence of sheet resistance for silicided polysilicon This second thermal annealing reduces the sheet resistance of the $TiSi_2$ layer by modifying the grain structure from C49 to C54 [14], [15]. In the Ni and Co cases, one-step annealing at 400 °C and 600 °C for 30 s were sufficient to fabricate low-resistivity NiSi and $CoSi_2$ layers without forming bridges of silicide between the source/drain and gate [11]. The unsilicided areas of Co and Ni were also selectively etched off in $H_20_2 + H_2SO_4$.

In $TiSi_2$, sheet resistance increases when the gate length is below 1.0 μm. Additionally, the abruptly increases as below 0.2 μm. On the other hand, in both $CoSi_2$ and NiSi, the sheet resistance slightly decreases as narrower gate length. The four-point probe pattern shown in Fig. 2-1-3 was used to take the measurements. In this pattern, the voltage terminals are separated by 250 μm, and the potential applied across the current terminals was 5 V. The average values of sheet resistance for a whole wafer (30 chips) are plotted in the figure. The variation of the sheet resistance in the measured value is well within 30 %. $TiSi_2$-Polycide: In the $TiSi_2$-polycide (or titanium silicided polysilicon) case, the dependence of sheet resistance on line width, *W,* is characterized by three distinct regions. I label these A, B, and C in the schematic illustration in Fig. 2-1-3. In region A (W > 1-2 μm*),* sheet resistance is independent of the width and is low valued. The sheet resistance begins to increase when the width falls to region B (1-2 μm > W > 0.2 μm). There is then an abrupt increase in $TiSi_2$-polycide resistance when the line width falls below 0.2 μm; this is region C *(*W < 0.1 μm). NiSi and $CoSi_2$ Polycide: In contrast with the $TiSi_2$ results, lines of NiSi and $CoSi_2$-polycide (NiSi and $CoSi_2$-polysilicon) exhibit little line width dependence; the resistance even decreases slightly as the line width falls.

iv) Analysis of sheet resistance behavior in $TiSi_2$

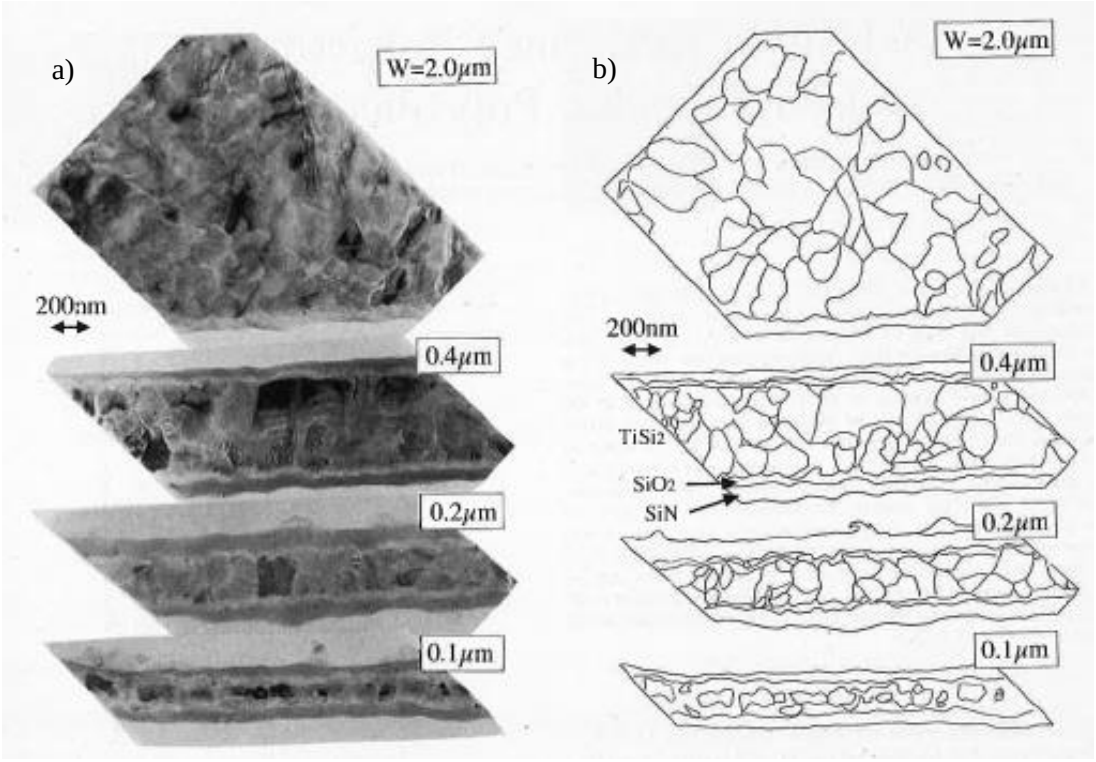


Figure 2-1-4. TEM photographs of $TiSi_2$ films of various line width.

I will first consider the observed resistance increase in the $TiSi_2$ case, looking mainly at the results for arsenic-doped samples. TEM determination of grain structure : The increase in sheet resistance in narrow $TiSi_2$ lines (down to 1-0.5 μm) has been explained [8], [9], [17] in terms of the difficulty of the phase transformation from C49 $TiSi_2$ grains ($ZrSi_2$ structure) to the C54 grain structure ($TiSi_2$ structure). The C49 structure is characterized by smaller grains (0.2 μm) and greater resistivity (60-80 μohm-cm) [17], while the C54 structure features a larger grain size as compared with the line width 0.2 μm and lower resistivity (10-15 μohm-cm) [16]. In order to compare our electrical measurements with the grain structure of the $TiSi_2$-polycide lines, we carried .out TEM observations on $TiSi_2$-polycide lines of various widths corresponding to regions A to C. Fig. 2-1-4 (a) shows TEM photographs of the top surface of $TiSi_2$-polycide lines of various widths. Only typical portions of the observed area are given here as examples. To give a clear picture of the grains, the boundaries in the photographs have been traced in Fig. 2-1-4 (b). In the 2.0 μm and 0.4 μm cases, the polycide line comprises a mixture of large and small grains. In the 0.2 μm and 0.1 μm cases. the lines are filled with small grains. These line widths are too small to allow growth of the larger grains. In order to compare the area distribution of each grain size, the dimensions of all grains were measured.

v) Grain size statistics and C54 to C49 ratio

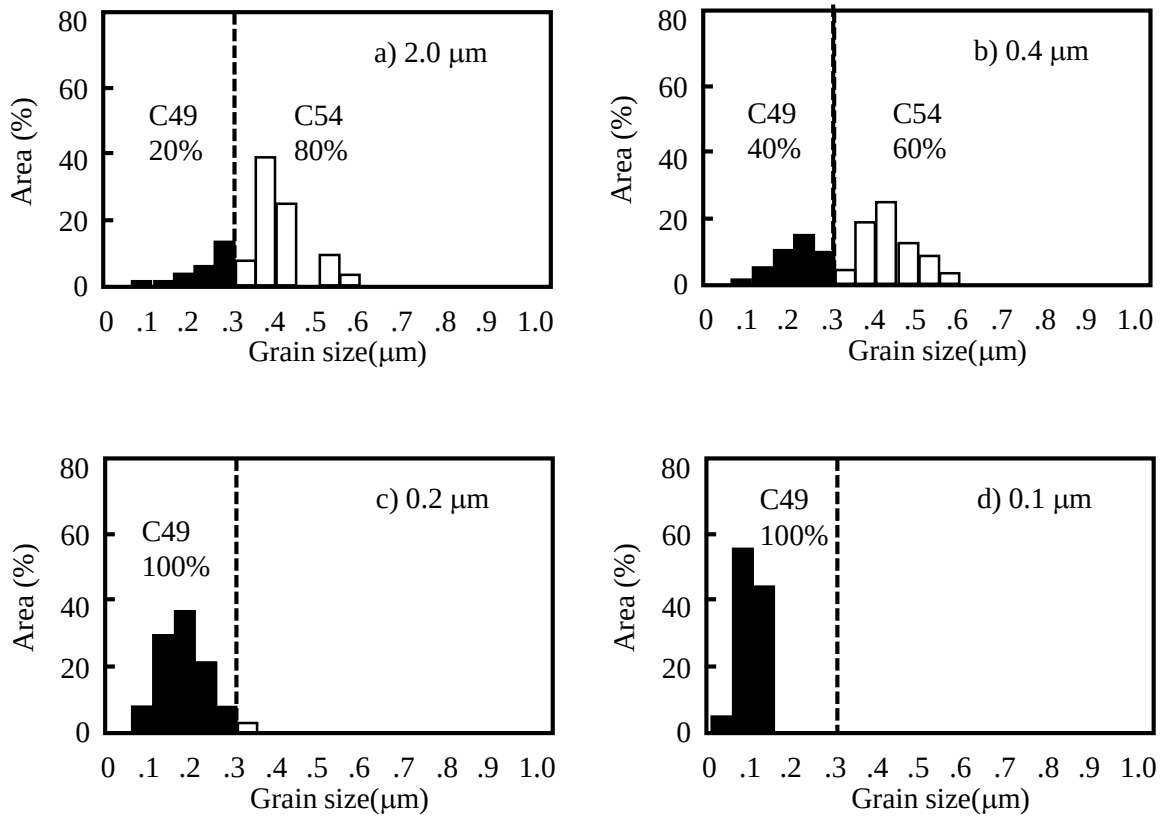


Figure 2-1-5. Line width dependence of C49 and C54 content.

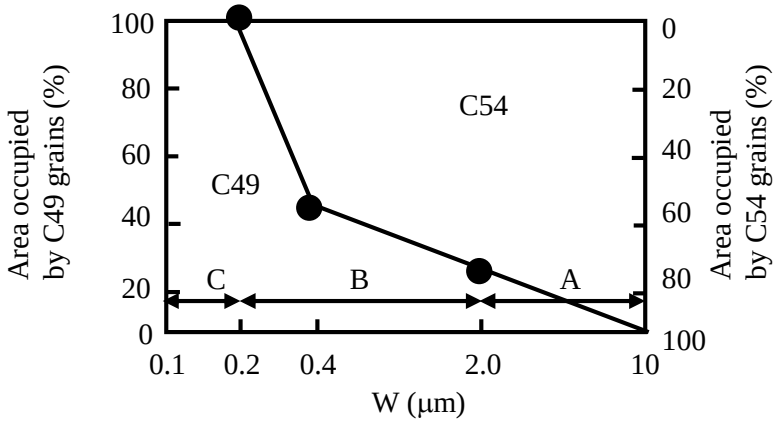


Figure 2-1-6. Line width dependence of ratio of C49 grains.

The ratio of area occupied by each size is plotted in Fig. 2-1-6. In making these measurements, the size of a grain is defined as $(r_l \times r_s)^{1/2}$, here r_l and r_s are the largest and smallest diameters of the grain, respectively. The grain area S is defined as $(1/4)\ \pi\ r_l \times r_s$,. The measured distributions in the 2.0 μm (Fig. 2-1--5 (a)) and 0.4 μm (Fig. 2-1-5 (b)) cases clearly show that there are two categories of grain size, a smaller one (<0.3 μm) and a larger one (>0.3 μm). In the 0.2 μm and 0.1 μm cases, only the smaller grains are present.

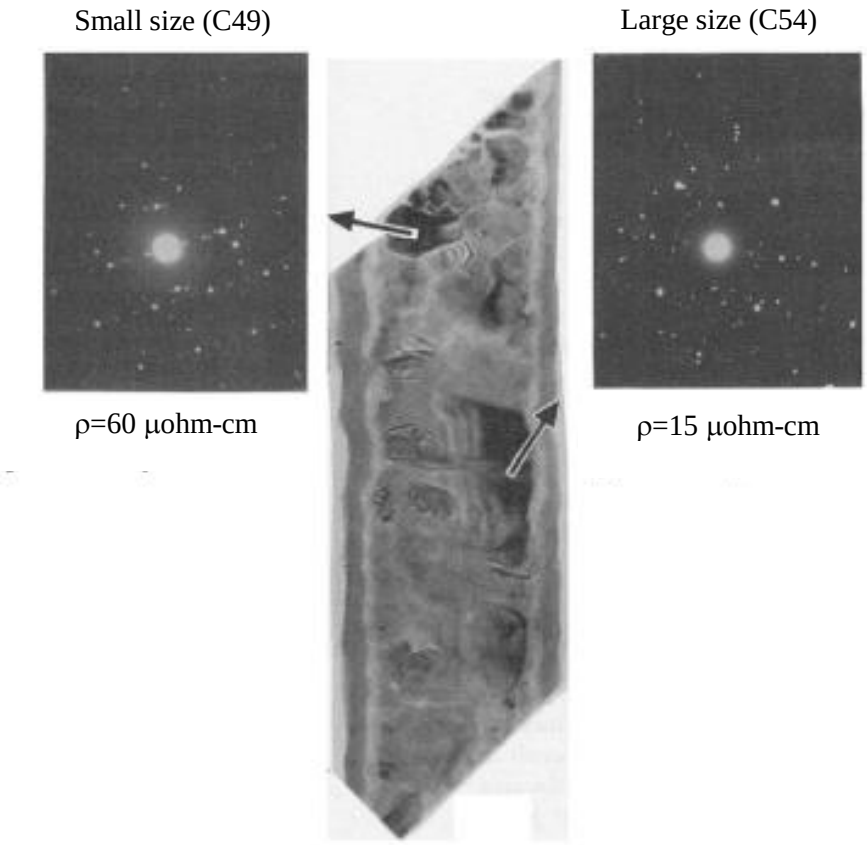


Figure 2-1-7. Selective area electron diffraction analysis of $TiSi_2$ polycide.

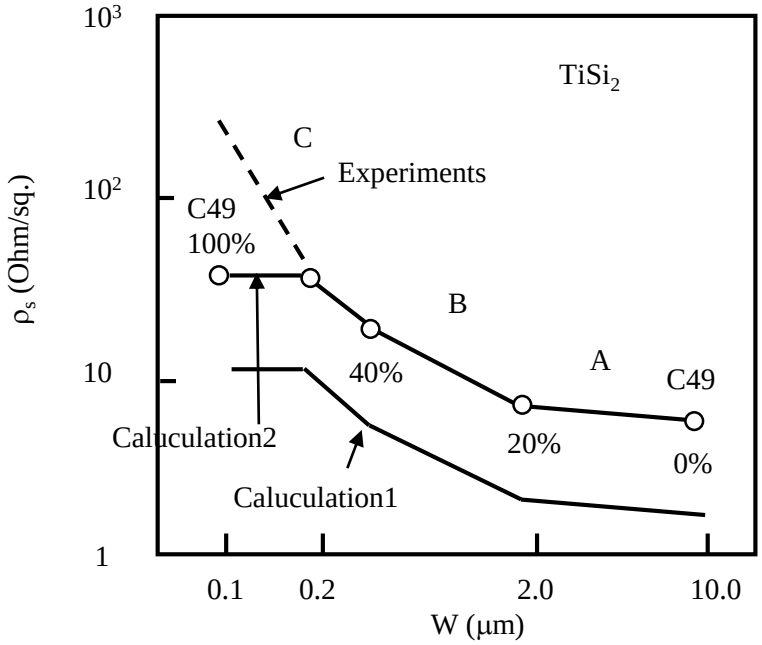


Figure 2-1-8. Line width dependence of $TiSi_2$- -polycide. Calculated according to the ratio of C49 and C54 content.

The structures of these two grain types were determined by selective area electron diffraction analysis, as shown in Fig. 2-1-7, verifying that the smaller grains consist of C49 and the larger of C54. Using these results, the dependence on line width of the ratio of C49 to C54 area was calculated. These results are plotted in Fig. 2-1-6. In region A as represented by the 2.0 μm case C54 grains take up 80 % of the total area. In region B, the area occupied by C54 falls to 60 % (the 0.4 μm case), finally becoming 0 % when the width falls to 0.2 μm. In region C, all the grains are C49. These results confirm quantitatively that the transformation from C49 to C54 is difficult when the lines are narrow. In particular, it was found that C54 is very unlikely to be formed when the line width is less than 0.2 μm, or less than the size of typical C54 grains.

The line width dependence of sheet resistance can be calculated on the basis of these area ratios of C49 and CS4. The results of doing this are shown in Fig. 2-1-8, where they are compared with the experimental data already given in Fig. 2-1-2. Bulk resistivity values for C49 and C54, taken from the literature were assumed to be 76 mohm-cm and 12.4 mohm-cm, respectively [17]. I used a simple model to calculate the sheet resistance for a region comprising a mixture of C49 and C54. In the case of a narrow line comparable with a grain size of about 0.4 μm, I assumed the line consists of high (C49) and low (C54) resistance portions connected in series, because only the following two grain configurations are likely to be present:

1) a C54 grain comparable in size with the line width occupies almost the entire width, or 2) there are no C54 grains in the width direction. so only C49 grains size, such as 2 μm, I assumed that the two resistances are connected in parallel; in our experiments, even the C54 grain size is not that large (0.3-0.6 μm) as already seen in Fig. 2-1-2, so both C54 and C49 grains occur in the width direction. The sheet resistance of the underlying polysilicon is too high to affect the overall polycide sheet resistance and can be ignored. Note that the sheet resistance is higher when C54 and C49 regions are linked in series than when they are in parallel.

vi) Line Width Dependence of $TiSi_2$ Film Thickness

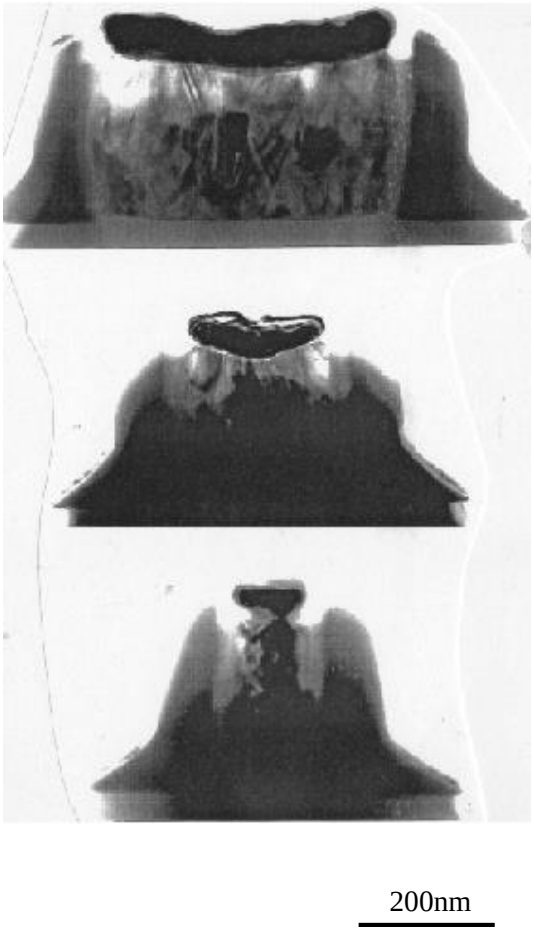


Figure 2-1-9. TEM photograph of cross section through $TiSi_2$-polycide.

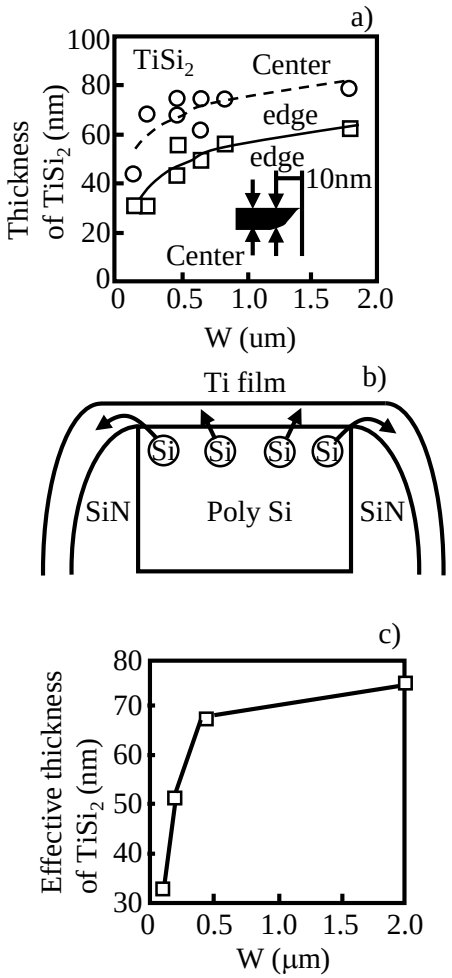


Figure 2-1-10. Line width dependence of $TiSi_2$ film thickness.

The dotted curve (Calculation- 1) in the figure shows the calculated results. Here, I assumed 100 % of the area is occupied by C54 in the 10 μm-wide line. The curve indicates a tendency for the resistance to rise with falling line width. However, the values are significantly less than the experimental results even in the 10 μm case, a result of using the bulk resistivity in the calculation. In a thin film, it is quite normal for the sheet resistance to be higher than the bulk value. I then fitted the calculated curve to the experimental results at W = 10 μm, thus taking account of thin film effects, as shown by the solid line (Calculation-2). The calculated results now approach very closely to the experiment. However, the curve remains significantly lower than the experimental results at W = 0.1 μm. Thus the varying crystal content the mix of C54 and C49 can almost explain the sheet resistance increase in narrow polycide lines, but is unable to explain the very high sheet resistance of a 0.1 μm-wide polycide line.

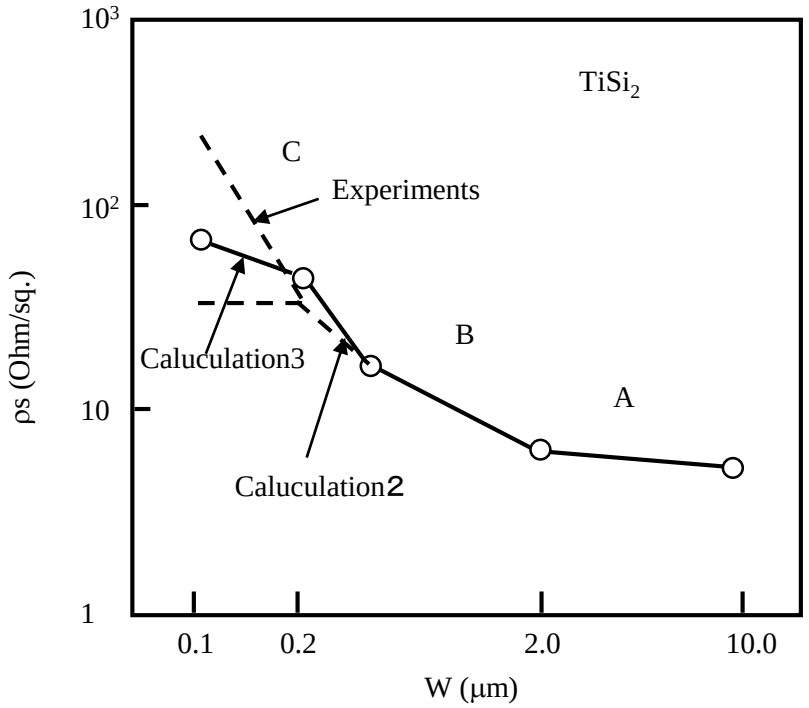


Figure 2-1-11. Line width dependence of $TiSi_2$ -polycide sheet resistance calculated including both C49 to C54 content ration and effective $TiSi_2$ film thickness.

Cross-Sectional observations by TEM: In order to look into the cause of the discrepancy between calculation and experiment in region C, cross sections through arsenic-doped $TiSi_2$-polycide lines were observed by TEM, as shown in Fig. 2-1-9. The figure shows only four cases of different line widths, but samples of other widths were also observed. The $TiSi_2$ film takes on a concave shape in the downwards direction, as seen in previously published references [9], [17], [20], [21] in our case, when the line width is less than 1 μm.

As of now, the reason for this curvature of the $TiSi_2$ film has not been clarified; it may be a result of shrinkage of the film during or after silicidation. Note that the thermal expansion (or shrinkage, in this case) coefficient of a $TiSi_2$ film (10.5×10^{-6}/K [22]) is much larger that of the underlying polysilicon (2.3×10^{-6}/K). In these photographs, it should be noted that the $TiSi_2$ film is thinner at the edge than that at the center. When the line width is in the 0.2-0.1 μm range, even the center portion of the $TiSi_2$ film is very thin. The dependence of film thickness at the edge and at the center on line width is shown in Fig. 2-1-10(a).

This thinning phenomenon can be explained in terms of the Ti silicidation mechanism, as shown in Fig. 2-1-10(b). In the case of $TiSi_2$, silicidation takes place in the Ti film by Si diffused from the polysilicon. At the edge, the density of diffused Si would be low, because the Si diffuses out two-dimensionally at the edge. Thus, Ti silicide film growth would be lower at the edge than that at the center. The line width dependence of effective $TiSi_2$ film thickness ($t_{eff} \sim S/W$, where S is the cross section of the $TiSi_2$ film, and W is the width of the polycide) is shown in Fig. 2-1-10(b). Note that the effective thickness in the case of a 0.1 μm line is less than half that of a 2 μm line.

Film Thickness*:* The thinning phenomenon described above would have a significant upward influence on sheet resistance, so we have recalculated the line width dependence of the $TiSi_2$-polycide sheet resistance to take account of it. The results are shown in Fig. 2-1-11 (Calculation 3). The new calculated plot is even closer to the experimental curve. However, the calculated value at W = 0.1 μm (or in region C) is still smaller than that measured in my experiments.

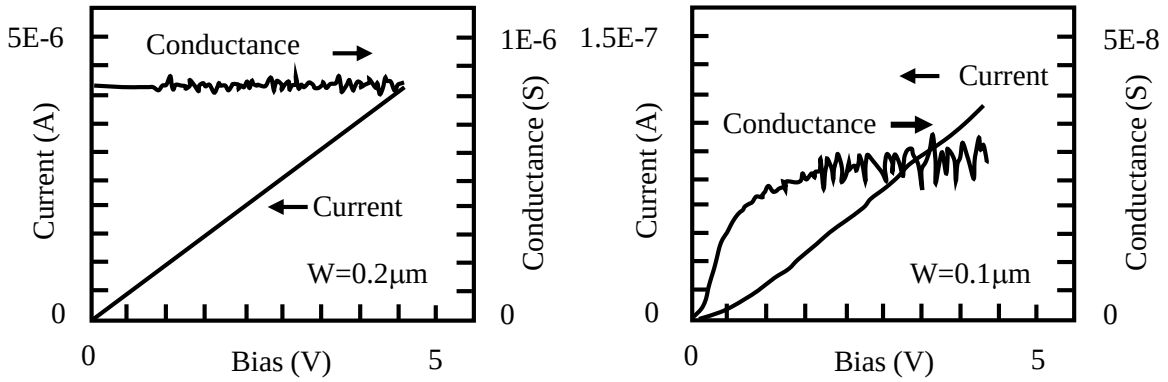


Figure 2-1-12. I-V characteristics and temperature dependence of sheet resistance for $TiSi_2$ lines; (long line; L = 250 μm). (a) I-V characteristics for L = 0.2 μm case, (b) I-V characteristics for L = 0.1 μm case, and (c). Temperature dependence of sheet resistance.

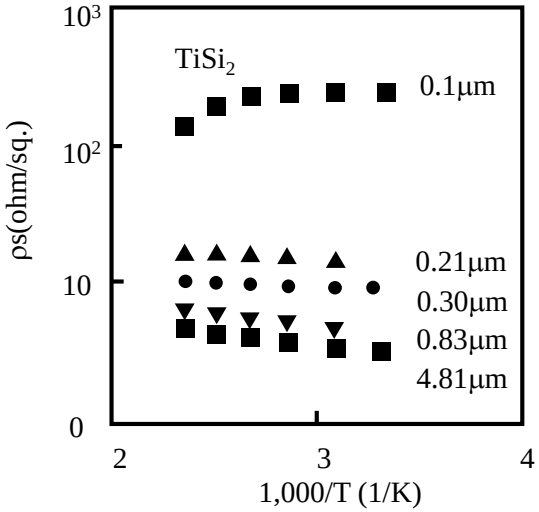


Figure 2-1-13. I-V Temperature dependence of sheet resistance of $TiSi_2$ polycide with various line width.

In order to investigate the remarkably high resistance in region C, the I-V characteristics and temperature dependence of sheet resistance were measured as shown in Fig. 2-1-12. While samples with W = 0.2 μm and greater (regions A and B) exhibit normal ohmic I-V characteristics, as shown in Fig. 2-1-12(a), the sample with W = 0.1 μm (region C) shows nonohmic behavior (Fig. 2-1-12(b)). The change in sheet resistance with temperature for each line width is shown in Fig. 2-1-13. These curves can be divided into two categories corresponding to the three *W* regions: a 0.1 μm-wide electrode (region C) has a negative temperature coefficient of resistance, while the others (regions A and B) are all positive. This suggests that conduction in the 0.1 μm electrode is limited by carriers which overcome some kind of barrier just as in the case of conduction in lightly doped polysilicon, where a grain boundary acts as a potential barrier [21].

vii) Electrical Characteristics of Ultra-Small Regions:

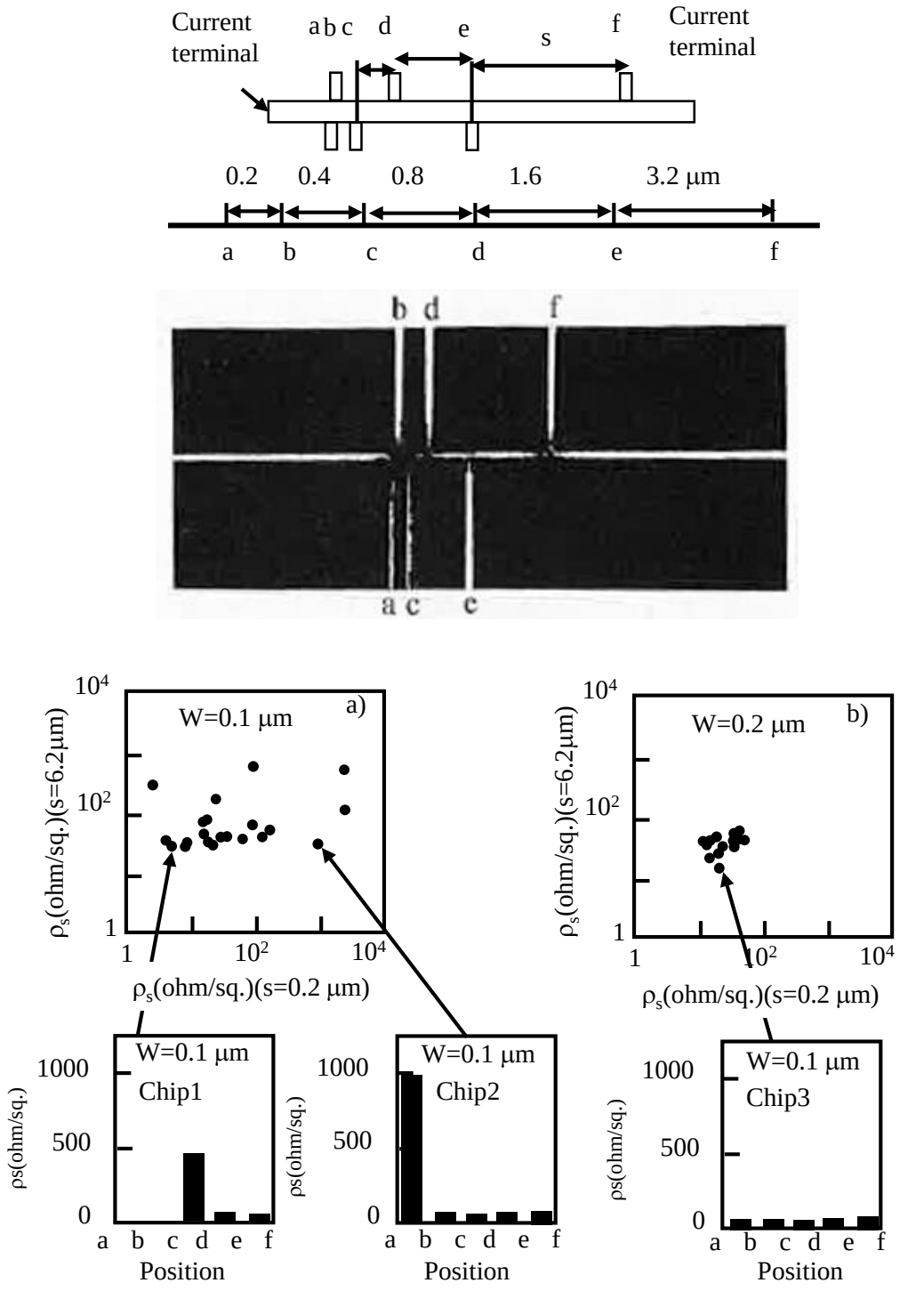


Figure 2-1-14. Sheet resistance of arsenic-doped $TiSi_2$-polycide as extracted from individual sections of special test pattern.

In order to further investigate the origin of this higher resistance at smaller line widths in region *C,* we carried out the first-ever detailed measurements of resistance in an ultra-small region. The resistance pattern used for these measurements consisted of two current terminals and six potential terminals, as shown in Fig. 2-1-14(a). The spacing of these potential terminals was 0.2, 0.4, 0.8, 1.6, and 3.2 μm (for a total length of 6.2 μm). Assuming a non-uniform distribution of resistance along the line, this pattern would enable us to detect the location, or at least the density, of high-resistance sections with a 0.2 μm resolution. Fig2-1-14(b) gives two typical examples of sheet resistance measurements from individual sections of this pattern when W = 0.1 μm. In the case of sample chip 1, the high resistance region happens to fall between terminals *c* and *d,* while in the case of sample 2 it falls between terminals *a* and *b.* It is clear that each area of high-resistance is extremely localized and that the length of these high-resistance regions is less than 0.2 μm. This is of the order of the grain size. The correlation between individual $TiSi_2$-polycide sheet resistance values extracted from 0.2 μm-long sections and the resistance of the whole 6.2 μm length of the same 0.1 μm line is also shown in Fig. 2-1-14(b). The sheet resistance of a 0.2 μm long section ranges from a few ohms-the ideal $TiSi_2$ sheet resistance-to several thousand ohms, while the resistance of the whole 6.2 um-long line is some tens of ohms or more. This indicates that at least one region of localized high resistance, exists in a 6.2 μm length of a 0.1 μm Ti-polycide line, but not necessarily in a 0.2 μm length. When the line width is 0.2 μm or greater, the sheet resistance of individual sections of the pattern is always low, as shown in Fig. 2-1-14(c) *(*W = 0.2 μm case). Thus no localized high-resistance portion exists.

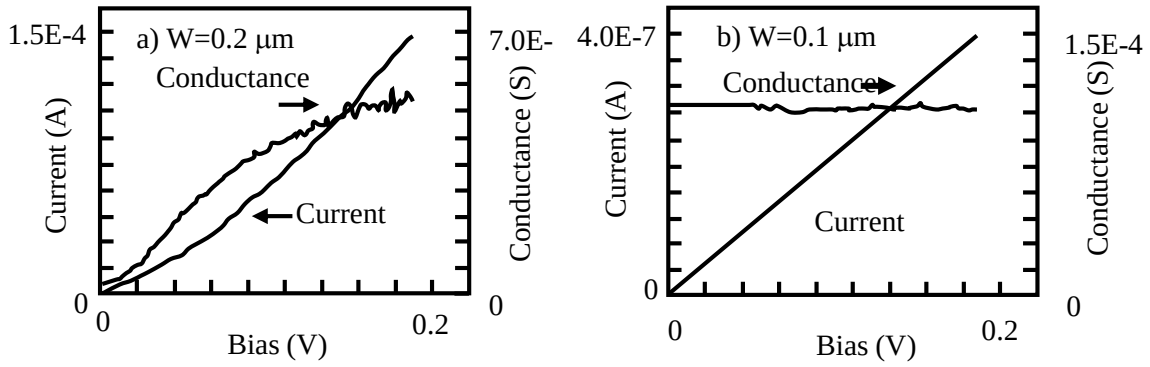


Figure 2-1-14. I-V characteristics and temperature dependence of sheet resistance for $TiSi_2$ line measured using the special test pattern (very short line; L = 0.2 μm; W = 0.1 μm).

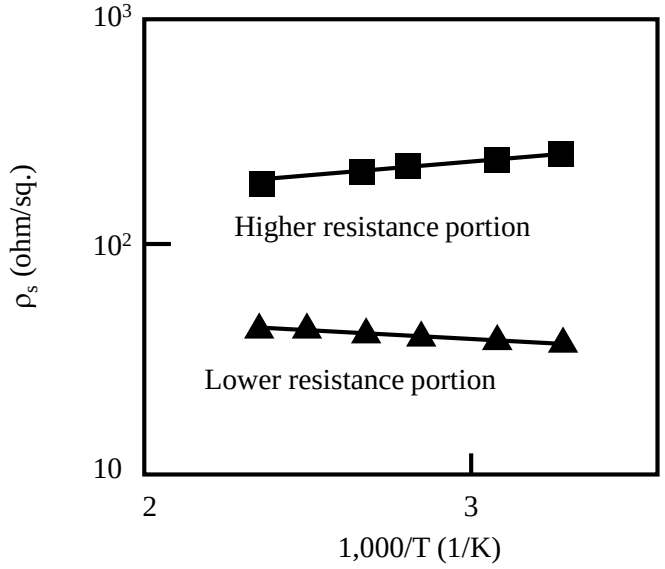


Figure 2-1-15. I-V Temperature dependence of sheet resistance for high- and low-resistance portions.

The I-V characteristics and temperature dependence of sheet resistance were measured for the individual sections of the test pattern for W = 0.1 μm. The results are shown in Fig. 2-1-14. The I-V characteristics of the localized high-resistance regions in the 0.1 μm polycide line indicate that the behavior is non-ohmic (see Fig. 2-1-14(a)), while the other lower resistance portions are typically ohmic (Fig. 2-1-14(b)). The overall result for a long line is a non-ohmic I-V characteristic. The temperature dependence is negative only within the localized high-resistance sections, and all other regions exhibit a positive temperature dependence, as shown in Fig. 2-1-15. Thus the non-ohmic IV characteristics and negative temperature dependence of the sheet resistance in long 0.1 μm-wide polycide lines, as already seen in Fig. 2-1-13, are the result of an accumulation of localized high-resistance regions.

TEM and EDX Analysis of Grain Boundaries:

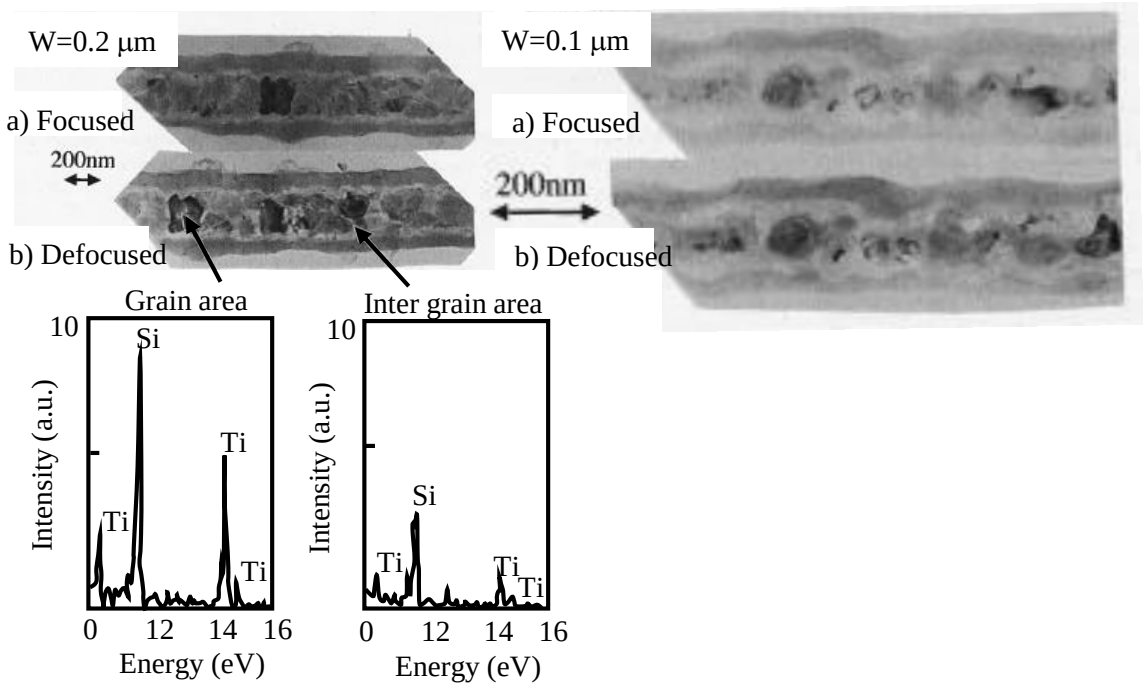


Figure 2-1-17. TEM and EDX analysis of grain boundary regions for $TiSi_2$-polycide.

The localized non ohmic behavior and areas of negative temperature coefficient within a span of 0.2 μm strongly suggest that the high resistance is caused by some kind of potential barrier at the grain boundary. The grain boundaries of As-doped $TiSi_2$ polycide were observed carefully by varying the focus during TEM measurements, as shown in Fig. 2-1-17. Such defocusing causes amorphous regions to be delineated, and significant amorphous regions were found between the grains. EDX (energy-dispersive x-ray spectroscopy) was used to determine the composition of both the grains and these inter-grain layers; the results are shown also in Fig. 2-1-17. The peaks are smaller in the inter-grain area than in the grains themselves. This suggests that the density or film thickness of the inter-grain area is smaller than that of the grain. It is quite likely that these amorphous inter-grain regions were formed by the TEM sample fabrication process by ion milling. However, it is also certain that prior to TEM sample formation the grain boundary region had originally been formed poorly. That is, either the region was thin, the density was low, or it was poorly silicided. Such poorly formed silicide inter-grain regions would cause the observed degradation in sheet resistance. The resistance of polycide lines would increase significantly where their width is comparable to the grain size, since a line could be completely blocked by a single grain boundary. As shown in Fig. 2-1-17, the inter-grain regions completely block a 0.1 μm-wide line.

2-1-3. Analysis of sheet resistance behavior in NiSi

I tum now to the case of NiSi, which in Fig. 2-1-2 is seem to suffer from no sheet resistance degradation.

1) Electrical Characteristics of 0.1 μm Lines

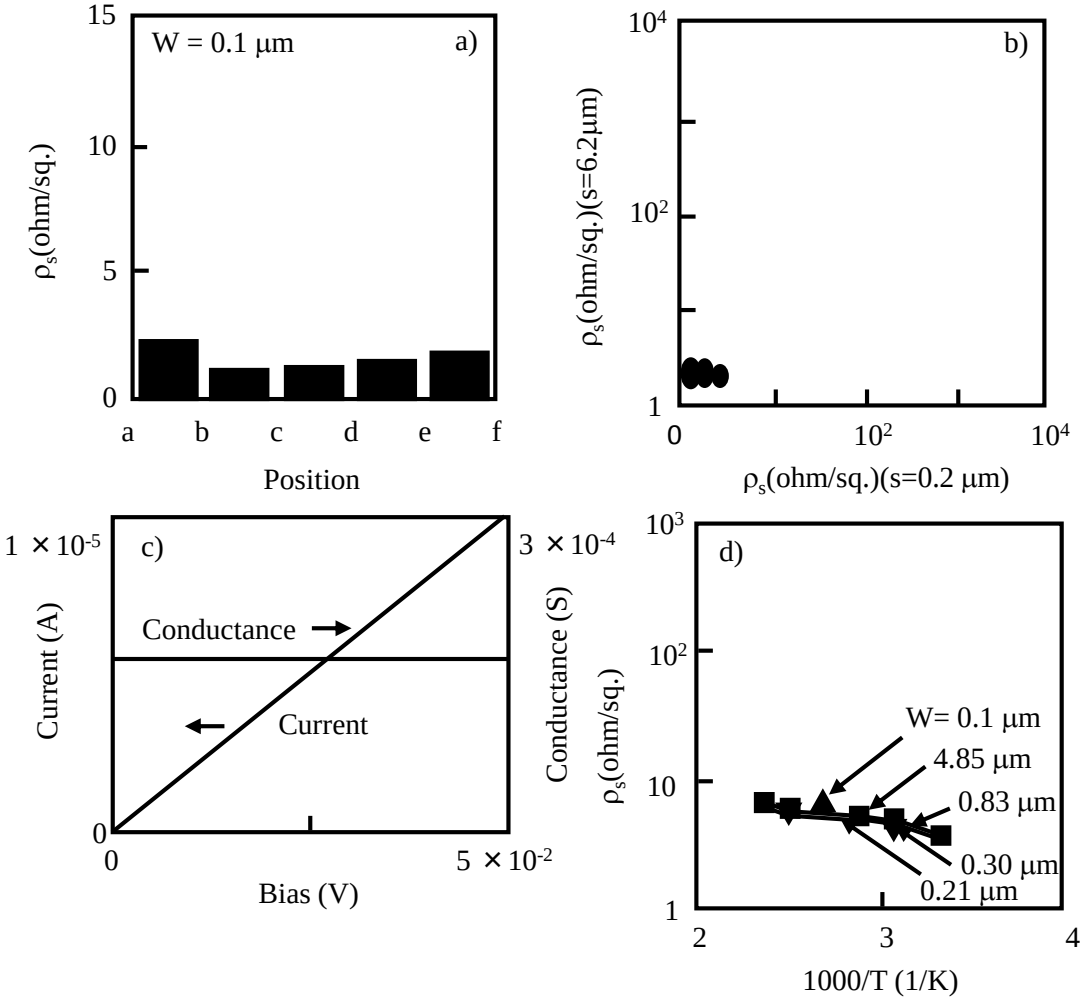


Figure 2-1-18. Electrical characteristics of arsenic-doped NiSi-polycide.

The electrical characteristics of 0.1 μm NiSi-polycide lines are shown in Fig. 2-1-18. Figure 2-1-18(a) gives a typical example of NiSi-polycide sheet resistance from individual sections of the test pattern used previously for the $TiSi_2$ -polycide measurements. The sheet resistance is uniform throughout all the sections and its value stays small. The correlation between NiSi polycide sheet resistance extracted from 0.2 μm-long sections and that for the whole 6.2 μm length of the same 0.1 μm line is shown in Fig. 2-1-18(b). The variations in resistance between the 0.2 μm-long and 6.2 μm-long sections are very small. The I-V characteristics of long lines are ohmic, as shown in Fig. 2-1-18(c).

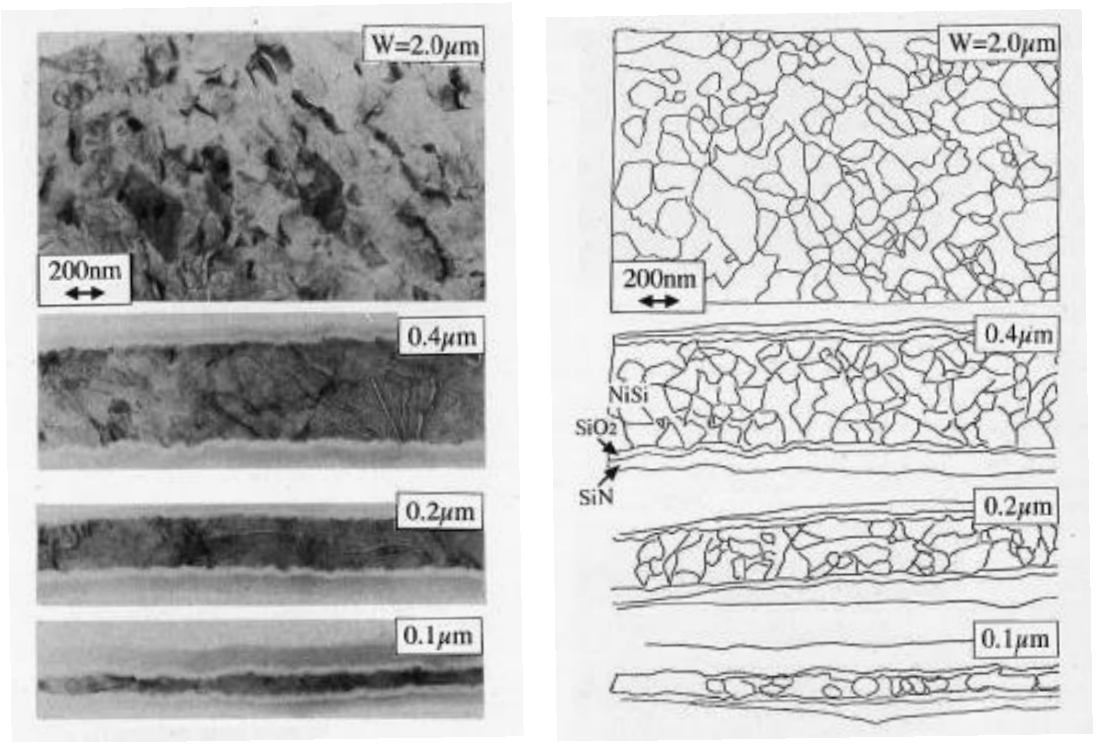


Figure 2-1-19. TEM photograph of arsenic-doped NiSi polycide cross section.

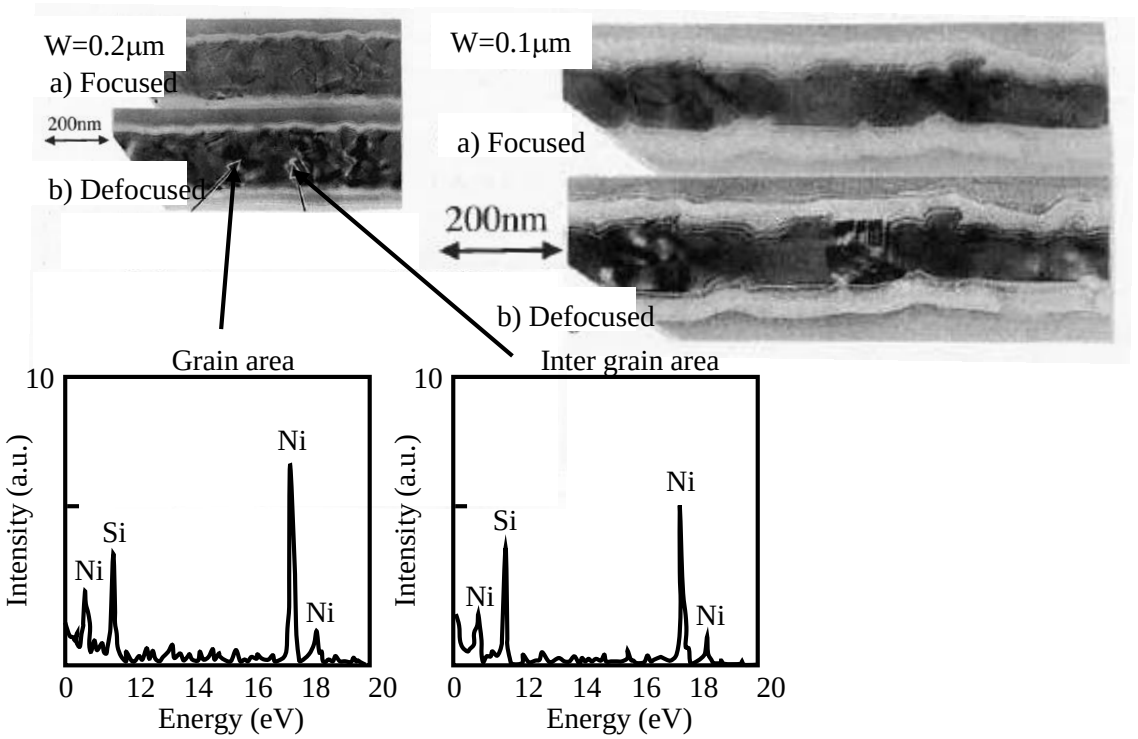


Figure 2-1-20. TEM and EDX analysis of grain boundary regions for NiSi-polycide.

These results suggests that NiSi-polycide has a tiny and quite uniform structure. No negative temperature coefficient of resistance can be seen even in the case of a 0.1 μm line, as shown in Fig. 2-1-18(d). The grains and their boundary structure seem different from those seen in the $TiSi_2$ case. The electrical characteristics of 0.1 μm NiSi-polycide lines . Results of TEM observations at different widths of NiSi-polycide lines are shown in Fig. 2-1-19. In contrast with the $TiSi_2$ case, the grain size is very small at least half that of $TiSi_2$ case. As the polycide line width is reduced, it is interesting to note that the grains seem to become larger. In the case of a 0.1 μm-wide line in particular, the grains appear to grow in the line's axial direction until they finally connect tightly together. The result is a straight polycide line boundary. This is in great contrast with the 0.1 μm $TiSi_2$- polycide line, where the grain:, seem to link up very poorly and their boundaries are very rough. Careful TEM investigations of the grain boundaries, which are shown in Fig. 2-1-20, have allowed us to deduce that NiSi-polycide contains no intergrain layers such as those seen in the $TiSi_2$ case. In fact, the results of EDX analysis of the grains and their boundaries, which are also shown in the figure, indicate that there is no compositional difference in the silicides. This tight linking of the grains and the absence of an inter-grain region explains why there is no degradation in sheet resistance in the case of NiSi-polycide.

Line Width Dependence of' NiSi Film Thickness

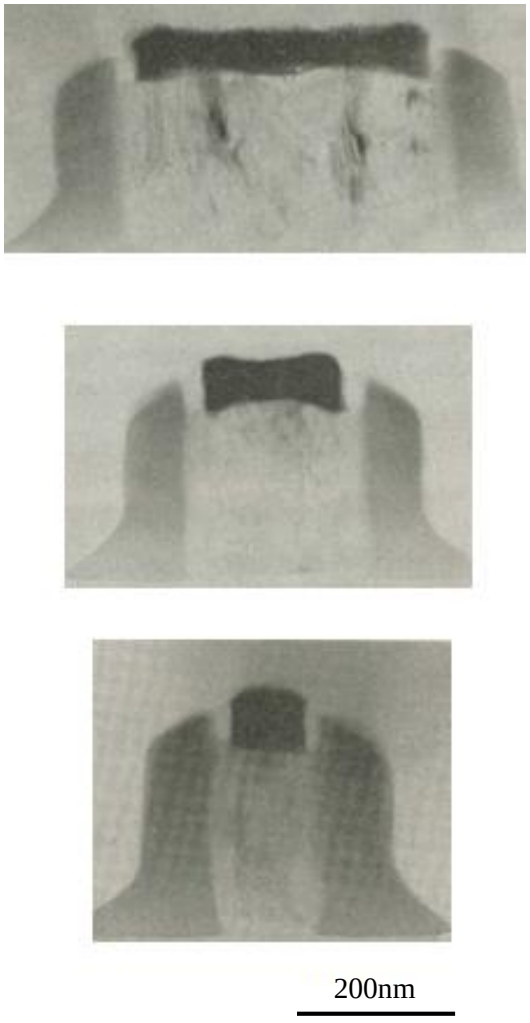


Figure 2-1-21. TEM photograph of NiSi polycide cross section.

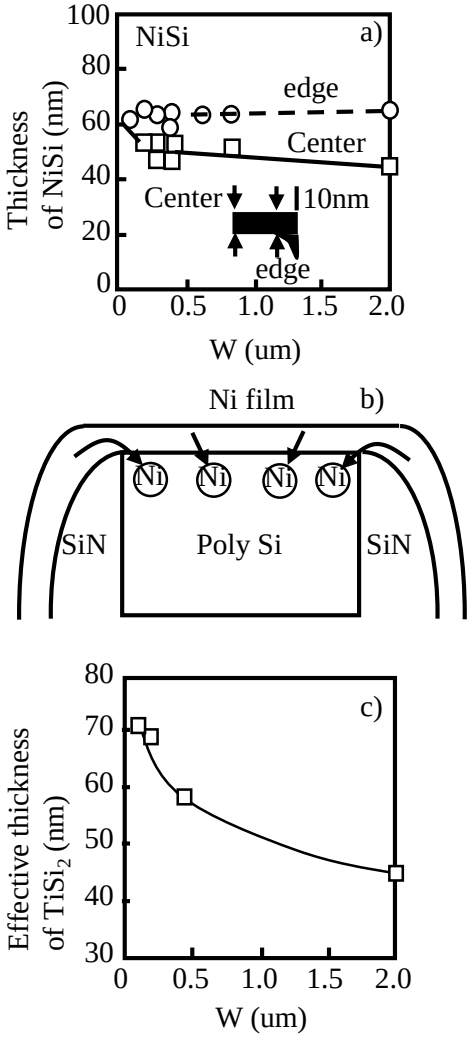


Figure 2-1-22. Line width dependence of NiSi film thickness.

In the NiSi case, a slight decrease in sheet resistance was observed as the line width was reduced, as previously mentioned. It has also been noted that the NiSi film is thick at W = 0.1 μm [21]. The dependence of NiSi film thickness on position in the polycide line was investigated by TEM observations, as shown in Fig. 2-1-21. This showed that film thickness is greater at the line edge than at the center. This is the converse of the $TiSi_2$ case. Film thickness at the edge and at the center, as well as effective film thickness *(teff =S/W,* where *S* is the cross-section of the NiSi film, and *W* is the width of the polycide), are plotted against polycide width in Figs. 2-1-22(a) and (c).

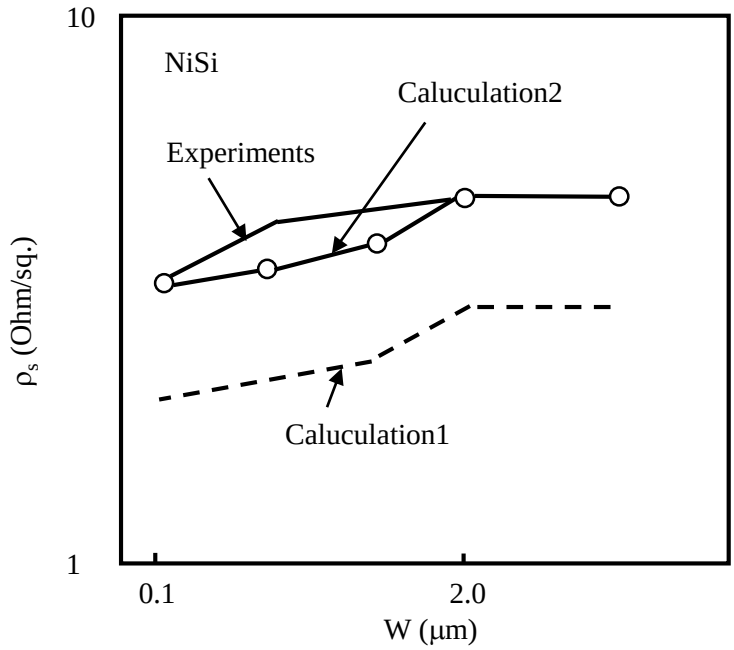


Figure 2-1-23. Line width dependence of NiSi polycide calculated after taking into account effective NiSi film thickness.

The thicker silicide at the edge of the polycide is thought to arise as a result of the NiSi silicidation mechanism described in Fig. 2-1-22(b). In the case of NiSi silicidation takes place in the polysilicon film by Ni diffused from the Ni film. A thicker silicide is formed at the edge since more Ni atoms are supplied there than at the center. Thus an arrow NiSi-polycide line has a relatively larger area of this thicker silicide. On the basis of the line dependence of effective NiSi film thickness, the sheet resistance of the NiSi-polycide is calculated and plotted against line width in Fig. 2-1-23. In this calculation, a bulk resistivity value of 21 μohm-cm [22] is adopted for NiSi. As in the $TiSi_2$ case, the results of calculations based on this bulk resistivity value (the dotted line: Calculation-1) are significantly lower than experimental results of the thin film effect. After fitting the calculated curve at W = 10 μm. the solid line (Calculation-2) results. This agrees very well with the experimental values. Thus the slight rise in sheet resistance with falling line width can be explained quantitatively in terms of the effective thickness of the NiSi-polycide line.

2-1-4. Analysis of sheet resistance behavior in $CoSi_2$

Grain Structure and Line Width Dependence of' $CoSi_2$ Film Thickness

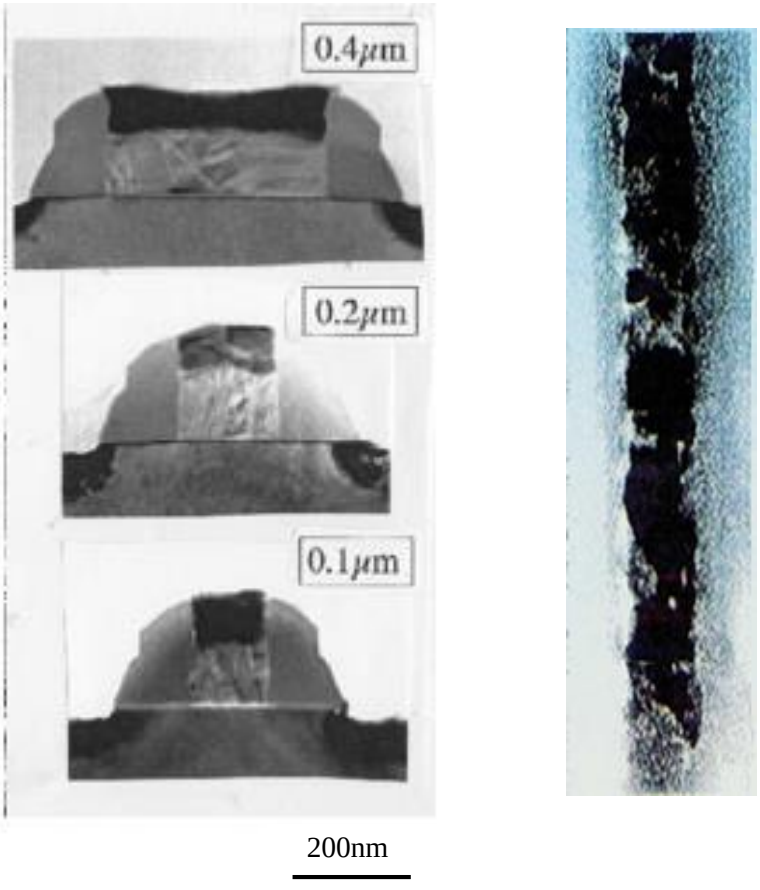


Figure 2-1-24. TEM photograph of $CoSi_2$.

Fig. 2-1-24 shows TEM photograph of $CoSi_2$. Narrow line effect in $CoSi_2$ is suppressed as well as NiSi because no agglomeration in 100 nm gate length is observed and the silicide thickness of gate edges becomes thicker as gate length decreases. This is caused by that diffusion species is Co during silicidation process.

In order to realize higher operation speed of digital circuits and higher gain of mixed-signal and RF circuits, not only scaling gate length but also lower gate resistance is required. Because higher gate resistance causes gate RC delay in digital case and the resistance causes higher power loss at gate electrode. Thus, lower sheet resistance of NiSi and $CoSi_2$ in narrow line means this silicide material are suitable for digital, mixed-signal and RF circuits than $TiSi_2$.

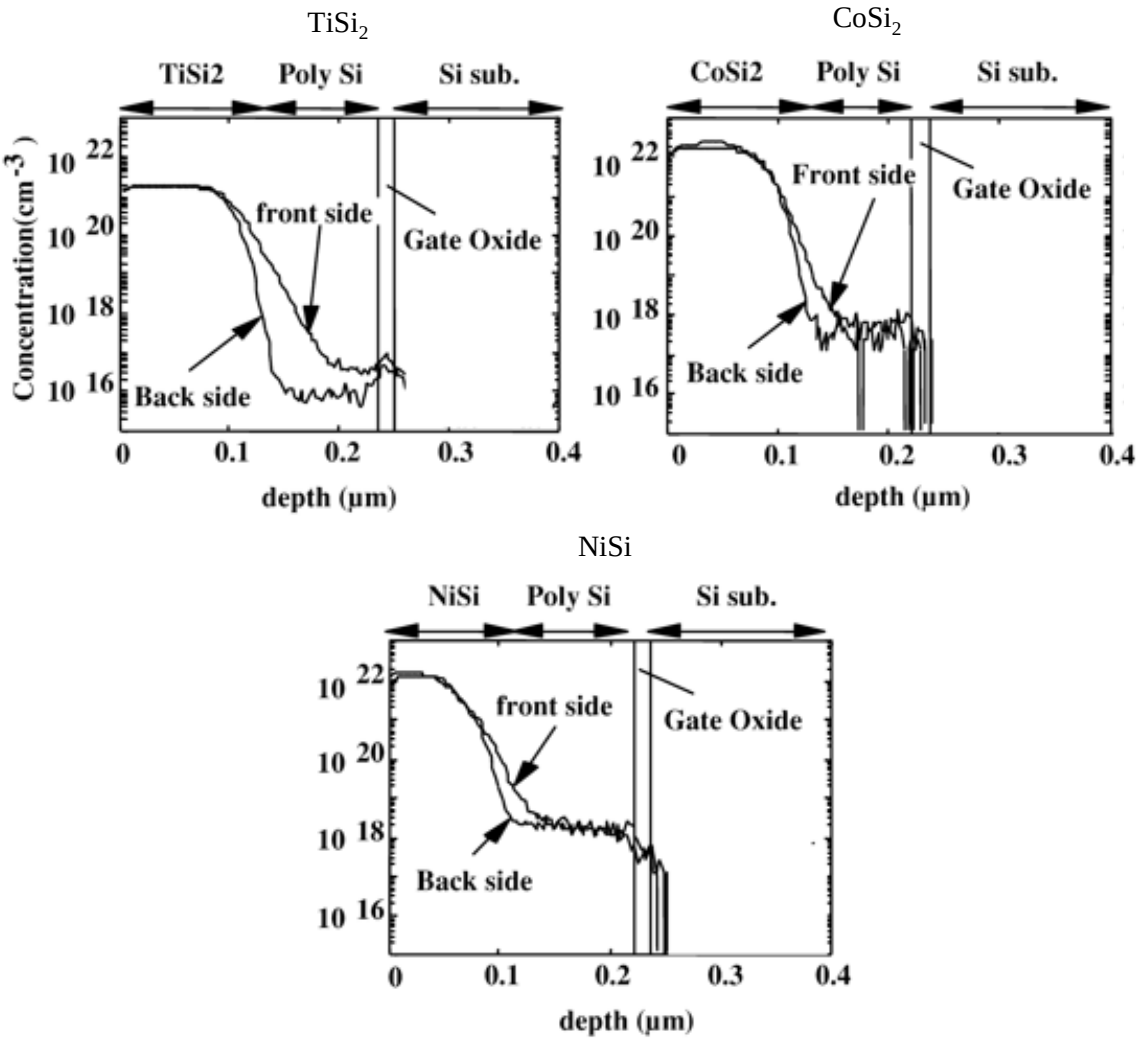


Figure. 2-1-25. SIMS profiles of poly-Si with silicide.

Figure 2-1-25 shows silicide metal profile in gate poly Si, gate insulator and Si substrate evaluated by SIMS. I measured the SIMS from both front side and back side. The profile of front side case is bower than that of back side case because of knock on effect. Thus, back side data is truer data. According to these profile, the metal diffuses to gate insulator and Ti and Ni seem to diffuse in Si substrate. However, no degradation in gate insulator reliability measurement such as TDDB were observed for three silicide materials. Additionally, MOSFETT normally operates. Thus, I consider no diffusion of Ti, Co and Ni in gate insulator and Si substrate.

Conclusion

The dependence of sheet resistance on line width has been investigated in detail for $TiSi_2$ and Nisi polycides. In the $TiSi_2$ case, resistance increases with falling line width, while conversely, in the NiSi case, it decreases slightly with falling line width. The sheet resistance increase in the $TiSi_2$ case was investigated in detail. It was found that the relationship between sheet resistance and line width, W is characterized by three distinct regions according to W. In region A *(*W >1-2 μm), the sheet resistance is independent of line width and is low valued. In region B (1-2 μm > W > 0.2 μm), the sheet resistance increases moderately. In region C (W<0.1 μm), there is an abrupt increase in sheet resistance. The mechanisms of these sheet resistance increases in regions B and C were investigated using TEM and EDX analysis in combination with electrical measurements with a newly developed test pattern. These investigations demonstrated that the mechanism is not simple.

In region B, the major cause of the sheet resistance increase is the greater C49 content in the narrow polycide line. The line width dependence of the ratio of C49 and CS4 content was also obtained quantitatively by TEM analysis. The line width dependence calculated based on the content ratio agrees with the experiments very well. In region *C,* there are two major causes for the abrupt sheet resistance increase. One is the reduced effective $TiSi_2$ film thickness in very narrow lines, the other being the barrier to conduction formed by inter-grain regions extending completely across the very narrow polycide line. This decrease in film thickness was found by cross-sectional TEM analysis, and can explained by the silicide at ion mechanism. The electrical characteristics of the inter-grain layer were analyzed to a spatial resolution of 0.2 μm using a specially developed test pattern in combination with TEM analysis. In contrast, no such inter-grain layers arise in NiSi films, and the grains link together very tightly. The film thickness even increases as line width is reduced. NiSi-polycide exhibits good resistance values even with 0.1 μm lines. Thus the NiSi process had been a suitable candidate to replace $TiSi_2$ since 180 nm CMOS devices. Beyond 65 nm technology, NiSi has been used for the CMOS production.

2-2 Analysis of junction leakage current degradation of NiSi

2-2-1. Suppression of junction leakage degradation of NiSi formed on arsenic doped Si substrate

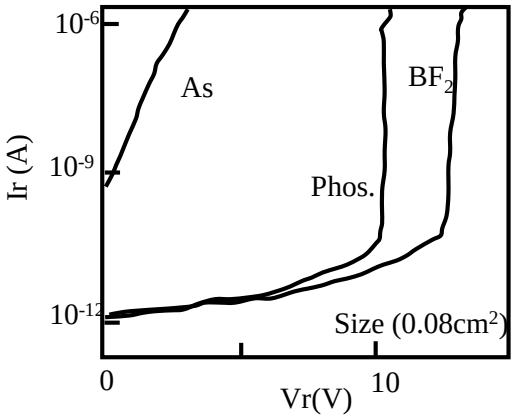


Fig. 2-2-1. Junction leakage current on BF_2 implanted p+/n and Phosphorous or Arsenic implanted n+/p junction.

Fig. 2-2-2. TEM photograph of NiSi film on Arsetnc implanted Si-sub near field oxide.

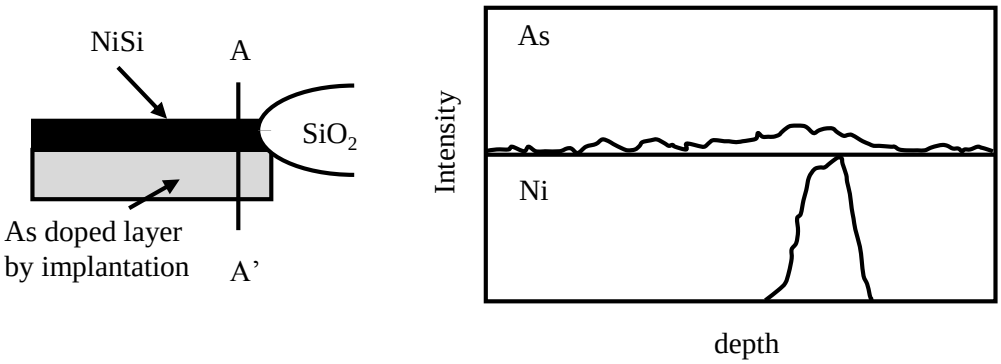
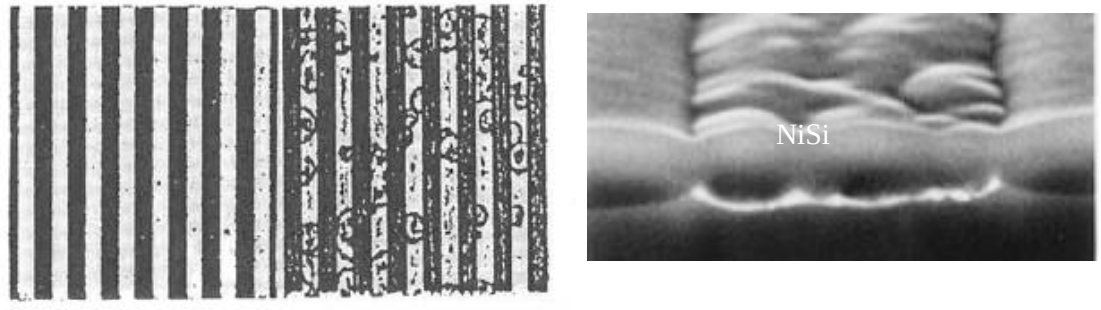


Figure 2-2-3. EDX analysis of the NiSi film on Arsentic implanted Si-sub.

As the device dimension falls into lower submicron to 0.1 μm range, the stable silicidation temperature range of $TiSi_2$, however, becomes too high for the lower process temperature of the small geometry MOSFETs. In addition, it was found that the sheet resistance of a Ti-salicided gate electrode increases significantly as the line width decreases as shown in Fig. 2-1-2 [8, 23]. On the other hand, NiSi is formed stably at a lower temperature [11] and has been discovered to show no sheet resistance degradation [24]. However, anomalously large junction leakage currents have been often observed in nickel silicided arsenic doped source and drain layers of MOSFETs. This phenomenon has not been observed in the cases of phosphorous doped and boron doped layers also shown in Fig. 2-2-1.



a) Before SiO_2 deposition b) After SiO_2 deposition

Figure 2-2-4. SEM photograph of the NiSi film on Arsentic implanted Si-sub after SiO_2 deposition.

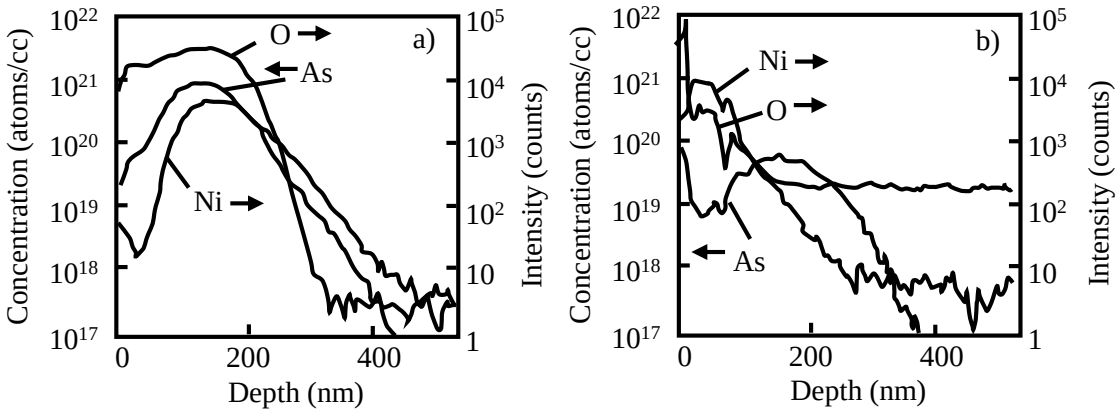


Fig. 2-2-5. SIMS analysis of another layer between NiSi and SiO_2. a)Arsenic implanted Si-sub b) $BF2^+$ implanted Si-sub.

In this section, I describe the results of analysis of the anomalously large leakage current, and shows the solution by using TiN capped silicidation process.

Junction leakage often occurs at the field edge by silicide encroachment. Thus, this was investigated at first. Figure 2-2-2 shows TEM photograph of a nickel silicided arsenic doped drain layer at the field edge. From the figure no NiSi encroachment at the field edge was observed. Figure 2-2-3 shows the Ni and As profiles measured by EDX at the field edge. This result shows Ni is within As doped region and no NiSi encroachment at the field edge as well as Fig. 2-2-2. It has been found that morphology of NiSi films on As doped silicon layer sometimes becomes very rough after CVO SiO_2 deposition on the silicide as shown in Fig. 2-2-4, though the morphology of the films before the CVD SiO_2 deposition was confirmed to be very good. From the SEM photograph of Fig. 2-2-4, the variation in the thickness of the silicide layer was found to be 200 nm, while the As doped junction depth was 100 nm.

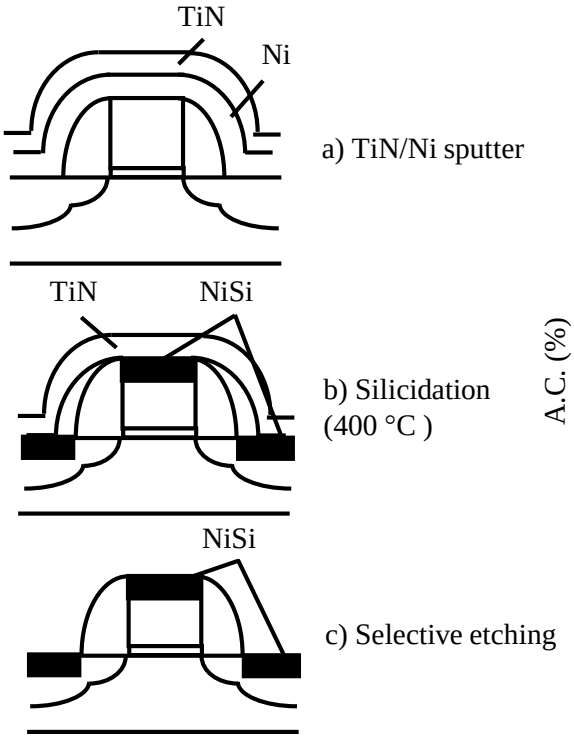


Fig. 2-2-7. Process flow of TiN cap Silicidation.

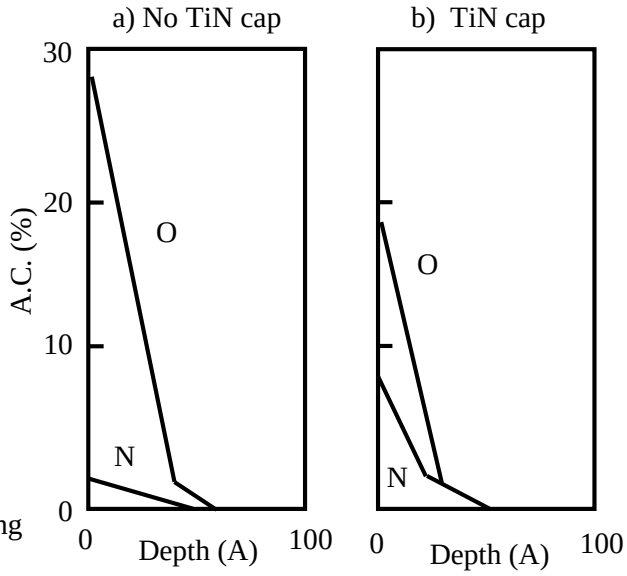
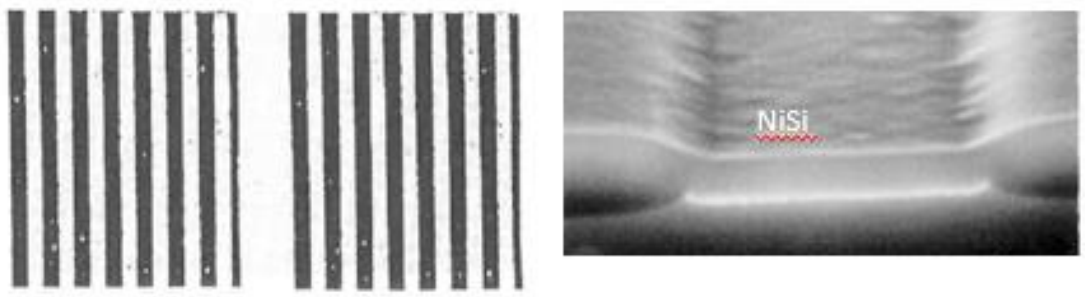


Fig. 2-2-8. AES analysis of NiSi film on Arsenic implanted Si-sub a) No TiN cap b) TiN cap.



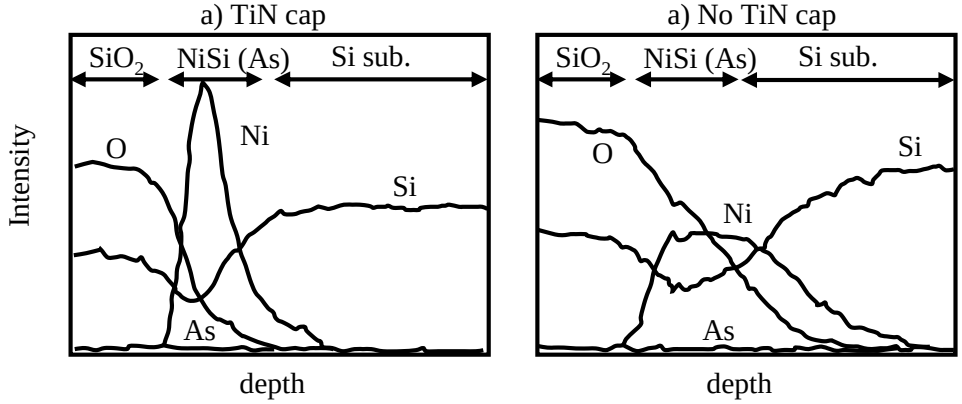
a) Before SiO_2 deposition

b) After SiO_2 deposition

Fig. 2-2-9. SEM photograph of the NiSi film on Arsenic implanted Si-sub by using TiN cap Process.

This roughness is the cause of the junction leakage current. SIMS analysis shown in Fig.2-2-5(a) indicates that this irregular silicided layer is composed of the compound of Ni, Si, O and As. Such a complicated compound was not observed in the case of NiSi on the B or P doped silicon layer. Note that in the case of B (Fig. 2-2-5(b)). the oxygen concentration is one order of magnitude smaller than that of As case (Fig. 2-2-5(a)). The large amount of As and O is estimated to be absorbed in the silicide layer at the silicidation process. Figure 2-2-7 shows TiN cap process during Ni silicide process. After fabrication of MOSFET and removal oxide film on Si substrate and poly Si by wet treatment, in conventional case, just Ni film is deposited, but in new process, Ni and TiN are deposited in series by sputtering. This TiN cap prevents the oxidation of nickel during the silicidation. The thickness of TiN film is 30 nm. During Ti sputtering process, Ar and nitrogen gas are used to react Ti and nitrogen. Oxygen profile immediately after the Ni silicidation for the As doped sample measured by AES indicates that there is huge amount of oxygen in the surface region of the silicide as shown in Fig. 2-2-8(a). Involvement of the huge amount of oxygen can be prevented by using TiN cap during the silicidation as shown in Fie. 2-2-8(b).

Figure 2-2-9 shows the morphology of NiSi films on As doped silicon layer before and after CVO SiO_2 deposition. No abnormal oxidation film was observed and the surface of NiSi film was very smooth by TiN cap process.



F! g. 2-2-10. AES analysis of NiSi film on arsenic-implanted Si-substrate after CVD SiO_2 deposition a) TiN cap b) No TiN cap.

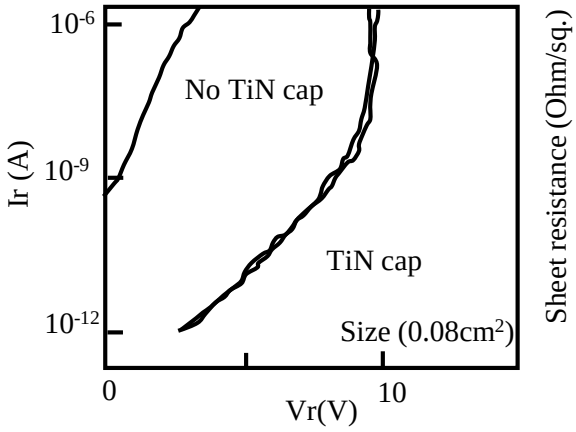


Figure. 2-2-11. Junction leakage current on Arsenic implanted n+/p junction by using TiN cap and No TiN cap.

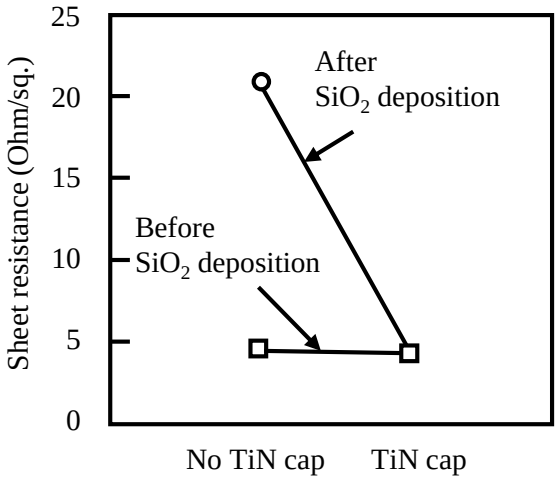


Figure. 2-2-12. Sheet resistance of Ni silicided Arsenic implanted Si-sub by using TiN cap or No TiN cap.

Figure 2-2-10 shows AES analysis of NiSi film after CVD SiO_2 deposition in TiN cap and No TiN cap process. This result indicates irregular layer did not exist in the case of TiN cap proces. AES profile of TiN capped sample shows shallow NiSi layer as shown in Fig. 2-2-10(a), while that of without the TiN cap shows deeper oxidized Ni silicided regions as shown in Fig. 2-2-10(b). The junction leakage current of NiSi by TiN cap process was improved significantly comparing with that of no TiN cap as shown in Fig. 2-2-11. A little bit weaker breakdown characteristics of TiN capped As junction in Fig. 2-2-11 than that of P or B in Fig. 2-2-1 is due to the difference of the junction profile of As, P, and B junctions. Note that Xj of As layer was 0.1 μm - 0.15 μm, while that of P or B was 0.2 μm. These indicate the profile of As is more abrupt than that of P or B. The sheet resistance of NiSi film by TiN cap process was 5 times smaller than that of irregular silicided layers with non capped process as shown in Fig. 2-2-12.

2-2-2. Nitrogen-doped nickel mono-silicide technique

i) Sample fabrication

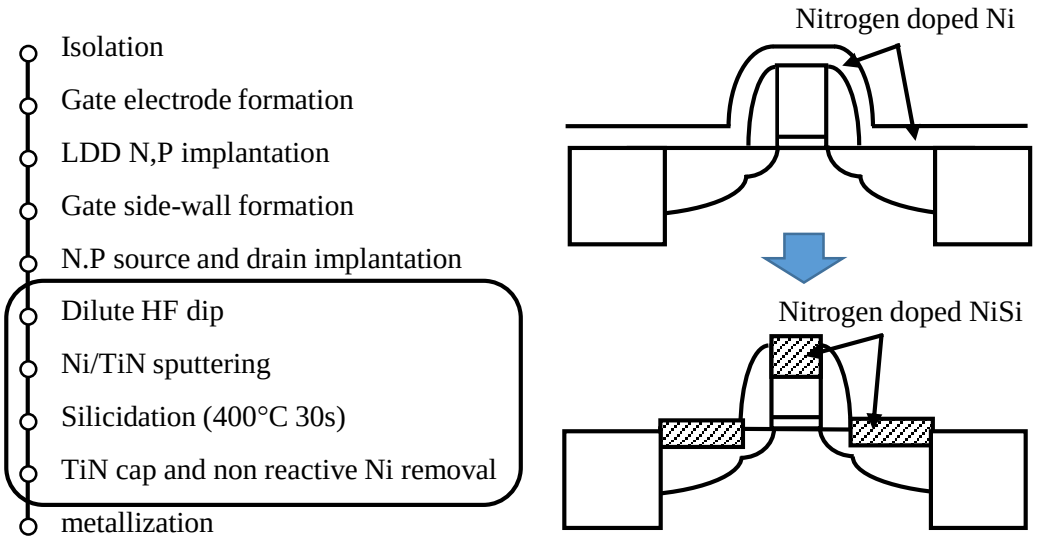
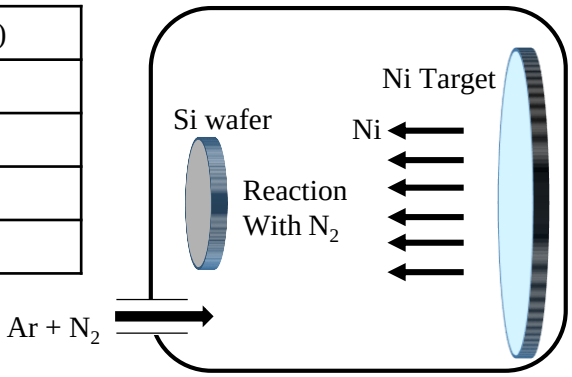


Figure 2-2-13. Process flow for nitrogen doped NiSi formation.

N_2 (%)	Ar (%)
0	100
2.5	97.5
5	95
10	90



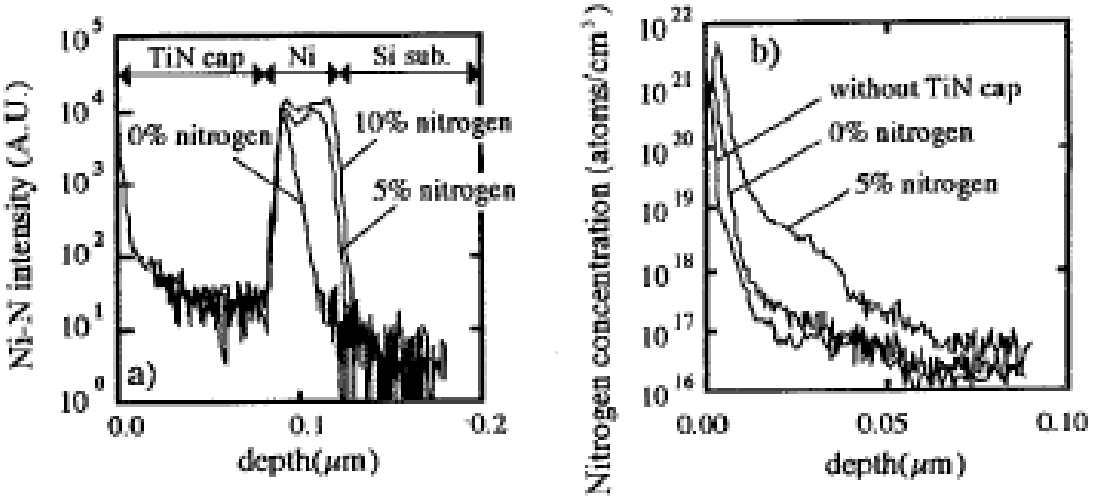


Figure 2-2-14. SIMS profile of (a) as sputtered Ni films and b) NiSi films.

As shown in Fig. 2-1-2, NiSi is suitable for digital, mixed signal and RF circuits because no degradation of sheet resistance when the gate length is below 0.1 μm. However, anomalously large junction leakage current and sheet resistance degradation have often been observed with this material. I have previously found that this problem is due to a very rough interface between the silicide layer and the silicon substrate; this is caused by oxidation of the NiSi film during the thermal process (especially in the case of silicide on arsenic doped diffused layers). I proposed the TIN cap method to overcome the problem. With this method, a nitride layer covers the surface of the NiSi to prevent oxidation, and thus suppressing interface roughness to a certain degree. However, even the TIN cap method is incapable of adequately suppressing roughness in the case of recent ultra-shallow source and drain junctions, since the nitride layer is so thin [25]. In this section, I propose a nitrogen-doped nickel mono-silicide technique. In order to more positively form the nitride on the NiSi film, nitrogen is introduced into the nickel film by sputtering the nickel in a mixture of argon and nitrogen. Results showing that the roughness of the interface is significantly improved are described, along with the electrical characteristics of MOSFETs with this nitrogen-doped NiSi in this section.

Figure 2-2-13 shows the process flow for a 0.15 μm CMOS device with nitrogen-doped NiSi salicide. After source and drain formation, the wafer is dipped in dilute HF. At this stage, Ni and TiN films are deposited by sputtering. The Ni sputtering is carried out in argon gas with added nitrogen. Table 2-2-1 shows the volume percentage of nitrogen and argon gases during the sputtering process. Silicidation was carried out by annealing at 400°C for 30 seconds in a nitrogen ambient. The TIN and non-silicided Si films were removed by treatment with a mixture of H_2O_2 and H_2SF_4.

Figure 2-2-14 shows SIMS profiles of the as-sputtered Ni films and NiSi films. Significantly large amounts of nitrogen are involved in the as-sputtered Ni films where sputtering has taken place in the mixed Ar and N_2 gas (Fig. 2-2-14(a)). After silicidation, the nitrogen concentration in the NiSi film is, of course, small. In the TiN cap case, a large concentration of nitrogen - which has diffused from the TiN - exists at the NiSi surface even with 0 % nitrogen sputtering. However, the nitrogen concentration falls rapidly with depth. In the case of mixed gas sputtering, it is confirmed that the nitrogen concentration increases with depth in the NiSi film.

ii) Experimental results

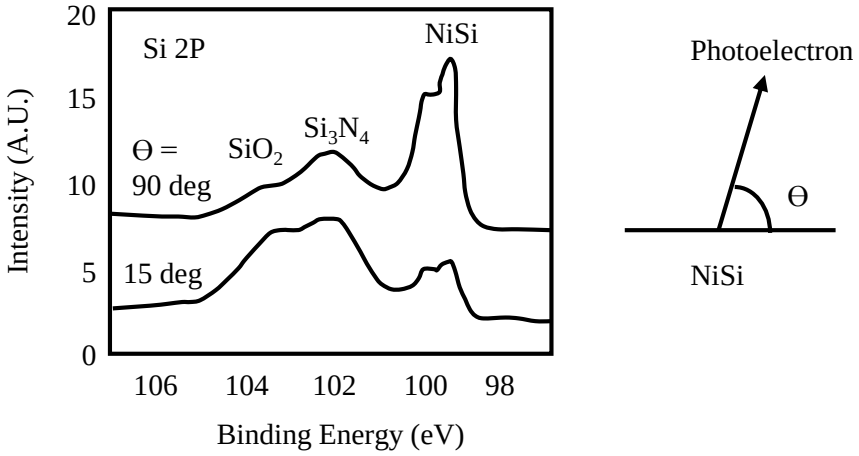


Figure 2-2-15. XPS analysis for 15 and 90 deg.

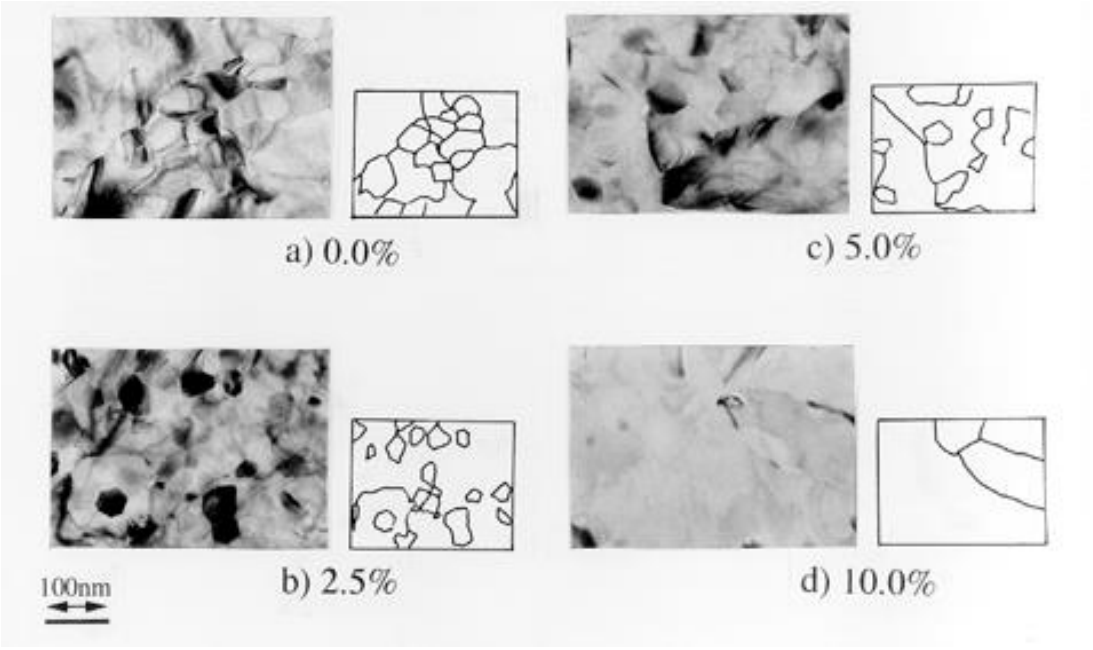


Figure 2-2-16. TEM photographs of Nisi for various nitrogen concentration(top view).

Using XPS analysis, it was found that nitrogen combines with Si to form Si_3N_4, as shown in Fig. 2-2-15 and this is assumed to suppress oxidation of the silicide. Figure 2-2-16 shows TEM photographs of the NiSi with various nitrogen concentrations after removing the TIN cap. The % represents the nitrogen concentration in the mixed gas. The grain size becomes larger as the nitrogen concentration increases. This results are expected that the resistivity becomes lower with be larger the grain size and the nitrogen doped NiSi is suitable for advanced CMOS because the parasitic resistance of source and drain becomes lower even if the NiSi thickness is thinner.

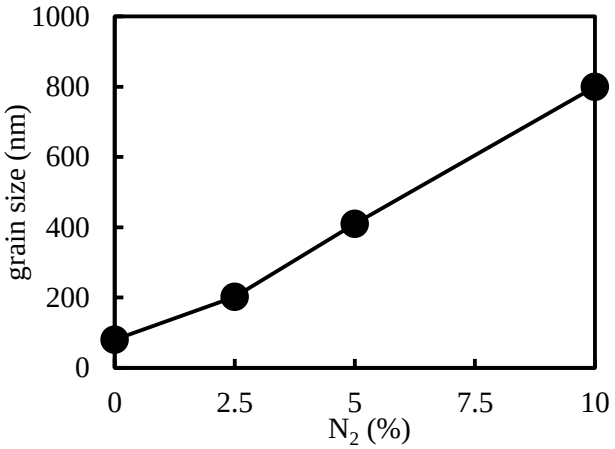


Figure 2-2-17. Dependence of grain size on nitrogen gas concentration.

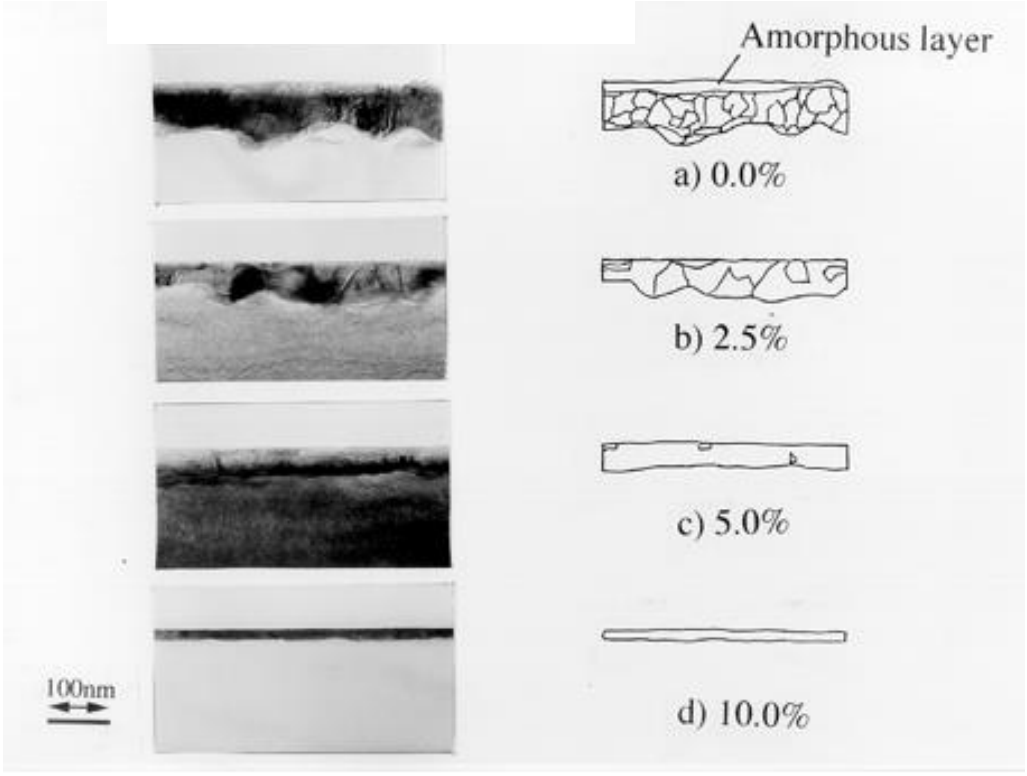


Figure 2-2-18. TEM photographs of NiSi for various nitrogen concentration (Cross section).

Fig. 2-2-17 shows dependence of grain size on nitrogen gas concentration. The size in 5 % nitrogen gas becomes 4 times that in 0 % nitrogen gas. The magnified view of part of a TEM cross section at the bottom of the silicide shown in Fig. 2-1-16 suggests that the crystals in the grains are aligned with those on the Si substrate. Figures 2-2-18 shows TEM photographs of the cross section of the NiSi with various nitrogen concentrations after removing the TIN cap (the figure indicates the nitrogen concentration in the mixed gas). The roughness at interface between NiSi and Si substrate becomes smaller as the nitrogen concentration increases.

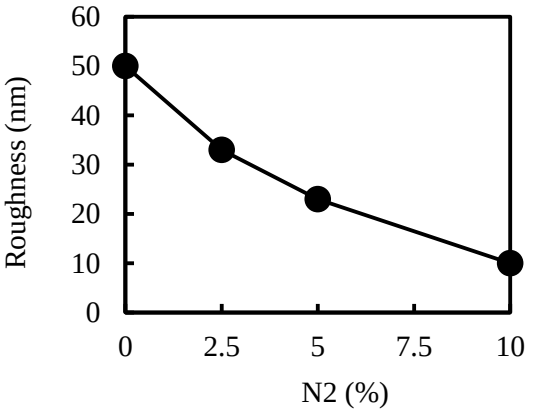


Figure 2-2-19. Dependence of roughness on nitrogen gas concentration.

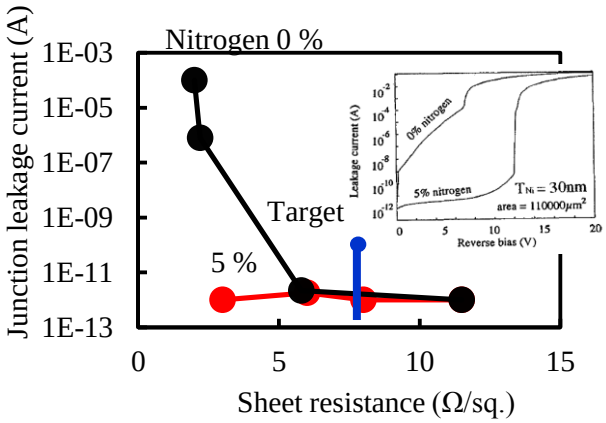


Figure 2-2-20. Dependence of leakage current on sputter thickness for various nitrogen concentration.

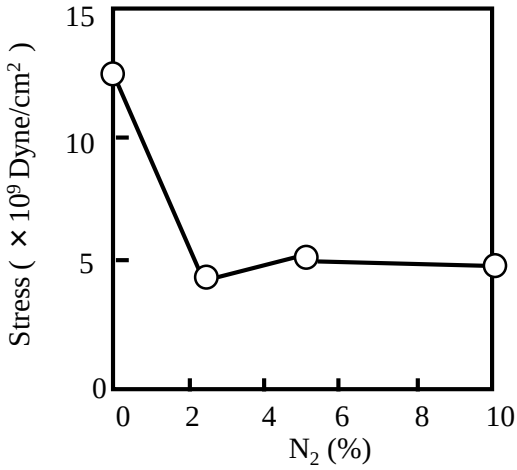


Figure 2-2-21. Dependence ol NiSi film stress on nitrogen gas concentration.

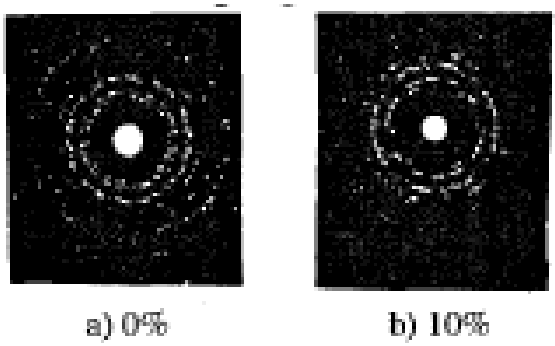


Figure 2-2-22. Electron diffraction. (measured arca is 3ccm *Φ).*

The roughness in 5 % nitrogen becomes half of that in 0% case as shown in Fig 2-2-19. This results are expected that junction leakage current becomes smaller as the concentration increases and this nitrogen doped NiSi is suitable for advanced CMOS because the junction depth of source and drain becomes shallower. Figure 2-2-20 shows dependence of leakage current on the sheet resistance of NiSi. In 5 % nitrogen case, the current is lower than 0 % case when the sheet resistance are same because the roughness in 5 % case is smaller than that in 0 % case. Figure 2-2-21 shows dependence of NiSi film stress on nitrogen gas concentration. Not only larger grain size and the smaller interface roughness but also the stress in the NiSi film drops as the nitrogen concentration increases. Figure 2-2-22 shows electron diffraction results of NiSi with a 0 % and 10 % nitrogen concentration. This results show crystal quality of 10 % nitrogen NiSi is better than that of 0 % case.

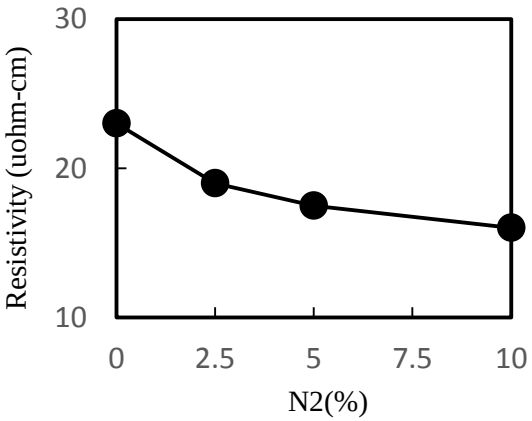


Figure 2-2-23. The dependence of resistivity on nitrogen gas rate.

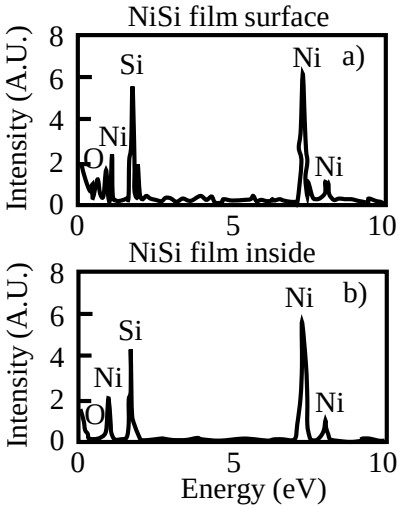


Figure 2-2-24. EDX analysis of a) NiSi lilm surlacc and b) NiSi inside for 0 % sample.

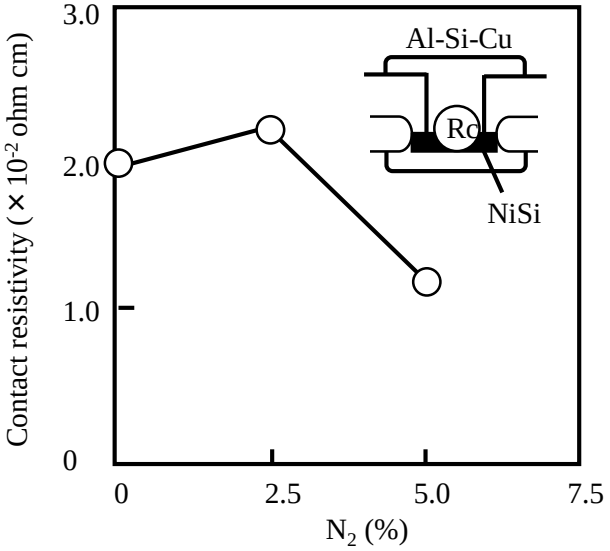


Figure 2-2-25. Dependence of contact resistance on nitrogen gas concentration.

Figure 2-2-23 shows dependence of resistivity on nitrogen gas rate. The resistivity decreases with nitrogen concentration because the grain size becomes larger. These advantageous qualities of NiSi films with higher nitrogen concentration are assumed to arise because of suppression of oxidation. In fact, NiSi with a lower nitrogen concentration contains an amorphous layer. This amorphous layer was found to be an oxide layer using EDX as shown in Fig. 2-2-24. Figure 2-2-25 shows dependence of contact resistivity on nitrogen gas rate. The resistivity decreases with nitrogen concentration because the grain size becomes larger. These advantageous qualities of NiSi films with higher nitrogen concentration are assumed to arise because of suppression of oxidation. In fact, NiSi with a lower nitrogen concentration contains an amorphous layer. This amorphous layer was found to be an oxide layer using EDX as shown in Fig. 2-2-24.

Conclusion

Anomalously large junction leakage current of Ni salicided arsenic doped junction has been investigated. It has been found that this is caused by irregularly rough shaped silicide layer composed by Si, O, Ni, As compound. It has been shown that this can be prevented by suppressing the oxidation of NiSi during the silicidation by TiN cap. However, even the TIN cap method is incapable of adequately suppressing roughness in the case of recent ultra-shallow source and drain junctions, since the nitride layer is so thin. Thus, A nitrogen-doped NiSi technique has been developed. It was found that the nitrogen suppresses oxidation of the silicide film because nitrogen combines with Si to form Si_3N_4 on the NiSi surface, resulting in significantly reduced roughness at the interface between silicide and the Si substrate. As a result, the leakage current through the silicided ultra-shallow diffused layer was significantly suppressed. The stress in the NiSi film drops as the nitrogen concentration increase, corresponding to the reduction in the roughness. Further, the nitrogen-doped NiSi film has the advantage of containing large single crystal grains, and this reduces the resistivity of the film.

After my paper "Nitrogen-doped nickel monosilicide technique for deep submicron CMOS salicide," *in IEDM Tech. Dig.*, pp. 453 - 456, December 1995 [26], several paper were submitted in order to improve the MOSFET with nitrogen doped NiSi. The process is however, difference from my proposal, that is not nitrogen doped in Ni sputtering but nitrogen implantation to Si substrate before Ni sputtering. The nitrogen doped NiSi by the implantation brings some effective improvements. 1) suppression of boron and arsenic in the NiSi to have hot carrier immunity [27-29] 2) Precise control of NiSi thickness [30] 3) Improvement of thermal stability of NiSi [31,32]. These papers show the nitrogen has an important role for better NiSi characteristics and MOSFET with the NiSi.

2-3. Application silicide to scaling MOSFET for high performance power amplifier

Table 2-3-1. Reported power device.

Device	Gate	L_g (μm)	Freq. (GHz)	V_d (V)	W_g (μm)	Power (W)	PAEmax (%)	Ref.
Si MOS	Mo	1.3	0.86	7.5	69	5	60	[1]
		0.8	1.5	6.0	7.5	3	55	[2] [3] [4]
				4.8		2	50	
			1.75			2	46	
			1.5	3.6		1	40	
Si MOS	$MoSi_2$ /Mo /$MoSi_2$	0.35	0.9	3.0	1.6	0.25	55	[5]
			1.5			0.23	36	
			2.0			0.13	33	
GaAs	-	0.15	0.9	1.5	40	1.4	66	[6]
HJFET	-	1/0	0.95	1.2	28	1.1	63	[7]

Mobile phone applications have generated considerable demand for telecommunications ICs with low power consumption. Low power consumption is achieved by reducing the supply voltage, so low-voltage techniques are crucial in this field. On the other hand, however, the transmission power of RF power amplifiers also falls when the supply voltage is reduced, and this can present major problems. However, depending on how high the required emission, it is often desirable to reduce the power amplifier supply voltage in line with the operating voltage of other ICs, such as high speed logic circuit, in the mobile system, because otherwise two separate supply voltages would be necessary. It should also be noted that the maximum permissible supply voltage, as defined by MOSFET reliability, has fallen with progress in LSI technology that has reduced MOSFET gate lengths. Table 2-3-1 shows a history of RF power Si-MOSFETs, showing clearly that supply voltage has continued to decrease. In 1983, Si power MOSFET's with Mo gate electrodes were reported by Itoh *et al.* [34]. Supply voltage and gate length were 7.5 V and 1.3 m, respectively, in this device. By 1992, the supply voltage of production-level devices had fallen to 6.0 V with shorter 0.8 μm Mo gates. In the same years, Si power devices operating at 4.8 V and 3.6 V, respectively, were reported at the research level by Yoshida *et al.* [35]–[37]. In these devices, the gate material was Mo and the gate lengths were 0.8 and 0.6 μm, respectively. Later, in 1995, we demonstrated a high PAE (maximum power-added efficiency) of more than 50 % at 900 MHz even at the low supply voltage of 3 V by reducing the gate length to 0.35 μm [38]. In these devices, the gate structure was Mo sandwiched between $MoSi_2$ layers.

2-3-1. Sample fabrication

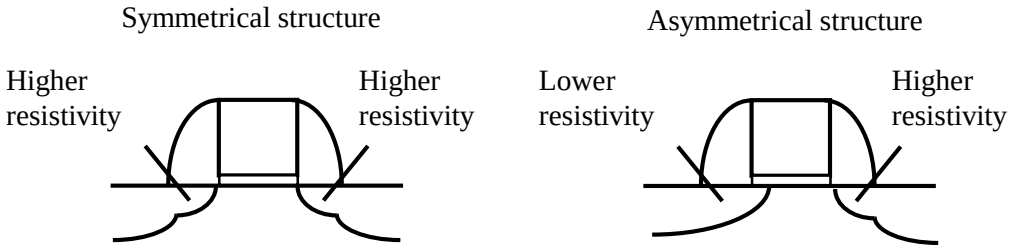
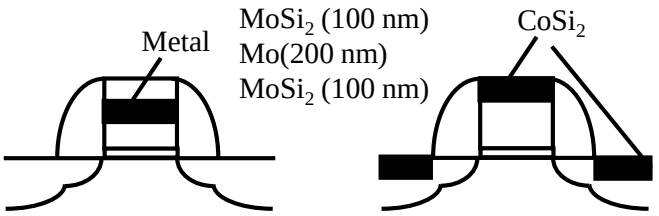


Figure 2-3-1. Comparison of symmetric and asymmetric RF power MOSFET structures.



	Metal	Co-salicide
Gate ρ_s	0.8 ohm/sq. (Lower)	2.1 ohm/sq. (Higher)
Diffusion layer ρ_s	200 ohm/sq. (Higher)	2.5 ohm/sq. (Lower)
Gate length control	Difficult	Easy

Figure 2-3-2. Comparison between metal and Co-salicided poly Si gates.

The upper $MoSi_2$ layer prevents oxidation of the Mo during furnace annealing, while the bottom one improves adhesion with the gate oxide. Efficiency, however, dropped to 30 % at the higher frequency of 2 GHz. This is explained by degraded drivability and transconductance due to over-etching during gate electrode patterning. In the case of compound semiconductor devices such as GaAs and HJFET, higher efficiencies of 63–66 % have already been obtained despite low supply voltages of 1.2 to 1.5 V. A 1.5 V power FET with 65 % power-added efficiency was reported by Tanaka *et al.* in 1995 [39], and a 1.2 V HJFET with 62.8 % power-added efficiency was described by Inosako *et al.* [40]. These excellent characteristics are possible because of the higher transconductance than in Si devices. However, though compound devices have made progress from the point of view of lower supply voltage, it is Si MOSFETs that have found increasing application in power devices because of their lower cost than GaAs, HJFET, and other compound designs. The purpose of this paper is to investigate the possibility of high-efficiency operation of RF power Si MOSFETs at 2 GHz at supply voltages down to 1 V.

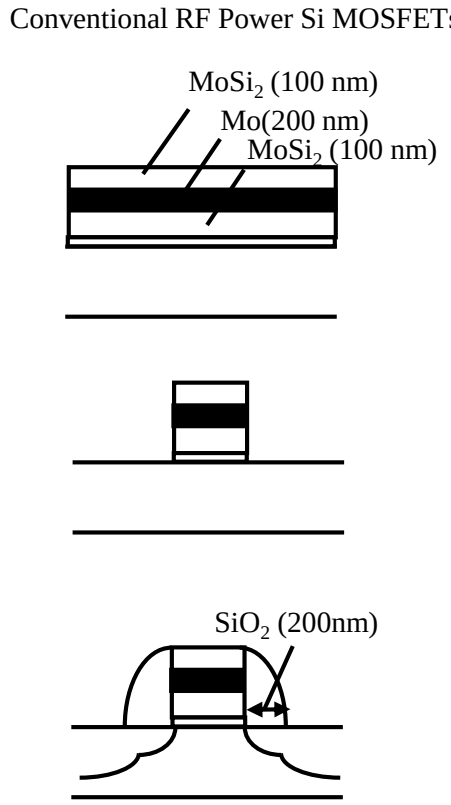


Figure 2-3-3. Sample fabrication for metal gate case.

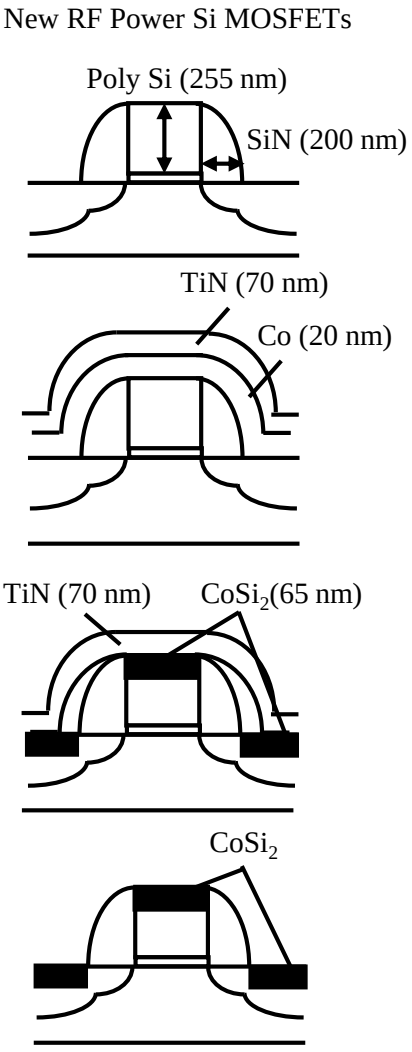


Figure 2-3-4. Sample fabrication for Co-salicided case.

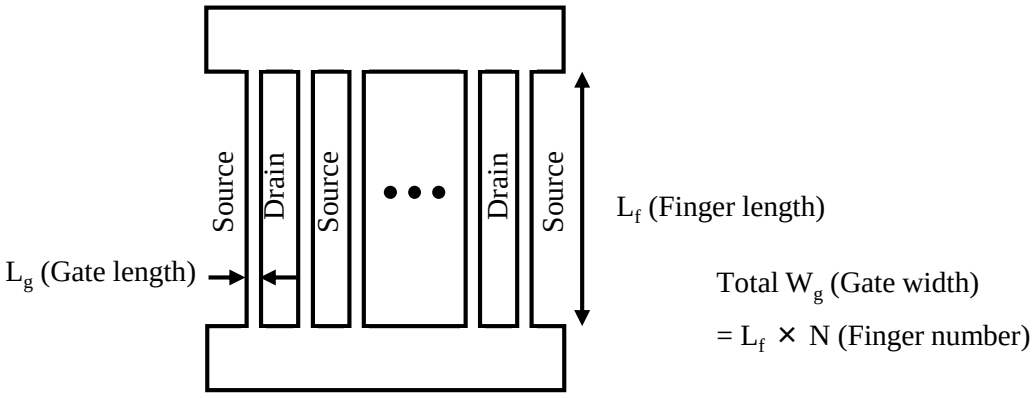


Figure 2-3-5. Top view of Si power MOSFET.

Two different source and drain structures are used for RF CMOS—symmetrical and asymmetrical—as shown in Fig. 2-3-1. With the asymmetrical structure, source resistance is reduced because the junction is deeper and dopant concentration is higher in the source region. As a result, higher RF performance can be expected. On the other hand, the symmetrical structure requires fewer process steps and compatibility with logic LSI processes is easily achieved. In this investigation, we choose to work with the symmetrical structure. Figure 2-3-1 shows the structures of both our conventional RF power Si-MOSFETs [36] and the new structure which forms the basis of the experiments described in this section. Our conventional structure makes use of a metal gate in order to reduce the gate electrode resistance. On the other hand, the new RF power Si MOSFETs use a Co salicide gate so as to reduce not only gate electrode resistance but also the resistance of diffusion layers such as the source and drain. With this structure, it is possible to combine power devices with logic circuits and RF devices because this Co-salicided structure is exactly the same as that in logic CMOS devices with gate lengths below 0.25 μm. Figures 2-3-3 and 2-3-4 illustrate the fabrication process for both the conventional and new RF power Si MOSFETs, respectively.

Conventional RF Power Si MOSFETs : After isolation formation, a thin sacrificial oxide was grown on the Si substrate. Ion-implantation channel doping was then carried out for n- and p-MOSFETs. The conditions were BF_2 at 30 KeV, 1.0×10^{13} cm^{-2} for NMOS and phosphorus 120 KeV, 5.0×10^{13} cm^{-2} , As 70 KeV, 4.0×10^{13} cm^{-2} . After removing the sacrificial oxide, the gate oxide was grown in a dry O atmosphere at 750 °C for 40 min. The gate oxide ranged in thickness from 5.0 to 25 nm. Metal layers consisting of $MoSi_2$ (100 nm)/Mo (200 nm)/$MoSi_2$ (100 nm) were laid down as the gate electrode, as shown in Fig. 2-3-3. After gate patterning with an excimer stepper, the resist width was thinned from 0.4 to 0.2 μm by an ashing technique [41], [42]. The minimum size of the gate electrode was 0.3 μm, as confirmed by SEM observations. With metal gate electrodes of this type, it is difficult to realize an below 0.3 μm because RIE of the three layers—$MoSi_2$ –Mo–$MoSi_2$ —which are highly selective to the gate oxide film results in significant taper. After forming the gate electrodes, As implantation (1.0×10^{13} - 2.0×10^{14} cm^{-2}) was carried out for n-formation; this determined the breakdown voltage between source and drain. After 200 nm SiO_2 gate side walls were formed, As implantation (5.0×10^{15} cm^{-2}) was carried out for n formation. Activation of the source and drain impurities was by rapid thermal annealing at 1000 °C for 20 seconds.

New RF Power Si MOSFETs : Up to deposition of the gate electrode material, the process is the same as for the conventional structure. Thereafter, in the new RF power structure case, *in-situ* phosphorus-doped n polysilicon gate electrodes were formed for the n-MOSFETs. The minimum gate electrode size was 0.2 μm, as confirmed by SEM observations. Such phosphorus-doped n poly silicon gates can be patterned for much shorter gate lengths than in the case of the metal gates because there are well-established techniques for the RIE of single film poly-Si gates with high selectivity to the oxide, and etching is very linear. After forming the gate electrodes, As implantation for n formation was done. After 200 nm SiN gate side-wall formation, As implantation (5.0×10^{15} cm^{-2}) was carried out for n fabrication. Next, rapid thermal annealing was carried out at 1000 °C for 20 seconds in order to activate the source and drain impurities. In these devices, $CoSi_2$ layers were formed on the source, drain, and gate regions by the Co salicide technique [43]–[45] shown in Fig. 2-3-4. After MOSFET formation, Co and TiN films were deposited by sputtering. $CoSi_2$ films were formed on the source, drain, and gate electrodes selectively by annealing at 500 °C for 60 seconds. The new RF power Si MOSFETs can be incorporated into LSI circuits because the structure is the same as used for logic devices with a 0.25 μm gate length. Figure 2-3-5 shows a top view of the new RF power Si-MOSFET. Gate electrodes consist of several fingers; typical finger length (L_f) and total gate width (W_g) in the experiment was 100 μm and 800 μm, respectively. In our experiments, values were from 25 to 200 μm and most cases evaluated were 800 μm.

2-3-2. Comparison between conventional and new RF power Si MOSFETs

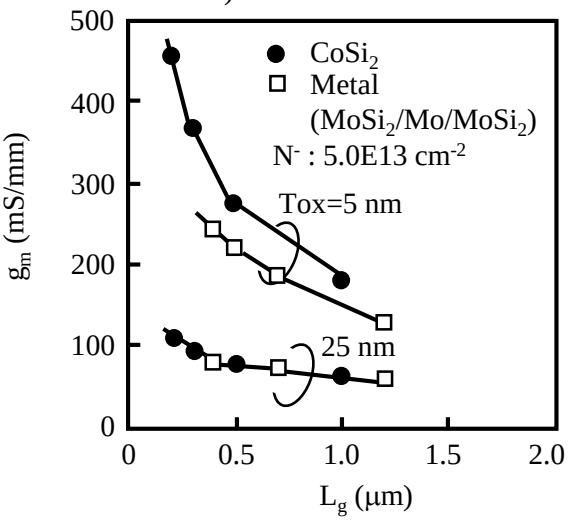


Figure 2-3-6. Dependence of gm on L_g for various tox in metal gate and Co-silicide cases.

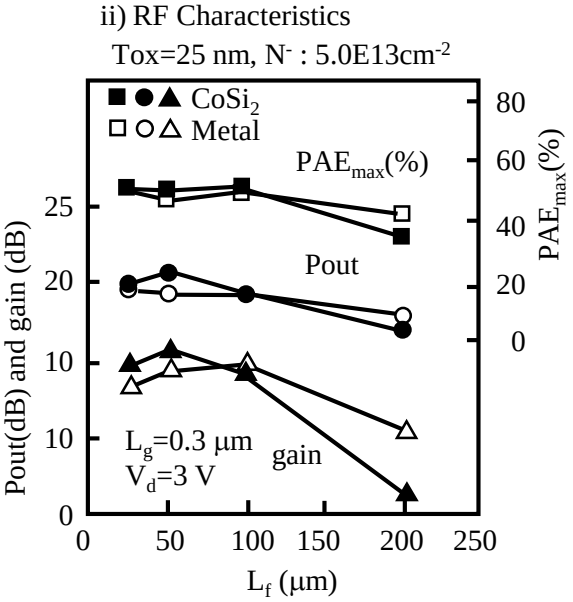


Figure 2-3-7. Dependence of output characteristics such as gain, output power, and power-added efficiency on L_f for metal gate and Co-sallicide cases.

Figures 2-3-6 and 2-3-7 show a comparison between the conventional structure, with metal gate electrodes, and the proposed new Co-salicide structure. The sheet resistance of the metal gate is lower, at around 0.8 ohm/sq. than that of $CoSi_2$, which is typically 2.1 ohm/sq. However, with regard to the diffusion layers, the resistance of those in Si MOSFETs with the Co-salicide structure is far lower. Further, as previously noted, in fabricating the gate electrode it is poly Si that must be etched in the new structure, while in the conventional structure metal is etched. In this cases. it easier to control the gate length correctly with the new structure. Figure 2-3-6 shows the dependence of transconductance on gate length for various gate oxide thickness. When the gate oxide is 25 nm thick, the difference in transconductance between the conventional and new structures is small. However, at 5 nm, the difference is considerable. Further, as the gate length falls, this difference in transconductance becomes more pronounced. This is because, as the gate oxide thickness decreases and the gate length is reduced, the channel resistance falls until the diffusion layer resistance become the major terms. The difference in total resistance between the conventional structure with high-resistance diffusion layers and the new structure with lower resistance widens as the gate oxide thickness and gate length are decreased.

This indicates that the new structure has advantages over the conventional structure because the transconductance of intrinsic MOSFETs improves when the gate oxide thickness is reduced or the gate length is decreased. In order to achieve high power-added efficiency (PAE) when operating at low supply voltages (V_d), it is important to design the MOSFET's such that they have high transconductance (gm). To obtain the high gm values required, we reduced the gate length from 0.3 to 0.2 μm and adopted the Co-salicide structure in place of the conventional metal gate structure, as already explained. The salicide structure reduces the source resistance and improves gm values significantly in the region of short gate length and thin gate oxide—where the intrinsic MOSFET gm value is high—as shown in Fig. 2-3-7. However, with this silicide design, the higher gate electrode resistance than in the metal gate case is a major concern. Figure 2-3-7 shows the dependence of power-added efficiency (PAE) on finger length (L_f). Because gate resistance can be reduced as the decreases, PAE improves with reducing . Providing the of the MOSFET is kept below 100 μm, there is no difference in power-added efficiency between the Co-salicided and metal gate structures. Thus, in for our work, a typical was set at 50 μm.

2-3-3. Low supply voltage design

i) Gate Oxide Thickness

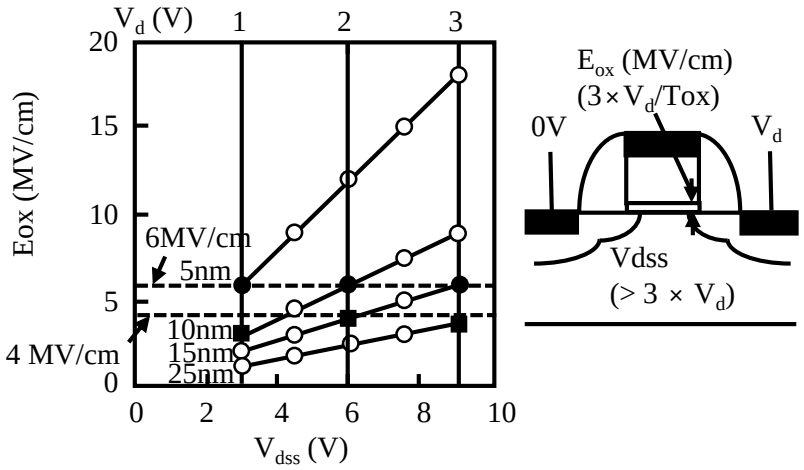


Figure 2-3-8. Dependence of electric field between gate and drain (E_{ox}) on supply voltage. Parameter is gate oxide thickness.

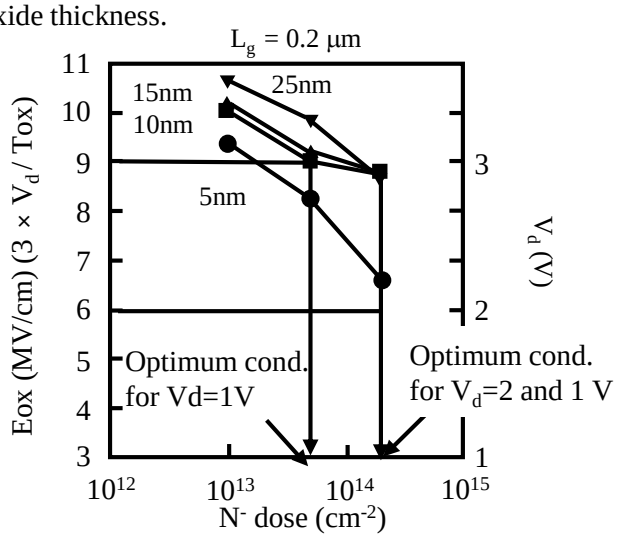


Figure 2-3-9. Dependence of breakdown voltage between source and drain (V) on n dose. Optimum n dose condition is determined by the value of V.

The gate oxide thickness is chosen in accordance with the TDDB reliability of the oxide, and two thickness corresponding to a maximum electric field ($E_{ox\text{-}max}$) of 4 and 6 MV/cm at 3 times were chosen for each in our experiment, as shown in Fig. 2-3-8. Three times value means addition reflection of signal to actual with margin. Power device should be guaranteed even under this large drain voltage case. The breakdown voltage between source and drain needs to be three times the supply voltage because of signal reflection. Thus, when the supply is 3 V, the breakdown voltage is 9 V. In this case, the electrical field between gate and drain through the gate oxide is nine divided by the gate oxide thickness

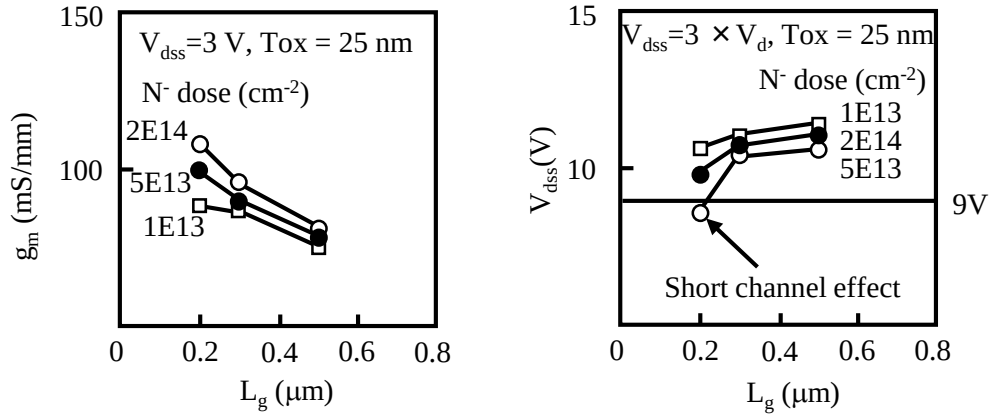


Figure 2-3-10. Dependence of g_m and V_{dss} on L_g for various n-dose. Optimum dosage is determined by requirements of higher g_m and V_{dss}.

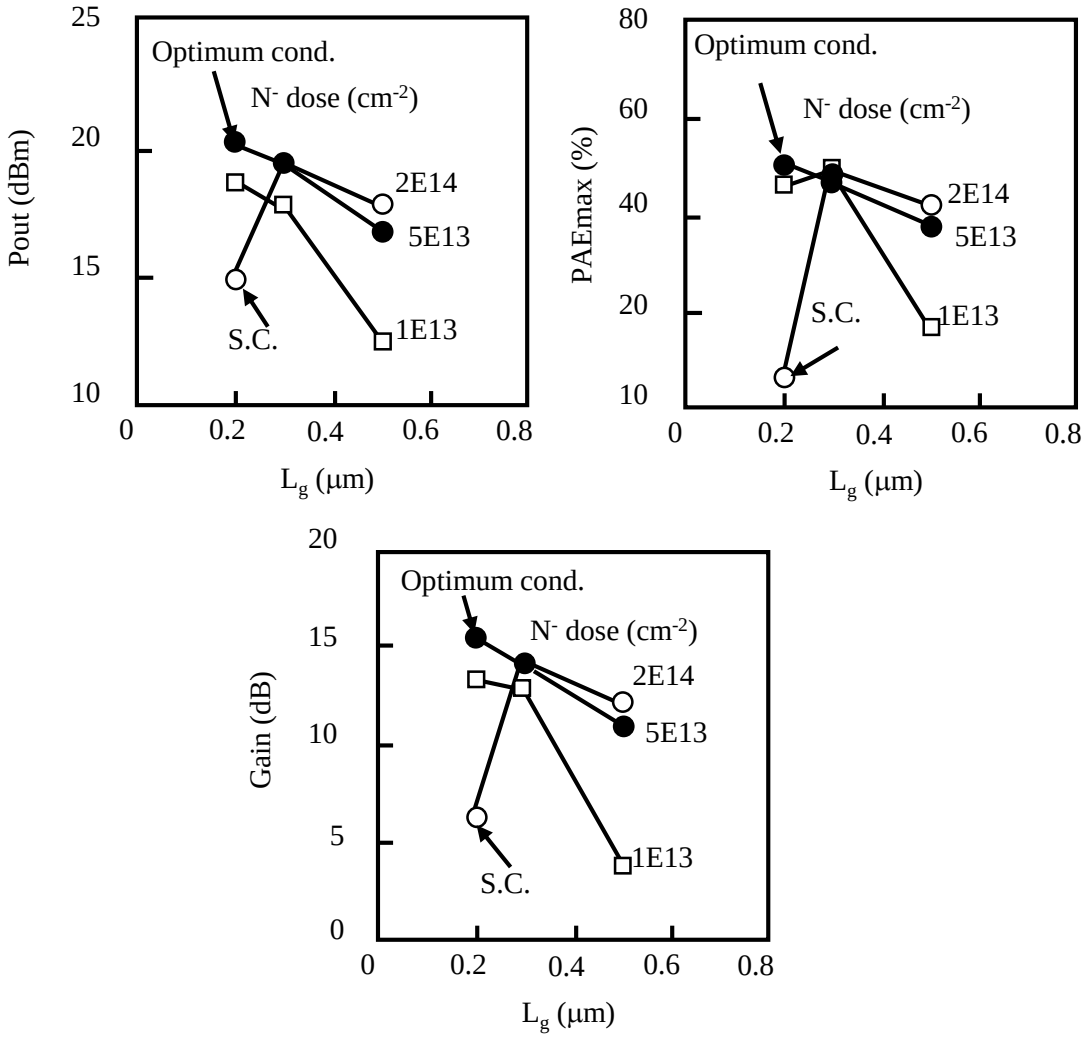


Figure 2-3-11. Dependence of output characteristics such as gain, output power and power-added efficiency on L_g for various n-doses. High performance of power-amplifier characteristics can be realized by using optimum dosage of n-.

Then, if the allowable electrical field value is 6 MV/cm, the gate oxide thickness is automatically fixed at 15 nm. In this way, the gate oxide thickness is determined as 10 and 5 nm, respectively, when the supply voltage is 2 V and 1 V. Figure 2-3-9 shows the experimentally obtained dependence of breakdown voltage on n dosage for various gate oxide thickness in 0.2 μm gate length MOSFETs. The breakdown voltage increases with reducing n^- dosage because parasitic resistance value becomes larger. The optimum n condition is determined from these results for each supply voltage and each gate oxide thickness. For example, when the supply voltage is 3 V, meaning that the breakdown voltage and gate oxide thickness are 9 V and 15 nm, respectively, the optimum n^- dose is 5×13 cm^{-2} based on these data. And when the supply voltage is 2 V, the breakdown voltage and gate oxide thickness are 6 V and 10 nm, respectively, and the optimum n dose is 2×14 cm^{-2} . In the same way, at 1 V, the optimum n^- dose is 2×14 cm^{-2} .

Figure 2-3-10 shows an example of n^- optimization for the case of V_d = 3 V. At the higher n^- dose of 2×14 cm^{-2} , the transconductance value increases significantly as shown in Fig. 2-3-10(a). However, the breakdown voltage is less than 9 V at 0.2 μm gate length as shown in Fig. 2-3-10(b) because of short channel effect. Thus, the middle dose of 5×13 cm^{-2} is the optimum. This is also clear from the performance of the power MOSFET at 2 GHz, as shown in Fig. 2-3-11. This series of figures show the dependence of output power, power-added efficiency, and gain on gate length. In the case of an -dose of 2×14 cm^{-2}, though the transconductance value is the highest of all cases, the output characteristics are worst due to the smaller.

Experimental results at low voltage

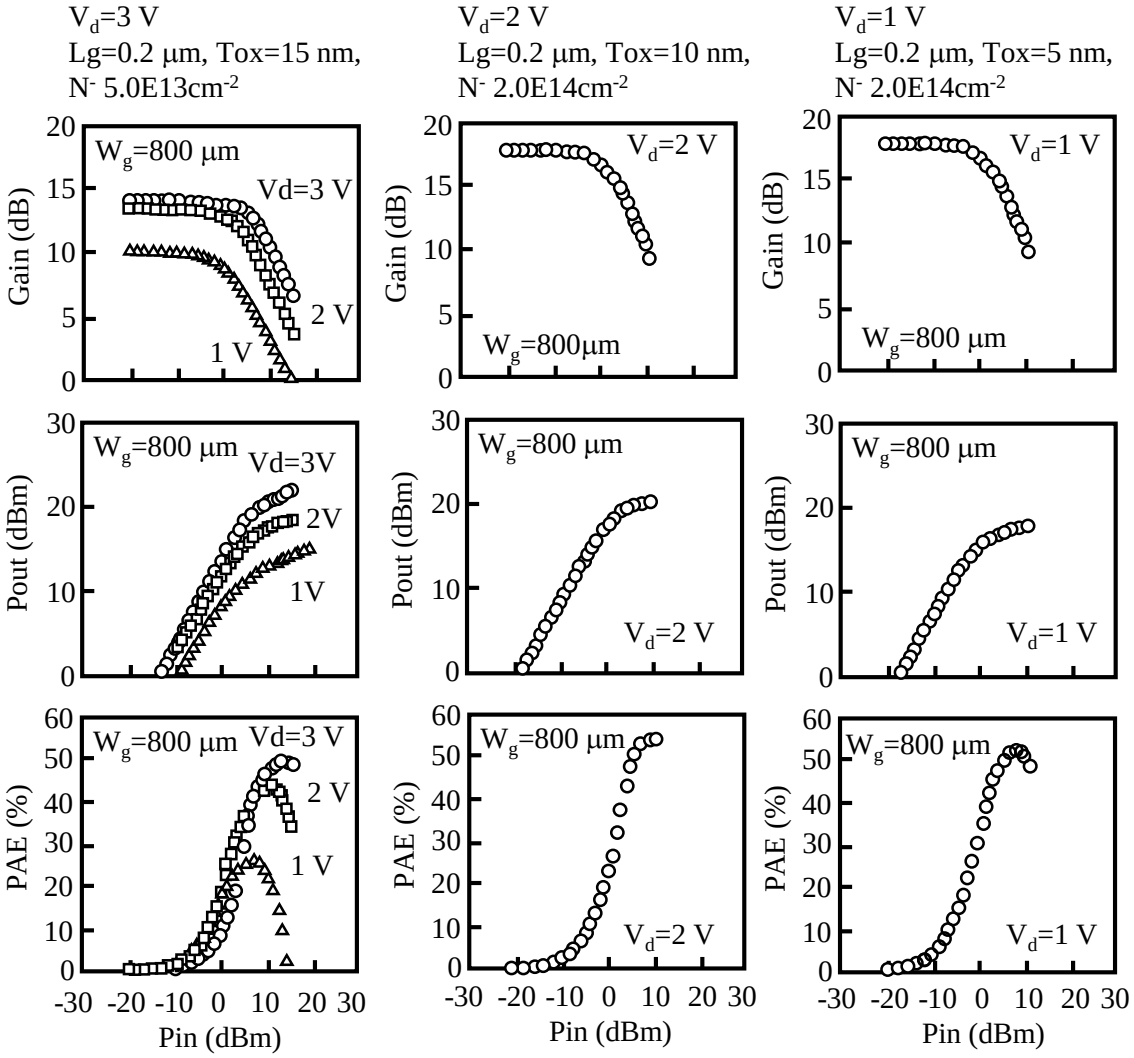


Figure 2-3-12. Input–output characteristics such as gain, output power and power-added efficiency for various supply voltages.

Table 2-3-2 Summary of RF characteristics for 1–3V power supply cases

L_g=0.2 μm, L_f=50 μm, W_g = 800 μm, Co salicide

V_d	Eox_max	Tox	N^-	V_{dss}	$g_{m_}$max
V	MV/cm	nm	cm^{-2}	V	mS/mm
3	4	25	5E13	9.8	89
	6	15	5E13	10.6	127
2	4	15	2E14	9.0	178
	6	10	2E14	9.0	236
1	4	10	2E14	9.0	220
	6	5	2E14	6.6	460

V_d	f_T	f_{MAX}	Gain	Pout (Pin=10 dBm)	PAE_{max}
V	GHz	GHz	dB	dBm(mW)	%
3	25	19	13.9	21.4(110)	50
	25.5	19	16.0	21.4(110)	50
2	35.6	22	14.3	19.8(95)	49
	41.7	20	17.7	20.2(105)	54
1	19	15	15.1	15.6(36)	40
	40	16	16.6	17.5(56)	53

Figure 2-3-12(a) shows the dependence of PAE, Pout, and gain at 2 GHz on Pin for a 0.2 μm gate length Co-salicide MOSFET (in the MV/cm case) with a 3 V power supply. PAE is 50 % at 2 GHz. At the lower supply voltages of 1 V and 2 V, the performance of this MOSFET is significantly degraded and PAE falls to 44 % and 36 % for V and 1 V, respectively, as shown in Fig. 2-3-12(b). Thus, according to the low-voltage design method described above, tox is reduced and n^- is optimized for each V_d. The results are shown in Fig. 2-3-12(b) and (c), for V and 1 V, respectively. A PAE of more than 50 % is confirmed at 2 GHz even at such low voltages. Table 2-3-2 summarizes all cases of low-voltage design. By choosing the optimum condition, a high PAE of around 50 % can be obtained in all cases with a sufficiently high breakdown voltage, . In particular, if we choose 6 MV/cm as , a high PAE of 53 % is realized even at V. Finally, it should be noted that hot carrier reliability would be a concern with 0.2 μm MOSFETs operating at 3 V. However, since hot carrier generation falls significantly with supply voltage, in operation at 1.0 V and 2.0 V hot carrier reliability is not a problem—as already guaranteed by logic CMOS devices. Thus, there are many advantages in decreasing gate length in order to realize higher gain, output power, and power efficiency at a lower supply voltage.

Conclusion

I have described a design methodology for RF power Si-MOSFETs for low-voltage, high-power-added efficiency operation. It has been demonstrated that 0.2 μm gate length Co-salicided Si MOSFET's can achieve a power-added efficiency of more than 50 % in operation at 2 GHz with sufficient breakdown voltage (V_{dss}) if the optimum gate oxide thickness and n^- extension impurity concentration are chosen. In particular, an efficiency of more than 50% was confirmed for the very low supply voltage of 1.0 V, as well as at higher voltages. Short gate length Co-salicided Si-MOSFETs are promising candidates for low-voltage, high-efficiency RF power circuits at 2 GHz. These results demonstrate that such Co-salicided Si MOSFET are effective in operation at RF under very low supply voltages [46].

2-4. Combination with Epitaxial technology for higher performance of mixed-signal and RF circuits

I introduced epitaxial technology to gate poly Si in order to reduce gate resistance. This technique brings T-shaped gate electrode. By combination this technique and Co silicide, the gate resistance decreases. The purpose of this combination is obtaining higher higher gain and f_{MAX}. Additionally, I tried to obtain higher mobility, drivability, V_{th} matching and lower 1/*f* noise when the non doped epitaxial layer was introduced to channel of MOSFET because low channel concentration and higher quality at interface between epitaxial Si layer and gate insulator.

Table 2-4-1. Epitaxial growth temperature and rate at atmospheric pressure for various source gases.

Gas	Boiling Point of the GAS	Growth Temp.	Growth Rate.
$SiCl_4$	57.1 °C	1150 - 1250 °C	0.7 - 1.5 nm/min.
$SiHCl_3$	31.7 °C	1100 - 1200 °C	0.7 - 2.0 nm/min.
SiH_2Cl_2	8.2 °C	1050 - 1150 °C	0.7 - 3.0 nm/min.
SiH_4	-11.2 °C	950 - 1050 °C	0.2 - 0.3 nm/min.

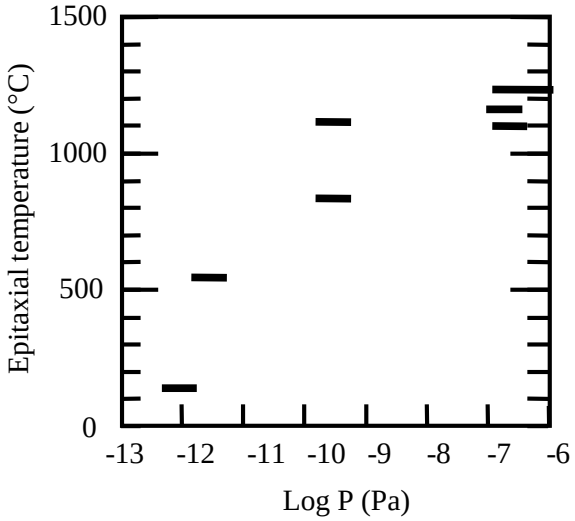


Figure 2-4-1. Dependence of epitaxial growth temperature on pressure in MBE case.

2-4-1. Epitaxial technology

In order to apply epitaxial technology to RF CMOS, there are three major requirements. First, low growth temperature is necessary to suppress the impurity redistribution and thus, to realize ultra-shallow source and drain. Secondly, good epitaxial Si quality is required in order to obtain low junction leakage current, low N_{it} and higher mobility. Thirdly, selective growth of the epitaxial layer is necessary to realize epitaxial channel and raised gate/source/drain structures. These structures will be described in detail. Table 2-4-1 shows the epitaxial growth temperature and rate at atmospheric pressure for various source gases [47]. The growth temperature depends on the gases. In the case of $SiCl_4$, the temperature is the highest. As Cl of SiH_xCl_y is replaced by H one by one, the growth temperature decreases by 50 °C. The temperature is 950 °C in the SiH_4 case. However, this temperature is not sufficiently low formation for deep sub-micron CMOS in which desirable maximum heat process is around 800 °C for 30 seconds after source and drain. In order to reduce the epitaxial growth temperature, lower pressure during the growth is useful. Figure 2-4-1 shows dependence of epitaxial growth temperature on pressure in molecular beam epitaxy (MBE) case [48-54]. The temperature decreases as the pressure decreases. In the case of 10^{-12} Pa, the temperature is below 300 °C.

Table 2-4-2. Selectivity of epitaxial Si growth for insulator such as SiO2 and Si_3N_4.

Insulator	Mixed gas	Growth Temp.	Mechanism	Selectivity
SiO_2	HCl	Higher	Reaction with O	Better
Si_3N_4	HCl	Lower	No reaction	Worse

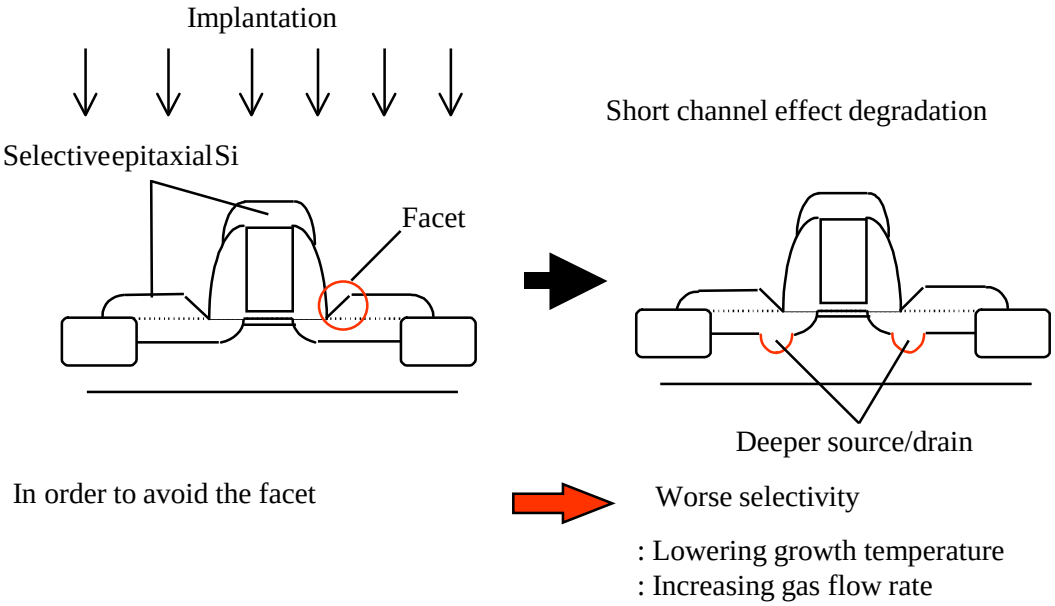


Figure 2-4-2. The problem of facet for CMOS.

Table 2-4-3. No facet condition in formation of raised gate / source / drain structure.

Source gas	Mixed gas	Growth rate	Pressure	Temp.	Final thickness
SiH_2Cl_2 (0.4 l/min.)	HCl (0.1 l/min.)	50 nm/min.	0.1 Pa	850 °C	50 nm

Selectivity of epitaxial growth can be controlled by mixing HCl into source gas and by controlling the growth temperature [55]. As the HCl gas flow rate increases, the selectivity becomes higher. However, growth rate becomes slower. As the growth temperature increases, the selectivity becomes higher for SiO_2 layer. Si in the source gas reacts with O in the SiO_2 and forms SiO gas at higher temperature which flows away from the SiO_2 layer. On the other hand, the selectivity becomes lower for Si_3N_4 layer in high temperature case. At high temperature, reacted Si at Si_3N_4 layer remains and will not evaporate. At low temperature, reaction of Si with the Si_3N_4 layer is suppressed. Thus selectivity becomes higher at low temperature for Si_3N_4 case. In general, the selectivity for SiO_2 layer is better than that for Si_3N_4 layer.

Table 2-4-4. cleaning method for Si surface before epitaxial growth.

Method	Merit	demerit
Ar sputtering	Low temperature	Damage
Heating	No damage	High temperature

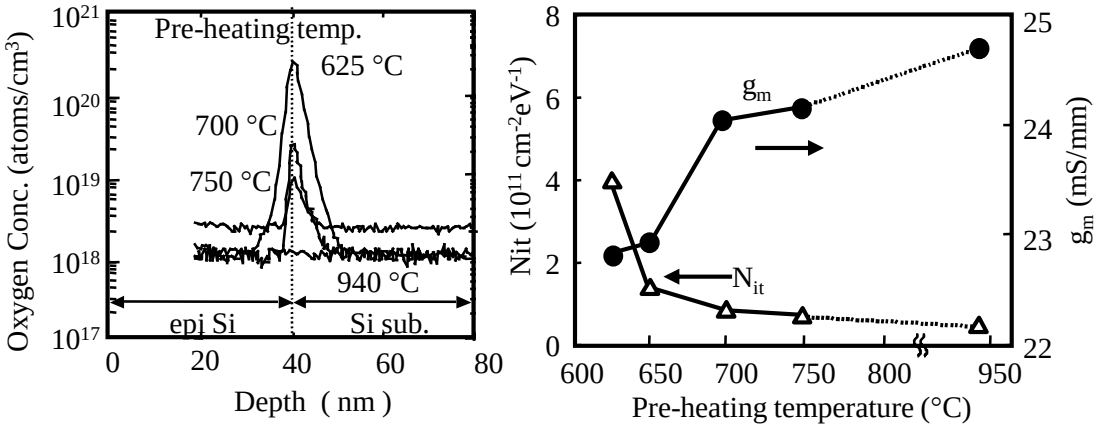


Figure 2-4-3. Oxygen profile after epitaxial growth for various pre-heating temperature and dependence of gm and Nit on the temperature.

Facet is a problem for raised source and drain structure as shown in Fig. 2-4-2. Because junction depth of gate edge becomes deeper, this junction brings short channel effects. The facet of epitaxial Si layer appears in growth condition with high selectivity [56, 57]. In order to avoid the facet, the condition of little worse selectivity is chosen by lowering temperature and increasing the gas flow rate. Table 2-4-3 shows the actual epitaxial growth condition for raised gate/source/drain structure. By using this condition, facet was completely suppressed. Regarding the epitaxial Si quality, it is important to clean the Si surface before epitaxial growth. In general, Ar sputtering and pre-heating are proposed for the pre-treatment before epitaxial growth. Ar sputtering is low temperature treatment, but damage due to this process is a serious problem. On the other hand, pre-heating method is useful to improve the Si epitaxial layer quality [58, 59] as shown in Table 2-4-4.

Figure 2-4-3 shows the oxygen profile after epitaxial Si growth for various pre-heating temperature [58]. As the temperature increases, the oxygen decreases. In the case of 940 °C pre-heating, the oxygen signal is below the resolution limit. Corresponding to the decrease in the oxygen concentration, transconductance and N_{it} of the epitaxial channel MOSFETs are improved the epitaxial channel MOSFETs will described later in this paper. The 940 °C is a little higher for deep sub-micron CMOS devices and it should be reduced.

2-4-2. Actual application to Si device

Table 2-4-5. The some of publication for selective epitaxial application.

Gas	Temp.	Authors	Application	Ref.
SiC_4-H_2	1200°C	B.A. Joyce, et al.		[61]
$SiCl_4$-H_2,$SiHCl_3$-H_2	1200-1240°C	Takabayasi, et al.		
$SiCl_4$-H_2-Hcl (HBr)	1150°C	D. M. Jackson, et al.		
$SiCl_4$-H_2-Hcl	1200°C	E. G. Alexander, et al.		
$SiCl_4$-H_2-Hcl	1200°C	M. Nomura, et al.		
$SiCl_4$-H_2,SiH_4-H_2	-	P. Rai-Choudhury, et al.		[62]
-	-	J. Nishizawa, et al.	(e)	[63]
$2SiI_4$	-	P. D. Braun, et al.		
SiH_2Cl_2-H_2-Hcl	950°C (RP-CVD)	Tanno, et al.	(a)	[64]
-	-	S. S. Wong, et al.	(g)	[65]
SiH_2Cl_2-H_2-Hcl	900°C (RP-CVD:0.4Pa)	H. Shibata, et al.	(c)	[66]
SiH_2Cl_2-HCl	900°C (RP-CVD:0.7Pa)	H. Shibata, et al.	(g)	[67]
SiH_2Cl_4	900°C (RP-CVD)	J. N. Burghartz, et al.	(b)	
-	560°C (UHV-CVD)	R. Schulze, et al.	(b)	[68]
Si_2H_6	-	M.Aoki, et al.	(d)	[69]
Si_2H_6	625°C (UHV-CVD)	T. Ohguro, et al.	(f)	[70]
SiH_2Cl_2	800°C (RP-CVD:0.1Pa)	T. Ohguro, et al.	(f)	[71]
SiH_2Cl_2-HCl	850°C (RP-CVD)	C. -P. Chao, et al.	(h)	[72]

Table 2-4-5 shows the some publications for selective epitaxial Si applications, and Figure 2-4-3 shows example of the device structures using selective epitaxial Si growth. The temperature of the selective epitaxial growth has reduced from 1200 °C to 800 °C in 35 years by changing gases from SiCl4 to SiH_2Cl_2 and reducing pressure from atmospheric pressure(AP) to reduced pressure such as 0.1 Pa (RP) . In the UHV CVD case, the temperature is reduced to 560 °C – 625 °C by using Si_2H_6 gas. In 1962, selective epitaxial Si growth was made on Si substrate for the first time by B. A. Joyce et al as shown in Fig 2-4-4(a).

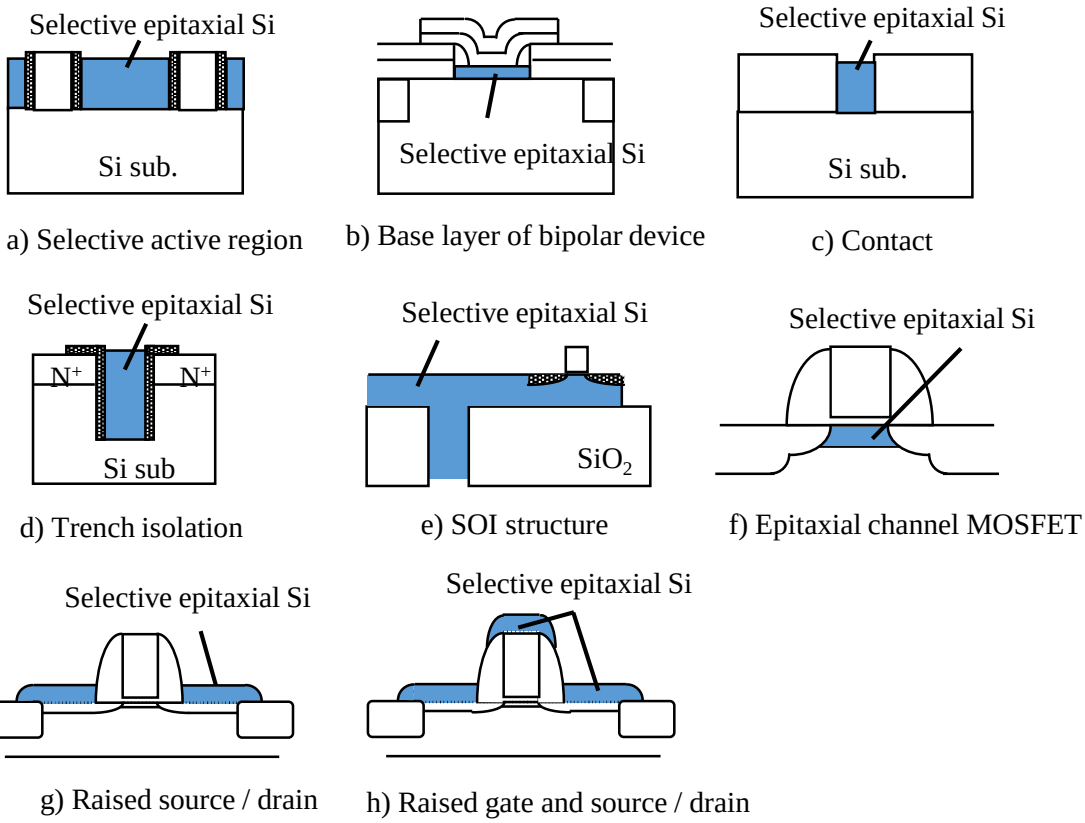


Figure 2-4-4. Example of the device structures using selective epitaxial growth.

From the middle of 1980s, when the growth temperature reduced to 900 °C, the selective epitaxial technology has applied to many kinds of devices. They are for example, a) selective active region b) selective base layer of bipolar transistors. c) selective Si filled contact hole d) selective Si filled trench isolation e) substrate - contacted silicon layer for SOI e) epitaxial channel for MOSFET e) elevated or raised source and drain for MOSFET f) elevated or raised gate/source/drain for MOSFET as shown in Fig. 2-4-4.

In the following section, two structures of these examples of epitaxial channel MOSFETs and raised gate source drain are described.

2-4-3. Epitaxial channel MOSFET

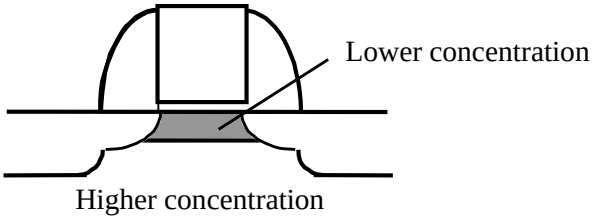


Figure 2-4-5. Cross sectional view of epitaxial channel MOSFET.

Low threshold voltage (V_{th}) is important for operation under low supply voltage in order to obtain high drivability, high transconductane and f_T value. Low threshold voltage can be realized by reducing the dopant concentration in the channel region. In order to suppress the short channel effect with low threshold voltage, very steep retrograde impurity profile with ultra-shallow layer with low dopant concentration and deeper layer with high dopant concentration as shown in Fig. 2-4-5. Very steep retrograde profiles are usually difficult to be realize, but easily made by selective epitaxial Si channel technique in which an ultra-thin un-doped Si layer is formed on the highly doped Si substrate as shown in Fig. 2-4-7.

Table 2-4-6. Publication of Si epitaxial channel MOSFET.

No.	Method	Temp.(°C)	Thick.(nm)	dope	Selective	L_g (nm)	Tox (nm)
1	Sim.	-	10	No	-	50-25	3.0-1.5
2	UHV-CVD	600	7.5-12.5	Boron	Yes	150	3.0
3	UHV-CVD	650	20-80	No	Yes	100	-
4	Sim.	-	10-50	No	-	50	-
5	UHV-CVD	625	10-50	No	Yes	100	3.0
6	UHV-CVD	650	10-50	Boron	Yes	150	-
7	UHV-CVD	-	10-40	No	Yes	160	5.8
8	RP-CVD	800	30	No	Yes	180	3.0
9	RP-CVD	800	30	No	Yes	110	2.5

No.	Type	g_m (mS/mm)	I_{d0} (mA/um)	V_d (V)	Ref.
1	CMOS	-	-	1.2	[72-74]
2	PMOS	300	0.13	1.5	[75]
3	CMOS	492	0.9	2.5	[76]
4	CMOS	-	-	0.5	[77]
5	PMOS	630	0.77	1.5	[78]
6	CMOS	-	0.55(N)/0.29(P)	2.5	[79]
7	PMOS	300	0.33	0.5	[80]
8	NMOS	680	-	1.2	[81]
9	NMOS	670	0.60	1.2	[82]

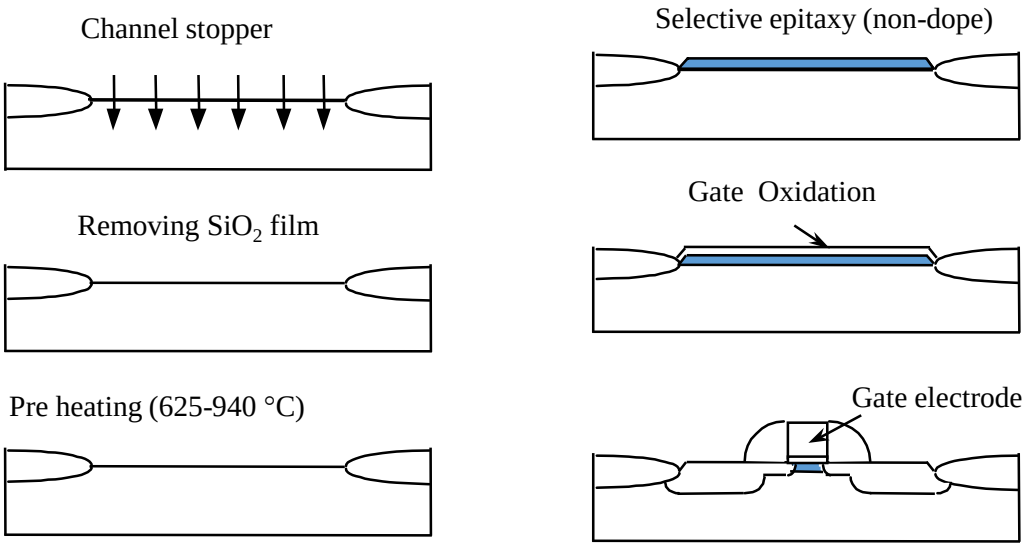


Figure 2-4-6. The process flow of epitaxial channel MOSFET.

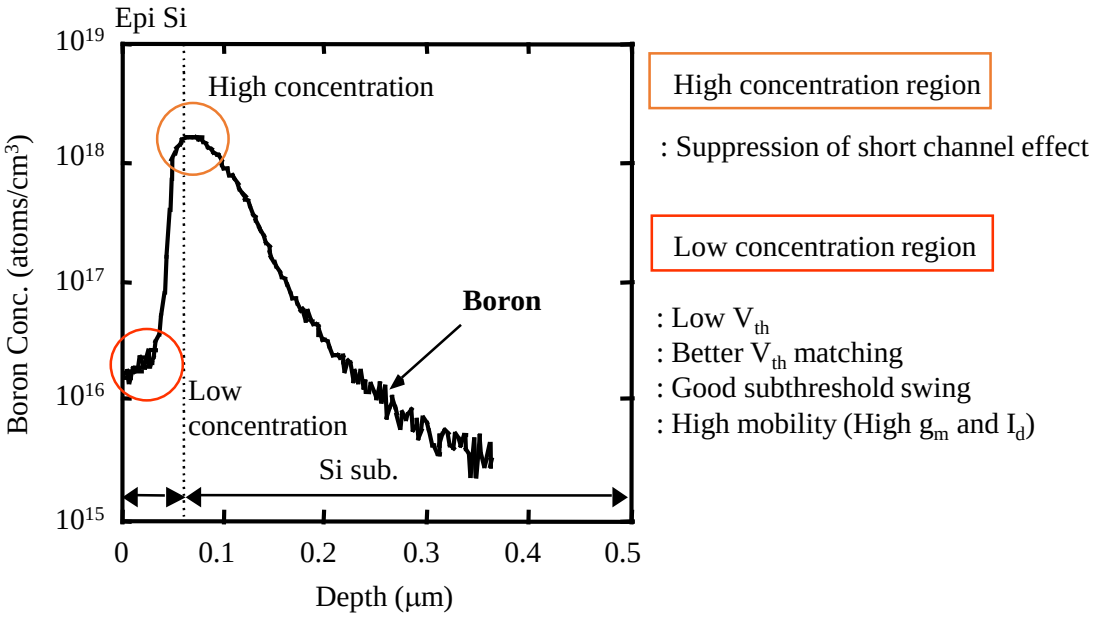


Figure 2-4-7. Boron profile in the epitaxial channel region after thermal process.

Publications of Si epitaxial channel MOSFETs are listed in table 2-4-6. In May 1993, C. Fiegna et al. demonstrated the importance of the ultra-thin un-doped epitaxial layer for sub 0.1 μm gate length MOSFETs and found that the epitaxial layer thickness is desirable to be around 10 nm in order to suppress the short channel effects for deep – sub 0.1 μm MOSFET. In order to realize the such an ultra-thin un-doped epitaxial layer, suppression of the impurity redistribution in the epitaxial layers the most important. Thus, they predicted the necessity of low temperature selective epitaxial growth on the channel region after the formation of isolation region. Similar simulated results for un-doped epitaxial channel MOSFETs were presented later in December 1994, by T. Andoh et al. In 1993, 1995 - 1998, the experimental results of MOSFETs with ultra-thin epitaxial channel layer which was selectively grown at low temperature were presented by T. Ohguro et al. The aim to use this structure is realization of low V_{th} with suppressing short channel effects in deep sub-micron device.

Figure 2-4-6 shows the process flow of epitaxial channel MOSFET. After isolation, ion implantation through thin sacrifice oxide was carried out in order to suppress short channel effects and to control V_{th}. Then the SiO_2 film was removed by wet treatment and pre heating to clean the surface of Si sub was done. The pre-heating condition was temperature of 940 °C and atmosphere of hydrogen. After cleaning process, non-doped epitaxial Si was grown only on active region. Gate oxide was formed by dry O_2 in 800 °C for 8 minutes. Then, gate electrode and source/drain were formed. Finally, Co salicide technique was applied to this device.

Figure 2-4-7 shows the boron profile in the epitaxial channel region after the heat treatments of gate oxidation (800 °C for 30 minutes) and RTA for source and drain (1000 °C for 10 second). The epitaxial Si thickness was 70 nm. Note the abrupt change of the boron concentration at the interface of the epitaxial layer and Si substrate. . The surface concentration was about 1×10^{16} cm^{-3}, though that of the substrate was about 1×10^{18} cm^{-3}. Higher concentration region suppresses the short channel effect. Low concentration of surface of channel brings low V_{th}, good subthreshold swing and high mobility.

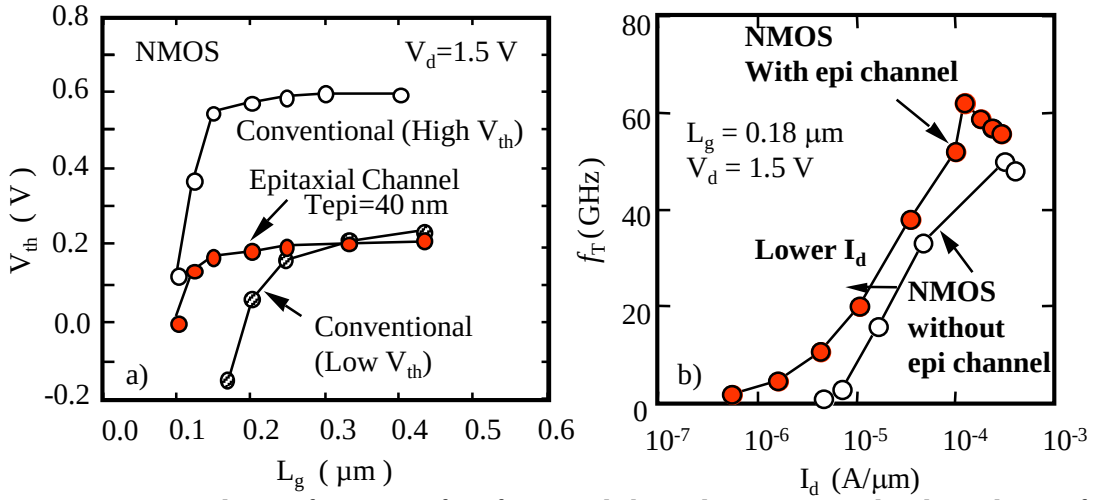


Figure 2-4-8. Dependence of V_{th} on L_g for of epitaxial channel MOSFET and I_d dependence of f_T .

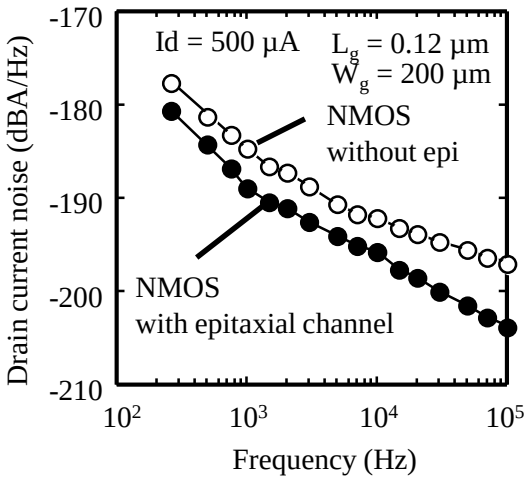


Figure 2-4-9. Dependence of 1/*f* noise on frequency for epitaxial channel MOSFET.

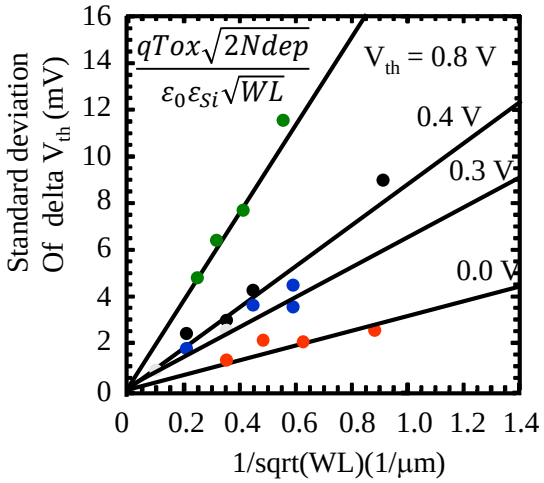


Figure 2-4-10. Dependence of V_{th} matching on V_{th} value.

By using this structure, low V_{th} can be realized with suppressing short channel effect even when L_g is 0.1 μm. On the other hand, ion implantation channel doping case, the profile is very broad. It is difficult to realize 0.1 μm MOSFET with low V_{th} because deeper concentration decreases as the surface that decreases as shown in Fig. 2-4-8(a). Fig. 2-4-8b) shows the dependence of f_T on drain current. The drain current of epitaxial channel MOSFET when the same f_T value is lower than that of normal V_{th} case. This result shows that low power consumption can be realized by using this structure.

Figure 2-4-9 shows dependence of 1/*f* noise on frequency for epitaxial channel MOSFET. The noise is about 5 dB lower than that of conventional structure. I think this is caused by improvement of roughness at interface between gate insulator and epitaxial Si layer. Figure 2-4-10 shows dependence of V_{th} matching on V_{th} value. This mismatch data usually obey Pelgrom's low. According to the low, the mismatch can be reduced by reducing V_{th}. Thanks to low V_{th}, this mismatch can be improved by epitaxial channel.

2-4-4. Raised gate/source/drain MOSFET with $CoSi_2$

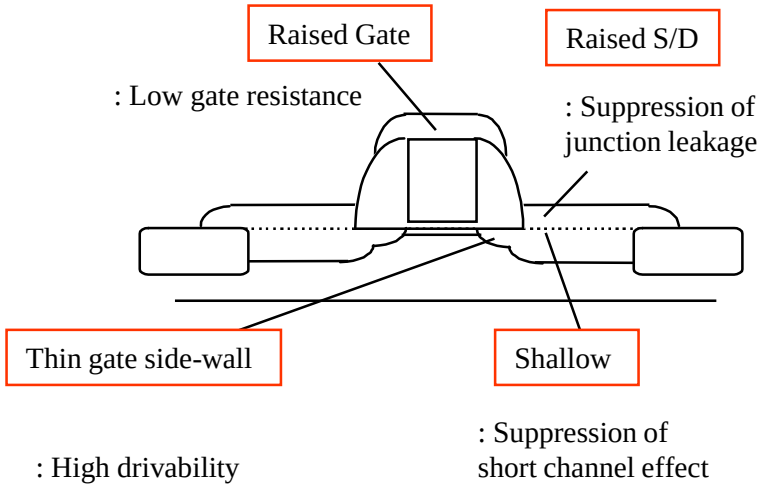


Figure 2-5-15. Cross sectional view of raised gate source and drain structures.

Table 2-5-7. Previous reports for raised (gate)/source/drain structure.

Method	Structure	Gas	Temp.	Ref.
RP-CVD	Raised S/D	-	-	[65]
RP-CVD	Raised S/D	SiH_2Cl_2-HCl	900 °C	[67]
RP-CVD	Raised G/S/D	-	700 °C	[83]
UHV-CVD	Raised G/S/D	Si_2H_6	660 °C	[84]
RP-CVD	Raised G/S/D	SiH_2Cl_2-HCl	850 °C	[71]
RP-CVD	Raised G/S/D	SiH_2Cl_2-HCl	800 °C	[70]
RP-CVD	Raised G/S/D	-	-	[85]

Fig. 2-5-15 shows the cross sectional view of a raised gate, source and drain structure. This structure has the following merits. First, lower drain and source resistances can obtained because the extension distance can be reduced as shown in Fig. 2-5-15. Thus, high drain current, high f_T, f_{MAX} and low $N.F._{min}$ can be realized. Secondly, the gate resistance becomes low, which is important for RF CMOS in terms of $N.F._{min}$ and f_{MAX}. Because the gate electrode is T-shaped like mushroom, the gate resistance is relatively small with narrow gate electrode. Another merit is the suppression of the junction leakage current of shallow drain with salicide process.

Table 2-5-7 shows previous reports for raised source and drain structures. In 1984, an elevated or raised source and drain structure was demonstrated by S. S. Wong et al. Recently, not only the source/drain but also gate electrode is raised by selective Si epitaxial growth as shown in the table.

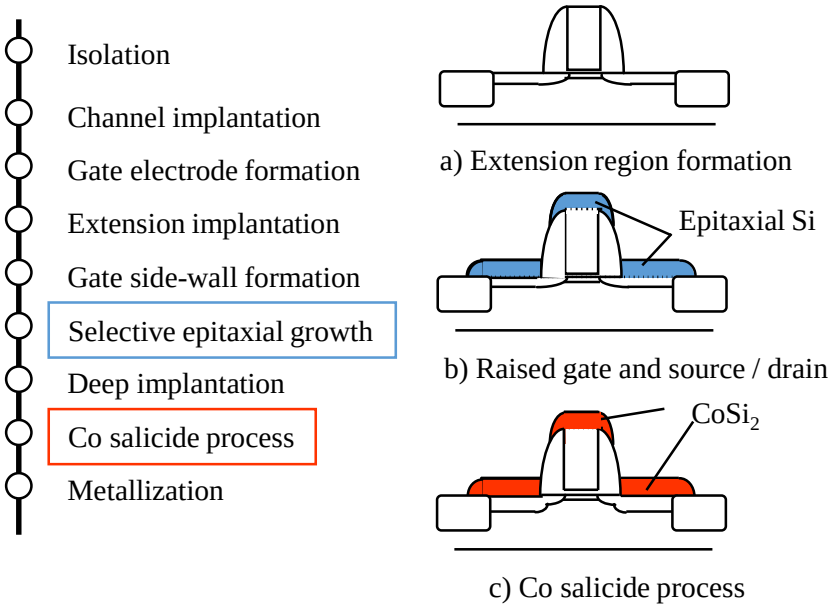
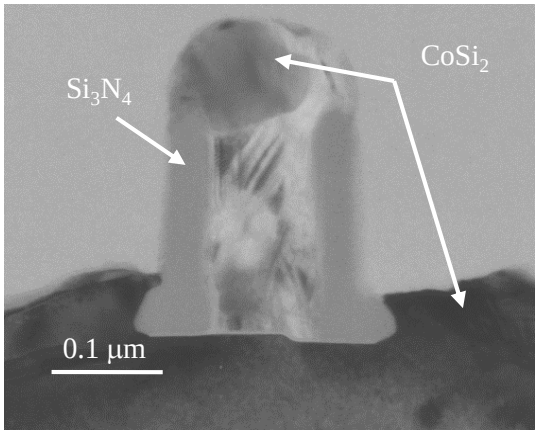


Figure 2-5-16. Process flow of raised gate/source/drain MOSFET.

Fig. 2-5-16 shows the process flow of raised gate/source/drain MOSFET used for RF CMOS. After formation of the gate electrode, extension region source and drain were formed by using ion implantation (Fig. 2-5-16a). Then, 50 nm Si_3N_4 sidewall are formed, and 50 nm undoped epitaxial Si layers were grown selectively on gate/source/drain regions by RP-CVD (Fig. 2-5-16b). Pre-heating before epitaxial growth of 940 °C for 30 seconds in H_2 atmosphere was carried out in order to clean the Si surface and to eliminate the native oxide layers. The gas and temperature during growing the epitaxial Si were SiH_2Cl_2 and 850 °C, respectively. A facet of epitaxial Si at the gate sidewall edge dose not appear in this growing condition. Then, As for NMOS and BF_2 for PMOS were implanted through epitaxial Si layers with the Si_3N_4 sidewall as a mask to form the n^+ and p^+ source/drain regions, respectively. A 950 °C annealing for 30 seconds was carried out to activate the dopant. Co-salicide was used in order to reduce gate/source/drain resistances significantly. 15 nm Co and 70 nm TiN films were deposited by sputter. Then, $CoSi_2$ films were formed on source, drain and gate electrode selectively by 500 °C for 60 seconds annealing. After removing non reactive Co and TiN films by using the mixture of H_2O_2 and H_2SO_4, Co silicide was changed from CoSi to $CoSi_2$ by 750 °C for 30 seconds annealing to reduce its resistivity in this experiments. The gate electrode was T-shaped and the line width at the top of the electrode was 0.16 μm while that of bottom was 0.10 μm., it is known that the thickness of $CoSi_2$ on gate electrode was larger than that on the source/drain.



Source gas	Mixed gas	Growth rate
SiH_2Cl_2 (0.4L/min.)	HCl (0.1L/min.)	50 (nm/min.)

Pressure	Temp.	Final thickness
0.1 Pa	850 °C	50 nm

Figure 2-5-17. Cross sectional view of raised gate/source / drain.

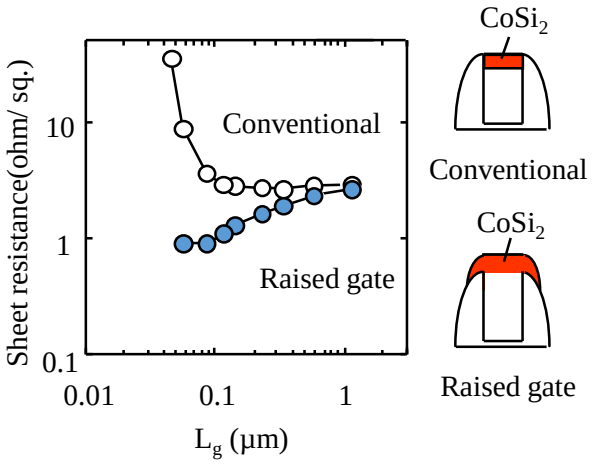


Figure 2-5-18. Dependence of Co salicided gate sheet resistance on L_g for the raised and conventional structures.

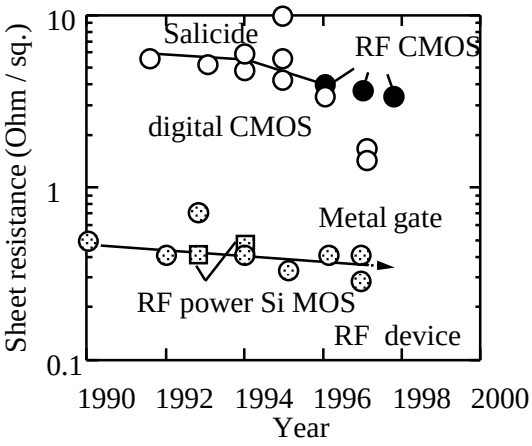


Figure 2-5-19. sheet resistance of gate electrode of digital, RF CMOS and discrete power Si MOSFET.

Figure 2-5-17 shows TEM photograph of raised gate , source, drain. The gate electrode was T-shaped and the line width at the top of the electrode was 0.16 μm while that of bottom was 0.10 μm, it is known that the thickness of $CoSi_2$ on gate electrode was larger than that on the source/drain. . Fig. 2-5-18 shows the dependence of Co salicided gate sheet resistance on L_g for the raised and conventional structures. The gate resistance decrease as the L_g decrease in raised cases and 1 ohm/sq. was realized as L_g = 0.10 μm, while even the significant resistance degradation appeared which is called as narrow line effect, when the gate length was below 0.10 μm in the case of conventional structure. The difference is caused by the top of gate electrode shape in which the line width of the electrode is about 0.1 μm larger than the bottom by the 50 nm epitaxial growth. The thickness of $CoSi_2$ in raised structure was larger than that of conventional structure. The value of gate sheet resistance was around 1 ohm/sq.

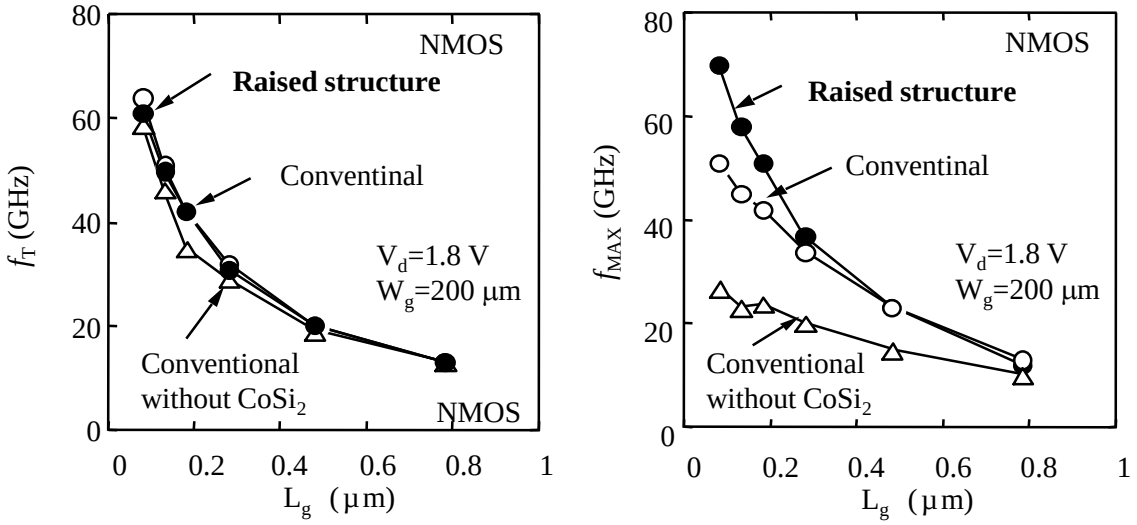
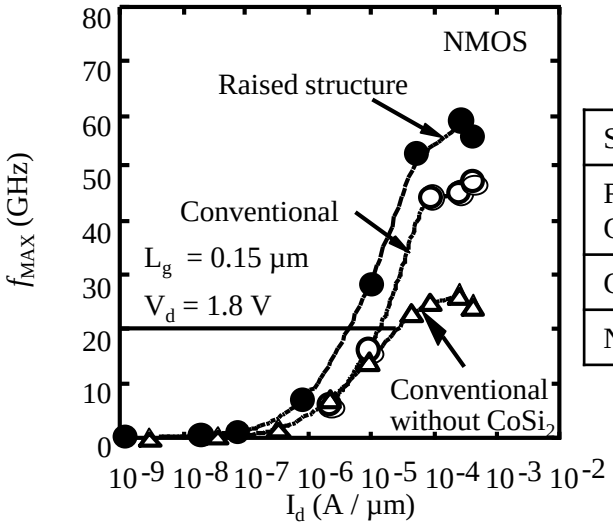


Figure 2-5-20. The dependence of f_T and f_{MAX} on L_g, and dependence of f_{MAX} on drain current.



Structure	I_d@ f_{MAX} =20 GHz
Rased structure + Co salicide	1.2 mA
Co saliicide	3.8 mA
No salicide	6.0 mA

Figure 2-5-21. shows f_{MAX} - I_d curves for the MOSFETs with L_g = 0.15 μm.

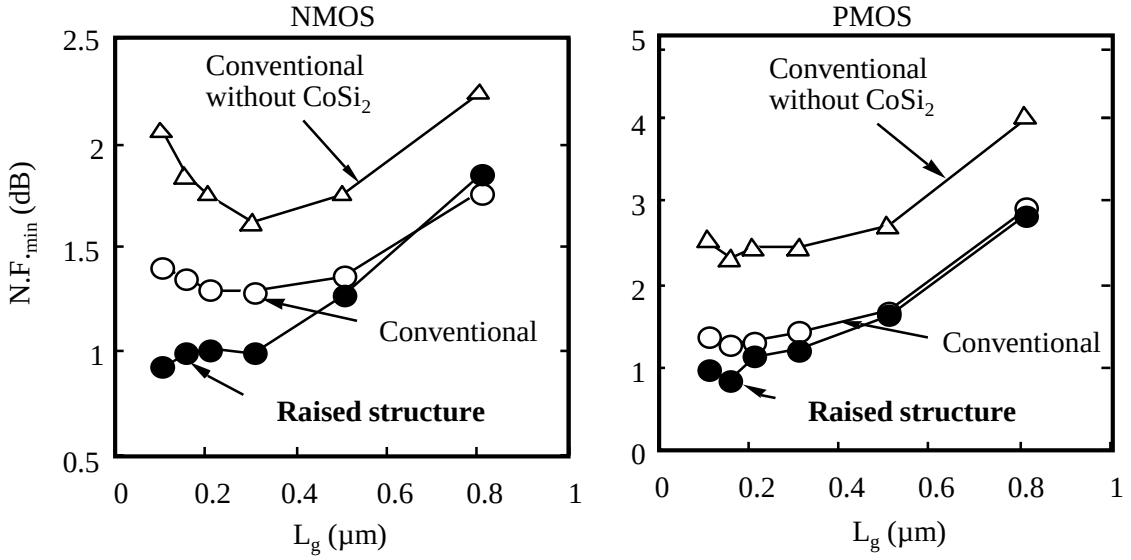


Figure 2-5-22. Gate length dependence of N.F.$_{min}$ for NMOS and PMOS.

Fig. 2-5-19 shows sheet resistance of gate electrode of digital, RF CMOS and discrete power Si MOSFET. In both digital and RF CMOS, the resistance is beyond 5ohm/sq, because the value is sufficient for suppression of parasitic resistance of source, drain and gate, while that of discrete power Si MOSFET is around 1 ohm/sq. because the lower power loss by gate electrode is required. The gate sheet resistance of gate electrode applied epitaxial growth and $CoSi_2$ was comparable with metal gate resistance. Figure 2-5-20 shows the dependence of f_T and f_{MAX} on L_g. The results of nMOSFETs without Co silicide and raised structure are plotted as a reference. F_T was almost the same in all samples because it does depend on not gate resistance but gm. Thus, f_T increase as the L_g decrease in all cases even if the case without Co silicide and raised structure. However there were large difference in f_{MAX} because it is strongly affected by the gate resistance. In case without Co silicide and raised structure, f_{MAX} of only 27 GHz is obtained when L_g is 0.1 μm. In MOSFETs with Co silicide, the difference of f_{MAX} becomes larger when L_g was below 0.3 μm. This is because gate resistance difference also becomes larger as shown in Fig. 2-5-8. Very high f_{MAX} value of 70 GHz was realized by the $CoSi_2$ 0.10 μm gate length n-MOSFET with the raised structure because gate resistance was extremely low as 1 ohm/sq. while the value is 52 GHz in the case without raised structure. This highest fmax value is comparable with that of high performance SiGe HBT devices. Fig. 2-5-21 shows f_{MAX} - I_d curves for the MOSFETs with L_g = 0.15 μm. In the $CoSi_2$ n-MOSFETS with the raised structure, drain current required to achieve the same f_{MAX} value is significantly smaller than other cases. Thus, low power consumption can be realized by using raised structure. Figure 2-5-22 shows the dependence of $N.F._{min}$ on L_g for NMOS and PMOS. It should be noted that de-embedding of the bonding pad effects on $N.F._{min}$ value was not applied in this measurements. Thus, the intrinsic MOSFET noise itself is smaller than the plotted value. $N.F._{min}$ degradation was observed when the L_g was below around 0.2 μm for non-Co-salicided or non-raised n-MOSFETs as well as f_{MAX}, because the increasing of gate resistance becomes remarkable. In the $CoSi_2$ raised structure case, however, no $N.F._{min}$ degradation was observed due to low gate resistance in both MOSFETs.

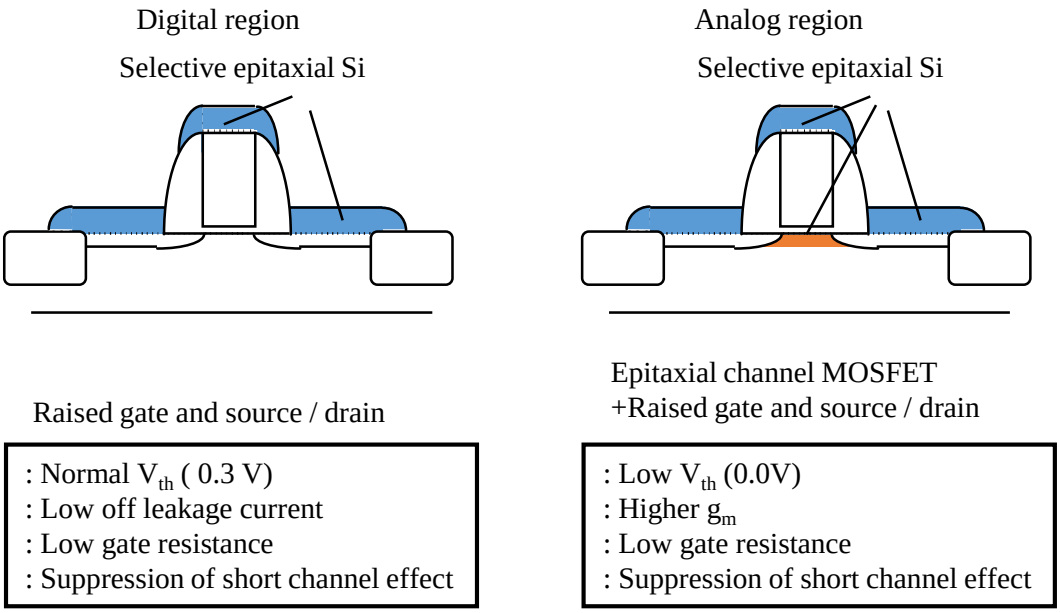


Figure 2-5-23. Selective epitaxial growth application to digital and analog MOSFET.

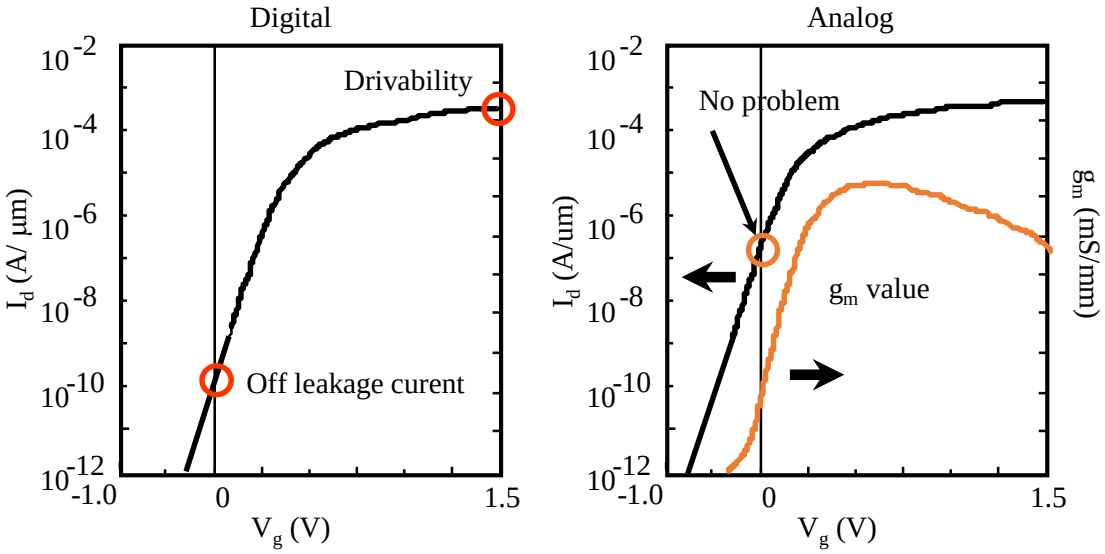


Figure 2-5-24. Requirements to digital and analog MOSFET.

In RF CMOS devices, low threshold voltage is required for analog RF MOSFET in order to obtain high gm, f_T and f_{MAX} under low gate bias. Subthreshold leakage current is not a problem because of the analog circuits configuration. Even zero voltage can be used for the threshold voltage value. On the other hand, threshold voltage of digital is higher than that of analog because off leakage current is problem as shown in Fig. 2-5-23 and 2-5-24.

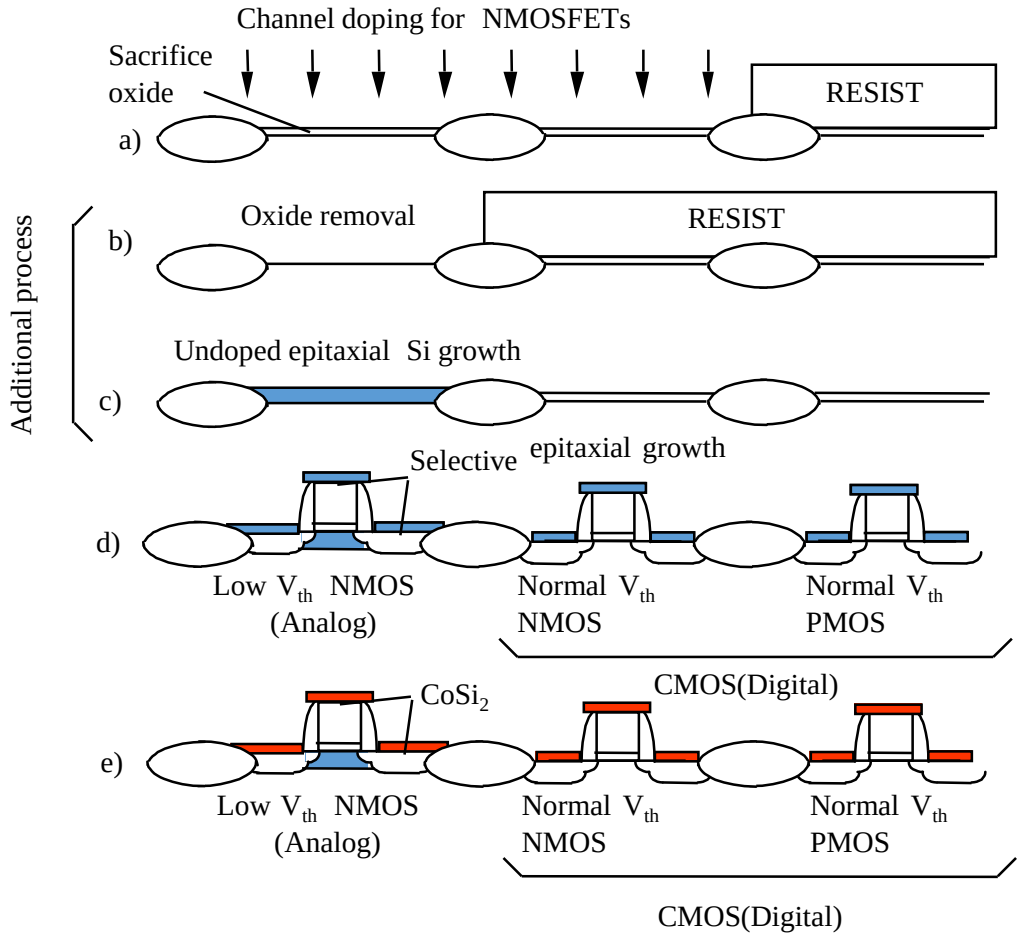


Figure 2-5-25. Process flow of RF CMOS for mixed epitaxial channel and raised gate/source/drain structures.

Figure 2-5-25 shows process flow of RF CMOS for 0.15 μm generation CMOS by using both the selective Si epitaxial channel and raised gate/source/drain techniques. MOSFETs in the digital logic circuits of RF CMOS is necessary to be sufficiently high to suppress the subthreshold leakage current. The optimum threshold voltage value should be above ±0.3V. Thus at least, two threshold voltages are required for nMOSFETs. This can be easily realized by using the selective Si epitaxial channel MOSFET technique. Another requirements for the RF CMOS is very low gate resistance of the short channel transistors. This can be realized by the use of raised gate, source, drain technique. The combination of the selective Si epitaxial channel and raised gate/source/drain techniques is attractive for the RF CMOS devices which involve both RF analog and digital circuits. The combination of the selective Si epitaxial channel and raised gate/source/drain techniques is attractive for the RF CMOS devices which involve both RF analog and digital circuits. Fig. 2-5-25 shows the process flow of RF CMOS for 0.15 μm generation using the above two techniques. The gate length of the 0.15 μm generation CMOS is chosen to be 0.11 μm.

Key process steps are explained using the cross-sectional views. After the formation of the isolation, thin sacrifice oxide was grown on Si substrate. Then, channel doping of n- and p-MOSFETs was carried out ion-implantation (Fig. 2-5-25a). The conditions are BF_2 at 30 KeV with dosage of 1 $\times 10^{13}$ cm^{-2} for digital and analog n-MOSFET and P^{++} at 120 KeV with 5.0 $\times$ 10^{13} cm^{-2}, As at 70 KeV with 4.0 $\times$ 10^{13} cm^{-2} and BF_2 at 15 KeV with 5 $\times$ 10^{13} cm^{-2} for digital p-MOSFETs, respectively. The sacrifice oxide was removed selectively in the analog n-MOSFET area by using a mask step (Fig. 2-5-25b). Then, un-doped epitaxial Si layer of 30 nm was grown selectively on this area by RP-CVD (Fig. 2-5-25c). The process conditions of RP-CVD are listed in Table 2-5-7. Just prior to the deposition, the native oxide layer was evaporated by using in situ high temperature pre-heating at 940 °C for 30 seconds in H_2 atmosphere. A 30 nm intrinsic or undoped silicon epitaxial layer was grown at 750 °C by using SiH_2Cl_2 gas. The growth rate is 2 nm / minute. After growing the selective epitaxial layers, the sacrifice oxide on the digital n- and p-MOSFET areas was removed by the etching of the entire region without masking as shown in Fig. 2-5-25d). Then, the gate oxide is grown. The temperature and time of gate oxide formation in dry O_2 atmosphere were 800 °C and 4 minutes, respectively. The thickness of gate oxide was 2.5 nm, which value is used for the supply voltage of 1.2 V. This thickness was determined by TEM photograph observation. The phosphorus doped polysilicon was used as the gate electrode. After the formation of the poly Si gate electrode, extension regions of source and drain (As : 10 KeV 2.0 $\times$ 10^{14} cm^{-2}) were formed by using ion implantation. After the formation of 50 nm Si_3N_4 sidewall, 50 nm undoped epitaxial Si layer were grown selectively on gate/source/drain by RP-CVD. T-shape gate electrode was fabricated after this process. Thanks to this shape of gate electrode, gate resistance was almost the same even if L_g decreases. Then arsenic implantation was carried out with the Si_3N_4 sidewall as a mask to form a source and drain region. A 950 °C for 30 seconds annealing was carried out to activate impurity. After that, Co salicide process was applied in order to reduce gate/source/drain resistance. After MOSFET formation, Co and TiN film were deposited by sputter. CoSi films were formed on source, drain and gate electrode selectively by annealing at 500 °C for 60 seconds. After removing non-reactive Co and TiN films, Co silicide was changed from CoSi to $CoSi_2$ by annealing at 750 °C for 30 seconds to reduce its resistively. Though sheet resistance of the gate electrode was 4 - 5 ohm/sq in conventional structure, 1.5 ohm/sq. can be realized in raised gate/source/drain structure.

It should be noted that I have 2 kinds of n-MOSFETs in a chip digital n-MOS without undoped epitaxial channel (with higher V_{th}) and analog n-MOS with undoped epitaxial channel (with lower V_{th}). After formation of CMOS, Co-salicide technique was used in this process to reduce source, drain and gate resistances significantly as shown in Fig. 2-5-25e). After MOSFET formation, Co salicide process was applied in order to reduce gate/source/drain resistance. By using this process, sheet resistance of the gate electrode below 5 ohm/sq. was realized even at the gate length of 0.1 μm. The sheet resistance of the source and drain were also 5 ohm/sq. Finally, metallization was carried out. The production cost for this multi-V_{th} CMOS is only slightly higher than that for the conventional single CMOS. The number of the process steps is only increased by 2: (1) removing sacrifice oxide (Fig. 2-5-25b) and (2) undoped epitaxial Si growth on analog n-MOSFET region (Fig. 2-5-25c).

Table 2-5-8. Comparing device parameter our new 0.15 μm NMOS with those of the 1997 SIA roadmap.

	L_g	Tox	Tsw	Extension : Conc.
Roadmap	0.12 μm	2-3 nm	60-120 nm	$1E10^{19}$ cm^{-3}
Our devices	0.12 μm	2.1 nm	50 nm	$1E10^{20}$ cm^{-3}

Extension : Xj	V_d	Drain structure	Channel engineering
30-60 nm	1.2-1.5 V	Drain extension	Implantation
40 nm	1.2-1.5 V	Raised source and drain	Implantation (digital)
			Epitaxial channel (analog)

Table 2-5-9. compared with those of 0.12 μm gate length logic and mixed analog CMOS of the 1997 SIA roadmap.

Max. I_{off} @25 °C	Nominal I_{drive}	Gate delay metric (CV/I)	Gate sheet res. (Ohm/sq.)	V_{th} variation (3 sigma)	f_T	$N.F._{min}$ @2 GHz
3 nA/um	600uA/um	9-10 ps	4-6	45 mV	40 GHz	1.3 dB
1 nA/um	640uA/um	4.7 ps	1-2 (effective)	60 mV	80 GHz	Below 0.1 dB

Table 2-5-8 shows comparing device parameters of our new 0.15 μm NMOS with those of the 1997 SIA roadmap. Basically our parameters and structure are compatible to those of the roadmap for 0.12 μm gate length MOSFET (or 0.15 μm technology generation), except MOSFET structure , T_{sw} and extension concentration. In our devices, because raised gate/source/drain structure is adopted, short channel effect can be suppressed even when T_{sw} is 50 nm. And in order to achieve higher drive current and g_m, extension concentration of our device is higher than that of roadmap. Our obtained characteristics are compared with those of 0.12 μm gate length logic and mixed analog CMOS of the 1997 SIA roadmap in Table 2-5-8. Requirements to RF analog device such as f_T and noise figure are satisfied, and those to digital device such as I_{off}, I_{drive} gate delay metric (CV/I) and gate sheet resistance were satisfied. However, V_{th} variation is still larger. This could be improved in future eventually as the technology becomes mature, but the specification may be also reconsidered.

Conclusions

Selective Si epitaxial growth technology and its application to Si devices have been reviewed. Especially, its application to RF CMOS has been explained. It was demonstrated that epitaxial channel and raised gate, source, drain techniques are very useful for improving mixed-signal and RF characteristics of CMOS.

By introducing non doped epitaxial Si layer to channel of MOSFET, higher drivability is achieved because low V_{th} and higher mobility with suppressing short channel effect due abrupt profile of boron. Thanks to lower channel concentration, standard deviation of delta of V_{th} between pair MOSFET is lower. Additionally, 2-5 dBA lower 1/*f* noise can be realized than conventional structure because high quality Si layer is formed on damage layer by well and channel ion implantation and interface state density becomes lower. By introducing non doped epitaxial Si layer to gate poly Si, T-shape gate structure is formed and gate resistance becomes lower. As a result, T-shape gate electrode with $CoSi_2$ brings higher f_{MAX} of 61 GHz when L_g = 0.15 μm are obtained while f_{MAX} of 50 and 30 GHz for non $CoSi_2$ and $CoSi_2$ without T-shape gate electrode.

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Chapter3 Reduction of 1/f noise of CMOS

3-1. Analog characteristics of CMOS with heavily nitrided NO oxynitrides

3-1-1. Introduction for 1/*f* noise

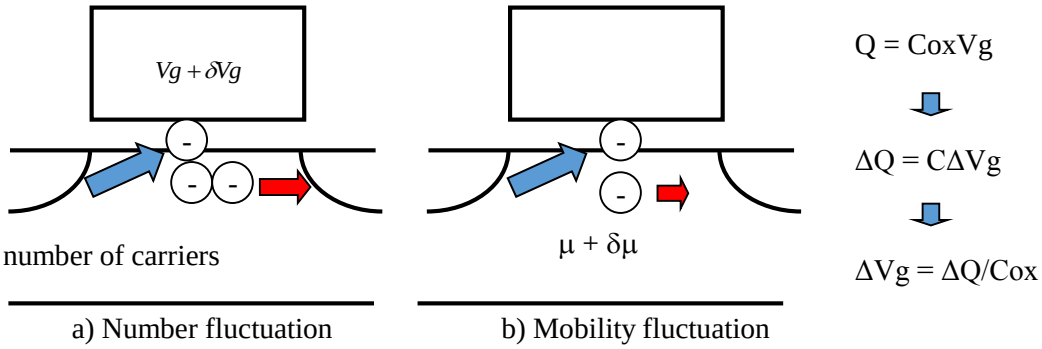


Figure 3-1-1. The mechanism of 1/f noise by trap and de-trap of carrier.

$S_{Id} \propto \frac{\tau}{1+\omega^2\tau^2}$: Sid by single trap $\quad \tau = \left(\frac{1}{\tau_c}+\frac{1}{\tau_e}\right)^{-1}$: time of trap and de-trap

$f1 = \frac{1}{\tau 1}$: frequency of trap and de-trap

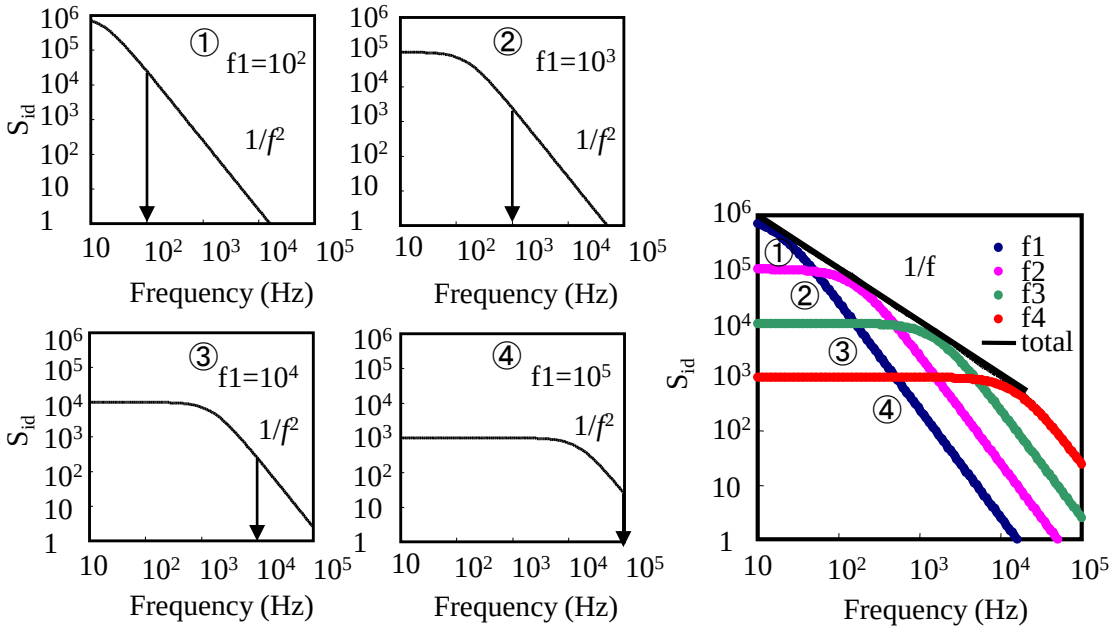


Figure 3-1-2. The explanation of frequency dependence of S_{id}.

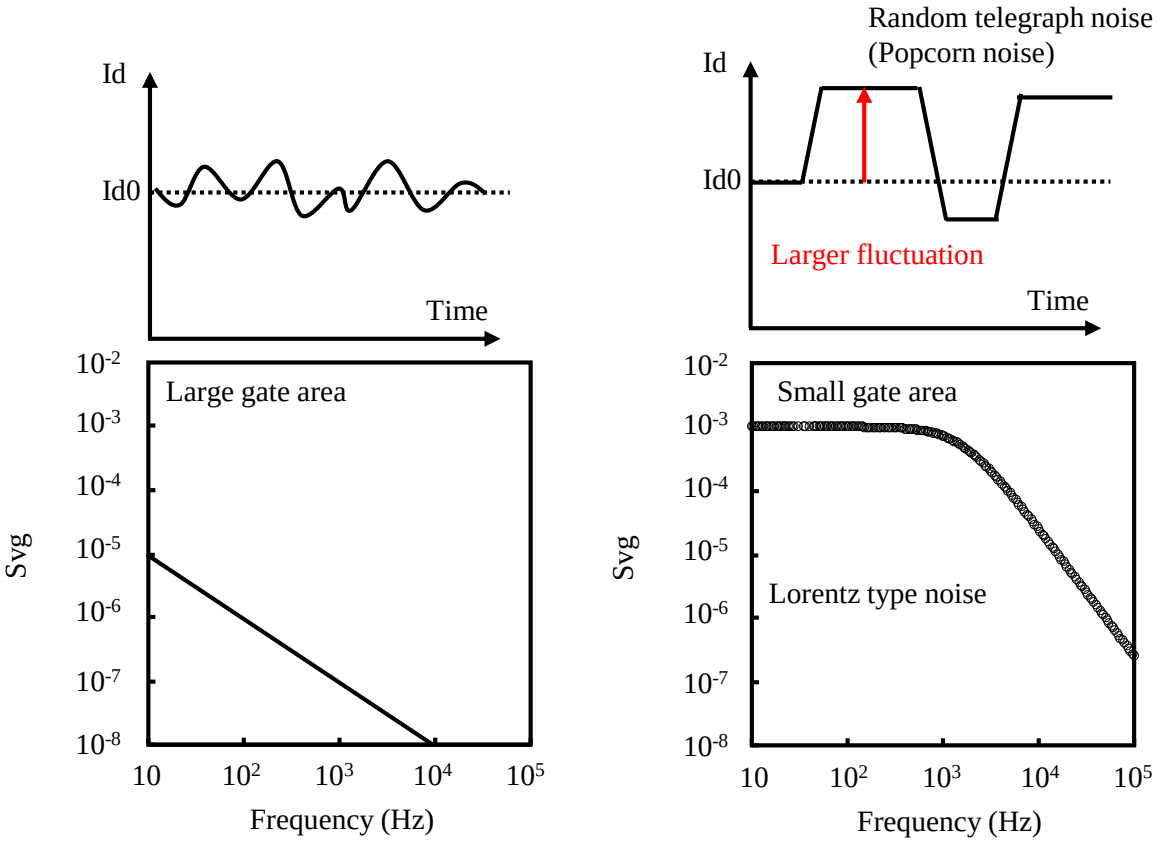


Figure 3-1-3. The behavior of current fluctuation at small and large gate area.

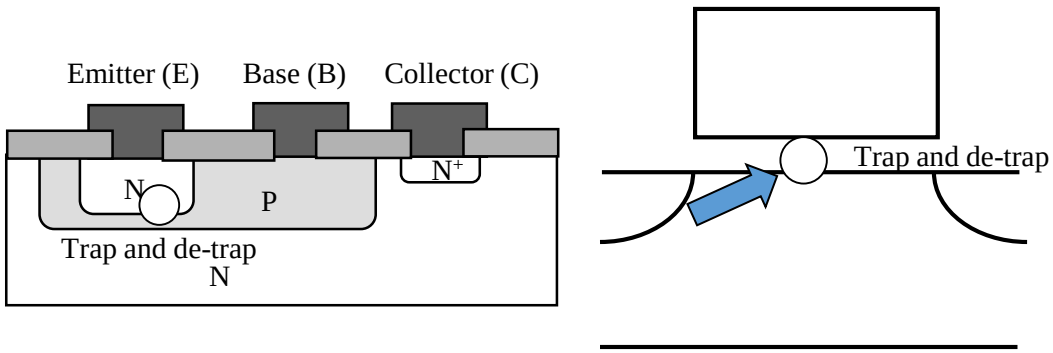


Figure 3-1-4. Comparison of 1/*f* noise between bipolar and MOSFET.

Fig. 3-1-1 shows the mechanism of 1/*f* noise by trap and de-trap of carrier. The trap and de-trap carrier causes fluctuation of gate voltage and make carrier number fluctuate (carrier number fluctuation). Or the trap and de-trap carrier causes fluctuation of mobility by column scattering (mobility fluctuation). The fluctuation increases as the gate area decreases because of smaller gate capacitance. Thus, scaling MOSFET has degraded 1/*f* noise. Fig. 3-1-2 shows the explanation of frequency dependence of S_{id}. When single trap and de-trap is occurred, the S_{id} show Lorentz type noise. When various trap and de-trap time, 1/*f* noise appears because the S_{id} consists of sum of the noise with various trap and de-trap time. When the gate area is small, Lorentz type noise appears because number of trap and de-trap becomes small as shown in Fig. 3-1-3. In this case, random telegraph noise (RTN), which sometimes called as Popcorn noise appears in time domain. This RTN has serious problem in CMOS image sensor or Flash memory because those use MOSFET or cell transistor with small gate area.

In bipolar device, the 1/*f* noise occurs at interface between emitter and base and the noise is in proportional to the junction area, that is emitter size as shown in Fig. 3-1-4. Thus, the noise is normalized by the emitter size. Generally, the 1/*f* noise (S_{vg}) of bipolar is 1-5 (μV^2-mm^2 /Hz) at 1Hz which is 2 order lower than that of MOSFET. Because MOSFET has interface between gate insulator and Si substrate, gate insulator and gate electrode, which causes carrier trapping and larger 1/*f* noise during operation of MOSFET, while the bipolar has no interface with insulator. Thus, the bipolar has advantage structure with lower 1/*f* noise.

3-1-2. Sample fabrication

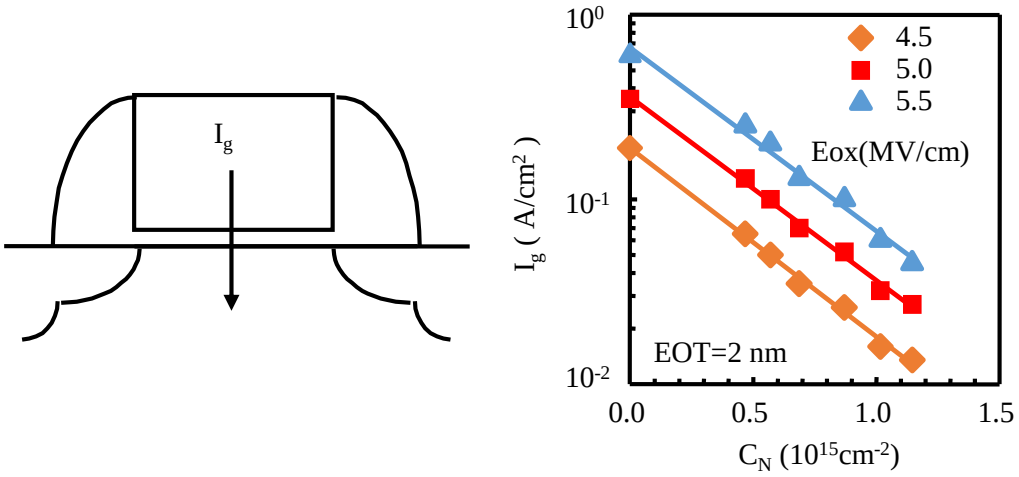


Figure 3-1-5. Nitrogen concentration dependence of gate leakage current [1].

- STI process
- **Well and channel formation (Surface or buried channel)**
- **Gate insulator formation Oxidation + Nitridation (NO gas)**
- Gate electrode formation
- Source and drain formation
- Co salicide process
- Metallization

Figure 3-1-6. Nitrogen concentration dependence of gate leakage current.

As the generation of MOSFET progresses, gate length size has been shorter and gate oxide has been thinner in order to realize high speed operation. But as the gate oxide becomes thinner especially below 3nm, gate leakage current increases rapidly due to direct tunneling current. This leakage current prevents realization of low power consumption chip. Recently, aggressive trials such as high-K materials have been introduced in order to solve the problems. On the other hand, heavily nitrided oxinitride film is one of some candidates to reduce the leakage current with increasing nitrogen concentration. Right hand in Fig. 3-1-5 is nitrogen concentration dependence of gate leakage current, which was reported by Dr. Fujiwara et al. in VLSI Symposium 2000 [1]. One order lower gate leakage current can be realize when areal density is ten times fifteenth per square cm. However, there are some problems for mixed analog and digital chip. Those are 1/*f* noise and mobility degradation. The larger the noise brings larger phase noise of VCO and lower mobility brings lower gain of some amplifiers.

Thus, we must know nitrogen concentration dependence of the noise and choose the optimum conditions for realization of high performance mixed analog and digital circuits.

Figure 3-1-6 shows process flow of our samples. After STI process to isolate activation area, ion implantation was carried out for well and channel formation. In this process, counter doped layer was formed for buried channel MOSFET. Then, after based gate oxide was thermally grown, oxynitrided was formed with NO gas annealing. Nitrogen concentration was controlled by the annealing conditions. In order to discuss nitrogen concentration dependence of 1/*f* noise accurately, effective gate oxide thickness was fixed by changing based oxide thickness for NO gas anneal conditions. After source and drain formation, Co-salicide was applied to these devices.

2-2-I-4) Mixed signal and RF characteristics

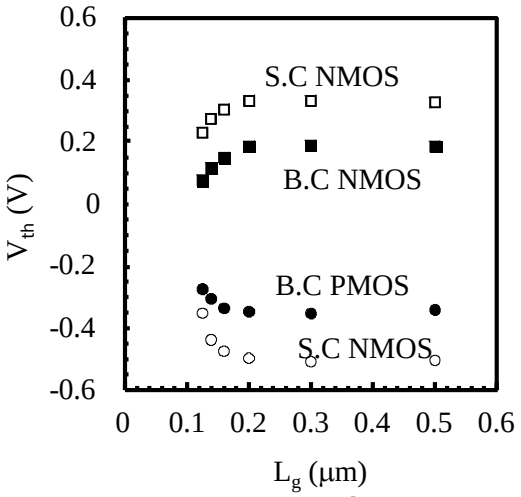


Figure 3-1-7. L_g - V_{th} characteristics for surface channel and buried channel structure MOSFETs.

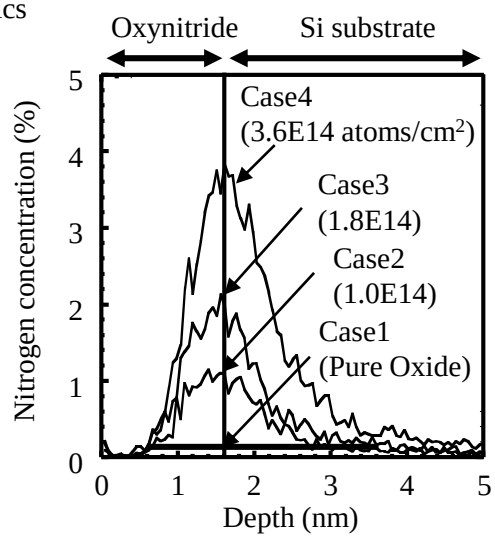


Figure 3-1-8. Nitrogen profile in oxynitride film.

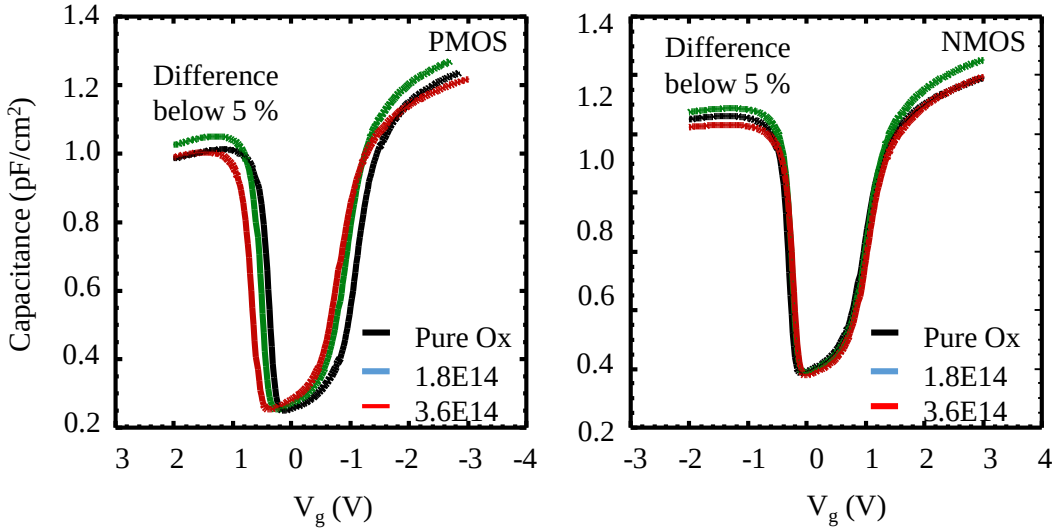


Figure 3-1-9. C - V measurement results of CMOS with pure oxide and oxynitride film.

Figure 3-1-6 shows process flow of our samples. After STI process to isolate activation area, ion implantation was carried out for well and channel formation. In this process, counter doped layer was formed for buried channel MOSFET. Then, after based gate oxide was thermally grown, oxynitrided was formed with NO gas annealing [2-17]. Nitrogen concentration was controlled by the annealing conditions. In order to discuss nitrogen concentration dependence of 1/*f* noise accurately, effective gate oxide thickness was fixed by changing based oxide thickness for NO gas anneal conditions. After source and drain formation, Co-salicide was applied to these devices. Figure 3-1-7 shows gate length dependent of V_{th} for surface channel (S.C.) and buried channel (B.C) NMOS and PMOS. The V_{th} value of B.C. is lower than that of S.C. because B.C. has counter doped layer. The short channel effect were suppressed down to gate length of 0.1 μm.

Figure 3-1-8 shows the nitrogen profile in various oxynitride films. The nitrogen areal density at interface between oxynitride and Si substrate was changed by NO gas annealing conditions. Case 1 is pure oxide case and Case 4 is highest density case such as 3.6E14 atoms/cm^2. I have observed roughness at interface between oxynitride and Si substrate for all samples by using TEM photographs but no difference was found.

Because flicker noise S_{vg} has dependence of square of gate capacitance, The C-V measurement for NMOS and PMOS was carried out as shown in Fig. 3-1-9. Comparing with all samples results, the difference was within 5 % for both NMOS and PMOS. Thus we can discuss only nitrogen concentration dependence of 1/*f* noise accurately, because this difference does not have large affection to 1/*f* noise results.

3-1-3. Mixed signal and RF characteristics

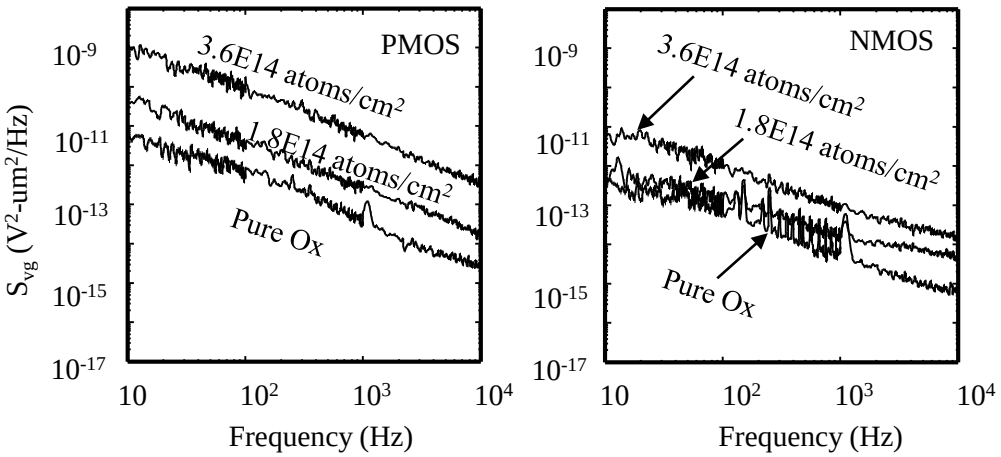


Figure 3-1-10. Nitrogen areal density dependence of 1/*f* noise (Surface channel).

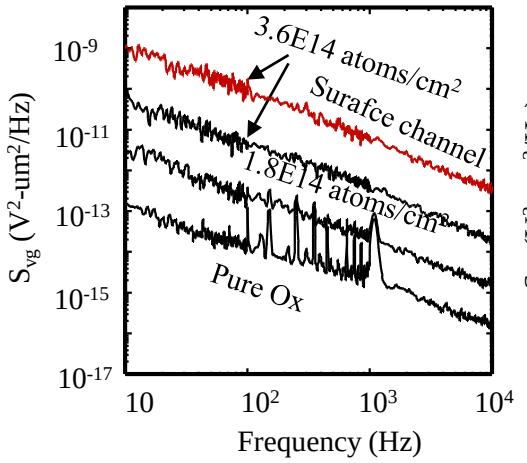


Figure 3-1-11. Nitrogen areal density dependence of 1/*f* noise (Buried channel pMOSFET).

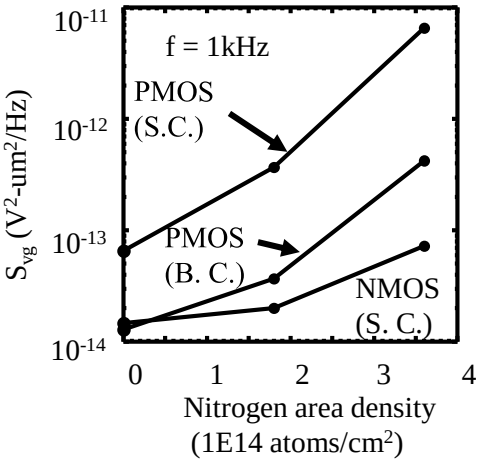


Figure 3-1-12. Dependence of S_{vg} on nitrogen area density.

Figure 3-1-10 shows nitrogen areal density dependence of 1/*f* noise for surface channel CMOS. In the case of PMOS, the noise was sensitive to nitrogen density and two orders higher noise was observed in highest density case. On the other hand, in the case of NMOS, increase of the noise due to nitrogen was smaller than that of PMOS and one orders higher noise was observed in highest density case. I think this difference may be caused by energy level of trap density, which is related to 1/*f* noise.

Figure 3-1-11 shows nitrogen areal density of 1/*f* noise for buried channel PMOSFET. A data in surface channel case with highest nitrogen concentration is plotted as a reference. The noise of buried channel cases in the same concentration were one or two order lower compared with surface channel cases. Nitrogen dependence of the noise was almost same as surface channel case and two orders higher noise was observed in highest density case. The thickness of inversion layer is larger in buried channel case at same gate bias and the hole in only surface region brings 1/*f* noise. Thus the noise of buried channel case was lower than that of surface channel case [18,19].

Figure 3-1-12 shows summary of nitrogen areal density dependence of S_{vg}. The slope of PMOS was larger than that of NMOS. I think that as nitrogen concentration increases, trap density, which is related to 1/*f* noise, also increases.

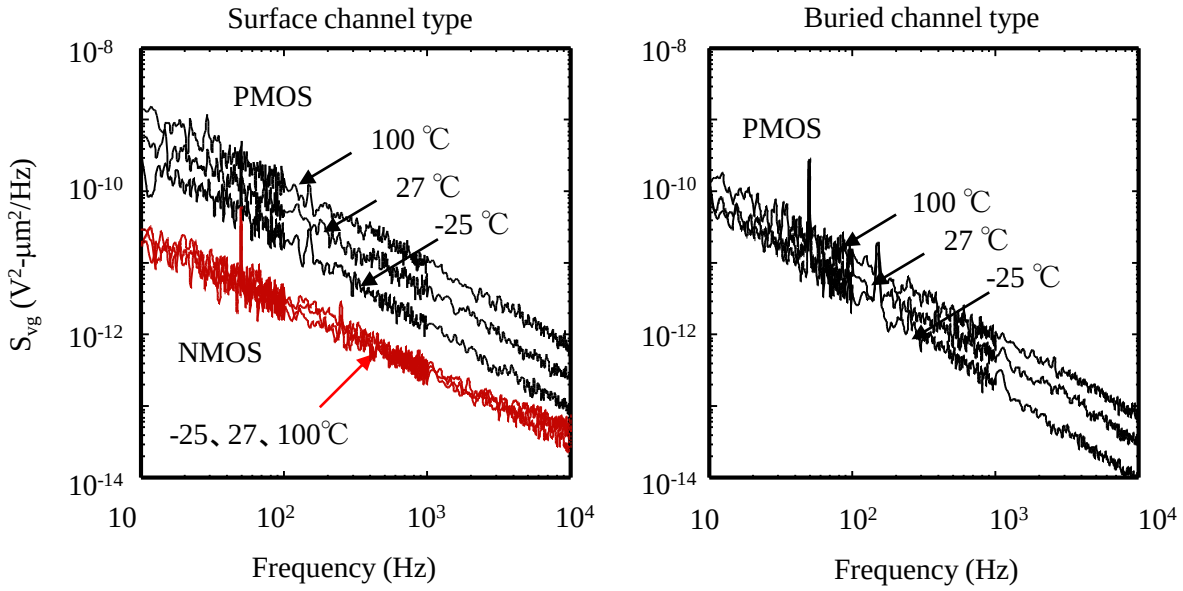


Figure 3-1-17. Temperature dependence of 1/*f* noise.

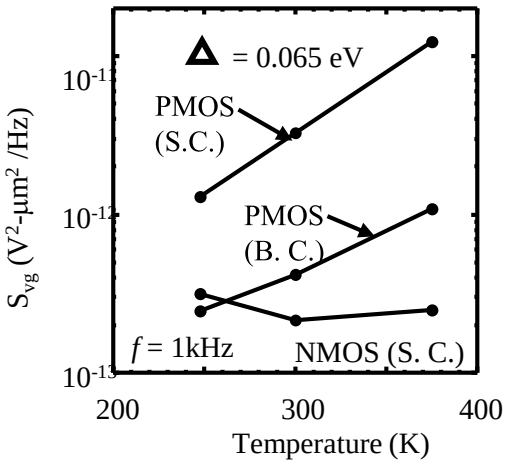


Figure 3-1-18. Temperature dependence of 1/*f* noise at 1k Hz.

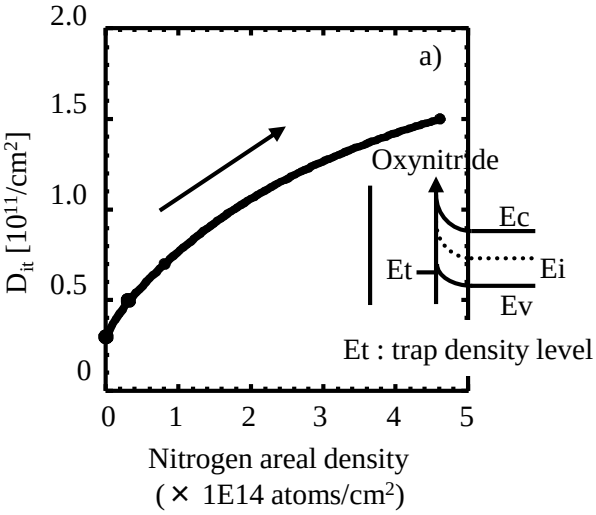


Figure 3-1-19. A model of 1/*f* noise degradation with nitrogen areal density.

Figure 3-1-17 shows dependence of 1/*f* noise on the temperature. The measurement frequency was 1K Hz. the slope of PMOS is extremely larger compared with NMOS and that is regardless of MOSFET structure such as surface and buried channel. If energy level of trap density is close to valence band, we can explain this phenomenon. Because in this case, the probability of trapped hole is larger than that of the electron. I estimated activation energy by using temperature dependence. The obtained value was 0.065 eV.

Figure 3-1-18 shows dependence of interface state density on nitrogen areal density. As the nitrogen concentration increases from 0 to 3.8E14 atoms/cm^2, the D_{it} increases from 0.3 to 1.4 E11 cm^{-2}. The increase is about 5 times. In generally, it is said that the larger D_{it} brings higher 1/*f* noise. Figure 3-1-19 explains 1/*f* noise degradation model in CMOS with heavily nitrided NO oxynitrides. First, trap density near valence band increase with increasing nitrogen concentration. Second is that energy level is 0.065 eV from valence band according to temperature dependence of 1/*f* noise.

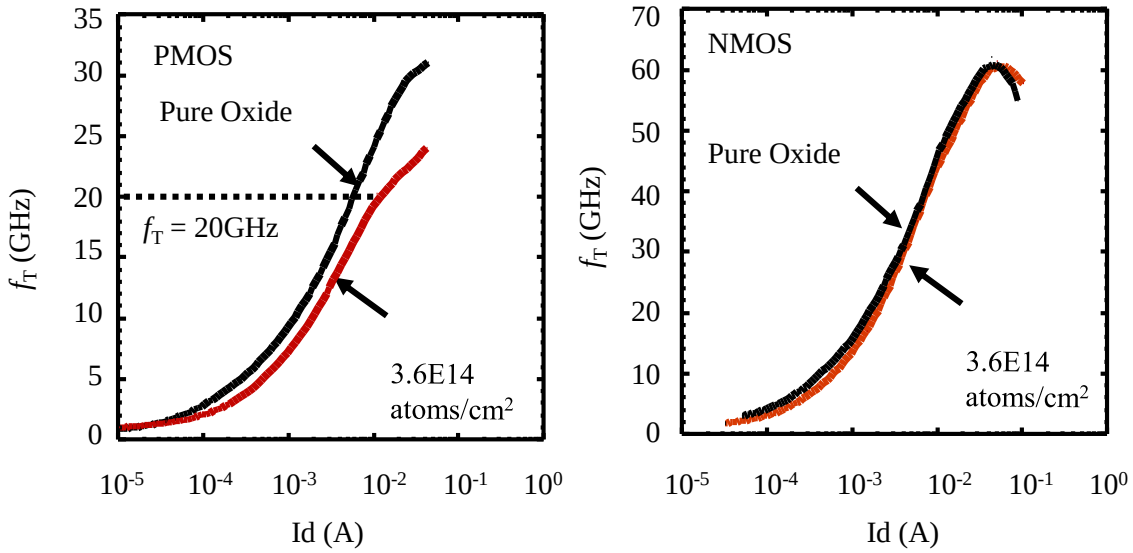
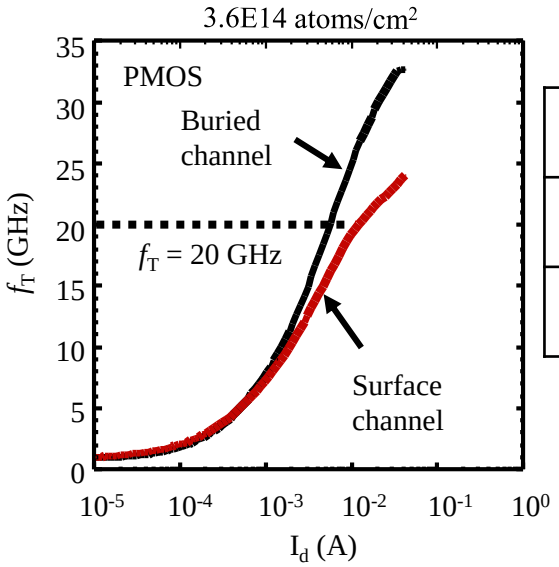


Figure 3-1-20. F_T - I_d characteristics (Surface channel) when L_g = 0.14 μm, W_g = 200 μm, V_d = 1.5 V.



	Surface channel		Buried channel
Nitrogen areal density	Pure Oxide	3.6E14 atoms/cm^2	3.6E14 atoms/cm^2
I_d at f_T=20 GHz	29 mA	60 mA	29 mA

Figure 3-1-21. F_T - I_d characteristics (Buried channel) when L_g = 0.14 μm, W_g = 200 μm, V_d = 1.5 V.

Figure 3-1-20 shows f_T-I_d characteristics for pure oxide and heavily nitrided oxynitride case. In the case of NMOS, no degradation was observed. On the other hand, In the case of PMOS, f_T max value was changed from 32 GHz to 25 GHz due to heavily nitrided oxynitride. The decrease was 22%. And seeing drain current when f_T value is 20 GHz, two times higher drain current needs compared with pure oxide case. However, f_T value recovered changing MOSFET structure from surface channel to buried channel. This slide shows f_T-I_d characteristics in buried channel case. The f_T max value recovered up to 34 GHz and drain current as f_T is 20 GHz become a same level as that of pure oxide case.

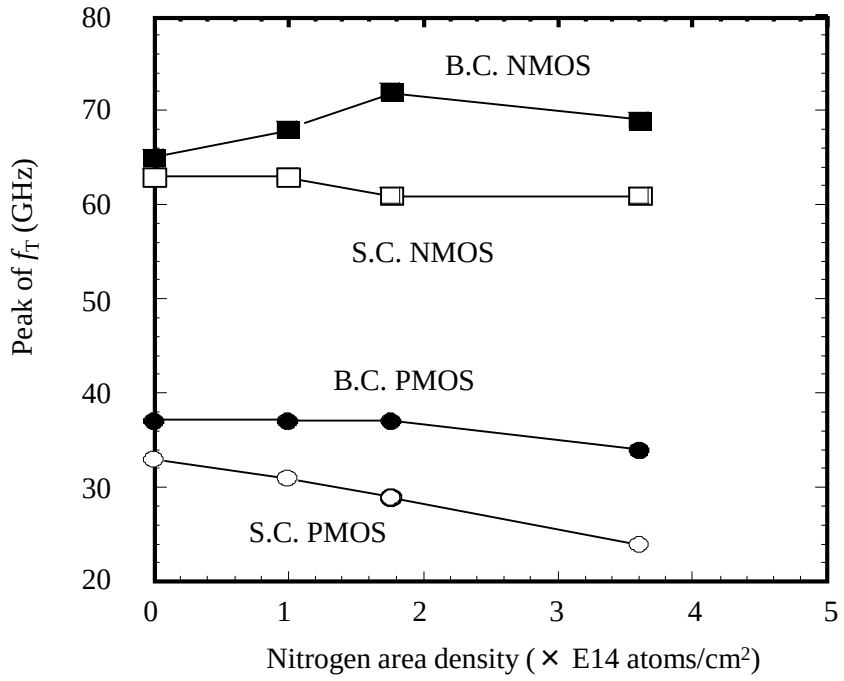


Figure 3-1-22. Nitrogen areal density dependence of f_T_peak.

Figure 3-1-22 shows summary nitrogen areal density dependence of peak f_T value. As nitrogen areal density increases, especially, f_T value in surface channel decreases. However, f_T value degradation is small in buried channel PMOSFET. This results shows that buried channel MOSFET is useful to suppress f_T value degradation as well as 1/f noise degradation when mixed analog and digital circuits are designed by using CMOS with heavily nitrided oxynitride films formed by NO gas annealing.

3-2. Oxynitride process, deuterium annealing and STI stress dependence of 1/*f* noise

3-2-1. Sample fabrication

- STI formation
- Well and channel formation
- Thermal oxidation
- **Nitridation (NO gas annealing or plasma nitridation)**
- Gate electrode formation
- Source and drain formation
- Co salicide process
- M1 formation
- **Dilute H_2 or D_2 gas annealing**

Figure 3-2-1. Process flow for sample fabrication.

Table 3-2-1 C_N and EOT values in oxynitride film for all samples

Process	NO gas annealing			Plasma nitridation		
C_N ($\times 10^{15}$) (cm^{-2})	0.25	0.40	0.94	0.72	1.36	2.71
EOT (nm)	1.9	1.9	2.0	2.2	2.0	1.8

C_N : Nitrogen areal density
EOT : Equivalent oxide thickness

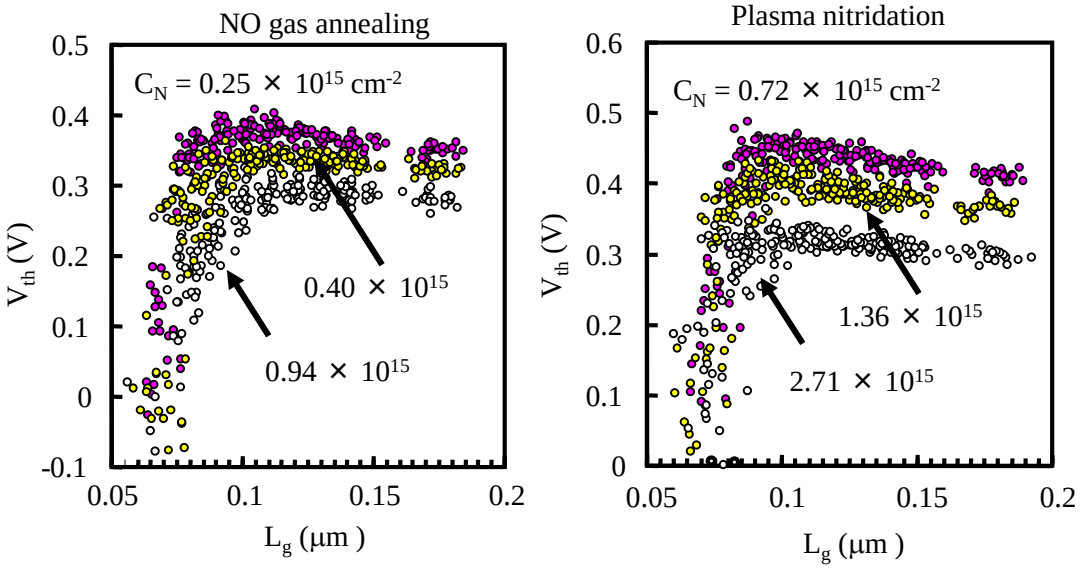


Figure 3-2-2. Gate length dependence of V_{th} for NMOS. Parameter is C_N in oxynitride film for all samples.

Process flow : After STI fabrication, well and channel ion implantation was carried out. After oxide was thermally grown, oxynitride was formed by NO gas annealing or plasma nitridation process [20-24]. Then, gate electrode, source and drain were formed. Co salicide was applied to device in order to reduce parasitic resistance. After M1 formation, sintering was done by dilute hydrogen or deuterium gas annealing [25-29].

Table 3-2-1 shows nitrogen areal density and EOT value in oxynitride for all samples. The areal density was measured by XPS analysis and EOT was estimated by C-V measurement. The EOT ranged from 1.9 to 2.1 nm in the samples. In the NO gas annealing case, the density ranged from 0.25 to 0.94 × 10^{15} cm^{-2}. On the other hand, in the plasma nitridation case, the density is higher than in the NO case, ranging from 0.72 to 2.71 × 10^{15} cm^{-2}.

Figure 3-2-2 shows gate length dependence of V_{th} for NMOS. Results for the NO gas annealing case are shown on the left. Those for the plasma nitridation case are shown on the right. The parameter is nitrogen areal density in oxynitride. The V_{th} slightly decreases as the density increases in both cases. Thanks to shallow source and drain, and thinner gate oxynitride film, short channel effect can be suppressed by 80 nm.

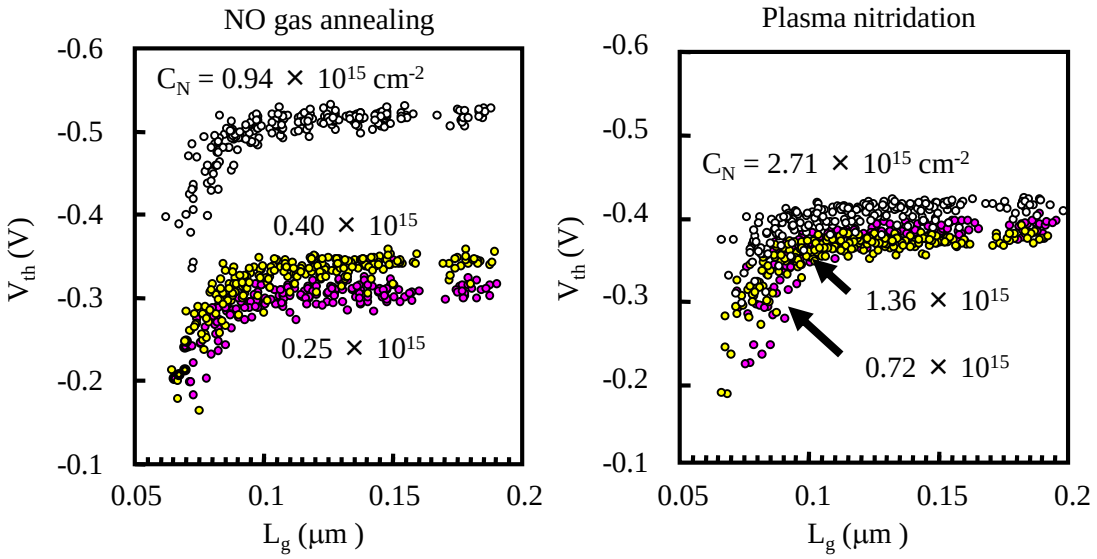


Figure 3-2-3. Gate length dependence of V_{th} for PMOS. Parameter is C_N in oxynitride film for all samples.

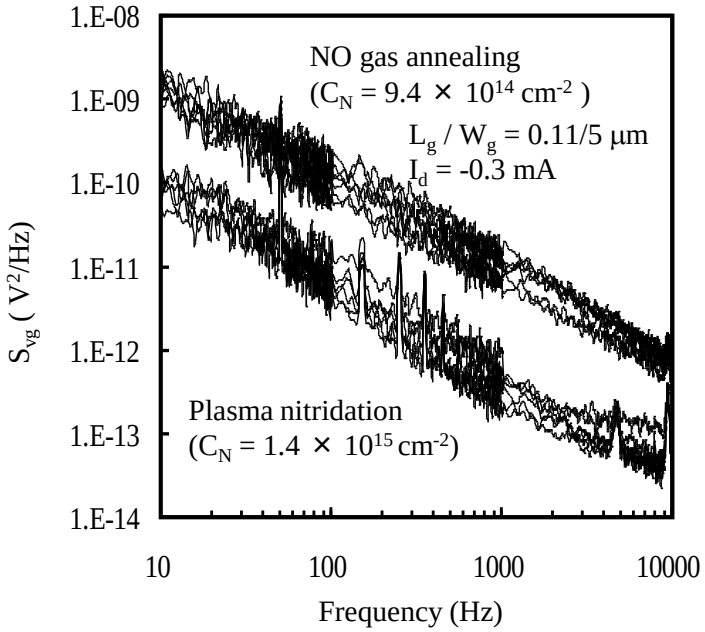


Figure 3-3-4. 1/*f* noise characteristics of PMOS with oxynitride gate insulator formed by NO gas annealing or plasma nitridation process.

PMOS is in contrast to NMOS, absolute V_{th} value increases with the areal density. V_{th} in PMOS, at 0.94 × 10^{15} cm^{-2} for the NO gas annealing case, is significantly larger than at any other density. The value is 0.54 V. On the other hand, maximum V_{th} is 0.42 V in the plasma nitridation case, though the density is far larger than in the NO case.

Figure 3-2-4 shows 1/*f* noise measurement results for NO gas annealing or plasma nitridation process. Horizontal axis shows frequency and vertical axis shows flicker noise. The areal densities in the NO annealing and plasma nitridation cases are 0.94 and 1.36 × 10^{15} cm^{-2}, respectively. In spite of the higher density, the flicker noise in the plasma nitridation is about one order lower than that in the NO annealing [11,12].

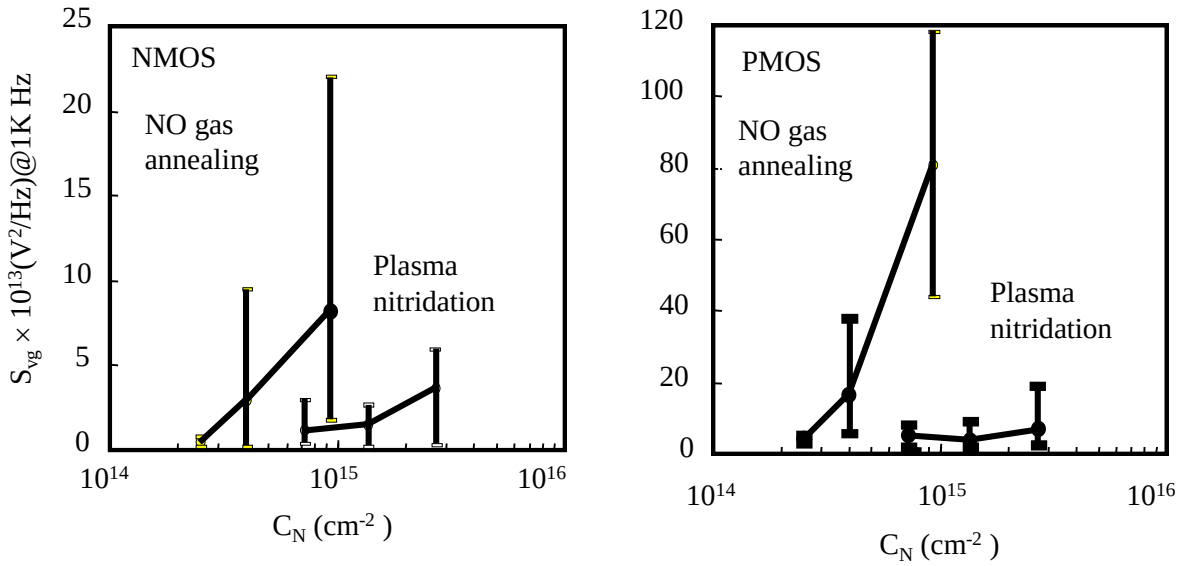


Figure 3-2-5. Dependence of S_{vg} on C_N for NMOS and PMOS.

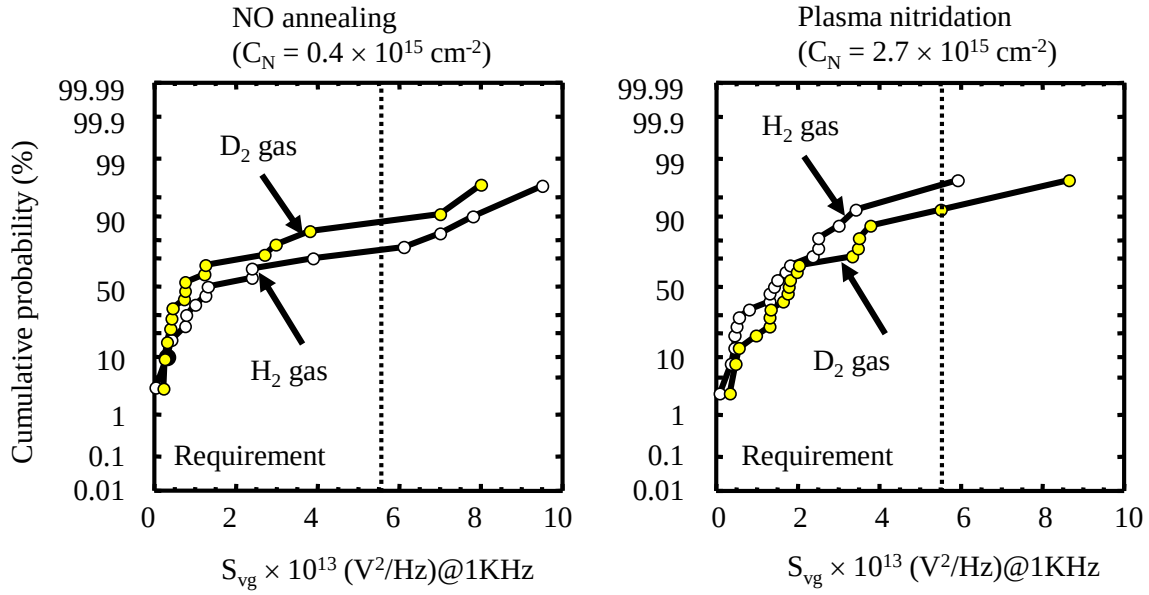


Figure 3-2-6. The effect of deuterium annealing for NMOS.

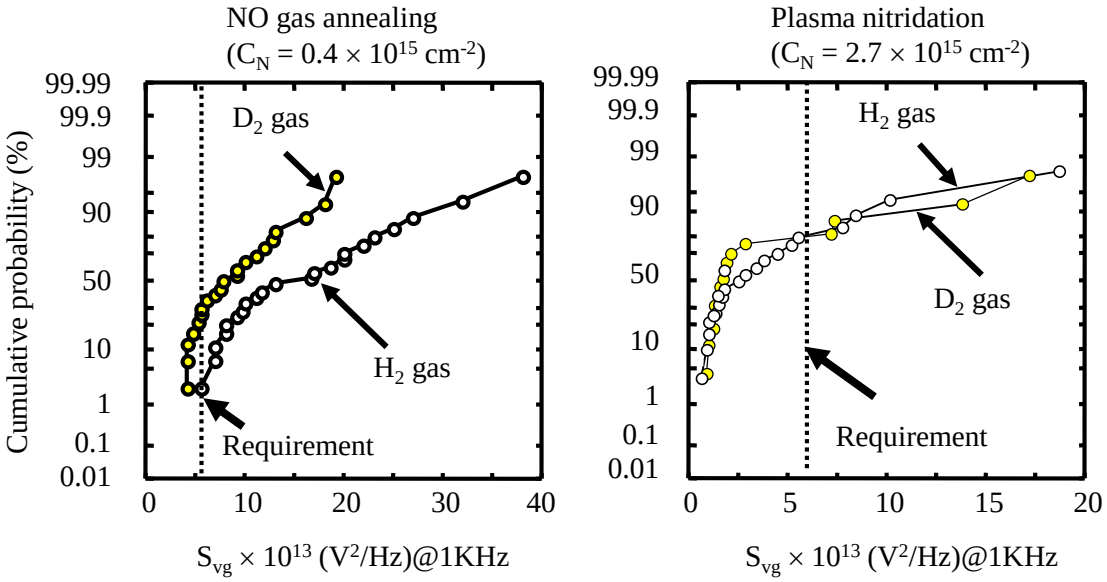


Figure 3-2-7. The effect of D_2 annealing for PMOS.

Figure 3-2-5 shows dependence of the noise on the nitrogen areal density for NMOS and PMOS. In these figures, not only average but also maximum and minimum values are plotted to confirm the dispersion. The flicker noise and the dispersion increased with increasing the areal density regardless of nitridation process. Especially, those of the NO gas annealing are significantly larger compared with the plasma nitridation case and even when areal density is 0.4 × 10^{15} cm^{-2}. In PMOS cases, the flicker noise is sensitive to nitrogen concentration significantly compared with those of NMOS. In order to satisfy the requirement, the areal density should be below 2.7 × 10^{15} cm^{-2} in plasma nitridation.

Figure 3-2-6 shows the effect of deuterium annealing for NMOS. Horizontal axis shows the flicker noise and vertical axis shows cumulative probability. Results for the NO gas annealing case are shown on the left. Those for the plasma nitridation case are shown on the right. In the case of NMOS, there is little difference in the noise and dispersion between dilute hydrogen and deuterium annealing. Figure 3-2-7 shows the effect of deuterium annealing for PMOS. In the case of plasma nitridation case, little difference was observed, while in the case of NO gas annealing, the average and dispersion in dilute deuterium annealing were half of those in the hydrogen annealing [12, 25,29].

3-2-3. Dependence of flicker noise on distance between gate and STI edge

Table 3-2-2. Device parameter for investigation of STI stress.

Device parameter	Value
EOT	2.5 nm
Process	NO gas annealing
C_N	1.0×10^{14} cm^{-2}
Lg / Wg	0.11 μm / 5 μm
Distance (D)	12, 5.0, 1.5, 0.5 μm

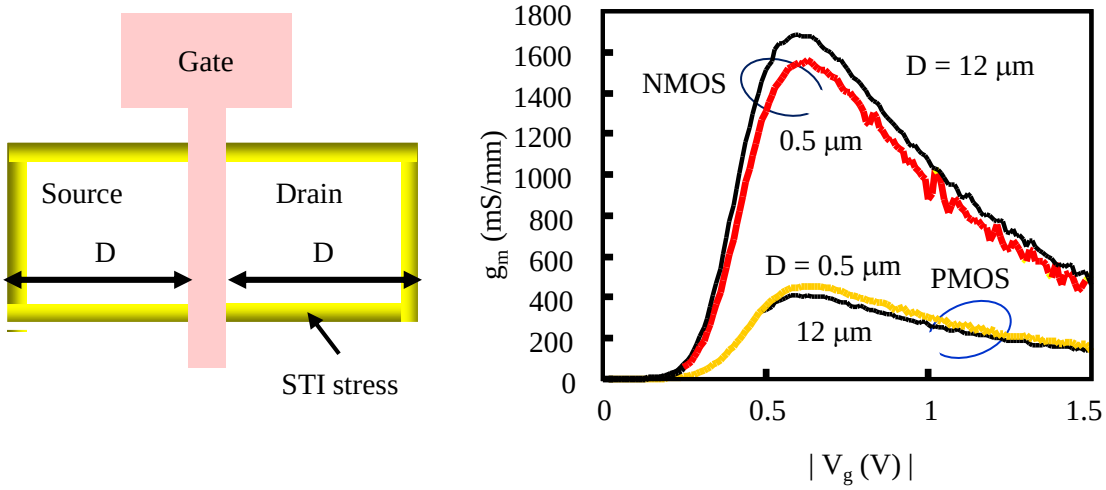


Figure 3-2-8. Effect of STI stress on DC characteristics.

Table 3-2-2 shows device parameters for samples in this experiments. EOT is 2.5 nm, nitrogen process is NO gas annealing, and the areal density of nitrogen is 1.0×10^{14} cm^{-2}. The distance between gate electrode and STI edge ranged 0.5 to 12 μm. Figure 3-2-8 shows transconductance – V_g curves in triode region for 0.11 μm CMOS. The transconductance in NMOS degraded as the distance between gate electrode and STI edge changes from 12 to 0.5 μm. On the contrary, that in PMOS increased as STI edge becomes closer to gate electrode.

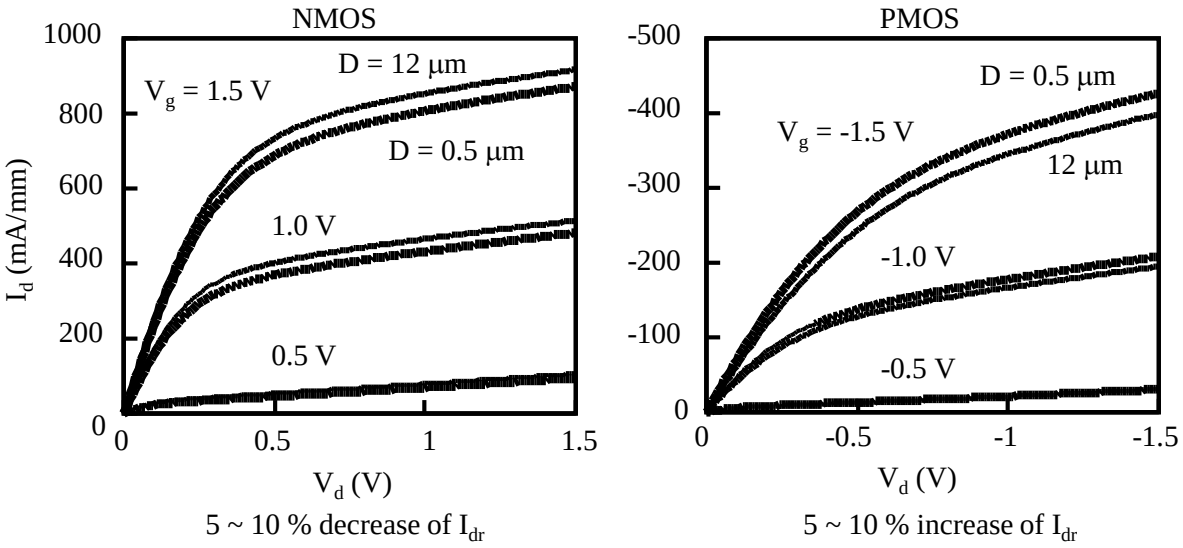


Figure 3-2-9. Effect of STI stress on DC characteristics.

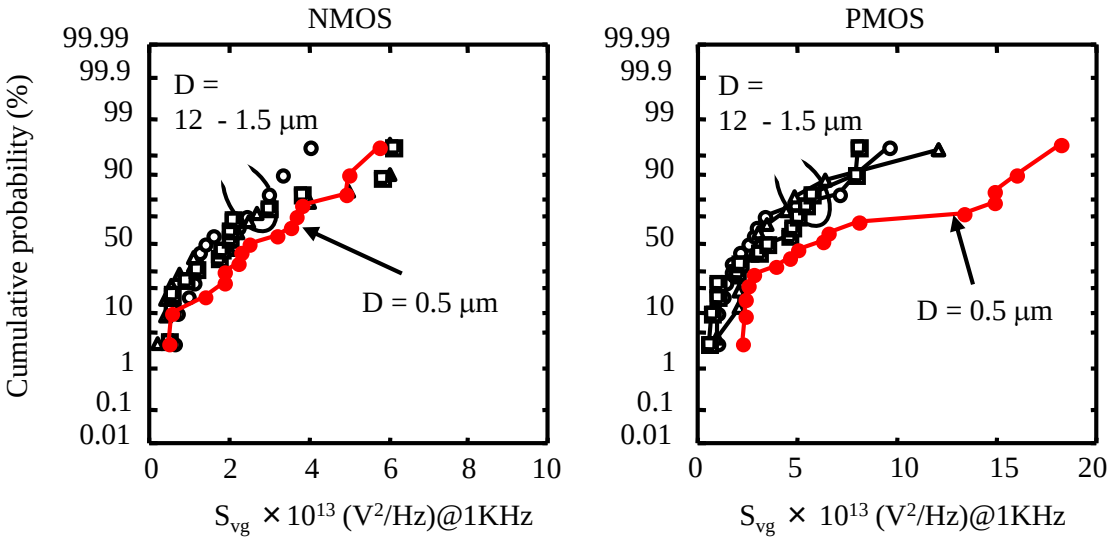


Figure 3-2-10. Effect of STI stress for 1/*f* noise.

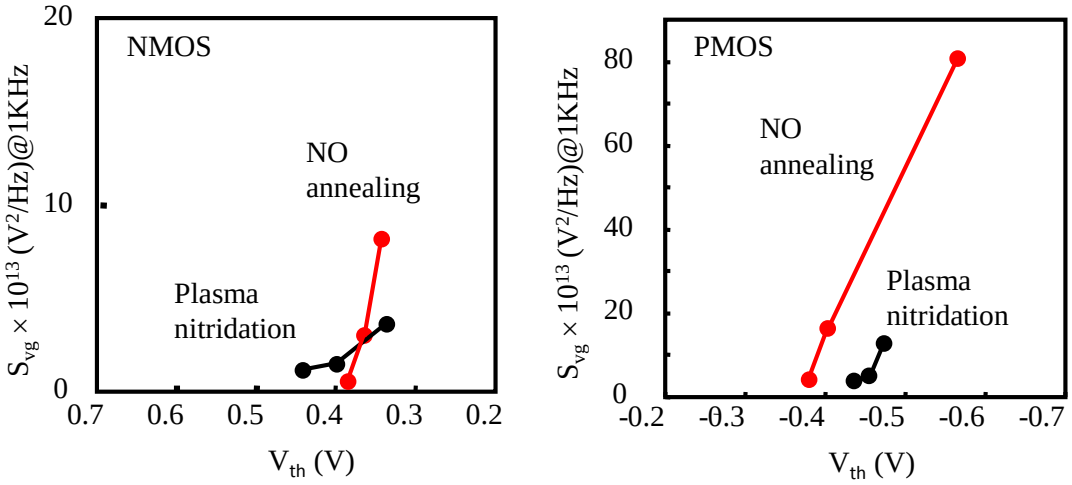


Figure 3-2-11 V_{th} dependence of flicker noise for NMOS and PMOS

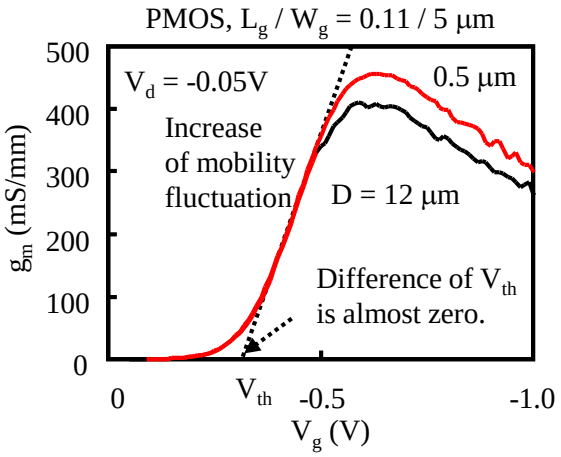


Figure 3-2-12. Difference of V_{th} in PMOS for D = 12 and 0.5 μm.

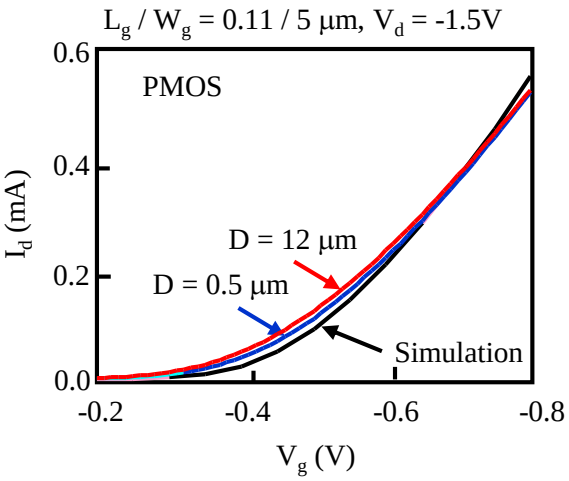
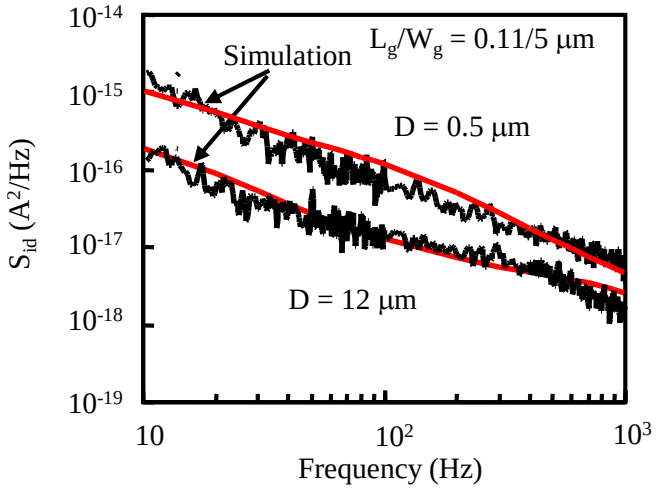


Figure 3-2-13. Simulation results of I_d-V_g for PMOS.



In D = 12 μm case
$N_t = 1 \times 10^{17}$ $cm^{-3}eV^{-1}$
$\alpha = 1.46 \times 10^{-15}$ Vs

In D = 0.5 μm case
$N_t = 1 \times 10^{17}$ $cm^{-3}eV^{-1}$
$\alpha = 1.46 \times 10^{-14}$ Vs

Figure 3-2-14. Simulation results of 1/*f* noise for PMOS.

Figure 3-2-9 shows $I_d - V_d$ curves for CMOS when the distance is 12 and 0.5 μm. In NMOS, from 5 % to 10 % decreases of I_{dr}, and in PMOS, from 5 % to 10 % increases of I_{dr} were observed. This I_{dr} changes are caused by compressive stress. Figure 3-2-10 shows the cumulative probability of the noise. In the case of NMOS, there is little difference in the noise and dispersion in all samples, while in the case of PMOS, while 1/*f* noise for PMOS was degraded as D is 0.5 μm. Figure 3-2-11 shows V_{th} dependence of flicker noise of CMOS with various areal density of nitrogen. In both NMOS and PMOS, the noise depends on V_{th} value significantly. In NO gas annealing case, larger V_{th} change than plasma nitridation due to electron traps is observed. These results indicate that density of trap site in NO gas annealing case is larger than plasma nitridation case. Figure 3-2-12 shows V_{th} for PMOS when the distance between gate and STI edge is 12 and 0.5 μm. V_{th} value does not change changed even when the STI edge is closer to gate electrode. This result shows the noise degradation in STI stress is caused not by trap density but by mobility fluctuation. DC characteristics calibration was carried out in order to simulate flicker noise. Figure 3-2-13 shows $I_d - V_g$ results. Both actual and simulation result are plotted in this figure. The results of DC characteristics fitting are good for flicker noise.

Figure 3-2-14 shows simulation results of flicker noise when the distance is 12 and 0.5 μm. The simulation results agree with actual measurement results. I found that the mobility fluctuation was 10 times larger when the STI edge is closer to gate electrode in PMOS by these fitting.

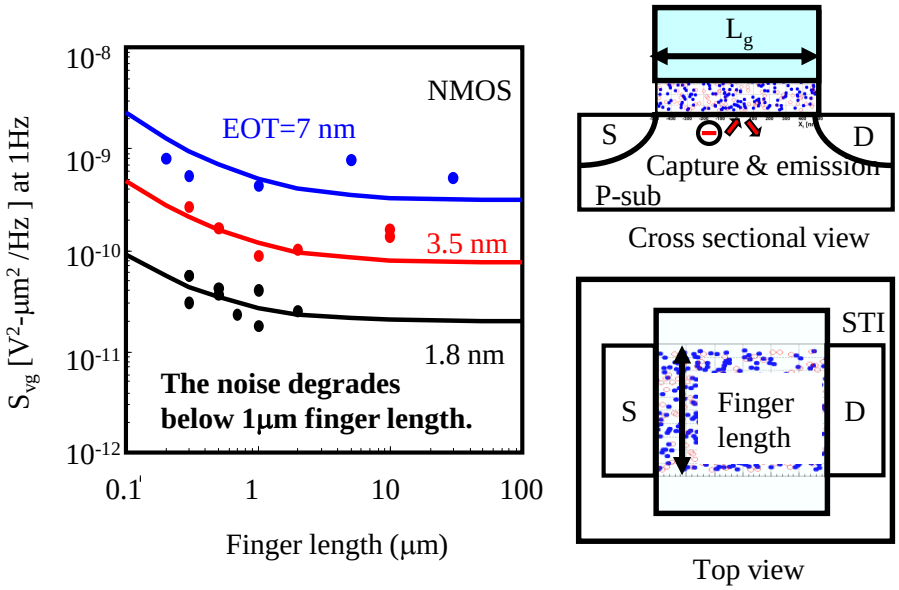


Figure 3-2-15. Gate width dependence of flicker noise for NMOS with various gate oxide thickness.

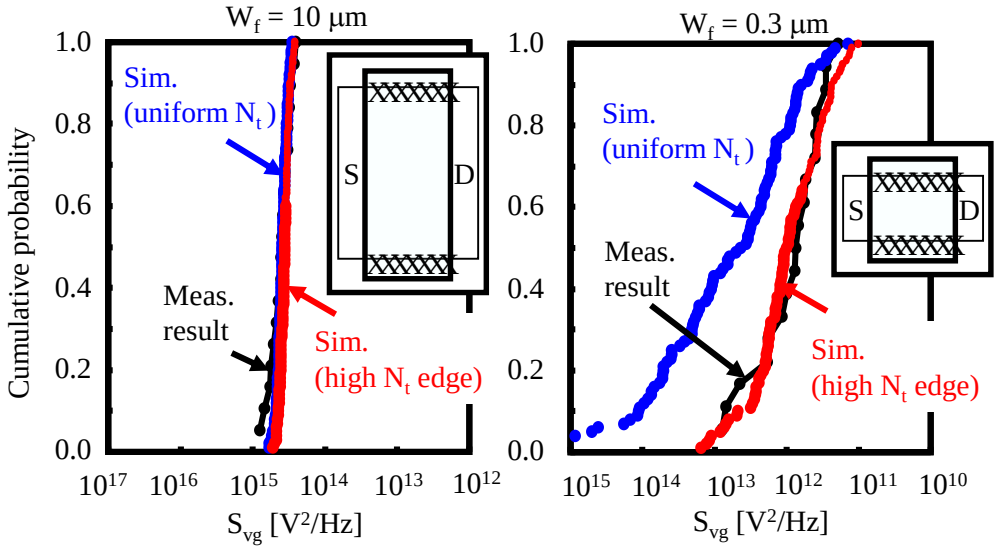


Figure 3-2-16. Simulation results of flicker noise of NMOS in Higher and lower trap density at STI edge [34].

Figure 3-2-15 shows gate width dependence of flicker noise for NMOS. The noise increases due to higher trap density at STI edge when gate width is below 1 μm in all gate oxide thickness cases. Those results shows the region within 0.5 μm from STI edge degrades flicker noise [30-33]. Dr. Higashi et al,. carried out simulation of gate width dependence of flicker noise [34]. Figure 3-2-16 shows the simulation results of flicker noise of NMOS in higher and lower trap density at STI edge. Cumulative probability of measurement data are also plotted in W_g = 10 μm and 0.3 μm. In W_g = 10 μm case, the probability in higher trap site case is same as that in uniform trap site. The result in higher trap site case is good agreement with measurement data when W_g = 0.3 μm [34].

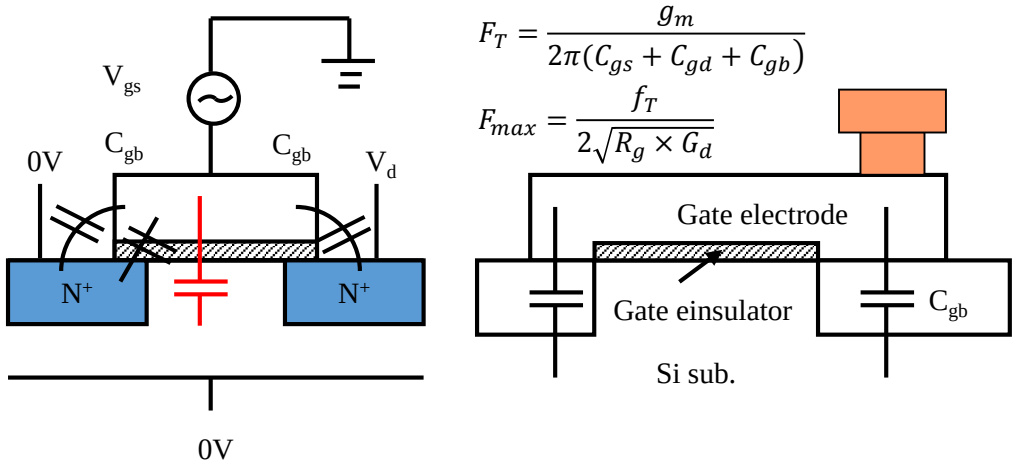


Figure 3-2-17. The formula to calculate f_T and f_{MAX}.

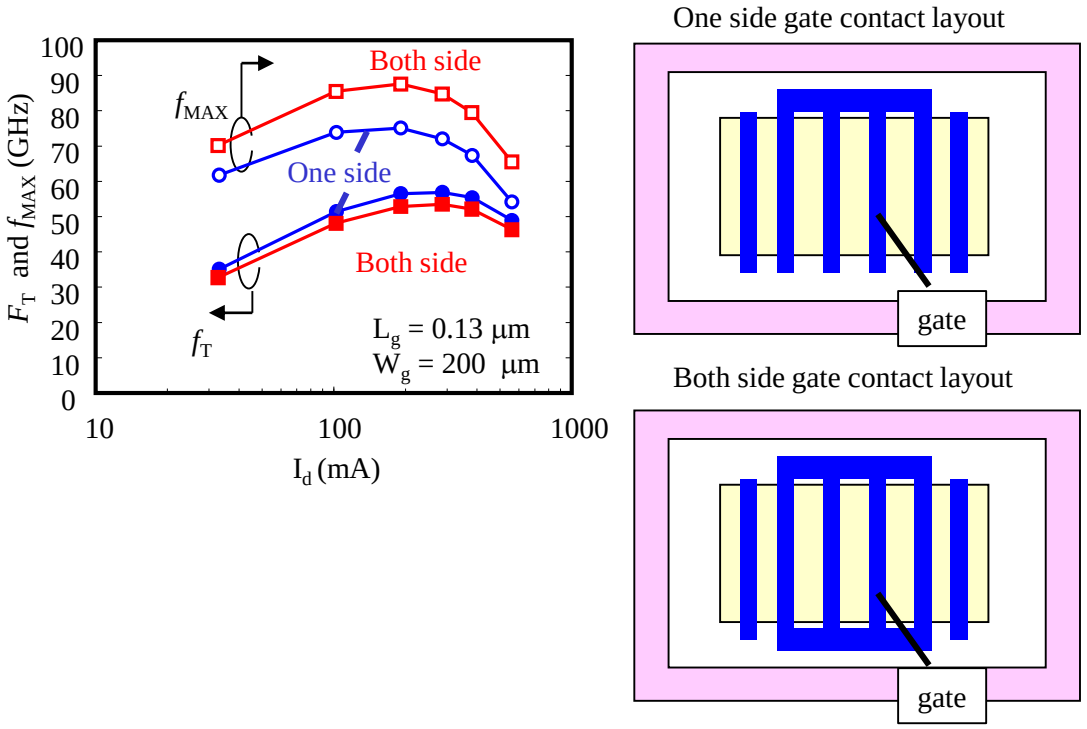


Figure 3-2-18. Drain current dependence of f_T and f_{MAX} for one side gate contact and both side gate contact.

Figure 3-2-17 shows the formula to calculate f_T and f_{MAX}. The f_T is determined by ratio of transconductance (g_m) and gate capacitance involving not only C_{gs} and C_{gd} but also C_{gb}. The C_{gb} is the capacitance between gate electrode and Si substrate at gate contact region. Fmax is determined by f_T, gate resistance and drain conductance. Figure 3-2-18 shows drain current dependence of f_T and f_{MAX} for one side gate contact and both side gate contact. F_T in both side contact case is smaller than that of one side contact case because of larger C_{gb} while f_{MAX} is larger because of smaller gate resistance.

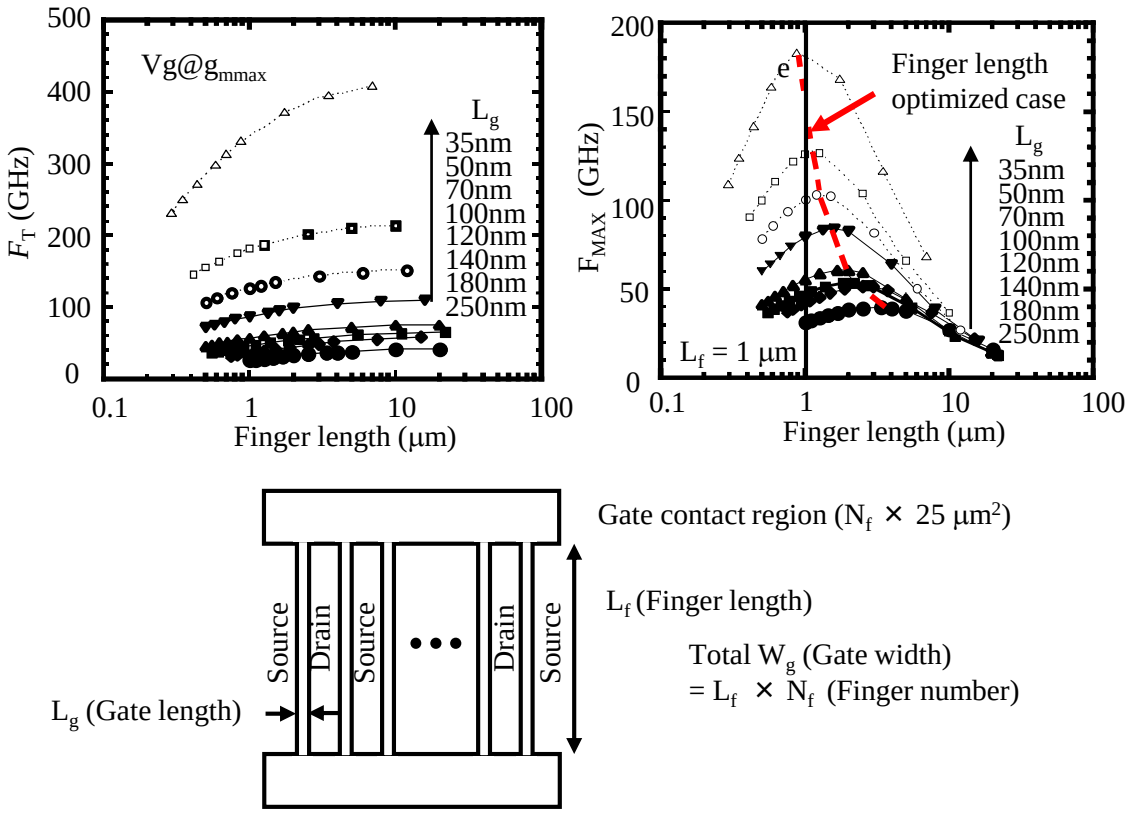


Fig.3-2-19. Finger length dependence of f_T and f_{MAX} for NMOS which the gate sheet resistance is 10 ohm/sq.[35].

Dr. Morifuji estimated the finger length dependence of f_T and f_{MAX} for NMOS by simulation [35]. Figure 3-2-19 shows the results of finger length dependence of f_T and f_{MAX} for NMOS. Gate contact region increases with shorter finger length because total W_g is fixed to 200 μm. As the finger length decreases, f_T value also decreases because of increases of C_{gd}. In the case of f_{MAX}, peak value appears because gate resistance decreases as the finger length decreases. According to our estimation, the optimum finger length is beyond 1μm till gate length is 50 nm. However, the length is 0.7 μm when the gate length is 35 nm. Thus it is required to reduce gate resistance from 10 ohm/sq. to 7 ohm/sq. in order to suppress the degradation of f_{MAX} when the finger length is 1.0 μm.

Conclusion

When using NO gas annealing to form oxynitride as gate insulator, MOS with buried channel is useful In order to reduce 1/*f* noise. Because carrier path is away from the interface between oxynitride and Si substrate and trap probability decreases. This structure is actually used for CMOS image sensor for the reduction of the noise.

1/*f* noise in PMOS is sensitive to 1) oxynitride formation process of gate insulator, 2) deuterium annealing after metal formation and 3) STI stress comparing with NMOS. Simulation results of 1/*f* noise show the degradation of 1/f noise due to STI stress is caused by not increasing trap density but mainly increasing mobility fluctuation. In order to reduce 1/*f* noise, it is important that plasma nitridation process is introduced and the distance between gate and STI edge is beyond 0.5 μm. Moreover, the finger length should be below 1 μm.

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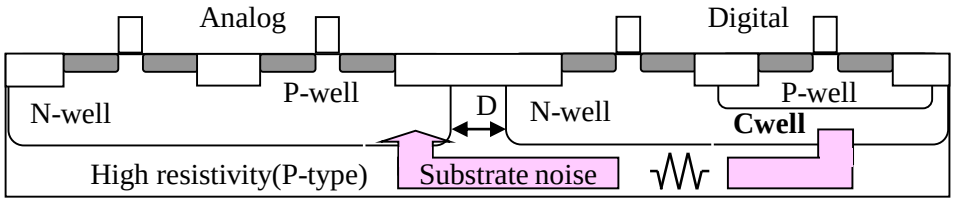
Chapter 4
Si substrate engineering for high performance of mixed-signal and RF characteristics

4-1. High resistivity substrate for high performance RF CMOS



Higher input impedance is needed in order to reduce substrate noise.

$Z = Rsub + 1/jwC$

Lower capacitance
(Triple well, high resistivity substrate)

High resistivity substrate

Figure 4-1-1. Requirement for Suppression of substrate noise.

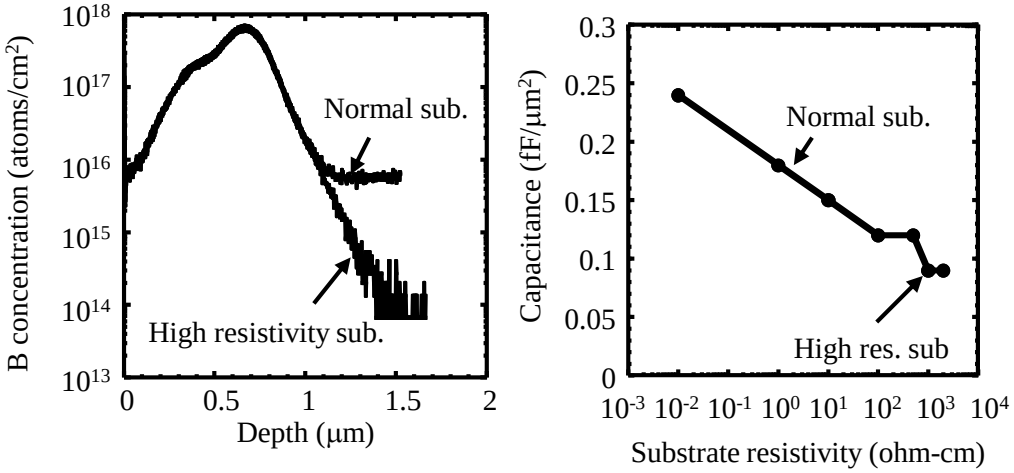


Figure 4-1-2. Si substrate resistivity dependence of junction capacitance between Nwell and P substrate.

High resistivity Si substrate is attractive for RF circuits because Q value of inductor becomes higher because eddy current flowing in the Si substrate can be reduced. Additionally, I expect the suppression of substrate noise which passes trough Si substrate between digital and RF circuits because of higher impedance even when operation frequency is higher. The purpose to introduce high Si resistivity is that higher performance RF circuits and digital circuits on the same Si substrate.

Figure 4-1-1 shows the impedance from digital to analog circuits which consists of resistance and capacitance. The higher impedance can reduce substrate noise from digital to analog circuits. As the clock frequency increases, imaginary part of the impedance decreases but real part is constant. In order to keep higher impedance at higher clock frequency, higher Si substrate resistivity is required. And the lower capacitance is also useful to realize higher impedance.

Figure 4-1-2 shows the boron profile in Nwell for normal and high resistivity substrate. The concentration 2 order lower compared with normal one. Right hand figure shows dependence of capacitance between nwell and Si substrate on the resistivity. As the resistuvity increases, the capacitance becomes lower because boron concentration decreases. The junction capacitance between Nwell and Psub with 1000 (1k) ohm-cm is half of that normal one [7,21].

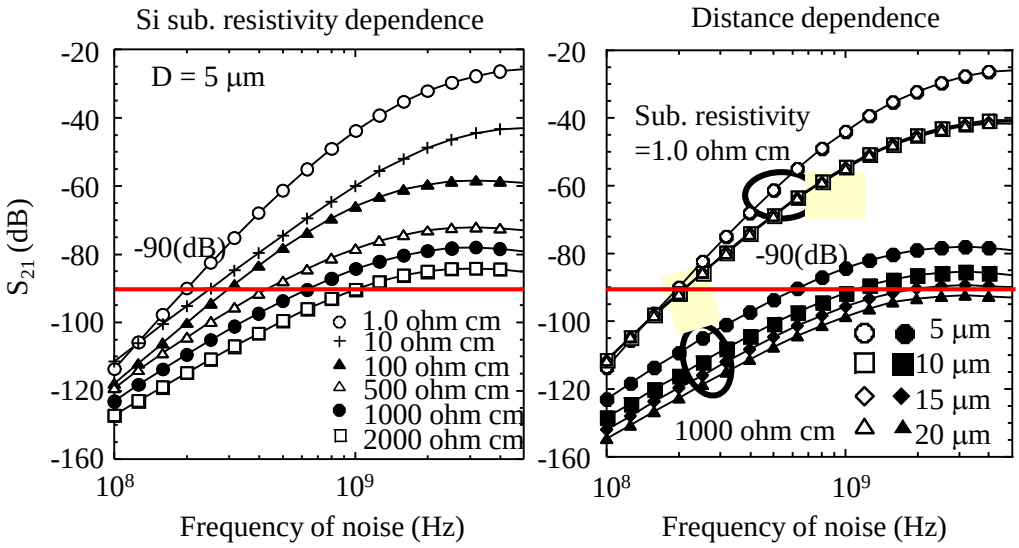


Figure 4-1-3. Dependence of substrate noise on the frequency for various substrate resistivity (Simulation).

Table 4-1-1. Design of substrate resistivity and analog - digital distance for realization of -90 dB S_{21}.

Frequency of noise (Hz)	Sub. resistivity (Ohm-cm)	Distance (Analog-digital)
200M	1.0	5 μm
300M	10	5 μm
500M	500	5 μm
750M	1000	5 μm
1G	1000	10 μm
	2000	5 μm

I carried out simulation of the substrate noise under consideration resistivity of Si substrate and capacitance between Nwell and Si substrate as shown in Fig. 4-1-3. Left hand figure shows dependence of the noise on the frequency for various substrate resistivity when distance between analog and digital is 5 μm. As the resistivity becomes higher, the noise decreases significantly. Additionally, as the distance (D) between analog and digital circuits becomes larger, the noise has significantly decreased in 1 k ohm-cm case, while no improvement was observed in 1.0 ohm-cm case as shown in right hand figure. I considered the design in order to realize penetration noise of –90 dB for various frequency.

Table 4-1-1 shows design of substrate resistivity and distance between analog and digital circuits. When the frequency is below 300 MHz, normal Si substrate with around 10 ohm cm can suppress the noise penetration. But, when the frequency is beyond 500 MHz, Si substrate with beyond 500 ohm are needed. In the case of 1kohm-cm, the noise can be suppressed by using wider distance such as 10 μm even when 1 GHz.

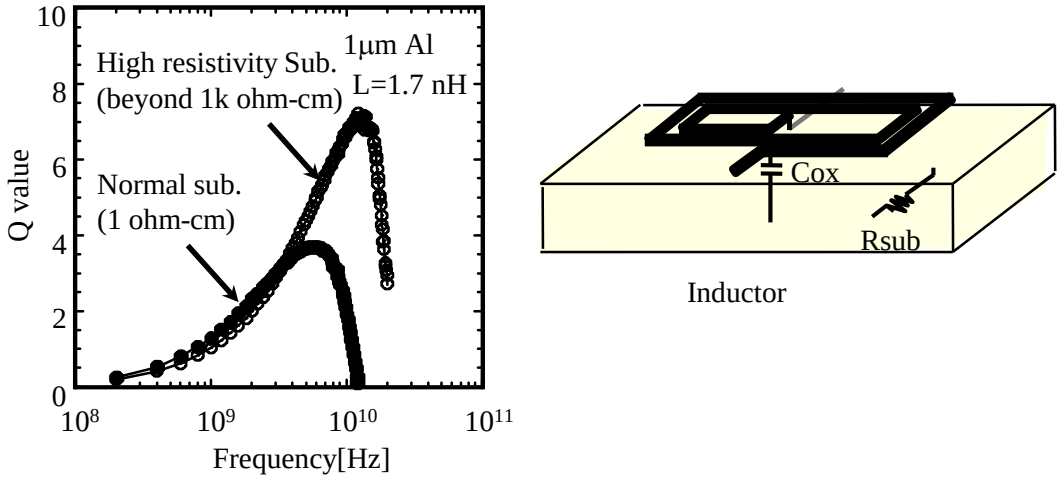


Figure 4-1-4 Frequency dependence of Q value on Si substrate with 1ohmcm and beyond 1 k ohm-cm

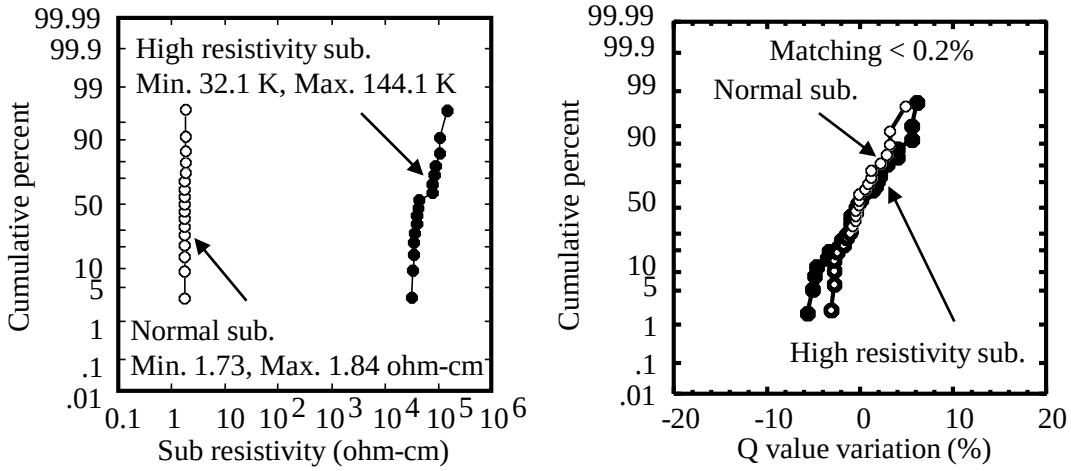


Figure 4-1-5. Variation of substrate resistance and Q-value.

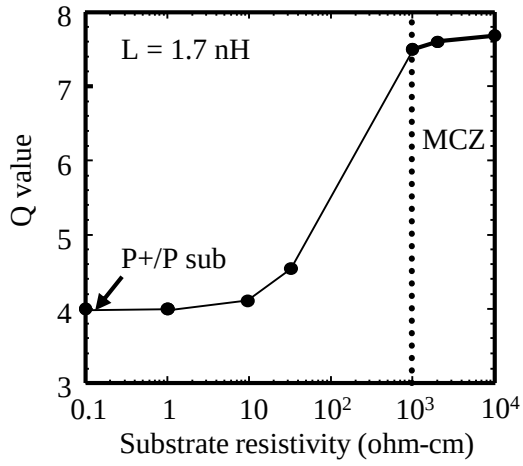
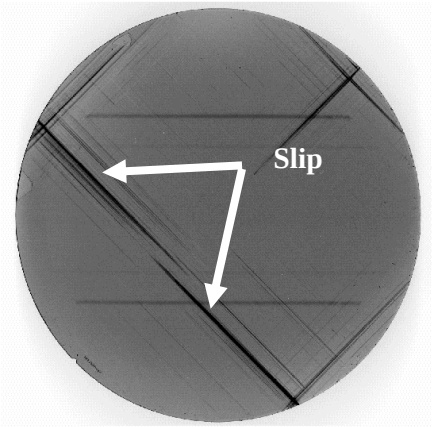


Figure 4-1-6. Dependence of Q value on substrate resistivity.

a) Slip generation



b) Higher leakage current between Nwells

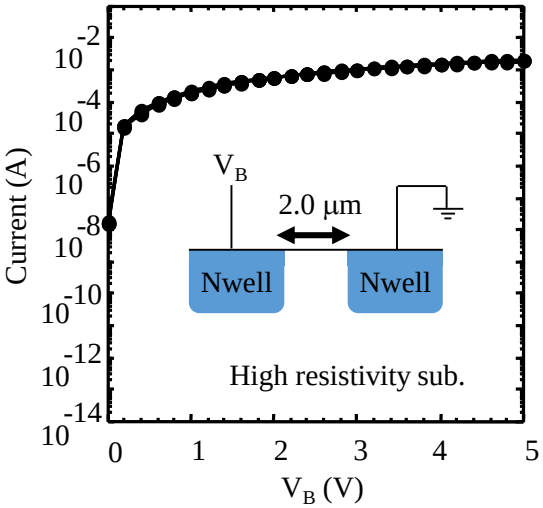


Fig.4-1-7. Problems of high resistivity substrate.

Figure 4-1-4 shows dependence of inductor Q value on operation frequency for 1 k ohm-cm and 1 ohm-cm Si substrate. The value in high resistivity substrate becomes 2 times higher that of 1 ohm cm. This result shows high resistivity Si substrate is effective for reducing the substrate loss during high frequency operation for passive elements. A lot of papers shows the resistivity is attractive for RF circuits [1-20].

Figure 4-1-5 shows variation of substrate resistance and Q value. In the case of MCZ with high resistivity, resistance variation is large such as from 32.1K to 144.1 k ohm-cm. On the other hand, the variation is small in the normal substrate. However, variation of Q value is almost same in both substrate. Matching of Q value is within 0.2 % in both cases.

Figure 4-1-6 shows dependence of Q value on substrate resistivity. When the value is below 10 ohm-cm or beyond 1 k ohm-cm, the value is almost same. Thus, the Q variation is small in our MCZ with high resistivity. These results show high resistivity substrate with at least 1 k ohm-cm is needed for both the suppression of noise penetration and Q value improvement of inductor. The high resistivity Si substrate is attractive for RF circuits but has some serious problems. Figure 4-1-7 shows problem of high resistivity substrate. One is slip generation, the other is higher leakage current between Nwells. Of course, nobody uses the substrate without solving these problems [7,15].

4-1-1. Sample fabrication to suppress slip in Si substrate with high resistivity

Fully oxygen precipitated Wafer with high resistivity (FOP)

STI formation

Additional well ion implantation (Boron)

Well and channel formation

Thermal annealing

Gate electrode(L_{min} = 0.11 μm) & resistor formation

Source and drain formation

Metallization

Figure 4-1-8. Process flow of CMOS on high resistivity substrate.

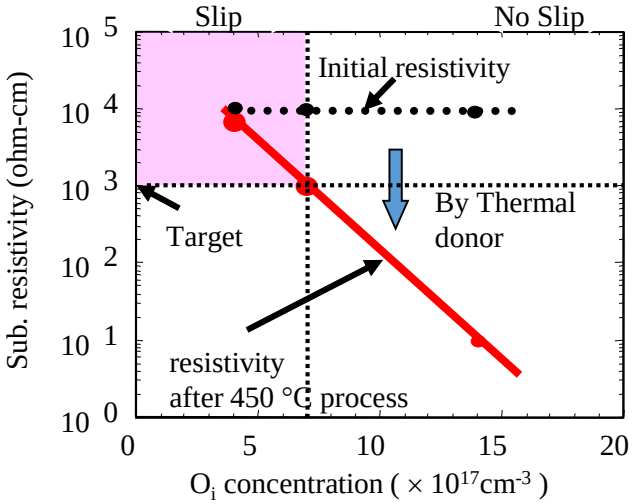


Figure 4-1-9. Relationship between residual oxygen O_i and the substrate resistivity.

Figure 4-1-8 shows process flow in our experiments. The fully oxygen precipitated wafer was used in order to suppress slip generation. After STI process, additional well ion implantation was carried out with high acceleration energy in order to suppress leakage current between adjacent Nwells. At this stage, no implantation was done in inductor, resistor and ESD region by using additional mask. After channel implantation, thermal annealing was carried out to remove any defects. Then, after poly Si deposition, patterning was carried out for not only gate electrode but also poly resistor. Minimum gate length was 0.11 μm. After source and drain formation, Co salicide was applied to reduce gate, source and drain resistance.

Figure 4-1-9 shows relationship between residual oxygen O_i and the substrate resistivity. The O_i control is very important for realizing high resistyvity. In an initial condition, high resistivity can be easily realized by reducing impurity concentration which does not depend on O_i. However, after 450 °C annealing, the value decreases significantly as the O_i increases due to thermal donor. For example, the value in 1.4×10^{18} cm^{-3} case decreased 3 order lower after the annealing. In order to keep 1000 (1k) ohm cm, O_i below $7 \times 10^{17} cm^{-3}$ is necessary. On the other hand, unfortunately, the substrate with O_i below 7×10^{17} cm^{-3} generates slip during high temperature process such as STI formation. So the relationship between high resistivity and slip generation is trade-off.

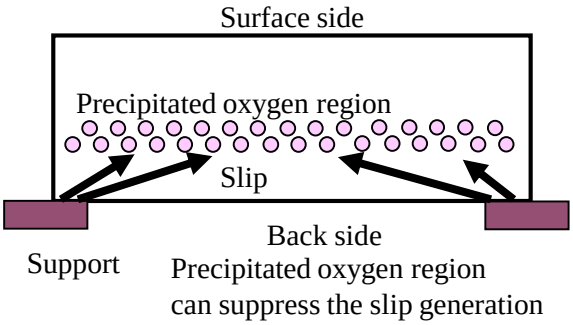


Figure 4-1-10. Suppression of slip generation in higher resistivity substrate.

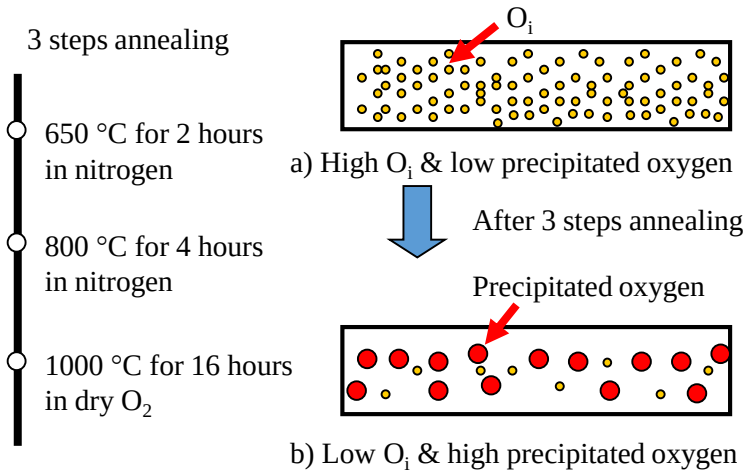


Figure 4-1-11. Process flow for Fully oxygen precipitated wafer with high resistivity (FOP) .

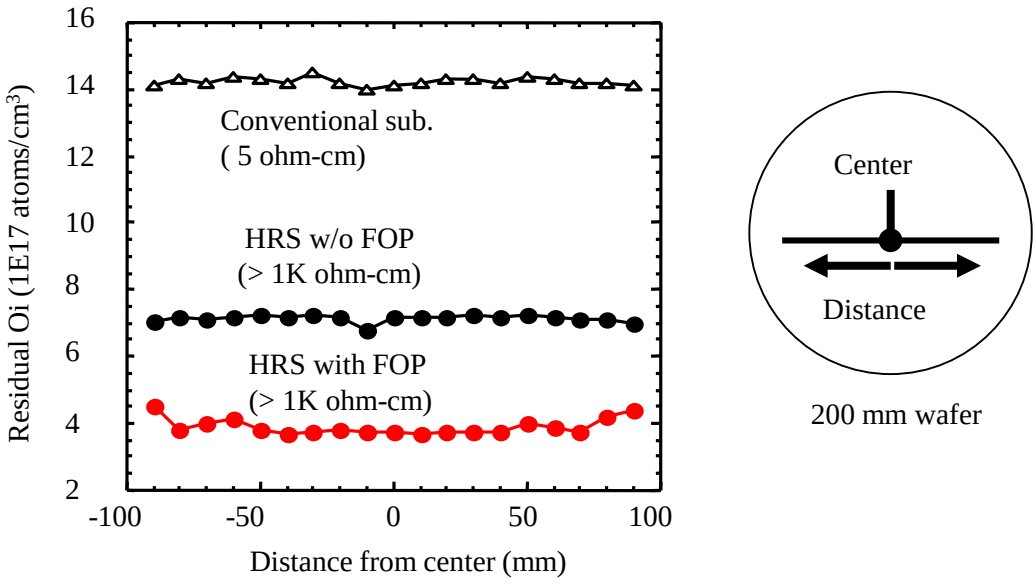
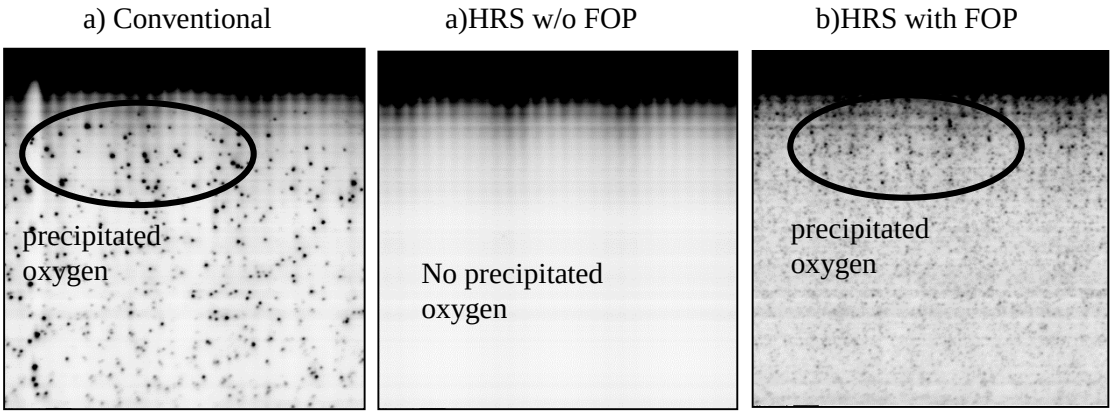


Figure 4-1-12. Distribution of residual O_i concentration on the wafer.

The slip generates from back-side of wafer during thermal process because substrate region contacted with support parts in annealing machine bring the slip due to any stress as shown in Fig. 4-1-10. It is well-known that precipitated oxygen can suppress the slip generation. And no resistivity increase occurs after 450 °C process because the precipitated oxygen does not work as thermal donor. I use fully oxygen precipitated wafer with high resistivity.

The wafers were cut from the crystals annealed by three steps as shown in Fig. 4-1-11. First is 650 °C annealing for 2 hours in nitrogen gas. Second is 800 °C annealing for 4 hours in nitrogen gas. And final is 1000 °C annealing for 16 hours in dry oxygen. The long time is for obtaining saturated oxygen precipitation. After 3 step annealing, residual oxygen O_i increased while fully oxygen were precipitated.

The wafers were cut from the crystals annealed by three steps as shown in Fig. 4-1-11. First is 650 °C annealing for 2hours in nitrogen gas. Second is 800 °C annealing for 4 hours in nitrogen gas. And final is 1000C annealing for 16 hours in dry oxygen. The long time is for obtaining saturated oxygen precipitation. After 3 step annealing, residual oxygen O_i increased while fully oxygen were precipitated.



By 3 steps annealing process, precipitated oxygen was observed in high resistivity substrate.

Figure 4-1-13. Cross-sectional view of various wafers.

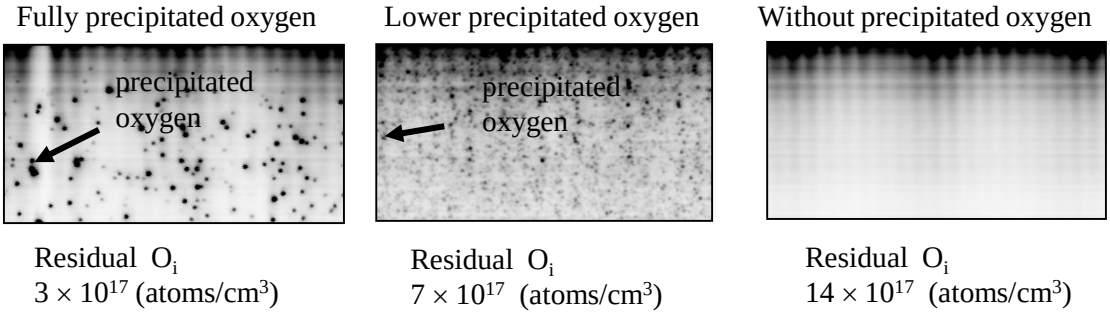
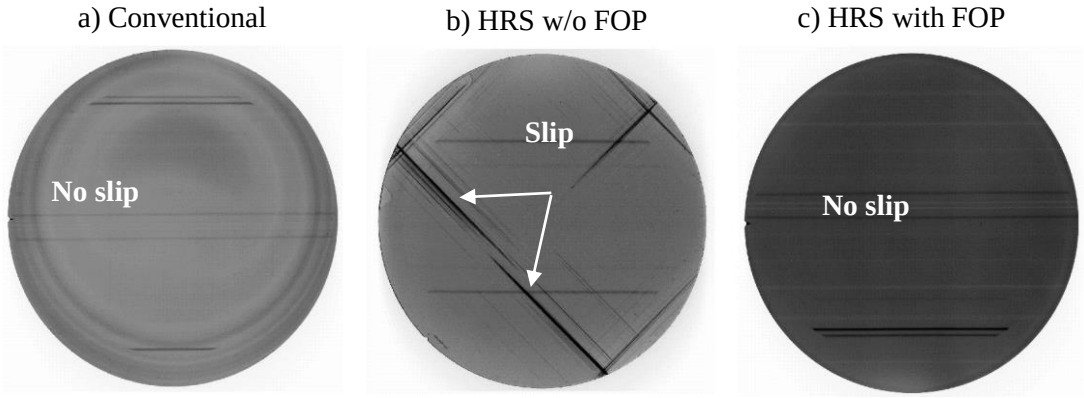


Figure 4-1-14. Residual oxygen in high resistivity substrate.



Precipitated oxygen suppress the slip generation

Figure 4-1-15. X-ray analysis of various wafers.

Figure 4-1-14 shows cross sectional view of 3 kinds of wafers. One is conventional wafer with 5 ohm-cm, The others are high resistivity substrate with and without 3 steps annealing. As you can see, 3 steps annealing substrate has precipitated oxygen. Figure 4-1-15 shows X-ray analysis to observe slip in any wafers after STI process. No slip was observed in fully oxygen precipitated wafer with high resistivity. This results show fully oxygen precipitated wafer suppresses the slip generation and keeps high resistivity.

4-1-2. Electrical characteristics

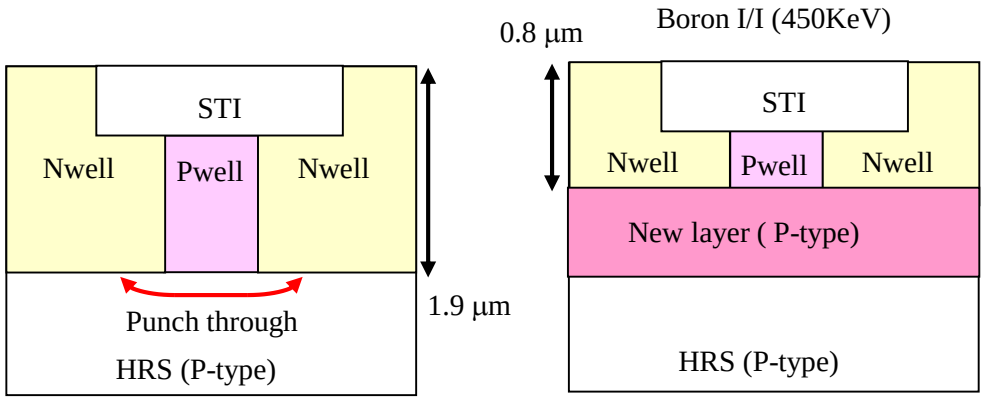


Figure 4-1-16. Schematic cross sectional view for suppression of Nwell-Nwell leakage current.

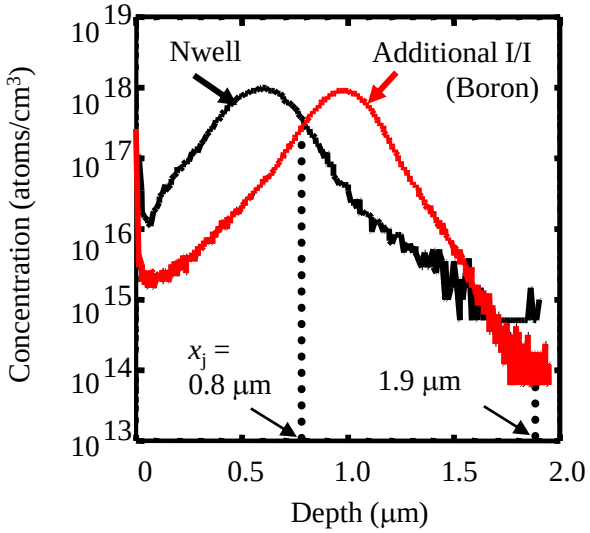


Figure 4-1-17. SIMS profile of Nwell and additional Boron.

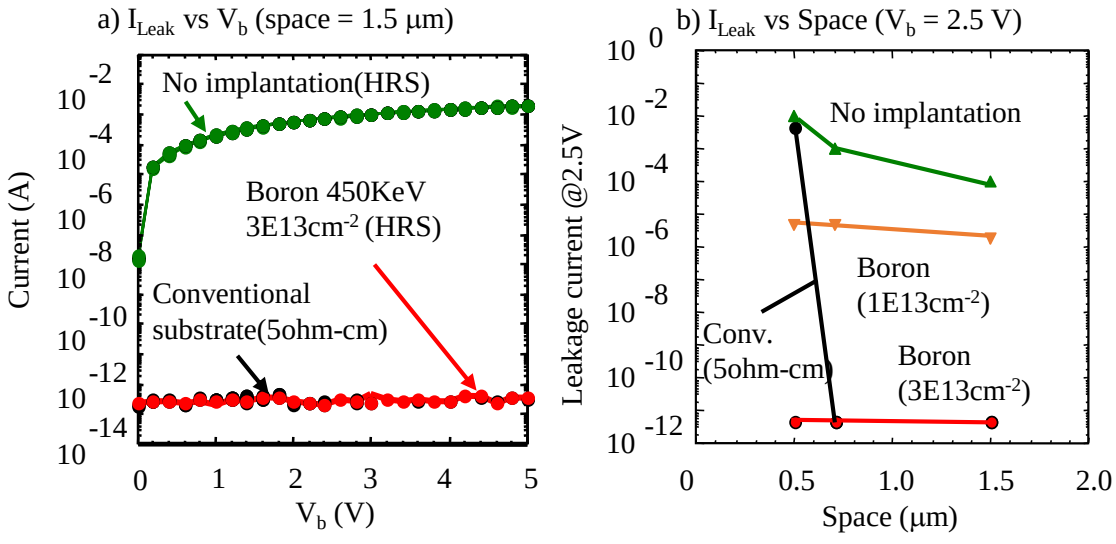


Figure 4-1-18. Leakage current between Nwells.

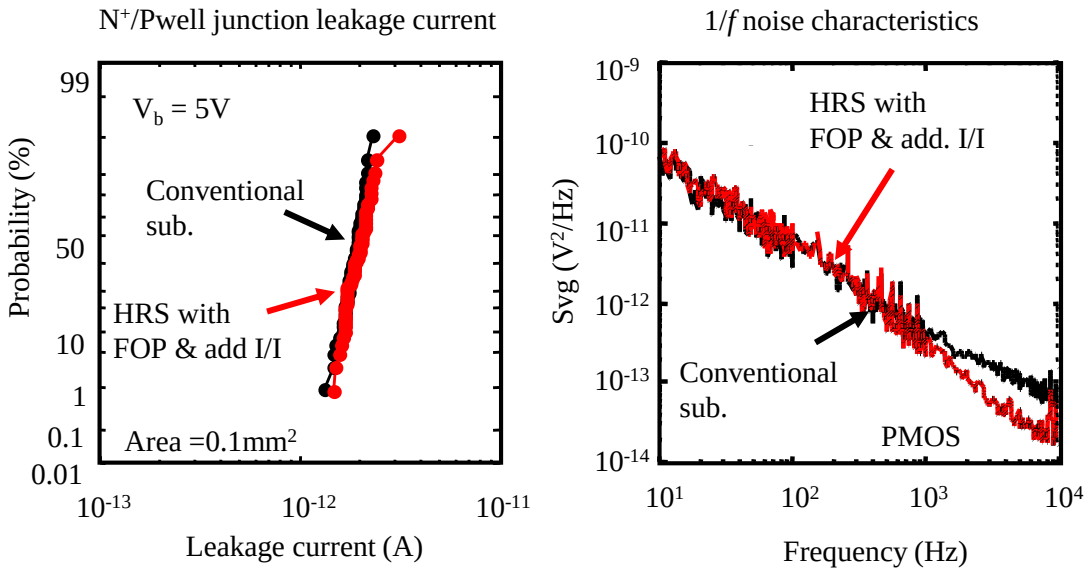


Figure 4-1-19 N⁺/Pwell junction leakage current and 1/*f* noise characteristics

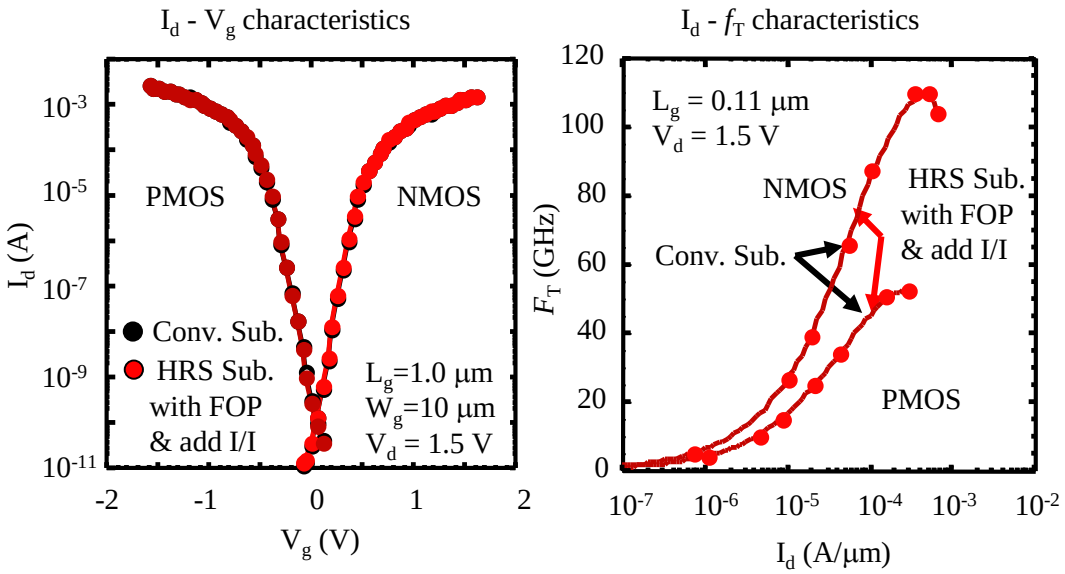


Figure 4-1-20. DC and RF characteristics with and without additional Boron implantation.

Figure 4-1-16 shows schematic cross sectional view after formation Nwell. The junction depth was 1.9 μm in HRS case because the substrate concentration was extremely lower such as 1E14 cm^{-3}, while that was 1.1 μm in conventional substrate due to higher concentration of 1E16 cm^{-3}. This deeper junction of Nwell brings the larger leakage current between the adjacent Nwells. So we made the junction become shallower by using additional Boron implantation as shown Fig. 4-1-17. Figure 4-1-17 shows SIMS profile of Nwell and additional implanted boron after thermal annealing. The boron implantation condition was 450 KeV acceleration energy and 3E13 cm^{-2} dosage. The junction depth of Nwell became shallower from 1.9 μm to 0.8 μm by the implantation. Left hand figure in Fig. 4-1-18 shows bias dependence of leakage current between Nwells with 1.5 μm space for conventional and high resistivity substrate. In high resistivity substrate without additional implantation case, larger leakage current was observed. However, the leakage current was suppressed by additional boron implantation, which was comparable with that of conventional substrate. Right hand figure is dependence of leakage current at 2.5 V on Nwells space. By using the additional implantation, the degradation of leakage current was suppressed to 0.5 μm space, which was greater than conventional substrate case. These results show no needed to change design rule of Nwell space even in high resistivity substrate case. This is important for mixed-signal and digital circuit design. N^+/Pwell junction leakage current which is sensitive to defect in wafer and 1/*f* noise which is sensitive to surface condition of wafer were observed in order to evaluate the quality of fully oxygen precipitated wafer. Difference between conventional and fully oxygen precipitated wafer was negligible regarding N^+/Pwell junction and 1/*f* noise characteristics as shown in Fig. 4-1-19. These results show the quality of fully oxygen precipitated wafer is no problem. I_d-V_g and I_d- f_T characteristics were measured in order to evaluate additional implantation affections.

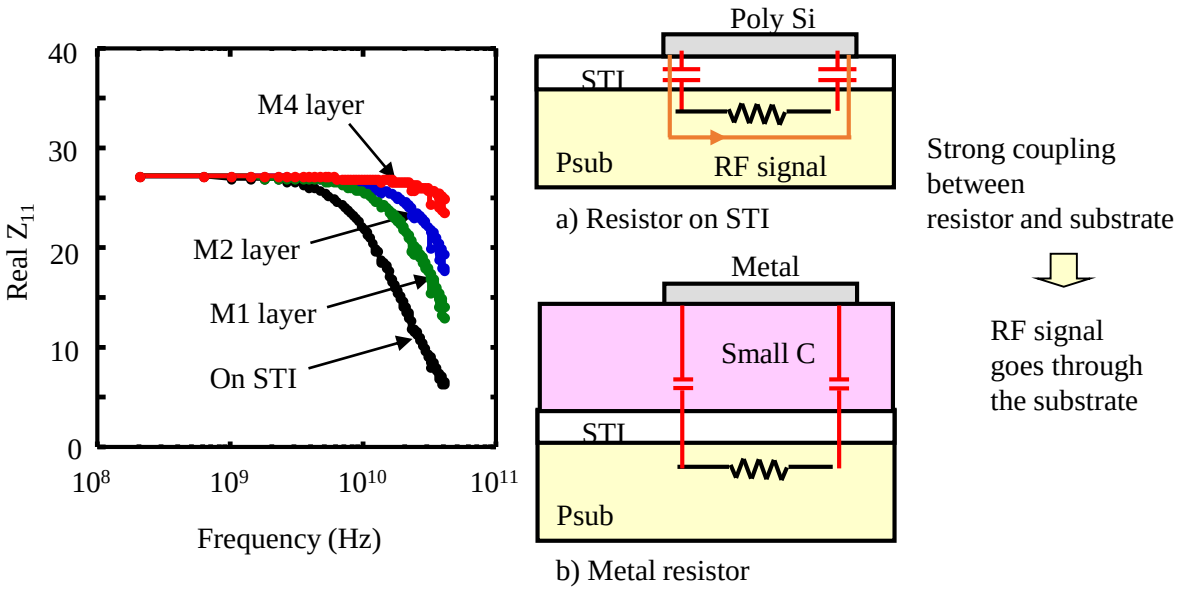


Figure 4-1-21. Dependence of RF signal on capacitance between resistor and Si substrate.

No difference of V_{th} and f_T were observed CMOS with and without the additional boron implantation as shown in Fig. 4-1-20. These results show the additional implantation does not influence over MOSFET characteristics. I describe not only solution for high resistivity substrate problems but also some additional merits.

Figure 4-1-21 shows the cross sectional view of resistor. In generally, on chip resistor has been formed on STI because poly Si is used as resistor which is also used as gate electrode. In this structure, resistor has strong coupling between resistor and substrate because resistor is close to substrate whose condition is difference from inductor and MIM capacitor. Thus, RF signal easily passes through not resistor but substrate, which is serious problem for RF circuits. In order to resolve this problem, lower capacitance between resistor and substrate and high resistivity substrate are effective. Figure 4-1-21a) shows parasitic capacitance dependence of RF signal. Vertical and horizontal axis shows Real Z_{11} and frequency of RF signal, respectively. The dropping of Real Z_{11} causes by flowing of RF signal in substrate. As the capacitance decreases, the dropping suppresses. In order to reduce parasitic capacitance, metal resistance is useful. However, the integration of metal resistor is not easy.

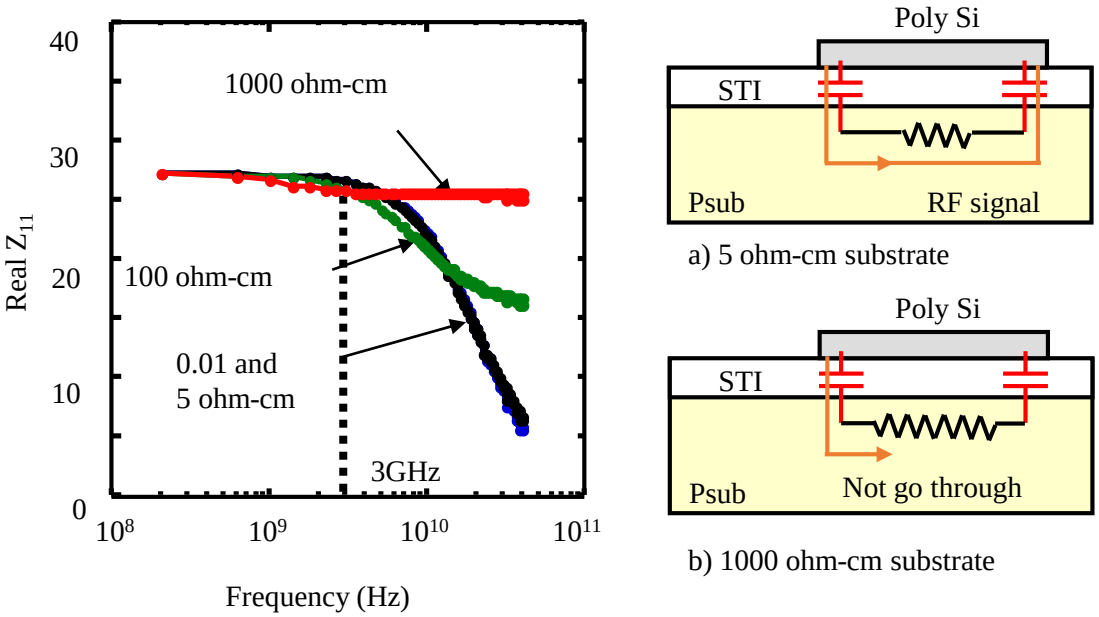


Figure 4-1-23. Substrate resistivity dependence of RF signal. High resistivity substrate is effective for beyond 3 GHz operation.

4-1-3) Substrate resistivity dependence of RF noise

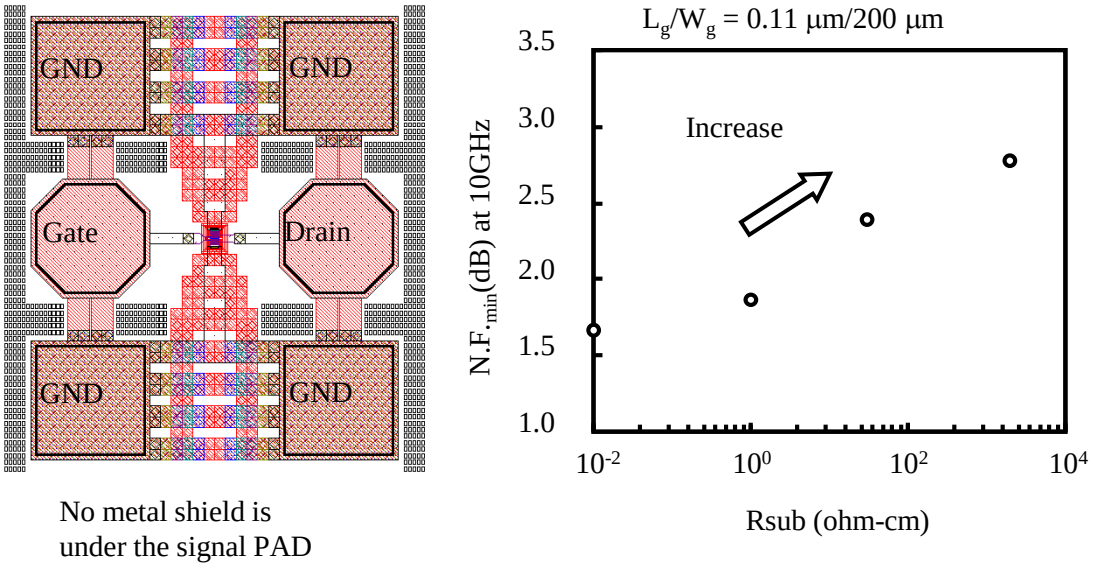


Figure 4-1-24. Si substrate resistivity dependence of noise figure.

4-1-3. Substrate resistivity dependence of RF noise

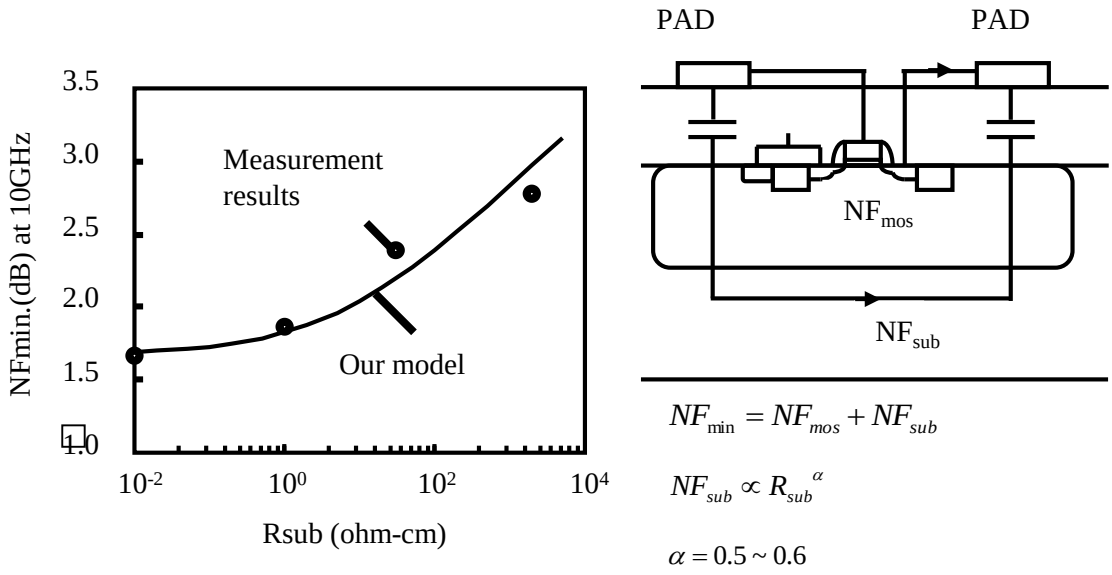


Figure 4-1-25. New model for Si substrate resistivity dependence of noise figure.

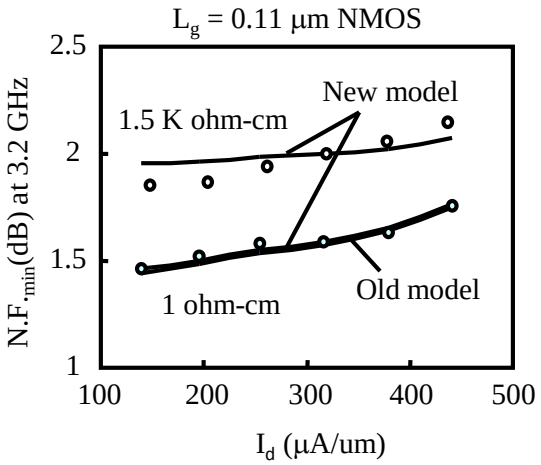


Figure 4-1-26. I_d dependence of RF Noise and fitting results with new model.

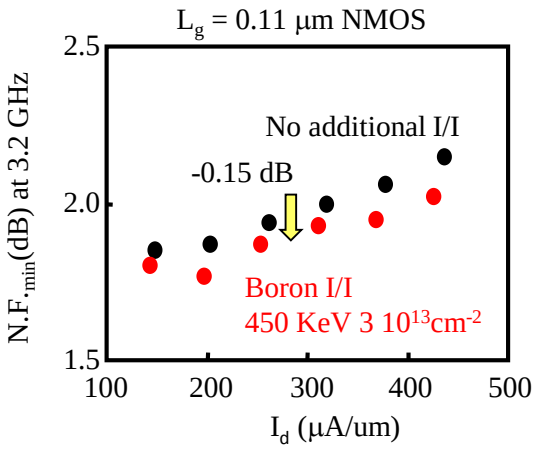


Figure 4-1-27. I_d dependence of RF Noise with and without boron additional implantation.

Figure 4-1-23 shows substrate resistivity of RF signal. When the frequency is below 3 GHz, the real Z_{11} is almost constant regardless of substrate resistivity. But, when the frequency is beyond 3 GHz, the real Z_{11} drops in the case of conventional wafer with 5 ohm-cm. As the resistivity increase, the dropping tends to be suppressed. And no dropping was observed in the 1000 ohm-cm substrate. So, high resistivity substrate is effective for resistor under beyond 3 GHz operation.

Figure 4-1--24 shows the noise figure minimum of 0.11 μm NMOS when no shield layer is under the signal PAD. As you can see, the NF_{min} increases with the Si substrate resistivity. Now we propose new and simple model for the Si substrate resistivity dependence of the noise. $N.F._{min}$ consists of two elements such as MOSFET and Si substrate part as shown in Fig. 4-1-25. And Substrate element of $N.F._{min.}$ is proportional to square root of Si substrate resistivity. The solid line in right hand figure is the results of our model based on the simple model. The model for the substrate resistivity dependence of the noise is almost in agreement with our measurement results. Figure 4-1-26 shows the drain current dependence of RF noise for 1 and 1.5 k ohm-cm resistivity, and fitting results with old and new model. White line is old one and red line are new one. This results shows the our new model is almost in agreement with our measurement results. Figure 4-1-27 shows the drain current of RF noise with and without 3×10^{13} cm^{-2} boron additional implantation in 1.5 k ohm-cm case. By using the additional implantation, 1.5 dB of the noise can be decreased. Metal shield layer under signal PAD and additional boron implantation have important roles in order to improve the RF noise in the high substrate resistivity case as shown in Fig. 4-1-28.

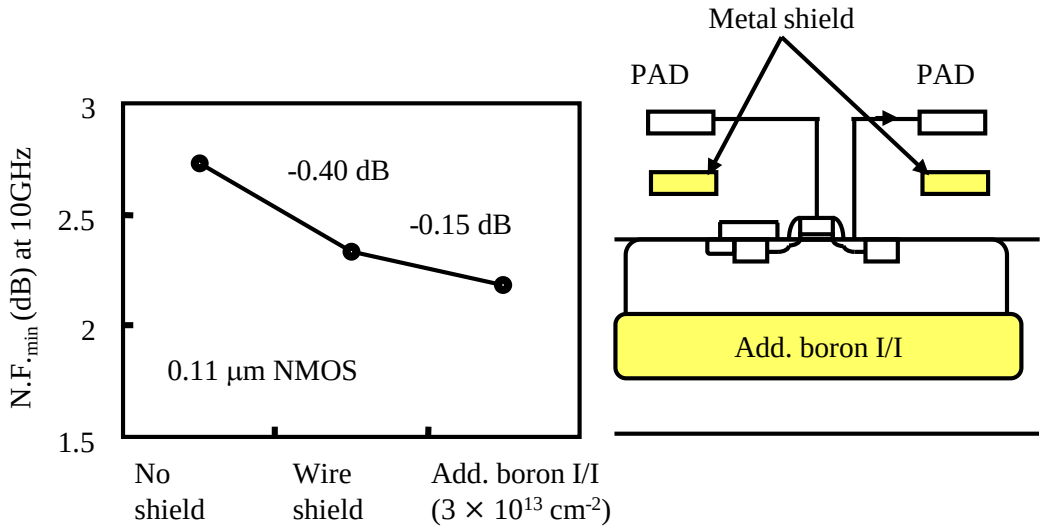


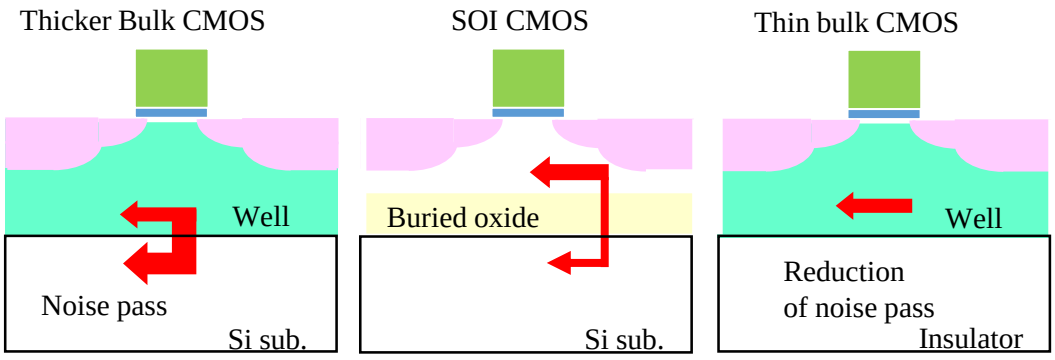
Figure 4-1-28 Layout and process dependence of RF Noise

Figure 4-1-28 shows the effect of metal shield under the signal PAD and the additional boron implantation for $N.F._{min}$ at 10 GHz. The value of 0.40 dB can be lowered by using shield layer under the signal PAD.

4-2. RF performance of CMOS on ultra-thin chip

Recently, 3D stacked research has been aggressive because 3D integration has been important in order to realize both high-density system in package (SIP) and high functionality with heterogeneous integration of materials, device, and signals. In order to realize high density 3D chip, not only TSV technology but also Si wafer thinning technology is required. The thinning of Si substrate is attractive for RF circuits because that causes lower substrate loss and lower noise figure [22,23]. The thin Si substrate thickness reported in some papers is 40 and 20um. RF characteristics in the ultra thin thickness such as 1.7um has been not known. Regarding to TSV technology, several papers propose how to make 3D stacked and point out stress issue or local bending [24-34]. We study and discuss DC, mixed-signal and RF characteristics through actual fabrication of CMOS on 1.7 μm Si substrate and the measurements.

4-2-1. Sample fabrication



Thicker Bulk CMOS	SOI CMOS	Thin bulk CMOS
1) Larger sub. noise 2) Lowest cost	1) Smaller sub. noise 2) Higher cost	1) Smaller sub. noise 2) Lower cost than Si on nothing substrate

Figure 4-2-1. The purpose to examine ultra-thin chip.

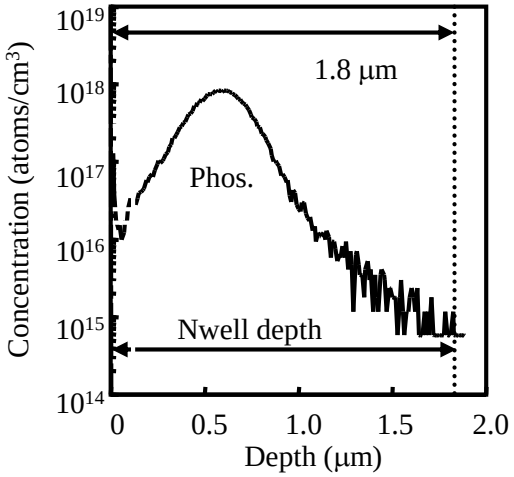


Figure 4-2-2. SIMS profile of phosphorus in Nwell.

The reduction of substrate noise is important for mixed chip of digital and analog circuits. In the case of thicker bulk Si substrate, the noise passes through well and Si substrate. On the other hand, the noise can be reduced by using SOI substrate, because there is buried oxide between well and Si substrate. However, SOI substrate is expensive comparing with bulk Si substrate. When Si substrate thickness is comparable with well layer, the noise can be reduced as well as SOI case because of reduction of noise pass as shown in Fig. 4-2-1.

Figure 4-2-2 shows SIMS profile of phosphorus in Nwell. The target of Si substrate thickness is below 1.8um because the junction depth was 1.3 μm according to SIMS profile. Figure 4-2-3 shows process flow of our samples. In this experiment, 1 ohmcm Si substrate was used. After STI process, well and channel implantation were carried out, 2.5 nm gate oxynitride was formed. Co salicide process was applied to reduce parasitic resistance after gate electrode, source and drain formation. The minimum gate length was 0.11 μm in this experiment. Inductor was formed by stacked metal of M3 and no well formation was carried out under the inductor.

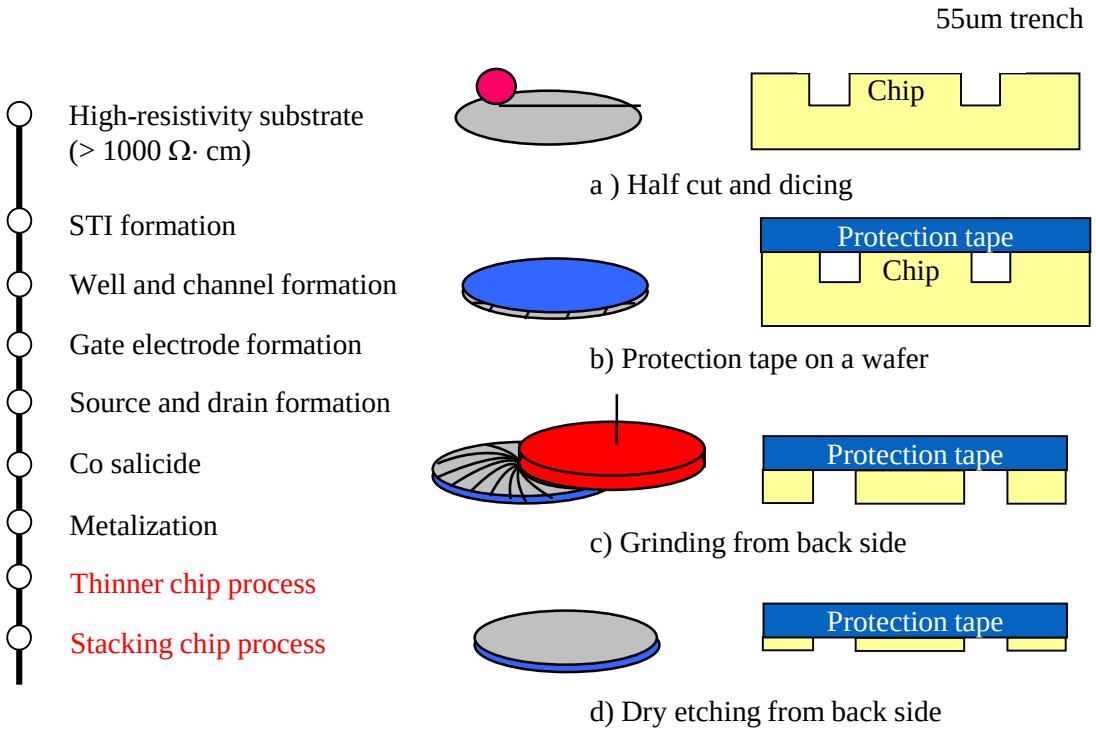


Figure 4-2-3. Process Flow of ultra thin chip fabrication.

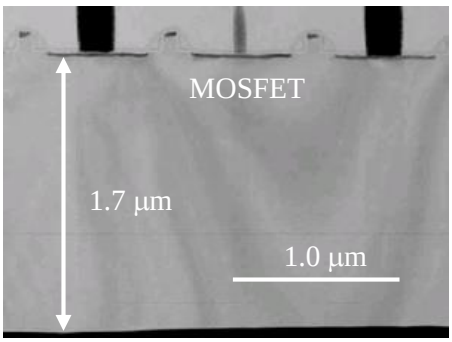


Figure 4-2-4. TEM photograph of ultra-thin chip. The thickness is comparable with Nwell depth.

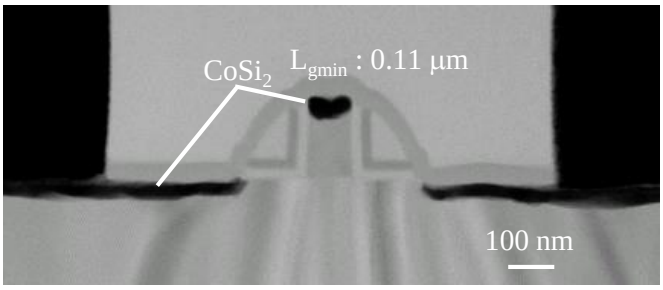


Figure 4-2-5. TEM photograph of ultra-thin chip. Gate length is 0.11 μm and $CoSi_2$ is formed.

Si thinner process are show in Fig. 4-2-3. After fabrication of MOSFET, thinner chip process and stacked chip process were carried out. After fabrication of MOSFET on a wafer, 55 μm trench was formed by pre-dicing process in order to prevent a wafer breaking during grinding. After setting protection tape on a wafer from front side, Si substrate was thinned by grinding and dry etching. The dry etching can not only make a Si substrate thin but also remove any damage layers due to grinding process. After the thin chip was cut, that was stacked on another chip which has metal wire. And the protection tape was peeled from the chip. Figure 4-2-4 shows a TEM photograph of ultra-thin chip. As you can see, small MOSFET was found. It was confirmed that Si substrate thickness was 1.7 μm. This thickness was comparable with Nwell depth which was almost our target.

4-2-2. Mixed signal and RF characteristics

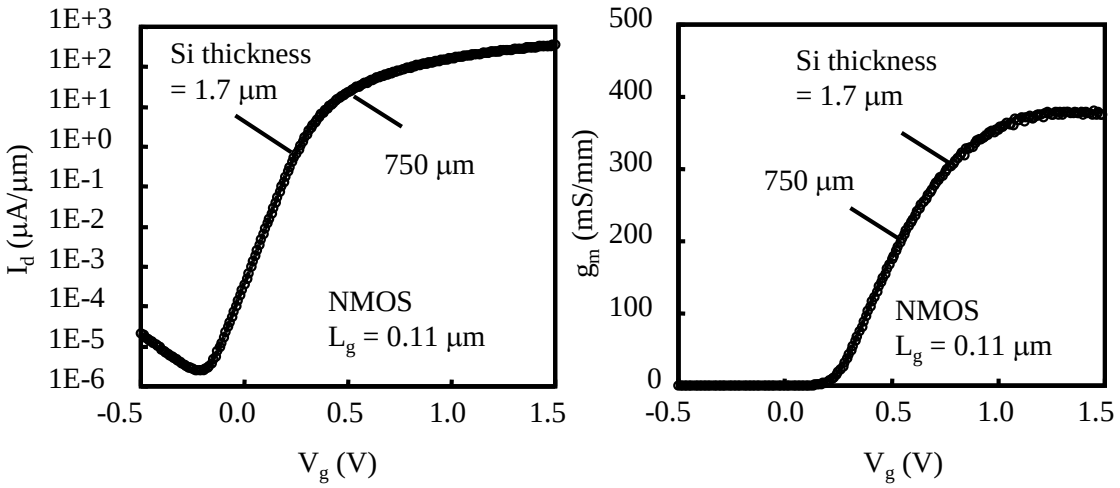


Figure 4-2-6. I_d-V_g and g_m-V_g characteristics of NMOS on ultra-thin chip.

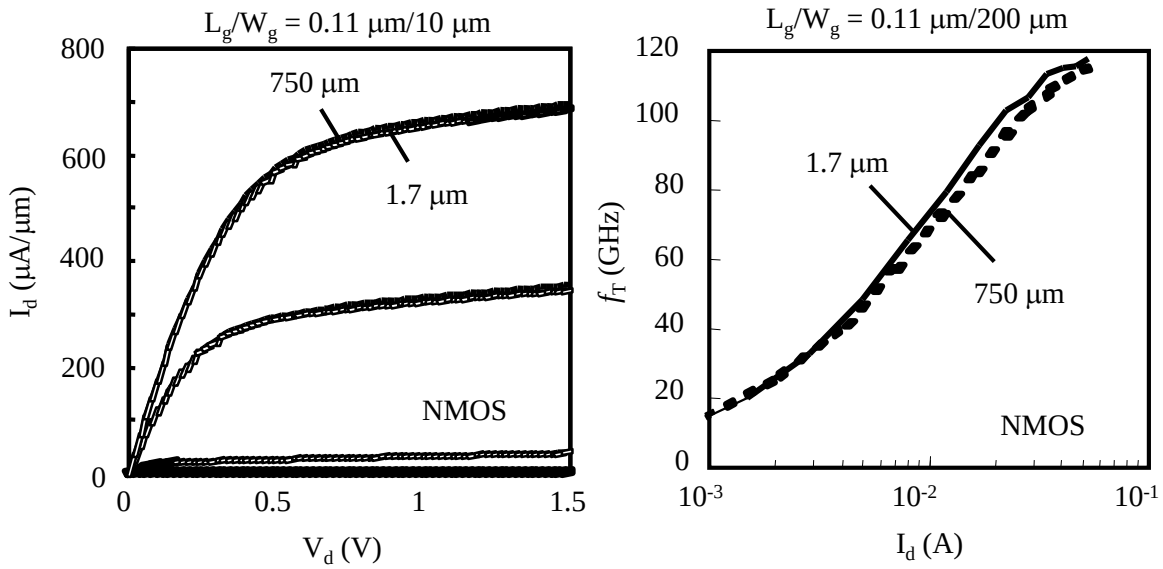


Figure 4-2-7. I_d-V_d and f_T – I_d characteristics of NMOS on ultra-thin chip with 1.7 μm Si substrate.

Figure 4-2-6 shows I_d – V_g and gm – V_g characteristics of NMOS with L_g = 0.11 μm and W_g = 10 μm for 750 μm and 1.7 μm Si substrate thickness. Both I_d-V_g and g_m-V_g characteristics for 1.7 μm case agree with those for 725 μm thickness.

And V_d-I_d characteristics results of NMOS with Lg = 0.11 μm and Wg = 10 μm is also same as shown in 1.7 μm and 725 μm thickness as shown in Fig. 4-2-7. However. The f_T – I_d depends on MOSFET layout described later.

4-2-3. Layout dependence

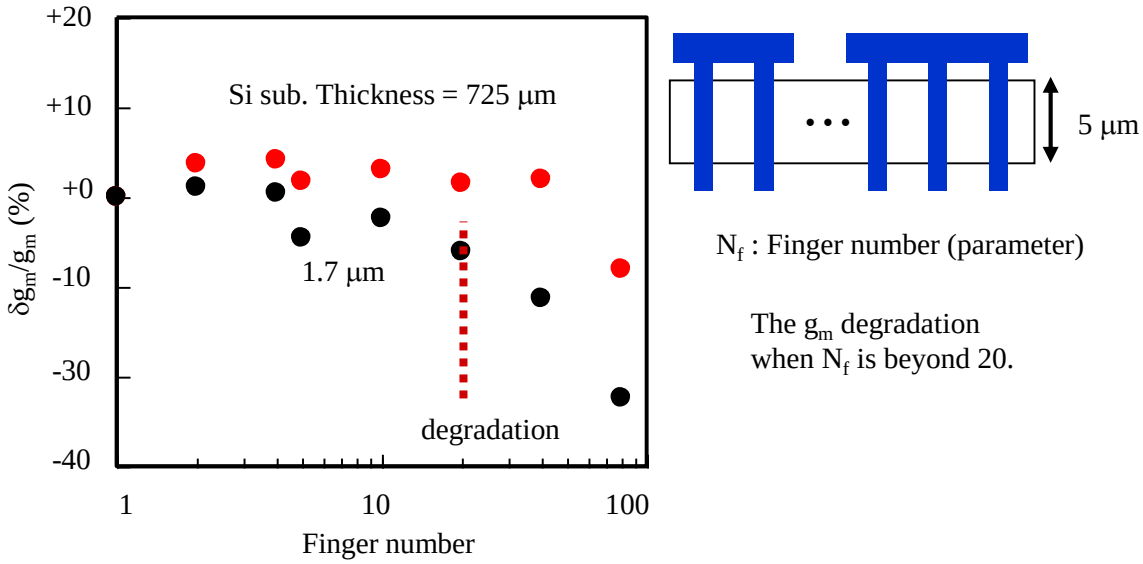


Figure 4-2-8. Finger number dependence of maximum gm value for NMOS on ultra-thin chip.

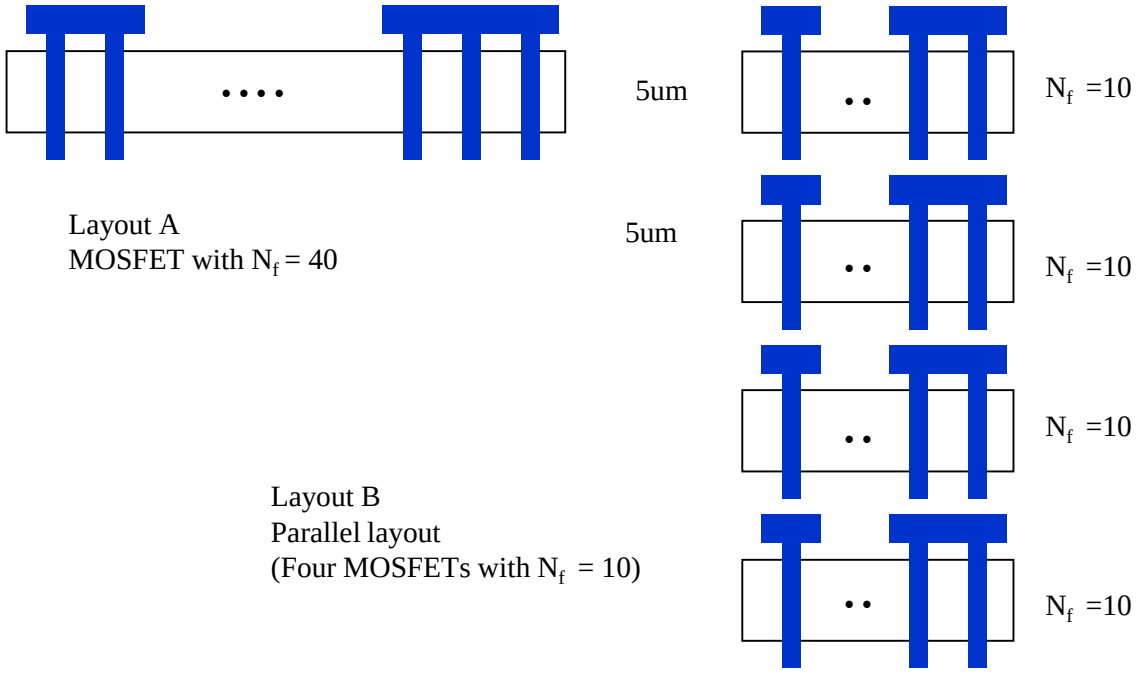


Figure 4-2-9. Multi finger structure for analog circuit(W_{totlal} = 200 μm).
Layout A and B are different from finger length.

Figure 4-2-8 shows finger number dependence of maximum g_m value for NMOS. Finger length of 5 μm is fixed and finger number is parameter. Horizontal axis shows the finger number and vertical axis shows delta gm, which is normalized by g_m at single gate case. This result shows the g_m degrades as the finger number increases. And the g_m significantly degrades in 1.7 μm Si substrate case when the finger number is beyond 20. I believe this degradation is caused by mechanical compressive stress and the stress becomes larger as the length of active area increases.

I changed multi finger structure from series layout to parallel layout as shown in Fig. 4-2-9. The series layout is shown in left hand figure. This structure has all gates on one active area. I define this structure as "Layout A". On the other hand, active area is divided into 4 parts in the parallel layout as shown in right hand figure. Each active area has ten fingers. I define this structure as "Layout B" which be thought as mechanical stress became smaller by reducing of active area length in the case of layout B.

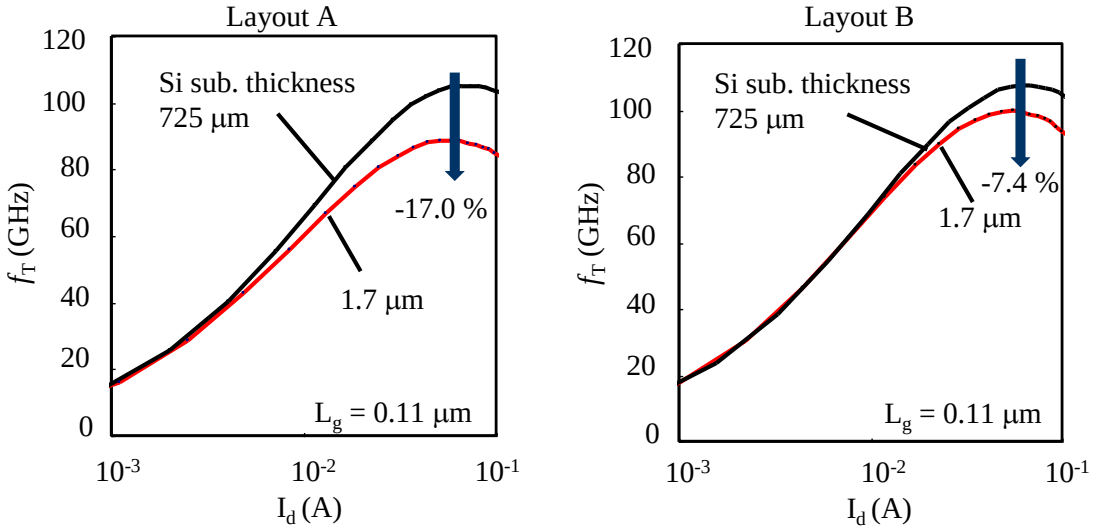


Figure 4-2-10 I_d – f_T curves of 0.11 μm NMOS for layout A and B

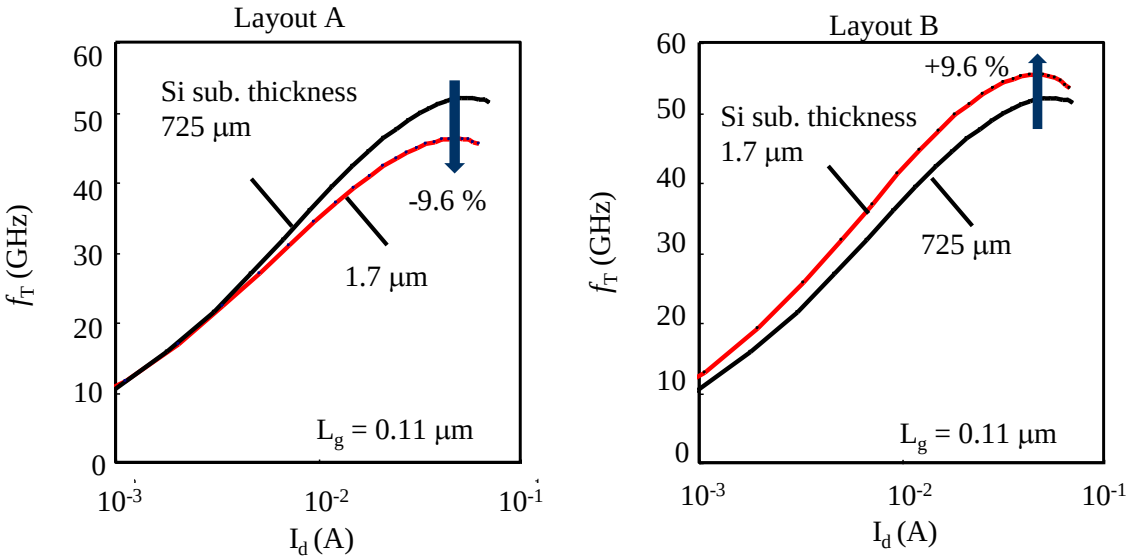


Figure 4-2-11 I_d – f_T curves of 0.11 μm PMOS for layout A and B

Figure 4-2-10 and 4-2-11 show I_d – f_T curves of 0.11 μm NMOS and PMOS for layout A and B, respectively. The maximum value of f_T in 725 μm Si substrate is almost the same in layout A and B of both NMOS and PMOS. However, those f_T in 1.7 μm Si substrate depends on the layout. In NMOS, the f_T was 17.0 % lower than that of 750 μm case in layout A. In the layout B, the f_T in 1.7 μm Si substrate was 7.4 % lower. In PMOS case, though the f_T was 9.6 % lower than that of 750 μm case in layout A, the f_T value was improved by changing to layout B and that exceeded f_T in 750 μm Si substrate thickness, that is 9.6 % increases. These results shows the f_T in layout B is better than that in layout A in 1.7 μm Si substrate.

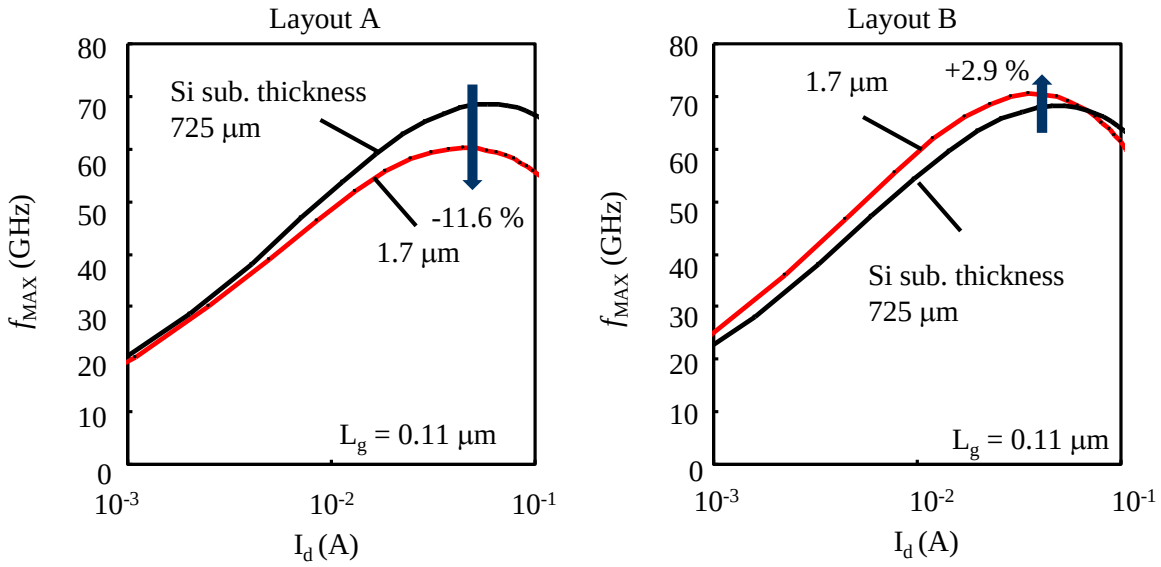


Figure 4-2-12. $I_d - f_{MAX}$ curves of 0.11 μm NMOS for layout A and B.

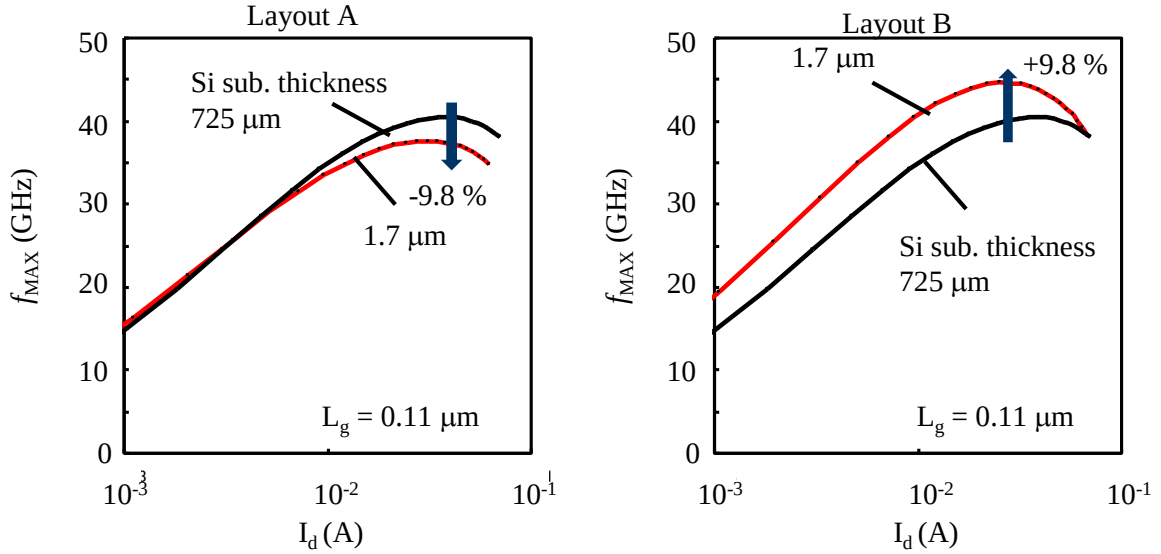
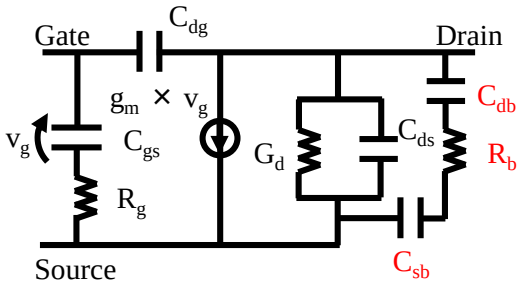


Figure 4-2-13. $I_d - f_{MAX}$ curves of 0.11 μm PMOS for layout A and B.

Figure 4-2-12 and 4-2-13 show $I_d - f_{MAX}$ curves of 0.11 μm NMOS and PMOS for layout A and B, respectively. The maximum value of f_{MAX} in 725 μm Si substrate is almost the same in layout A and B of both NMOS and PMOS. However, those f_{MAX} in 1.7 μm Si substrate depends on the layout as well as the f_T. In NMOS, the f_{MAX} was 11.6 % lower than that of 750 μm case in layout A. However, in the layout B, the f_{MAX} in 1.7 μm Si substrate was 2.9 % higher. In PMOS case, though the f_{MAX} was 9.8 % lower than that of 750 μm case in layout A, the f_{MAX} value was 9.8 % higher.

The layout dependence of MOSFET characteristics in 1.7 μm Si substrate has been serious problem for circuit design. Thus, we must continue to study to resolve this problem.

I describe the analysis results of Si substrate thickness dependence of f_T and f_{MAX} for NMOS and PMOS in layout B.



$$y_{11} = \omega^2 C_{gs}{}^2 Rg + j\omega(C_{gs} + C_{dg})$$
$$y_{12} = -j\omega C_{dg}$$
$$y_{21} = g_m - j\omega(C_{dg} + C_{gs} R_g g_m)$$
$$y_{22} = (G_d + \frac{1}{Rb}) + j\omega(C_{dg} + C_{ds} + C_{db})$$

Current gain

$$\frac{y_{21}}{y_{11}} = \frac{g_m - j\omega(C_{dg} + C_{gs} R_g g_m)}{\omega^2 C_{gs}{}^2 Rg + j\omega(C_{gs} + C_{dg})}$$

Maximum available power gain

$$U = \frac{|y_{21} - y_{12}|^2}{4[\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12})\,\mathrm{Re}(y_{21})]}$$

f_T calculation

$$g_m >> |\omega(C_{dg} + C_{gs} R_g g_m)|$$
$$\omega(C_{gs} + C_{dg}) >> \omega^2 C_{gs}{}^2 Rg$$
$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{dg})} \cong \frac{g_m}{2\pi C_{gs}}$$

f_{MAX} calculation

$$g_m >> |\omega(C_{dg} + C_{gs} R_g g_m)|$$
$$\omega(C_{gs} + C_{dg}) >> \omega^2 C_{gs}{}^2 Rg$$
$$f_{max} \cong \frac{f_T}{2\sqrt{R_g(G_d + \frac{1}{Rb})}}$$

Figure 4-2-14. Y-parameters calculation by equivalent circuit involved Si substrate resistance.

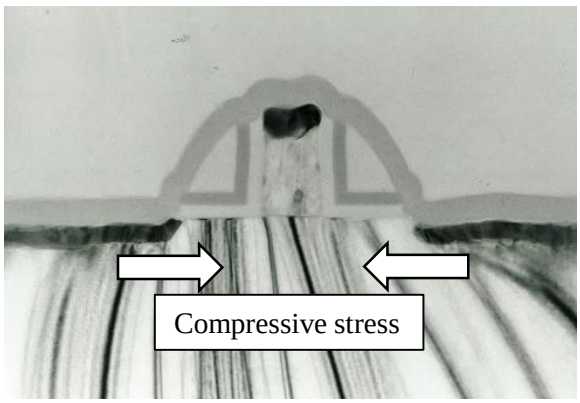


Fig. 4-2-15. TEM photograph of MOSFET on 1.7um thickness Si substrate. Wafer is bent in a convex downward and compressive stress is applied to MOSFET.

Figure 4-2-14 shows Y-parameter calculation results by using equivalent circuit of MOSFET involving substrate resistance. F_T depends on transconduactance and C_{gs} and f_{MAX} depends on not only f_T but also gate resistance (R_g), drain conductance (G_d) and Si substrate (R_b). Thus, thin Si substrate effect appears in f_{MAX}.

Fig. 4-2-15 shows TEM photograph of MOSFET on 1.7 μm Si substrate. The chip is bent in a convex downward and compressive stress is applied to MOSFET.

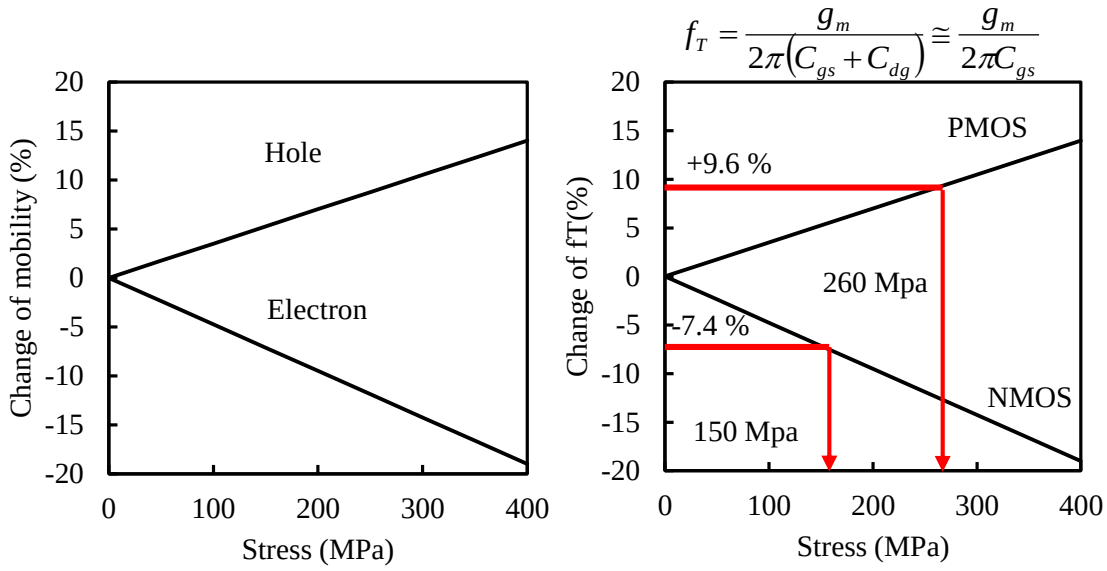


Fig.4-2-16. Compressive stress dependence of f_T for NMOS and PMOS.

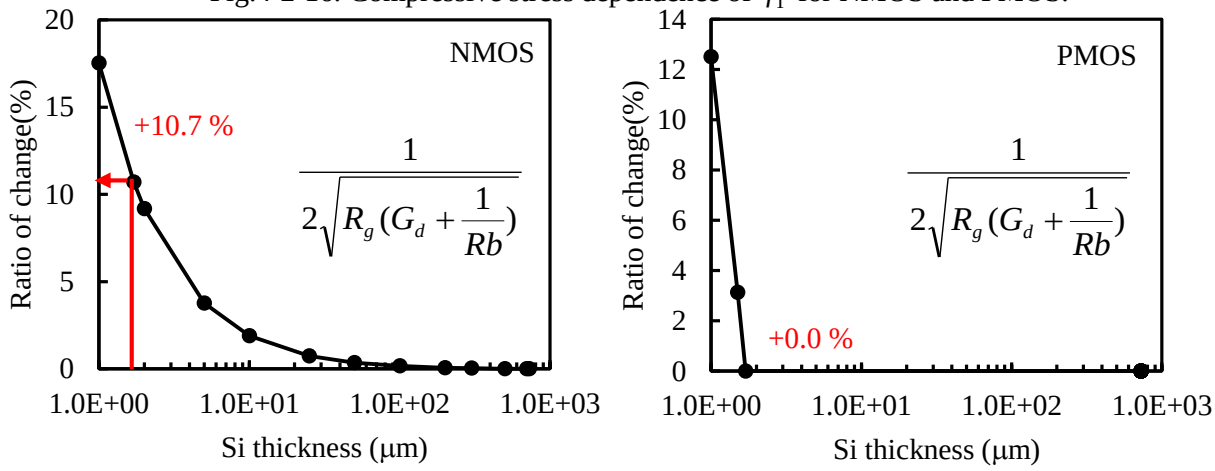


Figure 4-2-17. Ratio of f_{MAX} change by Si substrate thickness change for NMOS and PMOS.

Figure 4-2-16 shows stress dependence of f_T for NMOS and PMOS. In compressive stress, f_T of NMOS decreases and that of PMOS increases due to change of mobility of electron and hole. As shown in Fig. 4-2-10 and 11, the f_T of NMOS and PMOS in 1.7 μm Si substrate is 7.4 % lower and 9.6 % higher than those of 725 μm Si substrate, respectively. Right hand figure shows the estimation line is calculated based on actual data and mobility enhance model. The stress of about 150 - 260 MPa is applied to CMOS on 1.7 μm Si substrate according to these results.

Figure 4-2-17 shows Si thickness dependence of factor of f_{MAX} for NMOS and PMOS estimated by formula described in Fig. 4-2-14. This results indicate the factor increases with decreasing Si substrate thickness because the resistance of Si resistance increases. In NMOS, the resistance is almost in proportional to Si substrate thickness because P-type substrate is used. The factor becomes 10.7 % when the Si substrate thickness is 1.7 μm.

Table 4-2-1. Actual data and calculation results of f_T and f_{MAX} of NMOS and PMOS for normal thickness (725 μm) and ultra thin (1.7 μm).

NMOS	Formula	Value	Gain (%)	Reason
F_T	$f_T = \frac{g_m}{2\pi(C_{gs}+C_{dg})} \cong \frac{g_m}{2\pi C_{gs}}$	108 GHz (725 μm) 100 GHz (1.7 μm)	-7.4 %	Lower Mobility 150 Mpa (Compressive)
Factor	$\frac{1}{2\sqrt{R_g(G_d+\frac{1}{Rb})}}$	1.22 (725 μm) 1.35 (1.7 μm)	+10.7 %	Higher R_b 1.7 μm thin Si substrate.
F_{MAX}	$f_{max} \cong \frac{f_T}{2\sqrt{R_g(G_d+\frac{1}{Rb})}}$	69 GHz (725 μm) 71 GHz (1.7 μm)	+2.9 % (Data) +2.5% (Cal.)	Increase of factor of F_{MAX}

PMOS	Formula	Value	Gain (%)	Reason
F_T	$f_T = \frac{g_m}{2\pi(C_{gs}+C_{dg})} \cong \frac{g_m}{2\pi C_{gs}}$	52 GHz (725 μm) 57 GHz (1.7 μm)	+9.6 %	Higher Mobility 260 Mpa (Compressive)
Factor	$\frac{1}{2\sqrt{R_g(G_d+\frac{1}{Rb})}}$	1.09 (725 μm) 1.09 (1.7 μm)	+0.0 %	No change of R_b
F_{MAX}	$f_{max} \cong \frac{f_T}{2\sqrt{R_g(G_d+\frac{1}{Rb})}}$	41 GHz (725 μm) 45 GHz (1.7 μm)	+9.8 % (Data) +9.6 % (Cal.)	Increase of factor of F_{MAX}

Table 4-2-1 shows the analysis results of f_T and f_{MAX} of NMOS and PMOS for normal thickness (725 μm) and ultra thin (1.7 μm) in layout B. In NMOS, though the f_T degrade due to mobility degradation by compressive stress, f_{MAX} increases due to the increase of substrate resistance by thinning Substrate. In PMOS, the f_T becomes higher due to mobility increase by compressive stress. The f_{MAX} also increases due to the increase of f_T even without increases of the factor of f_{MAX}. In PMOS, the well resistivity is determined by the depth and concentration of Nwell, while in NMOS, the well resistivity is determined by both those of Pwell and the thickness and concentration of Si substrate because Psub is used for LSI circuit fabrication.

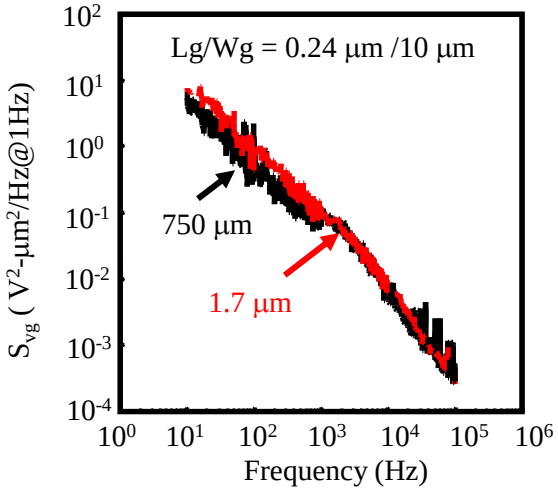


Figure 4-2-18. 1/*f* noise characteristics of 0.24 μm NMOS on ultra-thin chip.

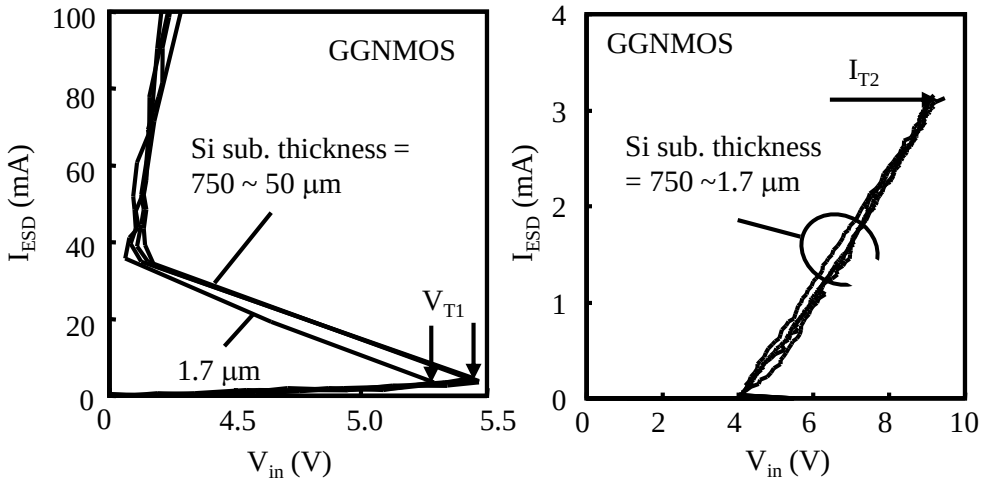


Figure 4-2-19 ESD characteristics of GGNMOS on ultra-thin chip

Figure 4-2-18 shows 1/*f* noise spectra of 0.24 μm NMOS. The noise was measured in order to evaluate the quality at the interface of gate insulator and Si substrate because the noise sensitive to interface density (D_{it}). No difference of 1/*f* noise was observed in both Si substrate thickness cases.

Figure 4-2-19 shows ESD characteristics of 1.7 μm and 725 μm Si thickness. The important points for ESD are snapback voltage Vt_1 and critical current It_2. Left hand figure shows Si substrate thickness dependence of snap-back characteristics. When Si thickness is 1.7 μm , the turn-on voltage was slightly lower than those of thicker substrates because the bipolar action of NPN in NMOS works easily due to higher substrate resistance which corresponding to base resistance of NPN. This performance is better from the view point of ESD because a thin gate oxide film easily break down. Right hand figure shows the critical current for various Si substrate thickness. The critical current in all cases are almost the same. These results show ESD performance slightly improve when Si substrate is thinned to 1.7 μm.

4-2-4. Substrate noise results

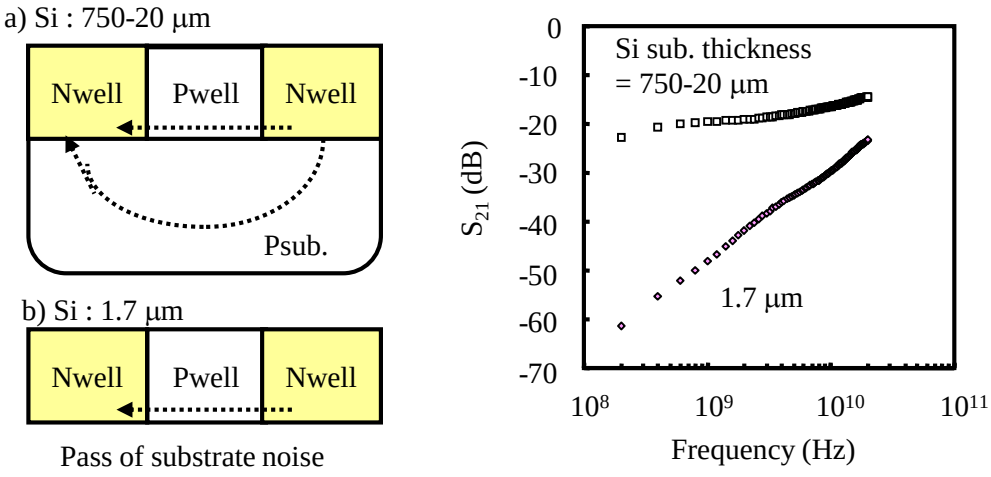


Figure 4-2-20. Frequency dependence of substrate noise (S_{21}).

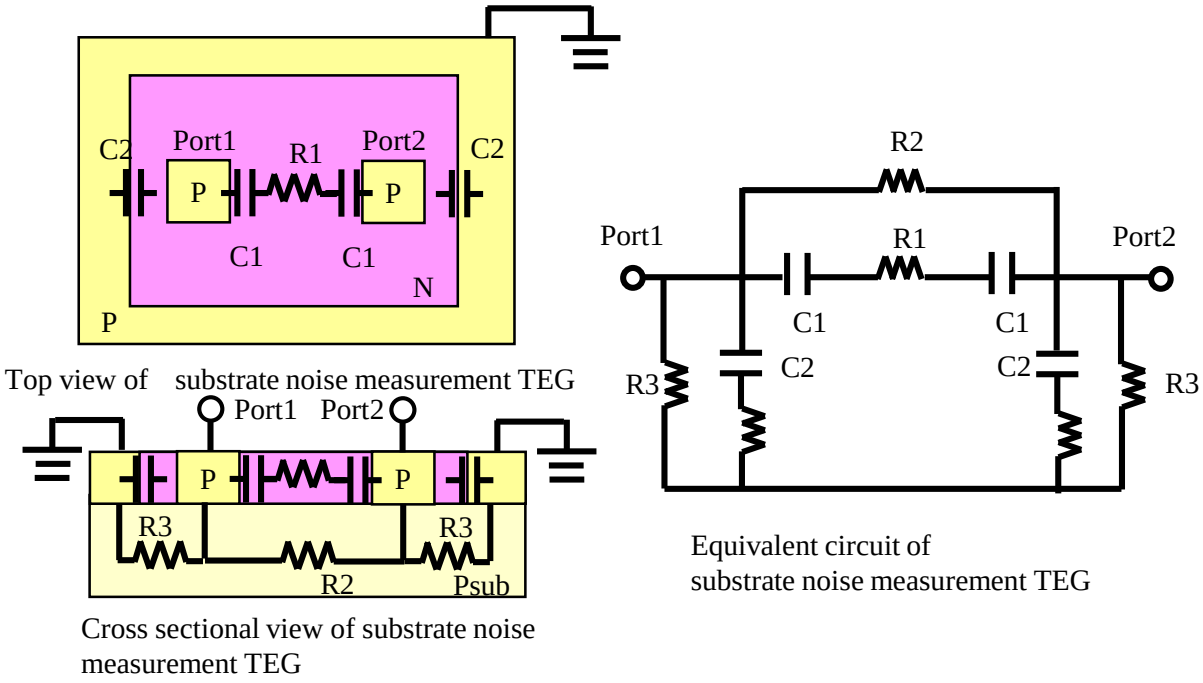
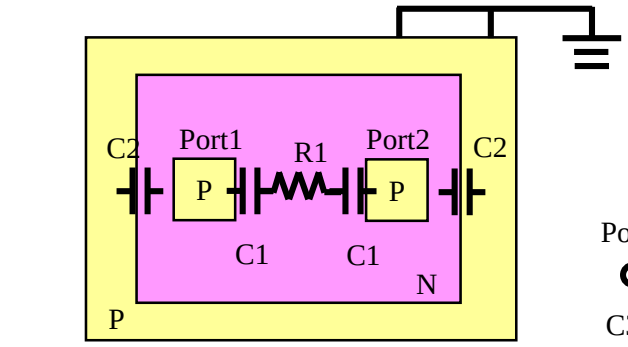
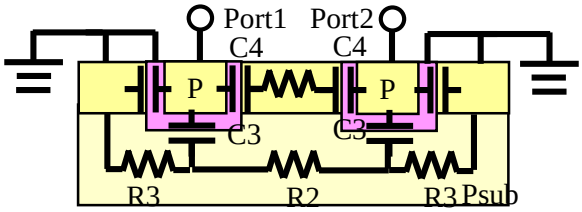


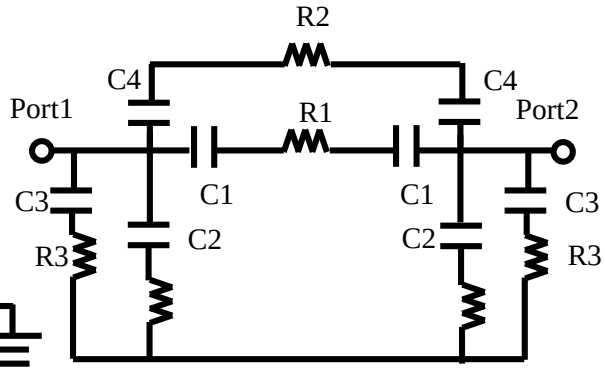
Figure 4-2-21. Modeling of substrate noise (S_{21}) in 725 μm Si substrate case using equivalent circuit.



Top view of substrate noise measurement TEG

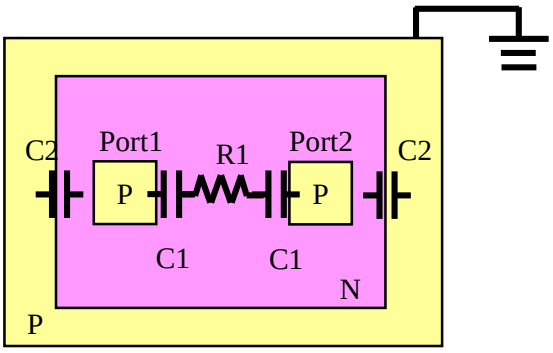


Cross sectional view of substrate noise measurement TEG

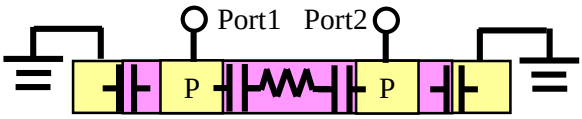


Equivalent circuit of substrate noise measurement TEG

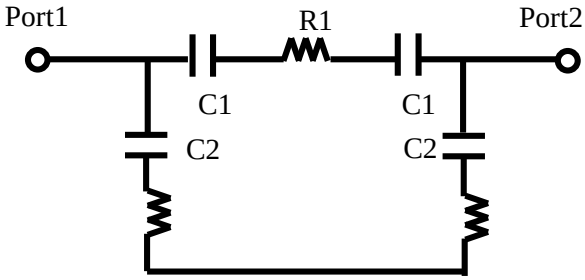
Figure 4-2-22. Modeling of substrate noise (S_{21}) with deep Nwell in 725 μm Si substrate case using equivalent circuit.



Top view of substrate noise measurement TEG



Cross sectional view of substrate noise measurement TEG



Equivalent circuit of substrate noise measurement TEG

Figure 4-2-23. Modeling of substrate noise (S_{21}) in thin Si substrate (1.7 μm) case using equivalent circuit.

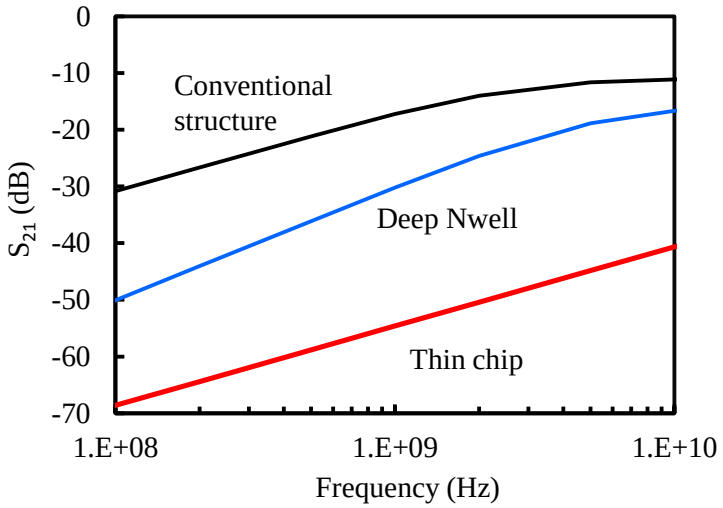


Figure 4-2-24 Calculation results of substrate noise (S_{21}) using equivalent circuit

Figure 4-2-20 shows frequency dependence of substrate noise between Nwell and the adjacent Nwell. Right hand figure shows frequency dependence of S_{21}. Horizontal axis shows the frequency and vertical axis shows S_{21}. Parameter is Si substrate thickness. As I expected, the larger reduction was observed in the case of 1.7 μm thickness because the penetration of the noise, which passes along Psub from Nwell can be suppressed. The reduction value was beyond 20 dB when the frequency was 1 GHz. This is excellent advantage point for mixed signal chip. In order to analyze this advantage, the equivalent circuit model for PNP junction with and without deep-Nwell in 725um Si substrate and PNP junction in 1.7 μm Si substrate as shown in Fig. 4-2-21,22,and 23. Figure 4-2-24 shows calculation results of substrate noise (S_{21}) using equivalent circuit. In 725 μm Si substrate cases, S_{21} becomes larger because junction capacitor with Si substrate is larger than that of 1.7 μm Si substrate case. Even if deep Nwell is used, the effect to reduce the substrate noise decrease with frequency. On the hand, in 1.7 μm Si substrate, the reduction is larger even when the frequency become higher.

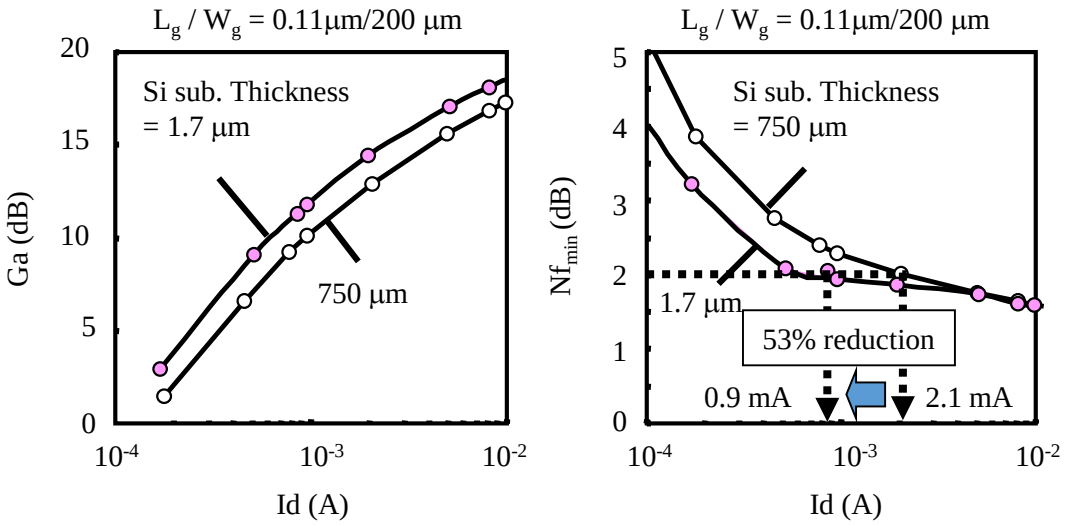
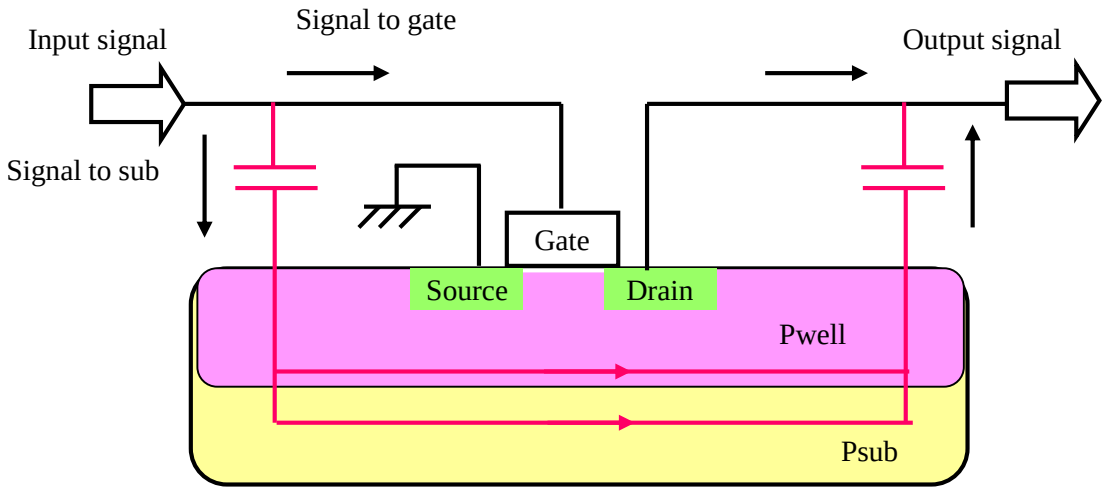


Figure 4-2-25. Drain current dependence of Ga and N.F.$_{min}$ at 3 GHz.



Signal to Si sub. decreases as the Si substrate becomes thinner

Figure 4-2-26. Explanation for improvement of gain in thinner chip.

The advantage point of ultra thin chip is not only substrate noise but also $N.F._{min}$ of MOSFET because lower substrate loss. Figure 4-2-25 shows drain current dependence of gain and $N.F._{min}$ for 0.11 μm NMOS at 3 GHz operation. These results in from 725 to 20 μm Si substrate thickness cases were almost the same. On the other hand, higher gain and lower $N.F._{min}$ were observed in 1.7 μm case. I compared the drain current at a certain $N.F._{min}$. For example, the current at 2.0 dB $N.F._{min}$ was 2.1 mA in 750 μm Si substrate, while that was 0.98 mA in 1.7 μm case, which was reduced by 53%. This result shows ultra-thin chip is effective for low current consumption of CMOS Low Noise Amplifier.

Figure 4-2-26 is explanation about improvement of Ga and $N.F._{min}$ in thinner Si substrate. A part of input-signal goes to the Si substrate because of coupling between signal line and Si substrate. This substrate signal is not amplified, while the signal going to the gate is amplified by MOSFET. In order to obtain higher gain, we want to make small the substrate signal, which goes to a Si substrate as much as possible. As the Si substrate thickness becomes thinner, the signal to the substrate becomes smaller because the impedance in Si substrate increases. If the gain becomes larger, the noise becomes smaller. Thus, higher gain and lower $N.F._{min}$ was observed in the case of ultra thin Si substrate such as 1.7 μm.

4-2-5. Inductor characteristics

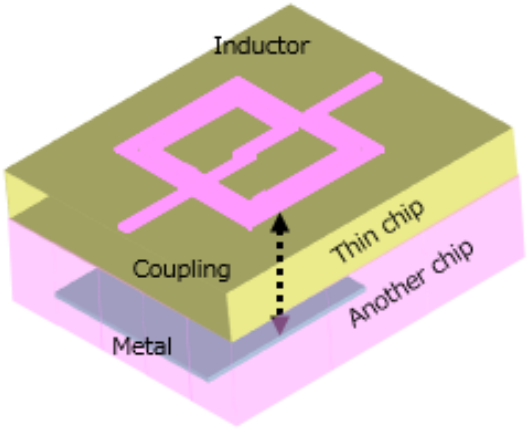


Figure. 4-2-27. Problem of Stacked structure with thin Si substrate chip. The coupling between Inductor and metal wire in stacked chip occurs.

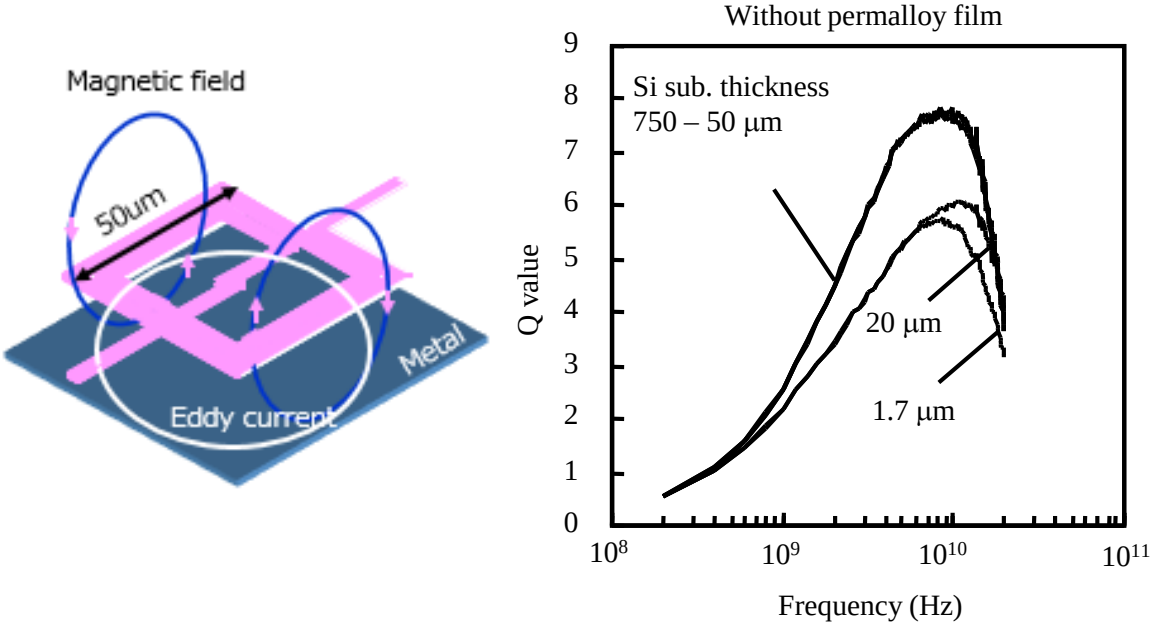


Figure 4-2-28. Frequency dependence of Q value on various Si substrate thickness.

Figure 4-2-27 shows the cross sectional view of stacked chip with inductor. The performance of Inductor degrades by making a Si substrate thin because of coupling between inductor and metal layer in stacked chip

Figure 4-2-28 shows frequency dependence of Q value of inductor with 50 μm outer length. When the thickness is from 750 μm to 50 μm, no degradation of Q value was observed, on the other hand, the Q value decreased when the thickness is 20 μm and 1.7 μm. This is caused by energy loss due to eddy current in metal layer in stacked chip, which induced by magnetic field. It depends on outer length of inductor for the distance between inductor and metal layer in which the Q value begins to degrade.

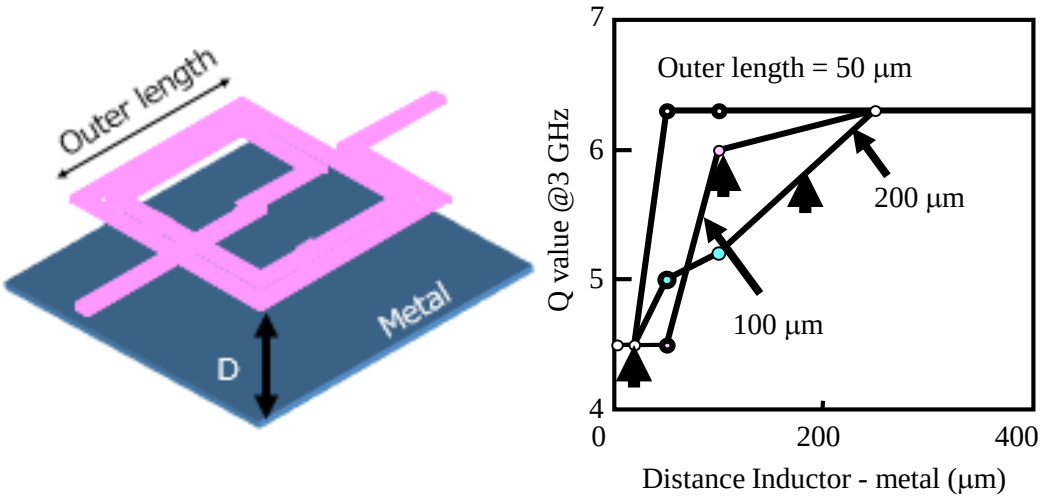
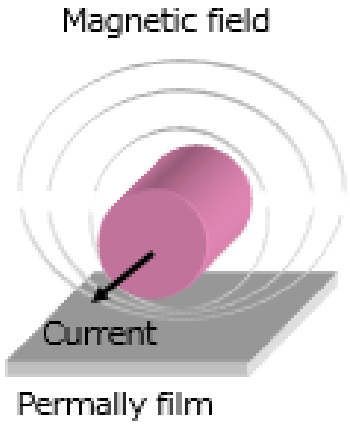


Figure 4-2-29. Outer length dependence of Q value.



Deposition : Sputtering

Fe : 16.9% Ni : 83.9%

Resistivity : 30 mΩ·cm

Thickness : 10 – 300 nm

Application of shield effect MRAM etc.

Figure 4-2-30. Permalloy film in our experiments.

The right hand figure in Fig 4-2-29 shows the distance between inductor and metal layer dependence of Q value. Horizontal axis shows a distance between inductor and the metal wire. And vertical axis shows the Q value at 3 GHz. Parameter is outer length of Inductor such as 50, 100 and 200 μm. According to these results, the Q value begins to degrade when the distance between inductor and metal layer is almost below the outer length. In order to suppress the Q value degradation in thin Si substrate thickness case, I propose magnetic shielding by permalloy (NiFe) film deposition.

A permalloy film is a magnetic alloy material of iron and nickel and is used for magnetic shielding. The application of this film is for example, Magnetic head and MRAM. Atomic % of iron and Ni in our permalloy film was 16.1 and 83.9%, respectively. The resistivity is 30 mohm cm as shown in Fig. 4-2-30. In our experiments, the deposition thickness of the permalloy film was from 10 to 300 nm.

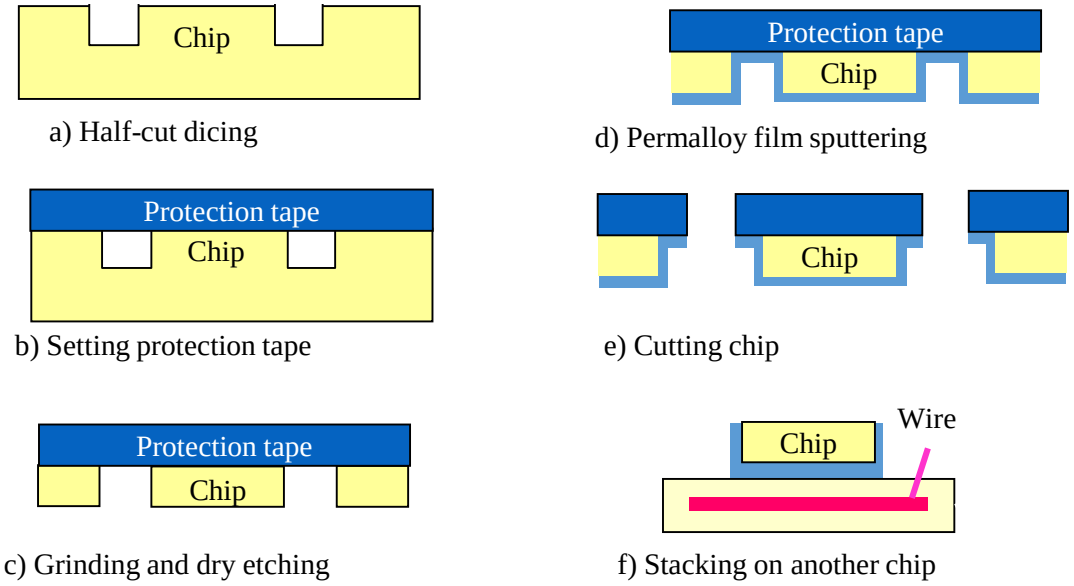


Figure 4-2-31. Permalloy film deposition process under ultra-thin chip and stacked chip process.

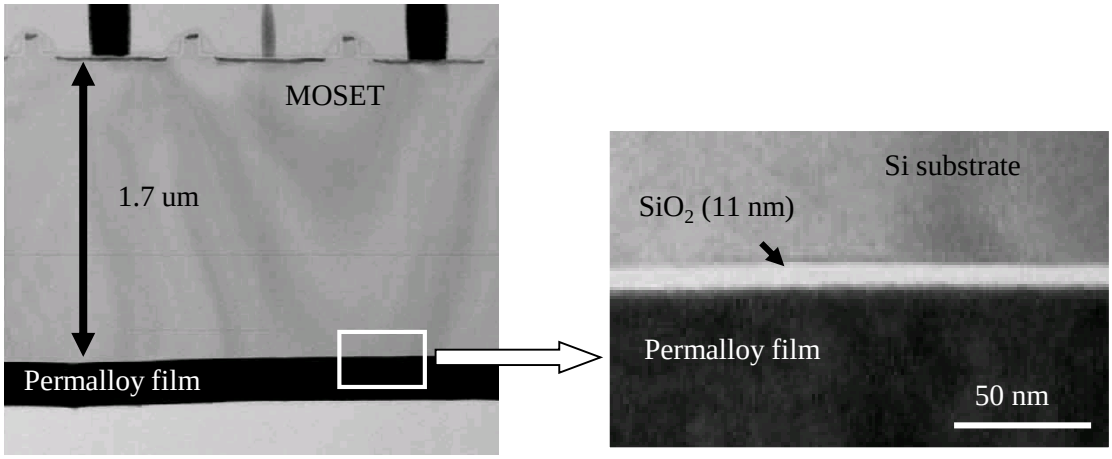


Figure 4-2-32. TEM photograph of ultra-thin chip with 300nm permalloy.

Figure 4-2-31 shows permalloy film deposition and stacking chip process. After grinding and dry etching, permalloy film was deposited on backside of Si substrate by sputtering. After the thin chip was cut and that was stacked on another chip which has metal wire. And the protection tape was peeled from the chip.

Figure 4-2-32 show a TEM photograph of ultra-thin chip with 300 nm permalloy film. This film does not degrade DC and analog performance, because permalloy film was isolated by 11 nm SiO_2 layer, seeing interface between the Si substrate and the film.

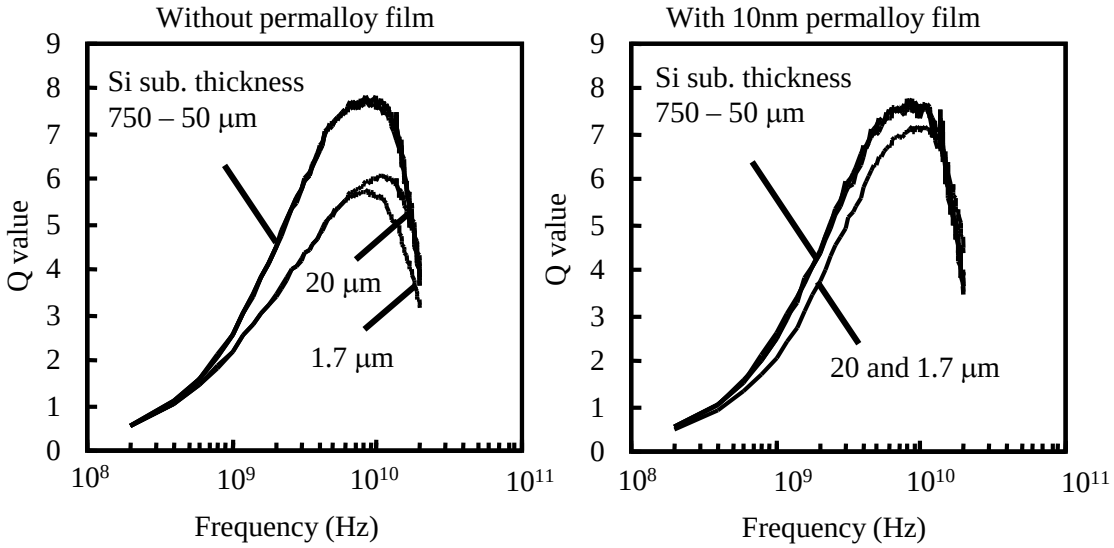


Figure 4-2-33. Frequency dependence of Q value of inductor with and without 10 nm permalloy film for various Si substrate thickness.

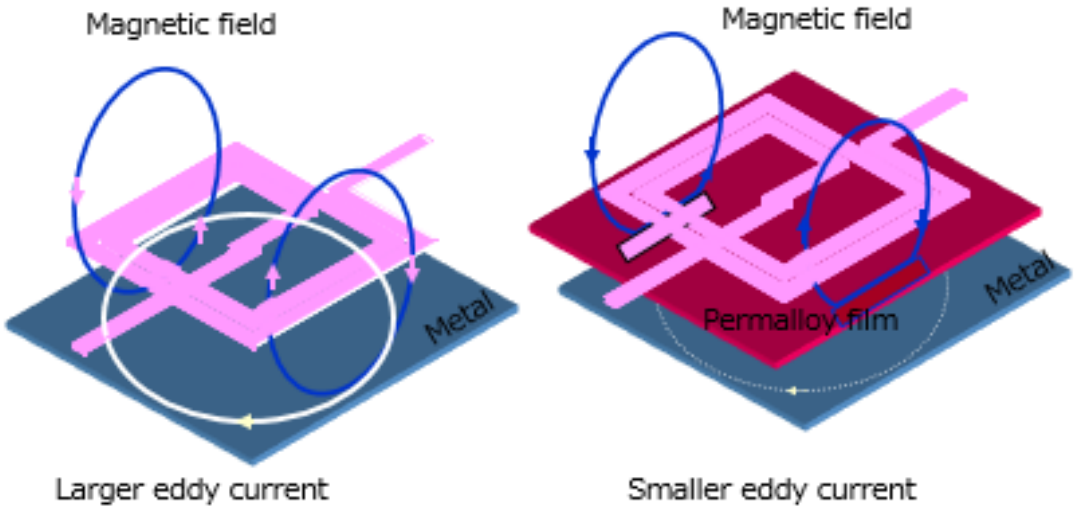


Figure 4-2-34. The effect of permalloy film deposition for inductor Q value.

Figure 4-2-33 shows frequency dependence of Q value for various Si substrate thickness with and without 10nm permally film. The Q value decrease of 27% was observed at 10 GHz in the 1.7 μm case without permalloy film. On the other hand, the Q value degradation in samples below 20 μm Si substrate thickness became smaller by the deposition of 10nm permalloy. Figure 4-2-34 shows effect of permalloy film deposition. The magnetic field occurred by inductor induces eddy current into metal wire without permalloy film, while the eddy current becomes smaller by permalloy inter layer because the paermalloy film can suppress penetration of the magnetic field into the metal wire.

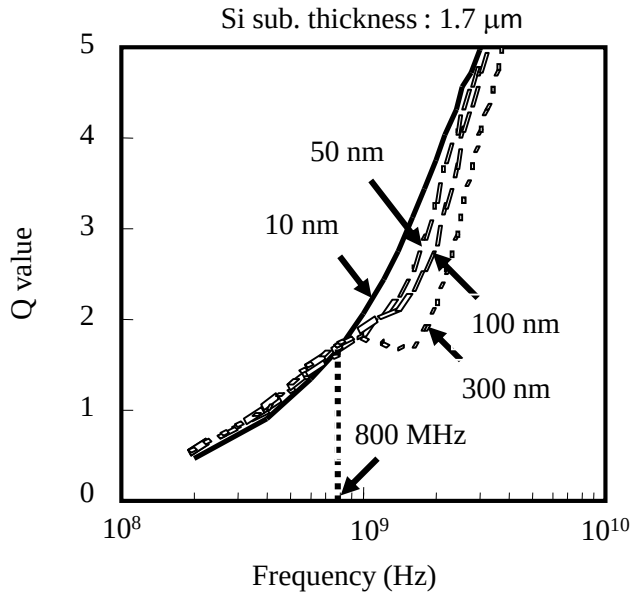


Figure 4-2-35. Frequency dependence of Q value for various permalloy thickness.

Figure 4-2-35 shows frequency dependence of Q value for various permalloy thickness samples when the Si substrate thickness is 1.7 μm. The degradation of Q value was observed as the film thickness increased when the operation frequency is beyond 800 MHz. . This is caused by eddy current in the permalloy film. In order to suppress this Q value degradation, The higher resistance of the film is required. According to our experiments, thin permalloy film such as 10 nm is suitable for suppression of Q value degradation.

Table 4-2-2. Comparison between high resistivity(>1000 ohm-cm) substrate and normal substrate (1 ohm-cm), normal thickness (725 μm) and ultra thin (1.7 μm).

	Resistivity (ohm-cm)	Slip	Thickness (μm)	Cost	Sub. noise
Normal sub.	1	-	725	Ref.	Ref.
High resistivity sub.	1000	Problem	725	Worse	Better
Method		Precipitated Wafer			
Ultra thin sub.	1	-	1.7	-	Better
Ultra thin sub.	1000	Problem	1.7	Worse	Better
Method		Precipitated Wafer			

	Thermal noise	Nwell leak	Latch up	Q value of Inductor
Normal sub.	Ref.	No	Ref.	Ref.
High resistivity sub.	worse	Worse	Worse	Better
Method	Metal under PAD	Additional boron implantation	Additional boron implantation	
Ultra thin sub.	Better	-	-	Worse (3D stack)
Ultra thin sub.	Better	-	-	Worse (3D stack)
Method				Permalloy (FeNi) sputtering

Table 4-2-2 shows Comparison between high resistivity(>1000 ohm-cm) substrate and normal substrate (1 ohm-cm), normal thickness (725 μm) and ultra thin (1.7 μm) . 725 μm high resistivity substrate is suitable for high Q inductor, but thermal noise, Nwell leakage current and latch up are degraded. In order to solve these problems, additional process are needed. On the other hand, ultra thin substrate with normal resistivity is better except Q value of inductor. However, because the thin wafer is required for high density 3D stacked chip, this substrate is suitable for future system in package.

Conclusion

High resistivity Si substrate is attractive for realization of high Q inductor. Fully precipitated oxygen wafer is useful because the wafer can suppress slip generation during STI process and keep high substrate resistivity during sinter process. The additional Boron implantation can suppress the leakage current between the adjacent Nwells due to shallow X_j. No affection to MOSFET characteristics by this implantation was observed.

Ultra-thin chip with 1.7 μm Si substrate thickness brings about a larger reduction of substrate noise and $N.F._{min}$ at 3GHz because the penetration of the noise which passes along Psub from Nwell can be suppressed. No degradation of fmax and 1/*f* noise indicate no degradation of mobility and D_{it} due to thinner process. The Q value degradation due to metal wire under chip can be suppressed by 10 nm permalloy(NiFe) deposition on backside of Si substrate because the film can shield wire from the magnetic field [35].

According to comparing results with high resistivity Si substrate, 725 μm high resistivity substrate is suitable for high Q inductor, but thermal noise, Nwell leakage current and latch up are degraded. In order to solve these problems, additional process are needed and wafer cost becomes higher. On the other hand, ultra thin substrate is better except Q value of inductor. The Q value degradation is easily suppressed by thin permalloy film deposition on backside of chip. Because the thin wafer is required for high density 3D stacked chip, I conclude this thin substrate is suitable than high resistivity substrate for future system in package.

The issue of CMOS in ultra-thin Si substrate such as 1.7 μm is layout dependence of the characteristics. This is serious problem for circuits designers. Thus, we must continue to study and develop new technology to resolve this issue.

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Chapter 5
Mixed-signal and RF characteristics of FinFET

In this chapter, mixed-signal and RF characteristics of FinFET are discussed because this is most aggressive device for digital circuits in order to realize scaled MOSFET with gate length below 30 nm. This Fin structure has advantage point to suppress short channel effect because there is gate electrode both side of Si fin. Already, this structure has been production level and digital designer start to design. However, production cost is higher comparing with planar MOSFET because narrow fin can not be fabricated without high spec lithography. Thus, this device has been used for high-end production which high speed operation digital circuits. When mixed signal and RF circuits are designed by advanced CMOS, we must understand those characteristics of the device. We investigated mixed-signal performance by measuring actual samples with various size of fin. Especially, I focus on 1/*f* noise which is important for both digital and mixed-signal circuits. The channel surface of FinFET is etched during fin structure. So, I think that the interface state density at interface between fin surface and gate insulator becomes worse and 1/*f* noise degrades. In this chapter, the process to improve the quality of fin surface is also discussed. Regarding to RF performance, such as ft and fmax I calculated those based on parasitic resistance and capacitance. When we use the finger structure of FinFET for mixed-signal and RF circuits, the parasitic capacitance becomes larger comparing with planar MOSFET because FinFET has non negligible larger gate capacitance between Fins. Thus, shrink of pitch is important to reduce the capacitance. But gate resistance increases as the pitch becomes smaller. Thus we must introduce metal not poly Si gate but gate electrode.

5-1. Sample fabrication of FinFET

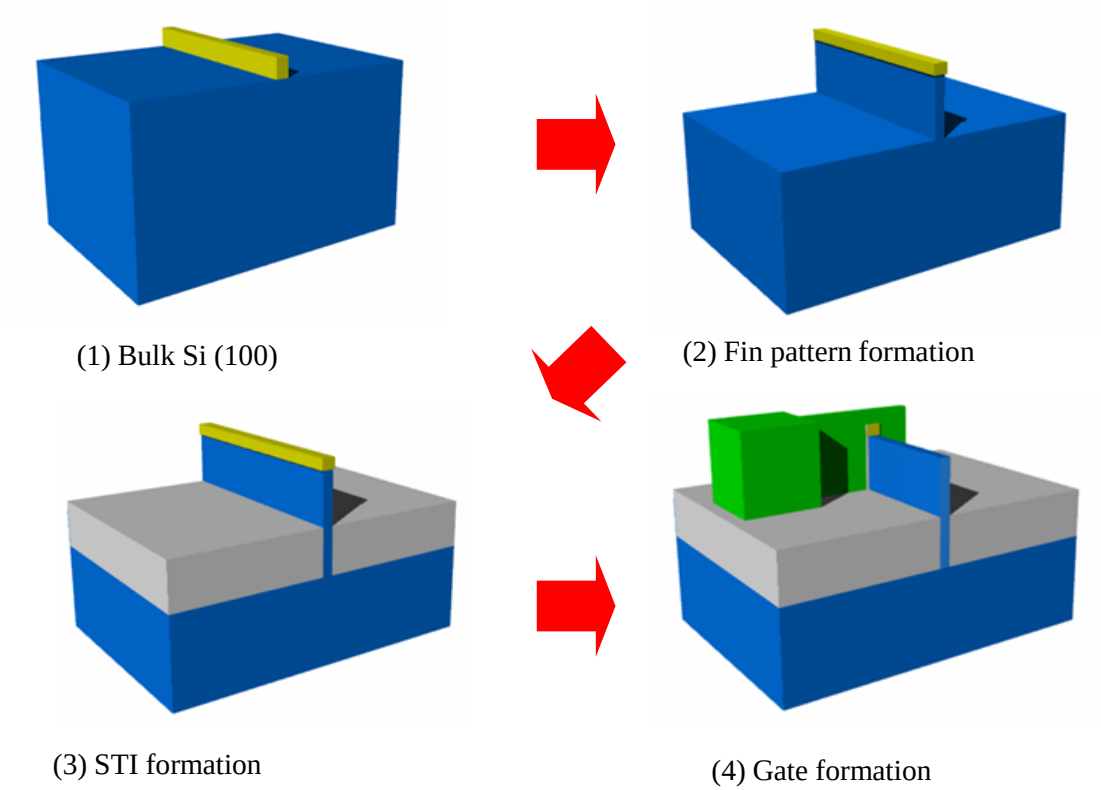

Figure 5-1. Process flow of FinFET formed on bulk Si substrate [4,6-9].

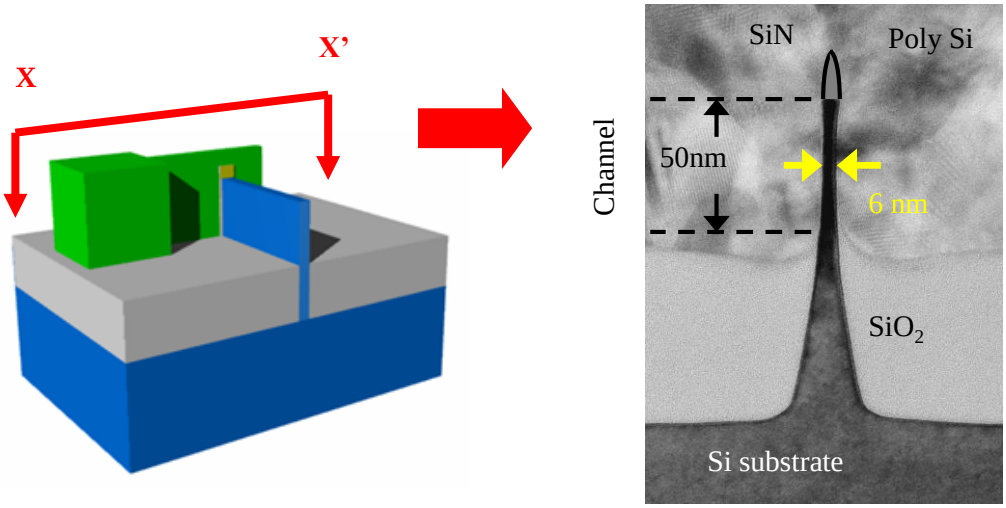

Figure 5-2. TEM photograph of FinFET along with X-X'. Uniform fin width down to 6 nm was fabricated [4,6-9].

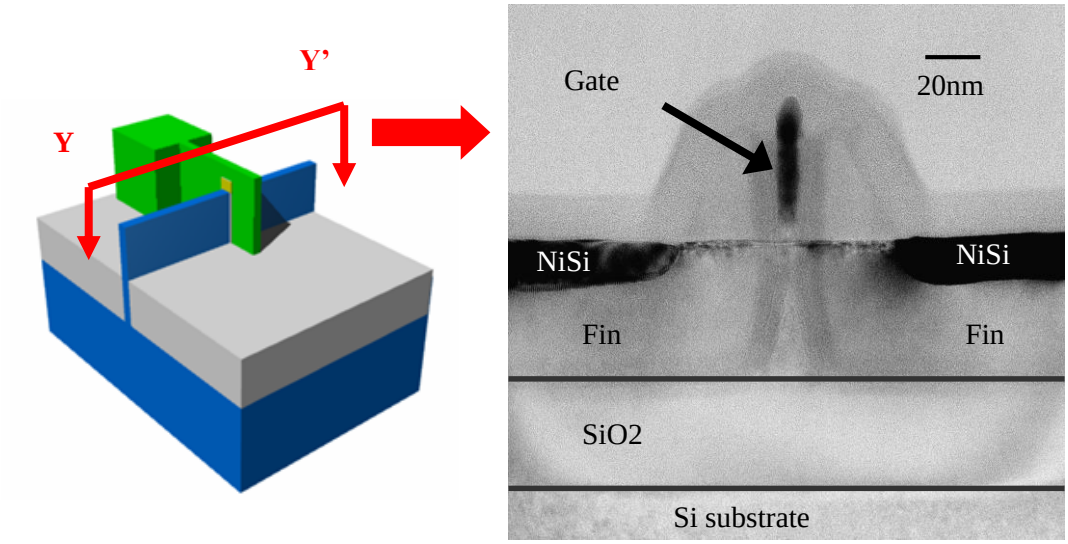

Figure 5-3. TEM photograph of FinFET along with Y-Y'. Poly-Si gate was fabricated down to 20 nm length [4,6-9].

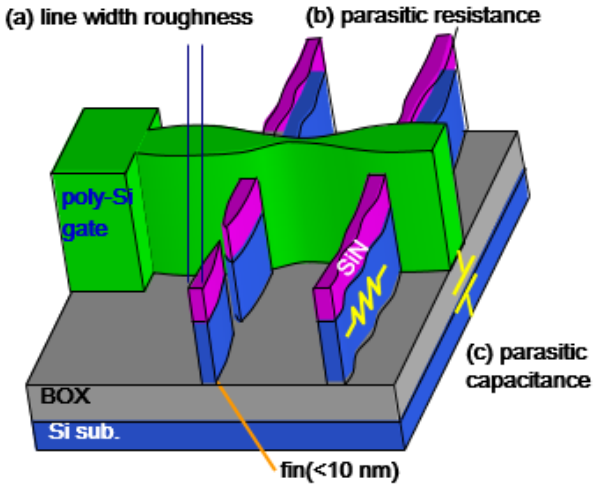

Figure 5-4. Summary of issue of FinFET. Those are line width roughness, parasitic resistance and parasitic capacitance [4,6-9].

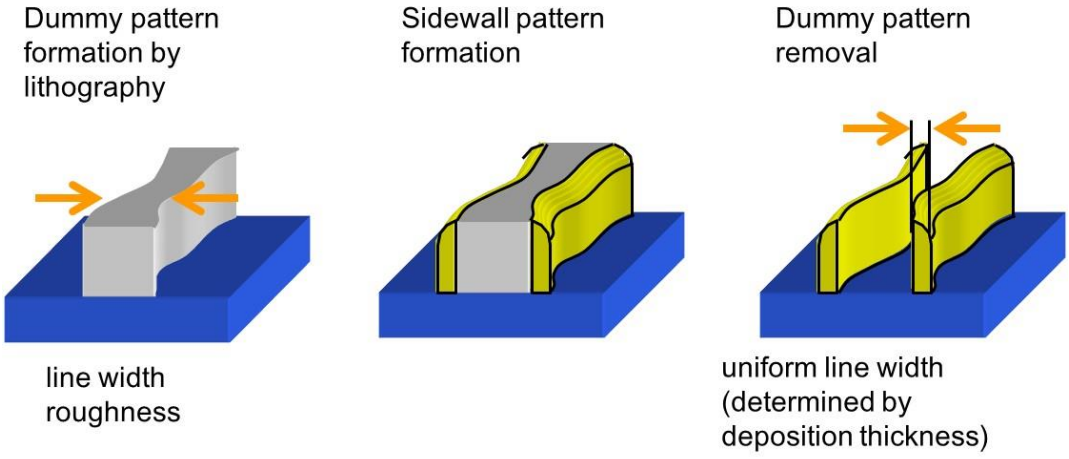

Figure 5-5. Narrow patterning process by side-wall transfer (SWT) [4,6-9].

The FinFET to measure DC and 1/*f* noise are fabricated by Dr. Inaba, Kaneko, Okano et al,. The detail of the process flow are described in ref. 4 and 6 - 9.

Figure 5-1 shows process flow for bulk-FinFET device fabrication on bulk Si substrate. The bulk Si wafer is used to suppress increase of the cost. The STI is formed after fin patterning. After that, gate electrode is formed. The issue to obtain high performance is how to fabricate narrow fin line and short gate length. They used side-wall transfer technique for the fabrication. Figure 5-2 shows cross sectional TEM image along X-X'. Uniform fin width down to 6nm was fabricated by side-wall transfer technique. Bottom of Fin is wider but active region within height of 50 nm is about 6 nm. Figure 5-3 shows cross sectional TEM image along Y-Y'. The poly-Si gate was fabricated down to 20 nm length. I used side-wall transfer technique for this gate electrode fabrication, too. The gate length is 20 nm. Figure 5-4 shows the summary of FinFET issue. First is line with roughness, which causes threshold voltage variation. Second is higher parasitic resistance due to narrow fin line, which causes the degradation of drivability. Third is higher parasitic capacitance between gate electrode and Si substrate, which causes the degradation of RF performance. Figure 5-5 shows the process of narrow line patterning by side-wall transfer. First step is dummy pattern formation by lithography. Next step is sidewall patterning formation by SiN film deposition and etching. After that, dummy pattern film is removed. They used this process to both fin and gate electrode formation.

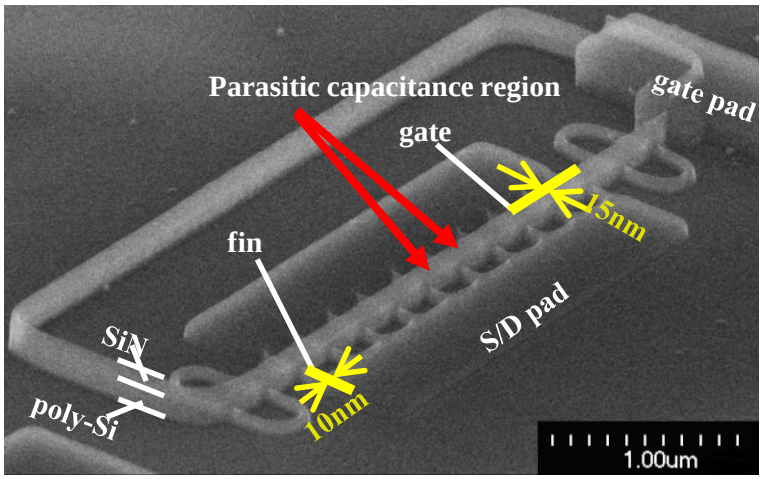

Figure 5-6. SEM photograph of FinFET fabricated by SWT process [4, 6-9].

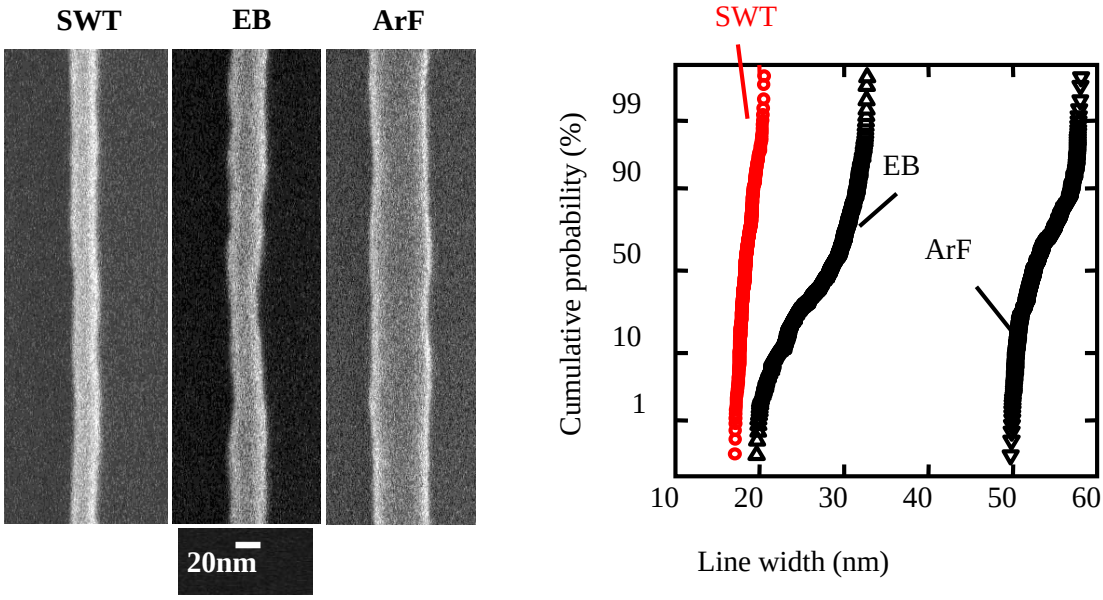

Figure 5-7. Comparison of Line width roughness. SWT process realized much smaller line width roughness [4, 6-9].

Figure 5-6 shows SEM photograph of FinFET used sidewall patterning. Gate length of 15 nm and fin width of 10 nm has been successfully fabricated.

Figure 5-7 shows comparison of line width roughness among three kinds of patterning process. Those are sidewall transfer, electron beam and ArF lithography. The sidewall transfer process can realize narrow line with small line width roughness.

5-1-2. Process dependence of DC characterstics

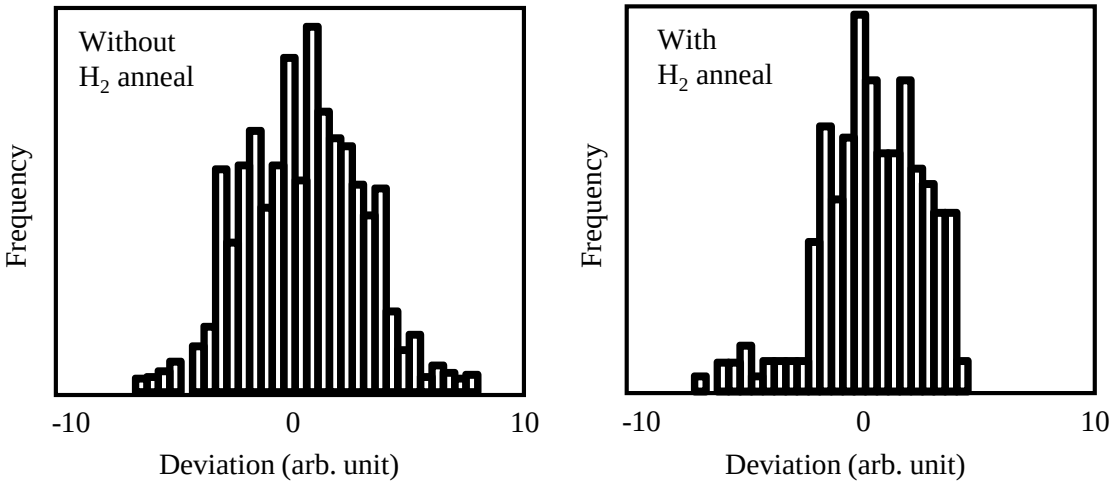

Figure 5-8. Surface treatment impact on Roughness of fin sidewall [4, 6-9].

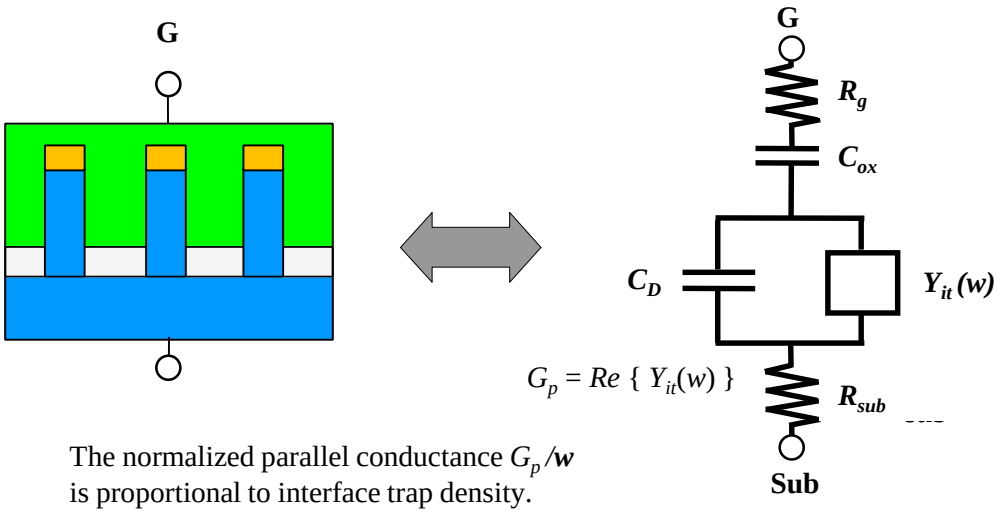

Figure 5-9. Parallel Conductance Measurement on Fin capacitor [4, 6-9].

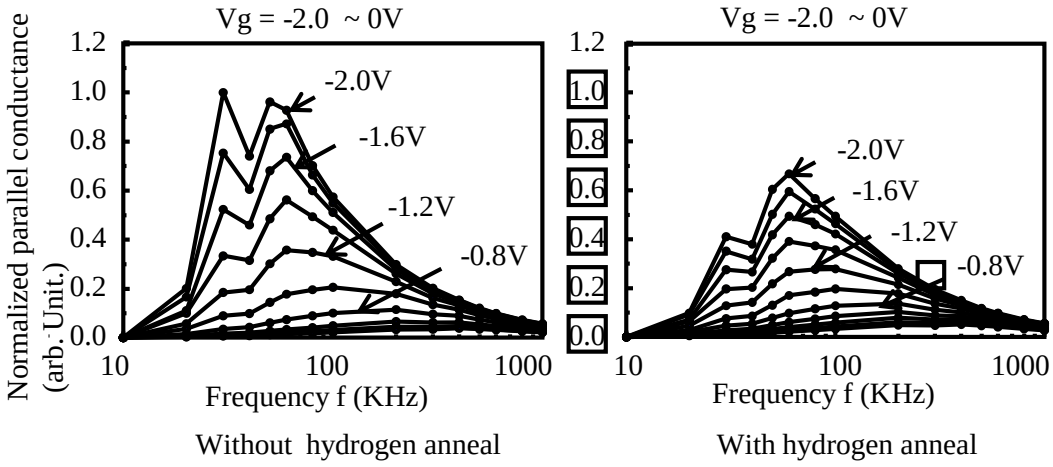

Figure 5-10. Trap reduction by surface treatment for Fin sidewall [4, 6-9].

Surface treatment after Si etching is also important to obtain higher performance of FinFET. They have some process to improve the quality of fin surface such as wet treatment and hydrogen annealing. They and I think hydrogen annealing is the best method for that. Figure 5-8 shows roughness of fin surface. The surface roughness can be improved by the annealing. Dr. Inaba used parallel conductance measurement on fin capacitor to evaluate quality of fin surface with and without hydrogen annealing. Equivalent circuit of the capacitor is shown in Fig. 5-9. I can estimate the quality by the normalized parallel conductance G_p/ω because that is proportional to interface trap density. Figure 5-10 shows the actual measurement results. This slide shows the frequency dependence of parallel conductance with and without hydrogen annealing. The conductance decreases due to the annealing after fin fabrication. This results exhibit the quality of Si surface improvement by the annealing.

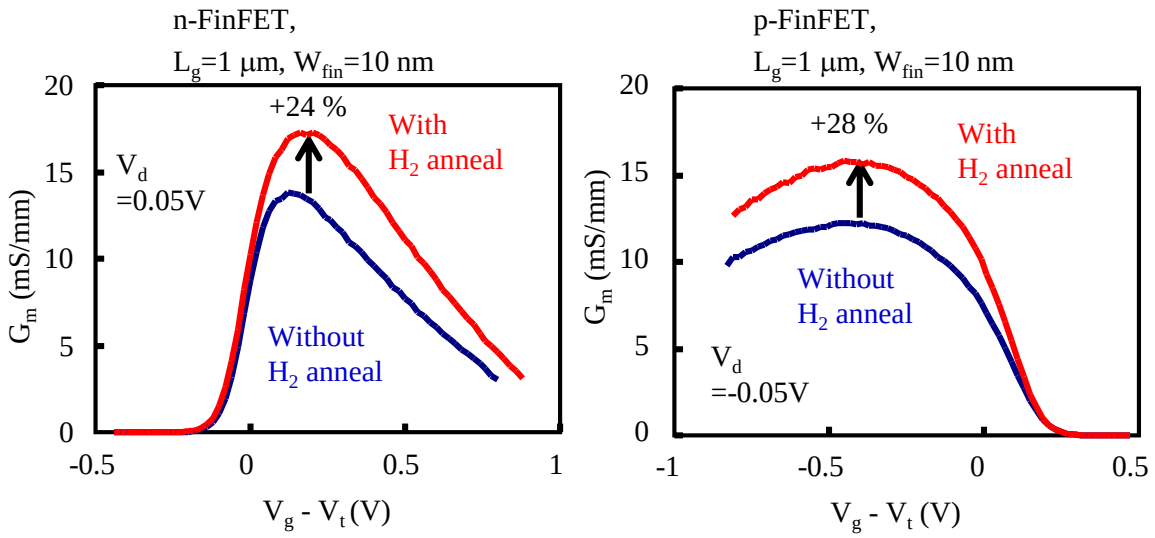

Figure 5-11. Transconductance difference between with and without H_2 annealing [4, 6-9].

5-3. Mixed-signal and RF performance of FinFET

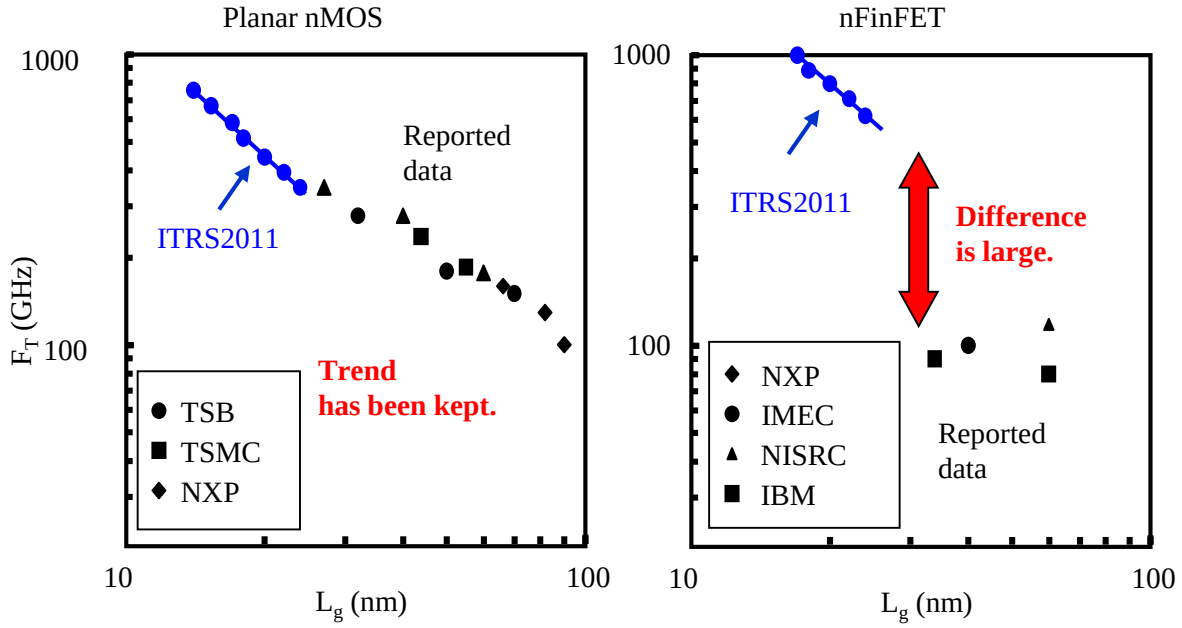

Figure 5-12. L_g dependence of f_T for planar MOSFET and FinFET.

Figure 5-11 shows the effect of improvement of fin surface is shown. As you can see transconductance for NMOS and PMOS are improved. These results show the mobility improved by the hydrogen annealing. Figure 5-12 shows the gate length dependence of f_T for planar and FinFET. In the case of planar MOSFET, the trend of f_T has been kept by the gate length scaling. On the other hand, in the case of Fin FET, the difference between estimation in ITRS road map and actual reported data is large.

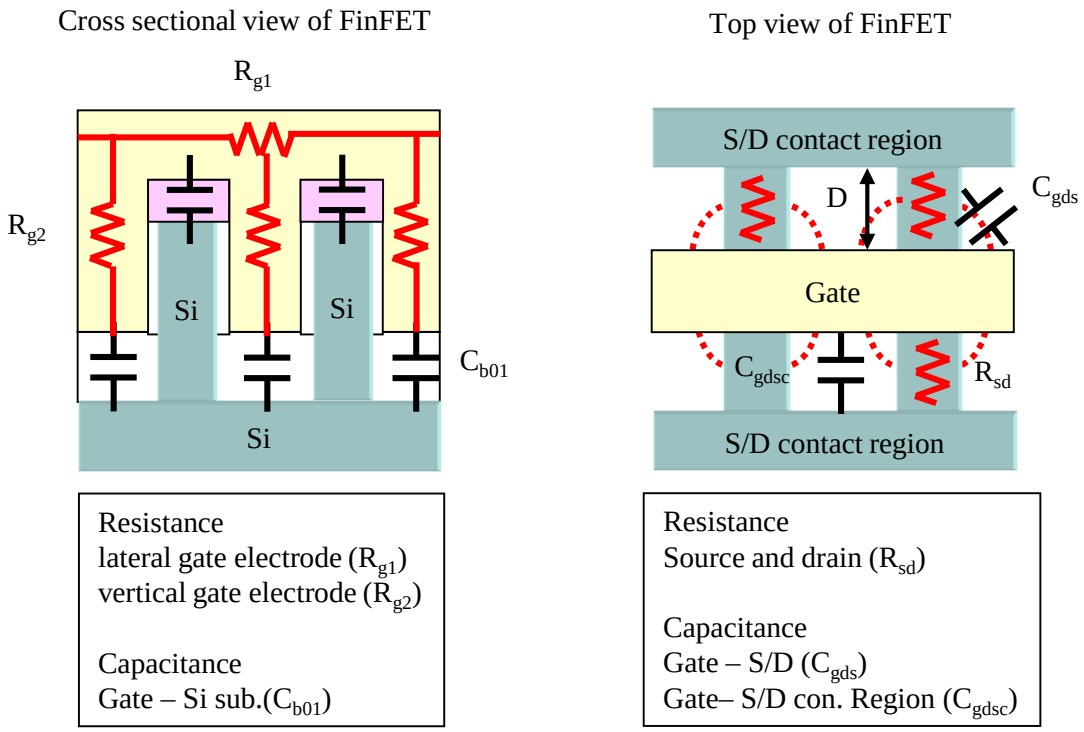

Figure 5-13. Parasitic resistance and capacitance of FinFET.

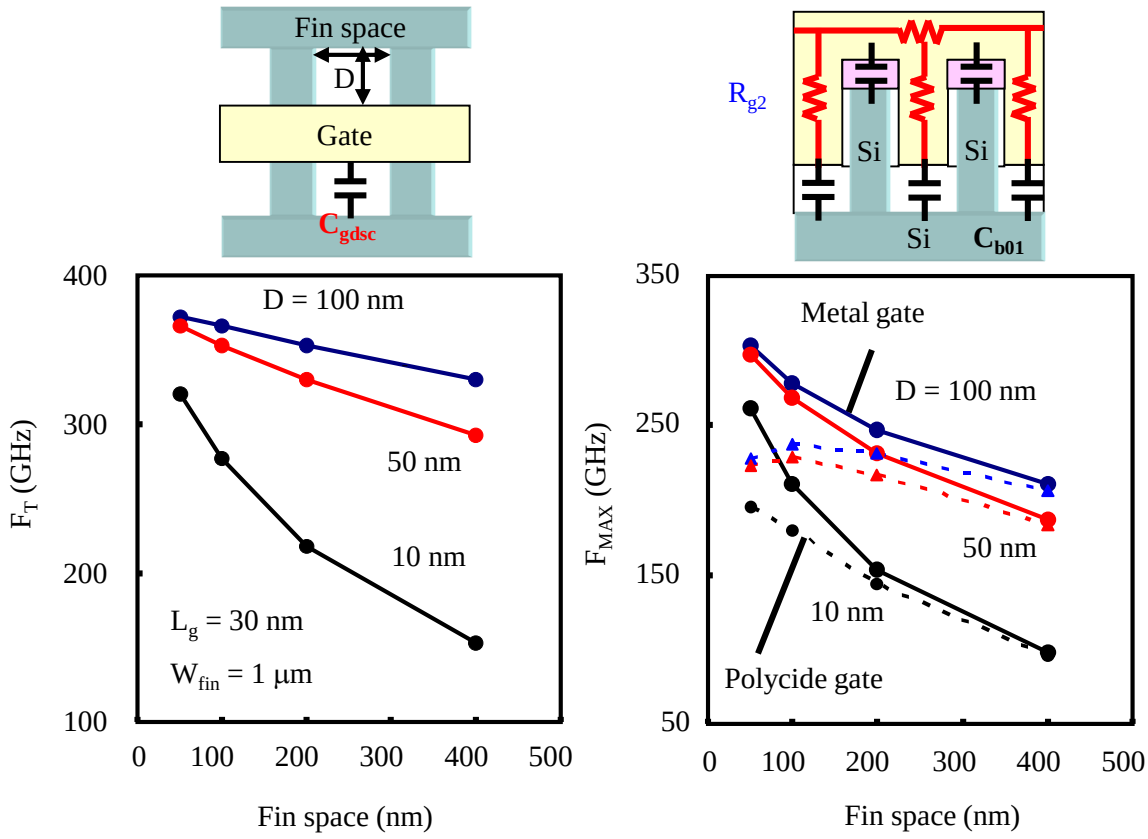

Figure 5-14. Fin space dependence of f_T and f_{MAX}.

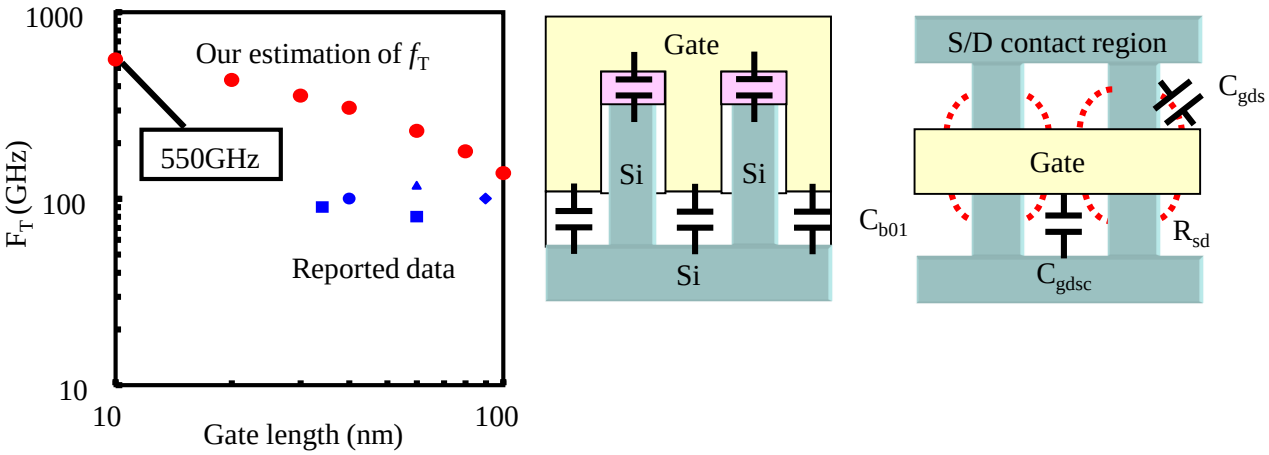

Figure 5-15. F_T of nFinFET with the optimum design.

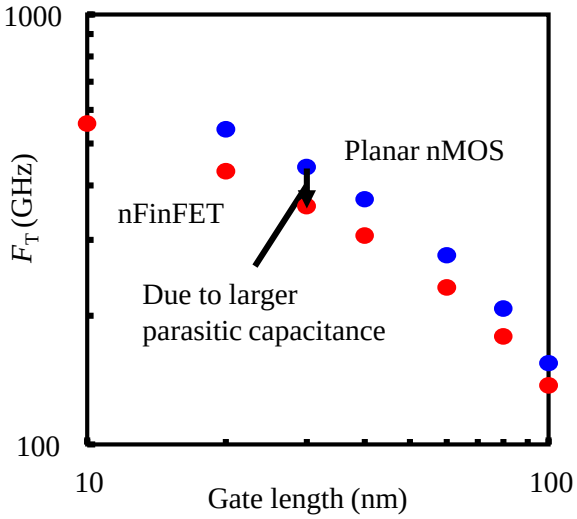

Figure 5-16. Comparison f_T between planar and nFinFET with the optimum design.

In order to analyze the lower f_T of FinFET, I focused on parasitic resistance and capacitance of FinFET. Figure 5-13 shows the parasitic effect of the FinFET. According to our simulation, the most serious capacitance is that between gate electrode and Si substrate through SiO_2 which gate electrode has between Fin and next Fin. Second is the capacitance between gate electrode and source and drain contact region. Figure 5-14 shows fin space dependence of f_T and f_{MAX}. F_T and f_{MAX} increases with reducing fin space because of decrease of parasitic capacitance. We must care the fin FET layout to be reduced the parasitic capacitance in order to obtain higher RF performance. I estimate f_T of nFinFET with the optimum design to be minimum the parasitic capacitance. According to our estimation, 550 GHz can be achieved when the gate length is 10 nm.. Figure 5-16 shows comparison of f_T between planar MOSFET and FinFET. Even f_T value of FinFET with the optimum device layout is lower than planar MOSFET when the gate length is below 20 nm. However, that will exceed planar MOSFET when the gate length is 10 nm.

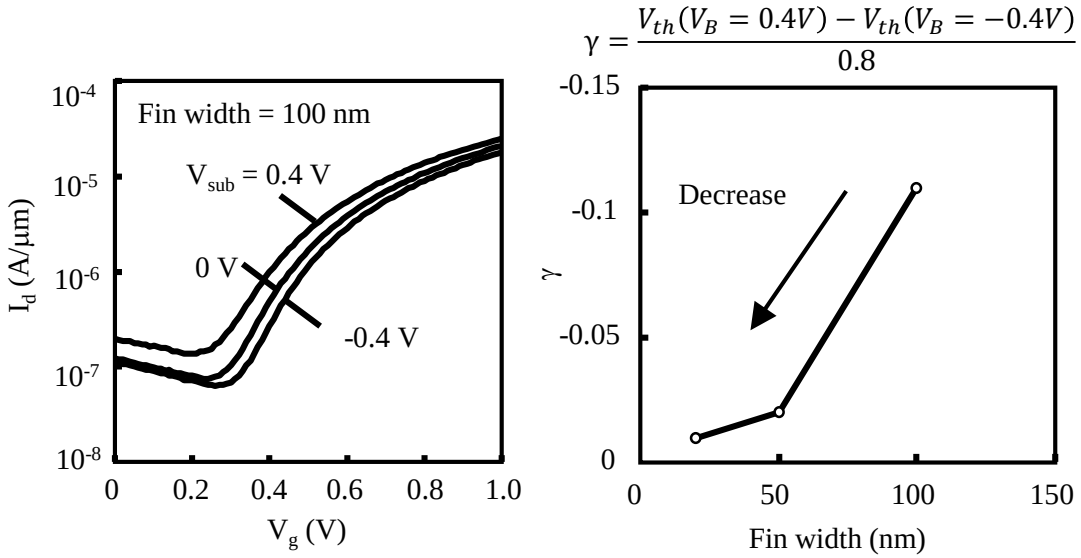

Figure 5-17. Dependence of V_{th} on V_B for Fin width of 20, 50 and 100 nm.

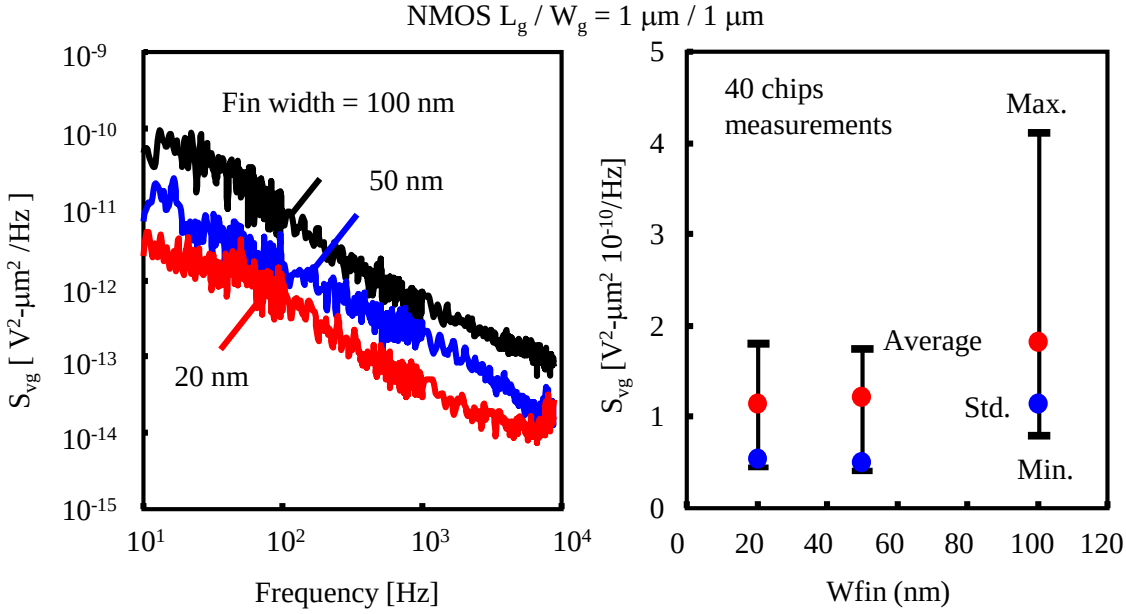

Figure 5-18. Fin width dependence of flicker noise.

Figure 5-17 shows dependence of V_{th} on back bias for fin width of 20, 50 and 100 nm. FinFET has advantage regarding to flicker noise. Figure 5-17 shows fin width dependence of the noise. Both the noise and the variation decrease with scaling fin width. The reason of decreases of the noise is shown in Fig. 5-18. As fin width becomes narrower, the electrical field from channel to gate electrode is relaxed. As a result, the trap probability decreases. This is the reason of lower flicker noise in narrow FinFET.

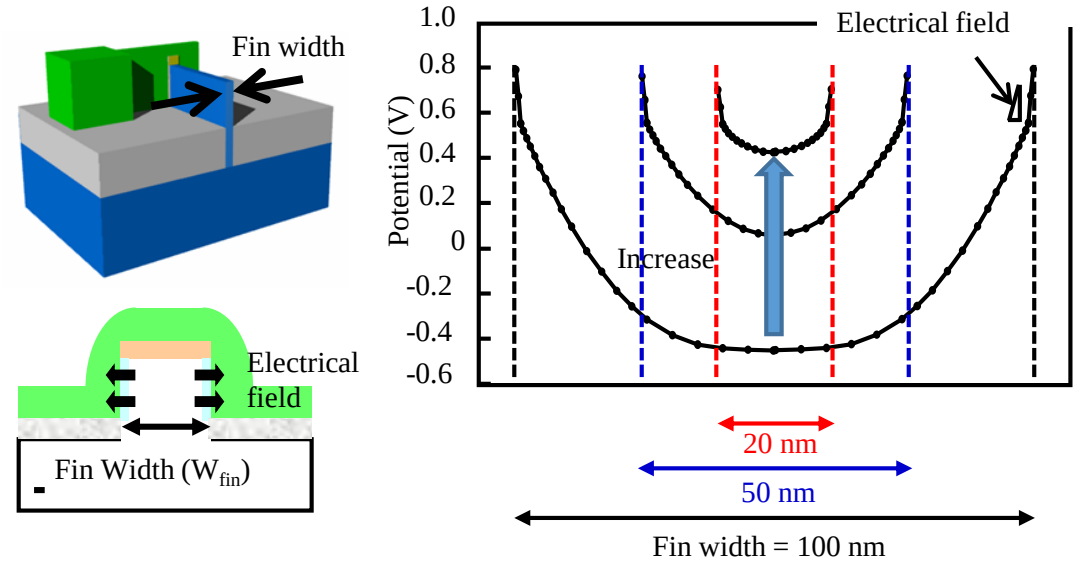

Figure 5-19. Fin width dependence of potential distribution in channel.

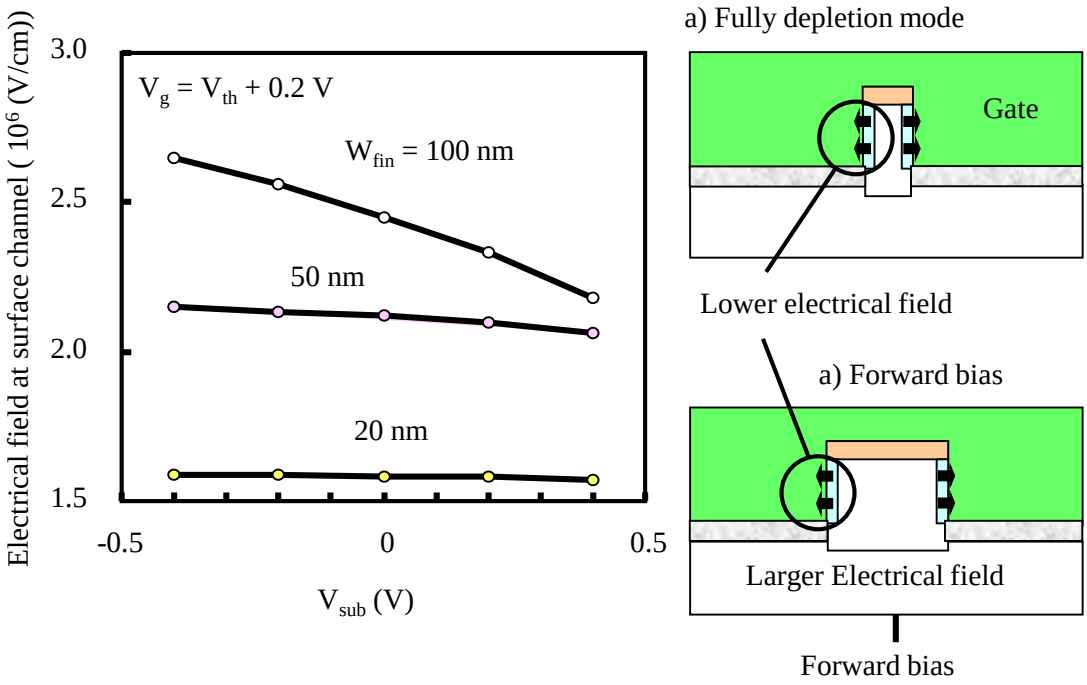

Figure 5-20. Fin width dependence of potential distribution in channel.

Figure 5-19 shows fin width dependence of potential distribution in channel. As the fin width becomes thinner, the potential at center increases and the slope, that is electrical field from channel, decreases. Figure 5-20 shows dependence of the electrical field on substrate bias. When the fully depletion mode, that is almost same and that of 20 nm fin width is 60 % smaller than that of 100 nm fin width.

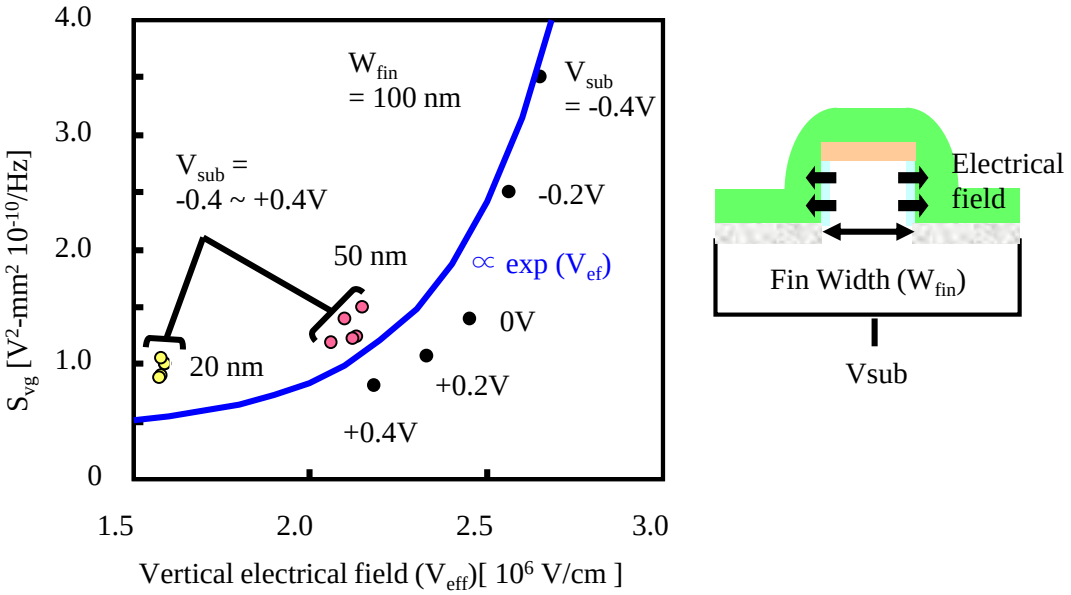

Figure 5-21. Vertical electrical field dependence of 1/*f* noise for nFinFET.

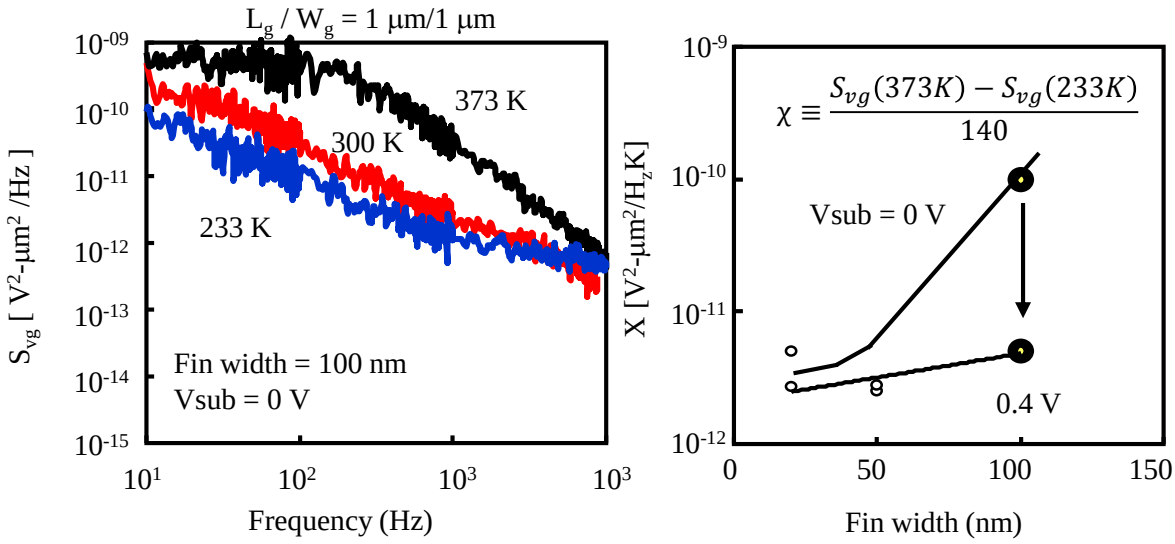

Figure 5-22. Temperature dependence of 1/*f* noise for nFinFET.

Figure 5-21 shows vertical electrical field dependence of 1/*f* noise. The field is calculated by simulation and 1/*f* noise is measurement data. The noise depends on the field significantly. Figure 5-22 shows temperature dependence of 1/*f* noise for nFinFET. The dependence becomes smaller as fin width decreases.

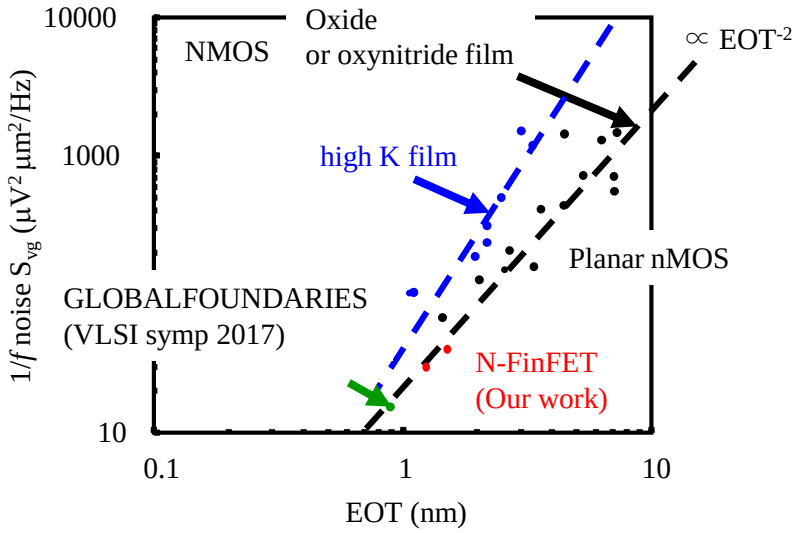

Figure 5-22 Benchmark results of 1/*f* noise of NMOS.

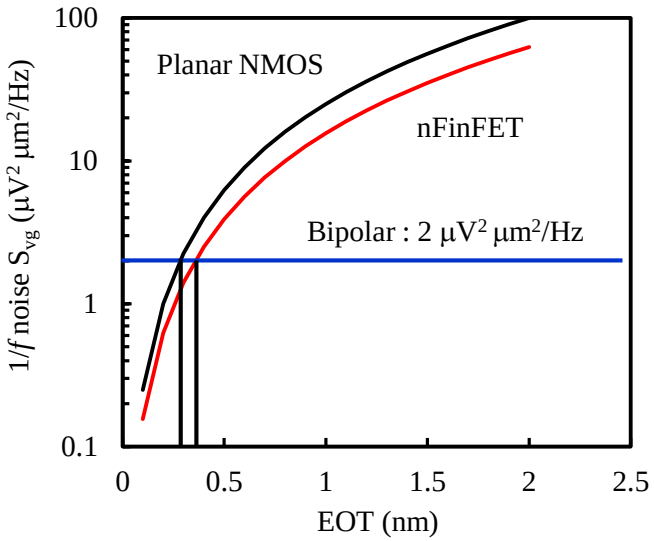

Figure 5-23. Estimation of 1/*f* noise for FnFET and planar MOSFET.

Figure 5-22 shows benchmark results of 1/*f* noise of NMOS. The data reported in J. Singh et al., VLSI symp. 2017 are plotted [23]. This results shows 1/*f* noise of FinFET is lower than that of planar MOSFET, which is agreement with my results.

Figure 5-23 shows estimation of 1/*f* noise for FnFET and planar MOSFET when the noise is in proportional to square EOT. In order to catch up he 1/*f* noise of bipolar, that is 2 $\mu V^2\,\mu m^2/Hz$, 0.35 nm for FinFET and 0.25 nm for planar MOSFET is required. I think it is very difficult to realize ultra-thin EOT. In general, high K material to obtain the thin EOT degrades the quality between Si substrate and gate insulator and becomes worse 1/*f* noise.

Conclusion

In this chapter, fabrication process of FinFET, DC, mixed-signal and RF characteristics are described. Side-wall transfer can realize very narrow line for fin and gate electrode of FinFET. Hydrogen annealing after Si etching is useful for improvement of the mobility and gate insulator quality. This treatment is required for reduction of flicker noise. The FinFET is attractive for high performance digital circuits because short channel effect can be suppressed by fully depletion mode operation in narrow fin structure. Moreover the flicker noise can be reduced with narrower fin width because the electrical field from channel to gate electrode is lower. This results indicate the FinFET is attractive for not only digital but also mixed-signal circuits. However, RF performance is inferior to planar MOSFET due to larger parasitic capacitance between fins. For example f_T of 30 nm gate length FinFET is 350 GHz and the value is corresponding to f_T of 50 nm planar MOSFET. Thus RF circuit designer should chose FinFET or planar structure based on system spec and the production cost.

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Chapter 6
Conclusion and expectation of mixed-signal and RF CMOS

6-1. Conclusion of device structure and process for higher performance of mixed-signal and RF characteristics

Table 6-1. Technology node and some production used our technology.

Tech node.	250nm	180nm	140nm	90nm	65nm	45nm	32nm	22nm
L_g min.	250nm	180nm	110nm	70nm	50nm	35nm	24nm	22nm
Salicide materials	$TiSi_2$	$CoSi_2$		NiSi				
Gate insulator	Pure Ox		Oxynitride			High K		
Digital production	Pentium	Coppermine	Tualatin	Intel processor Prescott	Xeon	Penryn	Clarkdale	Ivy Bridge
MS/RF	Bluetooth			Bluetooth				

Chapter 2. Reduction of resistive component for higher gain of CMOS.

In order to obtain higher f_{MAX} (Power gain) of MOSFET, it is important not only to scale down the gate length but also to reduce the parasitic resistance of the MOSFET. Especially, the lower gate resistance is necessary. Thus the silicide (Self aligned silicide) technology is required for the purpose. This technology has been introduced to CMOS for the digital circuits because the higher drivability and high speed operation can be realized. The issues of that are the increases of sheet resistance with decreasing the gate length due to the agglomeration during silicide process. The silicidation temperature depends on silicide material. For example, Ti, Co and Ni is 750-900 °C, 550-900 °C and 350-500 °C, respectively. I conclude NiSi is the best silicide material because the silicidation temperature is the lowest and Si consumption is the smallest. Actually, the NiSi has been used in CMOS devices beyond 90nm technology.

However, the NiSi has some issues to solve for applying to CMOS devices. That is the anomaly oxidation of NiSi formed on As doped Si substrate and degradation of leakage current of N^+/P junction. The problem can be solved by TiN cap during silicidation process. But even this TIN cap method is incapable of adequately suppressing roughness in the case of recent ultra-shallow source and drain junctions, since the nitride layer is so thin, I propose a nitrogen-doped nickel mono-silicide technique The nitrogen doped NiSi bring the smaller roughness at interface between the NiSi ans Si substrate and lower resistivity.

Table 6-1 shows transition of silicide material and gate insulator for each technology node. The NiSi has been used since 90 nm technology node because of no degradation of sheet resistance. This means NiSi development has large impact for progress of CMOS.

I applied $CoSi_2$ to NMOS used as power amplifier device in order to reduce the resistance of gate, source and drain. A metal gate has been used for the device to obtain higher power gain and f_{MAX} but the metal gate is difficult to realize short gate length due to problem of fabrication process. Thus, I used poly Si which is easy to realize short gate length. Though the resistivity of $CoSi_2$ is higher than that of metal gate, I reduced the gate resistivity by short finger length. As a result, I obtained 50% power efficiency at 2GHz operation. This result indicates Si MOS power amplifier can be integrated with mixed-signal, RF and digital circuits on the same chip. For additional reducing gate resistance, I used epitaxial technology because I can form T-shape gate electrode after growing selective epitaxial Si on poly Si gate. As a result, f_{MAX} of 70 GHz was achieve by Co silicided T-shaped gate at 0.1 μm gate length, while f_{MAX} of 55 GHz in the case without T-shaped gate. The epitaxial Si technology is useful for not only higher power gain but also higher drivability, improvement of V_{th} matching and lower 1/*f* noise because MOSFET with low concentration epitaxial Si channel realize low channel concentration and lower interface density between the epitaxial Si channel and gate insulator.

Chapter 3. Reduction of 1/*f* noise of CMOS.

In order to reduce of 1/*f* noise which is important for not only mixed signal such as VCO circuit but also the jitter of digital circuits. Beyond 250 nm technology node, the oxynitride film involving nitrogen is required to gate insulator for the suppression of boron penetration to Si substrate in surface type PMOS. The nitrogen profile is important to decrease the 1/*f* noise.

In the case of NO gas annealing process, the nitrogen is piled up at the interface between oxynitride and Si substrate. On the other hand, in the case of plasma nitridation process, that is piled up at the interface between oxynitride and gate electrode. The difference of the nitrogen profile causes the difference of the interface state density (D_{it}) at oxynitride and Si substrate. In plasma nitridation , the D_{it} is lower than that of NO gas annealing case. As a results, the plasma nitridation process is suitable for mixed-signal and RF circuits because of lower 1/*f* noise. In the case of NO gas annealing process, buried channel MOSFET is useful to reduce the noise because carrier path is away from the interface and the trap probability decreases. And according to our experiments, deuterium annealing is effective to reduce the noise for PMOS in the NO gas annealing case. Though the STI process has been used for device isolation since 250 nm, I must care defect and stress at STI edge which cause degradation of the 1/*f* noise. The noise depends on the distance between gate electrode and STI edge, and the finger length of MOSFET. When the distance between gate electrode and STI edge is smaller than 0.5 μm, the noise itself and the variation become larger. Especially, the degradation of PMOS is larger than that of NMOS because of larger mobility fluctuation. Thus we should care the MOSFET layout to suppress the noise degradation. And when the finger length is below 1.0 μm, the noise increases because the ratio of drain current flowing near the STI edge. I confirmed the degradation due to the higher interface density near STI edge by using simulation. This result also means we should care the finger length in mixed-signal and RF circuits design. On the other hand, smaller finger length is required for higher power gain and f_{MAX} because of lower gate resistance. According to our estimation, the optimum finger length to obtain the maximum of f_{MAX} is beyond 1.0 μm till 35 nm gate length. However, when below the 35 nm gate length, we must reduce gate resistance to suppress the degradation of the 1/*f* noise.

Chapter 4. Si substrate engineering for higher performance of mixed-signal and RF characteristics.

For obtaining higher RF performance, Si substrate engineering is also useful. For example, high resistivity substrate can reduce eddy current for inductor and we can obtain higher Q value. But the substrate has some problem which are slip occurrence during STI stress, higher leakage current between Nwells, lower latch-up voltage and larger noise figure. In order to solve slip, we showed Fully oxygen precipitated wafer with high resistivity (FOP) was required. And for higher leakage current and lower latch-up, we can suppress those by additional ion implantation.

For larger noise figure, metal layer under signal PAD is useful method because the thermal noise cause by signal in the high resistivity substrate. The metal layer with low resistivity reduce the noise even in the case of high resistivity substrate. The thin Si substrates is required for high density 3D stacked chips realization. The substrate is attractive for RF circuits too. Because that realizes lower substrate noise , lower thermal noise with latch-up free in the case without additional ion implantation used in high resistivity Si substrate. The effect to reduce substrate is larger than that using deep Nwell. The problem is degradation of Q value for inductor due to larger eddy current on the metal which is in other chip under RF chip when RF and digital is stacked. In order to suppress the current, permalloy film (NiFe) is effective because the metal shields magnetic field. The optimum thickness is 10 nm because too thickness cause the degradation of Q value due to eddy current on the permalloy film.

According to comparing results between high resistivity Si substrate and the ultra-thin Si substrate, 725 μm high resistivity substrate is suitable for high Q inductor, but thermal noise, Nwell leakage current and latch up are degraded. In order to solve these problems, additional process are needed. On the other hand, ultra thin substrate with normal resistivity is better except Q value of inductor. The Q value degradation is easily suppressed by thin permalloy film deposition on backside of chip. Because the thin wafer is required for high density 3D stacked chip, I conclude this thin substrate is suitable than high resistivity substrate for future system in package.

The issue of CMOS in ultra-thin Si substrate such as 1.7 μm is layout dependence of the characteristics. This is serious problem for circuits designers. Thus, we must continue to study and develop new technology to resolve this issue.

Chapter 5. Mixed signal and RF characteristics of FinFET

FinFET is already production level for MOSFET with gate length below 30 nm. The is attractive for digital circuits because of higher gate density. The thin fin structure reduce the electrical field from channel to gate electrode because the device operates in fully depletion mode when the fin width is below 50 nm. The lower field reduce 1/*f* noise because the provability of trapped and de-trapped of carrier becomes lower. Basically, higher interface density between Si substrate and gate insulator is concerned because Si substrate is etched. In order to improve the interface quality, hydrogen annealing is useful.

This process is needed for not only higher drivability and higher transconductance but also lower 1/*f* noise. These results are attractive for base band which has both digital and mixed signal circuits. However the FinFET has poorer about RF performance comparing with planar MOSFET because the FinFET has larger parasitic capacitance between the devices when we use finger structure. F_T of 30 nm gate length FinFET is 350 GHz and the value is corresponding to f_T of 50 nm planar MOSFET.

For future mixed-signal and RF circuits, it will be necessary to divide chip for base band chip involving digital and mixed-signal circuits and RF circuits. FinFET is useful for baseband to be required high gate density and lower 1/*f* noise. On other hand, planar MOSFET is useful for RF circuits because that is better performance and lower cost than FinFET. If the performance of planar MOSFET is acceptable, the MOSFET is attractive for the production.

In order to realize the system with baseband and RF, 3D stacked chip is required. According to my study, the substrate noise and thermal noise become lower by thinning Si substrate. The thin Si substrate is suitable for 3D stacked chip because TSV process is easier to apply the substrate. Thus I believe my study described in this thesis will been useful for near future.

6-2. Feature of high density 3D stacked chip with many functions

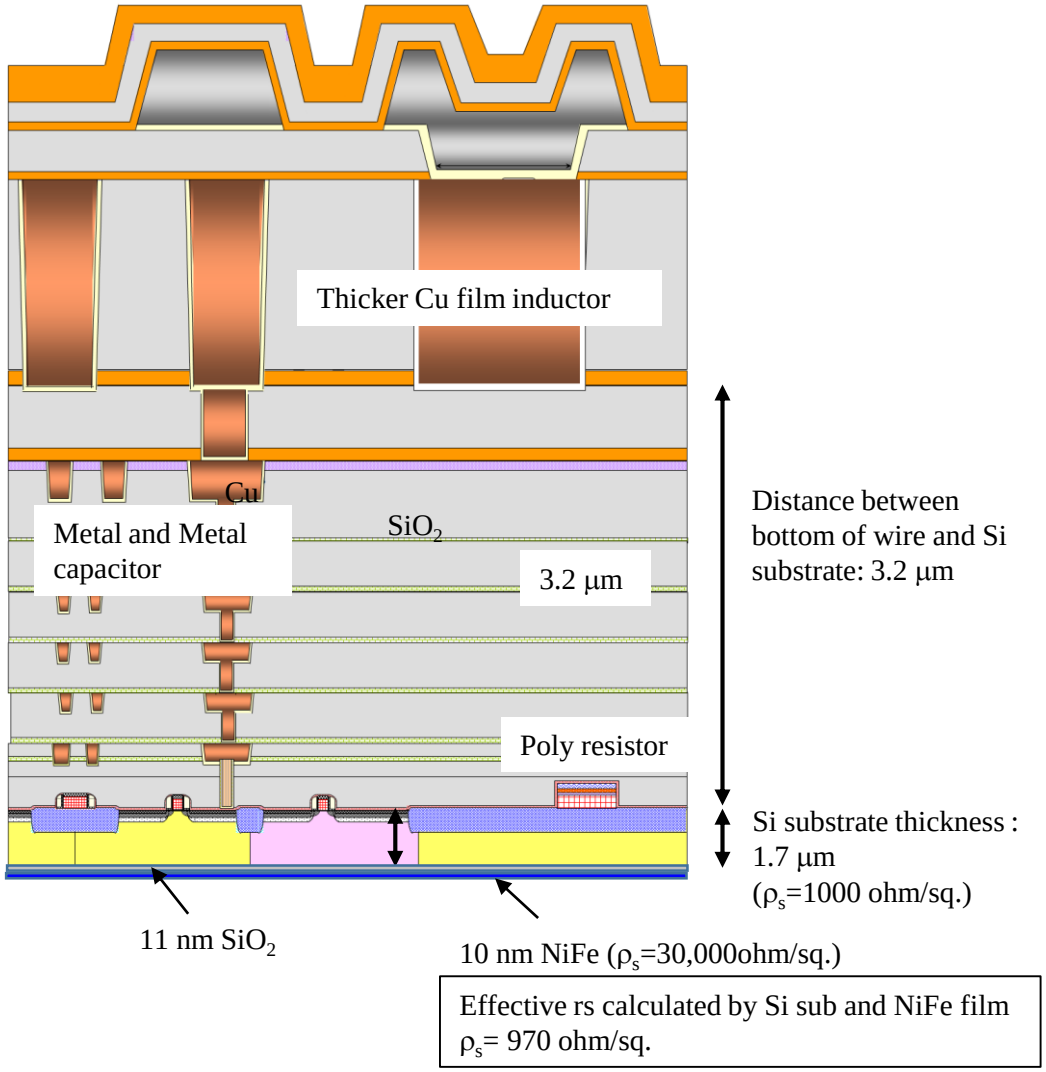
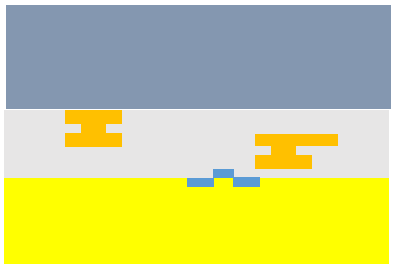


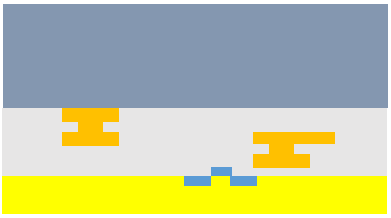
Figure 6-1. Schematic cross sectional view of CMOS devices on thin Si substrate with permalloy film.

In future, 3D stacked chips will be popular for realization of system on package (SOP) with various functions. In that case, coupling between wires degrades Q value of inductor. In order to suppress the degradation, permalloy film will have important role for RF circuits.

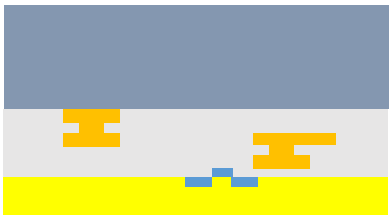
1. MOFET and Cu connect fabrication



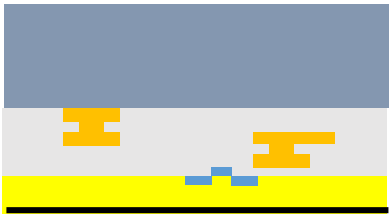
2. Joining with support substrate



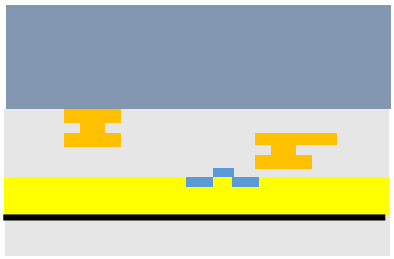
3. Wafer thinning by grinding, dry etching and CMP



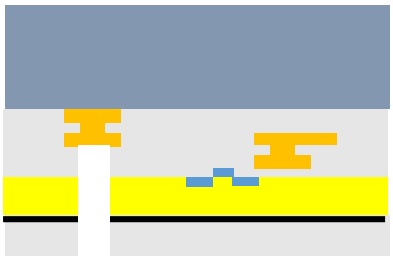
4. Thin SiO_2 (20 nm) deposition by plasma process



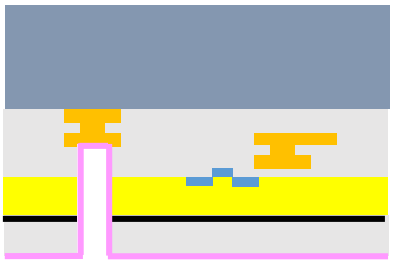
5. Thin permalloy film (NiFe) 10nm deposited by sputtering



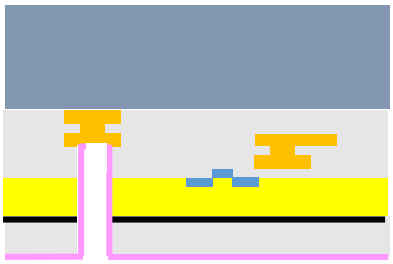
6. Thin SiO_2 (20 nm) deposition by plasma process



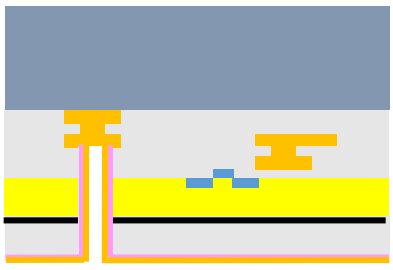
7. Hole fabrication



8. Insulator(SiO_2 or Si_2N_3) deposition

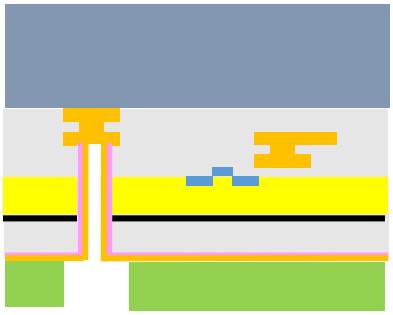


9. Etching of bottom of hole

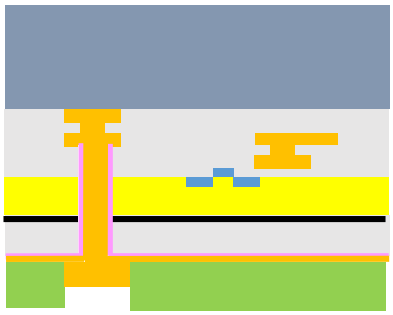


10. Barrier metal and Cu seed metal sputtering

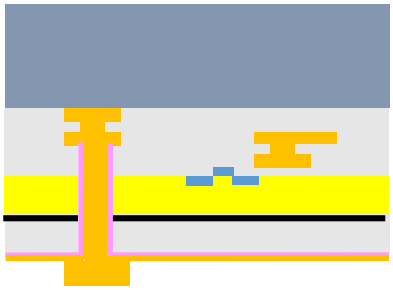
Figure 6-2a). Process flow of 3D stacked chip for ultra-thin chip with permalloy film.



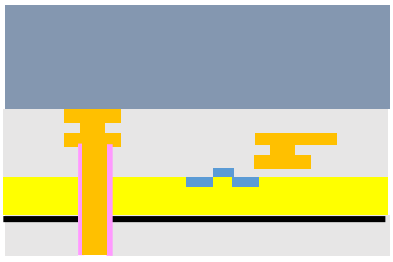
11. Lithography for Cu plating patterning



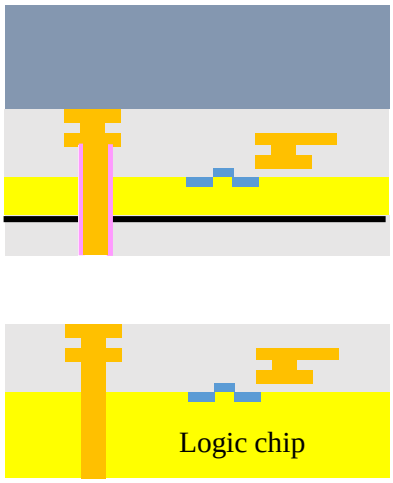
12. Cu plating patterning



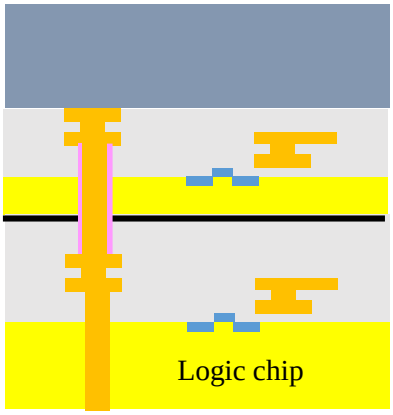
13. Removal of resist



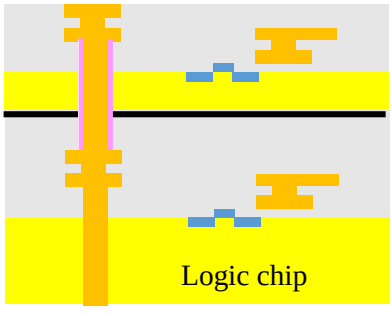
14. CMP process



15. Logic chip with TSV



16. Cu-Cu direct joining



17. Removal of support substrate

Figure 6-2b). Process flow of 3D stacked chip for ultra-thin chip with permalloy film.

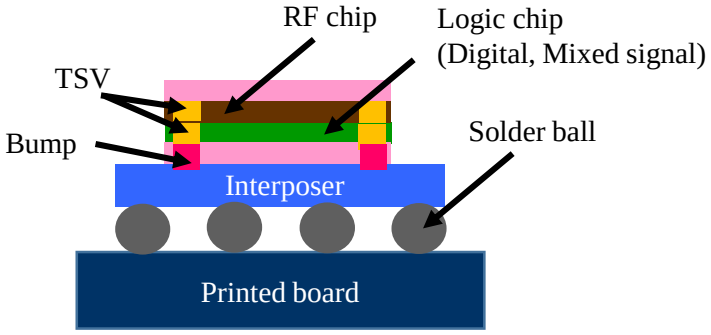


Figure 6-3. Ultra-thin chip with permalloy film and logic chip in a package.

Figure 6-1 Schematic cross sectional view of CMOS devices on thin Si substrate with permalloy film. Top metal is thicker Al or Cu which is used for high Q inductor. The distance between the inductor and Si substrate is just 3.2 μm. Thus, permalloy film (NiFe) is required to shield magnetic field during current flowing in inductor because inductor outer length is beyond 150 μm, according to my study, the Q value degrades when the distance between bottom of the inductor and metal is within the outer length. . Though the permaloy film is metal, the substrate noise degradation is negligible because the sheet resistance is extreme high such as 30 Kohm/sq. in 10 nm thickness comparing with 1 Kohm/sq. of Pwell in 1.7 μm Si substrate.

Figure 6-2 shows Process flow of 3D stacked chip for ultra-thin chip with permalloy film Firstly, MOSFET and Cu connect fabrication on normal Si substrate. Then joining this wafer with support substrate for wafer thinning. The thinning process is grinding, dry etching and CMP. After Si wafer thinning to 1.7 μm, thin SiO_2 is deposited by plasma process, which process temperature is below 300 °C . Then, permally film is deposited by sputtering. Next is thin SiO_2 deposition again. Then, hole fabrication and thin insulator film is deposited in order to prevent to connect permalloy film and barrier metal used in Cu plating process. After etching of bottom of hole, barrier metal and Cu seed is deposited by sputtering. The barrier metal suppress the diffusion of Cu. Then lithography for Cu plate patterning is carried out and Cu film is plated. After removal of resist, finally CMP process is carried out in order to make bottom surface of chip flat. In order to join another chip such as logic chip with TSV, direct joining process for Cu and Cu is used.

Figure 6-3 shows Ultra-thin chip with permalloy film and logic chip in a package. Top is RF chip and bottom is logic chip in order to suppress inductor Q value due to coupling between inductor and interposer.

3D stack with ultra-thin chip with permalloy film will be possible for high density SOP in near future.

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