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著者(和文)	SHAFIQFARHAN
Author(English)	Farhan Shafiq
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論 文 要 旨

THESIS SUMMARY

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学生氏名： Student's Name	FARHAN SHAFIQ	指導教員（主）： Academic Advisor(main)	一色　剛
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Accurate and fast performance estimation methods for modern and future multi-core systems are the focal point of much research due to the complexity associated with such architectures. Specially with the slowing down of the Moore's law, the focus turns to multi-core and multi-processor architectures. Such multi-processor architectures require parallel software applications to efficiently harness the computation power of the processors. The communication architecture of such systems has a huge impact on the performance and power of the whole system. Architects need to explore many design possibilities by using performance estimation techniques at early stages of design to make design decisions earlier in the design cycle. While software developers need to develop and test applications for the target architecture and gather performance measurements as early in the design cycle as possible. However, there is a huge gap between the growth trends of software complexity and growth trends of software design productivity. Hence better and more efficient design automation tools are required to fill this gap. Full system simulation techniques provide accurate performance values but are extremely time consuming and require a lot of development work. Static analysis techniques are fast but cannot capture the dynamic behavior associated with shared resource contention and arbitration. Moreover, synthetic traffic patterns have been used to analyze the communication architecture however, such patterns are not realistic enough and usually application dependent. In this research we propose a statistical based model to predict the performance cost of bus arbitration on the performance of a bus architecture. The proposed model uses workload trace of the actual applications to capture the real application traffic behavior. Statistics on the traffic patterns are collected and used as input to the analytical model which calculates performance values for the communication architecture under consideration. The mathematical model is developed using actual histograms of the application traffic which ensures estimation of accurate performance values for each specific application. By knowing the performance measures, designers can avoid over and under-design of the communication architecture. Moreover, it also provides bus-aware application performance measures in order to optimize application design for better bus performance. This research presents bus models capturing single-blocking, burst bus-transfers, and multi-blocking bus behaviors. Single Blocking Model (SBM) captures single interfering bus masters for each bus request at a time, Burst Blocking Model (BBM) captures multiple back-to-back bus transfers on a single interfering bus masters for each bus request at a time while Multi Blocking Model (MBM) captures
multiple bus transfers on multiple interfering masters for each bus request at a time. Performance estimation experiments are performed for multiple benchmarks using two different architectures i.e. four processing elements connected via a shared bus and eight processing elements connected via a shared bus. Recorded traffic from real benchmark applications namely; "ROBOT" which is a Newton-Euler dynamic control calculation for 6-degrees-of-freedom Stanford manipulator, "SPARSE" matrix solver Random sparse matrix solver for electronic circuit simulations, "FFT-1024-complex" which is a Fast Fourier Transform application with 1024 inputs of complex numbers, "SPEC95 FPPPP" which is a chemical program performing multi-electron integral derivatives. The estimation results are compared against a simulation based estimation technique for accuracy and speed. The Single Blocking Model (SBM), Burst Blocking Model (BBM) and Multi-Blocking Model (MBM) vary in complexity and accuracy. For most low traffic applications, SBM is able to exhibit high accuracy with estimation errors up to 0.2% however as burst traffic and number of Processing elements increase SBM starts to show more error up to 10%, while using BBM, the accuracy is maintained. Moreover, As the number of processing elements increases and applications become traffic intensive, MBM shows higher accuracy compared to BBM.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
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