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A Transformerless D-STATCOM Based on a Multi-Voltage Cascade Converter Requiring No DC Sources

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Abstract

This paper deals with a cascaded multilevel converter which has multiple dc voltage values (multi-voltage cascade converter, or hybrid multilevel converter) for a 6.6-kV transformerless distribution static synchronous compensator (D-STATCOM). A control method is proposed to realize dc voltage regulation of series-connected multiple cells in the STATCOM operation, making it possible to remove dc sources from all H-bridge cells. The simplified configuration without the dc sources makes the STATCOM small and lightweight. A downscaled STATCOM model rated at 220 V and 10 kVA is built and a series of verification tests is executed. Theoretical analysis and experimental results prove the stable operating performance of the proposed method in steady states and transient states.

Index Terms

Cascaded multilevel converter, dc voltage control, silicon carbide device, STATCOM, transformerless converter.

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A Transformerless D-STATCOM Based on a Multi-Voltage Cascade Converter Requiring No DC Sources

I. Introduction

In recent years, installed capacity of distributed generations such as residential photovoltaic systems is increasing. They are often connected to the distribution grid. Since their output power is affected by solar irradiance, the power flow may fluctuate and be bidirectional in the grids. As a result, voltage management of the grids may become difficult in the area where photovoltaic systems are densely installed [1].

The STATCOM (static synchronous compensator) is a vital solution to maintain grid voltages by supplying or consuming reactive power. It has been installed in the transmission grids, and its use is spreading to the medium voltage distribution grids as a D-STATCOM (distribution STATCOM). The existing D-STATCOM is equipped with a step-down transformer and an ac filter. In this case, the transformer and the filter inductors make the STATCOM bulky and heavy. For example, the weight of a prototype D-STATCOM rated at 360 kVA was 3,000 kg [2]. It is estimated that its transformer weighs 1,000 kg, and its ac inductors weigh 400 kg. Therefore, further reduction of volume and weight is required for the practical installation in the urban area.

Cascaded multilevel converters have been studied to realize a small and lightweight STATCOM [3], [4]. A single-phase full bridge or "H-bridge" inverter is a fundamental building block and it is called as a "cell." The identical cells are connected in series and the string composes a cascaded multilevel converter (called as "single-voltage cascade converter" in this paper). Since the cascade converter realizes high blocking voltage and low-harmonic output voltage, it needs no step-down transformers for medium voltage applications.

A cascaded multilevel converter which has more than two types of cells with different rated voltages (multi-voltage cascade converter, or hybrid multilevel converter) has been proposed in [5]–[7]. Different cells whose dc voltage ratio is typically 2:1 or 3:1 are connected in series and controlled together to compose low-harmonic output voltage. It can reduce voltage harmonics comparing to the single-voltage cascade converter with the same number of cells.

On the other hand, the multi-voltage cascade converter has difficulty in maintaining the dc voltage ratio to the predetermined value. Although it is confirmed that the dc sources consisting of isolated power supplies are effective to keep the dc voltages [5]–[7], the method needs power supplies in all cells and makes its configuration complex. The power supplies requiring high voltage isolation also makes the converter bulky. However, the dc sources are not essential for a STATCOM application. Control methods have been proposed to remove some dc sources by utilizing redundant switching patterns [8] and all power supplies by disabling the PWM control [9], which may

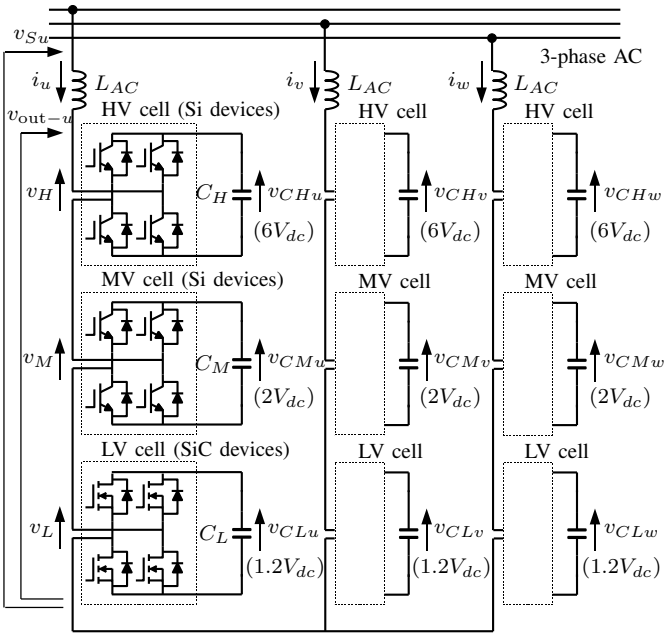


Fig. 1. A STATCOM based on a multi-voltage cascade converter.

increase some amount of output voltage harmonics.

This paper proposes a new dc voltage control method for the multi-voltage cascade converter. The control method realizes energy transfer between the series connected different cells during STATCOM operation. Combining with feedback controller, it can maintain all dc voltages to the predetermined reference value without dc sources. A downscaled STATCOM model rated at 220 V and 10 kVA is built and a series of verification tests is executed. Theoretical analysis and experimental results prove the stable operating performance of the proposed method in the startup, steady states, and transients under voltage sags.

II. Multi-Voltage Cascade Converters

A. System Configuration

Fig. 1 represents a circuit configuration of multi-voltage cascade converters. The converter consists of three clusters with star configuration, and each of the clusters consists of three series connected H-bridge cells which have different dc voltages from each other. These cells are described as "HV (high voltage) cell", "MV (medium voltage) cell", and "LV (low voltage) cell" in descending order of their dc voltages. The cells having higher dc voltage share larger conversion power with lower switching frequency. There are some options in the dc voltage ratio among v_{CHy}, v_{CMy}, and v_{CLy} (subscript y is either u, v, or w) . One typical ratio is $v_{CHy} : v_{CMy} : v_{CLy} = 4 : 2 : 1$ [5], [8]–[10], and other ratios such as $9 : 3 : 1$ and $6 : 2 : 1$ are also investigated in [11]–[13]. $v_{CHy} : v_{CMy} : v_{CLy} = 6 : 2 : 1$ is an optimum dc voltage ratio to obtain maximum output voltage levels under PWM operation of LV cells [12]. Based on the optimum ratio, the dc voltage ratio in this paper is set to $v_{CHy} : v_{CMy} : v_{CLy} = 6 : 2 : 1.2$, where

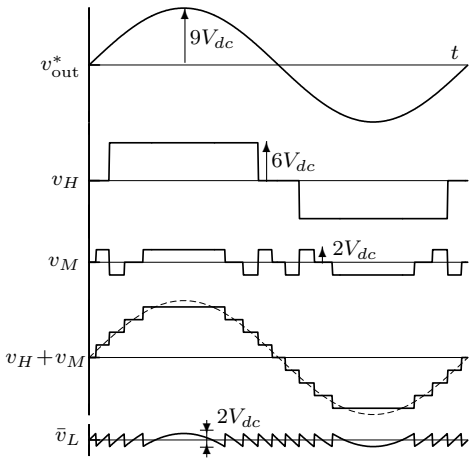


Fig. 2. Output voltage waveforms of each cell in the multi-voltage cascade converter whose dc voltage ratio is $6:2:1.2$.

v_{CLy} is increased by 20% in order to apply a control method proposed in this paper. The reference of dc voltages are v^*_{CHy} = $6V_{dc}$, v^*_{CMy} = $2V_{dc}$, and v^*_{CLy} = $1.2V_{dc}$ using unit dc voltage V_{dc}. V_{dc} is set to 0.6 kV for 6.6-kV utility and industrial distribution systems, and each dc voltage is v_{CHy} = 3.6 kV, v_{CMy} = 1.2 kV, and v_{CLy} = 0.72 kV. Then HV, MV, and LV cell can be composed of power devices rated at 6.5 kV, 2.5 kV, and 1.2 kV in blocking voltage, respectively. The LV cells operating with PWM can increase their switching frequency or reduce their switching loss by applying up-to-date 1.2-kV SiC-JFET [14] or SiC-MOSFETs [15], [16].

B. Output Voltage Synthesis

As well as single-voltage cascade converters, the multi-voltage cascade converter operates each of the clusters as a single-phase converter, and three clusters together as a three-phase converter. Therefore, its control method above the cluster level is the same as the single-voltage cascade converters.

On the other hand, output voltage synthesis in a cluster is characteristic to the multi-voltage cascade converter because the output pulses of the HV, MV and LV cells have different amplitudes. The control method discussed in this and next section is independently applied to each of the clusters. Therefore, all variables mean the value for the same phase and their subscript y is removed for simplicity.

Fig. 2 shows the output voltage waveforms of each cell with a nearest level modulation [13]. The output voltage reference $v^*_{\rm out}$ is a sinusoidal waveform whose amplitude is less than $9V_{dc}$. The output voltage of HV cell v_H and that of MV cell v_M are selected to make their total value $v_H + v_M$ be a nearest to $v^*_{\rm out}$. Then the HV cell outputs one positive and one negative pulses, and the MV cell outputs five positive and five negative pulses during a cycle. The mean output voltage of LV cell $\bar{v}_L$ outputs the remainder of $v^*_{\rm out}$, and it is given as follows:

$$\bar{v}_L = v^*_{\rm out} - v_H - v_M. \tag{1}$$

The LV cell outputs $\bar{v}_L$ in average with high frequency PWM. Then $\bar{v}_L$ exists in the following range:

$$-V_{dc} \leq \bar{v}_L \leq V_{dc}. \tag{2}$$

C. Dc Voltage Imbalance and Conventional Solutions

An ideal STATCOM does not supply/consume active power because output voltage $v_{\rm out}$ and output current i are in quadrature. Also in the each cell level, the mean values of dc voltages v_{CH}, v_{CM}, and v_{CL} do not change in the ideal condition. However, in reality, the dc voltages vary when some amount of active power flows into the converter to compensate its power loss. The active power is non-linearly distributed to each cell according to the voltage modulation index, which causes the dc voltage imbalance in the multi-voltage cascade converter [13]. Transient non-periodic current and variation of device characteristics may also cause the dc voltage imbalance.

Dc sources consisting of isolated power supplies can maintain the dc voltages when they are connected to all dc capacitors [5]–[7]. However, the dc sources need high voltage isolation among themselves and bidirectional power flow, making the converter bulky. The number of the dc sources can be reduced by applying novel modulation strategies to series connected two cells [17]–[19] and three cells [20] for motor drive and renewable energy applications. For STATCOM applications, the number of the dc sources can be reduced to three by utilizing redundant switching patterns [8]. All dc sources can be removed by increasing redundant switching patterns in case the PWM is not used [9], which may increases low order harmonics comparing to the PWM method.

III. A Proposed Output Voltage Synthesis and Energy Transfer Control in a Cluster

The proposed control method in this paper realizes energy transfer among HV, MV, and LV cells under PWM control with synthesizing low-harmonic output voltage. The control enables the voltage balancing of the dc capacitors C_H, C_M, and C_L together with voltage feedback controllers described in the section IV, resulting in requiring no dc sources.

Table I shows the output voltages of each cell in a multi-voltage cascade converter. According to the output voltage reference $v^*_{\rm out}$, the voltages v_H, v_M, and v_L are selected from nine combinations. Parameters $\Delta V'_{HM}$, $\Delta V'_{HL}$, and $\Delta V'_{ML}$ influence the boundary levels to switch the output voltages, making it possible to transfer the energy among C_H, C_M, and C_L in the same cluster. When $\Delta V'_{HM}$, $\Delta V'_{HL}$, and $\Delta V'_{ML}$ are set to zero, the control is the same as the conventional nearest voltage modulation transferring no energy among C_H, C_M, and C_L.

A. Energy Transfer between Two Cells

1) Energy Transfer between the HV Cell and the LV Cell: It is assumed that a cluster operates as a single-phase STATCOM and its output voltage reference $v^*_{\rm out}$ and output current i are the following sinusoidal waveforms.

$$v^*_{\rm out} = 9V_{dc} \sin \omega t \tag{3}$$

$$i = I \cos \omega t, \tag{4}$$

where $9V_{dc}$ and I are the amplitude of $v^*_{\rm out}$ and i.

TABLE I

OUTPUT VOLTAGE OF EACH CELL IN THE MULTI-VOLTAGE CASCADE CONVERTER WHOSE DC VOLTAGE RATIO IS $6:2:1.2$.

Condition of the output voltage reference $v^*_{\rm out}$	v_H	v_M	$\bar{v}_L$
$7V_{dc}-\Delta V'_{HM}+\Delta V'_{ML} \le v^*_{\rm out} < 9V_{dc}$	$6V_{dc}$	$2V_{dc}$	$v^*_{\rm out}-8V_{dc}$
$5V_{dc}+\Delta V'_{HL}+\Delta V'_{ML} \le v^*_{\rm out} < 7V_{dc}-\Delta V'_{HM}+\Delta V'_{ML}$	$6V_{dc}$	0	$v^*_{\rm out}-6V_{dc}$
$3V_{dc}+\Delta V'_{HM}+\Delta V'_{HL} \le v^*_{\rm out} < 5V_{dc}+\Delta V'_{HL}+\Delta V'_{ML}$	$6V_{dc}$	$-2V_{dc}$	$v^*_{\rm out}-4V_{dc}$
$V_{dc}+\Delta V'_{HL}+\Delta V'_{ML} \le v^*_{\rm out} < 3V_{dc}+\Delta V'_{HM}+\Delta V'_{HL}$	0	$2V_{dc}$	$v^*_{\rm out}-2V_{dc}$
$-V_{dc}+\Delta V'_{HL}+\Delta V'_{ML} \le v^*_{\rm out} < V_{dc}+\Delta V'_{HL}+\Delta V'_{ML}$	0	0	$v^*_{\rm out}$
$-3V_{dc}+\Delta V'_{HM}+\Delta V'_{HL} \le v^*_{\rm out} < -V_{dc}+\Delta V'_{HL}+\Delta V'_{ML}$	0	$-2V_{dc}$	$v^*_{\rm out}+2V_{dc}$
$-5V_{dc}+\Delta V'_{HL}+\Delta V'_{ML} \le v^*_{\rm out} < -3V_{dc}+\Delta V'_{HM}+\Delta V'_{HL}$	$-6V_{dc}$	$2V_{dc}$	$v^*_{\rm out}+4V_{dc}$
$-7V_{dc}-\Delta V'_{HM}+\Delta V'_{ML} \le v^*_{\rm out} < -5V_{dc}+\Delta V'_{HL}+\Delta V'_{ML}$	$-6V_{dc}$	0	$v^*_{\rm out}+6V_{dc}$
$-9V_{dc} \le v^*_{\rm out} < -7V_{dc}-\Delta V'_{HM}+\Delta V'_{ML}$	$-6V_{dc}$	$-2V_{dc}$	$v^*_{\rm out}+8V_{dc}$

A parameter ΔV_{HL} is introduced for the energy transfer between the HV cell and the LV cell. Polarity of $\Delta V'_{HL}$ is selected according to the output current i as follows:

$$\Delta V'_{HL} = \Delta V_{HL} \cdot \mathrm{sgn}(i), \tag{5}$$

where the sign function $\mathrm{sgn}(x)$ is defined as

$$\mathrm{sgn}(x) = \begin{cases} -1 & \text{if } x < 0 \\ 0 & \text{if } x = 0 \\ 1 & \text{if } x > 0. \end{cases} \tag{6}$$

Other parameters are set as $\Delta V_{HM} = \Delta V_{ML} = 0$. These values give a set of v_H, v_M, and $\bar{v}_L$ according to Table I.

Fig. 3 shows the voltage and instantaneous power waveforms in case $\Delta V_{HL} = 0$ (shown by dotted lines) and $\Delta V_{HL} > 0$ (shown by solid lines). The products of the output current i and the output voltages v_H, v_M, and $\bar{v}_L$ are instantaneous power flowing into the HV, MV, and LV cell, shown by p_H, p_M, and p_L, respectively. Δp_H, Δp_M, and Δp_L are differences between solid and dotted lines in p_H, p_M, and p_L. Averages of Δp_H, Δp_M, and Δp_L in a cycle are the received power of the HV, MV, and LV cell, shown by P_H, P_M, and P_L, respectively.

The theoretical analysis of P_H, P_M, and P_L gives (see Appendix)

$$P_H = -\frac{4}{3\pi}\Delta V_{HL} I \tag{7}$$

$$P_M = 0 \tag{8}$$

$$P_L = \frac{4}{3\pi}\Delta V_{HL} I. \tag{9}$$

This result means that energy transfer from the HV cell to the LV cell is controlled by ΔV_{HL}.

The range of $\bar{v}_L$ expands according to ΔV_{HL} as follows:

$$-V_{dc} - |\Delta V_{HL}| \le \bar{v}_L \le V_{dc} + |\Delta V_{HL}|. \tag{10}$$

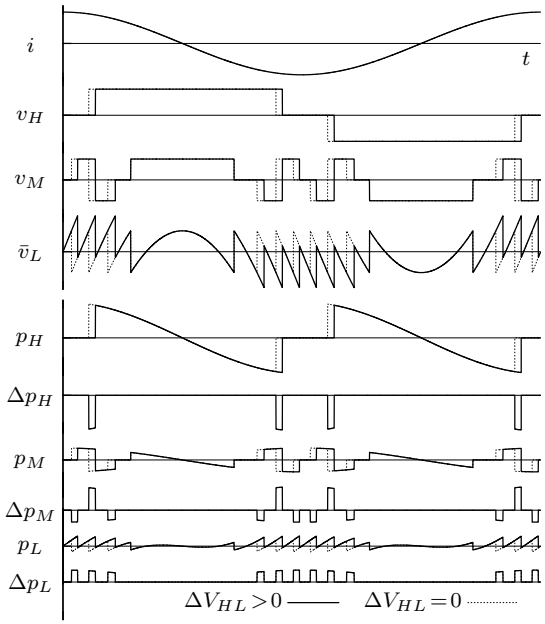


Fig. 3. Input power of each cell during energy transfer from the HV cell to the LV cell. Solid line is in case $\Delta V_{HL} > 0$, and dotted line is in case $\Delta V_{HL} = 0$. $\Delta V_{HM} = \Delta V_{ML} = 0$ in both cases.

To make the LV cell able to output the voltage in the range of (10), the dc voltage of the LV cell v_{CL} should be maintained as

$$v_{CL} \geq V_{dc} + |\Delta V_{HL}|. \tag{11}$$

2) Energy Transfer between the HV Cell and the MV Cell: A parameter ΔV_{HM} is used for the energy transfer between the HV cell and the MV cell. A set of v_H, v_M, and $\bar{v}_L$ is obtained by Table I and $\Delta V'_{HM}$ which is given by

$$\Delta V'_{HM} = \Delta V_{HM} \cdot \mathrm{sgn}(i). \tag{12}$$

Fig. 4 shows the voltage and instantaneous power waveforms in case $\Delta V_{HM} = 0$ (shown by dotted lines) and $\Delta V_{HM} > 0$ (shown by solid lines). Other parameters are set as $\Delta V_{HL} = \Delta V_{ML} = 0$.

The theoretical analysis of P_H, P_M, and P_L gives

$$P_H = -\frac{4}{3\pi}\Delta V_{HM} I \tag{13}$$

$$P_M = \frac{4}{3\pi}\Delta V_{HM} I \tag{14}$$

$$P_L = 0. \tag{15}$$

This result means that energy transfer from the HV cell to the MV cell is controlled by ΔV_{HM}.

The range of $\bar{v}_L$ expands according to ΔV_{HM} as follows:

$$-V_{dc} - |\Delta V_{HM}| \leq \bar{v}_L \leq V_{dc} + |\Delta V_{HM}|. \tag{16}$$

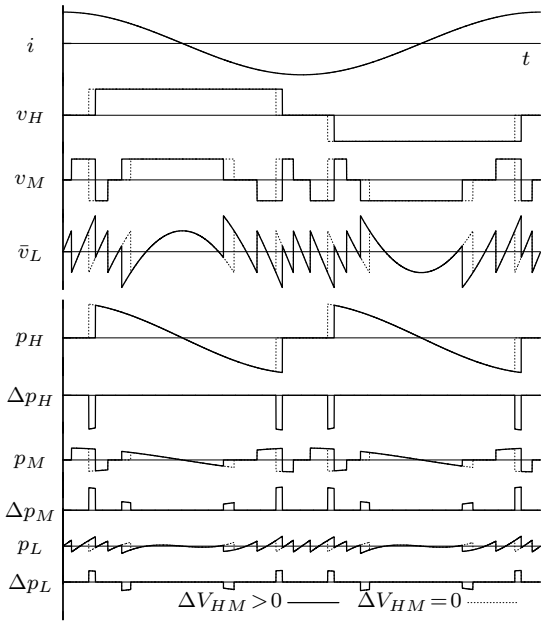


Fig. 4. Input power of each cell during energy transfer from the HV cell to the MV cell. Solid line is in case $\Delta V_{HM} > 0$, and dotted line is in case $\Delta V_{HM} = 0$. $\Delta V_{HL} = \Delta V_{ML} = 0$ in both cases.

To make the LV cell able to output the voltage in the range of (16), the dc voltage of the LV cell v_{CL} should be maintained as

$$v_{CL} \geq V_{dc} + |\Delta V_{HM}|. \tag{17}$$

3) Energy Transfer between the MV Cell and the LV Cell: A parameter ΔV_{ML} is used for the energy transfer between the MV cell and the LV cell. A set of v_H, v_M, and $\bar{v}_L$ are obtained by Table I and $\Delta V'_{HM}$ which is given by

$$\Delta V'_{ML} = \Delta V_{ML} \cdot \mathrm{sgn}(i). \tag{18}$$

Fig. 5 shows the voltage and instantaneous power waveforms in case $\Delta V_{ML} = 0$ (shown by dotted lines) and $\Delta V_{ML} > 0$ (shown by solid lines). Other parameters are set as $\Delta V_{HM} = \Delta V_{HL} = 0$.

The theoretical analysis of P_H, P_M, and P_L gives

$$P_H = 0 \tag{19}$$

$$P_M = -\frac{4}{3\pi}\Delta V_{ML} I \tag{20}$$

$$P_L = \frac{4}{3\pi}\Delta V_{ML} I. \tag{21}$$

This result means that energy transfer from the MV cell to the LV cell is controlled by ΔV_{ML}.

The range of $\bar{v}_L$ expands according to ΔV_{ML} as follows:

$$-V_{dc} - |\Delta V_{ML}| \leq \bar{v}_L \leq V_{dc} + |\Delta V_{ML}|. \tag{22}$$

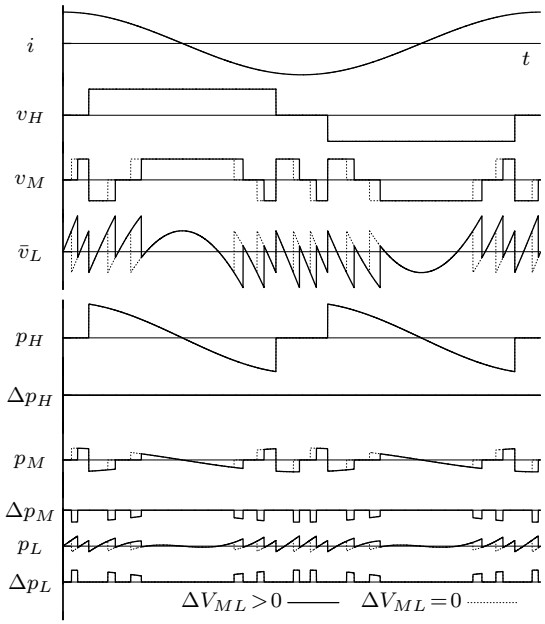


Fig. 5. Input power of each cell during energy transfer from the MV cell to the LV cell. Solid line is in case $\Delta V_{ML} > 0$, and dotted line is in case $\Delta V_{ML} = 0$. $\Delta V_{HM} = \Delta V_{HL} = 0$ in both cases.

To make the LV cell able to output the voltage in the range of (22), the dc voltage of the LV cell v_{CL} should be maintained as

$$v_{CL} \geq V_{dc} + |\Delta V_{ML}|. \tag{23}$$

B. Energy Transfer among Three Cells

Energy transfer among three cells is also realized by giving two parameters among ΔV_{HL}, ΔV_{HM}, and ΔV_{ML} together. For example, control of ΔV_{HL} and ΔV_{HM} realizes energy transfer among three cells because the MV cell and the LV cell can transfer their energy by way of the HV cell. Then, the range of $\bar{v}_L$ is expressed by (10), (16), and the following equation.

$$-V_{dc} - |\Delta V_{HL} + \Delta V_{HM}| \leq \bar{v}_L \leq V_{dc} + |\Delta V_{HL} + \Delta V_{HM}|. \tag{24}$$

To make the LV cell able to output the voltage in the range of (24), the dc voltage of the LV cell v_{CL} should be maintained to satisfy (11), (17), and the following equation.

$$v_{CL} \geq V_{dc} + |\Delta V_{HL} + \Delta V_{HM}|. \tag{25}$$

C. Dc Voltage Ratio for the Proposed Control

In the section II-A, v_{CL} was increased by 20% from V_{dc} to apply the proposed energy transfer control. However, the increase is not necessarily 20% but arbitrary value as long as satisfying (11), (17), (23), and (25). ΔV_{HL},

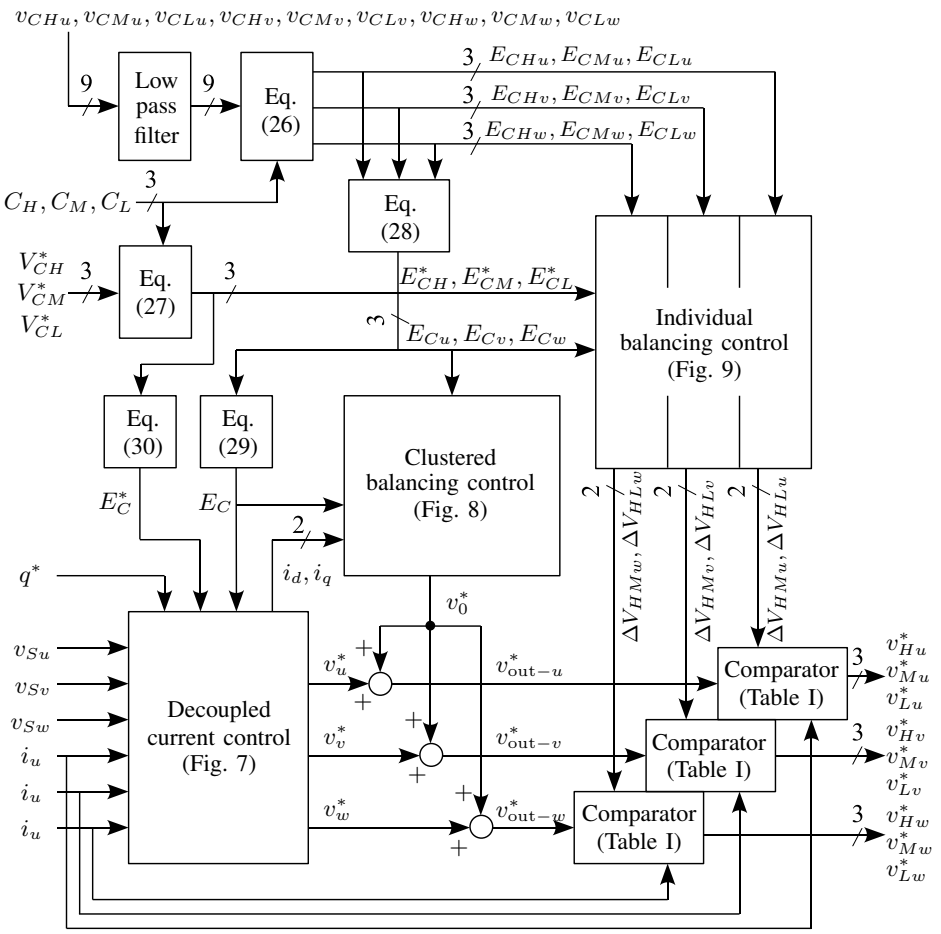


Fig. 6. Control block diagram for the STATCOM based on a multi-voltage cascade converter.

ΔV_{HM}, and ΔV_{ML} are much smaller than V_{dc} in usual operating conditions as a STATCOM, because the required amount of energy transfer in a cluster is small. Hence, $1.2V_{dc}$ is large enough for v_{CL} to satisfy the conditions.

Although the dc voltage ratio above was $6:2:1.2$, the proposed method is applicable for other voltage ratio such as $5:2:1.2$ and $4:2:1.2$. Furthermore, the proposed method is applicable if the ratio satisfies the modulation condition investigated in [12]: any pair of adjacent voltage levels can be modulated by switching only the LV cell. However, Table I has to be modified according to each of the dc voltage ratio.

When the output voltage is not enough for connecting grids, the voltage can be expanded with additional HV cells. Four-cell configuration whose dc voltage ratio is $6:6:2:1.2$ including two HV cells can output up to ac 11 kV. Similarly, a configuration including three HV cells can achieve ac 15 kV, and four HV cells can achieve 20 kV. In these configurations, the HV cells' switching angles are shifted each other like single-voltage cascade converters to synthesize low harmonic voltage waveform [3], [21], [22].

IV. Control Method for a STATCOM Based on a Multi-Voltage Cascade Converter

Fig. 6 shows an overall control block diagram for the proposed STATCOM based on a multi-voltage cascade converter. The fundamental architecture is based on three function blocks developed for single-voltage cascade converters [4], [23], that is a decoupled current control, a clustered balancing control, and an individual balancing control. Main differences for a multi-voltage cascade converter are as follows:

- Energy stored in the dc capacitors is calculated and used for control values instead of the dc capacitor voltages.
- Individual balancing control is modified to accommodate multi-voltage cascade converters.

Each block is explained in detail below.

A. Control Scheme Based on the Energy Stored in the Dc Capacitors

Balancing controls are constructed based on the energy stored in the dc capacitor. As a result, deviations from the reference values can be quantitatively compared among cells having different capacitances and voltages, which is effective for multi-voltage cascade converters.

Energy stored in the dc capacitor E_{Cxy} is given by

$$E_{Cxy} = \frac{1}{2} C_x V_{Cxy}^2, \tag{26}$$

where C_x is the capacitance and V_{Cxy} is the sensed dc capacitor voltage (subscript x is either H, M, or L). A reference of the stored energy E_{Cx}^* is calculated from its voltage reference V_{Cx}^* by

$$E_{Cx}^* = \frac{1}{2} C_x {V_{Cx}^*}^2. \tag{27}$$

The individual balancing control regulates the stored energy E_{Cxy} to be equal to its reference value E_{Cx}^*.

Total energy stored in the cluster is given by

$$E_{Cy} = E_{CHy} + E_{CMy} + E_{CLy}, \tag{28}$$

where E_{CHy}, E_{CMy}, and E_{CLy} are the energy stored in the HV, MV, and LV cell. The clustered balancing control regulates E_{Cu}, E_{Cv}, and E_{Cw} to balance each other.

Total energy stored in the converter E_C is given by

$$E_C = E_{Cu} + E_{Cv} + E_{Cw}. \tag{29}$$

Reference of the energy stored in the converter E_C^* is calculated using the values given by (27) as follows:

$$E_C^* = 3(E_{CH}^* + E_{CM}^* + E_{CL}^*). \tag{30}$$

The decoupled current control regulates E_C to be equal to its reference value E_C^*.

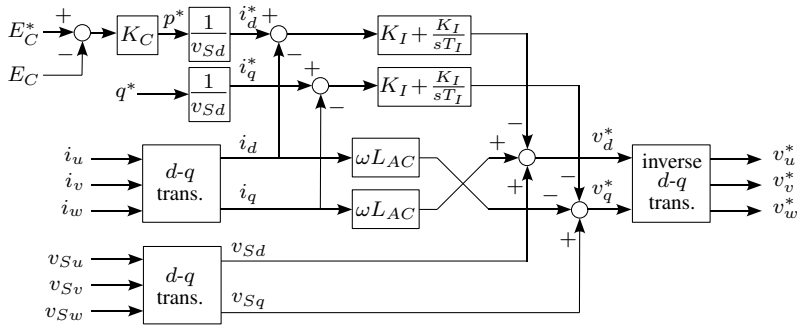


Fig. 7. Decoupled current control for a three-phase converter.

B. Decoupled Current Control

Fig. 7 shows a block diagram of the decoupled current control [23], [24]. The decoupled current control regulates instantaneous active and reactive power by considering a set of three clusters as a three-phase converter. The total stored energy in the converter is also regulated in this block. Output currents i_u, i_v, i_w and ac line voltages v_{Su}, v_{Sv}, v_{Sw} are transformed to the d-q rotating coordinate as i_d, i_q, v_{Sd}, and v_{Sq}. A proportional controller whose gain is K_C calculates the reference of instantaneous active power p^* based on the deviation between E_C and its reference E_C^*. A reference of instantaneous reactive power q^* is given by a system operator from the outside of this control block. Dividing p^* and q^* by the ac line voltage v_{Sd} gives the output current references i_d^* and i_q^*, which are calculated by

$$i_d^* = \frac{K_C(E_C^* - E_C)}{v_{Sd}} \tag{31}$$

$$i_q^* = \frac{q^*}{v_{Sd}}. \tag{32}$$

Proportional and integral controller decides the output voltages from the deviation between the references i_d^*, i_q^* and the actual currents i_d, i_q. The ac line voltage and voltage across the ac inductor L_{AC} are added to the output voltage reference in the feed-forward manner. Therefore, voltage references v_d^* and v_q^* are given by

$$\begin{aligned}\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \begin{bmatrix} v_{Sd} \\ v_{Sq} \end{bmatrix} + \begin{bmatrix} 0 & \omega L_{AC} \\ -\omega L_{AC} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \\ -K_I \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} - \frac{K_I}{T_I} \int \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} dt,\end{aligned} \tag{33}$$

where K_I and T_I are a proportional gain and a time constant of the current controller. The values are transformed to the three-phase voltage references v_u^*, v_v^*, v_w^* by an inverse d-q transformation.

C. Clustered Balancing Control

Fig. 8 shows a block diagram of the clustered balancing control proposed in [25], [26]. This control block operates to balance the energy stored in each cluster by considering a set of HV, MV and LV cells as a single-phase

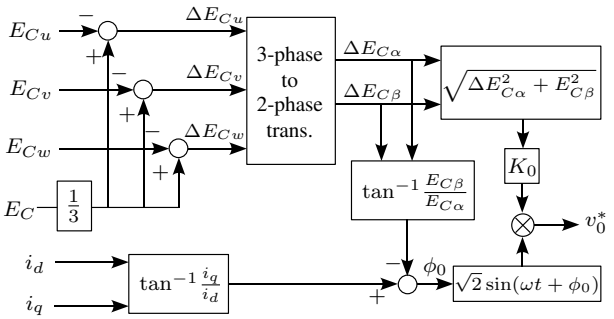


Fig. 8. Clustered balancing control between three clusters in a converter.

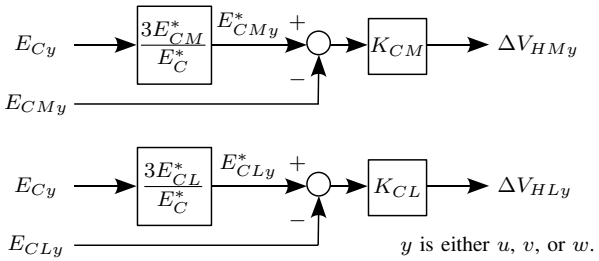


Fig. 9. Individual balancing control between three cells in a cluster.

converter. It injects a fundamental-frequency zero-sequence voltage v_0 to the voltage references v_u^*, v_v^*, v_w^* [25]. Although the injection of zero-sequence voltage v_0 causes no change in the line-to-line voltage and line currents, it allows to transfer active power among clusters. Here, ΔE_{Cu}, ΔE_{Cv}, and ΔE_{Cw} are the degree of imbalance of the energy stored in the cluster, and their three-phase to two-phase transformation gives $\Delta E_{C\alpha}$ and $\Delta E_{C\beta}$. They are calculated by

$$\begin{bmatrix} \Delta E_{C\alpha} \\ \Delta E_{C\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \frac{1}{3}E_C - E_{Cu} \\ \frac{1}{3}E_C - E_{Cv} \\ \frac{1}{3}E_C - E_{Cw} \end{bmatrix}. \tag{34}$$

Reference of the zero-sequence voltage v_0^* is given by

$$v_0^* = K_0\sqrt{\Delta E_{C\alpha}^2 + E_{C\beta}^2} \cdot \sqrt{2}\sin(\omega t + \phi_0) \tag{35}$$

$$\phi_0 = \tan^{-1}\frac{i_q}{i_d} - \tan^{-1}\frac{E_{C\beta}}{E_{C\alpha}}, \tag{36}$$

where K_0 is a proportional gain for amplitude regulation of v_0^*, and ϕ_0 is the phase angle of v_0^*.

D. Individual Balancing Control

Fig. 9 shows a block diagram of the proposed individual balancing control. This control maintains the dc voltage ratio of the HV, MV, and LV cell by applying the energy transfer method proposed in the section III. Fig. 9 depicts a block for a single cluster, and two more identical controllers are structured for other two clusters.

Reference of the energy stored in the MV cell E^*_{CMy} is derived from the total energy of the cluster E_{Cy} and the ratio of references $E^*_C/3$ and E^*_{CM} as follows:

$$E^*_{CMy} = \frac{3E^*_{CM}}{E^*_C} E_{Cy}. \tag{37}$$

A feedback controller provides ΔV_{HMy} from the error between the reference E^*_{CMy} and actual E_{CMy} as follows:

$$\Delta V_{HMy} = K_{CM}(E^*_{CMy} - E_{CMy}), \tag{38}$$

where K_{CM} is a proportional gain. In the same manner, E^*_{CLy} is given by

$$E^*_{CLy} = \frac{3E^*_{CL}}{E^*_C} E_{Cy}. \tag{39}$$

ΔV_{HLy} is calculated by a proportional gain K_{CL}, the reference value E^*_{CLy} and the actual value E_{CLy} as follows:

$$\Delta V_{HLy} = K_{CM}(E^*_{CLy} - E_{CLy}). \tag{40}$$

ΔV_{HMy} and ΔV_{HLy} are immediately reflected to Table I. Then the cluster operates to maintain its dc voltage ratio.

Although a pair of ΔV_{HMy} and ΔV_{HLy} are used in the explanation above, a pair of ΔV_{HLy} and ΔV_{MLy}, or ΔV_{MLy} and ΔV_{HMy} are also available instead of ΔV_{HMy} and ΔV_{HLy} in order to maintain the dc voltage ratio.

V. Experimental Results

A. Experimental Setup

A three-phase downscaled STATCOM rated at 220 V and 10 kVA was built and tested in the circuit configuration shown in Fig. 1. Table II and Fig. 10 show circuit parameters and a photo of the experimental setup. Si-MOSFETs (rated at 250 V for HV cells, 100 V for MV cells, and 60 V for LV cells) were applied to the circuit instead of IGBTs. The dc capacitors were designed to make their voltage ripple less than 10% in the rated power, and also to meet their current ripple rating. Starting resistors were temporarily inserted in series with ac inductors for pre-charging the dc capacitors before switching operation.

The controller consists of a DSP (Texas Instruments TMS320C6713, 32-bit, floating point, 225 MHz clock), a FPGA (Xilinx Spartan-3, 1.5 M system gates), and two AD converters (Analog Devices AD7266, 12-bit, 12-channel analog inputs). Its sampling and calculation interval was 50 μs. Current control gain K_I and time constant T_I were determined based on the experimental tests to achieve stable transient response. Control gains for the energy stored in capacitor K_C, K_0, K_{CM}, and K_{CL} were designed based on their startup operation characteristics to have slower response than the inner-loop current controller.

B. A Startup Operation

Fig. 11 shows experimental waveforms when the STATCOM was starting up. The bold, solid, and dotted lines show the values of u-phase, v-phase, and w-phase, respectively.

Fig. 11 (a) shows the waveforms when the converter was connected to an ac source. Although all MOSFETs were off-state, ac current was rectified by the anti-parallel diodes. The current charged dc capacitors by way of 5.6

TABLE II

CIRCUIT AND CONTROL PARAMETERS OF THE EXPERIMENTAL SETUP.

Nominal line-to-line rms voltage		220 V
Power rating		10 kVA
Ac inductor	L_{AC}	0.70 mH (4.5%†)
Background system inductance		0.27 mH (1.8%†)
Nominal dc voltage	V_{dc}	20 V
HV cell dc voltage	V^*_{CH}	120 V
MV cell dc voltage	V^*_{CM}	40 V
LV cell dc voltage	V^*_{CL}	24 V
HV cell dc capacitor	C_H	10.8 mF
MV cell dc capacitor	C_M	33.6 mF
LV cell dc capacitor	C_L	72.0 mF
Starting resistor		5.6 Ω
Active power control gain	K_C	1 s^{-1}
Current control gain	K_I	3 Ω
Current control time constant	T_I	0.01 s
Clustered balancing control gain	K_0	4 V/J
Individual balancing control gain	K_{CM}	10 V/J
Individual balancing control gain	K_{CL}	10 V/J
PWM carrier frequency		10 kHz
Equivalent switching frequency		20 kHz

† on a three-phase, 220-V, 10-kVA, 50-Hz base

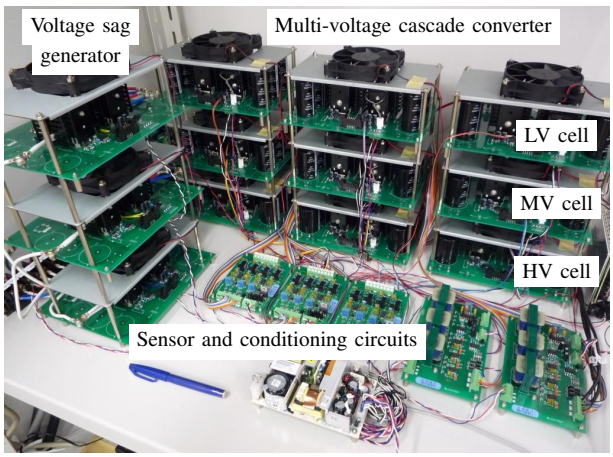
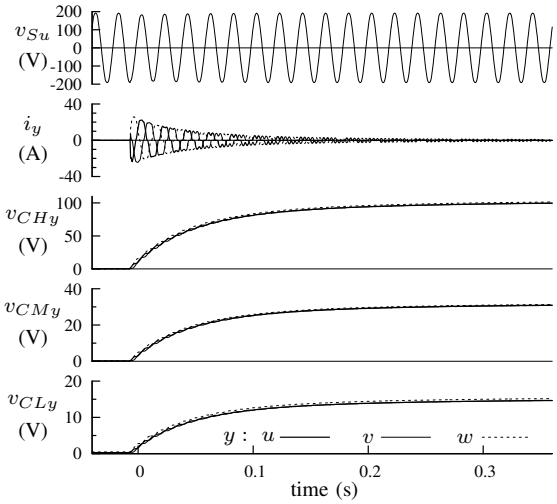
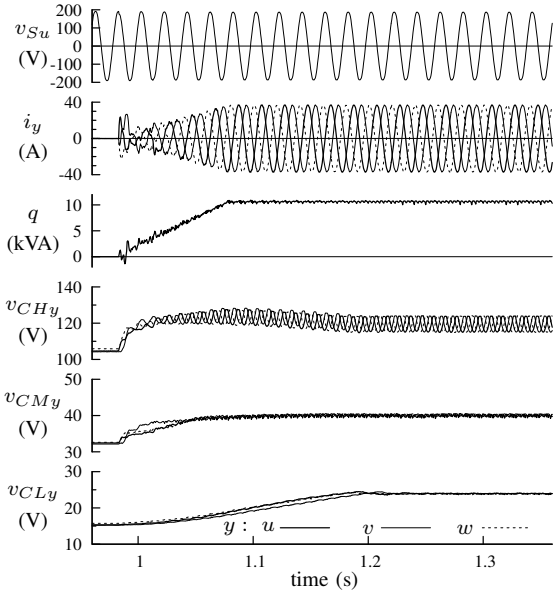


Fig. 10. Experimental setup.

Ω starting resistor. The dc capacitors were charged about 80% of the reference voltage during this mode. Since dc capacitors of the same cluster are connected in series in this mode, the dc voltage ratio can be maintained by



(a) Pre-charging through starting resistor.



(b) Startup of the converter switching.

Fig. 11. Experimental waveforms during startup.

simply setting their capacitances as

$$C_H : C_M : C_L = \frac{1}{V_{CH}^*} : \frac{1}{V_{CM}^*} : \frac{1}{V_{CL}^*}. \tag{41}$$

The capacitances C_M and C_L can be reduced according to their voltage and current ripple if a control to maintain the dc voltage ratio during the pre-charge is employed.

Fig. 11 (b) shows the waveforms after starting the switching operation. The reactive power q was increased to 10 kVA in 100 ms. Although some amount of voltage imbalance was observed during transient state, all dc voltages converged to the reference value in 200 ms.

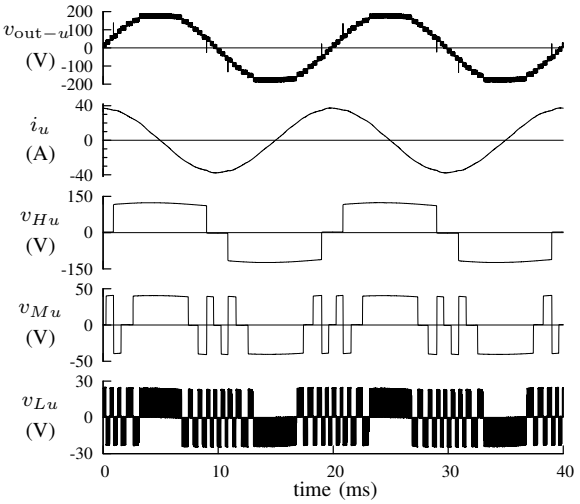


Fig. 12. Experimental waveforms with capacitive operation at 10 kVA.

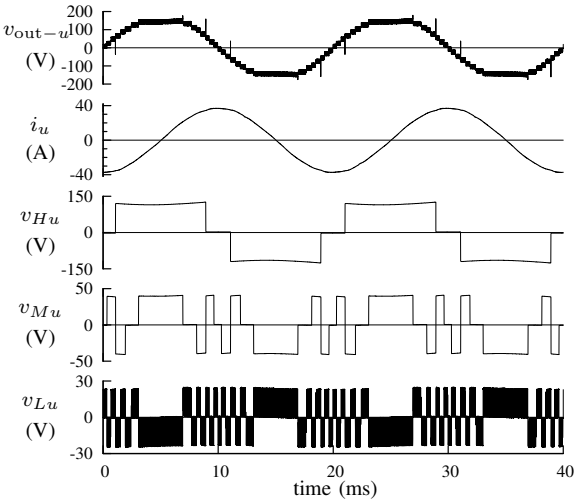


Fig. 13. Experimental waveforms with inductive operation at 10 kVA.

C. Steady State Operations

Fig. 12 shows the output voltage and current waveforms when the STATCOM was put into capacitive operation at 10 kVA. Phase angle of the output voltage $v_{\mathrm{out}-u}$ lags to that of the output current i_u by $\pi/2$ rad. The HV, MV, and LV cells operated at 50 Hz, 250 Hz, and 10 kHz switching, and composed $v_{\mathrm{out}-u}$ having 19 voltage levels. Total harmonic distortion (THD) of i_u was 1.4%, which is small enough to grid-tie requirement. Although $v_{\mathrm{out}-u}$ had some 1 μs glitches caused by the dead time, the glitches scarcely affected the output current.

Fig. 13 shows the output voltage and current waveforms when the STATCOM was put into inductive operation at 10 kVA. $v_{\mathrm{out}-u}$ had 17 voltage levels because the output voltage of the converter was slightly reduced resulting from the voltage drops in the ac inductors L_{AC}. Phase angle of i_u lags to that of $v_{\mathrm{out}-u}$ by $\pi/2$ rad, and the THD of i_u was 1.1%.

Fig. 14 shows the output voltage/current and dc capacitor voltage waveforms when the output power q was

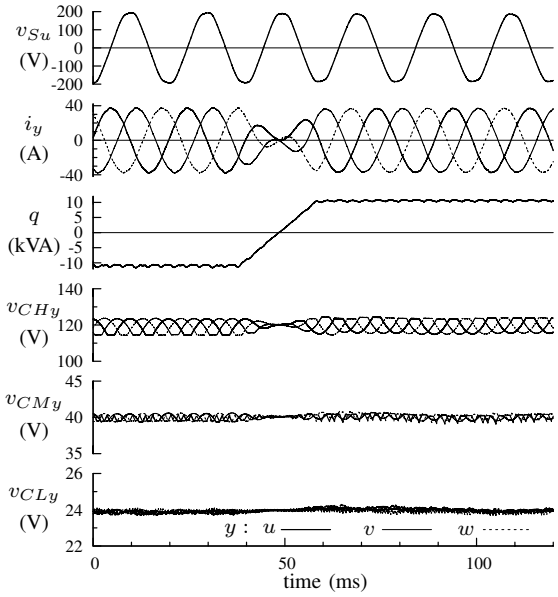


Fig. 14. Experimental waveforms during changing from capacitive to inductive operation at 10 kVA.

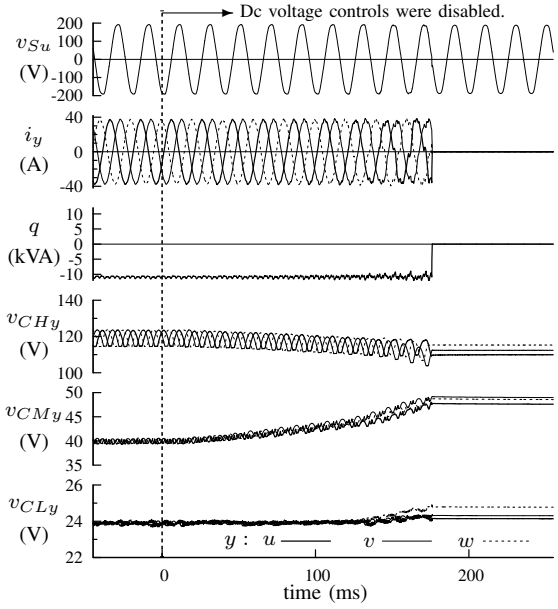


Fig. 15. Experimental waveforms after intentionally disabling the dc voltage controls.

changed from capacitive to inductive operation at 10 kVA in 20 ms. The mean values of the dc voltages v_{CHy}, v_{CMy}, and v_{CLy} are maintained to their reference values by the proposed dc voltage controls.

D. Dc Voltage Control Characteristics

Fig. 15 shows the waveforms when the dc voltage controls were intentionally disabled during operation in order to confirm the necessity of the control. After disabling the dc voltage controls, v_{CMy} started to increase and v_{CHy} and v_{CLy} started to decrease, resulting in the voltage imbalance in a cluster. The imbalance caused distortion in the

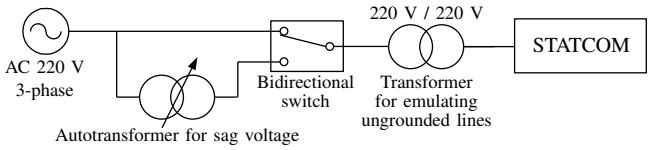


Fig. 16. Experimental setup for simulating voltage sag.

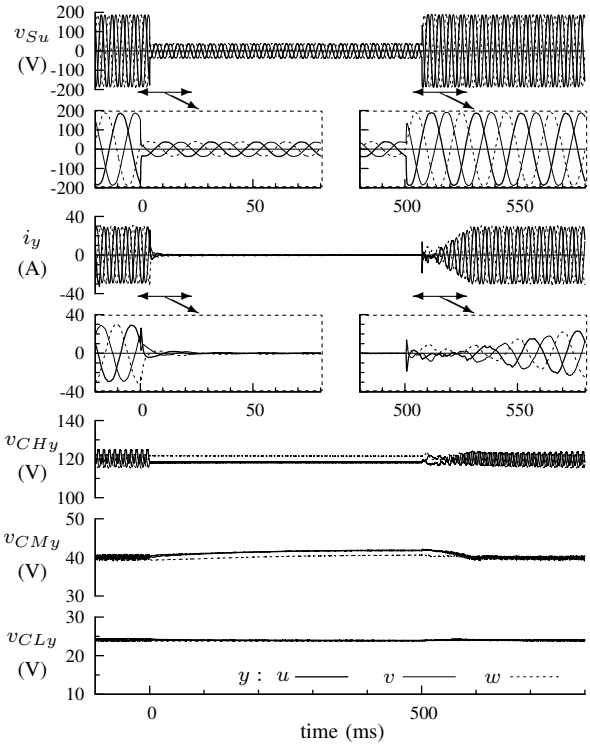


Fig. 17. Experimental results during three-phase 80% voltage sag condition.

output current i_y. Since v_{CMv} reached to 120% of the reference voltage 180 ms after the disabling, overvoltage protection halted the converter. This result shows the necessity of the dc voltage controls for the converter operation.

E. Operation Characteristics under Voltage Sags

Fig. 16 shows the experimental setup to confirm the STATCOM's operation characteristics under voltage sags. Typical voltage sags were emulated by a voltage sag generator consisting of an autotransformer and bidirectional semiconductor switches [27], [28]. A transformer is inserted between the voltage sag generator and the STATCOM in order to simulate both the voltage sags and the phase jumps in an ungrounded distribution line caused by a fault in high voltage transmission lines.

Fig. 17 shows the experimental results during three-phase 80% voltage sag. The sag continued for 500 ms. The STATCOM reduced its output current to zero under such a severe voltage sag in order to avoid voltage overshoot just after the fault clearing. LV and MV cells continued their switching to control the output current to zero. HV

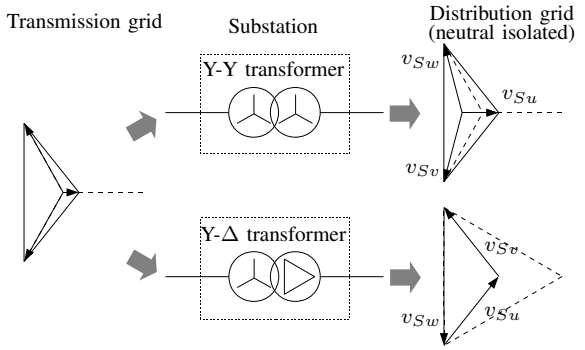


Fig. 18. Voltage sags in the distribution grid caused by the single-phase fault in the transmission grid.

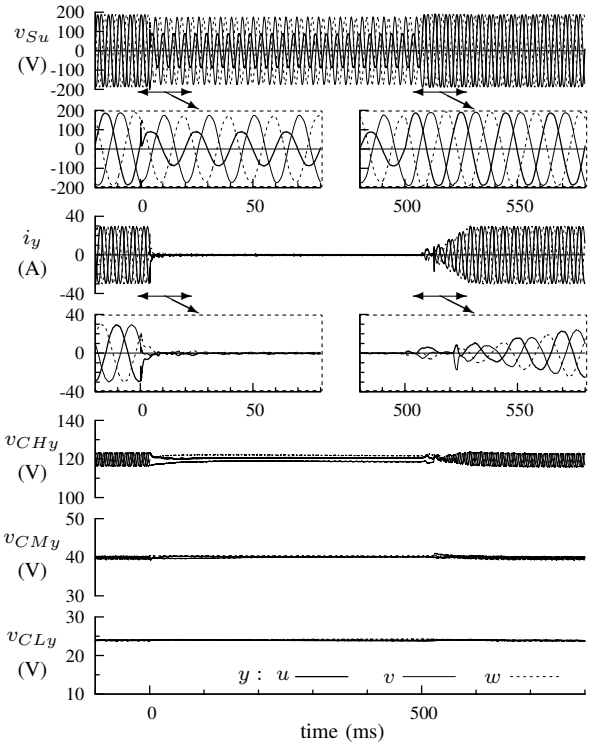


Fig. 19. Experimental results during single-phase 80% voltage sag by way of a Y-Y transformer.

cells did not switch during the sag because the line voltage was low. When the line voltage recovered after 500 ms, the STATCOM rapidly regained its output current. The dc voltages were kept almost constant during the operation.

Fig. 18 shows the possible voltage sag patterns in the distribution lines caused by a single-phase fault in the transmission line. The voltage sag changes according to the transformer's winding connection [29]. When Y-Y transformer is used in the substation, zero-phase-sequence voltage is eliminated in the distribution line. Then the phase angle of v_{Sv} and v_{Sw} jumps together. When Y-Δ transformer is used in the substation, v_{Su} and v_{Sv} drops and their phase angle also jumps in the distribution line. Both cases were verified by the experiments.

Fig. 19 shows the experimental results during single-phase 80% voltage sag assuming that Y-Y transformer is

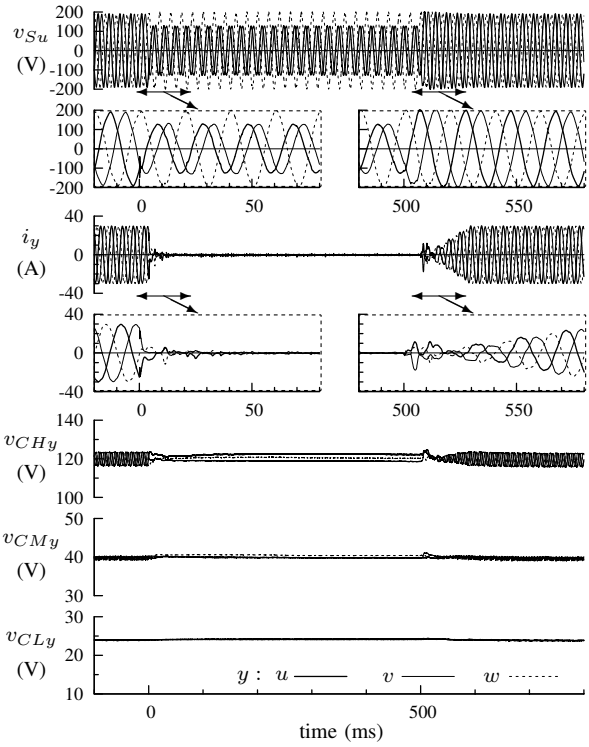


Fig. 20. Experimental results during single-phase 80% voltage sag by way of a Y-Δ transformer.

used in the distribution substation. Fig. 20 shows the case that Y-Δ transformer is used. Both of them continued their switching and kept the line currents to zero. The dc voltages did not deviated from the reference values and the STATCOM was able to regain its output current after the recovery of line voltage.

While the output current was reduced to zero during the sag in the experiment, the STATCOM has capability to keep its output current flowing in the three-phase balanced voltage sag shown in Fig. 17. Because the output voltage and output current of all clusters can be in quadrature, they cause no active power flow. However, the STATCOM can not keep its output current flowing in the three-phase unbalanced voltage sags shown in Figs. 19 and 20. This is because some amount of active power flows into the clusters, and the stored energy in the clusters becomes imbalanced.

VI. Conclusions

This paper has proposed a system configuration and a control method for a multi-voltage cascade converter in order to reduce power loss and volume of a 6.6-kV transformerless D-STATCOM. The proposed system has the following characteristics:

- The cascaded H-bridge configuration realizes direct connection to the 6.6-kV distribution lines without step-down transformers.
- The multi-voltage cascade configuration reduces output voltage harmonics, resulting in a reduction of ac filters.

- Only the cells having lowest dc voltage (0.72 kV) operate in high frequency PWM, resulting in a reduction of overall switching loss and low order harmonics.
- The cells having highest dc voltage (3.6 kV) consist of high blocking voltage IGBTs, resulting in a reduction of cascaded numbers and conduction loss.
- The reduction of switching and conduction loss downsizes heat dissipation system.

The proposed dc voltage balancing control method for the multi-voltage cascade converter realizes to remove the auxiliary dc sources from the all cells during STATCOM operation. This control realizes the energy transfer among the cells in the same phase by increasing dc voltage of the LV cell by 20%, and adjusting the phase angle of the output voltage pulses. A downscaled experimental model rated at 220 V and 10 kVA was built and tested. The experimental results proved the stable operation in the startup, steady state, and output power change of the proposed method. Fundamental fault ride through capability was also verified by the experiments.

APPENDIX

ANALYSIS OF THE TRANSFERRED POWER

This section deals with the analysis on the averaged transferred power among cells. The output voltage $v^*_{\rm out}$ and current i are in quadrature during STATCOM operation as follows.

$$v_{\rm out} = 9V_{dc}\sin\omega t \tag{42}$$

$$i = I\cos\omega t. \tag{43}$$

Since the waveforms are symmetrical, the following analysis is carried out in a range of $0 \le t \le \pi/2\omega$ (a quarter cycle). ΔV_x is the variation of output voltage V_x during a short period Δt_x from $t = t_x$ to $t = t_x + \Delta t_x$, and the relation is described as follows:

$$\frac{\Delta V_x}{\Delta t_x} = 9V_{dc}\omega\cos\omega t_x. \tag{44}$$

Fig. 21 shows the relation among the output voltage reference $v^*_{\rm out}$, the threshold to switch the output voltage of the cells V_{dc}, $3V_{dc}$, $5V_{dc}$, $7V_{dc}$, and the time to switch the output voltage t_a, t_b, t_c, t_d. It is assumed that the parameters $\Delta V_{HM} = \Delta V_{ML} = 0$. When ΔV_{HL} is used for the control parameter, the HV cell switches at $v^*_{\rm out} = 3V_{dc} + \Delta V'_{HL}$ according to Table I. Then the switching delays for Δt_b. According to (44), the relation is given by

$$\frac{\Delta V_{HL}}{\Delta t_b} = 9V_{dc}\omega\cos\omega t_b. \tag{45}$$

P_H is the average power flowing into the HV cell, which is the product of the HV cell's output voltage $6V_{dc}$, the output current i, and the period Δt_b divided by a quarter cycle $\pi/2\omega$. It is given by

$$P_H = -\frac{6V_{dc}\cdot I\cos\omega t_b\cdot\Delta t_b}{\pi/2\omega}. \tag{46}$$

Substituting (45) for (46) yields

$$P_H = -\frac{4}{3\pi}\Delta V_{HL}I. \tag{47}$$

The MV cell switches at $v^*_{\rm out} = V_{dc} + \Delta V_{HL}$, $v^*_{\rm out} = 3V_{dc} + \Delta V_{HL}$, and $v^*_{\rm out} = 5V_{dc} + \Delta V_{HL}$. Then the switching delays for Δt_a, Δt_b, and Δt_c, respectively. The average power flowing into the MV cell P_M is given by

$$\begin{aligned} P_M &= -\frac{2V_{dc} \cdot I\cos\omega t_a \cdot \Delta t_a}{\pi/2\omega} + \frac{4V_{dc} \cdot I\cos\omega t_b \cdot \Delta t_b}{\pi/2\omega} \\ &\quad - \frac{2V_{dc} \cdot I\cos\omega t_c \cdot \Delta t_c}{\pi/2\omega} \\ &= (-2V_{dc} + 4V_{dc} - 2V_{dc})\frac{2\Delta V_{HL} I}{9\pi V_{dc}} \\ &= 0. \end{aligned} \tag{48}$$

Total power of the HV, MV, and LV cell is zero in a cycle because the converter's output voltage $v_{\rm out}$ and current i is quadrature. That is expressed as

$$P_H + P_M + P_L = 0. \tag{49}$$

(47), (48), and (49) yield the average power flowing into the LV cell P_L as follows:

$$\begin{aligned} P_L &= -P_H - P_M \\ &= \frac{4}{3\pi}\Delta V_{HL} I. \end{aligned} \tag{50}$$

The analysis shows that the operation of ΔV_{HL} causes energy transfer from the HV cell to the LV cell without any influence on the MV cell.

It is assumed that $\Delta V_{HL} = \Delta V_{ML} = 0$. When ΔV_{HM} is used to transfer power from the HV cell to the MV cell, the HV cell's switching delays for Δt_b. Then P_H is given in the same manner by

$$\begin{aligned} P_H &= -\frac{6V_{dc} \cdot I\cos\omega t_b \cdot \Delta t_b}{\pi/2\omega} \\ &= -\frac{4}{3\pi}\Delta V_{HM} I. \end{aligned} \tag{51}$$

At the same time, the MV cell's switching delays for Δt_b and Δt_d. Then P_M is given by

$$\begin{aligned} P_M &= \frac{4V_{dc} \cdot I\cos\omega t_b \cdot \Delta t_b}{\pi/2\omega} + \frac{2V_{dc} \cdot I\cos\omega t_d \cdot \Delta t_d}{\pi/2\omega} \\ &= (4V_{dc} + 2V_{dc})\frac{2\Delta V_{HM} I}{9\pi V_{dc}} \\ &= \frac{4}{3\pi}\Delta V_{HM} I. \end{aligned} \tag{52}$$

(49), (51), and (52) yield the average power flowing into the LV cell P_L as follows:

$$\begin{aligned} P_L &= -P_H - P_M \\ &= 0. \end{aligned} \tag{53}$$

The analysis shows that the operation of ΔV_{HM} causes energy transfer from the HV cell to the MV cell without any influence on the LV cell.

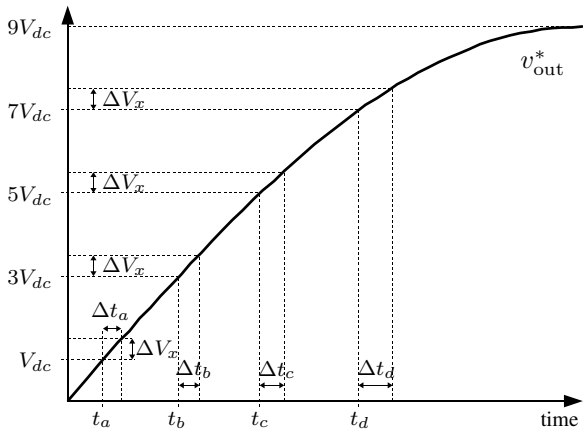


Fig. 21. Relationship between the output voltage reference and the time to switch the output voltage patterns.

It is assumed that $\Delta V_{HM} = \Delta V_{HL} = 0$. When ΔV_{ML} is used to transfer power from the MV cell to the LV cell, the HV cell's switching time does not change. That is expressed as

$$P_H = 0. \tag{54}$$

The MV cell's switching delays for Δt_a, Δt_c, and Δt_d, respectively. Then P_M is given by

$$\begin{aligned} P_M &= -\frac{2V_{dc} \cdot I \cos \omega t_a \cdot \Delta t_a}{\pi/2\omega} - \frac{2V_{dc} \cdot I \cos \omega t_c \cdot \Delta t_c}{\pi/2\omega} \\ &\quad - \frac{2V_{dc} \cdot I \cos \omega t_d \cdot \Delta t_d}{\pi/2\omega} \\ &= (-2V_{dc} - 2V_{dc} - 2V_{dc}) \frac{2\Delta V_{ML} I}{9\pi V_{dc}} \\ &= -\frac{4}{3\pi} \Delta V_{ML} I. \end{aligned} \tag{55}$$

(49), (54), and (55) yield the average power flowing into the LV cell P_L as follows:

$$\begin{aligned} P_L &= -P_H - P_M \\ &= \frac{4}{3\pi} \Delta V_{ML} I. \end{aligned} \tag{56}$$

The analysis shows that the operation of ΔV_{ML} causes energy transfer from the MV cell to the LV cell without any influence on the HV cell.

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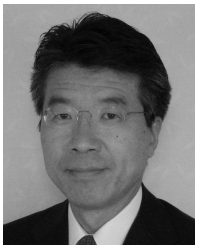
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