/

Article / Book Information

Title	Yield-aware mask assignment by positive semidefinite relaxation in triple patterning using cut process
Authors	Yukihide Kohira, Chikaaki Kodama, Tomomi Matsui, Atsushi Takahashi, Shigeki Nojima, Satoshi Tanaka
Citation(English)	Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3), Vol. 15, No. 2, pp. 1-7
/Pub. date	2016, 3
DOI	http://dx.doi.org/10.1117/1.JMM.15.2.021207
/Copyright	Society of Photo-Optical Instrumentation Engineers Copyright 2016 Society of Photo-Optical Instrumentation Engineers. One print or electronic copy may be made for personal use only. Systematic reproduction and distribution, duplication of any material in this paper for a fee or for commercial purposes, or modification of the content of the paper are prohibited.

Yield-aware mask assignment by positive semidefinite relaxation in triple patterning using cut process

Yukihide Kohira
Chikaaki Kodama
Tomomi Matsui
Atsushi Takahashi
Shigeki Nojima
Satoshi Tanaka

Yield-aware mask assignment by positive semidefinite relaxation in triple patterning using cut process

Yukihide Kohira,[a,*] **Chikaaki Kodama,**[b] **Tomomi Matsui,**[c] **Atsushi Takahashi,**[d] **Shigeki Nojima,**[b] **and Satoshi Tanaka**[b]
[a]University of Aizu, School of Computer Science and Engineering, Tsuruga, Ikki-machi, Aizu-Wakamatsu, Fukushima 965-8580, Japan
[b]Toshiba Corporation, Semiconductor and Storage Products Company, 2-5-1 Kasama, Sakae-ku, Yokohama 247-8585, Japan
[c]Tokyo Institute of Technology, Department of Social Engineering, 2-12-1-W9-98 Ookayama, Meguro-ku, Tokyo 152-8550, Japan
[d]Tokyo Institute of Technology, Department of Communications and Computer Engineering, 2-12-1-S3-58 Ookayama, Meguro-ku, Tokyo 152-8550, Japan

Abstract. LELECUT type triple patterning lithography is one of the most promising techniques in 14 nm logic node and beyond. To prevent yield loss caused by overlay error, LELECUT mask assignment, which is tolerant to overlay error, is desired. We propose a method that obtains a LELECUT assignment that is tolerant to overlay error. The proposed method uses positive semidefinite relaxation and randomized rounding technique. In our method, the cost function that takes the length of boundary of features determined by the cut mask into account is introduced. © *2016 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JMM.15.2.021207]

Keywords: triple patterning; LELECUT; design for manufacturability; positive semidefinite relaxation.

Paper 15181SSP received Nov. 15, 2015; accepted for publication Feb. 19, 2016; published online Mar. 11, 2016.

1 Introduction

Multiple patterning techniques enable us to fabricate small features without using advanced technologies such as extreme ultraviolet lithography. Triple patterning lithography (TPL) is one of the most promising techniques in 14 nm logic node and beyond. In order to realize a target pattern, various types of techniques including design for manufacturability such as LELE type double patterning lithograph,[1–7] LELELE type TPL,[8–20] LELECUT type TPL,[21–23] and sidewall process[24–29] are used in addition to a basic litho-etch process with optimized mask. These techniques are summarized in Refs. 30 and 31.

Sidewall process[24–29] forms a wall feature with unique width so that it surrounds the prefabricated polygon. The sidewall process that is used in self-aligned double patterning enables us to fabricate finer pattern pitch by combining a slimming process, but the variety of target patterns that can be fabricated is limited.

Two types of TPL technologies are often discussed in literature. In LELELE, litho-etch process is repeated three times. However, it is difficult to achieve high yield due to native conflict and overlay problems. In LELECUT, the third mask called cut (or trim) process removes a part of a fabricated pattern. It is used to improve the quality of fabricated patterns as well as to enhance the flexibility of the layout. However, it has overlay problems and lithographical limitations. In order to prevent yield loss caused by overlay error as much as possible, LELECUT mask assignment, which is tolerant to overlay error, is desired.

To the best of our knowledge, two LELECUT mask assignment methods have been proposed. In Refs. 21 and 23, LELECUT mask assignment problem is formulated as an integer linear programming problem. Although it minimizes the weighted summation of the number of conflicts and stitches, the effect of cuts on layout quality is not taken into account. In Ref. 22, LELECUT mask assignment

problem is solved by positive semidefinite relaxation. Although it minimizes the weighted summation of the number of conflicts, stitches, and polygons in the cut mask, the yield of obtained layout is also not discussed. Figure 1 shows mask assignments in LELECUT. A target pattern is shown in Fig. 1(a). The layouts obtained by two LELECUT mask assignments, which are represented by blue and magenta, and cut masks without overlay error, are shown in Figs. 1(b) and 1(d). These mask assignments have no conflicts, no stitches, and the number of polygons in the cut mask is the same. The layouts shown in Figs. 1(b) and 1(d) with overlay error, in which blue and magenta, and cut masks move to the lower left, the upper right, and the left, respectively, are shown in Figs. 1(c) and 1(e), respectively. The former is expected to have lower yield than the latter since a longer dimension of features such as p_1 and p_2 is determined by the cut mask and is affected directly by the overlay error. The length of a boundary of a feature that is determined by the cut mask should be small enough to prevent the yield loss caused by overlay error.

In this paper, we propose a method that obtains an LELECUT assignment, which is tolerant to overlay error. The proposed method is an enhancement of the method proposed in Ref. 22 and uses positive semidefinite relaxation and randomized rounding technique. In our method, the cost function that takes the length of boundary of features determined by the cut mask into account is introduced to obtain an overlay tolerant LELECUT assignment.

2 Preliminaries

2.1 Problem Definition

Let $P = \{p_1, p_2, \ldots, p_n\}$ be the set of polygons in a target pattern. A polygon may represent a polygon decomposed by given stitch candidates. A stitch edge is defined between two polygons if and only if two polygons are decomposed by a
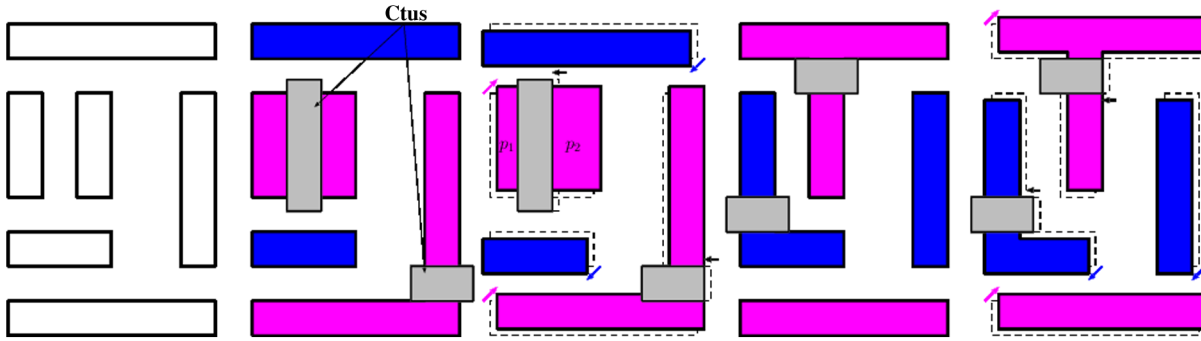

Fig. 1 Mask assignments in LELECUT. (a) A target pattern, (b) a mask assignment, (c) mask assignment shown in (b) with misalignment, (d) another mask assignment, (e) mask assignment shown in (d) with misalignment. Mask assignment shown in (c) has higher yield than that shown in (d).

stitch candidate. A polygon conflict edge is defined between two polygons if and only if two polygons are too close to assign the same mask. A cut candidate is defined between two polygons connected by a polygon conflict edge if and only if they can be cut by the cut mask when they are assigned to the same mask. A cut candidate c has a cost $l(c)$, which is defined by the length of boundary between polygons in the target pattern and the cut candidate. A cut candidate may not be independent of other cut candidates. A cut conflict edge is defined between two cut candidates if and only if they cannot be used simultaneously. Note that even if the distance between two cut candidates is not long enough, they can be used simultaneously if they can be merged into one. A cut conflict edge is not defined between two cut candidates if the distance between them is long enough or if they can be merged into one without affecting the critical dimension of the pattern. Let S, C_P, T, and C_T be the set of stitch edges, the set of polygon conflict edges, the set of cut candidates, and the set of cut conflict edges, respectively. Note that both the set of stitch edges S and the set of polygon conflict edges C_P are families of unordered pairs of polygons in P, the set of cut candidates T is a subset of the set of polygon conflict edges C_P, and the set of cut conflict edges C_T is a family of unordered pairs of cut candidates in T.

Figure 2 shows an example of the problem. In this example, $P = \{p_1, p_2, p_3, p_4\}$, $S = \{\{p_3, p_4\}\}$, and $C_P = T = \{c_1, c_2, c_3, c_4, c_5\}$, where $c_1 = \{p_1, p_3\}$, $c_2 = \{p_1, p_4\}$, $c_3 = \{p_1, p_2\}$, $c_4 = \{p_2, p_3\}$, and $c_5 = \{p_2, p_4\}$ with costs $l(c_1) = 2, l(c_2) = 2, l(c_3) = 1, l(c_4) = 2$, and $l(c_5) = 2$, respectively. The set of cut conflict edges is given by $C_T = \{\{c_1, c_2\}, \{c_1, c_3\}, \{c_2, c_3\}, \{c_3, c_4\}, \{c_3, c_5\}, \{c_4, c_5\}\}$.

In this paper, a polygon is assigned to one of the two masks except the cut mask. The problem of finding an assignment of polygons, and/or two-coloring, is essentially equivalent to a maximum cut problem. We employ a $\{-1, 1\}$ formulation represented by function $x : P \to \{-1, 1\}$, which is introduced by Goemans and Williamson[32] for a max cut problem. This formulation naturally yields a positive semidefinite relaxation appearing in Sec. 3. For two-coloring x, the set of polygon conflict edges that connect the same color polygons is represented by

$$C_P(x) \overset{\text{def.}}{=} \{\{p, q\} \in C_P | x(p) = x(q)\}.$$

Similarly, the set of stitch candidates that connect the different color polygons is represented by

$$S(x) \overset{\text{def.}}{=} \{\{p, q\} \in S | x(p) \neq x(q)\}.$$

The set of feasible cuts for two-coloring x is a subset of $C_P(x) \cap T$ and an independent set of cut graph (T, C_T). The problem we consider is given as follows:

P1: minimize

$$\alpha_1 |C_P(x) \setminus T'| + \alpha_2 |S(x)| + \alpha_3 \sum_{c \in T'} l(c)$$

$$= \alpha_1 |C_P(x)| + \alpha_2 |S(x)| - \alpha_1 \sum_{c \in T'} 1 + \alpha_3 \sum_{c \in T'} l(c)$$

$$= \alpha_1 |C_P(x)| + \alpha_2 |S(x)| + \sum_{c \in T'} (\alpha_3 l(c) - \alpha_1),$$

where α_1, α_2, and α_3 are the weights of the evaluations, subject to

- $x(p) \in \{-1, 1\}$ $(\forall\ p \in P)$,
- $T' \subseteq C_P(x) \cap T$,
- T' is an independent set of cut graph (T, C_T).

In this formulation, the weighted sum of the number of unresolved conflict edges, the number of caused stitches, and the total cost of used cut candidates is minimized. In the following, we assume that $\alpha_1 \geq \alpha_2 \geq 0$ and $\alpha_1 \geq \alpha_3 l(c) \geq 0$. According to this assumption, the total cost of used cut candidates is minimized under the condition that the number of conflict edges that connect the same polygons is minimized and the number of used cut candidates is maximized.
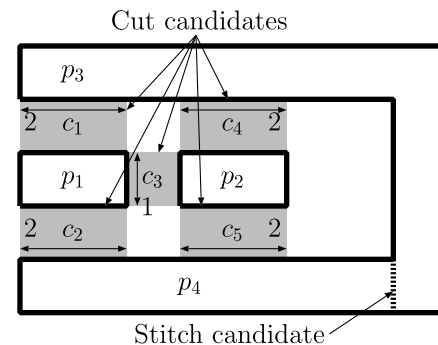

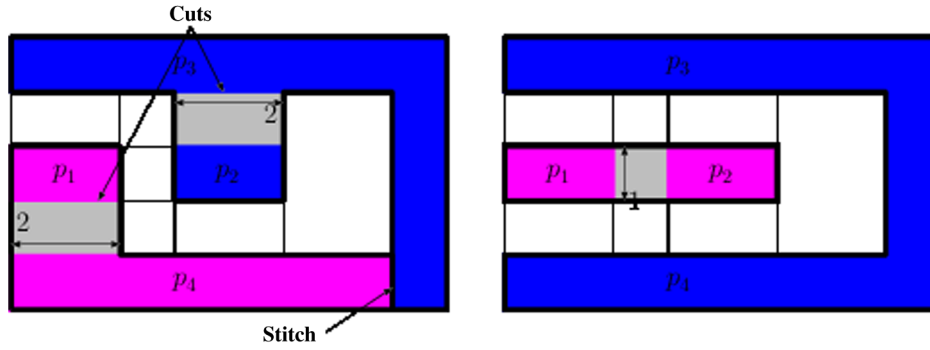**Fig. 2** Polygons with stitch and cut candidates.

Fig. 3 Mask assignments for layout in Fig. 2. (a) Two cuts with total cost 4 and one stitch and (b) one cut with total cost 1.

Figure 3 shows the examples of mask assignments. The mask assignment shown in Fig. 3(a) has two cuts with total cost 4 and one stitch. On the other hand, the mask assignment shown in Fig. 3(b) has one cut with total cost 1. Obviously, the mask assignment shown in Fig. 3(b) is better than that shown in Fig. 3(a).

2.2 *Maximum Independent Set with Minimum Total Cost Problem*

For a given two-coloring $x : P \rightarrow \{-1,1\}$, the problem P1 is equivalent to a maximum independent set with minimum total cost problem MISMTCP1 since we assume $\alpha_1 \geq \alpha_3 l(c)$.

MISMTCP1: maximize

$$\sum_{c \in T'}(1 - \alpha l(c)),$$

where α is a weight of the cut cost.

subject to

- $\alpha l(c) < 1$,
- $T' \subseteq C_P(x) \cap T$,
- T' is an independent set of cut graph (T, C_T).

A maximum independent set with minimum total cost problem is known to be NP-hard. In this paper, the following 1-0 integer linear programming MISMTCP2 is formulated by introducing 0-1 variable $y(c)$.

MISMTCP2: maximize

$$\sum_{c \in T}y(c) \cdot [1 - \alpha l(c)],$$

subject to

$$y(c) \in \{0,1\} \quad (\forall \, c \in T), \tag{1}$$

$$y(c) + y(c') \leq 1 \quad [\forall \, (c, c') \in C_T], \tag{2}$$

$$y(c) = 0 \quad [\forall \, c \in T \setminus C_P(x)]. \tag{3}$$

3 Positive Semidefinite Relaxation

3.1 *Outline of Proposed Method*

The outline of the proposed method is shown in the following.

Step 1: Formulate a positive semidefinite relaxation SDP-L.
Step 2: Solve SDP-L by SDP solver.
Step 3: Obtain a mask assignment by randomized rounding algorithm with iterative improvement.

The proposed method is based on the method proposed in Ref. 22. In the proposed method, a positive semidefinite relaxation of P1 called SDP-L is formulated and a mask assignment is obtained from an optimum solution of the relaxation by randomized rounding technique with iterative improvement. It is well known that a positive semidefinite programming problem can be solved by interior point methods in polynomial time.

3.2 *Our Semidefinite Relaxation*

In this section, we introduce a positive semidefinite relaxation of P1. Our relaxation is an enhancement of the formulation proposed by Goemans and Williamson[32] for a max cut problem to handle a maximum independent set with minimum total cost.

First, we represent the objective function of P1 as a linear function. An arbitrary two-coloring $x : P \rightarrow \{-1,1\}$, satisfies: $x(p) = x(q) \leftrightarrow x(p)x(q) = 1$ and $x(p) \neq x(q) \leftrightarrow x(p)x(q) = -1$. By using these properties, $|C_P(x)|$ and $|S(x)|$ are represented in terms of x as follows:

$$|C_P(x)| = \sum_{\{p,q\} \in C_P}\left(\frac{x(p)x(q)}{2} + \frac{1}{2}\right),$$

$$|S(x)| = \sum_{\{p,q\} \in S}\left(-\frac{x(p)x(q)}{2} + \frac{1}{2}\right).$$

Let X be the $n \times n$ matrix whose (p, q)'th element is $X_{pq} = x(p)x(q)(\forall \, p, \forall \, q \in P)$. Let C and S be the matrixes that represent polygon conflicts and stitch candidates, respectively. That is, C and S are the $n \times n$ symmetric matrixes, and

$$C_{pq} = \begin{cases} \frac{1}{4} & [(p,q) \in C_P], \\ 0 & [(p,q) \in C_P], \end{cases} \quad S_{pq} = \begin{cases} \frac{1}{4} & [(u,v) \in S], \\ 0 & [(u,v) \in S], \end{cases}$$

respectively. Then, we have

$$|C_P(x)| = \sum_{\{p,q\} \in C_P} \left(\frac{x(p)x(q)}{2} + \frac{1}{2} \right) = C \cdot X + \text{const},$$

$$|S(x)| = \sum_{\{p,q\} \in S} \left(-\frac{x(p)x(q)}{2} + \frac{1}{2} \right) = -S \cdot X + \text{const},$$

where $M \cdot M'$ is defined as $\sum_i \sum_j M_{ij} M'_{ij}$ for square matrixes M and M' of the same size. Let $y(c)$ be a 0-1 variable for a cut candidate c. c is assigned to the cut mask, if and only if $y(c) = 1$. Then, we have

$$\sum_{c \in T'} [\alpha_3 l(c) - \alpha_1] = \sum_{c \in T} y(c) \cdot [\alpha_3 l(c) - \alpha_1].$$

Therefore, the objective function of P1 is represented as

$$\alpha_1(C \cdot X) - \alpha_2(S \cdot X) + \sum_{c \in T} y(c) \cdot (\alpha_3 l(c) - \alpha_1) + \text{const}.$$

$$(4)$$

Note that C and S are the constant matrixes.

Next, the constraints of P1 are represented as linear functions in terms of X and y. Constraint (3) in MISMTCP2 is represented as

$$0 \leq y(c) \leq \begin{cases} 1 & [\text{if } c \in T \cap C_P(x)], \\ 0 & [\text{if } c \in T \setminus C_P(x)]. \end{cases}$$

Then, constraint (3) is represented by using two-coloring x as follows:

$$0 \leq y(c) \leq \frac{x(p)x(q)}{2} + \frac{1}{2} [\forall \ c = (p,q) \in T].$$

The representations of other constraints are straightforward, and P1 is represented as follows:

P2: minimize

$$\alpha_1(C \cdot X) - \alpha_2(S \cdot X) + \sum_{c \in T} y(c) \cdot (\alpha_3 l(c) - \alpha_1)$$

subject to

$$X_{pq} = x(p)x(q) \quad (\forall \ (p,q) \in P^2), \tag{5}$$

$$x(p) \in \{-1, 1\} \quad (\forall \ p \in P), \tag{6}$$

$$y(c) \in \{0, 1\} \quad (\forall \ c \in T), \tag{7}$$

$$y(c) + y(c') \leq 1 \quad (\forall \ \{c, c'\} \in C_T),$$

$$0 \leq y(c) \leq \frac{x(p)x(q)}{2} + \frac{1}{2} \quad (\forall \ c = \{p,q\} \in T).$$

The objective function of P2 is obtained from Eq. (4) by removing constant term. Note that $X_{pp} = 1$ for all $p \in P$.

Since X in P2 is a positive semidefinite symmetric matrix, the problem P2 has a positive semidefinite programming relaxation as follows. Let $\mathcal{S}_+^n$ be the set of $n \times n$ positive semidefinite symmetric matrix. A positive semidefinite relaxation problem SDP-L is obtained from P2 by restricting X within $\mathcal{S}_+^n$ and ignoring 0-1 constraints for y, instead of constraints (5), (6), and (7).

SDP-L: minimize

$$\alpha_1(C \cdot X) - \alpha_2(S \cdot X) + \sum_{c \in T} y(c) \cdot (\alpha_3 l(c) - \alpha_1)$$

subject to

$$X_{pp} = 1 \quad (\forall \ p \in P),$$

$$y(c) + y(c') \leq 1 \quad [\forall \ (c, c') \in C_T],$$

$$0 \leq y(c) \leq \frac{1}{2} X_{pq} + \frac{1}{2} \quad [\forall \ c = (p,q) \in T],$$

$$X \in \mathcal{S}_+^n.$$

SDP-L is a positive semidefinite programming problem and can be solved by interior point methods in polynomial time.

3.3 Randomized Rounding for LELECUT

In this section, we propose a randomized rounding technique based on the "hyperplane separation" technique proposed by Goemans and Williamson,[32] which gives 0.878 approximation algorithm for a max cut problem. The randomized rounding technique is based on the method proposed in Ref. 22, and the iterative improvement is applied as postprocessing.

For any positive semidefinite symmetric matrix $X \in \mathcal{S}_+^n$, there exists a matrix Z satisfying $X = Z^\top Z$. This decomposition is called Cholesky decomposition.

We solve problem SDP-L by an SDP solver and obtain an optimal solution $(\widetilde{X}, \widetilde{y})$ for SDP-L. Let $\widetilde{Z}^\top \widetilde{Z}$ be the Cholesky decomposition of $\widetilde{X}$ and d be the number of rows of $\widetilde{Z}$. Here, we note that columns of $\widetilde{Z}$ are indexed by polygons in P and the length of every column vector is equal to 1. For each polygon $p \in P$, vector $\vec{z}(p) \in \mathbb{R}^d$ denotes the corresponding column vector of $\widetilde{Z}$. Algorithm RR shown in the following outputs a two-coloring $\widetilde{x}: P \to \{-1, 1\}$ and the set $\widetilde{T}$ of cuts.

Algorithm RR

Step 1: Generate a random unit vector $\vec{u} \in \mathbb{R}^d$ (satisfying $\|\vec{u}\| = 1$).

Step 2: For each polygon $p \in P$, set

$$\widetilde{x}(p) = \begin{cases} 1 & [\text{if } \vec{u}^\top \widetilde{z}(p) > 0], \\ -1 & (\text{otherwise}). \end{cases}$$

Step 3: Construct a subgraph $\widetilde{G}$ of cut graph (T, C_T) induced by vertex subset $C_P(\widetilde{x}) \cap T$. Find a maximal independent set $\widetilde{S}$ of $\widetilde{G}$ by employing a heuristic algorithm for maximum independent set with minimum total cost problem.

Table 1 ISCAS benchmarks.

Circuit	|P|	# Seg	|C_P|	# Comp Total	# Comp Target	|T|
c432	850	4918	540	414	1	12
c499	1491	9518	1489	502	50	278
c880	1872	10,666	1422	717	168	934
c1355	2656	15,246	1514	1328	76	514
c1908	4191	24,370	3141	1733	182	1462
c2670	6371	37,564	5802	2056	585	4298
c3540	8188	47,244	6897	2896	775	4794
c5315	11,498	68,476	10,097	3926	1193	7552
c6288	11,605	64,762	5602	6259	256	1282
c7552	17,167	99,526	14,027	6258	1448	9325

Note: $|P|$ is the number of polygons; # Seg is the number of line segments; $|C_P|$ is the number of polygon conflict edges; total is the number of components in the conflict graph (P, C_P); target is the number of components in the conflict graph (P, C_P) in which cuts must be inserted; and $|T|$ is the number of cut candidates in the target components.

Step 4: Apply the greedy iterative improvement in which mask assignment of a polygon is changed and a heuristic algorithm for maximum independent set with minimum total cost problem is applied until the solution is not improved.

The mask assignment is modified by the greedy iterative improvement so that better solutions are obtained. The quality of the obtained mask assignment depends on the generated random unit vector and the runtime of Algorithm RR is very small. Therefore, Algorithm RR is repeated appropriate times and the best mask assignment is output. During the repetition, we might choose a comfortable mask assignment as well.

4 Experiments

Our proposed mask assignment method is implemented by using an SDP solver and C++ language. We compare the following five methods. ILP-# and ILP-L are the ILP formulations based on Ref. 21, which minimizes the number of cuts and minimizes the total cost of cuts, respectively. SDP-# is the positive semidefinite relaxation proposed in Ref. 22, which minimizes the number of cuts. SDP-L Imp and SDP-L are the proposed methods, which minimizes the total cost of cuts defined by the length of boundary between polygons in the target pattern and the cut candidate. SDP-L Imp applies the greedy iterative improvement as postprocessing and SDP-L does not. The methods are executed on a Linux machine with 12 GB memory by using Intel core i7-3770 of 3.40 GHz. In our implementation, SDP problems are solved by SDPA 7.3.8,[33] which is a free tool. On the other

Table 2 Experimental results. The obtained mask assignments have no polygon conflicts and cut conflicts in ILP-#, ILP-L, SDP-#, and SDP-L Imp. The units of cost and time are (nm) and (s), respectively.

Circuit	ILP-# |T'|	ILP-# Cost	ILP-# Time	ILP-L |T'|	ILP-L Cost	ILP-L Time	SDP-# |T'|	SDP-# Cost	SDP-# Time	SDP-L |T'|	SDP-L |C_P(x)|	SDP-L Cost	SDP-L Time	SDP-L Imp |T'|	SDP-L Imp Cost	SDP-L Imp Time
c432	1	40	0.01	1	40	0.01	1	40	0	1	0	40	0	1	40	0
c499	58	2720	0.42	58	2720	0.45	58	6030	0.12	62	0	2940	0.12	58	2720	0.15
c880	172	11720	2.46	198	10390	6.25	172	20590	0.44	202	2	11105	0.35	198	10390	0.51
c1355	90	9760	1.10	122	8320	6.10	90	13230	0.27	130	2	9635	0.17	122	8320	0.37
c1908	211	37700	5.77	373	30410	24.34	211	41140	0.73	411	13	36600	0.43	373	30410	1.37
c2670	686	76950	10.52	958	64710	38.98	686	101975	2.32	1069	66	84540	1.39	952	65775	5.26
c3540	821	73560	11.06	1044	63445	29.61	821	111330	2.24	1090	11	72630	1.47	1044	63445	3.02
c5315	1259	108290	17.52	1572	93965	53.23	1259	162510	3.59	1647	13	106280	2.33	1572	93965	4.11
c6288	256	10320	2.39	256	10240	2.33	256	29840	0.66	256	0	10240	0.45	256	10240	0.66
c7552	1587	162980	20.02	2122	138905	89.62	1587	221025	4.47	2243	23	159505	3.01	2122	138905	6.12
ave.	0.82	1.12	0.50	(1)	(1)	(1)	0.82	1.77	0.09	1.05		1.12	0.07	1.00	1.00	0.12

Note: $|T'|$ is the number of inserted cuts; $|C_P(x)|$ is the number of conflicts in the obtained mask assignment; cost is the total cost of cuts in the obtained mask assignment; time is the computational time; and ave. is the average normalized by ILP-L.

hand, ILP problems are solved by CPLEX 12.6.1,[34] which is one of the most famous commercial ILP solvers. In these methods, a speedup technique in which the conflict graph $(P, S \cap C_P)$ is decomposed into connected components is adopted. This speedup technique is discussed in many previous studies.[1–3,5,6,21,22] If a connected component has no conflict, it is assigned to the first mask. Therefore, the density of the first mask is much larger than that of the second mask. Although the density balance can be taken into consideration by enhancing the SDP relaxation method proposed in Ref. 15 that takes the density balance in LELELE into consideration, it will be part of our future work. In this experiment, we do not prepare stitch candidates to focus on observing the total cost, the number of cuts, and the number of conflicts. The parameters in objective functions are set to $\alpha_1 = 10^6$ and $\alpha_3 = 1$. $\alpha_1 = 10^6$ is much larger than cut costs. Algorithm RR is applied 100 times in SDP-#, SDP-L, and SDP-L Imp.

ISCAS benchmarks shown in Table 1, which were used in Refs. 3 and 5, are used. The benchmarks are reproduced from the information given by authors of Refs. 3 and 5 and from figures in Ref. 3, though we could not obtain the same data. We followed the parameters as in Refs. 3 and 5, where the minimum polygon space in a mask is 54 nm. If stitches are allowed to be inserted, the mask assignment without cuts is obtained. Therefore, we also do not insert stitches in this experiment. Table 2 shows the results. Note that the mask assignments obtained by all methods except SDP-L have no polygon conflicts and cut conflicts. Since the minimization of the total cost is added into the objective function of ILP-L, the total cost obtained by ILP-L is optimum. Similarly, since the minimization of cuts is added into the objective function of ILP-#, the number of cuts obtained by ILP-# is optimum. Although ILP-# and SDP-# obtain mask assignments with the minimum number of cuts, the total cost of the mask assignment obtained by them is larger than that by ILP-L since the minimization of cuts does not correspond to that of the total cost. Although SDP-L is fast, it obtains mask assignments with conflicts. The total cost of the mask assignment obtained by SDP-L Imp is the same as that by ILP-L in 9 out of 10 circuits. Moreover, SDP-L Imp is much faster than ILP-L. Consequently, SDP-L Imp obtains optimum solutions in the shortest computational time in almost all circuits.

5 Conclusions

In this paper, we propose a fast LELECUT mask assignment method to be tolerant to overlay error. The proposed method applies a positive semidefinite relaxation. The experimental results show the efficiency and the validity of the proposed method. We will take the mask density balance, stitch direction, and so on into account to improve the quality of the mask assignment in our future works.

References

1. A. Kahng et al., "Layout decomposition for double patterning lithography," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD 2008)*, pp. 465–472 (2008).
2. K. Yuan, J.-S. Yang, and D. Pan, "Double patterning layout decomposition for simultaneous conflict and stitch minimization," in *Proc. of the Int. Symp. on Physical Design (ISPD)*, pp. 107–114 (2009).
3. J.-S. Yang et al., "A new graph-theoretic, multi-objective layout decomposition framework for double patterning lithography," in *Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pp. 637–644 (2010).
4. S.-Y. Chen and Y.-W. Chang, "Native-conflict-aware wire perturbation for double patterning technology," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 556–561 (2010).
5. X. Tang and M. Cho, "Optimal layout decomposition for double patterning technology," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 9–13 (2011).
6. Y. Kohira et al., "Yield-aware decomposition for LELE double patterning," *Proc. SPIE* **9053**, 90530T (2014).
7. Y. Yokoyama et al., "Localization concept of re-decomposition area to fix hotspots for LELE process," *Proc. SPIE* **9053**, 90530V (2014).
8. B. Yu et al., "Layout decomposition for triple patterning lithography," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 1–8 (2011).
9. S.-Y. Fang, Y.-W. Chang, and W.-Y. Chen, "A novel layout decomposition algorithm for triple patterning lithography," in *ACM/EDAC/IEEE Design Automation Conf. (DAC)*, pp. 1181–1186 (2012).
10. Q. Ma, H. Zhang, and M. Wong, "Triple patterning aware routing and its comparison with double patterning aware routing in 14 nm technology," in *Proc. of the 49th Annual Design Automation Conf. (DAC)*, pp. 591–596 (2012).
11. H. Tian et al., "A polynomial time triple patterning algorithm for cell based row-structure layout," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 57–64 (2012).
12. Y.-H. Lin et al., "TRIAD: a triple patterning lithography aware detailed router," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 123–129 (2012).
13. J. Kuang and E. Young, "An efficient layout decomposition approach for triple patterning lithography," in *50th ACM/EDAC/IEEE Design Automation Conf. (DAC)*, pp. 69:1–69:6 (2013).
14. Y. Zhang et al., "Layout decomposition with pairwise coloring for multiple patterning lithography," in *Proc. of the Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 170–177 (2013).
15. B. Yu et al., "A high-performance triple patterning layout decomposer with balanced density," in *Proc. of the Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 163–169 (2013).
16. H. Tian et al., "Constrained pattern assignment for standard cell based triple patterning lithography," in *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 178–185 (2013).
17. B. Yu et al., "Methodology for standard cell compliance and detailed placement for triple patterning lithography," in *Proc. of the Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 349–356 (2013).
18. T. Matsui et al., "Positive semidefinite relaxation and approximation algorithm for triple patterning lithography," *Lect. Notes Comput. Sci.* **8889**, 365–375 (2014).
19. B. Yu et al., "Layout decomposition for triple patterning lithography," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **34**(3), 433–446 (2015).
20. B. Yu et al., "Methodology for standard cell compliance and detailed placement for triple patterning lithography," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **34**(5), 726–739 (2015).
21. B. Yu, J.-R. Gao, and D. Z. Pan, "Triple patterning lithography (TPL) layout decomposition using end-cutting," *Proc. SPIE* **8684**, 86840G (2013).
22. Y. Kohira et al., "Fast mask assignment using positive semidefinite relaxation in LELECUT triple patterning," in *20th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pp. 665–670 (2015).
23. B. Yu et al., "Triple-patterning lithography (TPL) layout decomposition using end-cutting," *J. Micro/Nanolith. MEMS MOEMS* **14**(1), 011002 (2015).
24. C. Kodama et al., "Self-aligned double and quadruple patterning aware grid routing with hotspots control," in *18th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, pp. 267–272 (2013).
25. F. Nakajima et al., "Detailed routing with advanced flexibility and in compliance with self-aligned double patterning constraints," *Proc. SPIE* **8684**, 86840A (2013).
26. F. Nakajima et al., "Self-aligned quadruple patterning-aware routing," *Proc. SPIE* **9053**, 90530C (2014).
27. F. Nakajima et al., "Self-aligned quadruple patterning-compliant placement," *Proc. SPIE* **9427**, 942708 (2015).
28. T. Ihara, A. Takahashi, and C. Kodama, "Rip-up and reroute based routing algorithm for self-aligned double patterning," in *Proc. the 19th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI 2015)*, pp. 83–88 (2015).

29. T. Ihara, A. Takahashi, and C. Kodama, "Effective two-dimensional pattern generation for self-aligned double patterning," in *2015 IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 2141–2144 (2015).
30. B. Yu et al., "Dealing with IC manufacturability in extreme scaling," in *Proc. of the Int. Conf. on Computer-Aided Design (ICCAD)*, pp. 240–242 (2012).
31. A. Takahashi et al., "Multi patterning techniques for manufacturability enhancement in optical lithography," in *Proc. the 2014 Int. Conf. on Integrated Circuits, Design, and Verification (ICDV 2014)*, pp. 117–122 (2014).
32. M. X. Goemans and D. P. Williamson, "Improved approximation algorithms for maximum cut and satisfiability problems using semidefinite programming," *J. ACM* **42**, 1115–1145 (1995).
33. SDPA Project, "SDPA ," 7.3.8, http://sdpa.sourceforge.net/ (21 January 2013)
34. IBM, "CPLEX Optimizer," 12.6.1, http://www-01.ibm.com/software/commerce/optimization/cplex-optimizer/ (2014).

Yukihide Kohira is a senior associate professor at the University of Aizu. He received his BE, ME, and DE degrees from Tokyo Institute of Technology, Tokyo, Japan, in 2003, 2005, and 2007, respectively. His research interests are in VLSI design automation and algorithms. He is a member of ACM, IEEE, IEICE, and IPSJ.

Chikaaki Kodama is an engineer at the Toshiba Corporation, Semiconductor and Storage Products Company. He received his BE, ME, and DE degrees in electronic and information engineering from Tokyo University of Agriculture and Technology in 1999, 2001, and 2006, respectively. His current research interests include design for manufacturability, especially mask optimization and multiple patterning for optical lithography. He is a senior member of IEEE and IEICE.

Tomomi Matsui is a professor at the Tokyo Institute of Technology. He received his DS degree in systems science from Tokyo Institute of Technology in 1992. He had been with Tokyo University of Science from 1990 to 1992, with University of Tokyo from 1992 to 2006, with Chuo University from 2006 to 2013, and with Tokyo Institute of Technology from 2013. His research interests include combinatorial optimization algorithms. He is a member of ORSJ, JSS, and IPSJ.

Atsushi Takahashi is a professor at the Tokyo Institute of Technology. He received his BE, ME, and DE degrees in electrical and electronic engineering from Tokyo Institute of Technology in 1989, 1991, and 1996, respectively. He had been with Tokyo Institute of Technology from 1991 to 2009 and from 2012, and with Osaka University from 2009 to 2012. His research interests include VLSI design and algorithms. He is a member of IEEE, ACM, IEICE, and IPSJ.

Shigeki Nojima is a quality expert at the Toshiba Corporation, Semiconductor and Storage Products Company. He received the MS degree in mineralogy from the University of Tokyo in 1994. He has worked for Toshiba Corporation, where he is engaged in development of lithography, optical proximity correction, verification, design for manufacturability, and CAD for emerging lithography. He is a member of SPIE.

Satoshi Tanaka is a senior specialist at the Toshiba Corporation, Semiconductor and Storage Products Company. He received his MS degree in nuclear engineering from the University of Tokyo in 1992 and joined ULSI Research Center of Toshiba Corporation. He had engaged in research and development of optical lithography simulation field, and his current interest includes computational lithography. He is now temporarily transferred to the EUVL Infrastructure Development Center.