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著者(和文)	LEIYIMING
Author(English)	Lei Yiming
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論 文 要 旨

THESIS SUMMARY

専攻： Department of	物理電子システム創造　専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of	(engineering)
学生氏名： Student's Name	LEI YIMING	指導教員（主）： Academic Supervisor(main)	角嶋　邦之	
		指導教員（副）： Academic Supervisor(sub)	筒井　一生	

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis is titled with「A Study on Atomic Layer Deposited SiO_2 for SiC Gate Dielectrics」, and contains 8 chapters. The abstract of each chapter is as follow:

The first chapter introduced the background of SiC semiconductor devices. Silicon carbide (SiC) is a promising candidate for replacing traditional Si semiconductor, owing to its superior physical characteristics such as wide bandgap and high thermal conductivity. However, SiC has long been suffered from low interface properties between gate dielectrics and SiC. The reported methods to improve interface characteristics such as nitride oxide (NO_x) gas annealing and high temperature oxidation has been introduced and unsolved issue for gate dielectrics on SiC has been discussed. On the other hand, the problem of uneven gate oxide by thermal SiO_2 on trench MOSFET has been introduced, and the advantage of using ALD-SiO_2 to suppress oxide thickness fluctuation has been discussed. Based on the above introduction, the purpose and structure of this thesis have also been presented in this chapter.

The second chapter introduced fabrication processes and physical analysis methods of SiC devices in this thesis. The evaluation methods for electrical characteristics like interface state density (D_{it}) for MOS-capacitor and electron mobility for MOSFET has also been introduced in this chapter.

The third chapter introduced the precursor selection of ALD-SiO_2 deposition. Although residual carbon (C) density in deposited film is higher than other candidates for the precursor, tris(dimethylamino)silane (TDMAS) is chosen as the precursor material attribute to its high vapor pressure and high thermostability. The process parameter, the deposited ALD-SiO_2 film properties and dielectric breakdown property have been discussed. With O_2 plasma as an oxidant for the deposition, a fine ALD-SiO_2 film can be deposited with low interface roughness of 0.3nm, density of 2.4g/cm^3 and high breakdown filed of 8MV/cm.

The fourth chapter discussed the properties of SiC capacitors with ALD-SiO_2 gate dielectrics. Although post-deposition annealing (PDA) improved characteristics of ALD-SiO_2 with higher temperature has been found, the improvement is limited and further improvement is still necessary. On the other hand, post-metallization annealing (PMA) successfully reduced fixed charge and hysteresis at relatively low temperature compared with thermal oxidation. Furthermore, with long time annealing at 950^{o}C, a low D_{it} of 10^{11}cm^{-2}/eV magnitude can be achieved, which is considered to be an extremely low value for

deposition gate dielectrics. Based on the results, a model has been presented that PMA achieved low oxygen partial pressure in oxide film by electrode layer capped annealing, which consistently suppressed interface oxidation that generates new C and removed residual C in ALD-SiO_2 dielectrics at the same time.

The fifth chapter discussed the enhanced oxidation effect with La_2O_3 insertion for SiC. The reaction process of deposited La_2O_3 reacted with SiC substrate, formed with La-silicate and thick SiO_2 has been introduced. A model has been presented that radical oxygen generated by the catalytic effect of La_2O_3 enhanced oxidation of SiC. Although reaction formed La-silicate agglomerated at the interface, an insertion of ALD-SiO_2 interface layer with deposition of ALD-SiO_2 capping layer on La_2O_3 successfully suppressed the La_2O_3 agglomeration and reduced interface roughness. Also, the residual C density in ALD-SiO_2 was reduced to 1/10 with catalytic effect by radical oxygen during the annealing.

The sixth chapter introduced the properties of SiC capacitors with ALD-SiO_2 and interface La-silicate gate dielectrics. The D_{it} has been reduced with La-silicate and large reduction of oxide trap density has been achieved with the insertion of La-silicate. Base on physical analysis, La atoms diffusion into the region that more than 10nm away from La-silicate/ALD-SiO_2 interface, the existence of La atom in ALD-SiO_2 layer may be critical for the trap density reduction with La-silicate interface.

The seventh chapter introduced electrical characteristics of SiC MOS structure with ALD-SiO_2/ La-silicate interface layer. With a combination of PMA treatment and La-silicate interface layer, an ideal flatband voltage, less than 20mV hysteresis voltage, and low Dit of $2.6\times10^{11}\mathrm{cm}^{-2}/\mathrm{eV}$ for MOS-capacitor has been obtained. High mobility over $16\mathrm{cm}^2/\mathrm{Vs}$ for MOSFET has also been demonstrated based on electron mobility evaluation, indicated that high quality deposited gate dielectrics is achievable for SiC power devices.

The eighth chapter is the conclusion that summed up the research achievement in this thesis, and discussed the further work for realizing high mobility and better interface properties of SiC power devices.