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A Study on Atomic Layer Deposited SiO_2 for SiC Gate Dielectrics

Tokyo Institute of Technology
Interdisciplinary Graduate School of Science and Engineering
Dissertation for the Degree of Doctor of Engineering

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Prof. Kazuo Tsutsui

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Candidate: Yiming Lei

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ABSTRACT

Silicon carbide (SiC) is a promising candidate for high-efficiency power device application. However, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) using silicon dioxide (SiO_2) as gate dielectrics suffer from degraded mobility and reliability issues. Furthermore, for the application of trench SiC MOSFETs, the crystalline face dependent oxidation rate of SiC may cause reliability issue by introducing uneven SiO_2 insulator inside the trench gate structure. Deposited gate dielectrics can be a promising method for replacing the thermally grown SiO_2 for trench SiC MOSFETs. However, the electrical properties of the deposited gate dielectric are still insufficient. Quality improvements of the deposited gate dielectric are the key point for its application on SiC devices.

In this study, the properties of gate dielectrics for SiC power devices using atomic layer deposition (ALD) method with SiO_2 and La-silicate interface layer have been investigated by multiple physical and electrical analyses. Deposition of ALD-SiO_2 has been conducted with a precursor of tris-dimethylamino-silane (TDMAS) and an oxidant of O_2 remote plasma. The roughness of ALD-SiO_2 is much smaller than that of thermally grown SiO_2, which is the unique advantage of ALD process.

Electrical properties of SiC capacitors using ALD-SiO_2 gate dielectrics have also been studied. A high flat-band voltage with wide hysteresis voltage indicates the existence of large trap density in the ALD-SiO_2 layer. However, significant properties improvements can be achieved by post-deposition annealing (PDA) and post-metallization annealing (PMA) treatment. A low interface state density (D_{it}) of 3×10^{11} cm^{-2}/eV has been achieved for SiC capacitors with sufficient PMA treatments. The out-diffusion of oxygen atoms from the gate electrode as well as the intake of oxygen molecules from the environment

are believed to be the sources to compensate the defects in the ALD-SiO_2. Secondary-ion mass spectroscopy (SIMS) analysis has revealed that residual carbon density in the ALD-SiO_2 layer has been reduced significantly with PMA treatment, which may be the origin of the electrical properties improvements. Field effect electron mobility of 12 cm^2/Vs has been achieved for SiC MOSFET with ALD-SiO_2, which is comparative to the one with SiC MOSFETs using thermally grown SiO_2 gate dielectrics.

Although annealing processes improve the properties of the ALD-SiO_2 layer as well as the interface, further elimination of residual carbon atoms is considered to be important. Lanthanum silicate (La-silicate) is known to generate radical oxygen during oxygen annealing, which can be used for further carbon-related traps reduction. Since the interface reaction of La_2O_3 on SiC has not been clarified, the reaction of La_2O_3 with SiC substrate was investigated firstly by Fourier transform infrared analyses. Formation of La-silicate has been confirmed and an enhanced oxidation of SiC substrate has also been found with La_2O_3 capping annealing. However, the formed La-silicate agglomerated on an unevenly formed SiO_2 layer, which should be attributed to facet dependent oxidation on SiC substrate. Suppression of the oxidation fluctuation can be achieved with ALD-SiO_2 capping and ALD-SiO_2 IL insertion, which should be attributed to the reduction of SiC substrate oxidation. ALD-SiO_2 with La_2O_3 capping revealed a reduction of residual in ALD-SiO_2, and La atoms diffuse into the layer of ALD-SiO_2. The incorporation of residual C reduction and La atoms diffusion may attribute to the electrical properties improvement of SiC MOS devices.

Stacking of an ALD-SiO_2 on a La-silicate layer has been investigated as gate dielectrics for SiC capacitors. Uniform La-silicate can be realized with SiO_2-capped annealing at the low annealing temperature. A reduction of oxide trap density by two orders of magnitude

by La-silicate insertion has been achieved. Since La-silicate has been demonstrating to reduce the residual C concentration in ALD-SiO2, and La atoms diffusion in ALD-SiO_2 has been observed by EELS, the electrical properties improvement by La-silicate insertion can be attributed to both carbon density reduction and La atom incorporation in the oxide layer.

Radical oxygens generated by the La-silicate layer reduce the carbon density in ALD-SiO_2 and also enhance the oxidation of SiC substrate. Therefore, the formation of an uneven SiO_2 interface layer (IL) may degrade the electrical properties. This issue can be solved by insertion of a thin film of ALD-SiO_2 between the SiC substrate and the La-silicate layer. With thin SiO_2 IL, a significant improvement of border trap and interface state density reduction can be achieved. A D_{it} value of 2.6×10^{11} cm^{-2}/eV indicated the interface defects has been suppressed significantly. Also, the flat-band voltage of SiC capacitor with La-silicate/IL ALD-SiO_2 showed an ideal theoretical value after PMA treatment, which should be attributed to the significant reduction of the bulk trap in gate dielectrics. A field effect electron mobility of 16.3 cm^2/Vs for SiC MOSFET with La-silicate/IL-SiO_2 layer has been achieved.

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Chapter 1

Introduction

1.1 Introduction of SiC semiconductor and its application

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1.1 Introduction of SiC semiconductor and its application

Silicon carbide (SiC) is one of the IV-IV group element semiconductor, which was first artificially synthesized by Acheson in 1882 [1-1]. Silicon carbide powder has been mass-produced since 1893 for use as an abrasive [1-1]. Electronic applications of SiC as light-emitting diodes (LEDs) and detectors in early radios were first demonstrated around 1907 [1-1]. In 1940, a publication by Seitz "Theory of solids" introduced the notion of semiconductor, which has also stated the possibility of SiC as a semiconductor [1-1].

In the 1950s, driven by the huge demand of developing semiconductor devices capable of high-temperature operation, the research of SiC semiconductor devices has started. However, due to lack of high-quality wafers and a series of problems, the research of SiC semiconductor device get stuck. At the same time, the technology of Si semiconductor devices developed rapidly, the research of SiC devices was set aside for a long time. However, benefit from the technology of bulk crystal growth and step controlled epitaxy in the 1980s, the study of SiC revitalized. In the 1990s, crystal growth structure, elucidation of step control epitaxy, precise control of impurity doping, all the basic technology has been settled. The research of SiC semiconductor device has had a big breakthrough.

SiC is a compound semiconductor with a stoichiometric ratio of Si: 50%, C: 50%. The interatomic distance between Si and C is as short as 0.189 nm, which has a high bonding energy of 4.5 eV. Due to this high bonding energy, SiC has extremely high hardness only less than diamond. From semiconductor physics side of view, the high bonding energy gives SiC the nature of wide bandgap and high electrical breakdown field. Table.1.1.1 shows a comparison of basic physics parameter of silicon and 4H-SiC [1-1]. From which we could see, SiC has a wide bandgap of 3.26 eV and a high breakdown field of 2.8

MV/cm which is 10 times larger than that of Si. The saturated electron velocity of SiC is also two times of that of Si. A wide bandgap and fine thermal stability makes SiC suitable for power devices for high-temperature operation. High breakdown filed means SiC is has overwhelming characteristic for power device application over traditional silicon semiconductor. High saturated velocity also shows the possibility for improving the performance of high frequency operation devices.

Material	Si	4H-SiC
E_g (eV) Bandgap	1.12	3.26
E_{BD} (10^6V/cm) Breakdown field	0.3	2.8
μ(cm^2/Vs) mobility	1450	900
υ_{sat} (10^6 cm/s) Saturated electron velocity	10	22
κ(W/cmK) Thermal conductivity	1.2	5

Table 1.1.1 Comparison of basic parameters of silicon and 4H-SiC [1-1]

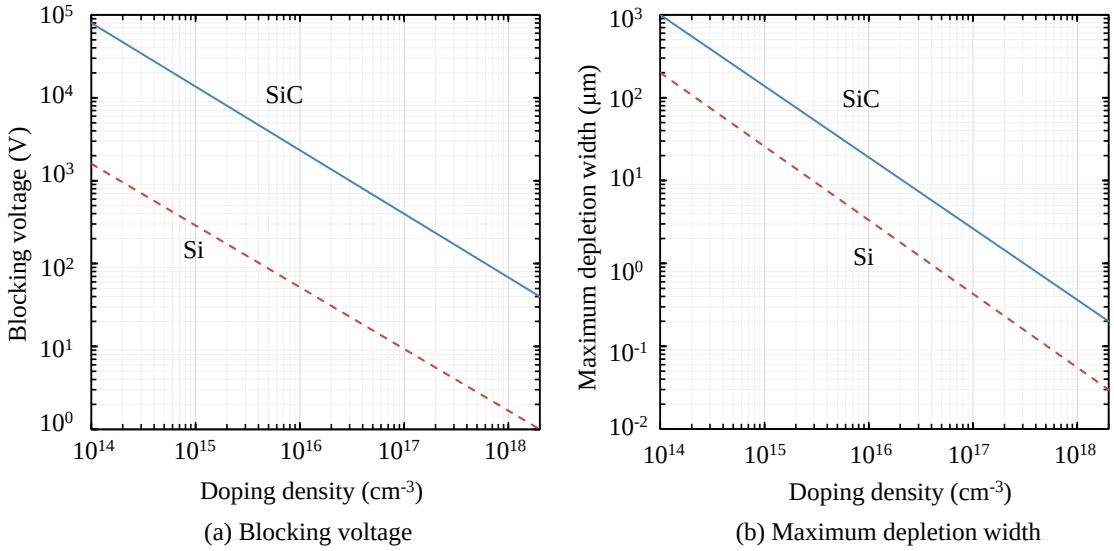


Fig 1.1.2 Relation of doping density of Si and 4H-SiC with (a) blocking voltage (b) maximum depletion width, based on theoretical dielectric breakdown field [1-1]

Fig 1.1.2 shows the relation of doping density in a pn junction in consideration of theoretical dielectric breakdown field of 4H-SiC. Fig 1.1.2 (a) shows the relation of blocking voltage and Fig 1.1.2 (b) shows the relation of maximum depletion width with doping density respectively. For contrast, the characteristic of silicon has also been shown at the same time. For having blocking voltage of 1000 V, the necessary doping density of SiC is about 2×10^{16} cm^{-3} and 2×10^{14} cm^{-3} for Si [1-1]. Under the condition, the depletion width for SiC and Si is 8 μm and 80 μm, respectively. From the comparison, it is clear that SiC has significantly better characteristic over traditional silicon semiconductor.

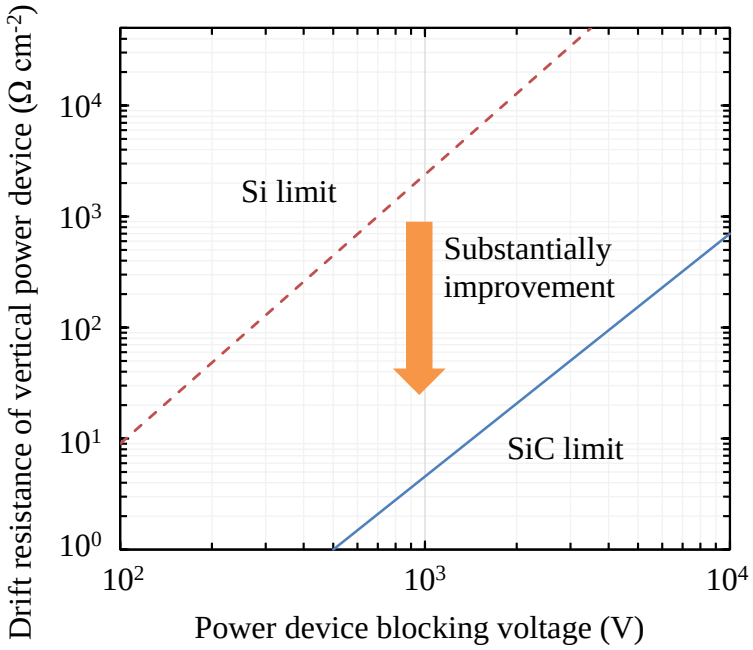


Fig 1.1.3 Relation of ON resistance of 4H-SiC and Si vertical power MOS device per unit area with blocking voltage

In application field of power devices, the on-resistance is a critical parameter to evaluate the electrical characteristic of the device. Fig 1.1.3 shows the relation of ON-resistance of 4H-SiC and Si vertical power MOS device per unit area with blocking voltage. Under same blocking voltage, a dramatical reduction of drift resistance by 1/300 ~1/500 can be achieved by replacing Si power device to SiC power device (for the unipolar device), which demonstrate SiC should be a promising material for power devices.

As the classification of traditional silicon power devices, for silicon diode, Schottky barrier diode (SBD) was used under 200 V blocking voltage, beyond this voltage, PiN diode was utilized. For switching devices, 300 V and 600 V is the border for application of unipolar Si device to bipolar Si device. On the other hand, a blocking voltage of

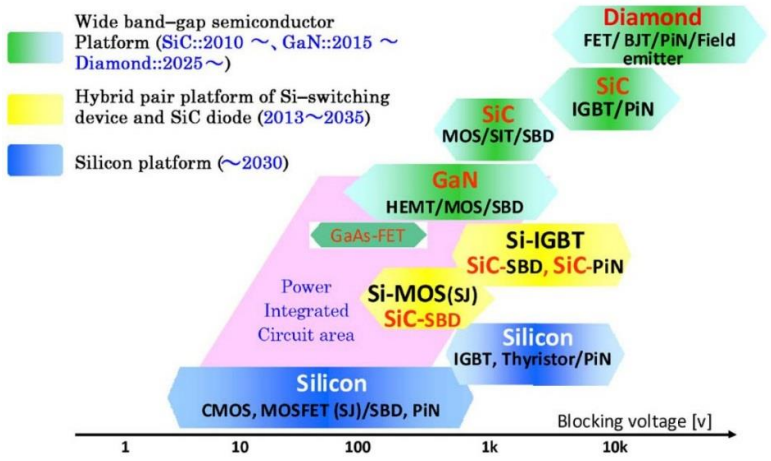


Fig 1.1.4 Application field and trend of semiconductor power devices

unipolar SiC power devices over 5 kV is applicable. For SiC PiN diode and Insulated Gate Bipolar Transistor (IGBT), ultra-high voltage application over 5 kV is predicted. Fig 1.1.4 shows the application field and trend of power density for different kind of semiconductor power devices [1-2]. The combination of Si-switching devices and SiC freewheeling diodes is applicable for higher blocking voltage and higher power density. For applications of blocking voltage over 10kV, whole power devices using SiC IGBT/PiN is potential to be used, which can be applied at higher power density at the same time.

Now the performance of silicon power devices is reaching the limitation of the material of silicon. An innovation in material or new technology is highly demanded for power devices applications. Due to the excellent physics nature of SiC, such as wide bandgap, high breakdown field, high saturated electron velocity and thermal conductivity, SiC power devices are able to operate under high temperature, high frequency, high voltage with a smaller size and with far fewer energy losses. A huge

energy saving effect can be achieved by shifting from Silicon power devices to SiC-based power devices, which could be a significant improvement for the construction of environmentally friendly society.

1.2 Degraded electron mobility issue for SiC power devices and relations with interface state density

A unique advantage of SiC over other wide bandgap semiconductor is the ability of SiC to grow SiO_2 by thermal oxidation, which is advantageous for device fabrication using traditional silicon process. However, SiC MOSFETs using thermally grown SiO_2 dielectrics suffers from low electron mobility problem. Most of reported the channel electron mobility of SiC MOSFETs using thermally grown SiO_2 still at the level of 10 cm^2/Vs~40 cm^2/Vs [1-3,1-4]. This low inversion channel mobility inevitably leads to much higher on resistance of SiC power devices [1-5, 1-6].

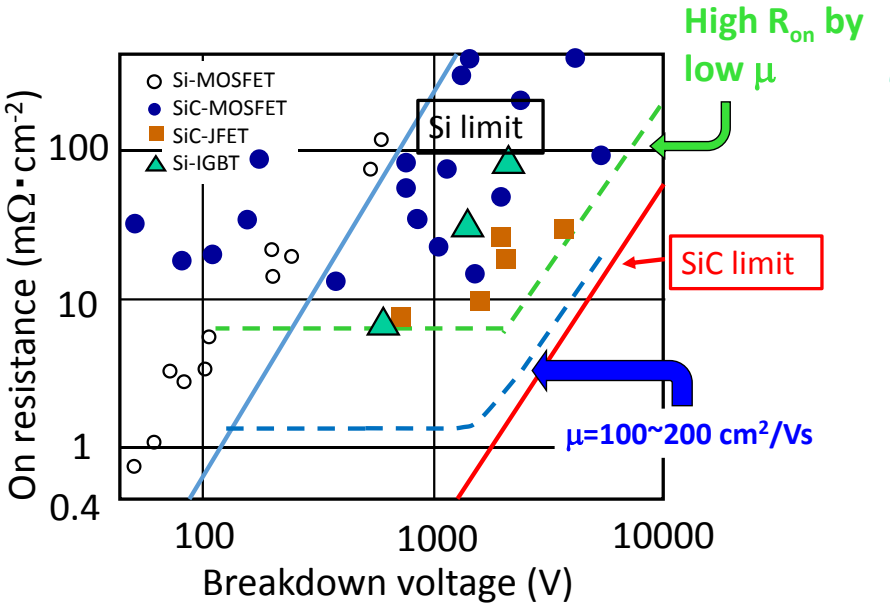


Fig 1.2.1 *The relationship of each switching devices' on resistance with breakdown voltage.*

Fig 1.2.1 shows the relationship of each switching devices' on resistance with breakdown voltage. The blue point and brown point refer to the on resistance and blocking voltage of SiC MOSFET and JFET, respectively. As shown in the figure, the on resistance of SiC MOSFET is still comparatively high. This kind of increase of on-resistance more clear at the low voltage region, which is because of the increase ratio of channel resistance in the whole on resistance, due to the low electron mobility of SiC devices. In order to reach the performance limit of SiC material, mobility of 100 to 200 cm^2/Vs is necessary. Improvement in the channel mobility is critical for achieving high-performance SiC power devices.

Lots of evidence shows that this poor electron mobility should be attributed to high D_{it} near the interface of SiO_2 and SiC [1-7]. Many models have been proposed to explain the defect mechanism at SiC/SiO_2 interface. Carbon defect has been suspected as one of the reasons for interface state density. During thermal oxidation of silicon carbide, most of the excess carbon is believed to be transferred to CO molecules leaving the interface by diffusion. However, some of the carbon atoms can remain at the interface and form carbon clusters or graphitic regions [1-8, 1-9, 1-10]. Oxide defects are also considered resulting in the D_{it} at the upper part of the bandgap in SiC. V. V. Afanas'ev et al., found that the high D_{it} occurring near the SiC conduction band edge originates from oxide defects located close to the interface and suggested that these defects are responsible for the observed mobility degradation [1-11, 1-12]. This kind of defect may result from the oxidation vacancy, or from the dangling bond originates from the lattice mismatch of SiO_2 with SiC. Many reports have shown that there is a strong relationship of D_{it} with electron mobility for SiC MOS-devices [1-13, 1-14, 1-15, 1-16]. An inverse proportional relationship of D_{it} and electron mobility can be easily summarized for increasing of

mobility with reduction of D_{it}. It is clear that to achieve high electron mobility, reduction of D_{it} down to 10^{11}~10^{10} cm^{-2}/eV magnitude is necessary for high-performance SiC power devices.

Numerous interface treatment has been applied to reduce the interface traps at the SiO_2/SiC interface. Annealing in ozone ambient has been found effective for reducing interface state density for SiC MOS capacitor. During annealing process, ozone molecules are thermally dislocated into radical oxygen, leading to a passivation effect on the SiO_2/SiC interface. R. Kosugi et al [1-17] introduced a mix oxygen/ozone gas annealing into oxidation furnace, where the atomic oxygen was formed by thermal decomposition of the O_3 molecules at elevated temperatures. The oxidation at 1200°C results in the significant reduction of the D_{it}. Consequently, the D_{it} near conduction band-edge was reduced in the oxidation of atomic oxygen compared to that of O_2.

Besides ozone, hydrogen thermal treatment has also shown a *D*it reduction effect of SiC devices. Annealing in H_2. In Si MOS technology, it is well known that H_2 annealing terminates dangling bonds of Si at the SiO_2/Si interface and reduces *D*it of MOS structures. Tsuchida et al. reported that the clear absorption bands of the Si-H stretching vibrations were observed from the 6H-SiC (0001) surface after H_2 annealing at temperatures between 1073 K to 1273 K [1-18]. This suggests that hydrogen effectively terminates the dangling bonds of Si or C atoms at the SiO_2/SiC interface after annealing at high-temperature. *D*it reduced to one-fifth has been achieved by annealing in H_2 at 1000°C compared with a sample without H_2 treatment [1-19].

NO or N_2O gas annealing is one of the most effective methods for SiC surface passivation. Nitridation of SiC surface has been attributed as the most considerable reason for *D*it reduction by NO, N_2O gas annealing [1-20, 1-21, 1-22]. By introducing N doping

in SiC MOS interface, termination of dangling bonds of Si or C atoms and removal of carbon residues can be promoted, which lead to a reduction of D_{it} and negative fix charge and improved effective electron mobility [1-23]. The mechanism of NO_x gas annealing interface passivation has been studied for a long time, the previous study found that the NO_x annealing can reduce the carbon-related defect near the SiC/SiO_2 interface [1-24]. A recent study shows that the reduction of near interface states (NIT) by NO can also be explained in terms of the counter doping effect [1-25], which effectively reduce the effects of surface roughness scattering. However, surplus N doping shifts the flat-band voltage, which was attributed to the influence of fix charge in gate dielectric induced by SiON, SiN compound near gate oxide/SiC interface [1-26]. Despite that the channel mobility of 4H-SiC MOSFET can be improved significantly by NO_x gas annealing, the channel mobility is still far low compared with the bulk mobility of 4H-SiC. The report shows that high concentration of residual carbon with the percentage of 25% still exists in the film of SiO_2 after NO gas annealing for 2 hours [1-27], which means that NO gas annealing still cannot effectively eliminate the residual carbon in the SiO_2 film. The elimination of residual carbon in SiO_2 gate oxide on SiC may be an important issue for further mobility improvement.

Beside NO and N_2O gas annealing, phosphorous atoms either by $POCl_3$ annealing has also been reported to reduce *D*it and achieved high inversion layer mobility of 75~100 cm^2/Vs [1-28]. However, a severe negative threshold voltage (V_{th}) shift has been observed after positive bias at elevated temperature. This is because a polar material phosphosilicate glass (PSG) has been formed by P_2O_5 with SiO_2 after annealing, which induced threshold voltage instabilities.

Recently, a report from X. Yang, et al, [1-29] shows that by using lanthanum silicate (La-silicate) as the interface layer between SiO_2 and SiC substrate, a significantly reduced *D*it can be achieved. Fig 1.2.1 shows the interface state density with and without La-silicate interface layer. One magnitude reduction of D_{it} is presented in comparison of that without La-silicate IL, due to the passivation effect of La-silicate dielectric. Another study of using La-silicate passivation layer for 4H-SiC MOS-capacitor with Al_2O_3 gate dielectrics reported that a lower leakage current density, a high electric breakdown electric field, a smaller *C–V* hysteresis has been obtained with La-silicate passivation [1-30]. However, D_{it} and border trap density of SiC capacitor with La-silicate IL are as high as 10^{13} cm^{-2}/eV and 10^{12}~10^{13} cm^{-2}/eV, respectively. For SiC power devices using La-silicate IL, the clear elucidation of passivation mechanism of La-silicate is necessary.

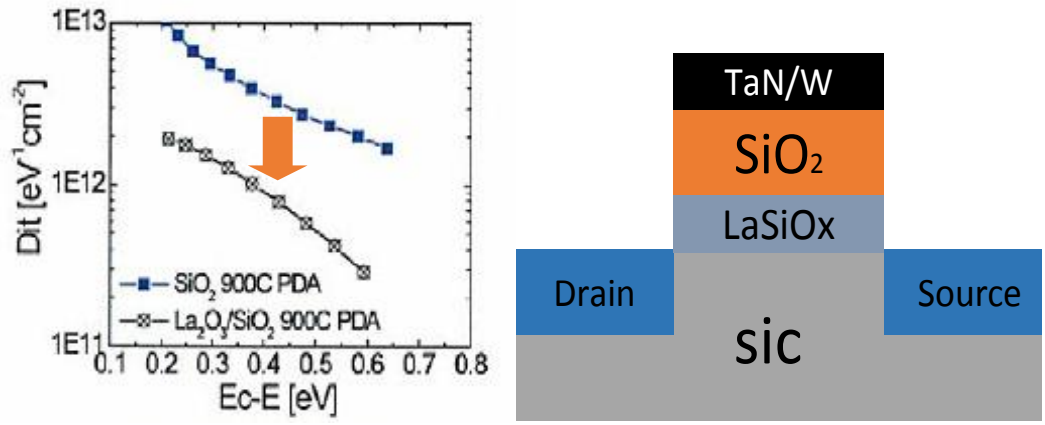


Fig 1.2.2 D_{it} of sample with and without La-silicate IL (Terman method) [1-26]

Here, we summarize the peak mobility and threshold voltage of reported MOSFET in figure 1.2.2. As shown in the figure, for SiC MOSFETs without treatment after SiO_2 formation by dry and wet oxidation. The peak mobility stays at the poor value of lower than 10 cm^2/Vs. For SiC MOSFETs with dry oxidation formed SiO_2 followed with NO_x

gas annealing. The mobility of MOSFETs firstly increased to 28 cm^2/Vs, however, the further mobility increase on the sacrifice of the threshold voltage. The threshold voltage decreases with the increase of annealing time. The same problem happens for SiC MOSFETs with PSG interface passivation, a high mobility of 80 cm^2/Vs but with threshold voltage shift to negative value. X. Yang, et al, reported high peak mobility of SiC MOSFETs of a value of 139 cm^2/Vs without significant degradation of the threshold voltage. However, the C-V characteristics of the capacitor with La-silicate IL revealed high hysteresis voltage of 500~1000 mV and high D_{it} of 10^{12}~10^{13} cm^{-2}/eV [1-29]. The passivation mechanism of the La-silicate layer on SiC MOS-devices is still necessary to be elucidated.

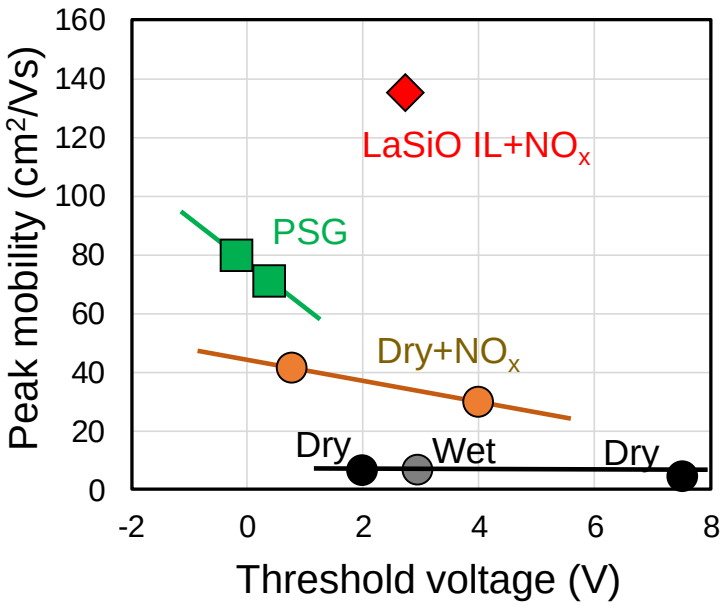


Figure 1.2.2 Reported peak channel electron mobility with threshold voltage of SiC MOSFET, from reported data of PSG [1-28], *LaSiO* [1-29], *Dry/Wet* [1-31], *NO_x* [1-32].

1.3 Material selection of deposited gate dielectric on SiC power devices

Although it is capable for SiC to form thermally grown SiO_2 by oxidation, a facet dependent oxidation happens when oxidation occurs at multiple crystalline planes. For SiC trench MOSFET, oxidation of 3D gate structure will cause oxidation fluctuation, which may cause serious reliability problems. Deposited gate dielectric may be a promising candidate for replacing thermally grown SiO_2 for trench MOSFET. Since the deposition can be operated at low temperature and facet dependent oxidation can be avoided.

For the application of deposited gate dielectrics on SiC power devices, sufficient band offset between gate dielectrics and SiC in the view of band structure is necessary in order to prevent large leakage current from the gate electrode. Since the bandgap of SiC is normally 3 times larger than Si, the bandgap of candidate material should also be big enough to support large band offset between gate dielectrics with SiC. Figure 1.3.1 shows bandgap and dielectric constant data for various gate oxides [1-33]. Most of the materials in the diagram are dielectrics with high permittivity, namely high-k dielectrics, which are useful for reducing gate leakage current for Si MOSFET devices [1-34]. However, the bandgap of dielectric material is in inverse proportion to the dielectric constant, as illustrated in fig 1.3.1. During the selection of deposition gate dielectrics on SiC, large bandgap and band offset is the necessary requirement. SiC MOS-capacitor using HfO_2 and SiON stacked gate dielectric has been reported in 2007 [1-35]. Less number of trapped charges are shown for the capacitor with HfO_2/SiON gate dielectrics and comparable values of interface state density has been achieved. However, until now there is no report about SiC MOSFET using HfO_2 as gate dielectrics. The band structure of HfO_2/SiC has been studied with x-ray photoelectron spectroscopy (XPS) and density

functional theory (DFT) [1-36]. XPS measurement shows that the conduction band offset (ΔE_c) of HfO_2 and SiC is only 0.7 eV, DFT simulation shows that the ΔE_c with Si-terminated face and C-terminated face is 0.35 eV and 0.97 eV, respectively. The insufficient band offset of HfO_2 on SiC may enlarge the leakage current, which makes it difficult to realize the advantage of HfO_2 for SiC power devices. Compared with HfO_2, Al_2O_3 is a promising material for gate dielectric using in MOS structure on SiC, considering its large bandgap of 8 eV. A SiC MOSFET using metal-organic chemical vapor deposited (MOCVD) Al_2O_3 gate dielectrics has been reported [1-37]. A high electron mobility of 284 cm^2 /Vs has been obtained with Al_2O_3 deposited at 150^oC and a thin layer of SiO_2 interface formed by low temperature annealing at 600^oC. However, the mobility of the SiC MOSFET using Al_2O_3 degrade rapidly with the increasing annealing temperature. Considering that sufficient annealing temperature is necessary for the following process such as ohmic contact annealing for the gate electrode. The electrical properties of SiC MOSFET using Al_2O_3 is difficult to control and may cause reliability issue. A stacked gate dielectric structure of aluminum oxynitride (AlON) /SiO_2 on 4H-SiC MOSFET has been reported in 2011 [1-38]. The leakage current in the AlON/SiO_2 MOS capacitor is much lower than the NO_x-SiO_2 at both room temperature and 200°C, especially in high-electric-field condition. However, a reduction of mobility has been found for AlON/SiO_2 MOSFET compared with MOSFET with NOx-SiO_2. Further electrical properties improvement is necessary for MOSFET with AlON/SiO_2 gate dielectrics. Recently, A SiC-MOSFET fabricated with ALD-SiO_2 using 3-aminopropyltriethoxysilane (APTES) as precursor has been reported [1-39]. A mobility of 25 cm^2/Vs has been achieved for ALD-SiO_2 with N_2O gas annealing. With uniform

layer formation capability on trench structure by ALD process, ALD-SiO_2 can be a promising candidate for gate dielectric on 4H-SiC trench MOSFET.

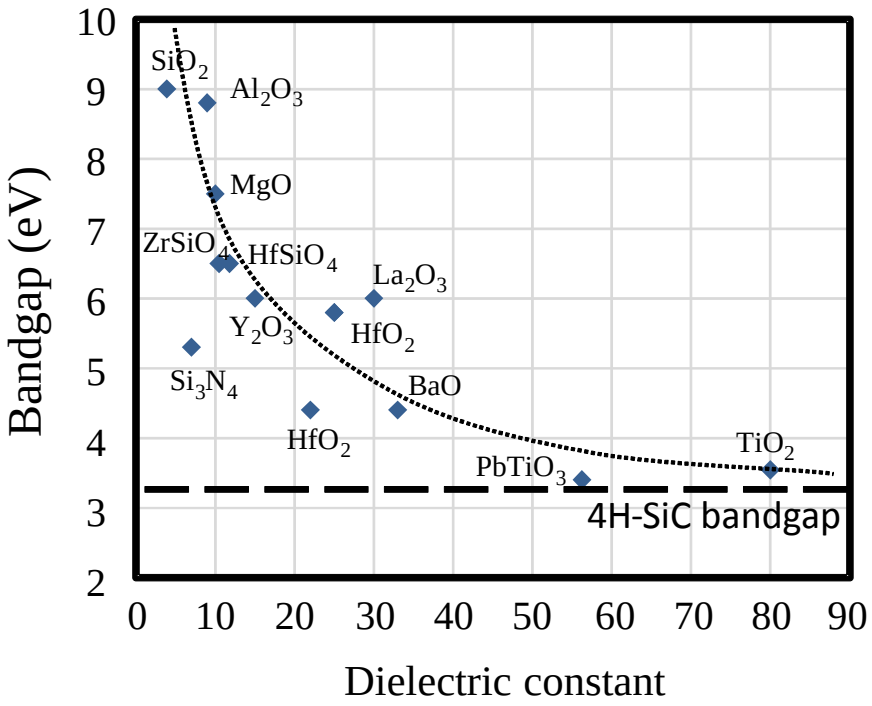


Fig 1.3.1 Static dielectric constant versus band gap for candidate gate oxides [1-30]

1.4 Purpose and outline of this thesis

To achieve large scale industrialization of SiC power devices, improvements in the gate oxides for SiC MOS-channel is critically important for high-performance SiC power devices. ALD-SiO_2 is a promising candidate for SiC trench MOSFET gate dielectrics. But serious electrical properties issues of ALD-SiO_2 is still unsolved, including large trap density induced by high concentration of carbon residue in the deposited SiO_2 layer or SiO_2/SiC interface. Annealing in oxygen ambient can be one method to reduce carbon residue concentration in the dielectric layer, the control of annealing condition is a key for large electrical properties improvement. Also, La-silicate is promising to reduce

carbon residue concentration in ALD-SiO_2 layer with the generation of radical oxygen to remove carbon by the reaction. However, the reaction mechanism of La-silicate is still unknown on SiC substrate. In this study, electrical characteristic improvement of SiC MOS-structure by Tungsten capped annealing and La-silicate layer insertion has been discussed. A large reduction of the residual carbon atoms in ALD-SiO_2 has been achieved by tungsten capped annealing and also electrical properties improvements by La-silicate dielectric cooperation have been found including a significant reduction of oxide trap density.

This thesis consists of 8 chapters. In chapter 1, SiC semiconductor and its issues for the application have been introduced. Mobility degradation with thermal grown SiO_2 is one of the issues for SiC MOSFET devices and many efforts has been made for mobility modification. For SiC trench MOSFET, large oxidation fluctuation by facet dependent oxidation on trench gate structure is the main problem. Deposited gate dielectrics are promising candidates for solving the issue by avoiding oxidation of SiC substrate. In chapter 2, the common experiment process used in this study is described.

In chapter 3, the deposition properties of ALD-SiO_2 has been investigated. A deposition of SiO_2 by atomic layer deposition (ALD) is achieved with the precursor of TDMAS (Tris-dimethylamino-silane) and oxidant of O_2 plasma. Deposited SiO_2 density is 2.32g/cm^3, which is well in agreement with the density of thermal grown SiO_2.

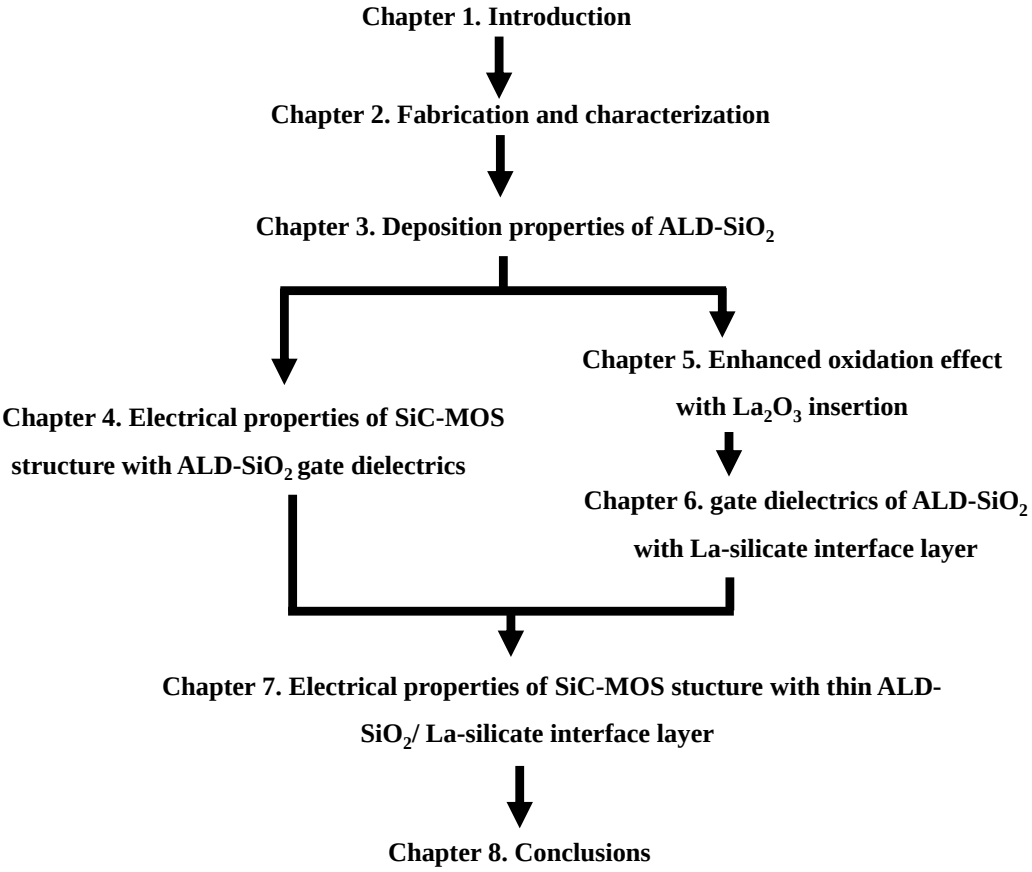
Chapter 4 describes electrical properties of SiC-MOS structures with ALD-SiO_2 gate dielectrics. High concentration of carbon residue is the main issue for ALD-SiO_2 gate dielectric on SiC. A huge reduction of carbon concentration in ALD-SiO_2 has been achieved by tungsten capped annealing and low D_{it} of 10^{11} /eVcm^2 has been confirmed.

In chapter 5, the enhanced oxidation by La_2O_3 on SiC has been discussed. The reaction of La_2O_3 and SiC was investigated firstly by La_2O_3 capping annealing on SiC substrate in O_2 ambient. Formation of La-silicate has been confirmed by TEM image and XPS analysis. An enhanced oxidation rate that about two orders of magnitude higher than thermal oxidation of SiC substrate have also been found with La_2O_3 capping annealing. Generation of radical oxygen by La-silicate should be the reason for oxidation enhancement. Although facet dependent oxidation happened during the annealing, the oxidation fluctuation can be suppressed by ALD-SiO_2 capping and ALD-SiO_2 IL insertion. Physical analysis of ALD-SiO_2 with La_2O_3 capping annealing revealed a diffusion of La atoms and reduction of C concentration in ALD-SiO_2, which may be the reason for ALD-SiO_2 electrical properties improvement with La_2O_3 dielectric.

In chapter 6, Electrical properties of SiC MOS-capacitor with ALD-SiO_2 and La-silicate interface layer has been investigated. Conductance method revealed improvement in the D_{it} and the reduction in the surface potential fluctuation with the La-silicate IL. Moreover, two orders of magnitude reduction in the N_{ot} in the ALD-SiO_2 layer adjacent to the La-silicate IL was confirmed. The origin of the improvements with La-silicate IL may be attributed to both carbon density reduction and La atom incorporation in oxide layer discussed in the last chapter.

In chapter 7, a new gate dielectric structure of SiO_2/La-silicate/SiO_2 has been proposed and investigated. With the insertion of a thin SiO_2 interface layer, significant improvement of electrical properties including both reduction of *D*it and oxide trap density has been found. Also, the electron mobility of SiC planar MOSFET has been improved to 16.3 cm^2/Vs, indicating La-silicate interface layer and modified annealing process can effectively improve the electrical properties of SiC MOS-structure power devices.

Finally, in chapter 8, conclusions and prospects for future work are summarized. Chapter structure in this thesis is summarized in the following chart.



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Chapter 2 Fabrication and characterization

2.1 Experiment procedure

Fig. 2.1.1(a) shows the typical fabrication flow of SiC capacitor samples used in this study. *n*-SiC (0001) substrates are first cleaned by SPM and HF treatment. For samples with SiO_2 interface layer, a thin film of SiO_2 with a thickness of 1nm to 8 nm was firstly deposited by ALD process. After that, one layer of La_2O_3 with a thickness ranging from 2 nm to 10 nm was deposited by electron beam (EB) evaporation. ALD-SiO_2 with thickness of 40 nm was then deposited on top of La-silicate. Then, samples were annealed in O_2 ambient at 900°C to 1100°C for 30 min. A 50-nm-thick W layer was deposited by magnetron sputtering, followed by 50-nm-thick TiN capping layer to protect the surface against oxidation. The metal layers were patterned by reactive ion etching (RIE) using Cl_2 and Ar chemistry to form gate electrodes. Backside contact was formed by thermal evaporation with a 50-nm-thick Ni layer. Post-metallization-annealing (PMA) was then carried out at 950°C by rapid thermal annealing (RTA) in forming gas (N_2: H_2=97%: 3%) ambient up to 5×10^3 secs. A gate electrode area of 50×50 μm^2 was used to measure the C-V characteristics. Further analysis has also been conducted to show more properties of ALD-SiO_2 and La-silicate on SiC substrates. For comparison, sample without la_2O_3 has also been fabricated and measured. Fig. 2.1.2(a) shows the sample structure fabricated by this process. Fig. 2.1.1(b) show the experiment procedure for SiC MOSFET. SiC substrate with S/D doping has been used in this study. The procedure of SiC MOSFET before gate patterning is as same as SiC MOS-capacitor. After gate patterning by RIE, a photoresist was coated on the SiC substrate, followed by lithography for patterning the contact region for source and drain electrodes. A wet etching by BHF was followed for remove of insulator on the S/D electrode area. Photoresist was coated on SiC sample by spin coating again follow with lithography. And after then Ni electrode for S/D contact was deposited

by sputtering. Then a lift-off process is followed to remove photoresist and excess Ni on SiC-MOSFET samples. After that sample was treated with PMA process in F.G gas ambient for 0-5000 s. And finally, SiC MOSFET was measure by electrical properties and physical analysis method.

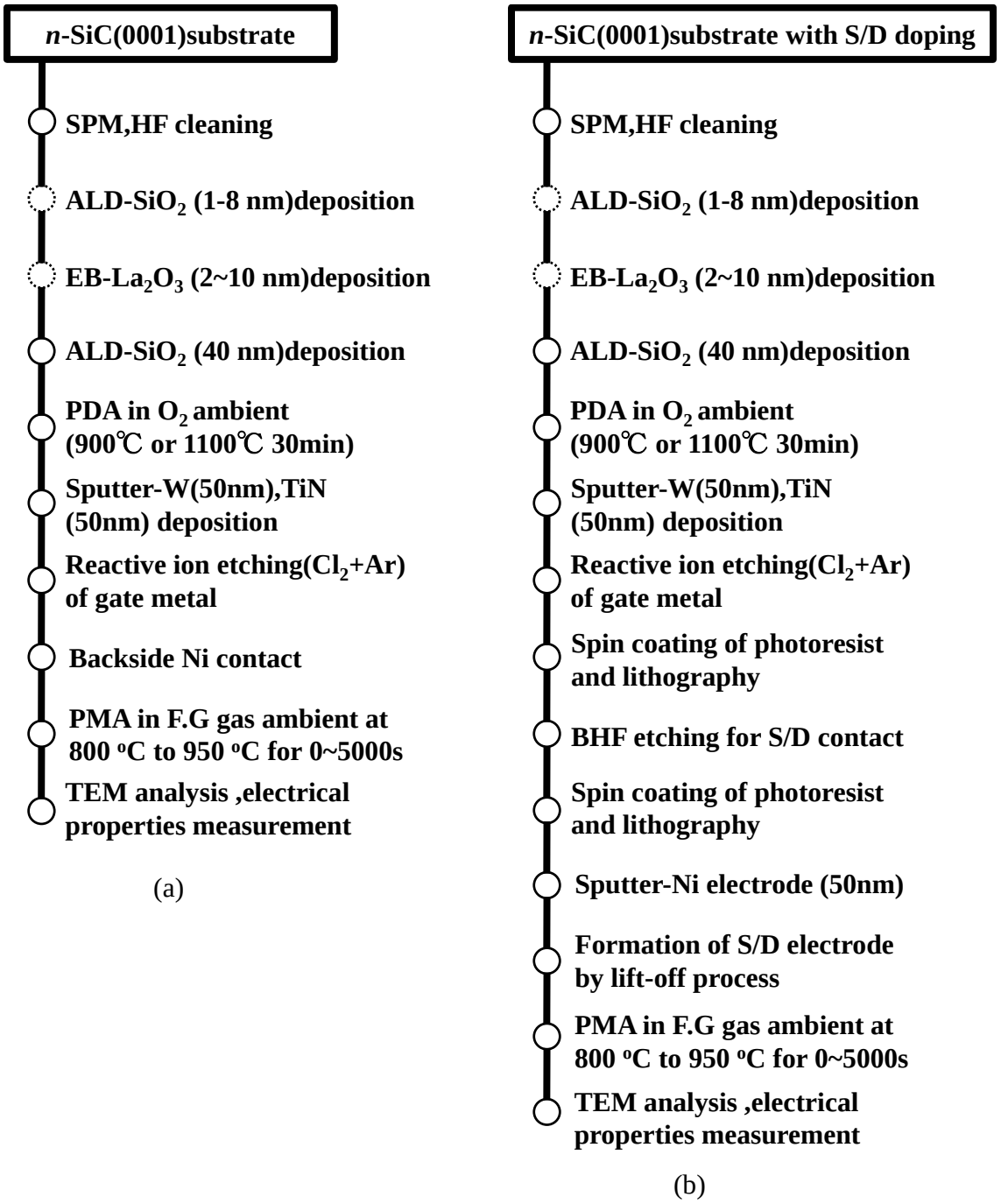
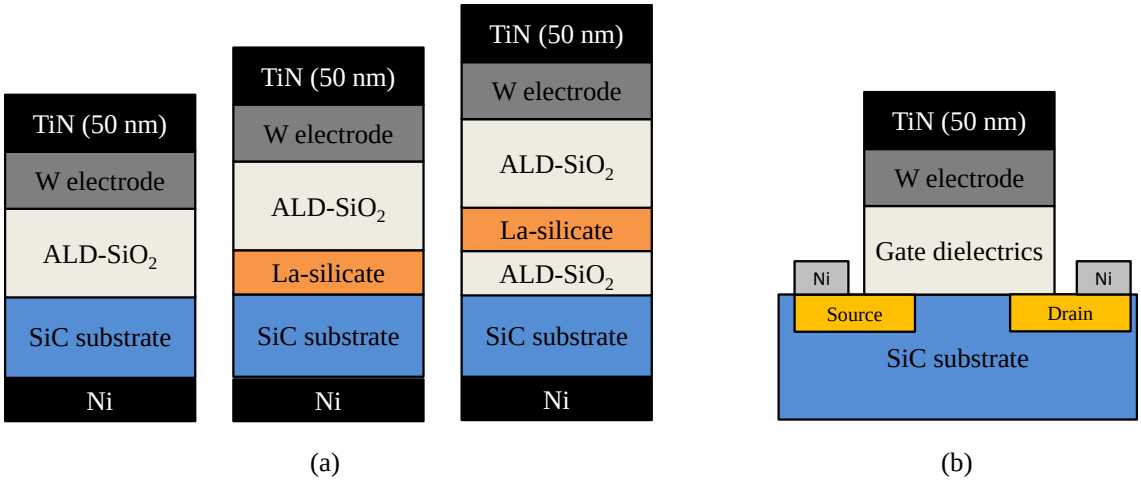


Fig 2.1.1 Fabrication procedure (a) SiC MOS-capacitor (b) SiC MOSFET



(a) (b)

Fig 2.1.2 sample structure (a) SiC MOS-capacitor (b) SiC MOSFET

2.2 Experiment process

2.2.1 Surface cleaning

Pretreatments for the wafer sample is necessary as the substrate before pretreatment basically has pollution of inorganic pollution such as metal and nature oxide film, organic pollution and so on. Sulfuric acid-hydrogen peroxide mixture (SPM) treatment, using piranha solution which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), is effective for removing organic residue on the substrate surface. It will also hydroxylate the substrate surface, making the substrate highly hydrophilic.

Hydrofluoric acid (HF) treatment is another pretreatment process for removing inorganic pollutions on the substrate. Due to the acid property, hydrofluoric acid is able to remove most metal residues and oxides on the substrate. HF treatment is often followed after SPM treatment.

In this study, the solution radio of H_2SO_4 and H_2O_2 is set to 3:1, fresh solution heat up to 180℃was used, the sample was treated in H_2SO_4/H_2O_2 solution for 4 minutes for removing organic pollutions. After SPM treatment, samples were set into 20% HF for 2

minutes to removing residue particle and metal pollutions.

2.2.2 Electron beam evaporation (EB)

EB is a method using in this study for deposition of La_2O_3 on SiC substrate. The illustration of deposition by EB has been shown in Figure 2.2.1. The source of La_2O_3 was set on a water-cooled holder, Electron beam generated by heated-filament was accelerated by high electron filed. After circular motion in a magnetic field, electron beam hit on source ingot. Sources were then transformed into gaseous phase and coating on the sample surface.

In this study, the deposition of La_2O_3 was conducted in high vacuum under 10^{-6} Pa. The sample holder was slowly rotated to ensure the deposited La_2O_3 was uniform. A shutter was used for start and stop the deposition.

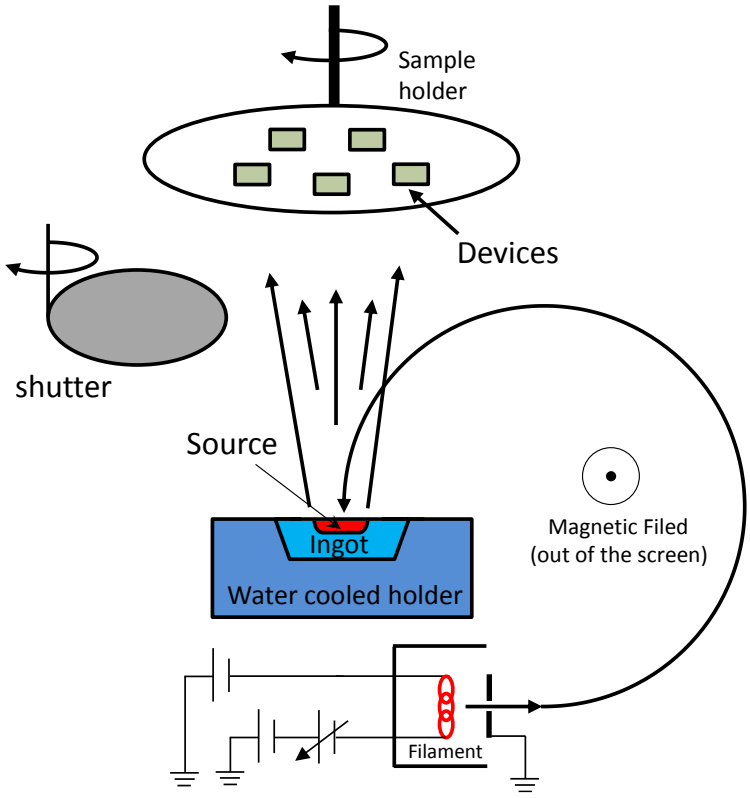


Fig 2.2.1 Illustration of La_2O_3 deposition by electron beam

2.2.3 Rapid thermal annealing (RTA)

PMA is a thermal treatment conducted by RTA. After deposition of the gate electrode by sputtering. The samples were send into rapid thermal annealing chamber for annealing. The temperature curve in annealing process is shown in Fig 2.2.2. A rapid heating rate was obtained by high-intensity lamps. In this study, annealing temperature from 500ºC to 1000ºC is used for the annealing with forming gas (FG) gas and 5%O_2/95% N_2 mixture gas.

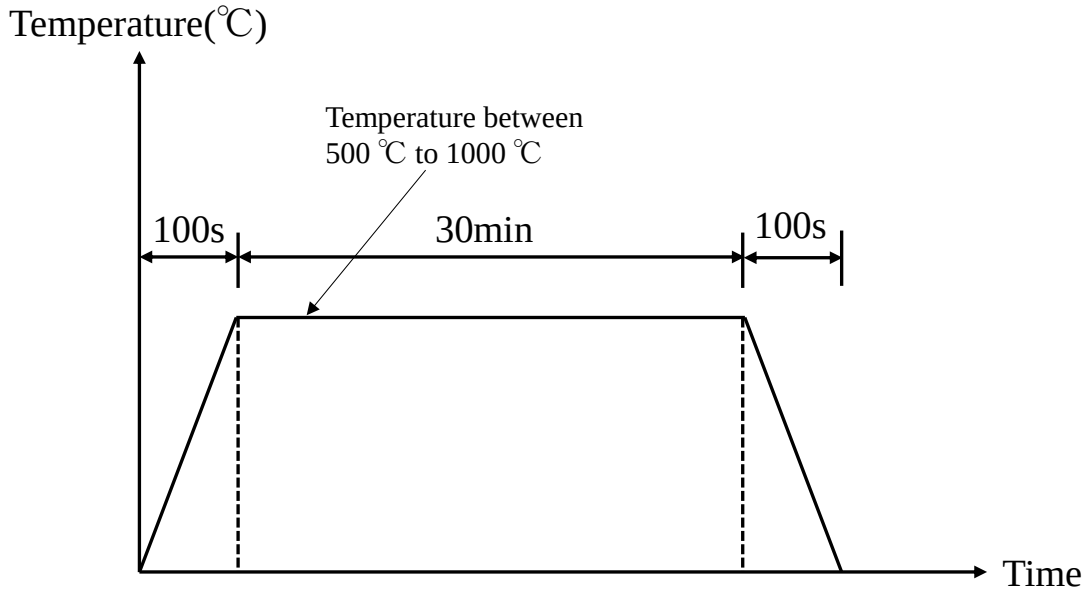


Fig 2.2.2 temperature curve in post-deposition annealing process

2.2.4 RF magnetron sputtering

In this study, Deposition of the gate electrode is conducted by Radio Frequency (RF) magnetron sputtering. The illustration figure of RF magnetron sputtering is shown in Fig 2.2.3. A high electron field is applied between substrate and target. A magnet is set under the target. Ar gas flow into the chamber in the process and ionized by high electric field. Ar atoms then hit the target and the target atoms are emitted by the impact. Ejected target

atom then fly through the vacuum chamber and deposit on the substrate. In this experiment process, the pressure in reaction chamber is controlled to 1 Pa. The flow rate of Ar is set to 0.7 sccm. The RF power is set to 200 W.

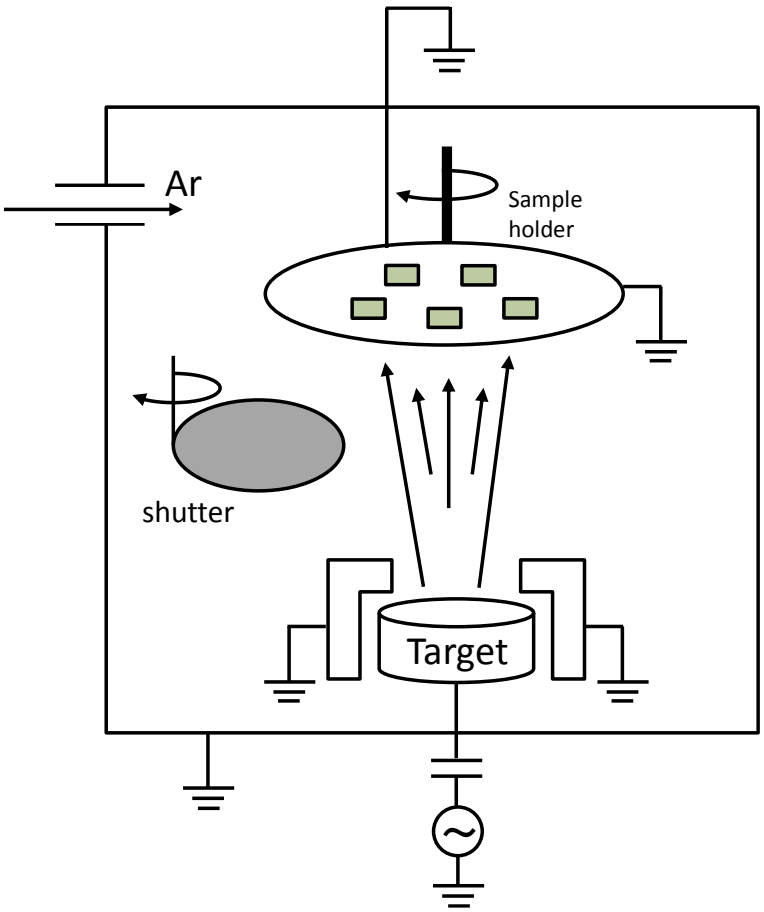


Fig 2.2.3 Schematic illustration of RF magnetron sputtering

2.2.5 Atomic layer deposition

ALD is a key process for deposition of SiO_2 gate dielectrics in this study. ALD is a thin film deposition method in which a film is grown on a substrate by exposing its surface to alternate gaseous species, which are typically referred to as precursors. Compared with chemical vapor deposition, the precursors are never present in the reactor at the same time, but they are inserted as a series of sequential pulses. In each of these pulses, the

precursor molecules react with the surface in a self-limiting way, so that the reaction terminates once all the reactive sites on the surface are consumed. Consequently, the maximum amount of material deposited on the surface after a single exposure to all of the precursors (a so-called ALD cycle) is determined by the nature of the precursor-surface interaction.[2-1].

Figure 2.2.5 illustrated the basic cycling process for deposition of ALD-SiO_2, In process (1), the precursor of TDMAS (Tris-dimethylamino-silane) is added to the reaction chamber containing the material surface to be coated by ALD. After precursor has adsorbed on the surface, any excess is removed from the reaction chamber. Oxidant O_2 plasma (red) is added (process 3) and reacts with the precursor to create another layer on the surface. After reaction of oxidant with precursor finished excess O_2 is then cleared from the reaction chamber by Ar purge again and this process is repeated until the desired thickness is achieved and the resulting product can be formed as shown in process 4.

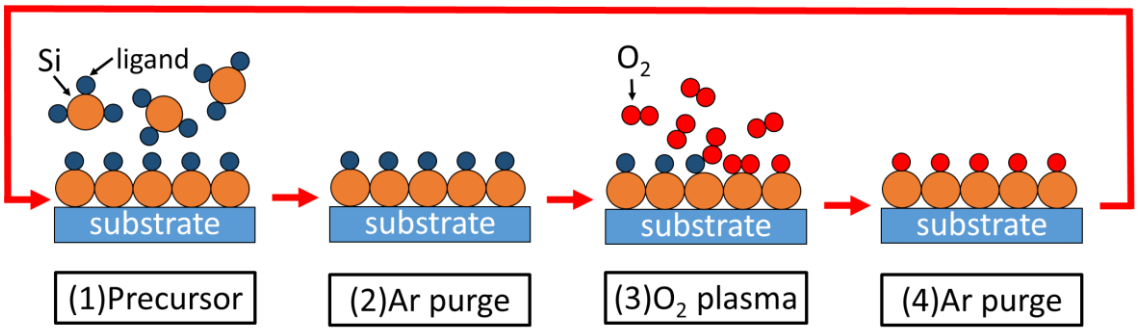


Fig 2.2.5 Schematic illustration of atomic layer deposition process

2.3 Characterization method

2.3.1 Attenuated Total Reflection Fourier transform infrared spectrometer

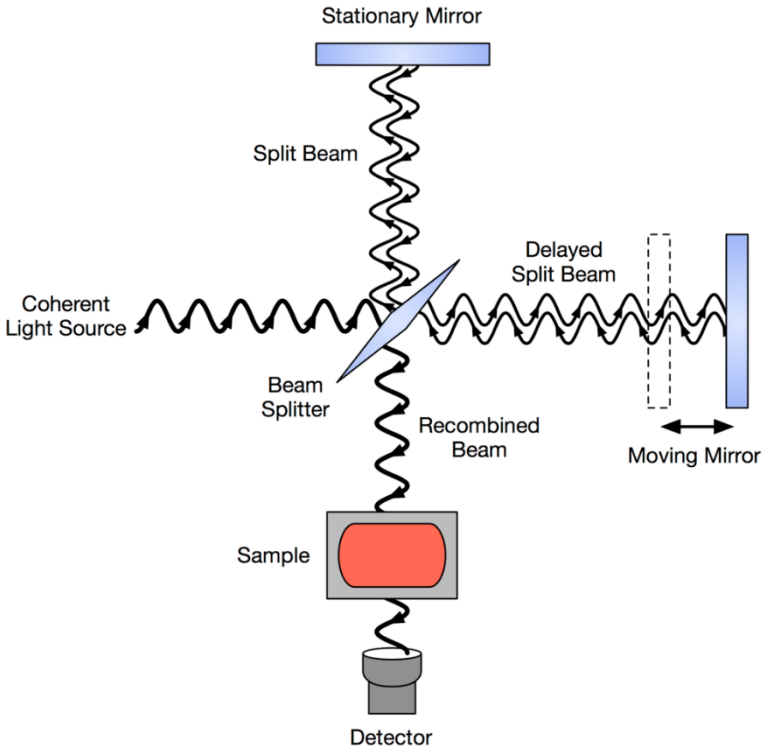


Fig 2.3.1 Schematic diagram of Michelson interferometer [2-2]

Fourier transform infrared spectroscopy (FTIR) is a vibrational spectroscopy measurement method used to obtain an infrared spectrum of absorption, emission, photoconductivity or Raman scattering of a solid, liquid or gas. Basically, Fourier transforms infrared spectroscopy is the general for infrared spectroscopy using two interference light. The Schematic diagram of Michelson interferometer, which is used to generate interference light for FTIR analysis, are shown in Fig 2.3.1 [2-2]. One beam splitter is set in the middle, a stationary mirror and a moving mirror are set at two places. An infrared light source is generated from a coherent light source when the infrared light reaches the beam splitter. Ideally, 50% of the light is refracted towards the fixed mirror and left 50% light is transmitted to the moving mirror. Light is then reflected from the

two mirror back to beam splitter. As a result, encountered two light beams interfered and pass into the sample compartment. There, the light is focused on the sample. On leaving the sample compartment the light is refocused on to the detector. By moving the right-side mirror, the optical path difference of two separated beam changes and different interference light can be generated. By calculating the received intensity of infrared light through Fourier transform, the absorption infrared spectrum can finally gain.

IR spectroscopy is useful for identification, structure determination of the compounds by identifying the various vibrational modes of a molecule. When the frequency of the infrared radiation matches the transition energy of the bond or group that vibrates. The radiation will be absorbed and the bond or group will be excited to a high energy level. For absorption of electromagnetic radiation, molecules with a dipolar moment allow infrared photons to interact with the molecule causing excitation to higher vibrational states. The homo-polar diatomic molecules do not have a dipolar moment since the electronic fields of its atoms are equal. Also, monatomic molecules are not able to interact with IR radiation because they consist only of single atom. For same dipole molecules, different vibration mode such us symmetrical stretching, antisymmetrical stretching, twisting mode response to radiation frequency, which can be observed on the FTIR spectrum.

In this study, attenuated total reflection FTIR (ATR-FTIR) is used for identification of the bond structure of gate dielectric on SiC substrate. ATR-FTIR enables samples to be examined directly in the solid or liquid state without other sample preparation [2-3]. Fig 2.3.2 shows the schematic illustration of reflection in ATR-FTIR measurement. The measuring face of the sample was fit-closely to a Ge prism by a mechanical holder. During measurement, infrared radiation enters the Ge-prism and occurs total reflection at

sample/prism interface, because the incident angle θ is larger than the critical angle. Infrared absorption happens at the reflection interface by the vibration of molecular at the substrate surface. In Fig.2.12, D_p is the depth from the interface and given by

$$D_p = \frac{\lambda}{2\pi n_1 \sqrt{\sin^2\theta - (\frac{n_2}{n_1})^2}} \quad (2.1)$$

where λ is wave number, θ is the incident angle, n_1 is Ge prism reflective index, n_2 is sample reflective index. ($n_1 > n_2$ where n_1 and n_2 are higher and lower refractive index [2-4]. The whole measurement is conducted in N_2 ambient to eliminate the disturbance of IR absorption from CO_2.

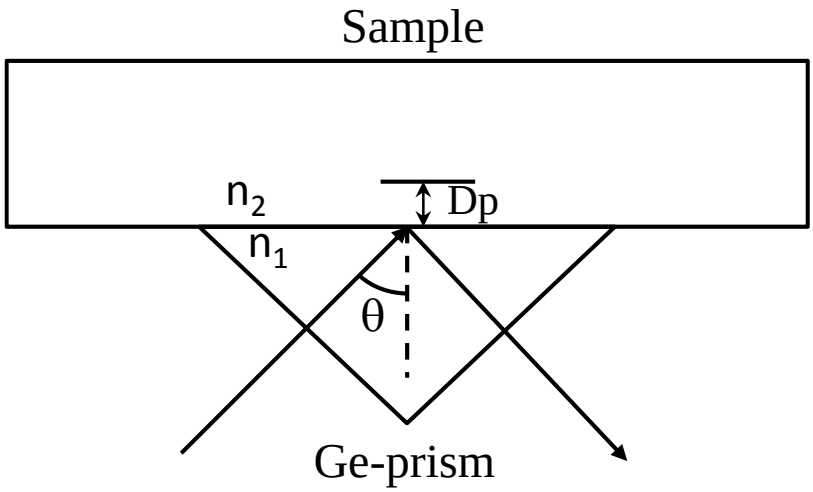


Fig 2.3.2 Schematic illustration of reflection in ATR-FTIR measurement

2.3.2 Transmission electron microscopy

Transmission electron microscopy (TEM) is a method to obtain high-resolution image by transmitting electron beam through the ultra-thin specimen. TEM is competent for ultra-high resolution imaging, owing to the small de Broglie wavelength of electrons. It is capable for analysis small specimen such us atomic arrangement and virus

configuration of nanometer scale. TEMs find application in cancer research, virology, materials science as well as pollution, nanotechnology, and semiconductor research.

Fig 2.3.3 shows the schematic illustration of TEM. On the top side is a filament that used as electron emission source, which may be a tungsten filament or a lanthanum hexaboride (LaB_6) source. Contrast with tungsten filament, the LaB_6 source can generate an electron beam with small energy dispersion. The extraction of the electron beam is by the use of Wehnelt cylinder. The extracted electrons are then accelerated by high electron field (typically 100~300 kV), and emitted into the vacuum. The electron beam is then focused and manipulated by condenser lens, which allows the formation of the electron beam to desired size and location for later interaction with the sample. The lens used in TEM are magnetic field based that manipulate electron beam by adjusting the magnetic flow. The lens consists a series of coils that deflect the direction of electron beam. The convergence of electron beam is enabled by modifying the amount of current to change the magnetic flow in the coil. After transmitted through the sample, the image is magnified and focused by objective lens and imaging lens, and finally project onto o an imaging device, such as a fluorescent screen.

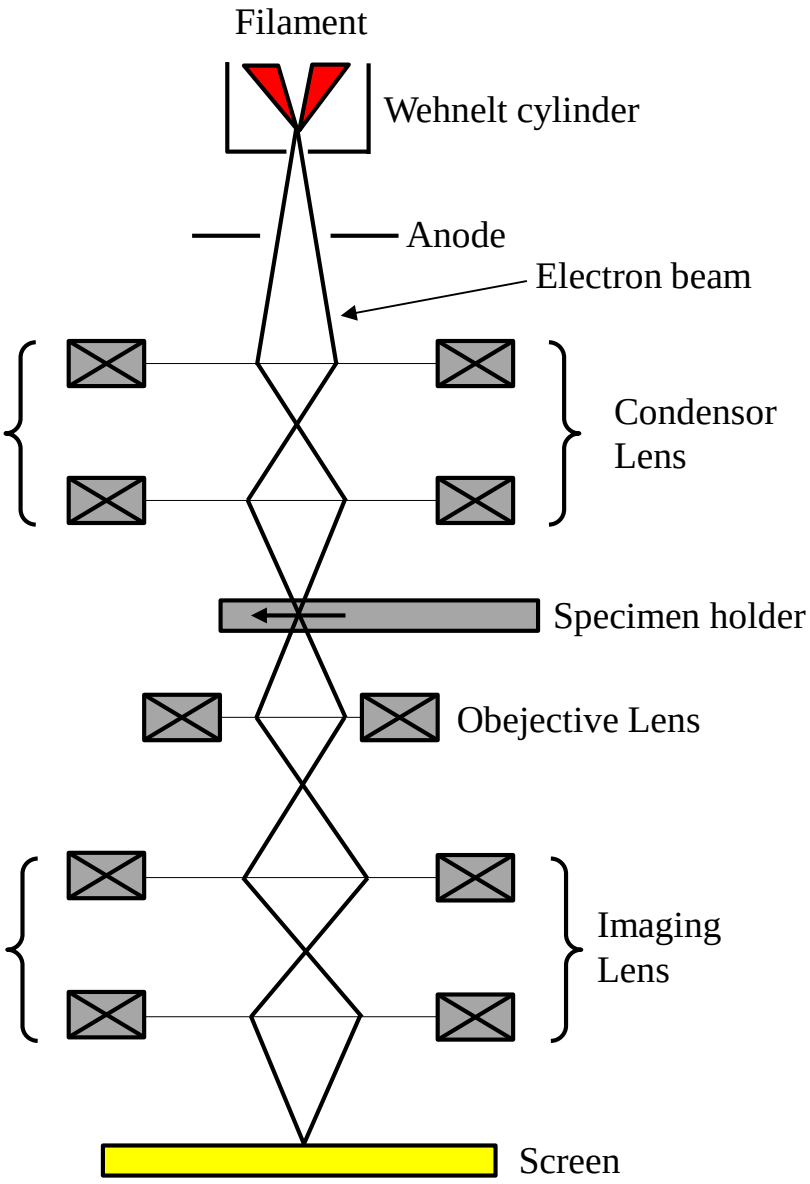


Fig 2.3.3 Schematic illustration of TEM device structure

2.3.3 Electron Energy Loss Spectroscopy

Electron Energy Loss Spectroscopy (EELS) by a method to analyze the composition and chemical bonding states by analyzing of the spectroscopy of inelastically scattered electron generated by the interaction of incident electron beam with sample material. With the corporation of scanning transmission electron microscope (STEM), detection of the

ultra-micro area with high spatial resolution can be possible.

Figure 2.3.4 shows the illustration of the structure of EELS analysis. The electron which loses energy by inelastic scattering in the sample is split by the spectrometer, and the energy strength spectra of an electron with energy loss can be detected. With the investigation of the energy loss peak where an inner-shell electron is excited to the conduction band, the element composition and chemical state of the sample can be analyzed.

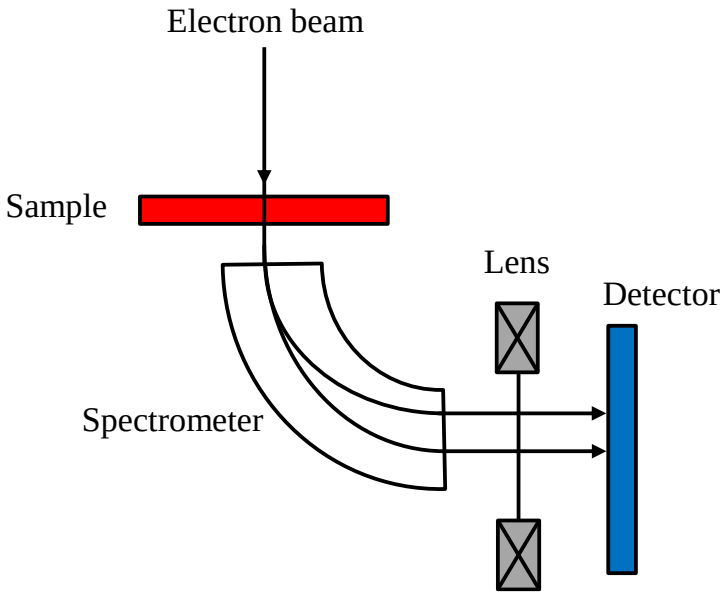


Fig 2.3.4 Schematic illustration of EELS device structure

2.3.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a useful tool for analysis of surface element composition for semiconductor devices. It's a surface-sensitive quantitative spectroscopic technique that that element composition at the parts per thousand range, empirical formula, chemical state and electronic state of the elements that exist within the material can be detected.

Fig 2.3.5 shows the schematic illustration of XPS measurement. A focused x-ray beam has been radiated on the sample surface. The inner electrons or valence electrons in atoms interacted with x-ray and being stimulated, escape from the sample surface. The escaped electron was collected by electron energy analyzer to analysis the kinetic energy of the electron escaped. The signal then is collected by electron detector to get the XPS spectra of the sample surface.

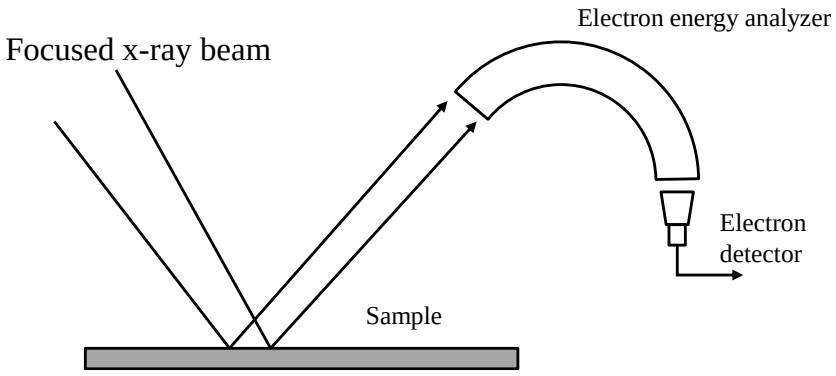


Fig 2.3.5 Schematic illustration of XPS measurement

For a certain XPS measurement, the particular x-ray beam is used so that the energy is known. And because the emitted electrons' kinetic energies can be measured, the electron binding energy of each of the emitted electrons can be determined by using an equation that is based on the work of Ernest Rutherford (1914):

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \qquad (2.4)$$

Where $E_{binding}$ is the binding energy (BE) of the electron, E_{photon} is the energy of the X-ray photons being used, E_{kinetic} is the kinetic energy of the electron as measured by the instrument and ϕ is the work function dependent on both the spectrometer and the material.

XPS depth profiling can be done by using bombination of ion beam etching or chemical etching to expose the deep layer in the sample. By continuous measurement, the

composition as weel as the distribution in-depth orientation can be obtained through etching.

2.3.5 X-ray Reflectivity analysis

X-ray Reflectivity (XRR) is a method that can analyse the thin film properties of materials on semiconductor [2-5]. Fig 2.3.6 shows the schematic illustration of XRR analysis. By incident x-ray into thin film with a small angle, the reflected x-ray by film surface and film/substrate interface and other interface interfered with each other. By gradually changing the incident angle, a profile of reflectance can be obtained. The thickness of the thin film can be known from the cycle length of reflectance profile, which is vibrated in the cycle by the interference of reflection x-ray from the film and film/substrate surface. Also, the roughness information can be obtained from the x-ray attenuation fraction and the density information can be obtained from the critical angle of the film and width of the vibration period.

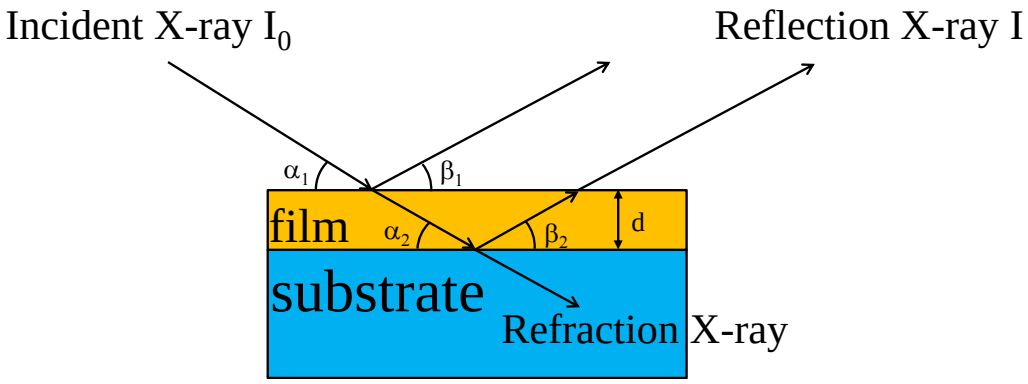


Fig 2.3.6 Schematic illustration of XRR analysis

2.3.6 Secondary ion mass spectrometry

Secondary ion mass spectrometry (SIMS) is a method can quantitatively measuring the element composition with the depth profile of the sample. The schematic illustration is shown in figure 2.3.7. Firstly a beam of ion (primary ion) with an acceleration energy of 100eV~20kV will be sputtering on the surface of the sample, then, some neutral particle, secondary ion, and electron can be ejected from the substrate surface. Secondary ion will then collected by the spectrometer and split into different mass/charge ratios. After that, the spectra will be analyzed by the detector to determine the elemental, isotopic, or molecular composition of the sample surface.

In this study, SIMS has been used to determine the C and O composition in SiC MOS structure. To obtain the depth profile of the element in metal or dielectric layers. Sample surface was continually eroded by the incident electron beam. And by plot, the intensity of a given mass signal as a function of time, the variation of its abundance/concentration with depth below the surface can be reflected.

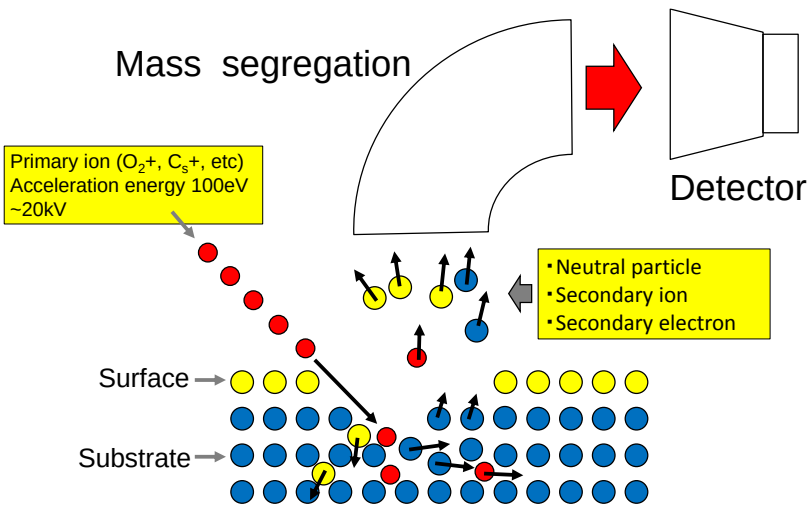


Fig 2.3.7 Schematic illustration of SIMS measurement

2.3.7 Capacitance-Voltage characteristic measurement

Capacitance-Voltage (*C-V*) characteristic measurements were performed with various frequencies (10 kHz ~ 1 MHz) by precision LCR (E4980A, Agilent). The measurement of capacitance is conducted with automatic balance bridge method. The schematic illustration of the circuit is shown in fig 2.3.8. The circuit consists of voltage measurement block and current measurement block. A sine-wave oscillator and two voltmeters and a current-voltage converter have been used. The current measurement block consists of a current-voltage converter and a voltmeter, with the feedback signal of the high gain amplifier, the input terminal (Low) can keep zero potential, which achieved zero impedance in the current measurement block. The current flow through the sample (with the impedance of Z_x) is defined as I_s, should be equal to the feedback current (I_r) flow through the resist R_r. To define the Voltage of V_1 to be v_s, the voltage of V_2 to be v_r, and the impedance of sample is Z_x, the current I_s can be:

$$I_s = I_r = \frac{v_s}{Z_x} = \frac{v_r}{R_r} \tag{2.5}$$

Hence, the impedance of sample can be expressed as:

$$Z_x = R_r \frac{v_s}{v_r} \tag{2.6}$$

And capacitance of the sample C_x can be given by:

$$C_x = \frac{j}{\omega Z_x} = \frac{jv_r}{\omega R_r v_s} \tag{2.6}$$

Since all the parameter is known factor, the measurement of the capacitance of the sample can be achieved.

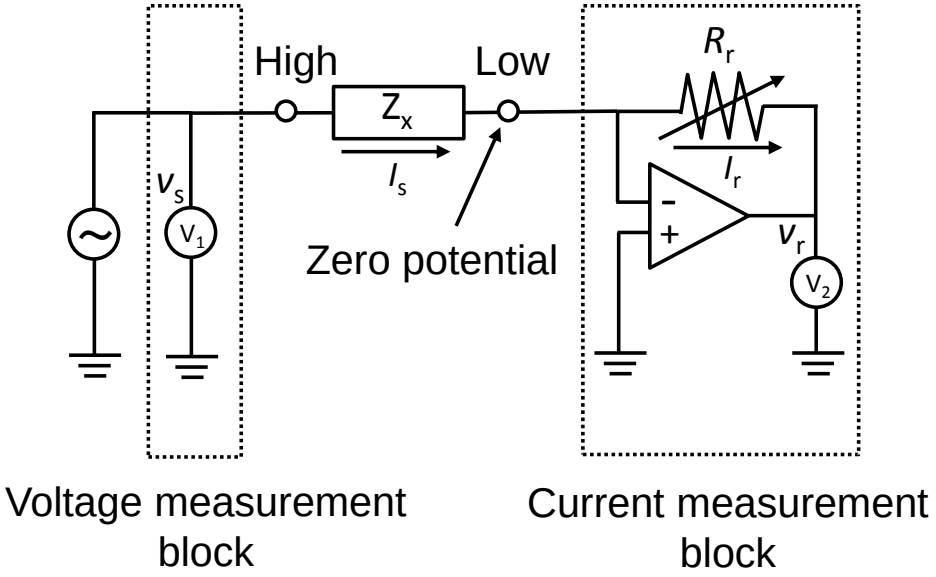


Fig 2.3.8 Schematic illustration of automatic balance bridge circuit

2.3.8 Extraction of interface state density by conductance method

The conductance method, which was proposed by Nicollian and Goetzberger in 1967 [2-6], is one of the most sensitive methods to determine interface state density (D_{it}). Conductance method is based on measuring the equivalent parallel conductance G_p of an MOS-Capacitor as a function of bias voltage and frequency. The conductance represents the loss mechanism due to interface trap capture and emission of carriers, which is a measure of the interface trap density.

The simplified equivalent circuit of an MOS-capacitor applied with the conductance method is shown in fig. 2.3.7 (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_S, and the interface trap capacitance C_{it}. The resistance R_{it} represent the capture-emission of carriers by D_{it} is a lossy process. The circuit can be simplified to the circuit in fig. 2.3.7 (b), where C_P and G_P are given by [2-7]:

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.9}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.10}$$

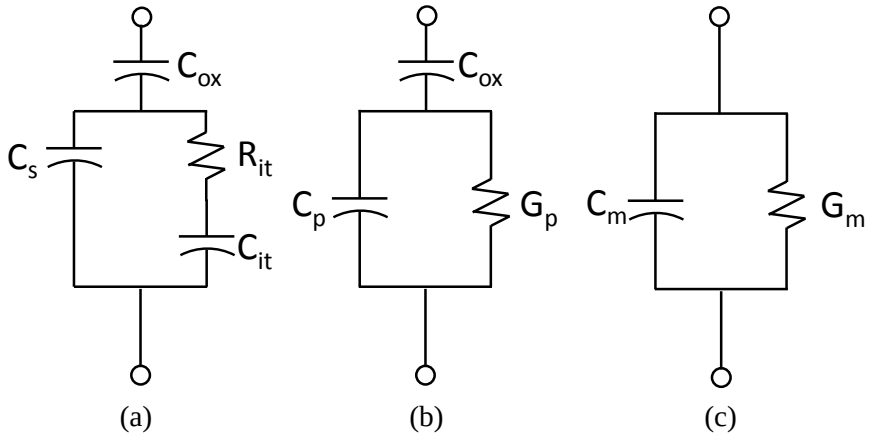


Fig. 2.3.7 Equivalent circuits for conductance measurements; (a) MOS-Capacitor with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit,[2-7].

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, which is given by $\tau_{it} = [\upsilon_{th}\sigma_p N_A \exp(-q\phi_s/kT)\,]^{-1}$ [2-7]. Dividing G_P by ω makes Eq. (2.10) symmetrical in $\omega\tau_{it}$. Equations (2.9) and (2.10) are for interface traps with a single energy level in the band gap. However, in the real situation, interface traps at the SiO_2-Si interface are continuously distributed in energy within the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as [2-7]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln[1+(\omega\tau_{it})^2] \tag{2.11}$$

The conductance is measured as a function of frequency and plotted as G_P/ω versus ω. G_P/ω has a maximum at $\omega = 1/\tau it$ and at that maximum $D_{it} = 2G_P/q\omega$. For Eq. (2.11) we find $\omega \approx 2/\tau_{it}$ and $D_{it} = 2.5G_P/q\omega$ at the maximum. Hence we determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. An approximate expression giving the interface trap density in terms of the measured maximum conductance is [2-7]:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{\max} \tag{2.12}$$

Capacitance meters generally assume the device to consist of the parallel $C_m - G_m$ combination in fig. 2.3.7 (c). A circuit comparison of fig. 2.3.7 (b) to 2.3.7 (c) gives G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as [2-7]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.13}$$

assuming negligible series resistance. The conductance measurement must be carried out over a wide frequency range. The portion of the band gap probed by conductance measurements is typically from flat-band to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50 mV or less to prevent harmonics of the signal frequency giving rise to spurious conductance.

2.3.9 Field Effect Mobility of MOSFET

When the transistor is operated in the linear region (or "ohmic mode"), where V_{DS} is small and I_D increase proportional with V_{DS}. The field-effect mobility is determined from the transconductance, defined by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (I_{DS}\text{=constant}) \tag{2.14}$$

Where I_D is the drain voltage, V_{GS} is the bias voltage between gate and source of MOSFET, and V_{ds} is the bias voltage between drain and source. The drift component of the drain current with $Q_n = C_{ox}(V_{GS} - V_T)$ is:

$$I_D = \frac{W}{L}\mu_{FE}C_{ox}(V_{gs} - V_T)V_{DS} \tag{2.15}$$

When the field-effect mobility is determined, the transconductance is can be given as:

$$g_m = \frac{W}{L}\mu_{FE}C_{ox}V_{DS} \tag{2.16}$$

Where W and L are the width and length of the channel, C_{ox} is the capacitance of gate insulator. When this equation is solved for the mobility, it is known as the field-effect mobility:

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{2.17}$$

In this study, the V_{DS} is controlled to be 50 mV when measuring the *field-effect mobility*.

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Chapter 3. Film properties of ALD-SiO_2

3.1 Introduction

With low on-resistance advantage, trench type MOSFET is becoming the mainstream of SiC MOS-structure. However, a strong crystallographic orientation dependent oxidation on the 3D-gate structure may result in the formation of an uneven SiO_2 layer, which may pose reliability issues [3-1]. On this point, gate dielectrics formed by conformal deposition processes seem to be prominent ways for replacing the thermally grown SiO_2 ones. ALD has been indicated to be a feasible method to form a conformal SiO_2 layer on semiconductor surfaces [3-2]. Also, as the ALD process can be performed at low process temperature, the risk of forming carbon deficiency in the sub-surface SiC channel can be reduced [3-3].

In this chapter, ALD deposition has been conducted with tris-dimethylamino-silane (TDMAS) precursor, due to its high vapor pressure and high thermostability at room temperature. The deposition properties including deposition rate and density will be introduced. Finally, the electrical characteristics of ALD-SiO_2 on Si wafer have also been discussed.

3.2 Selection of precursor for ALD-SiO_2

For ALD process, selection of precursor is very important and can significantly influence the deposition process and film properties. A variety of precursor has been reported using for ALD process including chlorosilanes, alkoxysilanes, alkoxysilanes, alkylaminosilanes, and aminosilanes [3-4,3-5,3-6,3-7,3-8,3-9]. Among those types of the precursor, aminosilanes is a prospective material for ALD process in safety and operability perspectives aspect. Here, we present three kinds of aminosilanes structure, including

bis(tertiarybutylamino)silane (BTBAS), bis(diethylamino)silane (BDEAS), and TDMAS. The molecule structure of the three kind of precursor is as follow:

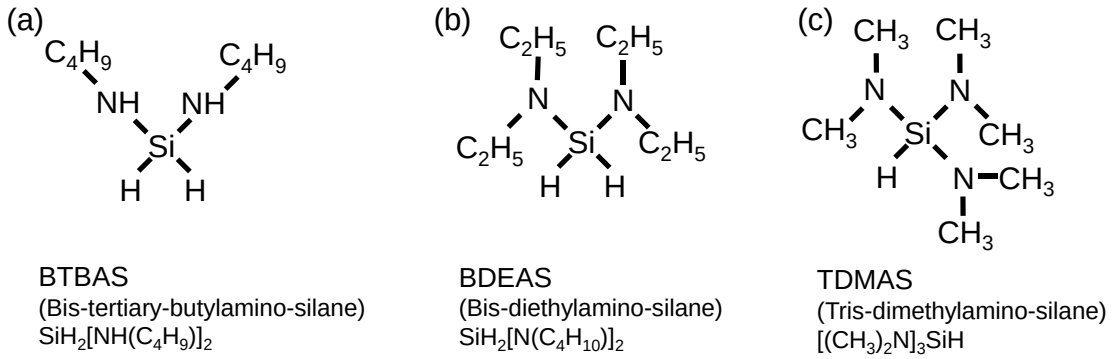

Fig 3.2.1 Molecule structure of (a) BTBAS (bis(tertiarybutylamino)silane) (b) BDEAS (bis(diethylamino)silane) (c) TDMAS (tris(dimethylamino)silane)

Contrast to TDMAS, BTBAS and BDEAS have more hydrogen directly bonded to silicon, which makes them more reactive and can achieve high deposition rate in ALD process. However this kind of high activity also attributed to low thermostability, BTBAS and BDEAS can easily decompose at room temperature rapidly with respect to TDMAS. On the other side, although the deposition rate of TDMAS is lower than BTBAS and BDMAS. The deposition rate of 0.8 nm/cycle is achievable with deposition temperature ranging from 250 ^oC to 600 ^oC, which is acceptable for ALD-SiO_2 deposition.

The carbon concentration in deposited SiO_2 also showed the difference between each precursor [3-10]. Table 3.2.1 shows the carbon concentration in ALD-SiO_2 after deposition using different precursor. Compared with BTBAS and BDEAS, the carbon residue concentration in deposited SiO_2 is about one order higher, which may increase the trap density in bulk of ALD-SiO_2 by carbon-related defects. Annealing in oxygen ambient

after ALD process may be a feasible method for carbon residue reduction, by reaction of an Oxygen molecule with carbon to generate CO gas diffuses out of the SiO_2 layer.

precursor	Residual carbon concentration
BTBAS	$5x10^{19}$ /cm^3
BDEAS	$5x10^{19}$ /cm^3
TDMAS	$4x10^{20}$ /cm^3

Table 3.2.1 Carbon concentration in deposited ALD-SiO_2 by different precursor [3-12]

Besides of carbon concertation in the deposited SiO_2 layer, the vapor pressure of precursor is also important for the operability of ALD process. Figure 3.2.2 shows the relationship of vapor pressure with temperature for each precursor. Compared with BTMAS and BDEAS, higher vapor pressure can be obtained with TDMAS. The vapor pressure of TDMAS can be about 1×10^3Pa high at room temperature, which is a unique advantage of TDMAS over BTMAS and BDEAS.

Finally, considering these factors comprehensively, we chose TDMAS as the precursor for ALD-SiO_2 deposition. O_2 remote-plasma has been used as an oxidant for ALD process. The deposition rate and other properties of ALD-SiO_2 will be discussed in the next two chapters.

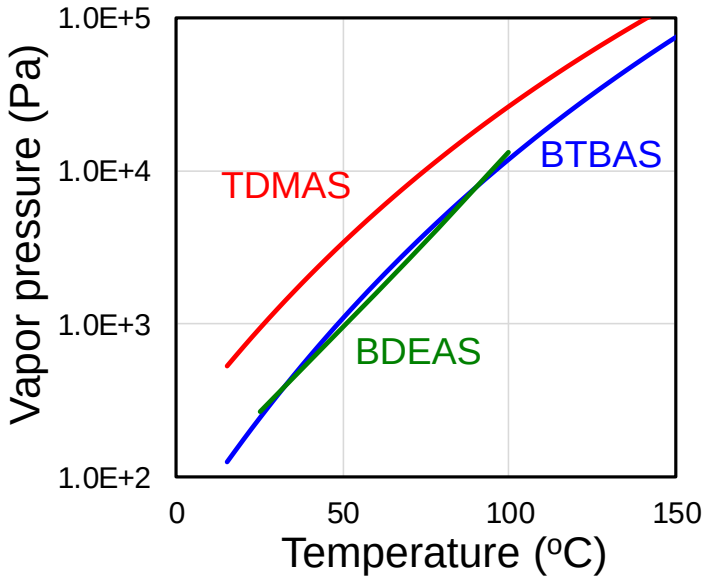

Fig 3.2.2 Vapor pressure of BTBAS, BDEAS, and TDMAS

3.3 Deposition rate and density of ALD-SiO_2

Deposition of ALD-SiO_2 with a precursor of TDMAS and oxidant of O_2 plasma has been conducted. The substrate temperature during deposition was set at 300 °C and the injection time of TDMAS was 0.4 second per cycle. After injection of TDMAS, O_2 plasma exposure is conducted for 20 sec to ensure sufficient reaction of TDMAS. Then, redundant gas and reactant will be evacuated and reaction chamber will be prepared for a new cycle of deposition.

Fig 3.3.1 shows the deposition rate of ALD-SiO_2 with TDMAS and O_2 plasma. The thickness of SiO_2 after deposition of 100, 150, 200 cycles was measured by an ellipsometer, respectively. A linear relationship has been found for the deposition thickness with a number of deposition cycles. And deposition rate of 0.04 nm/cycle has been achieved of ALD-SiO_2 deposition on SiC substrate. An initial thickness of 1.8 nm

can be observed on the figure when deposition cycle is zero, which should be the surface reaction of SiC substrate with the O_2 plasma.

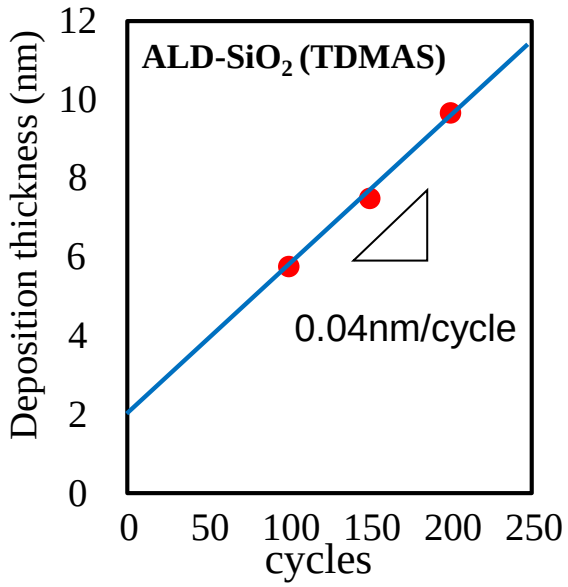

Fig 3.3.1 Deposition rate of ALD-SiO_2 with TDMAS precursor and O_2 plasma oxidant

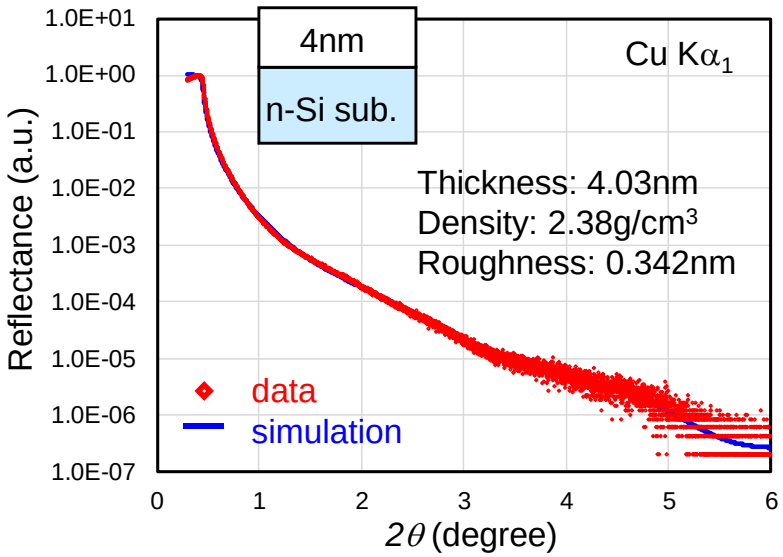

Fig 3.3.2 Density and roughness of ALD-SiO2 by XRR analysis.

To extract the density of ALD-SiO_2, a silicon wafer with 4-nm-ALD-SiO_2 has been prepared and analyzed by XRR, as shown in fig. 3.3.2. The density of SiO_2 is 2.38g/cm^3 with an interface roughness of deposited SiO_2 is 0.342 nm on average, based on the fitting of XRR data. The density of deposited SiO_2 is a little higher than that of thermal grown SiO_2 (2.27 g/cm^3), which is considered to be attributed to the Si-rich deposition during ALD process. The roughness of ALD-SiO_2 is less than thermal grown SiO_2, which is a unique the advantage for ALD process formed SiO_2.

3.4 Breakdown properties of ALD-SiO_2

To examine the electrical properties of ALD-SiO_2, MOS capacitors have been fabricated on Si substrate. SiO_2 film was then deposited on Si substrates by ALD with a thickness of 8.67nm. Tungsten electrode was deposited on top of the SiO_2 layer for 50nm and followed with annealing in FG gas ambient at 420 ^oC for 30min. Fig 3.4.1 shows C-V characteristics of Si capacitor with ALD-SiO_2 gate dielectric. C-V characteristics were measured with different frequency ranging from 10 kHz to 1 MHz. Although a frequency dispersion has been observed in C-V characteristics, which can be related to the existence of near-interface-trap, the MOS-capacitor operated normally. Using the maximium capacitance of the Si capacitor as oxide capacitance and the permittivity of SiO_2 of 3.45×10^{-13} Fcm^{-1}, the equivalent oxide thickness (EOT) can be derived to be 8.64 nm, which coincides with the value of the physical thickness of deposited ALD-SiO_2.

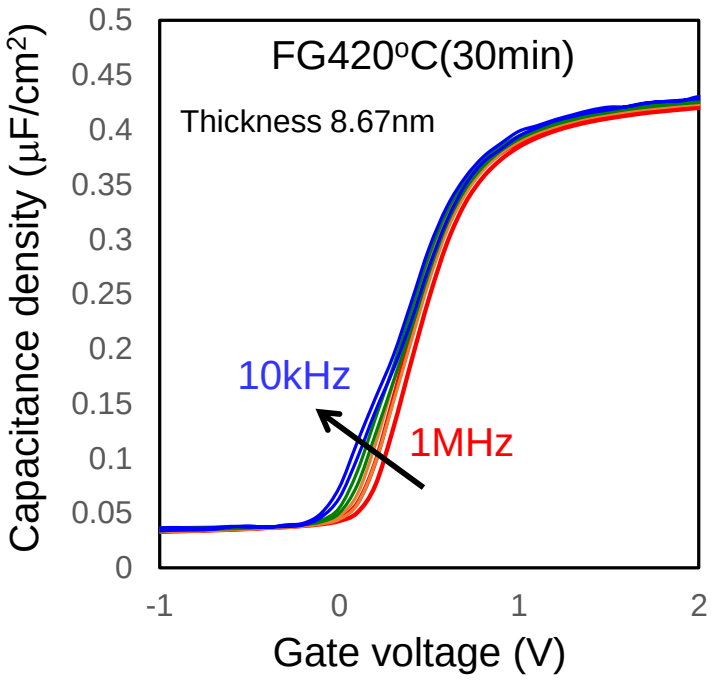

Fig 3.4.1 Capacitance-voltage characteristics of Si capacitor with ALD-SiO_2 gate dielectric

The reliability of ALD-SiO_2 is also the main concern of deposition gate dielectric on SiC. Breakdown electrical field (E_{BD}) is one of the main parameter for reliability characteristics of the gate dielectrics. The breakdown filed of ALD-SiO_2 was measured with Si capacitor with 8.67 nm ALD-SiO_2. The distribution properties of breakdown filed were shown in Fig 3.4.2. Based on the Weibull distribution model, the breakdown field of ALD-SiO_2 can be determined to be 8 MV/cm. It is a little lower than that of thermal grown SiO_2, which can be as much as 10 MV/cm. Nevertheless for a deposition gate dielectric, the breakdown field is comparatively good.

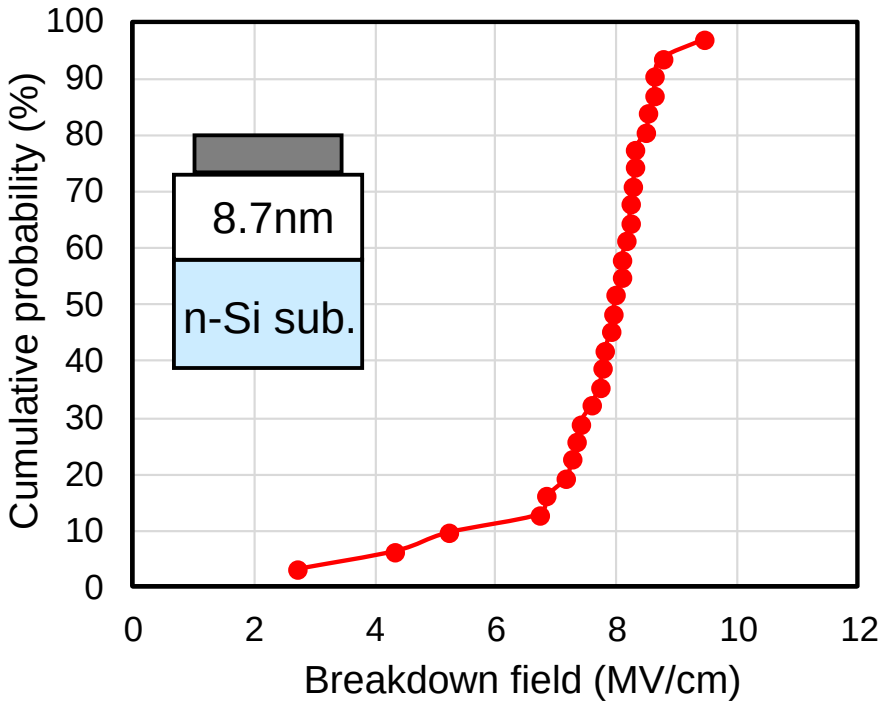

Fig 3.4.2 Breakdown field distribution of ALD-SiO_2 on Si substrates

3.5 Summary of chapter 3

Deposition of ALD-SiO_2 has been investigated in process and electrical properties aspects. The precursor of TDMAS and oxidant of O_2 remote plasma has been used in ALD process to form a SiO_2 layer. A deposition rate of 0.04 nm/cycle has been demonstrated for ALD-SiO_2 and the density of deposited SiO_2 is 2.38 g/cm^3. Interface roughness of ALD-SiO_2 is much smaller than that of thermal grown SiO_2, which is a unique advantage of SiO_2 deposited by ALD process. The breakdown field of ALD-SiO_2 is about 8 MV/cm, which is comparatively good for deposited SiO_2. The fine quality of ALD-SiO_2 makes it a potential material of gate dielectric for high-performance SiC power devices.

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Chapter 4 Electrical properties of SiC-MOS structure with ALD-SiO_2 gate dielectrics

4.1 Introduction

In this chapter, we will discuss the electrical properties of ALD-SiO_2 film on SiC substrates. As the ALD process can be performed at low process temperature, the risk of forming carbon deficiency in the sub-surface of SiC channels can be reduced [4-1]. For ALD-SiO_2, high density of bulk trap has been introduced due to the high concentration of carbon residue by precursor material during the ALD process [4-2], its reliability property, as well as the interface property for SiC gate dielectrics, are not clear. Therefore, additional treatments need to be performed to reduce the carbon impurities.

In this work, SiC MOS-capacitors were fabricated with ALD-SiO_2 using TDMAS precursor. To improve the electrical properties of the deposited ALD-SiO_2 gate dielectric. PDA has been performed after ALD process. For further properties improvement, PMA by tungsten electrode capped annealing has been introduced. The electrical properties and modification mechanism have also been investigated for SiC MOS capacitor with PDA and PMA treatment.

4.2 Effect of Post-deposition-annealing (PDA)

Figure 4.2.1 shows the *C-V* characteristics of SiC MOS capacitor with ALD-SiO_2 before any thermal treatment. A positively shifted *C-V* curve with V_{fb} of 29.0 V indicates a large density of bulk traps exist in the layer of ALD-SiO_2. Hysteresis voltage about 1.04 V suggested a large concentration of oxide traps near the SiO_2/SiC interface. Also, the initial sweep of *C-V* curve shows huge flat-band voltage change, which can be attributed to high-density electron trap in ALD-SiO_2. The properties above revealed that although *C-V*

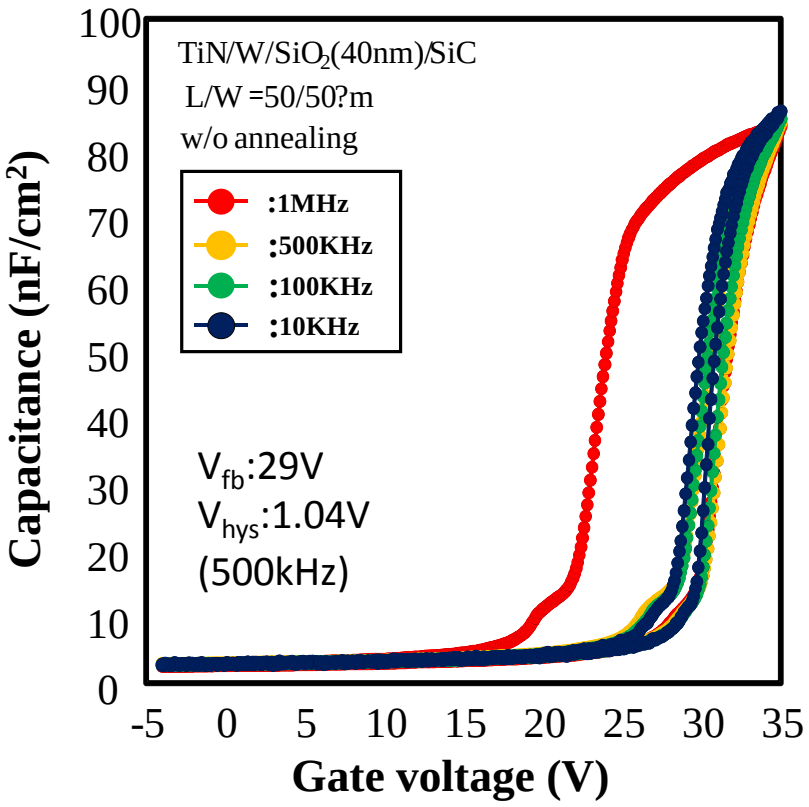

Figure 4.2.1 C-V characteristics of ALD-SiO_2/SiC sub. with and without the PDA treatments.

characteristics can be confirmed for SiC capacitor with ALD-SiO_2, additional treatment is necessary for electrical properties improvement of ALD-SiO_2.

Reduction of bulk trap density in thermal grown SiO_2 by post-oxidation annealing in O_2 ambient has been demonstrated on SiC substrate [4-3]. For ALD-SiO_2, the elimination of residual carbon in the oxide layer is a key for electrical properties improvement on SiC substrates. The same effect can be expected to be gained by PDA process in O_2 to eliminate residual carbon in ALD-SiO_2 layer. The *C-V* characteristics of the devices with PDA at 1000°C or 1100°C are shown in figure 4.2.2. The *C-V* curves of SiC capacitor with ALD-SiO_2 revealed a large shift to negative direction back toward the ideal

theoretical *C-V* curve with the PDA treatment, indicating that negatively charged defects in the SiO_2 layer were compensated by the treatment. The negative charges can be considered to be the electrons trapped at broken bonds in the SiO_2 layer during the SiO_2 deposition by plasma exposure. The trapped electrons are reported to be removed by annealing [4-4]. On the other hand, the hysteresis (V_{hyst}) in the *C-V* curves was found to be reduced to 0.18 V with the PDA at 1100°C, suggesting the reduction in the border traps near the SiO_2/SiC interface. Compared with the capacitance of SiC capacitor without any thermal treatment in fig. 4.2.1, the decrease in the accumulation capacitances indicates additional interface oxidation during the PDA treatment. Although the V_{fb} recovery and a slightly reduced D_{it} of 1.3×10^{12} cm^{-2}/eV can be obtained with the high-temperature PDA process, longer or even higher PDA temperature treatments will result in further interface

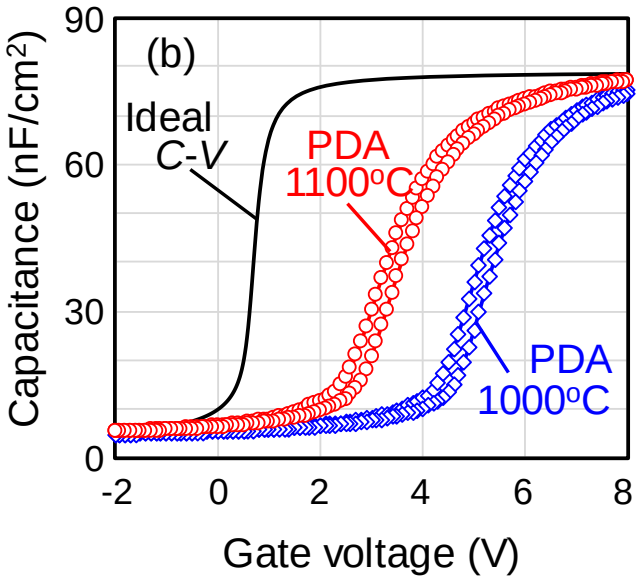

Figure 4.2.2 C-V characteristics of ALD-SiO_2/SiC sub. with and without the PDA treatments.

oxidation, which may suffer from uneven interface oxidation due to orientation dependent oxidation rate.

4.3 Electrical properties of ALD-SiO_2 with PMA treatment

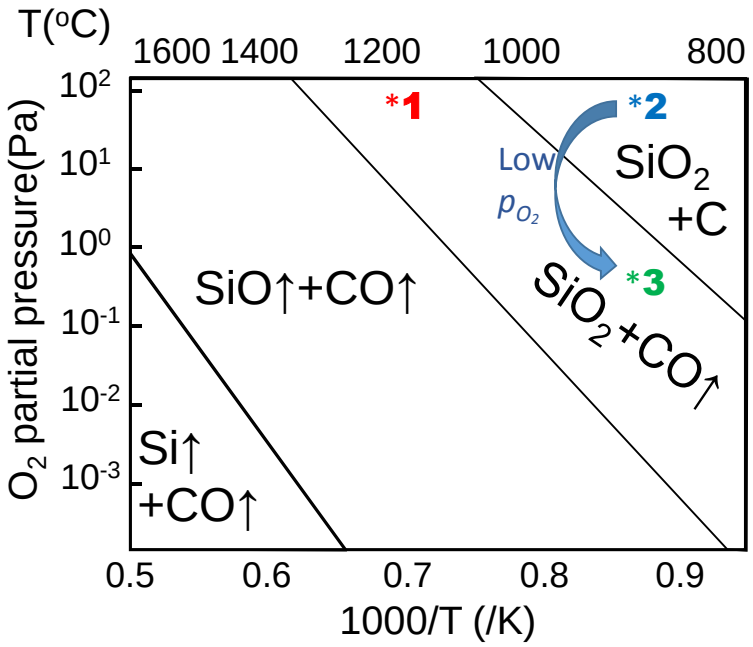

Fig 4.3.1 predicted $P(O_2)$–T phase diagram for SiC(s)+O_2(g) reaction based on the thermodynamic model [4-5]

For further electrical properties improvement for ALD-SiO_2, an additional annealing treatment is necessary for interface properties modification. Fig 4.3.1 shows the relationship of oxidation reaction on SiC substrate with oxidation temperature and oxygen partial pressure (PO_2) [4-5]. For SiC oxidation, the ideal model is to form SiO_2 with carbon transform into CO gas deviate from the substrate. However, as illustrated by the $P(O_2)$-T phase diagram, the high temperature is necessary for oxidation at atmosphere

situation. As illustrated by point 1 in the figure, a temperature of about 1200°C is necessary for thermally grown SiO_2 on SiC substrate. Low-temperature annealing, as illustrated by point 2 in the figure, will trigger the reaction to form C residue at the SiO_2/SiC interface, which may cause reliability problem issue for an SiO_2 gate dielectric. But for low-temperature annealing, a reaction that generates SiO_2 and CO can also happen at low O_2 partial pressure condition, as point 3 shown in the figure. So the control of O_2 partial pressure is a key for annealing of SiC device at low-temperature condition.

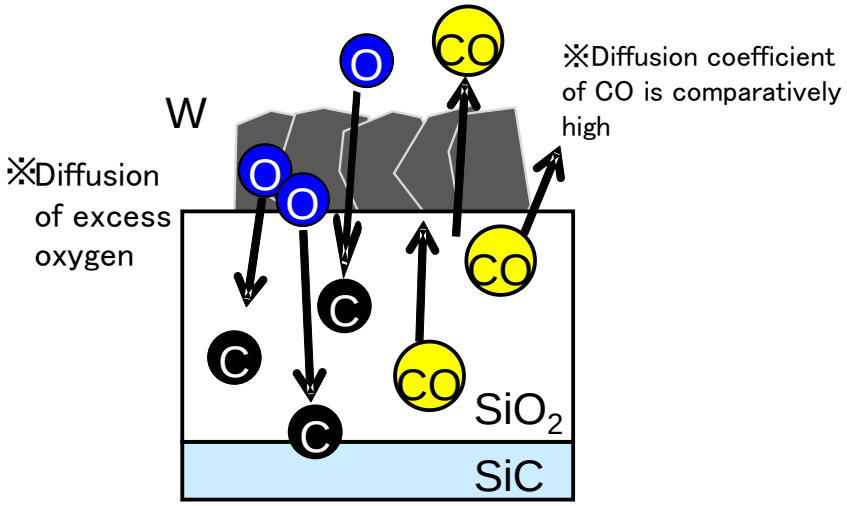

Fig 4.3.2 illustration of oxygen diffusion and reaction with Carbon residue in SiO_2 and at the SiO_2/SiC interface

To achieve thermal treatment condition with low O_2 partial pressure, tungsten capped annealing is considered to be capable to generate low concentration oxygen during the annealing by diffusion. Sputter deposited W layers are known to incorporate a high concentration of oxygen atoms [4-6], which originates from the sputter targets. As illustrated in fig 4.3.2, by diffusion of excess oxygen atom in W layer or from the ambient during the annealing, the elimination of carbon residue in SiO_2 and the SiO_2/SiC interface

can be achieved by reaction of diffused oxygen with carbon residue. Since the oxygen concentration in W is much lower than that in the atmosphere, low O_2 partial pressure condition can be realized during the annealing. By W capped annealing at low temperature, elimination of carbon residue can be expected without generation of new carbon atom at the interface, which is promising for electrical modification of SiC devices with ALD-SiO_2.

Figure 4.3.3 shows the *C-V* characteristics of the samples processed with PDA at 1100°C for 30 mins followed by PMA at 850 or 950°C for 10^3 sec. Figure 4.3.3(a) shows that once the PMA is conducted, the accumulation capacitance showed a slight reduction for both samples, indicating additional interface reaction to increase the thickness of the SiO_2 layer. The accumulation capacitance stayed constant even with longer PMA duration. With longer PMA duration, the *C-V* curves shift to the negative direction toward that of the ideal *C-V* curve, illustrated by V_{fb} reduction with longer annealing duration, in fig 4.3.4, indicates the reduction of the negatively charged fixed defects in the SiO_2 layer and/or at the SiO_2/SiC interface. In addition, as illustrated by figure 4.3.4 (b), the reduction in the V_{hyst} along with PMA duration suggests the reduction of the oxide traps near the SiO_2/SiC interface. As the slopes of the *C-V* curves become steeper, one can also expect a reduction in the D_{it} with longer PMA duration. Indeed, as illustrated in figure 4.3.5, conductance spectra of the samples at a surface potential of -0.024 eV below the Fermi level revealed a large reduction in the amplitude; a D_{it} of 3.1×10^{11} cm^{-2}/eV can be achieved when annealed for 5×10^3 sec. The calculated electron capture cross section of 5×10^{-19} cm^2 at an energy of 0.24 eV below the E_C is in good agreement with the reported value [4-7]

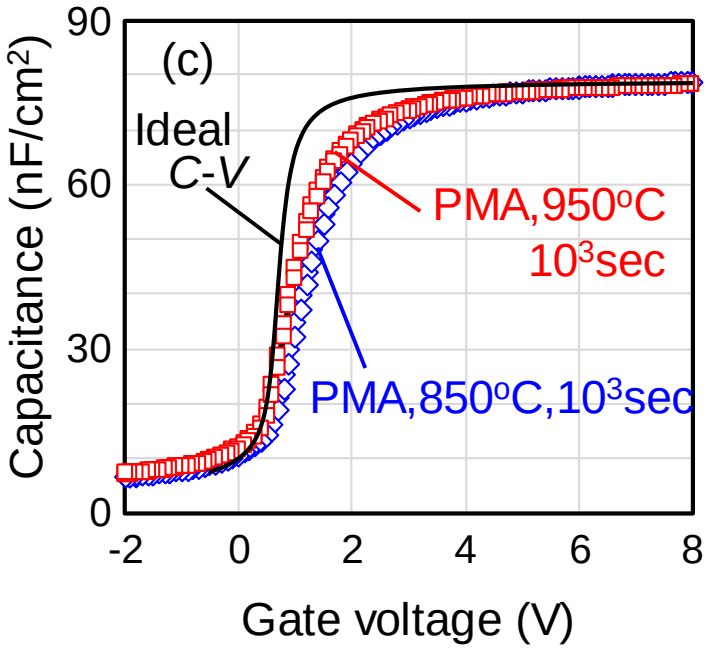

Figure 4.3.3 C-V characteristics with different PMA temperature for 10^3 sec.

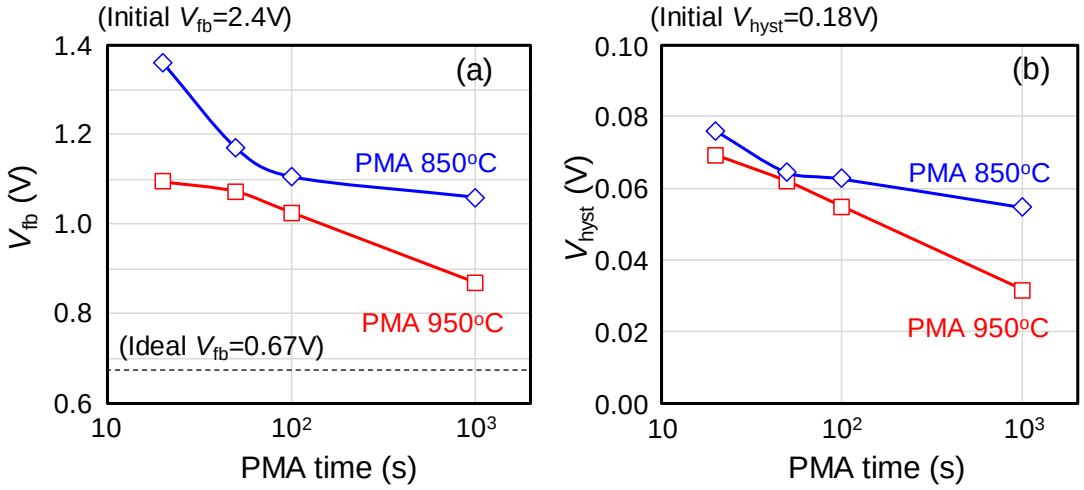

Figure 4.3.4 (a) V_{fb} and (b) V_{hyst} dependence on PMA durations at 850 and 950°C.

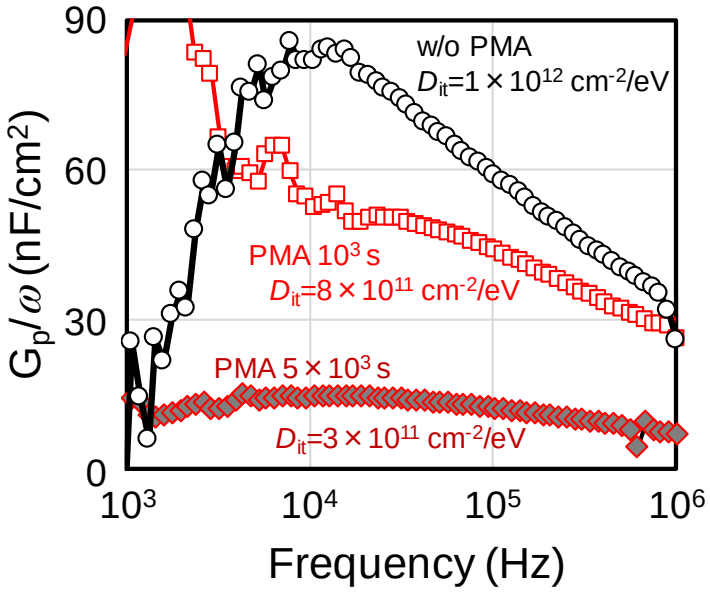

Figure 4.3.5 G_p/ω spectra at E_C-0.24 eV of MOS capacitors with PMA at 950°C.

4.4 Cross-sectional image observation and concentration analysis of O and C

Cross-sectional TEM images of the samples before and after PMA treatment are shown in figure 4.4.1 (a) and (b), respectively. One can confirm the formation of a uniform SiO_2 layer for both samples without any rough interface. The thickness of the SiO_2 layer for the sample after PMA treatment is found to be increased by 3.8 nm. Therefore, the reduction in capacitance after PMA treatment observed in the *C-V* measurements is due to the additional interface oxidation to form SiO_2. Since the annealing is performed with a metal layer and in the forming gas ambient, the source of oxygen atoms for the additional oxidation might be the ones initially stored in the W layer. Although a W target with a high purity (4N) has been used in this study, the absorption of oxygen molecules at the grain boundary in the target might be the origin. The Ellingham diagram predicts

the oxygen partial pressure of 10^{-9} Pa under thermal equilibrium at 950°C [4-8]. Thus, the oxygen atoms in the W layer should out diffuse along with the annealing time.

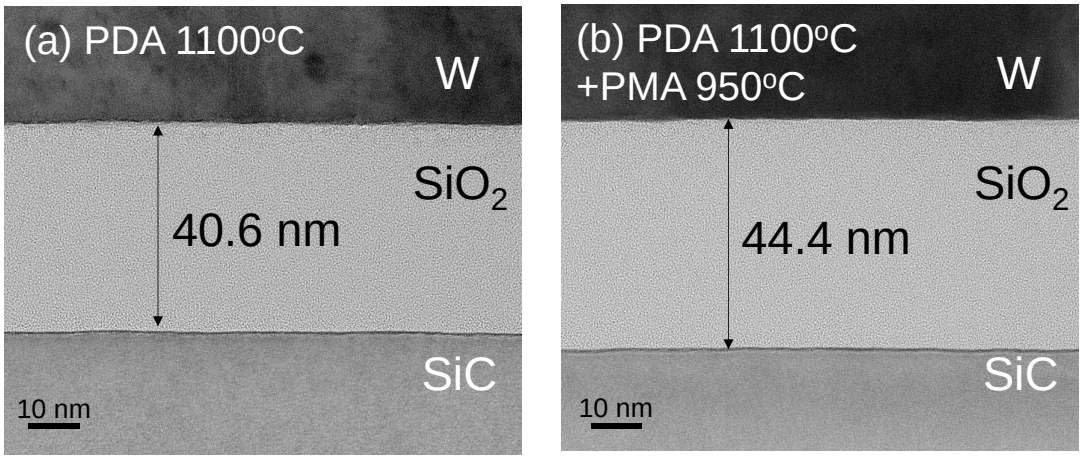

Figure 4.4.1 TEM images of ALD-SiO_2/SiC sub. after (a) PDA at 1100°C and (b) PMA at 950°C reveal the increase in the SiO_2 thickness.

Figure 4.4.2 shows the secondary ion mass spectrometry (SIMS) of blanket samples, which were processed with PDA at 1100°C for 30 min. The concentration of carbon and oxygen before and after annealing has been shown in fig 4.4.2(a) and fig 4.4.2(b), respectively. For carbon in ALD-SiO_2 layer, a high concentration of C concentration (10^{20} cm^{-3}) before the PMA has been revealed. The concentration was reduced slightly below 10^{19} cm^{-3} by the additional PMA process at 900°C for 10^3 sec, indicating that C atoms can be effectively removed by the PMA process. On the other hand, a high oxygen atom concentration of 4×10^{19} cm^{-3} in the W layer was found to be reduced by one-third with the PMA treatment, suggesting the diffusion of oxygen atoms either or both into the capping TiN layer or the SiO_2 layer. It has been reported that outward diffusion of the oxygen atoms from the W layer during PMA proceeds the interface reaction between a gate dielectric and a semiconductor [4-9]. Nevertheless, one of the origins of the

improvements in the electrical characteristics with PMA process may be the reduction in the C atoms in the SiO_2 layer.

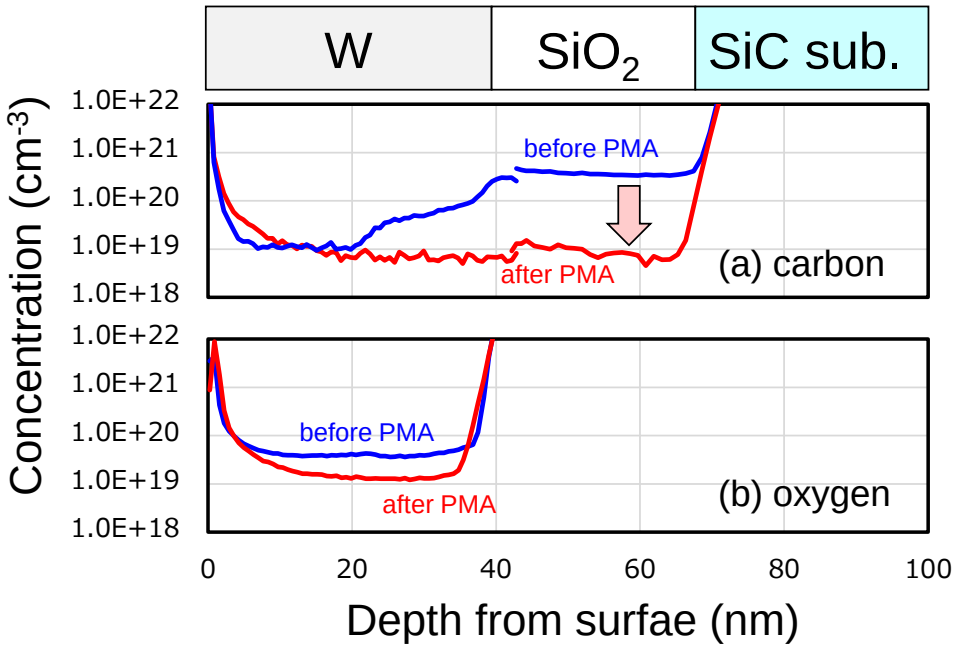

Fig 4.4.2 (a) SIMS depth profiles of carbon ions showed a large reduction in the carbon concentration in the SiO_2 layer. (b) The concentration of oxygen ions in the W layer was also reduced by the PMA treatment.

The distinctive difference between the PDA at 1100°C in an oxygen ambient and the PMA at 950°C in FG ambient is the oxygen partial pressure during the annealing. Thermodynamic calculations indicate that the PDA condition is expected to oxidize the SiC surface with carbon atoms as byproducts [4-5]. Thus one need to use high temperature, typically 1300°C, to suppress the creation of C atoms [4-10]. On the other hand, low oxygen partial pressure the PMA process is the condition to oxidize SiC the surface with CO(g) molecules as byproducts, so that the additional interface oxidation may not increase the C concentration in the SiO_2 layer. With the out-diffusion of oxygen atoms

from the W layer and also oxygen atoms from the surface during with the PMA process, the oxygen partial pressure gradually decreases to inhibit the interface oxidation. The oxygen atoms may be consumed to compensate the oxygen vacancies and remove the residual C atoms in the whole SiO_2 layer.

4.5 Electrical properties of SiC-MOSFET with ALD-SiO_2

Although the electrical properties improvement of ALD-SiO_2 gate dielectric by PMA and PDA has been demonstrated on SiC capacitor, the quality improvement effect on SiC MOSFET by thermal treatment is still unknown. In this section, we investigated the electrical properties of SiC-MOSFET using ALD-SiO_2 gate dielectrics. The field-effect mobility of SiC-MOSFET has been analyzed, and the mobility improvement by PMA treatment has been introduced.

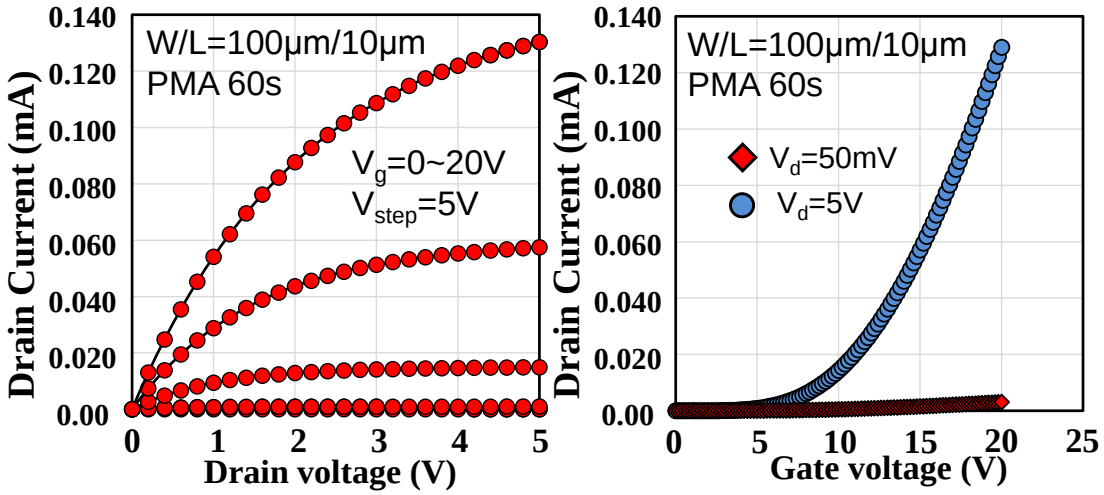

Fig 4.5.1 MOSFET characteristics of SiC-MOSFET with ALD-SiO_2 (a) I_d-V_d characteristic (b) I_d-V_g characteristic

Figure 4.5.1 shows the I_d-V_d characteristic and the I_d-V_g characteristic of SiC-MOSFET using ALD-SiO_2 gate dielectric. The oxide thickness (T_{ox}) of deposited SiO2 is measured to be 41.7 nm. To gain ohmic contact on the source and drain with Ni contacts, PMA treatment at 950 ^oC for the 60s has been applied to the fabricated sample. For I_d-V_d characteristic shown in Figure 4.5.1(a), the drain current (I_d) curve increase with the gate voltage (V_g), and shows a parabolic relationship with V_d. I_d-V_g characteristic was shown in figure 4.5.1(b) and was plotted when V_{ds} is 5 V and 50 mV, respectively. Both the I_d-V_d and I_d-V_g characteristic are showing that the MOSFET is functioning normally.

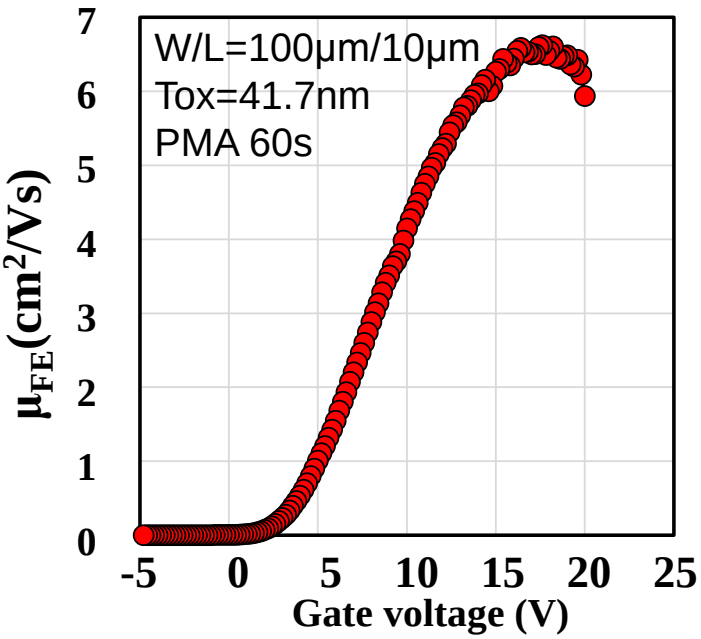

Figure 4.5.2 field effect mobility of SiC-MOSFET with ALD-SiO_2.

Additional PMA treatment has been conducted on SiC-MOSFET samples at 950^oC and with duration from 60s to 2000 s. Figure 4.5.3 illustrated that with different PMA duration, I_d continually increased with the duration of PMA treatment. I_d-V_g characteristic is

measured by a double method in this experiment which can sweep from low voltage to high voltage and return back from high voltage to low voltage. As shown in figure 4.5.3(a), with PMA duration, the hysteresis of I_d increased firstly when PMA duration increased from 60 s to 100 s. The hysteresis was then reduced significantly with PMA duration and almost no hysteresis can be found on I_d-V_g characteristic. The maximum I_d at V_g of 20 V showed an increase from 3.02μA to 6.82μA. More than one time of current magnification has been realized by PMA treatment, which could be attributed to the improvement of electron mobility of SiC MOSFET channel.

Figure 4.5.4 shows the μ_{FE} of the SiC MOSFET. As shown in the figure, μ_{FE} were largely increased with PMA duration. With PMA treatment for 2000s, μ_{FE} has been increased from 6.6 cm^2/Vs to 11.8 cm^2/Vs, about 80% mobility enhancement has been achieved with PMA process. Also, with PMA duration, the mobility start to rising up at lower gate voltage, which indicated that the V_{th} has been reduced with PMA treatment. The reduction of V_{th} can be attributed to the reduction of the bulk trap in ALD-SiO_2 gate dielectric with reduction of the residual carbon-related trap.

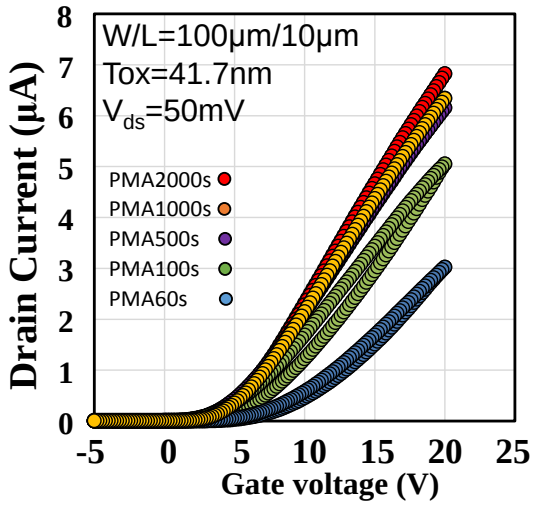

Fig 4.5.3 I_d-V_g characteristic of MOSFET with PMA for 60s to 2000s

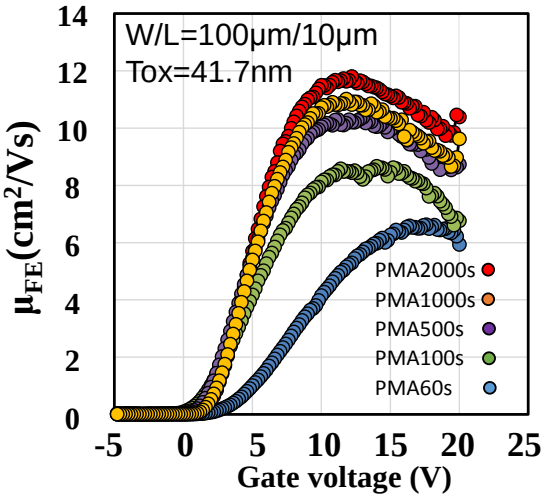

Fig 4.5.4 Field-effect mobility of MOSFET with PMA for 60s to 2000s.

4.6 Summary of chapter 4

In conclusion, the electrical properties of ALD-SiO_2 on SiC-MOS structure has been investigated. Although large V_{fb} and V_{hyst} voltage have been found for ALD-SiO_2 without annealing treatment, which indicates that large bulk and oxide trap density exists in the dielectric layer and dielectric/SiC interface. ALD-SiO_2 with PDA and PMA treatment showed large properties improvement. PMA process can effectively reduce both bulk and interface defects in the ALD-SiO_2 gate dielectrics on SiC substrates. The out-diffusion of oxygen atoms in the gate W layer is one of the sources to form additional interface oxidation. With longer PMA duration, reduction in the oxygen partial pressure results in the inhibition of the interface oxidation and the oxygen atoms may compensate oxygen deficiency and to remove the residual carbon atoms in the SiO_2 layer. Also, SiC MOSFET fabricated with ALD-SiO_2 has been investigated, the electron mobility of about 12 cm^2/Vs has been achieved with PMA treatment, which is comparatively good compared with SiC MOSFET using thermal grown SiO_2 [4-11].

4.7 Reference

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Chapter.5 Enhanced oxidation effect with La_2O_3 insertion

5.1 Introduction

La_2O_3 has long been studied as a higk-k material for scaling of gate oxide on Si MOSFET devices [5-1, 5-2, 5-3]. Reaction of La_2O_3 with Si substrate has been found to be capable even at low temperature and uniform layer of La-silicate can be formed after the annealing [5-4]. La_2O_3 is also known to create radical oxygen atoms from oxygen molecules [5-5]. For ALD-SiO_2 gate dielectric, the high concentration of carbon residue is the main issue for reliability on SiC power devices. With La_2O_3 generating radical oxygen during the annealing process, one can expect for a reduction in carbon concentration in gate dielectric film, which may improve the quality of ALD-SiO_2 on SiC as gate dielectrics. However, the reaction of La_2O_3 on SiC substrate has seldom been studied. To elucidate the modifying mechanism of La-silicate on SiC substrate, the understanding of reaction and formation of La-silicate on SiC is necessary.

In this chapter, the reaction of La_2O_3 on SiC substrate and formation of La-silicate will be introduced. The reaction on SiC substrate has been studied by ATR-FTIR and XPS and formation of La-silicate has been found. The morphology of SiC substrate after La_2O_3 capped annealing was illustrated by TEM cross-sectional image and a hypothesis of enhanced oxidation has been proposed.

5.2 An enhanced oxidation effect by La_2O_3 capped annealing on SiC

Fig.5.2.1 (a) and Fig. 5.2.1 (b) shows the infrared spectra of SiC substrate without and with 2 nm La_2O_3 after annealing at from 500^{o}C to 1000^{o}C. Both are annealed in 5% O_2/95% N_2 ambient and are normalized by a signal from SiC substrate. Fig. 5.2.1 (a) shows the IR absorption spectra of the same SiC substrate annealed at a different temperature. The absorption peak at around 1250 cm^{-1} with limited intensity was observed,

which are attributed to the longitudinal (LO) mode of the asymmetric stretching vibration of Si-O-Si bond absorption [5-6]. The absorption of Si-O-Si bond absorption appeared at 600 °C and increase with raising of temperature. Fig. 2b shows the IR absorption spectra of same SiC substrate with 2nm La_2O_3 deposited at the different annealing temperature. The large absorption peak at around 1250 cm^{-1} and 1065 cm^{-1} are attributed to the LO modes of the asymmetric stretching vibration of Si-O-Si and La-O-Si-O bond [5-7]. Both of the peaks appeared at 900 °C and increase significantly with the temperature raises. The tremendous increase of Si-O-Si bond absorption peak indicates that the oxidation of SiC substrate was enhanced by La_2O_3 capped annealing.

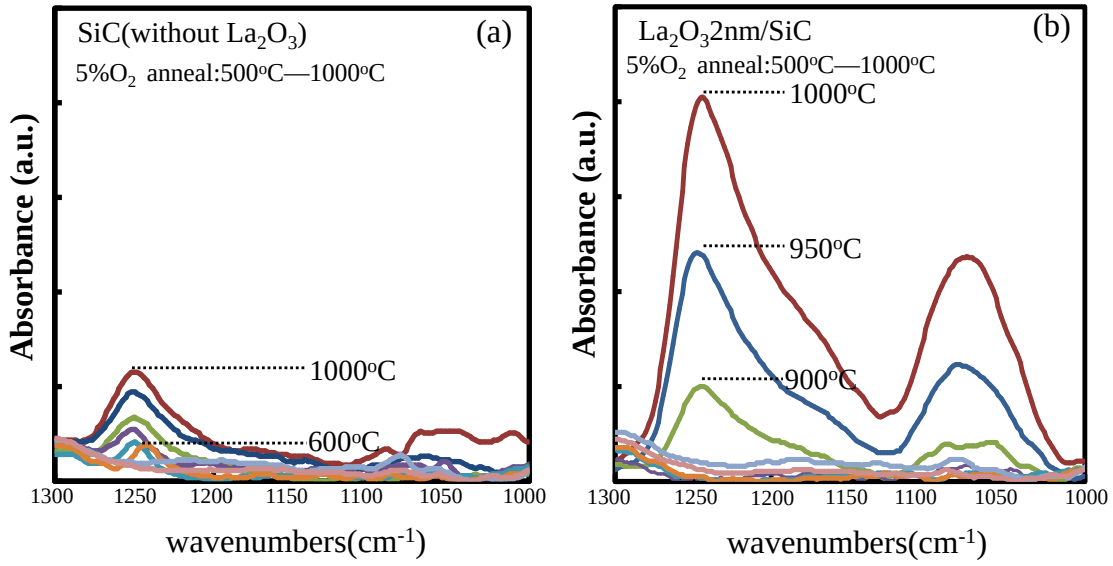

Figure 5.2.1 IR absorption spectra of (a)SiC substrate without La_2O_3 (b)SiC substrate with 2nm La_2O_3

The enhancement of SiC oxidation by La_2O_3 capped annealing is considered to be related to the generation of radical oxygen during the annealing by La_2O_3. From previous

study, we have found La_2O_3 has the ability to generate radical oxygen during annealing in an oxygen ambient. The oxidation of SiC substrate by radical oxygen has to be taken into account during the SiC oxidation process. Y. Song et al, present a modified Deal-Grove model for SiC thermal oxidation which modified the oxidation model of SiC by taking into consideration of CO gas out-diffusion [5-8]. For the oxidation at SiC surface, the oxidation rate is just a related to the local concentration of oxygen and CO gas. And the growth rate of SiO_2 can be expressed as follow:

$$\frac{dX}{dt} = \frac{Js}{N_0} = \frac{K_f C_{O_2} - K_r C_{CO}}{N_0} \tag{1}$$

Where X is the thermal grown SiO_2 thickness, K_f and K_r are the rate constant for the forward and reverse reaction. C_{O2} and C_{CO} refer to the concentration of O_2 and CO, respectively. And N_0 is the number of oxidant molecules incorporated into a unit volume. But for La_2O_3 capped oxidation on the 4H-SiC substrate, the oxidation by radical oxygen should also be considered. Assume the concentration of radical oxygen is C_{O*}, and the rate constant is K_g, the oxidation rate for La_2O_3 capped oxidation can be express as the following:

$$\frac{dX}{dt} = \frac{Js}{N_0} = \frac{K_f C_{O_2} - K_r C_{CO} + K_g C_{O*}}{N_0} \tag{2}$$

Since the radical oxygen is highly reactive, the rate constant of radical oxygen K_g can be much higher than that of the oxygen molecule, so an enhanced rate of oxidation can be achieved for La_2O_3 capped annealing on SiC substrate. With the cooperation of radical oxygen during the annealing, one can expect more consumption of residual carbon in ALD-SiO_2 gate dielectric layer.

5.3 Cross-sectional image of interface above SiC substrate after annealing by TEM

Since the formed La-silicate is far-more thinner than SiO_2. It is necessary to know the morphology of formed gate dielectric on SiC by annealing. Fig 5.3.1 shows the cross-sectional image of interface above SiC substrate after annealing. The dark region in the SiO_2 film is La-silicate and the bright region on SiC substrate is SiO_2. From the TEM image, we could see that the La-silicate is agglomerated in the SiO_2 film. The SiO_2 that formed on by oxidation, however, is much thicker than the origin deposited La_2O_3 on SiC. SiO_2 remains in amorphous and has a thickness of about 10 nm. A large oxidation fluctuation has been shown by the surface roughness of formed SiO_2. The agglomerated La-silicate grain seems tend to gather on the top of SiC epitaxial step. This kind of uneven La-SiO_2 and La-silicate may cause reliability issue such as local electric filed crowding and remote-surface-roughness scattering [5-9] to degrade the mobility of SiC MOSFET.

The oxidation fluctuation could be attributed to the facet oxidation of SiC. Compared with thermal oxidation of Si, the unique properties of SiC is to generate CO molecules during the oxidation process, the following reaction governs the oxidation of SiC:

$$SiC+1.5O_2 \longleftrightarrow SiO_2+CO \qquad (1)$$

Fig 5.3.2 shows the facet dependent oxidation rate of SiC [5-8], from which we could see that for SiC, C-face (000-1) has the highest oxidation rate, since out-diffusion of CO gas is more easily on C-face. Oxidation rate on α–face (11-20) follows the C-face. Compared with C-face, the oxidation rate of Si-face (0001) is one-tenth of C-face, lowest

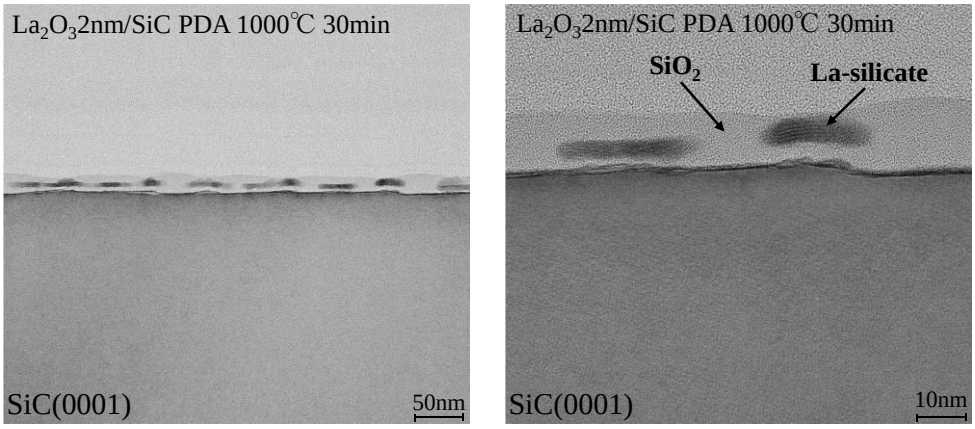

Fig 5.3.1 sectional image of interface above SiC substrate after annealing

in all SiC face because the unfeasible for out-diffusion of CO gases. For SiC, step controlled epitaxy is a basic process to improve the crystal quality used for device fabrication. By step controlled epitaxy, SiC substrate surface is jagged and form structure so-called terrace and step. The terrace is the original Si-face and the crystal face of the step is considered to be α–face (11-20). The illustration image for oxidation of SiC substrate with epitaxy layer is shown in Fig 5.3.3. Since the oxidation rate on different crystal face is different, a thicker layer of SiO_2 will firstly grow on top of the step position. With the oxidation process, the step will gradually consume and finally form a SiO_2 layer with an uneven surface. For La_2O_3 capped annealing, the same facet oxidation can happen and also cause the oxidation variation of SiO_2.

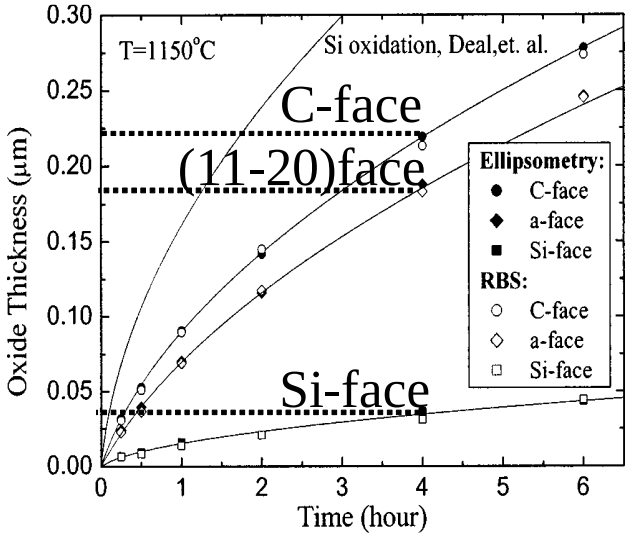

Fig 5.3.2 Oxide thickness as a function of time for dry thermal oxidation of the (0001) C-face, (11-20) a-face, and (0001) Si-terminated faces of 4H-SiC at 1150 °C

Fig 5.3.3 the simulation of oxidation of SiC epitaxy surface layer

Although La-silicate grain agglomerated in the grown SiO_2 layer, a thickness of approximately 10 nm has been achieved by annealing in 5% O_2 at 1000 °C for 30 min. Fig 5.1.6 shows the enhanced oxidation effect of La_2O_3 capped annealing compared with traditional dry thermal oxidation. The dashed line is the SiO_2 growth rate of thermal oxidation [5-10]. The red mark is the oxidation rate by this study. Compared with traditional thermal oxidation, the oxidation rate of La_2O_3 capped annealing is two orders of magnitude larger at oxidation temperature at 1000 °C, which should be attributed to the catalytic effect of La_2O_3.

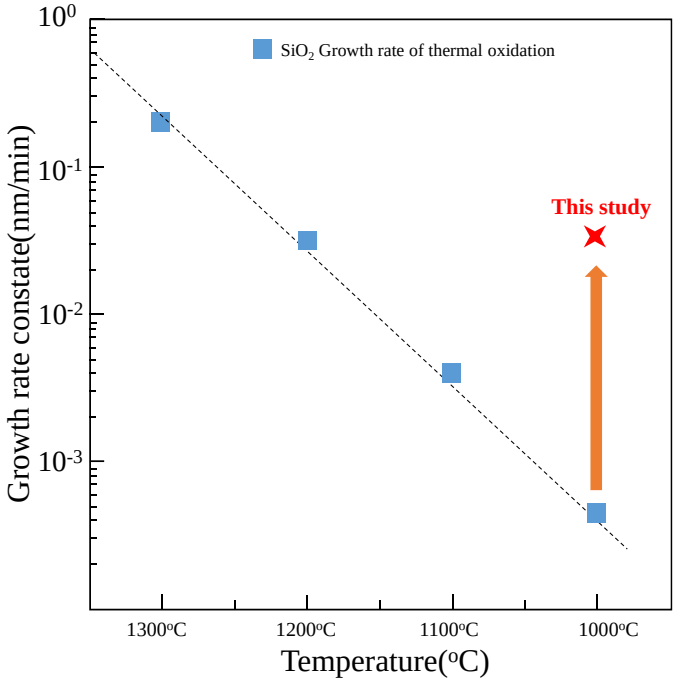

Fig 5.1.6 Enhanced oxidation by La_2O_3 capping compared with dry thermal oxidation

5.4 XPS analysis of interface above SiC substrate with La-silicate

To re-check the chemical composition on reacted La_2O_3 capped SiC substrate. XPS measurement has also been conducted. Fig 5.4.1 shows the deconvoluted binding energy of O (1*s*) and Si (2*p*) peak of SiC with 2nm deposited La_2O_3. Fig 5.4.1 (a) shows the deconvoluted binding energy of O(1s). The biggest peak with a binding energy of 533 eV should originate from O-Si bond, a small peak around 531.5 eV is from the bond of La-O-Si [5-11]. Fig 5.4.1 (b) shows the deconvoluted XPS spectra of Si (2*p*). Si 2*p* was decomposed into Si-O, Si-O-La, Si-C bond, with bonding energy of 155.5 eV, 153.5 eV, 152 eV, respectively, the biggest peak is Si-O, which should be attributed to the composition of SiO_2. A small peak of Si-O-La shows the ratio of La-silicate in oxides grown on SiC is fairly small compared to SiO_2. A weaker peak Si-C should originate from the SiC substrate. Compare the intensity of O-Si, La-O-Si bond in O1s spectra and Si-O,

Si-O-La bond in Si 2*s* spectra, it is clear that the XPS signal from SiO_2 is much higher than La-silicate, which means that SiO_2 is the dominate gate oxide in the formed gate dielectrics.

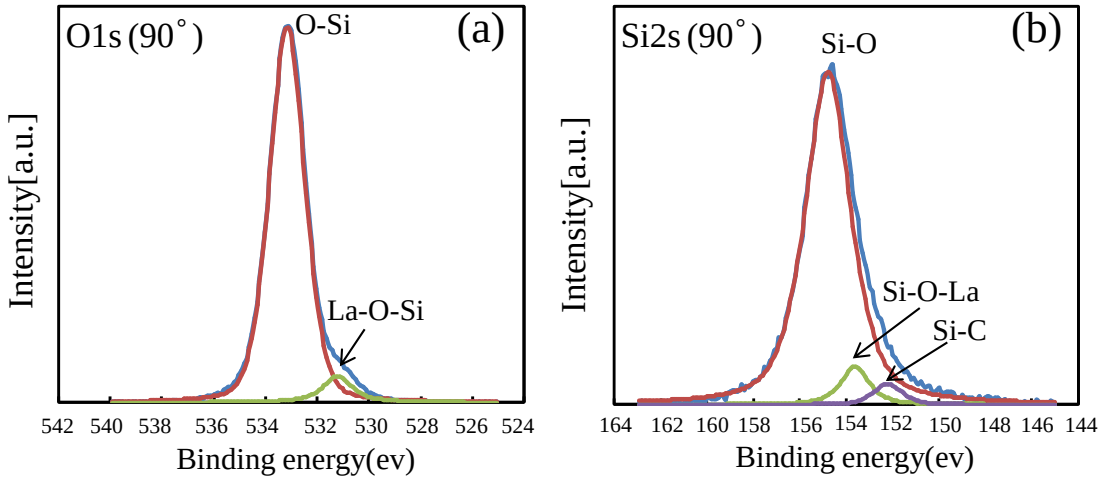

Fig 5.4.1 Deconvoluted of binding energy of (a) O *1s* and (b) Si *2s* XPS spectra

5.5 Suppression of oxidation fluctuation for SiC substrate with La-silicate

In section 5.3, the formation of La-silicate on SiC substrate has been discussed. Annealing of La_2O_3 on SiC in O_2 ambient created a La-silicate layer as well as 10-nm-thick thermally grown SiO_2 layer. However, La-silicate has not formed as a uniform layer but agglomerated in the thermal reaction formed SiO_2. This kind of agglomerated La-silicate grains in SiO_2 layers may cause electrical reliability problems. For suppression of the agglomeration of La-silicate, a SiO_2 capped annealing has been applied for La-silicate formation. Fig 5.5.1 illustrated the uniform La-silicate formation mechanism by SiO_2 capped annealing. Without SiO_2 capping layer, during the annealing, the upward direction flow is dominating for formed La-silicate. Since the oxidation of SiC substrate is highly

facet dependent, finally an uneven La-silicate layer will be formed. However, with SiO_2 capping layer, the upward flow of La-silicate are suppressed and the flow of interface layer can be uniform. With even flow of La_2O_3 and La-silicate, suppression of La-silicate agglomeration can be prospected.

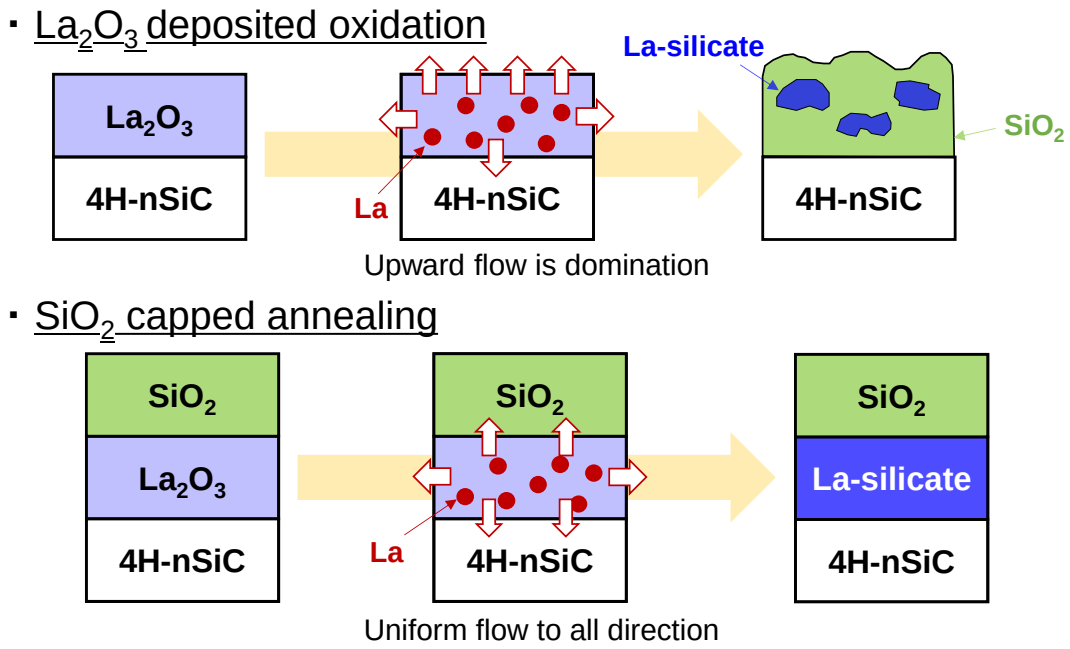

Figure 5.5.1 Illustration of SiO_2 capped annealing for uniform lanthanum silicate layer formation

For indication, a SiC substrate with 2 nm La_2O_3 and 40 nm ALD-SiO_2 has been annealing in O_2 ambient at 1100°C for 30 min. Figure 6.2.2 shows the TEM cross-sectional image of the SiC substrate with La_2O_3 and SiO_2 after annealing. The formed La-silicate has not agglomerated but formed a layer between ALD-SiO_2 and thermally grown SiO_2. However, an oxidation fluctuation has been observed for thermally grown SiO_2. The thickness of thermally grown SiO_2 is ranging from 4 nm to 7 nm. This kind of thick

SiO_2 is generated by SiC substrate reacted with radical oxygen generated by La_2O_3 during the annealing. A roughly SiC surface indicated that facet dependent oxidation has occurred during the annealing. The SiO_2 upon the hollow of SiC surface is thick than the bunch of SiC. Also, the La-silicate is much bright upon the hollow region of SiC surface, which should be attributed to La_2O_3 reaction with more SiO_2 generated by thermal oxidation.

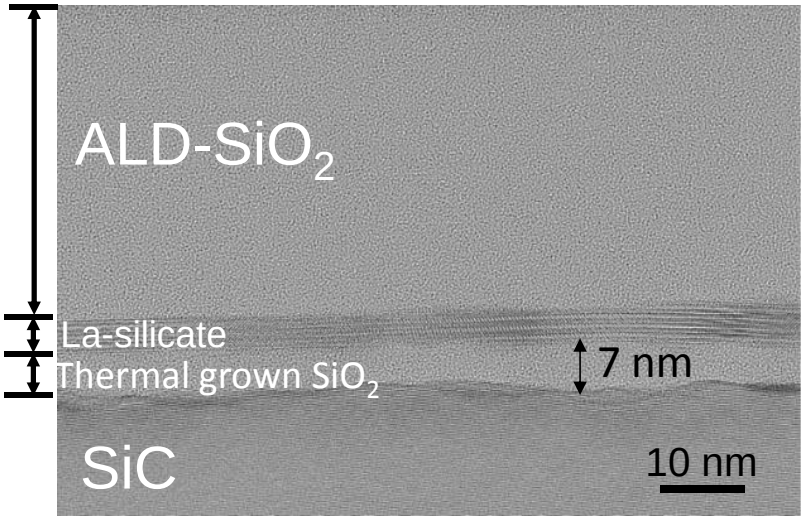

Figure 5.5.2 TEM cross-sectional image of SiC substrate with La_2O_3 and ALD-SiO_2 after annealing

Although the agglomeration of La-silicate has been suppressed by SiO_2 capped annealing. The SiC oxidation enhancement by La_2O_3 still occurred and result in forming uneven interface SiO_2 and La-silicate layer. To achieve high reliability and high properties SiC MOS-devices, the formation of uniform gate dielectrics is necessary. For the reaction of La_2O_3 on SiC, the facet oxidation inevitably occurred after high-temperature annealing due to the generation of radical oxygen by La_2O_3. Insertion of the deposited SiO_2 layer

between SiC substrate and La_2O_3 is considered to be effective to suppress the oxidation of SiC substrate. Figure 5.2.3 shows the TEM sectional image of SiC substrate with 8 nm ALD-SiO_2 IL and 10 nm La_2O_3 layer capped by 40 nm ALD-SiO_2 after annealing in O_2 ambient at 1100°C for 30 min. A uniform layer of La-silicate and interface SiO_2 has been observed. With SiO_2 IL, radical oxygen diffused to SiC surface can be diminished. Also, La-silicate can be formed by reaction of La_2O_3 with SiO_2 upon 800°C [5-12]. Indeed, the interface layer of SiO_2 slight reduced after annealing, which is an evidence for the reaction of La_2O_3 with SiO_2 IL. Since La_2O_3 and deposited SiO_2 are both amorphous before annealing, a uniform layer of La-silicate can be formed by reaction of La_2O_3 and SiO_2.

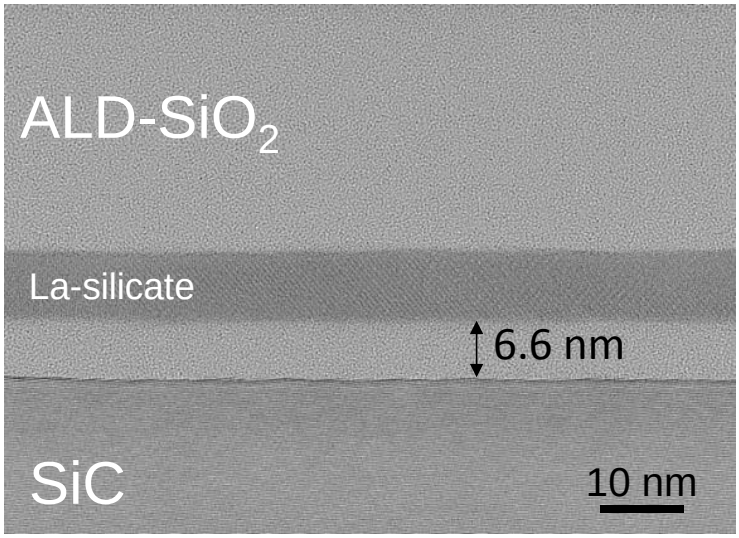

Figure 5.5.2 TEM cross-sectional image of SiC substrate with La_2O_3 and ALD-SiO_2 IL with thick ALD-SiO_2 capping layer after annealing

5.6 Reduction of residual C concentration in ALD-SiO_2 by La_2O_3

La_2O_3 and La-silicate are known to produce highly reactive oxygen radicals with the supply of O_2 molecules [4-4]. During the silicate reaction at PDA process, these oxygen

radicals may oxidize the residual species, namely C and N atoms, reside in the ALD-SiO_2 layer. To confirm the reduction in the C concentration by the presence of La_2O_3 layer, La_2O_3 capped annealing experiment has been conducted. Samples having a 40-nm-thick ALD-SiO_2 layer on SiC substrates were fabricated. After PDA at 1100°C for 30 min, 2-nm-thick La_2O_3 layer was capped on one of the samples and one without the La_2O_3 layer was fabricated as a reference. A 50-nm-thick W layer was deposited on both samples followed by PMA at 950°C for 10^3 s. Figure 6.3.3 shows the C concentration of both samples measured by SIMS. The minimum C concentration in the ALD-SiO_2 layer decreased from 3×10^{20} cm^{-3} to 3×10^{19} cm^{-3} by the La_2O_3 capping and the PMA treatment. Therefore, with La_2O_3 capping annealing, the reduction of residual C concentration in ALD-SiO_2 can be achieved.

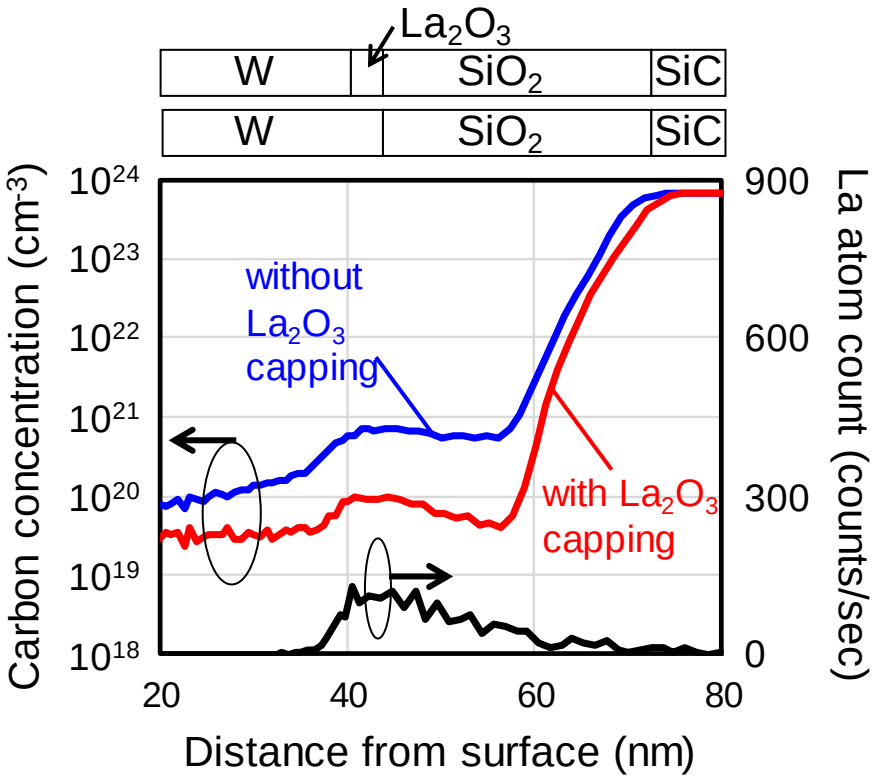

Figure 5.6.1 SIMS depth profile of C and La atoms with and without La_2O_3 capping.

Besides, the diffusion of La atom into the SiO_2 is also observed as shown in fig. 5.6.1. It is reported that the diffusion of La atoms into the ALD-SiO_2 can contribute to passivate oxygen vacancy defects in the layer [5-13]. As the glass transition temperature of a thin La-silicate film is reported to be 600^oC [4-7], annealing above this temperature can release the strain in the film to reduce the defects [5-14]. The reduction in the C concentration and the incorporation of La atoms may be the origin of the improvements in the electrical characteristic with La-silicate IL.

5.7 Summary of chapter 5

In this chapter, the reaction, and formation of La-silicate on SiC substrate by La_2O_3 capped annealing has been investigated. An enhanced oxidation by La_2O_3 capped annealing in O_2 ambient has been found, which should be attributed to the catalytic effect of La_2O_3 to generate radical oxygen during the annealing. TEM cross-sectional image of interface layer after annealing shows that about 10 nm thick thermal grown SiO_2 has been formed, compared with thermal dry oxidation, about two magnitudes of oxidation enhancement has been obtained. However, La-silicate has not formed a uniform layer but agglomerated in the layer of SiO_2, which may induce electrical reliability issues. SiO_2 capped annealing effectively suppress La-silicate agglomeration, but facet dependent oxidation still occurred on SiC with the enhancement by La_2O_3. With the incorporation of SiO_2 capping and IL-SiO_2 insertion, a uniform layer of La-silicate and SIO_2 IL after annealing has been achieved, due to the diminution of SiC oxidation by IL-SiO_2. Physical analysis of ALD-SiO_2 with La_2O_3 capped annealing revealed that residual C

concentration in ALD-SiO_2 reduced with La_2O_3 capping. Also, Lanthanum atoms diffuse into the layer of ALD-SiO_2, which may be one electrical characteristic improvement reason for SiC MOS-devices with the La_2O_3 layer.

5.8 Reference

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Chapter 6 Gate dielectrics of ALD-SiO_2 with La-silicate interface layer

6.1 Introduction

For ALD-SiO_2 using TDMAS as a precursor material, a high concentration of residual carbon atoms was detected in the deposited SiO_2 layer [6-1].Since carbon residue in the SiO_2 layer may cause reliability problem and degradation of electrical properties, the elimination of residual carbon becomes a key for application of ALD-SiO_2 gate dielectric on SiC power devices. In chapter 4, the method using PMA treatment for carbon residue reduction and one order of carbon concentration reduction has been found for the sample with PMA treatment. For more electrical properties improvement, further elimination of carbon trap is necessary.

In this chapter, the electrical properties of SiC MOS-capacitor with lanthanum silicate interface layer has been evaluated, and the chemical composition of gate dielectric has been investigated by multiple physics methods. A simulation model has been used for extraction of border trap density in gate dielectrics for SiC capacitor with La-silicate interface layer.

6.2 Interface properties of a capacitor with La-silicate

A SiC capacitor with 2 nm thick La-silicate IL has been fabricated for electrical properties investigation. A 2-nm-thick La_2O_3 layer was deposited by electron beam evaporation. Then, a 50-nm-thick SiO_2 layer was deposited by ALD process. After the ALD process, the sample was post-deposition-annealed (PDA) in O_2 ambient at 900^oC for 30 min. La-silicate IL is formed by interface reaction between the La_2O_3 and the SiO_2 layers during the PDA process [6-2].

The cross-sectional TEM image of the capacitor with the La-silicate IL is shown in fig. 6.2.2, where a uniform 2-nm-thick amorphous IL can be observed. No interface SiO_2 has

been formed between La-silicate and SiC substrate indicating the oxidation of SiC has been suppressed successfully. The uniformity of La-silicate has also demonstrated that agglomeration of La-silicate was eliminated by SiO_2 capped annealing.

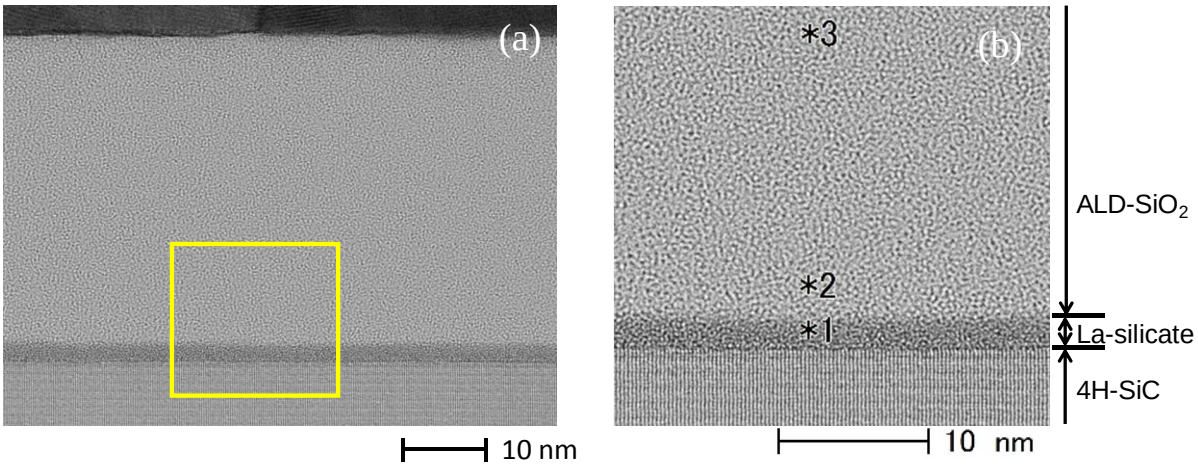
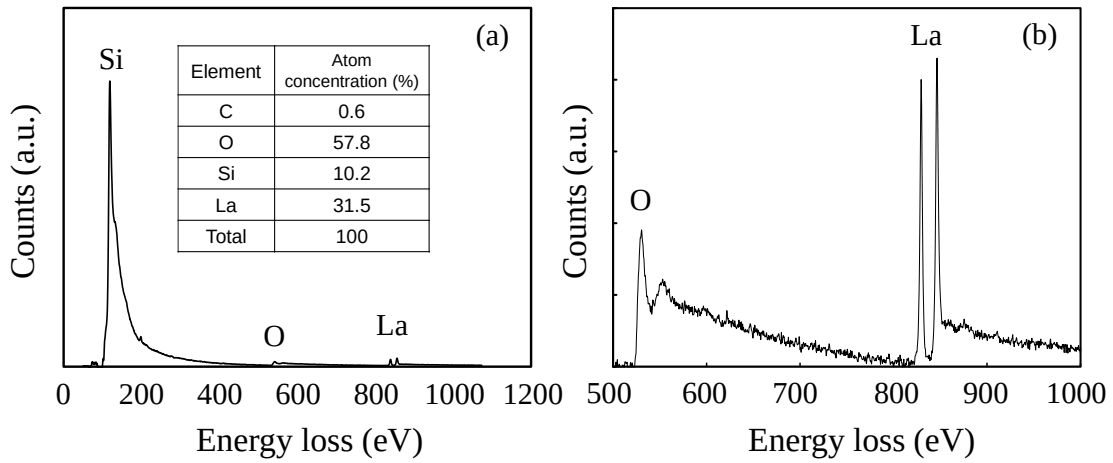


Figure 6.2.2 (a) Cross-sectional TEM image of the capacitor with La-silicate IL. 2-nm-thick La-silicate IL is formed directly on the 4H-SiC surface. (b) The magnified area at SiC/La-silicate/SiO_2 interface.

Figure 6.2.3 shows the electron energy loss spectroscopy (EELS) analysis of the interface layer which is considered to be La-silicate. The peak of Si at 118 eV, O at 550 eV, 560 eV and La at 837 eV, 858 eV has appeared in the spectra, and the semi-quantitative analysis by EELS also revealed an atomic composition of the IL layer to be roughly La:Si:O=3:1:6, which indicates the formation of La-silicate has been achieved by SiO_2 capping annealing of La_2O_3 on SiC substrate.



Element	Atom concentration (%)
C	0.6
O	57.8
Si	10.2
La	31.5
Total	100

Figure 6.2.3 (a) EELS analysis for La-silicate layer (b) magnified spectra showing La and O peak of EELS (point 1 in figure 6.2.2 (b)

Fig 6.2.4 shows the C-V characteristic of SiC-MOS capacitor with and without 2 nm of the La-silicate interface layer, respectively. For a sample with the lanthanum silicate interface layer, a slightly positive shift away from the ideal C-V direction indicates that little increase of the negatively charged fixed defects in the gate dielectric and/or at the dielectric/SiC interface. However, compared to sample with the single SiO_2 gate dielectric, the slopes of the *C-V* curves become steeper for SiC capacitor with lanthanum silicate layer, so a reduction in the D_{it} can be expected. Terman method [6-3] revealed D_{it} reduction from 3.4×10^{12} cm^{-2}/eV to 1.6×10^{12} cm^{-2}/eV at 0.24 eV away from the 4H-SiC conduction band edge (E_C) with the La-silicate IL. However, due to the detection accuracy limit of the Terman method, quantitative analysis is required to extract the D_{it} [6-4]. In addition, the frequency dispersion of *C-V* characteristic is smaller for the sample with La-silicate layer, which could be attributed to the reduction of border trap in SiO_2 gate dielectric [6-5].

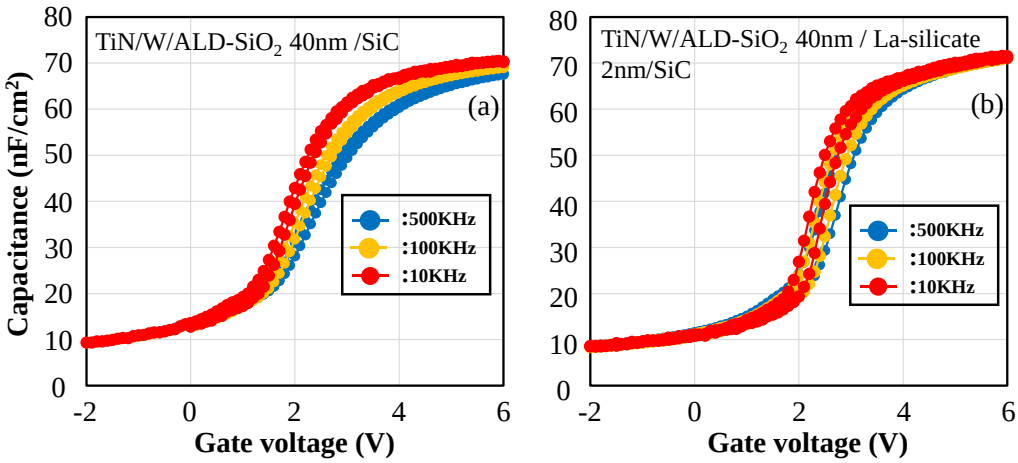


Figure 6.2.4 C-V characteristics of the samples (a) with ALD-SiO_2 gate dielectric only (b) with lanthanum silicate interface gate dielectric.

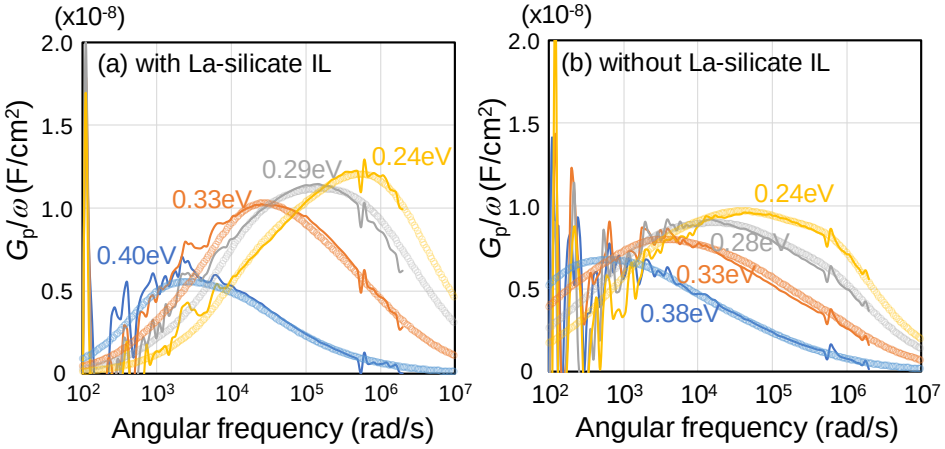


Figure 6.2.5 G_p/ω spectra of MOS capacitors fabricated (a) with and (b) without La-silicate IL.

For further electrical properties investigation, conductance method has been used for interface state density extraction. Figure 6.2.5 (a) and 6.2.5 (b) revealed the frequency dependency of *G*p/ω for the sample with and without a La-silicate layer, respectively. Although the maxim value of *G*p/ω is larger for the sample with La-silicate layer,

However, narrower spectra with smaller full-width half-maximum (FWHM) can be observed with the La-silicate IL. Moreover, the asymmetrical shape in the spectra strongly suggests a steep change in the D_{it} within the bandgap due to the surface potential fluctuation [6-6]. Therefore, detailed characterization is needed to understand the interface properties. Numerical curve fitting to the obtained G_p/ω spectra based on continuum distribution of interface states [6-7, 6-8]. Indeed, accounting for the surface potential fluctuation with a standard deviation (σ_s) was also shown in the fig 6.2.6 (a) revealed that smaller surface potential deviation has been achieved for the sample with La-silicate interface layer. Generally, a high σ_s indicates the presence of a large amount of Q_{fix} or D_{it} at the interface [6-6], Furthermore, σ_s is also influenced by the dielectric constants of semiconductor and dielectric [6-6]. A simple formula based on solving an electrostatic problem of a point charge at the interface between a semiconductor and a dielectric indicates that σ_s is proportional to $(\varepsilon_s+\varepsilon_{ox})^{-1}$, where ε_s and ε_{ox} are the dielectric constants of the semiconductor and the dielectric, respectively [6-6]. Assuming a dielectric constant of the La-silicate to be 8 [4-4], the σ_s of the MOS capacitor without the La-silicate IL should present a higher value by a factor of 1.3 compared to the one with the La-silicate IL. As the σ_s values revealed more than the contrast in the dielectric constants, one can conclude that the La-silicate IL can reduce the Q_{fix} or D_{it} at the interface. The D_{it} showed only a slight reduction from 8.5×10^{11} cm^{-2}/eV to 7.4×10^{11} cm^{-2}/eV at 0.24 eV from E_C with the La-silicate IL, as shown in fig 6.2.6 (b). Therefore, the reduction in σ_s can be mainly due to the reduction of Q_{fix} at the interface. An increasing trend in the σ_s toward the E_C of the 4H-SiC strongly suggests the interface states are mainly acceptors, in other words, positively charged when emptied [6-9]. Also, the D_{it} distribution shows increasing trend toward the E_C for both MOS capacitors, which is the common trend for

SiO_2/4H-SiC interfaces [6-10]. With these analyses, the origin of the positive shift in the *C-V* curves might be the negative charges reside in the bulk SiO_2 layer.

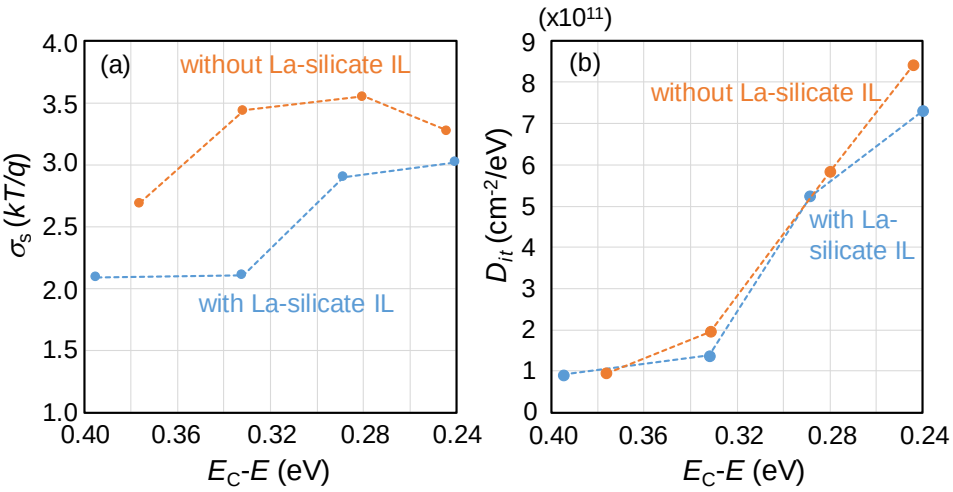


Figure 6.2.6 Distribution of (a) Extracted σ_s normalized by thermal energy and (b) D_{it} with and without La-silicate IL in the bandgap.

6.3 Extraction of border trap for a capacitor with La-silicate

The distribution of the oxide traps near the interface was extracted based on the model presented in refs. [6-3] and [6-11]. Assuming traps located at a position *x* from the SiC surface, the intrinsic oxide capacitance (C_{ox}) can be divided into C_1 and C_2, as shown in fig. 6.3.1. The C_{ot} and G_{ot}, also shown in the small-signal equivalent circuit, the conductance of the traps at the position *x* coupled to the SiC surface, respectively. The sheet density of traps at the position *x* can be derived from $D_{ot}=qC_{ot}$ relationship. Therefore, the trap distribution, $N_{ot}(x)$, in the gate dielectrics can be obtained by taking the differential of the $D_{ot}(x)$. The time constant τ_{ot}, which is the product of C_{ot} and G_{ot}, reflects the average time to empty and to capture electrons. As electrons are captured

based on tunneling probability, τ_{ot} is exponentially proportional to the distance from the SiC surface and can be expressed as [6-12]

$$\tau_t = \tau_0 \exp(2\kappa x). \qquad (6.1)$$

Here, τ_0 is the pre-exponential factor determined by $(\sigma_n v_{th} n_s)^{-1}$, where σ_n, v_{th} and n_s are the electron capture cross section of the traps, thermal velocity and the density of electrons, respectively. κ is the attenuation coefficient of the electron wave function tunneling process. A simple estimation of the κ can be expressed as

$$\kappa = \frac{\sqrt{2m^* \phi_B}}{\hbar}, \qquad (6.2)$$

where m^* and ϕ_B and $\hbar$ are the electron mass of the gate dielectric band offset at the interface, and reduced Plank's constant, respectively [6-12]. Under accumulation condition, n_s can be approximated as the effective density of state (DOS) in the conduction band of the 4H-SiC. By using $m^*=0.55m_0$ and $\phi_B=2.7$ eV with $\sigma=10^{-18}$ cm^2, τ_0 and κ can be calculated as 3×10^{-9} s and 2.5 nm^{-1}, respectively [6-12, 6-13, 6-14]. With these parameters, traps located at 1.2 nm away from the SiC surface can be probed at a frequency of 1 MHz, where those at 2.5 nm can be probed at 1 kHz signal.

Figure 6.3.1 (a) and 6.3.1 (b) show the fitting results to the capacitance (C_m) and the conductance (G_m) values measured from 1 kHz to 1 MHz respectively. The extracted N_{ot} is shown in fig. 6.3.2. Although a slight reduction in the N_{ot} can be observed with the IL insertion, N_{ot} over 10^{20} cm^{-3} is estimated for both samples in the range of 1.5nm<x<2.0nm.

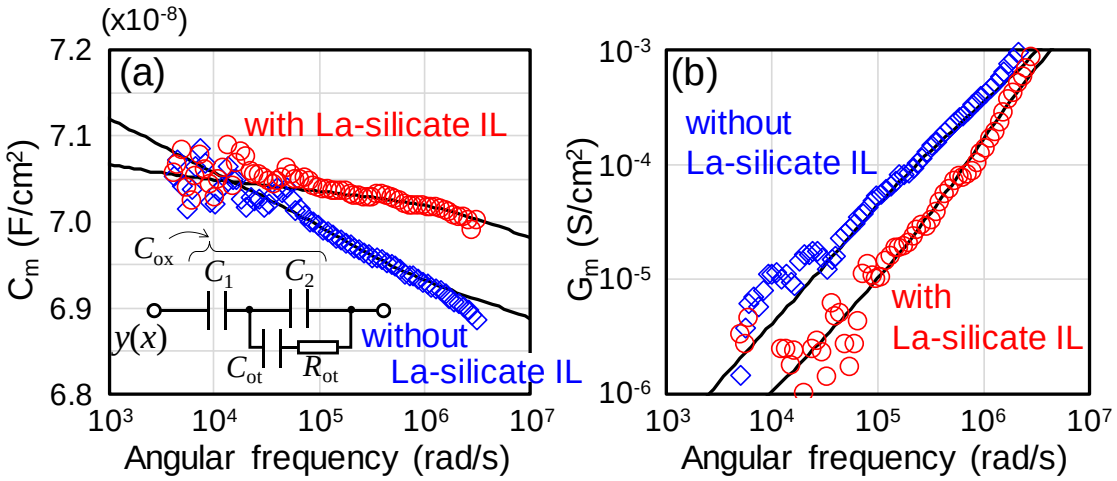


Figure 6.3.1 (a) Frequency dependent capacitance (C_m) values (b) Frequency dependent conductance (G_m) values of the MOS capacitors.

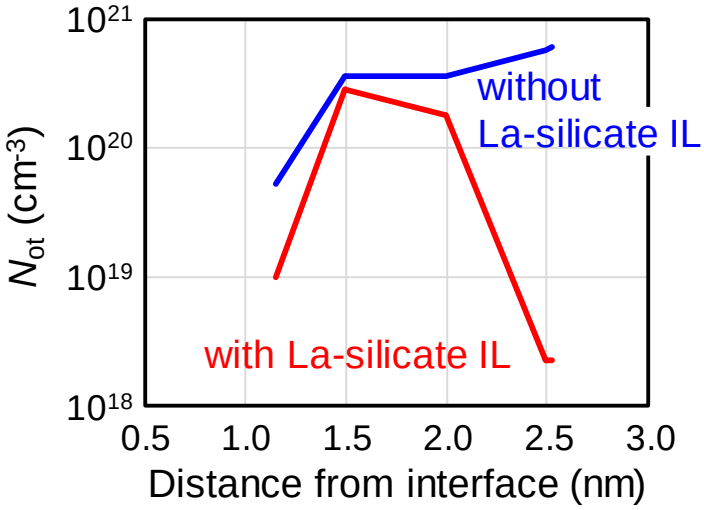


Figure 6.3.2 Extracted N_{ot} of the MOS capacitors.

However, a lower value was obtained near the gate dielectric/SiC interface for a capacitor with the La-silicate interface layer insertion. Moreover, a lower N_{ot} is also obtained at a distance more than 2 nm with the La-silicate sample. Since the boundary of La-silicate and ALD-SiO_2 is about 1.5-2 nm from the gate dielectrics/SiC interface, we could

conclude that a reduction of N_{ot} of two magnitude for SiO_2 adjacent to the interface has been achieved with La-silicate IL insertion. Since La_2O_3 has been demonstrated can effectively reduce the residual C concentration in ALD-SiO_2 by annealing, the obtained improvements in the *C-V* characteristics may be due to the reduction in the C impurity concentration.

It is necessary to mention that the concentration of radical oxygen decade exponentially in the dielectric film [3-1]. For SiC MOS capacitor with the La-silicate interface layer, the residual C at the top of the SiO_2 layer near the gate electrode may hard to be removed. This kind of residual C at the oxide layer near gate electrode can become the origin of fixed charge, which may shift the threshold voltage of SiC MOSFET.

Besides, the EELS analysis of the ALD-SiO_2 layer 2 nm (point 2 in fig. 6.2.2(b)) and 19 nm (point 3 in fig. 6.2.2 (b)) away from the La-silicate layer revealed the presence of La atoms with atomic concentrations of roughly 0.5 % and 0.2 %, respectively. The La atoms presence in ALD-SiO_2 may reduce the electron trap site in ALD-SiO_2 [5-13, 5-14]. The reduction in the C concentration and the incorporation of La atoms may be the origin of the obtained improvements in the electrical characteristic with La-silicate IL.

6.4 Summary of chapter 6

In this chapter, The effect of La-silicate IL on the electrical characteristics SiC MOS capacitors with ALD-SiO_2 gate dielectrics have been investigated. Conductance method revealed improvement in the D_{it} and the reduction in the surface potential fluctuation with the La-silicate IL. Moreover, two orders of magnitude reduction in the N_{ot} in the ALD-SiO_2 layer adjacent to the La-silicate IL was confirmed. Since the physical analysis of

ALD-SiO_2 revealed the reduction of residual C by La_2O_3 capped annealing. Also, the incorporation of La atoms in the SiO_2 layer adjacent to the La-silicate IL. The origin of the improvements with La-silicate IL may be attributed to these contributions.

6.8 Reference

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Chapter 7. Electrical properties of SiC-MOS structure with thin ALD-SiO_2/ La-silicate interface layer

7.1 Introduction

Interface properties improvement of gate dielectric/SiC is a key point for achieving high-performance SiC power devices. Many research group has reported that the severe degrade channel mobility of SiC MOSFET is due to high density of interface electron traps close to the conduction band edge [1-11, 1-12, 7-1]. A big portion of these electron traps are considered to be oxide traps N_{ot} in the gate dielectrics near the SiC interface [7-2, 7-3, 7-4]. Passivation of this kind of high density of N_{ot} is critical for electrical properties enhancement of gate dielectrics for SiC MOS devices.

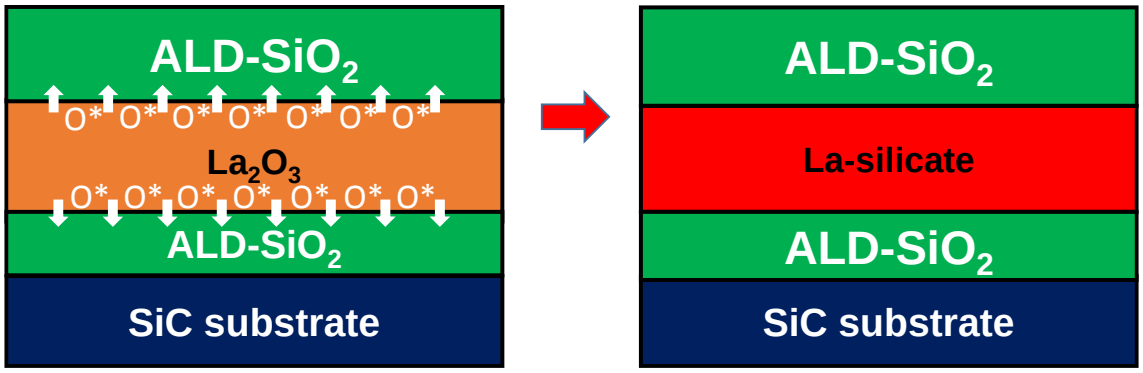

Fig 7.1.1 the schematic structure of ALD-SiO_2/La-silicate/IL SiO_2 gate dielectrics on SiC substrate before and after annealing.

In order to achieve interface passivation of ALD-SiO_2 gate dielectrics, a stacked structure of ALD-SiO_2/La-silciate/ALD-SiO_2 IL stacked gate dielectrics for SiC MOS devices has been proposed and investigated. Figure 7.1.1 shows the schematic structure of the stacked gate dielectrics layer before and after annealing. As we have discussed in chapter 5, La-silicate has the ability to generate radical oxygen that reduce the residual carbon atom in ALD-SiO_2, which result in dramatic reduction of oxide traps in ALD-SiO_2 layer. With the insertion of IL ALD-SiO_2 layer, during thermal annealing the oxide trap

in the IL can be effectively reduced with the incorporation of La_2O_3 generation of radical oxygen to reduce carbon-related defects. Thus the N_{it} can be reduced due to the reduction of N_{ot} near the interface.

On the other side, most high-k materials show the small value of band-gap, and the band-gap width of an insulator decreases with increasing dielectric constant, leading to a low band offset at the interfaces of SiC with the high-k material. As a result of insufficient barrier height, a large leakage current can be expected [7-5]. In order to suppress leakage currents of SiC devices using high-k gate dielectrics, a thin film of SiO_2 can be introduced as a buffer layer between SiC and high-k dielectric with higher band-offset [7-6, 7-7, 7-8, 7-9]. Since the band offset of SiO_2 film on SiC surfaces is about 2.7 eV to 2.8 eV on the 4H-SiC substrate [7-10], the suppression of leakage current can be achieved with high-k layer/SiO_2/SiC structure. For La-silicate, insertion of the SiO_2 thin film is still a useful method for preventing the leakage current.

In this chapter, further electrical properties improvement by using SiO_2/La-silicate interface structure has been illustrated. Both SiC capacitor and MOSFET with SiO_2/La-silicate interface has been fabricated and investigated. Formation of uniform La-silicate layer has been demonstrated by TEM image. And higher electrical mobility has been achieved with SiO_2/La-silicate interface structure, compared with SiC-MOSFET using ALD-SiO_2 only.

7.2 Approaches for further electrical properties improvement with La-silicate layer

In chapter 5, SiC MOS-capacitors with a La-silicate IL were investigated. Compared with SiC capacitors with SiO_2 dielectrics, both N_{ot} and D_{it} reduction were achieved.

However, the V_{fb} and V_{hys} of SiC capacitor with La-silicate are still relatively high (2.48V and 0.32V, respectively). The high V_{fb} can be attributed to large oxide trap density in the ALD-SiO_2 film, which is considered to be related to insufficient diminution of residual C in gate dielectrics. For further electrical properties improvement, the elimination of C induced defect in the SiO_2 layer is necessary. In chapter 5.2, we have demonstrated that PDA treatment is an effective method for reducing the bulk trap in ALD-SiO_2 layer. Also La-silicate is considered to be effective to reduce residual C atoms by generating radical oxygen to enhance the reaction with C atom. Therefore with a thicker La_2O_3 layer, more radical oxygen can be generated and thus reaction with residual C in gate dielectrics can be enhanced, as illustrated in figure 7.2.1.

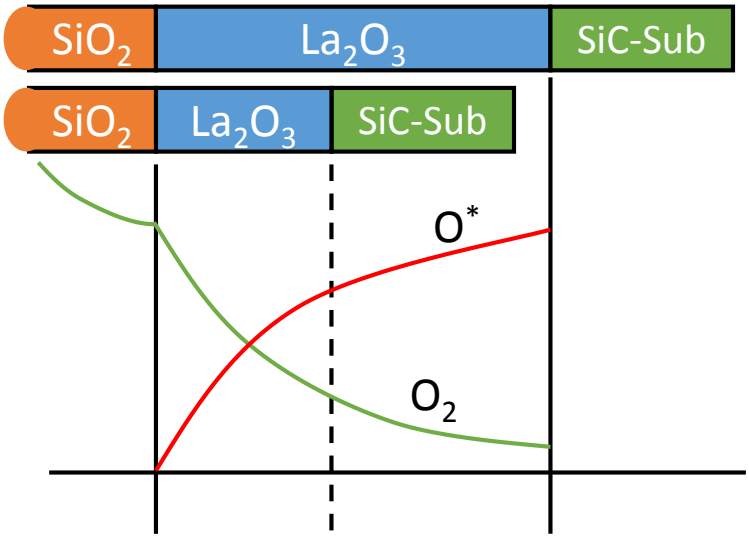

Fig 7.2.1 Illustration of radical oxygen generation enhancement by thicker La_2O_3

To elucidate the effect of PDA treatment in higher temperature and with the thicker La-silicate interface layer, SiC capacitors having a La-silicate interface layer with a thickness ranging from 2-10 nm has been fabricated and was annealing in O_2 ambient at 1100°C

after gate dielectric deposition. Figure 7.2.2 shows the electrical properties of SiC capacitor with deposition of La_2O_3 layer 2 nm, 4 nm, and 10 nm, respectively. For contrast, a capacitor with SiO_2 gate dielectric only has also been fabricated and investigated. As shown in the figure 7.2.2 (a), with increasing thickness of La-silicate interface layer, the flat-band voltage of SiC capacitor shift to the negative direction, which indicated the reduction of bulk trap density in gate dielectrics. The equivalent oxide thickness (EOT) has been confirmed to increase with the insertion of La-silicate layer, which should be attributed to the enhanced oxidation by radical oxygen generated from La_2O_3 layer during annealing. The increase of EOT for SiC capacitor with 2nm, 4nm, and 10nm La_2O_3 layer is 8.0 nm, 3.6 nm and 2.1 nm, respectively.

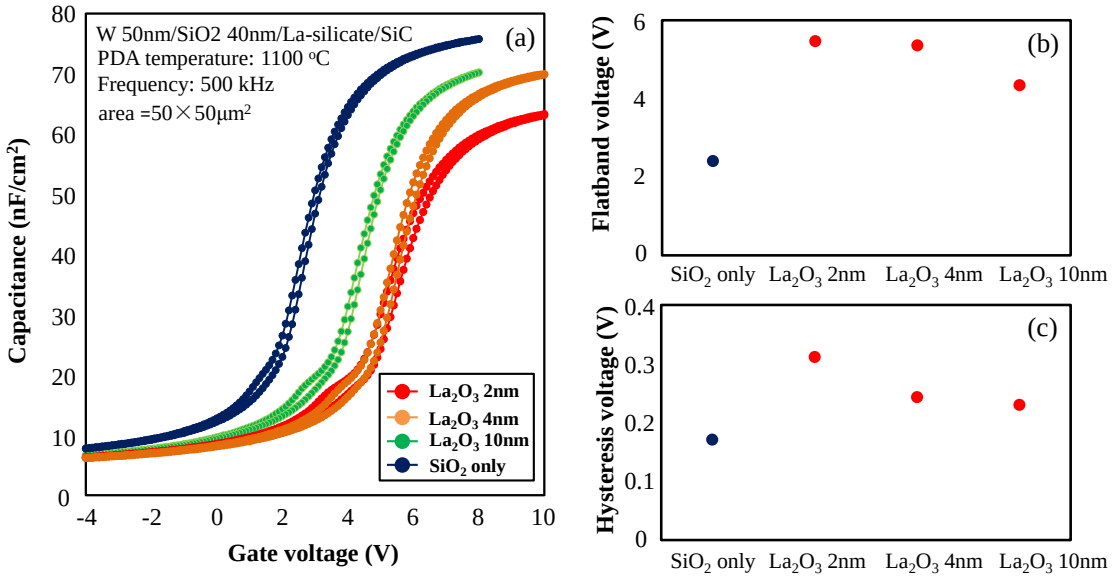

Fig 7.2.2 Electrical properties of SiC capacitor with different thickness of La-silicate layer (a) C-V characteristics (b) flat-band voltage (c) hysteresis voltage

Figure 7.2.3 shows the TEM cross-sectional image of SiC capacitor with 2 nm La_2O_3 interface layer after annealing. As shown in the figure, the formed La-silicate, intermittently appeared with the dark region and bright region, is crystallized. The thermally formed SiO_2 under La-silicate layer showed a thickness fluctuation from 4-7 nm. The bright region of La-silicate upon the hollow of SiC surface is considered to be formed with thermally grown SiO_2. Since the oxidation rate of SiC varies largely with a crystalline face, the SiO_2 grown much rapidly upon the hollow of SiC surface, which result in forming La-silicate with low Si concentration. This kind of oxidation fluctuation and uneven gate dielectric layers may cause local electric field accumulation and degrade the electron mobility by Coulomb scattering from dielectrics layer of SiC MOS-devices. The reduction of EOT by La_2O_3 layer thickness increase is considered to be related with La_2O_3 reaction with thermal grown SiO_2 during the annealing. La_2O_3 has been reported to react with SiO_2 upon 800°C [5-12]. With less La-silicate at the interface, the consumption of SiO_2 formed by thermal grown is smaller and more interface SiO_2 remained after annealing. Figure 7.2.2 (c) shows the hysteresis voltage of capacitor with different thickness of La-silicate. A reduction of hysteresis has also been found with the thicker La-silicate interface layer, which should be attributed to the reduction of border trap at the near-interface. However, all the SiC capacitor with La-silicate interface layer shows larger flat-band voltage and hysteresis voltage compared with the capacitor of SiO_2 gate dielectric, which means that both the bulk trap and border trap of gate dielectrics have been increased with La-silicate layer insertion. This kind of electrical properties degradation can be attributed to the growth of interface SiO_2 by annealing in O_2 ambient. According to figure 4.3.1, annealing at low temperature will trigger the reaction of SiC with oxygen to form C residue. So the thermal grown SiO_2 at 1100°C may contribute to

the generation of the high density of C atom at the interface, which may degrade the interface properties and thus increase the bulk trap and border trap density. Although PDA treatment can significantly improve the electrical properties of ALD-SiO_2 by reducing C related defects. The performance of capacitor using ALD-SiO_2 with La-silicate interface layer was degraded by the generation of interface properties of thermal grown SiO_2 ones.

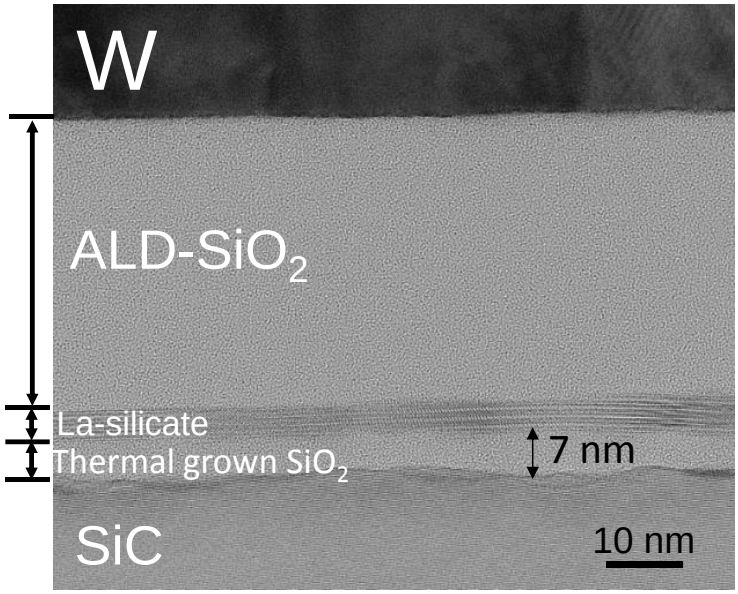

Fig 7.2.3 TEM cross-sectional image of SiC capacitor with 2 nm La-silicate interface layer after annealing at 1100°C.

7.3 Interface properties improvement by ALD-SiO_2/La-silicate IL

In chapter 6, the electrical properties of SiC capacitor with different thickness of La-silicate interface layer has been investigated. The generation of low properties thermal grown SiO_2 interface layer becomes a problem for SiC capacitor with La-silicate gate dielectric layer. For suppressing of thermal grown SiO_2 layer formation, An ALD-SiO_2 interface layer was introduced between SiC substrate and La_2O_3 dielectric layer. By

insertion of deposited SiO_2 layer bellow La_2O_3 layer, the diffusion of both oxygen and radical oxygen to SiC surface can suppress during annealing, and thus reduce the oxidation of SiC substrate. Since La_2O_3 can react with SiO_2, a uniform La-silicate formation can be expected even at low temperature.

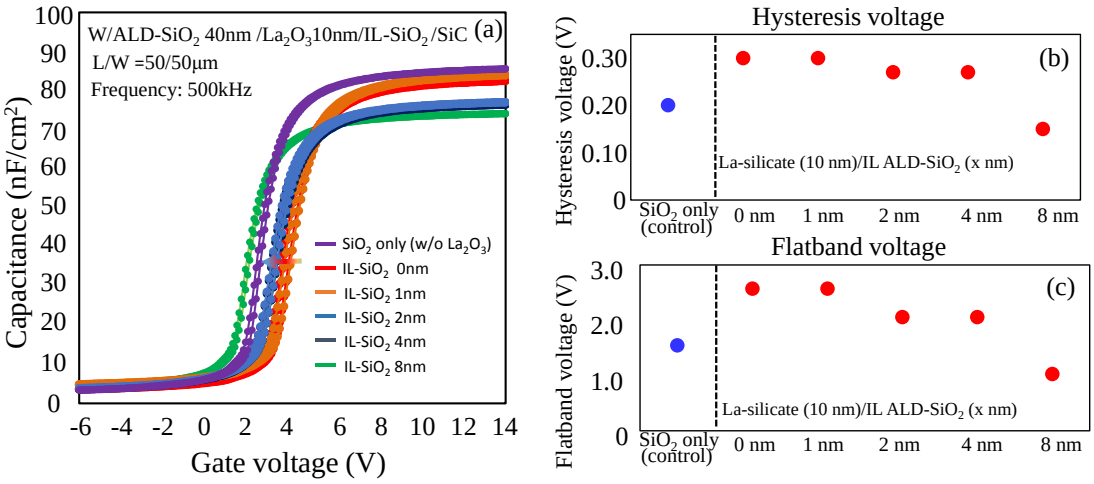

Fig 7.3.1 (a) C-V curves of SiC capacitor with different thickness of interface SiO_2 layer (b) Interface ALD-SiO_2 thickness dependency on hysteresis (c) Interface ALD-SiO_2 thickness dependency on V_{fb}.

To investigate the modification effect of interface SiO_2 (IL-SiO_2) gate dielectric, SiC capacitor with different thickness of IL-SiO_2 has been fabricated and investigated. Figure 7.3.1 shows the electrical properties of SiC capacitor with an IL-SiO_2 thickness ranging from 0-8nm. For contrast, a capacitor with SiO_2 gate dielectric only has also been fabricated. Figure 7.3.1 (a) shows the C-V characteristics of the sample with a different thickness of IL-SiO_2, with an increase of IL-SiO_2 thickness, it is clear that C-V curve shift to the negative direction. The interface ALD-SiO_2 thickness dependency on flat-band voltage (V_{fb}) and hysteresis is shown in fig. 7.3.1 (b) and fig 7.3.1 (c), respectively. By

increasing the thickness, a gradual recovery in both V_{fb} and hysteresis can be obtained and also, with the 8-nm-thick interface ALD-SiO_2 layer, the V_{fb} showed a value of 1.2V, almost very close to the ideal value (0.67V). And the hysteresis exhibited smaller value compared to the sample with a single ALD-SiO_2. The reduction of Vfb and hysteresis indicate that bulk trap and border trap in gate dielectric has been successfully reducing with the insertion of the IL-ALD-SiO_2 layer.

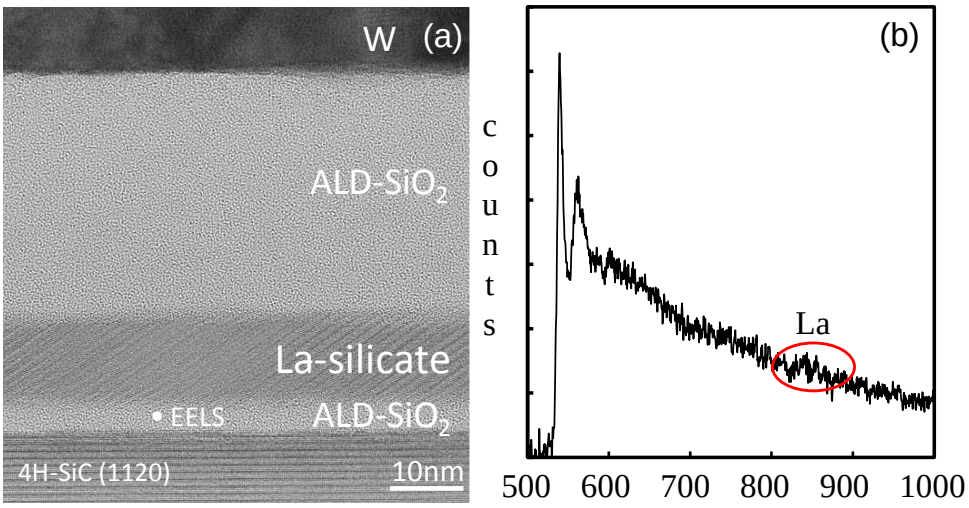

Fig. 7.3.2 (a) TEM image of La-silicate on an interface ALD-SiO2 layer. (b) EELS spectra revealed the presence of La atoms in the interface ALD-SiO2 layer.

Cross-sectional transmission electron microscope (TEM) image of SiC/gate dielectric/electrode has also been analyzed for investigation of the morphology of gate dielectric stacked layer. Figure 7.3.2 (a) shows a sectional image of gate dielectric layer after annealing. La-silicate layer, with a thickness of 10nm, has been formed between ALD-SiO_2 gate dielectrics. Although formed La-silicate is crystallized since the annealing temperature is as high as 1100^{o}C, a uniform layer of La-silicate has been formed and do not agglomerate on the top of ALD-SiO_2. This should be attributed to the

insertion of ALD-SiO_2 layer. Since La-silicate formation is between La_2O_3 and SiO_2, which are both amorphous before annealing, a reaction without growth rate fluctuation at the whole layer can be expected. The interface SiO_2 layer thickness is about 5nm thick after the annealing, indicating that the interface SiO_2 has also reacted with La_2O_3 to form a La-silicate layer. The presence of La atoms in the interface ALD-SiO_2 was confirmed by a small signal in the electron energy loss spectrum (EELS) of the interface ALD-SiO_2 layer. As illustrated in figure 7.3.2 (b). The presence of La atoms in the interface SiO_2 layer might be the key to improve the gate dielectric/SiC interface properties.

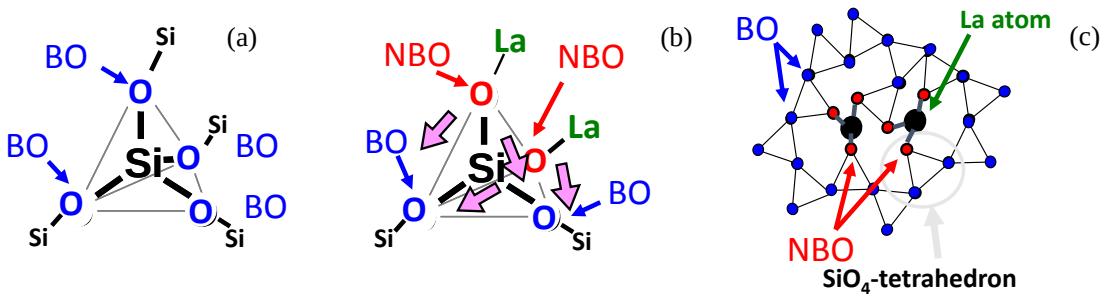

Fig 7.3.3 bonding structure and illustration of moderation effect of La atom in the SiO_2 network (a) Si-O-Si bonding (b) La-O-Si bonding (c) La atom in SiO_2 network

For the interface layer between La-silicate and SiC substrate surface, which is thermal growth by annealing, the little existence of La atom may have an effect to moderate the SiO_2 network [6-15]. Figure 7.3.3 shows the bonding structure and illustration of moderation effect of La atom in the SiO_2 network. For the SiO_2 network, the oxygen atom is fixed by the bridging bond between a silicon atom and an oxygen atom, after annealing, thermal stress may remain in the SiO_2 network and cause the creation of defects. However, the bond of La and oxygen are flexible the oxygen are non-bridging. In the SiO_2 network,

with the non-bridging bond introduced by La atom. The stress left by thermal treatment can be absorbed and the SiO_2 network can be modified.

7.4 Effect of PMA treatment with ALD-SiO_2/La-silicate IL

With the insertion of interface ALD-SiO_2 layer between SiC substrate and La-silicate layer. The formation of low properties thermal grown SiO_2 has been reduced, also a uniform layer of La-silicate has been formed. However, with high-temperature annealing, it is inevitable to form SiO_2 by oxidation of SiC substrate and C residue in gate dielectric layer will increase, which may still degrade the electrical properties of SiC devices with the La-silicate layer. In order to achieve further elimination of carbon-related defects, PMA treatment is considered to be prominent to reduce the C residue at the interface and bulk of gate dielectrics layer. Since the oxygen source is W electrode, which means that the oxygen take part into the reaction is limited and at low concentration, according to the $P(O_2)$–T phase diagram from fig. 5.3.1 the oxidation reaction product of SiC and oxygen will be CO gas and without new C residue generation at the interface. More than that, for SiC substrate with a La-silicate capping layer, furthermore modification effect can be achieved with generating radical oxygen by transferring oxygen into radical oxygen during the PMA treatment duration. Since oxidation of SiC surface is limited by the total amount of oxygen in W electrode layer and diffusion of oxygen in the gate dielectrics. The elimination of C residue can proceed without a new generation of C atom from the substrate surface and thus further electrical properties improvement can be achieved.

Figure 7.4.1 illustrates the *C-V* curve of SiC capacitor with SiO_2 gate dielectric only, with La-silicate and IL-SiO_2 interface and with La-silicate interface, respectively. All the sample are shown by *C-V* characteristics without PMA and with PMA treatment for 5000s

in each figure. With PMA treatment, all the sample shows a large flat-band voltage reduction and *C-V* curve shift to the negative direction. For a sample with La-silicate interface only, a slight reduction of maximum capacitance reveals that EOT of the sample with the direct interface of La-silicate on SiC sub. has been increasing. But for the sample with SiO_2 gate dielectric only and for the sample with ALD-SiO_2/La-silicate IL, almost no EOT increase has been shown, which means that the suppression of SiC substrate oxidation has been successfully achieved with the existence of interface SiO_2 layer. Also, it should be noticed that C-V curve of SiC capacitor with ALD-SiO_2/La-silicate IL shift a little bit larger to the negative direction, which should be attributed to the small value of flat-band voltage for the sample with ALD-SiO_2/La-silicate IL. Also, it is clear that after PMA for 5000s, the hysteresis of C-V curves was almost invisible, showing a significant reduction of border trap for samples with and without La-silicate. The *C-V* curves for all the samples become steeper after PMA treatment for 5000s, which indicated a reduction of interface state density has been achieved.

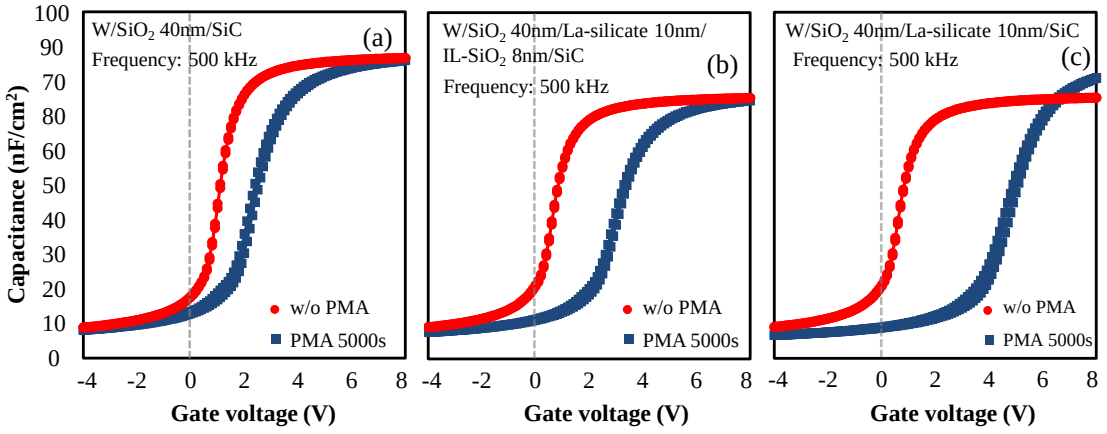

Fig 7.4.1 C-V curves of SiC capacitors (a) with SiO_2 gate dielectric only (b) with ALD-SiO_2/La-silicate IL (c) with La-silicate interface layer.

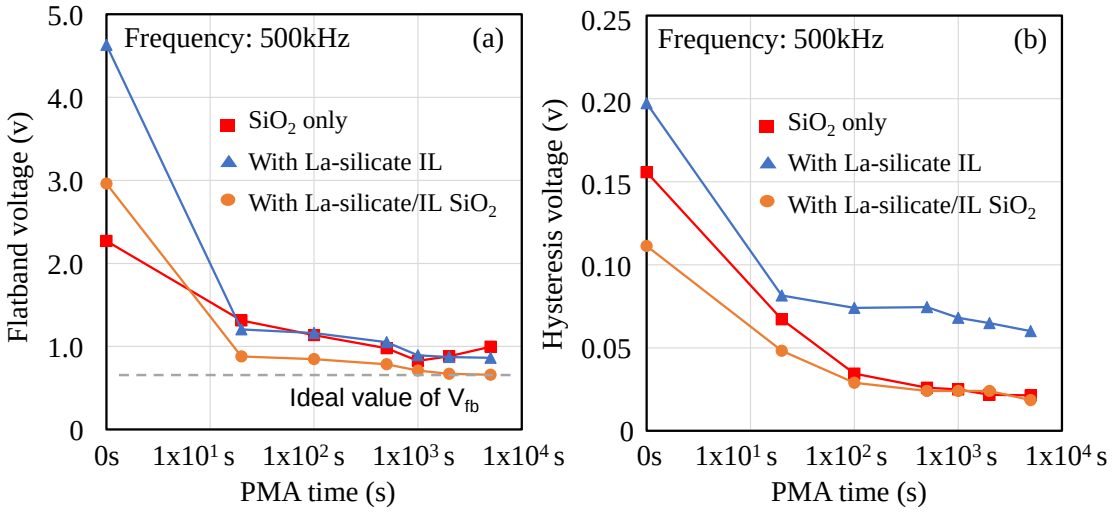

Figure 7.4.2 PMA duration dependency for SiC capacitor of (a) flat-band voltage (b) hysteresis voltage.

Figure 7.4.2 shows the PMA duration dependency of flat-band and hysteresis voltage for the sample with SiO_2 gate dielectric only, with ALD-SiO_2/La-silicate IL and with La-silicate interface, respectively. For a sample with the La-silicate interface layer, both hysteresis and flat-band voltage is showing bigger value than the sample having SiO_2 gate dielectric with and without PMA treatment. For the sample with ALD-SiO_2/La-silicate IL, after PMA treatment, both the flat-band voltage and hysteresis are becoming smaller than that of SiC capacitor with SiO_2 gate dielectric only. The hysteresis has been reduced to 18mV, indicating a tremendous reduction of border traps. The flat-band voltage has also been reduced to 0.66V, which is almost ideal value for SiC capacitor with W electrode (ideal V_{fb}: 0.665V). The flat-band voltage shift to ideal value demonstrated that the further modification of electrical properties of ALD-SiO_2 has been achieved with ALD-SiO_2/La-silicate interface layer. It should also be noticed that the reduction of hysteresis become very slow after PMA for 1000s. Considering the oxidation of SiC

substrate occurs during the whole annealing process. A small ratio of C might be generated by oxidation of SiC which sustained the residual C concentration at the interface with a low value. And this kind of carbon-related traps near the interface could be the origin of the hysteresis value sustain around 18 mV for the capacitor with La-silicate/IL-SiO_2.

To investigate the interface properties of SiC capacitor with a different structure of gate dielectrics, conductance measurement has been conducted for each sample after annealing. Figure 7.4.3 illustrate the Gp/ω spectra at a surface potential of -0.05 eV for capacitors with a single ALD-SiO_2 layer, with ALD-SiO_2/La-silicate IL and with La-silicate interface layer only, respectively. Compared with *G*p/ω spectra for samples without PMA treatment, the peak value of *G*p/ω curves reduced after PMA treatment. For a sample with La-silicate interface layer, the value of *G*p/ω increased after PMA for 5000s, which is considered to be related to generation of low properties SiO_2 by oxidation of SiC substrate. For SiC capacitor with IL SiO_2/La-silicate, the maximum value of *G*p/ω reduced gradually with PMA duration increased. A D_{it} value of 2.6×10^{11} cm^{-2}/eV has been achieved for SiC capacitor with ALD-SiO_2/La-silicate IL after PMA treatment for 5000s, which is comparatively nice for deposited gate dielectrics on 4H-SiC.

Figure 7.4.4 shows the comparison of D_{it} for the 4H-SiC capacitor with ALD-SiO_2/La-silicate IL in this study and other deposited gate dielectrics from reported data. [7-11. 7-12, 1-38, 1-26]. As shown in the figure, SiC capacitor with ALD-SiO_2/La-silicate IL in this study shows minimum Dit value compared with other deposition dielectrics. The low value of D_{it} indicates that the interface properties have been improved significantly with a combination of using IL SiO_2/La-silicate gate dielectrics structure and PMA treatment method.

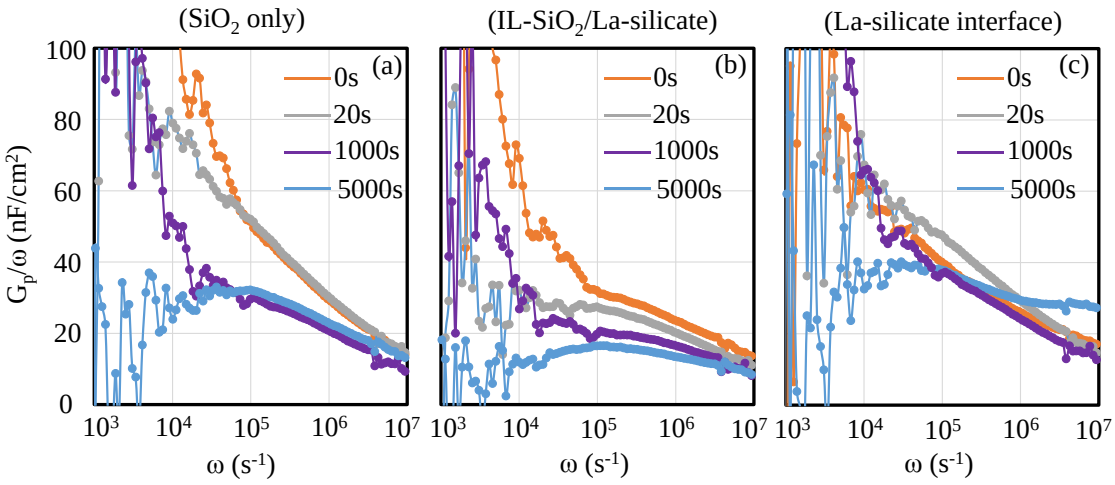

Figure 7.4.3 Gp/ω curves of capacitors with (a) single ALD-SiO_2 layer and (b) a La-silicate on an 8-nm-thick interface ALD-SiO_2 layer (c) La-silicate interface layer.

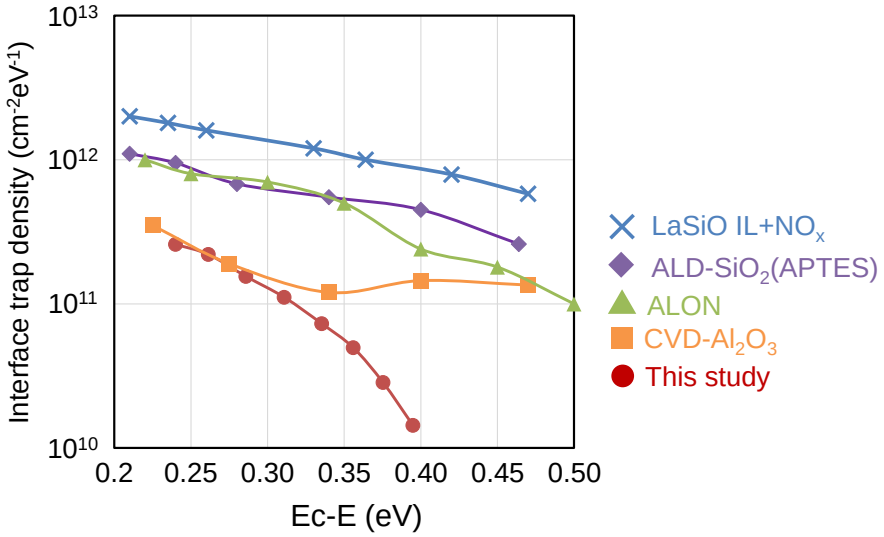

Figure 7.4.4 D_{it} of 4H-SiC capacitor with deposited gate dielectrics, from reported data of this study, CVD-Al_2O_3 [7-11], ALON [7-12], ALD-SiO_2 (APTES)[1-39], LaSiO&NO_x [1-26]

7.5 MOSFET with ALD-SiO_2/La-silicate IL

Figure 7.5.1 (a) shows the I_d-V_d characteristic of SiC-MOSFET with ALD-SiO_2/La-silicate IL. The drain current (I_d) curve increase with the gate voltage (V_g), and shows a parabola relationship with a drain voltage (V_{ds}), which indicted the MOSFET with ALD-SiO_2/La-silicate IL are functioning normally. For comparison, under low drain voltage condition, I_d-V_g characteristic of SiC-MOSFET with ALD-SiO_2/La-silicate IL and with La-silicate interface only has been shown in fig. 7.5.1 (b). The drain current was increased more than 1 time for MOSFET with interface SiO_2 compared for the sample with La-silicate interface only, which should be attributed to the increase of mobility of MOSFET channel by insertion of ALD-SiO_2 interface. Also, the hysteresis for drain current becoming smaller for the sample with the SiO_2 interface, indicating a reduction of border trap of gate dielectrics.

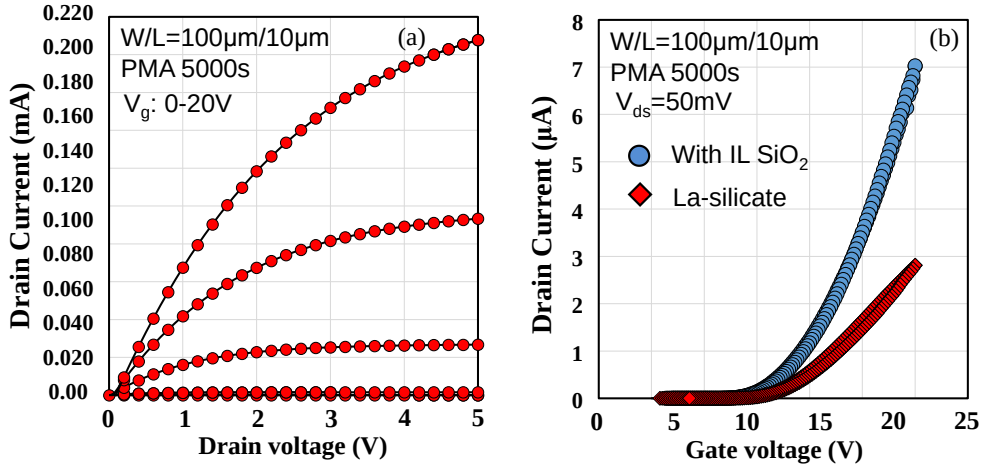

Figure 7.5.1 (a) I_d-V_d characteristics for the sample with IL-SiO_2/La-silicate (b) I_d-V_g characteristics at low drain voltage condition for the sample with IL-SiO_2 and with La-silicate only

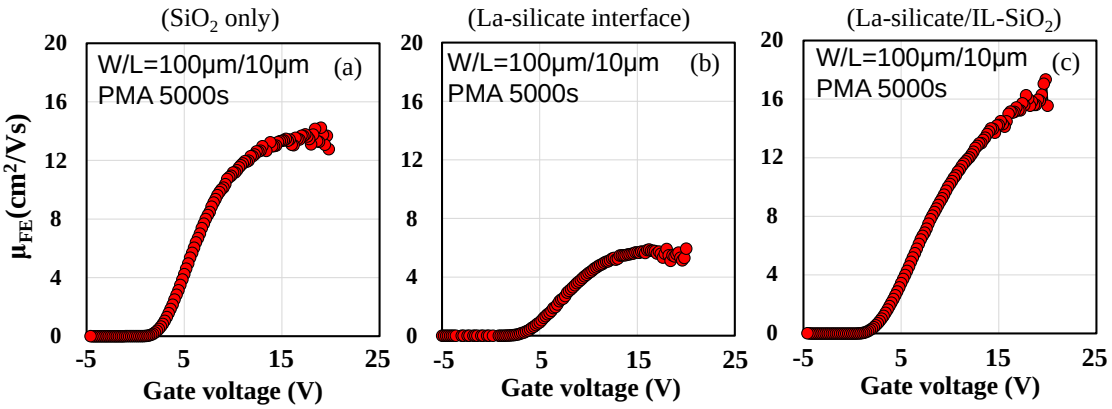

Figure 7.5.2 The field effect electron mobility of SiC-MOSFET (a) with SiO_2 only (b) with IL-SiO_2/La-silicate (c) with La-silicate interface

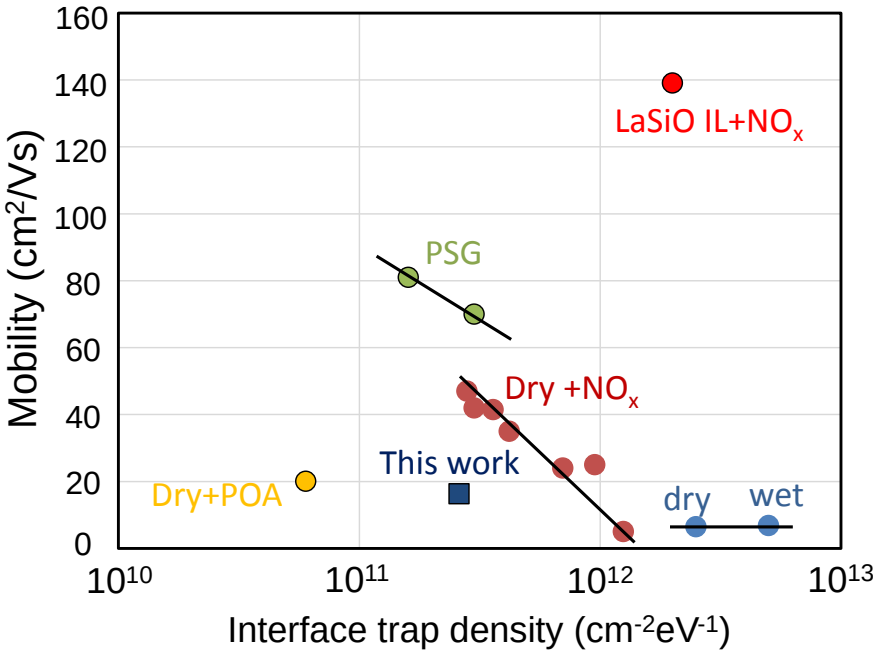

Figure 7.5.3 The relationship of D_{it} with mobility by different interface passivation method.

The electron mobility of SiC MOSFET with SiO_2 gate dielectric, and that with La-silicate/ALD-SiO_2 IL and also with La-silicate interface are investigated and the result is

shown in figure 7.5.2. For SiC MOSFET with SiO_2 gate dielectric only, an electron mobility of 14 cm^2/Vs has been achieved with PMA for 5000s, which is superior to most of SiC MOSFET using thermal grown SiO_2. For SiC MOSFET with La-silicate interface layer, as shown in fig. 7.5.2. (c), the mobility has been degraded to 6.5 cm^2/Vs, which should due to over-oxidation of SiC substrate. Since the quality of thermal formed SiO_2 is lower than that of ALD-SiO_2, a degradation of mobility can be expected by the introduction of low properties interface layer. Compared with the SiC MOSFET with La-silicate interface layer, SiC-MOSFET with ALD-SiO_2/La-silicate IL shows the highest electron mobility compared among the samples with SiO_2 and with La-silicate layers. A peak value of 16.3 cm^2/Vs has been achieved by the introduction of ALD-SiO_2/La-silicate IL structure. In contrast with SiC MOSFET with SiO_2 gate dielectric only, about 20% mobility improvement has been gained. Since PMA treatment has been proved to be capable for reduction of C residue density in gate dielectric layer, and La-silicate can magnify the elimination effect by generation of radical oxygen during the annealing, the further electrical properties improvement may can be attributed to the further reduction of carbon-related defects in the bulk and the interface of gate dielectrics.

Figure 7.5.3 shows the relationship of interface state density with mobility by different interface passivation method [1-25, 1-27, 1-28, 1-29, 7-13]. The blue square point shows the mobility and D_{it} of this study. As shown in the figure, although mobility has been reduced to 2.6×10^{11} cm^{-2}/eV and mobility is more than twice larger than thermally grown SiO_2 formed by dry or wet oxidation. The mobility is comparatively lower than that with NOx and PSG interface treatment. The further improvement by combination with other method is introduced in section 8.2.

7.6 Summary of chapter 7

In this chapter, the SiC capacitor and MOSFET with interface SiO_2/La-silicate layer has been discussed. For gate dielectrics with La-silicate interface, the generation of SiO_2 by enhanced oxidation of SiC substrate degraded the electrical properties by the poor quality of thermal grown SiO_2. By introducing an interface layer of SiO_2 between SiC substrate and La-silicate layer, the oxidation of SiC substrate has been suppressed significantly. Also, with the generation of radical oxygen to enhance the elimination of C residue in gate dielectrics by La-silicate, further electrical properties improvement has been achieved with a combination of PMA treatment and introducing of La-silicate layer. Finally, the electron mobility of 16.3 cm^2/Vs for SiC MOSFET with ALD-SiO_2/La-silicate IL layer has been achieved, which is superior to SiC MOSFET with ALD-SiO_2 gate dielectric only.

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Chapter 8

8.1 Conclusion of the thesis

8.2 Further Works for ALD-SiO_2 on SiC Power Devices

8.3 Reference

8.1 Conclusion of the thesis

Silicon carbide (SiC) is a promising candidate for next-generation power device semiconductor. The poor quality of thermal grown SiO_2/SiC interface and difficulty to form a uniform oxide layer on trench structure make it very important to find another method for the formation of gate dielectrics for SiC power devices. In this study, ALD-SiO_2 has been investigated for the formation of high-quality gate dielectrics on SiC MOS-devices.

Chapter 3 investigated the deposition properties of ALD-SiO_2. The precursor of Tris-dimethylamino-silane (TDMAS) and oxidant of O_2 remote plasma has been used in ALD process to form a SiO_2 layer. The roughness of ALD-SiO_2 is as small as 0.342nm for average, which is a unique advantage over thermal grown SiO_2 on SiC. The breakdown field of ALD-SiO_2 is about 8MV/cm, comparatively good for deposition SiO_2. However, high density of carbon concentration in the deposited SiO_2 film is one of the major concern for properties issue of ALD-SiO_2.

In chapter 4, the effect of annealing process on ALD-SiO_2 electrical properties has been discussed. Although large flat-band voltage and hysteresis voltage for capacitors with ALD-SiO_2 without annealing treatment indicate that large bulk and border trap density exist in the dielectric layer and dielectric/SiC interface, a significant properties improvement has been achieved for ALD-SiO_2 with thermal treatment. PDA process effectively improved the electrical properties of SiC MOS-capacitor with ALD-SiO_2, which should be attributed to the reduction of carbon-related defects during the annealing. PMA treatment can significantly reduce both bulk and interface defects in the ALD-SiO_2 gate dielectrics on SiC substrates. The out-diffusion of oxygen atoms in the gate electrode layer and in diffusion oxygen molecules from the environment is suggested to be the

source to form additional interface oxidation. SIMS analysis has demonstrated that carbon density in ALD-SiO_2 has been reduced significantly with PMA treatment, which may be the key for electrical properties improvement for SiC capacitor with ALD-SiO_2. A SiC MOSFET using ALD-SiO_2 shows an electron mobility of about 12cm^2/Vs with PDA and PMA treatment, which is comparatively good compared with SiC MOSFET using thermal grown SiO_2.

In chapter 5 the oxidation enhancement effect of La_2O_3 on SiC has been studied. The reaction of La_2O_3 with SiC substrate was investigated firstly by La_2O_3 capping annealing on SiC substrate in O_2 ambient. Formation of La-silicate has been confirmed by TEM image and XPS analysis. An enhanced oxidation rate that about two magnitudes higher than thermal oxidation of SiC substrate has also been found with La_2O_3 capping annealing. Generation of radical oxygen by La-silicate should be the reason for oxidation enhancement [5-5]. However, facet dependent oxidation of SiC substrate has still occurred and La-silicate agglomerated in the grown SiO_2 layer. This kind of oxidation fluctuation can be suppressed by thick ALD-SiO_2 layer capping and thin ALD-SiO_2 IL insertion. The reduction of oxidation reaction by suppression of oxygen molecule and radical oxygen diffusion is considered to be the main reason for improvement of interface layer uniformity. By physical analysis of ALD-SiO_2 with La_2O_3 capping after annealing, a reduction of residual C and diffusion of La atoms in ALD-SiO_2 has been observed, which is promising for electrical characteristics improvement for SiC MOS-device with La_2O_3 gate dielectric.

In chapter 6, electrical properties of SiC MOS-capacitor with ALD-SiO_2 and thin La-silicate IL gate dielectrics has been investigated. Conductance method revealed improvement in the D_{it} and the reduction in the surface potential fluctuation with the La-

silicate IL. Moreover, two orders of magnitude reduction in the N_{ot} in the ALD-SiO_2 layer adjacent to the La-silicate IL was confirmed. Physical analyses have revealed the reduction in carbon impurity concentration with La-silicate IL. Also, the incorporation of La atoms in the SiO_2 layer adjacent to the La-silicate IL. The origin of the improvements with La-silicate IL may be attributed to these contributions.

Finally, in chapter 7 the effect of La-silicate/ALD-SiO_2 IL on the electrical characteristics of 4H-SiC MOS structure was investigated. Although La-silicate can enhance the elimination of C residue in ALD-SiO_2 layer, an increase of SiC substrate oxidation occurred at the same time and degraded quality thermal grown SiO_2 layer has been formed, which on the contrary degrade electrical properties. La-silicate/ALD-SiO_2 IL structure successfully suppress the oxidation of SiC substrate. A reduction of flat-band voltage to ideal value after PMA 5000s has been found, revealing a significant reduction in bulk trap density for SiC capacitor with La-silicate/ALD-SiO_2 IL. Low hysteresis reduced to 20 mV and small *D*it of 2.6×10^{11} cm^{-2}/eV reveal tremendous improvement of interface properties. A high channel electron mobility of 16.3 cm^2/Vs has been achieved for SiC MOSFET with La-silicate/IL-SiO_2 layer, which is superior to SiC MOSFET with ALD-SiO_2 gate dielectric only.

8.2 Further Works for ALD-SiO_2 on SiC Power Devices

In this study, a deposited ALD-SiO_2 gate dielectric on SiC MOS devices has been investigated. Although comparably good properties of deposited gate dielectric by ALD-SiO_2 has been obtained. Further electrical properties improvement and process modification are still necessary for maximum utilization of the advantage of SiC material.

Among those influence parameter of channel mobility, the interface trap has a significant influence on MOSFET channel mobility, which can drastically reduce the electrons in the inversion layer, and trapped electrons act as a scattering center of the electrons [8-1]. Many reports shows that the interface trap near the conduction band edge (Ec) causes the low channel mobility in SiC MOSFETs [8-2, 8-3, 8-4]. Nitride oxide (NO, N_2O) gas annealing is an effective method which can effectively reduce interface trap density (Dit) near Ec [8-5]. Some other reports show that the mobility improvement by N_2O gas annealing is also achievable for deposited SiO_2 [8-6]. For ALD-SiO_2 gate dielectrics on SiC, the same effect can be predicted with utilize of NO, N_2O gas annealing.

Channel mobility improvement of SiC MOSFETs with ALD-SiO_2 may also be achieved by using alternative crystal faces of SiC. Hiroshi Yano et al. [8-7], reported 4H-SiC MOSFET fabricated on (11-20) face show a high channel mobility of 95.9 cm^2/Vs, which is 5 times higher than that fabricated on (0001) face with the same process. An even higher mobility of MOSFET fabricated on (11-20) face and (1-100) face about 119 cm^2/Vs has been reported with high temperature NO gas annealing [8-8]. A recent study shows that the improvement of mobility should be attributed to the significant reduction of D_{it} near the conduction band edge [8-9]. With a good understanding of the materials development, oxide reliability, and stability for these crystal faces, high mobility SiC MOSFET with ALD-SiO_2 can also be achieved using alternative crystal faces of SiC.

In this studies, the effect of thermal treatment like PMA and PDA on ALD-SiO_2 has been discussed. In particular, the oxygen molecule and radical oxygen played an important role in electrical properties improvement mechanism of ALD-SiO_2. However, the effect of other gas like N_2 and H_2 has seldom been discussed in this study. In fact, N_2 and H_2 can also passivate the SiO_2/SiC interface, H_2 has been reported to be able to passivate the D_{it} of 4H-SiC capacitor with thermal SiO_2 after annealing at 1000^{o}C for 30 min [1-18], and nitridation of the interface is achievable for SiC/SiO_2 by N_2 annealing at high temperature above 1350^{o}C [8-10]. The elucidation of interface passivation effect by other gas like N_2 and H_2 is also necessary.

For improving the electrical properties of ALD-SiO_2, PMA at 950^{o}C with a long duration of 5000 s has been used in this study. However, in the commercial manufacture, this kind of long annealing duration time may enormously increase the cost of manufactured devices. The key to electrical property improvements by PMA is to reduce the residual C by annealing, and in the meantime, create ideal reaction condition for SiC oxidation with low oxygen partial pressure. The relationship of SiC oxidation reaction with O_2 partial pressure and temperature is shown in figure 8.2.1. The red line in the figure shows the boundary of reaction generate CO gas and C residue. In this study, the oxygen partial pressure is suppressed by electrode capping layer in PMA. By control the electrode layer thickness and the gas ambient, the partial pressure of oxygen at the SiO_2/SiC interface can also be controlled. With suitable design of the deposition and annealing process, the oxygen pressure can be enlarged and the oxidation reaction condition can be controlled under the red line in the figure at the meantime, which means that the annealing duration time can be reduced with the well-designed process. Also, the carbon concentration in ALD-SiO_2 can be controlled with oxygen partial pressure and annealing

temperature. During PMA treatment, although low oxygen partial pressure annealing significantly reduced the carbon density in ALD-SiO_2, small ratio of SiC oxidation reaction still generate C residue during the annealing, which may prevent further reduction of C concentration in ALD-SiO_2 film. Since the oxidation reaction of SiC can be controlled by oxygen partial pressure and temperature (fig. 8.2.1), by further reduction of oxygen pressure and increase the annealing temperature, the reaction will more shift to the reaction that generates CO gas, which can further reduce the residual C concentration by preventing new C generation from SiC surface.

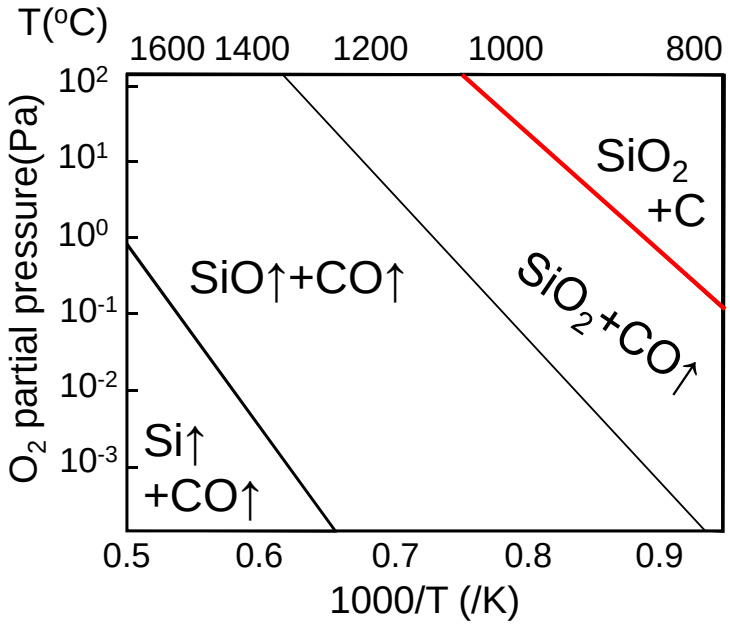

Figure 8.2.1 Oxygen partial pressure and the byproducts.

To achieve high reliability of SiC MOSFETs gate dielectric, high breakdown electric field and low leakage current is two key parameter for insulator reliability. Silicon oxynitride (SiON) is a promising candidate for gate dielectric layer on SiC with the

benefit of low leakage currents and high thermal stability [8-11]. A higher conduction band offset has been reported for SiON on SiC substrate [8-12], which could lead to more lower leakage current and reliability. For ALD-SiO_2 gate dielectric with La-silicate interface layer (IL), insertion of SiON IL is capable of improving dielectrics reliability. The dielectric structure is shown in figure 8.2.2. With SiON IL, reduction of leakage current can be achieved with higher band offset of SiON with SiC, Since introducing of nitrogen into silicon oxide is reported to effectively increase the dielectric constant [8-13], reduction of the electric field in dielectrics film when MOSFET at on-state can be achieved with same EOT of the insulator. Furthermore, SiON is reported to be effectively reducing the oxygen diffusion as a gas barrier [8-14], a significant reduction of SiC substrate oxidation by SiON interface layer can be predicted. The suppression of oxidation rate fluctuation on SiC can contribute to the reduction surface roughness of channel in SiC MOSFETs, which can improve the reliability of gate dielectrics on the other side.

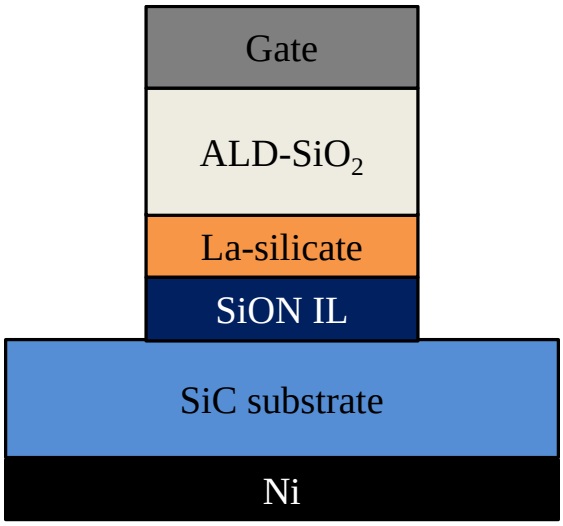

Figure 8.2.2 Schematic gate dielectrics stack with SiON interface layer.

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