T2R2 東京科学大学 リサーチリポジトリ
Science Tokyo Research Repository

論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Threshold voltage control technology in metal/high-k pFET consisting of high germanium content SiGe channel and fixed charge/oxygen vacancy control in gate stack
著者(和文)	山口晋平
Author(English)	Shimpei Yamaguchi
出典(和文)	学位:博士(工学), 学位授与機関:東京工業大学, 報告番号:甲第10986号, 授与年月日:2018年9月20日, 学位の種別:課程博士, 審査員:若林 整,筒井 一生,渡辺 正裕,大見 俊一郎,角嶋 邦之
Citation(English)	Degree:Doctor (Engineering), Conferring organization: Tokyo Institute of Technology, Report number:甲第10986号, Conferred date:2018/9/20, Degree Type:Course doctor, Examiner:,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	論文要旨
Type(English)	Summary

Powered by T2R2 (Science Tokyo Research Repository)

（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

専攻： Department of	物理電子システム創造　専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of	（　工学　）
学生氏名： Student's Name	山口　晋平	指導教員（主）： Academic Supervisor(main)		若林　整
		指導教員（副）： Academic Supervisor(sub)		

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

In advanced complementary metal oxide semiconductor (CMOS) technology, metal gate electrode and high-k gate dielectric has been introduced from 45nm node to overcome gate leakage issue with conventional silicon dioxide (SiO2) film and enable further scaling. One of the challenges associated with metal gate / high-k gate dielectric technology has been a control of threshold voltage of field effect transistor (FET), especially p-type FET (pFET). In gate-first integration where metal gate / high-k dielectric sees high thermal budget (activation anneal), effective work function of pFET was typically not high enough to provide sufficiently low threshold voltage (Vt). To achieve practical pFET Vt, two solutions have been proposed against this problem, one is gate-last or replacement metal gate (RMG) technology where gate stack is formed after high thermal anneal by replacing dummy poly silicon gate and SiO2 gate dielectric with metal gate and high-k gate dielectric. The metal gate and high-k dielectric stack doesn' t see high thermal budget, therefore effective work function can be kept high. Other solution is to implement silicon germanium (SiGe) in the channel of pFET. SiGe is typically deposited on Si substrate by epitaxy. Thanks to its higher valence band energy, pFET Vt is reduced without modifying gate stack itself.

In this thesis, SiGe channel device has been fabricated and its device characterization was studied. We investigated the impact from thermal budget on various device characteristics such as threshold voltage, carrier mobility, electrical oxide thickness (Tinv), and off-stage leakage current and found out that lower temperature process is key to achieve low Vt and high hole mobility by preserving high germanium content in the channel and also by keeping high bi-axial compressive strain in the channel. From this point of view, source / drain formed with in-situ boron doped epitaxial SiGe has been integrated with SiGe channel to eliminate the source / drain electrode by ion implantation and high temperature activation anneal. Furthermore, layout dependence on device performance of SiGe channel device has been investigated. In scaled channel width, we confirmed that carrier mobility is significantly enhanced thanks to the relaxation of compressive strain in transvers direction. TCAD analysis has been done and it could qualitatively explain the silicon data, although there is some mismatch in the magnitude of hole mobility improvement. We also investigated the interaction between SiGe channel and embedded SiGe stressor. It was found that even with same germanium concentration in the channel and source / drain, embedded SiGe stressor can provide similar hole mobility boost for SiGe channel to the one for Si channel. In case of SiGe channel devices, channel stress is released during cavity recess etching. Therefore, the net stress gain by embedded SiGe is less than the one for Si channel. However, piezo electric constant for SiGe under bi-axially compressive strain was found to be higher than unstrained Si and we found higher piezo electric constant compensates lower applied stress by embedded SiGe stressor and realizes similar hole mobility boost for SiGe channel. In the last section of SiGe channel, scalability of raised source drain and embedded source drain is discussed. Despite of the degraded drive current with raised source drain device compared to embedded source drain device, raised source drain devices showed superior short channel control over embedded source drain devices enabled shorter minimum gate length by 4nm, and thus smaller intrinsic delay was achieved with raised source drain devices.

In second part of this thesis, on the other hand, effective work function control technique using gate stack engineering is discussed. Even with gate-last or RMG integration scheme, a recent report highlighted effective work function lowering in scaled equivalent oxide thickness (EOT) region (EOT < 10 A). Therefore, it is still highly important to push the effective work function further towards valence band edge to achieve lower pFET Vt at scaled EOT region. Here we identified the high temperature annealing post metal/high-k stack is the key to realize low pFET Vt. We revealed two

kinds of phenomena are happening concurrently during this annealing. One is intermixed layer formation at the interface of TiN gate electrode and HfO2 dielectric. It was found that this layer contains negative fixed charge and reduces pFET Vt. The other is diffusion of oxygen from TiN gate electrode (which is originally oxidized during air exposure) toward HfO2/Si substrate. Some part of the diffused oxygen passivates and electrically neutralizes the pre-existing oxygen vacancies in the HfO2 dielectric. As oxygen vacancies are positively charged and increases pFET Vt, once they are neutralized, pFET Vt is reduced. The combination of these two phenomena enabled band edge effective work function at scaled EOT devices and also enabled wider coverage of transistor Vt option which is highly important in system-on-chip (SoC) application.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

注意：論文要旨は、東工大リサーチリポジトリ（T2R2）にてインターネット公表されますので、公表可能な範囲の内容で作成してください。
Attention: Thesis Summary will be published on Tokyo Tech Research Repository Website (T2R2).