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Article / Book Information

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種別(和文)	論文要旨
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（博士課程）
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論 文 要 旨

THESIS SUMMARY

専攻： Department of	Physical Electronics 専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of (Philosophy)
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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis outlines the trends and challenges of the Bluetooth Low-Energy (BLE) transceiver (TRX) design on deep sub-micron CMOS technology for the Internet-of-Things applications and describes a novel TRX architecture that utilized the DTC-based ultra-low-power (ULP) fractional-N digital phase-locked loop (DPLL) as a central component to minimize the power consumption of the TRX while maintaining the good sensitivity and blocker performances for the receiver (RX). The proposed novel digital-to-time converter (DTC) featuring good linearity and excellent power efficiency, which improves the jitter and spur performances of the DPLL, is also discussed. A proof-of-concept chip of the DTC-based ULP fractional-N DPLL confirms the linearity and power efficiency improvements of the proposed DTC. A proof-of-concept chip of the BLE TRX using the wide-bandwidth DTC-based ULP fractional-N DPLL confirms the merits of the proposed low-power TRX architecture.

Chapter 1 begins with an overview of the wireless standards for IoT applications and carries out the importance of the BLE standard. Chapter 1 also analyzed the design challenges for the BLE TRX design when considering the PHY specifications. The reciprocal mixing effect is explained in detail for the RX design, and the corresponded phase noise and spur performances of the DPLL are calculated and given. Chapter 2 introduces some fundamentals and essential features of both the analog-type fractional-N PLL and the digital-type fractional-N PLL. The focus of Chapter 2 is on the digital-type PLL toward advanced CMOS technology. Different DPLL architectures are introduced to show the trade-offs between the power, jitter, locking time, etc. for each DPLL architecture. Then, various time-to-digital converter (TDC) and DTC architectures are introduced and reviewed for their power, jitter, and linearity trade-offs. Finally, the phase noise of the LC oscillator is introduced for understanding the noise to the phase noise conversion mechanism. Chapter 3 presents the proposed ULP fractional-N DPLL, which achieves sub-mW operation, a worst-case fractional spur of -56 dBc, and a jitter-power FOM of -246 dB. A 1st-order DSM-based fractional-division controller is discussed and analyzed for demonstrating its potential to support the sub-mW operation for a DPLL with a good jitter performance. A 10-b isolated constant-slope DTC is proposed to demonstrate the linearity and power

efficiency improvements over the conventional DTC architectures. The gain-and-offset calibration of the time amplifier (TA) is introduced to help minimize the in-band phase noise degradation by both TA gain error and the TA offset. Finally, the whole fractional-N DPLL design is carried out and measured with the proposed techniques. The comparison with the state-of-the-art fractional-N DPLL is summarized for demonstrating the merits of using the proposed techniques. Chapter 4 introduces a BLE transceiver that utilized the proposed DPLL above as a central component. The embedded low-power wide-bandwidth fractional-N DPLL performs as 1) DPLL-based analog-to-digital converter (ADC) for the RX; 2) local oscillator (LO) for the RX; 3) phase and frequency synchronization for the RX; 4) direct frequency modulator for the TX. The multi-function of the DPLL minimizes the power consumption of the TRX. The wide-bandwidth DPLL supports the single-path demodulation method for reducing the conventional I/Q branches to only I channel in RX. Hence, the number of the required analog baseband circuits is reduced by half, which helps reduce the RX power consumption significantly. Besides, the dynamic range of the DPLL-based ADC is greatly enhanced by 18 dB thanks to the proposed DAC feedback structure. It substantially improves the sensitivity and blocker performances. Finally, the entire BLE TRX is introduced and evaluated, which achieved the recorded low power consumption when compared with other state-of-the-art BLE TXs/RXs.

Chapter 5 presents the conclusion and future directions of the thesis. Solutions for reducing the power consumption of the BLE TRX have been implemented and evaluated. The recorded power consumption of 2.3 mW for RX is achieved with a sensitivity of -94 dBm. The RX also satisfied all in-band and out-of-band interference requirements with enough margin. A 5.0-mW TX is achieved when delivering an output power of 0 dBm with an FSK error of only 1.89%. In Chapter 5, some potential directions for this study, such as improving the speed of DTC gain calibration, removing the DC quantity from the DPLL-based ADC, and improving the convergence speed of phase and frequency speed, are discussed and explained as well. The outcomes of this study could be of relevance for both the academic viewpoint and the industrial viewpoint.