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Authors	Tomoaki Oba, Takamasa Kawanago, Shunri Oda
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Tomoaki Oba
Takamasa Kawanago, Shunri Oda
QNERC and Dept. of EE., Tokyo Institute of Technology, 2-12-1-S9-12, Ookayama, Meguro-ku, 152-8550, Tokyo, Japan
oba.t.ae@m.titech.ac.jp

Gated Four-Probe Method for Evaluation of Electrical Characteristics in MoS_2 Field-Effect Transistors

Layered semiconductor of transition metal dichalcogenides (TMDC) has been considerable attention because of their various properties [1]. New classes of semiconductor materials motivate an investigation of carrier mobility and contact resistance in field-effect transistor configuration from the view point of both scientific interests and practical applications. This study describes the gated four-probe method to evaluate the relation between interfacial properties and channel mobility in MoS_2 FETs [2, 3].

Heavily-doped p^+-type Si wafer was subjected to SPM and 1% HF cleaning. Thermal SiO_2 was grown by dry oxidation at 1000 ^oC for 5 min. Subsequently, Al_2O_3 was deposited by ALD (TMA, H_2O, 300 ^oC) on SiO_2. Au (40 nm)/Ti (10 nm) was deposited by thermal evaporation and lift-off for source/drain contact and two potential probes. After removal of back side SiO_2 with BHF, Au (30 nm) / Ti (10 nm) for back gate contact was deposited on the back side of the substrate by thermal evaporation. Next, the substrate was subjected to oxygen plasma to form hydroxyl groups on the surface of Al_2O_3. Then, the substrate was immersed into 2-propanol containing 5 mM n-octadecylphosphonic acid (ODPA) for 4 hours at room temperature [4]. Annealing was conducted at 100 ^oC in N_2 for 30 min to stabilize ODPA. The gate dielectric consists of hybrid ODPA/Al_2O_3/SiO_2. Mechanically exfoliated MoS_2 were transferred to the substrate with the PDMS elastomer. Finally, devices were annealed in N_2 at 150 ^oC for 30 min to improve source/drain contact. The fabrication process and device structure are summarized in Fig. 1. Fig.2 shows microscope image of fabricated FET.

The channel mobility were evaluated with four-probe method based on the equations, as shown in Fig. 3. Fig. 4 shows the representative I_d-V_d characteristics of MoS_2 FET with gated four-probe method. The FET operation was observed with this four-probe configuration. Fig. 5 shows the representative I_d-V_g characteristics of MoS_2 FET without SAM. Hysteresis in clockwise direction was observed. On the other hand, formation of SAM can suppress the hysteresis in I_d-V_g characteristics as shown in Fig. 6. The channel potential was estimated during I_d-V_g measurement using internal two probes between source and drain contact. Fig. 7 shows the C-V characteristics of Si MOSCAP for SiO_2 and Al_2O_3/SiO_2 gate dielectric. The physical thickness of SiO_2 was 15.7 nm. The physical thickness of Al_2O_3 corresponds 14 nm when the dielectric constant of Al_2O_3 was assumed to be 8.5. Also, the physical thickness and dielectric constant of ODPA are 2.1 nm and 2.5 [4]. Consequently, the overall capacitance of ODPA/Al_2O_3/SiO_2 is 0.13 $\mu m/cm^2$. Fig. 8 shows V_g dependence of four-probe conductivity (σ). The channel mobility (μ_{4w}) was evaluated from the σ using the equation as shown in Fig. 3. The μ_{4w} with SAM is improved as high as 28 cm^2/Vs, while the μ_{4w} without SAM shows 19.7 cm^2/Vs. The interfacial properties is responsible for the channel mobility of MoS_2 FET

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[3] V. Podzorov et al. Appl. Phys. Lett., 84, 3301 (2004).
[4] T. Kawanago et al., Appl. Phys. Lett. 108, 041605 (2016).

Figures

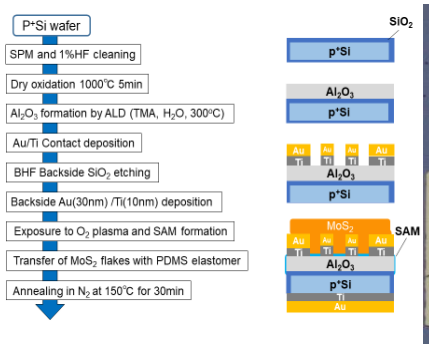

Figure 1: Fabrication process and device structure.

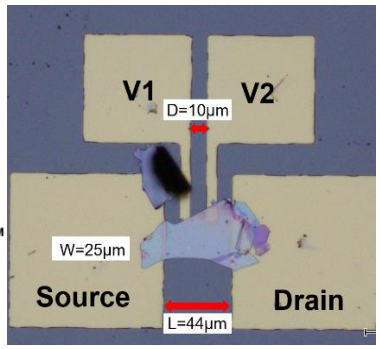

Figure 2: Microscope image of fabricated FET.

Channel Conductivity $\sigma = \frac{I_{SD}}{V_{4W}}$

Intrinsic electron mobility $\mu = \frac{D}{WC_i} \cdot \frac{d\sigma}{dV_G}$

Contact resistance $R_{contact} = \frac{V_{SD}}{I_{SD}} - \frac{L}{D} \cdot \frac{V_{4W}}{I_{SD}}$

D: distance between the voltage probes
C_i: capacitance of the gate dielectric
d: derivative operator

Figure 3: Equations to evaluate channel mobility & contact resistance with gated four-probe method.

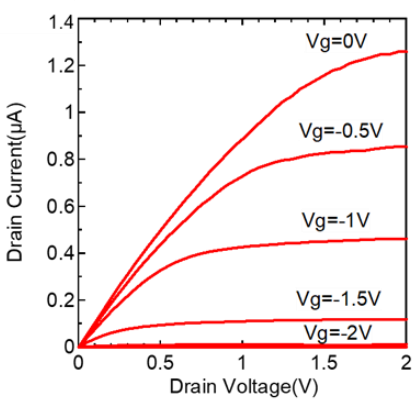

Figure 4: Representative I_d-V_d characteristics of MoS_2 FET with gated four-probe method.

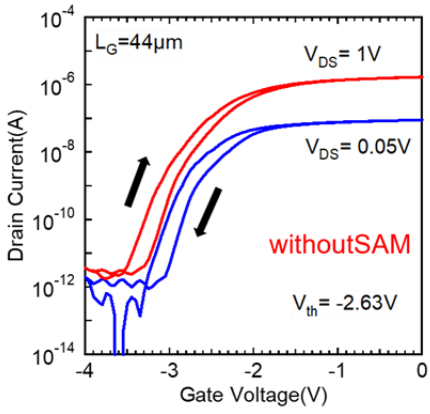

Figure 5: Bidirectional I_d-V_g characteristics of MoS_2 FET without SAM.

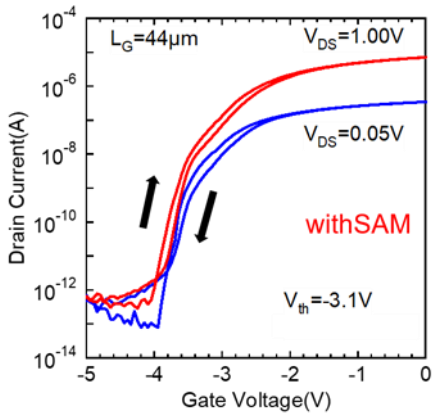

Figure 6: Bidirectional I_d-V_g characteristics of MoS_2 FET with SAM.

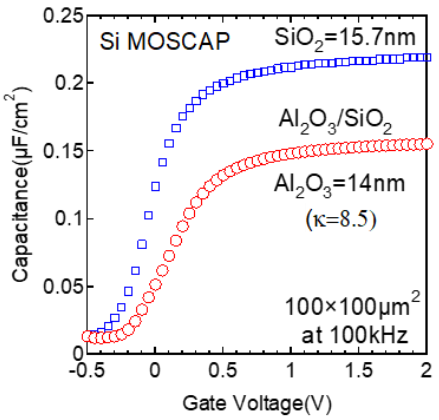

Figure 7: C-V characteristics of Si MOSCAP for SiO_2 and Al_2O_3/SiO_2 gate dielectric.

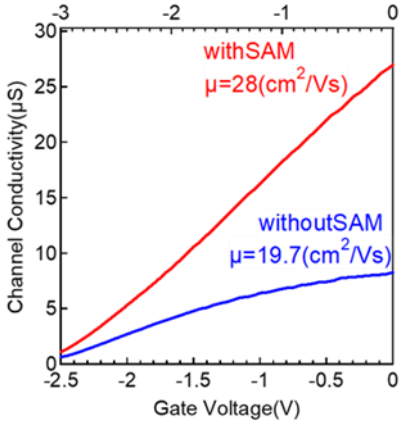

Figure 8: Impact of SAM on channel mobility estimated by four-probe method.