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Dissertation outline

Spin-valve effect in nanoscale Silicon spin-valve devices

Duong Dinh Hiep

The spin MOSFET is considered to be the building block of low-power-consumption electronic devices in the beyond CMOS era. However, there is no spin-MOSFET demonstrated so far, due to issues such as conductivity mismatch between ferromagnetic metal (FM) electrodes and semiconductor (SC) channels which causes the poor spin injection efficiency, and the loss of spin information in micro-long diffusive SC channels. As the consequence, the spin-valve ratio as well as the spin-dependent output voltage in FM / SC / FM spin-valve devices studied so far are very small. In this dissertation, the ballistic transport in nanoscale spin-valve devices is proposed as the solution to overcome those issues. This dissertation presents the experimental investigation of the spin transport in the nanoscale Si-based spin-valve devices with Fe electrodes, (Mg)/MgO/Ge tunnel barriers, and a 20 nm-long Si channel.

Firstly, investigation of spin transport in nanoscale Si spin-valve devices with the FM and tunnel barrier prepared by electron beam (EB) evaporation was described. A high magnetoresistance (MR) of 12 Ω corresponding to a MR ratio of 0.8 % and a large spin-dependent output voltage of 13 mV were achieved for a device with an MgO/Ge tunnel layer, which are among the highest values reported at that time. Systematic investigations of the bias voltage dependence, temperature dependence, and magnetic-field direction dependence of the MR indicate that the observed spin-valve effect is governed by the spin transport through the nanoscale Si channel. The spin-valve effect decreases with increasing temperature but remains observable up to 200 K.

Secondly, the spin transport in spin-valve devices fabricated by the molecular beam epitaxy (MBE) method was characterized. An enormous spin-valve effect with $|\Delta R|$ up to 57 kΩ, corresponding to $|\Delta R/R|$ = 3% was achieved. The author also observed the inverse spin-valve effect in these devices at low temperature and proposed the spin-blockade model of defect states in the MgO tunnel barrier as an explanation. A high spin-dependent output voltage of 20 mV was observed, which is among the highest values reported in lateral Si-based spin-valve devices at that time.

Thirdly, the author demonstrated two important roles of (quasi) ballistic transport in the nanoscale Si channels: (i) generation of spin-valve effect even when there is no barrier at room temperature, and (ii) suppress spin-flip scattering to achieve a higher spin-valve ratio at low temperature. Indeed, the observed spin-valve ratio of 3% is much larger than those observed in μm-long lateral Si channel devices reported so far. Nevertheless, the electron transport in the nanoscale devices may be quasi ballistic rather than fully ballistic, because the channel length (20 nm) is not much shorter than that of the mean free path of 20 ~ 40 nm for the studied n-type Si channels with an electron concentration of 10^{18} cm^{-3}. By further downsizing the Si channel length to sub-10 nm, fully ballistic transport and higher spin-valve signals can be achieved.

Fourthly, the MgO tunnel barrier thickness of spin-valve devices prepared by MBE was optimized to achieve a higher spin-dependent output voltage. In a device with MgO (1.5 nm) / Ge (1 nm) double layers grown by MBE, the author achieved a spin-dependent output voltage of 25 mV, which is the highest value reported so far.

Fifthly, the spin-valve ratio was improved by inserting an ultrathin Mg layer between the tunnel barrier MgO and the Fe electrodes to prevent the formation of a magnetically-dead layer at this interface. By optimizing the Mg buffer layer thickness (1 nm Mg) and MgO tunnel barrier thickness (3.5 nm MgO), the MR ratio has been improved up to -3.6 %. This value is the highest reported so far in lateral spin-valve devices.

The results in this dissertation give better understanding and control of the spin transport in nanoscale Si spin-valve devices, and are helpful for improving the performance of Si-based spin MOSFET.