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Study on self - sensing system of semiconductor array matrix

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February 06, 2019

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(Subtitle) A sensing system of drive TFT in two-TFTs/one-capacitor pixel circuit of LTPS AM-OLED display for producing high-uniformity images

Abstract

A self-sensing system was developed for semiconductor array matrices, in which semiconductor elements such as transistors and diodes are arranged in an array. A semiconductor array matrix can be classified as an active or passive matrix array.

In Part I, the self-sensing system was applied to an active-matrix organic light emitting diode (AM-OLED) display as an example of an active matrix array. Peripheral circuits and transistors in an active matrix array control an operating point of a drive thin film transistor (TFT) on the AM-OLED. After that, each pixel's V_{th} of the drive TFT on the AM-OLED was sensed as a manufacturing parameter. Highly uniform pictures were found to be produced by the compensation of the sensed variations in V_{th}.

In Part II, the self-sensing system was applied to a photovoltaic (PV) system as an example of a passive matrix array. First, environmental parameters were estimated using a circuit model, device model, and sensed data. The environmental parameters indicated an operating point on the current–voltage (I-V) curve, such as operating temperature, of the PV system. Next, faults and degradation were calculated as the manufacturing parameters using the estimated environmental parameters. The faults and degradation of the PV system were found to be highly precisely estimated without additional sensors.

Finally, as an examination of future work, the implementation of machine learning is discussed for improving sensing accuracy and expanding application to array matrices that they do not consist of semiconductors.

Acknowledgements

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Chapter 1

Introduction

1.1 Overview

A self-sensing system was developed for semiconductor array matrices, in which semiconductor elements such as transistors and diodes are arranged in an array. Semiconductor array matrices can be classified as active or passive matrix arrays.

The concept of the developed self-sensing system for semiconductor array matrices is shown in Fig. 1.1. The minimal unit of a semiconductor matrix is called a cell, and a unit in which these cells are arranged in an array is called a cell array.

In an active array matrix, a row decoder and a column decoder are equipped on the semiconductor array matrix, and the cell to be sensed is selected by these decoders. Here, the data of the selected cell is detected using a driver with as few configurations as possible. In a passive array matrix, it is common for a driver to be installed to operate the cell array. Therefore, additional sensors and drivers are not required.

In an active array matrix, peripheral circuits and transistors control

an operating point on the current–voltage (I-V) curve before the manufacturing parameters are calculated. In contrast, in a passive array matrix, environmental parameters that indicate an operating point on the I-V curve, such as operating temperature, of the array matrix are estimated using a circuit model, device model, and sensed data.

The self-sensing system visualizes the V_{th} of the transistor, the faults, and the state of degradation of a cell or cell array. This means that the performance of a semiconductor array matrix as a circuit and device can be measured. In this introduction, we explain why we focus on semiconductor array matrices and the significance of applying the self-sensing system to active and passive array matrices.
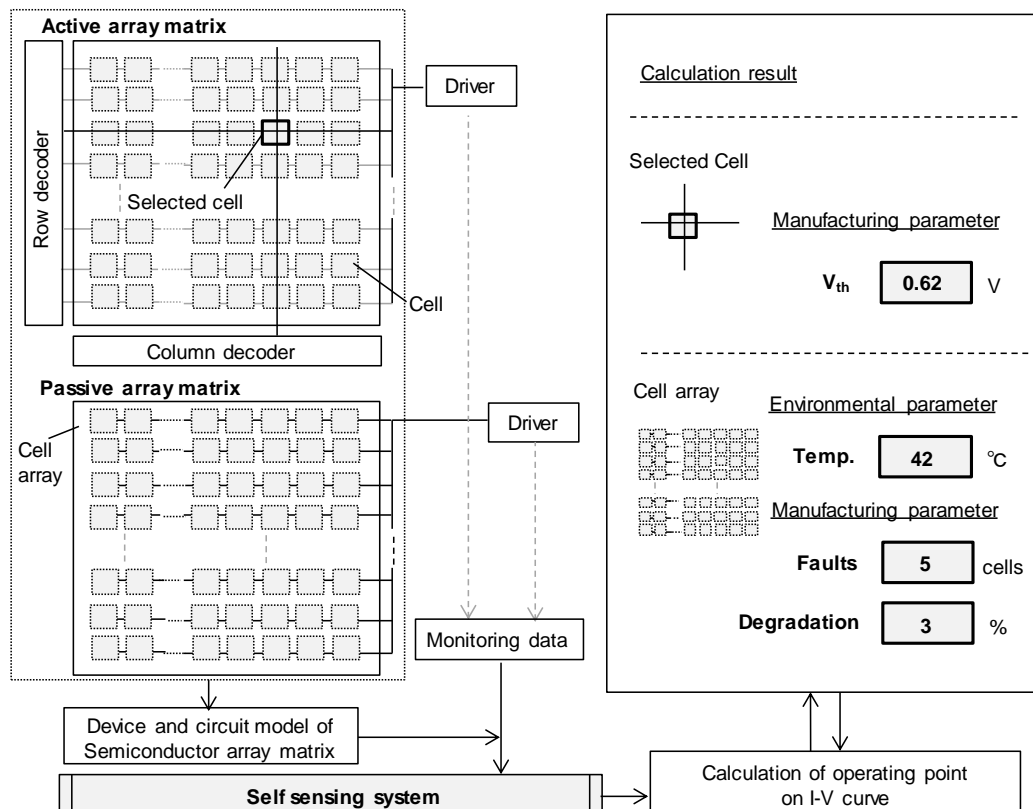
Figure 1.1. Concept of self-sensing system of semiconductor array matrix

1.2 Semiconductor array matrix

Semiconductor array matrices are a key component in the progress of information society. They have been important in all fields of electronic industry including memory, display, and image sensors for over 50 years [1–5]. Recently, in the field of electric power systems, power devices and photovoltaic (PV) cells, which have many manufacturing techniques in common with electronic systems, are expected to become key components of the environmental society that the UN's Sustainable Development Goals (SDGs) aim for [6–7].

1.2.1 Active array matrix

From the viewpoint of using chip area as efficiently as possible, the production of memory, display, and image sensors is basically equivalent to that of a cell array, a row decoder, a column decoder, and an input/output interface circuit, as shown in Fig. 1.2 [2][5][8]. A cell array consists of cells arranged in a two-dimensional matrix. A switch is built in each cell. The reading and writing of data are executed in each cell. A cell existing at the intersection of the N line of a row decoder and M line of a column decoder are selected among the cell array.

As shown in Fig. 1.3, each cell for memory, display, and image sensors is added to the transistor for high response and fine control. In this paper, a system equipped with an array matrix possessing a cell with a transistor, as mentioned above, is defined as an active array matrix.
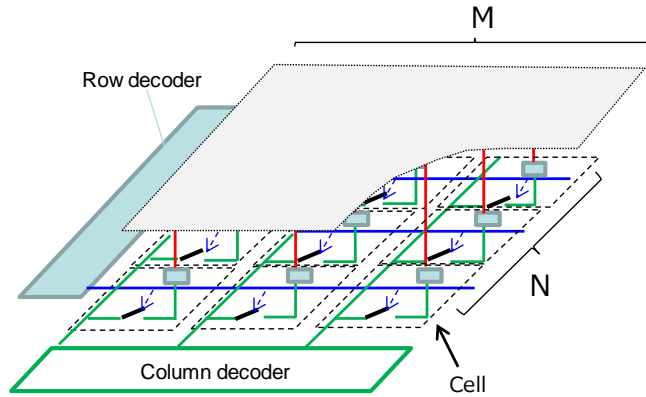
Figure 1.2. Basic configuration of active array matrix

(Memory, Display and Image sensor)
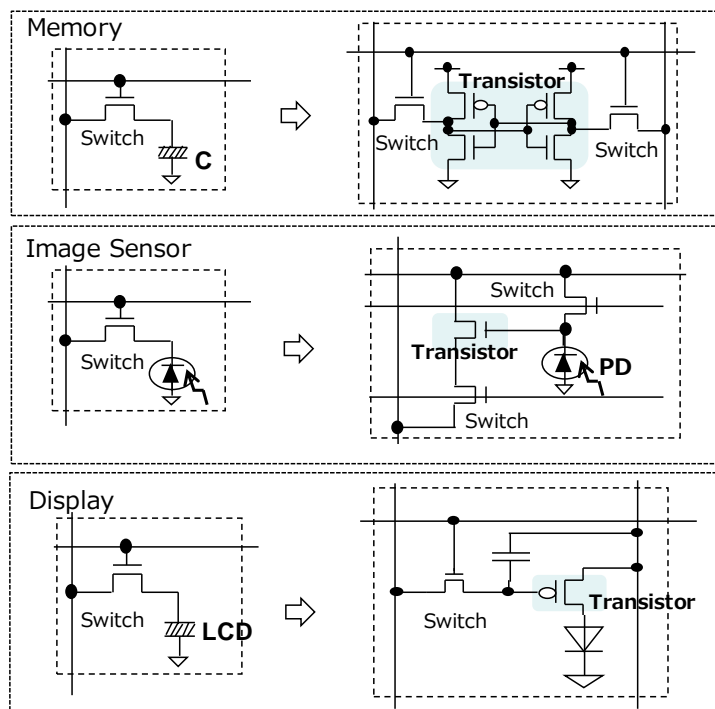
Figure 1.3. Cell to which transistor is added (Active array matrix)

In active array matrices, the miniaturization of cells has been advanced with the development of lithographic technology for transferring a layout pattern created from circuit design data onto a silicon wafer. As a result of this miniaturization, the minimal feature size of memory has evolved from a µm order in the 1970s to a 7-nm order in 2018 [9]. Regarding display, cell arrays consisted of hundreds of thousands of cells (pixels) in the 2000s [10]. In 2019, a cell array consists of millions of cells; this is the standard type of cell array [11]. The miniaturization of cells in array matrices has made it possible to increase the capacity and resolution of electronic systems, and it has advanced the electronics market.

1.2.2 Passive array matrix

The main element of a cell in a PV system, passive-type displays, and other such systems is a diode, shown in Fig. 1.4. A cell array is controlled by a driver, as shown in Fig. 1.5. The anode and cathode of each cell are connected to a driver. Many cells can be arranged in a limited area by making a driver into one chip using a time-sharing control technique, capacity enlargement and wafer-scale integration.
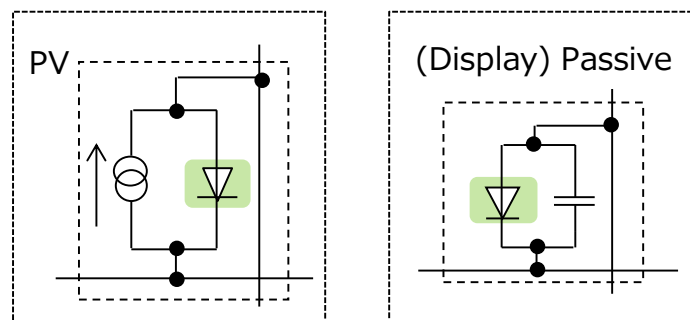
Figure 1.4. Cell of passive array matrix
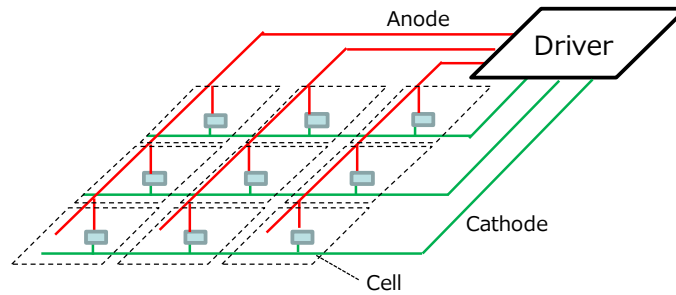
Figure 1.5. Basic configuration of a passive array matrix

(PV, Display (passive type))

The energy efficiency of crystalline silicon PV cells and thin film solar cells has improved [12], and PV cells are a promising power source for renewable energy, along with wind power generation. (Lithium-ion battery (LIB) cells are promising as electricity storage devices because of improvement in energy density [13]. Another type of storage system also consists of LIB cells arranged in an array, although LIB cells are not semiconductor devices.)

Placing as many of these cells (PV and LIB cells) as possible on a limited amount of land results in high energy-efficiency. The way to achieve the best efficiency with respect to area is to place these cells in an array. Figure 1.6 shows the cell arrays in a PV and storage system [14–15]. A plurality of cells connected in a series is called a module; a plurality of modules connected in series is called a string. A plurality of strings connected in parallel is a cell array. A cell array is connected to an inverter. A cell array's current data and voltage data measured in each inverter are collected and sent to a monitoring system using a connection such as Ethernet.

Arranging a cell array as shown in Fig. 1.6 secures high energy-efficiency relative to area, and a large-scale power or storage system can be made even on limited land. For example, an 82-MW PV power plant was made by efficiently laying approximately 341,040 PV modules (20,462,400 cells) on 105-hectare land [16].

Considering that an inverter is treated as a driver, and multiple anode and cathode lines are bundled to the inverter, it is the same as the configuration in Fig. 1.5. In this paper, an array matrix possessing a cell in which the main element is a diode is defined as a passive array matrix.
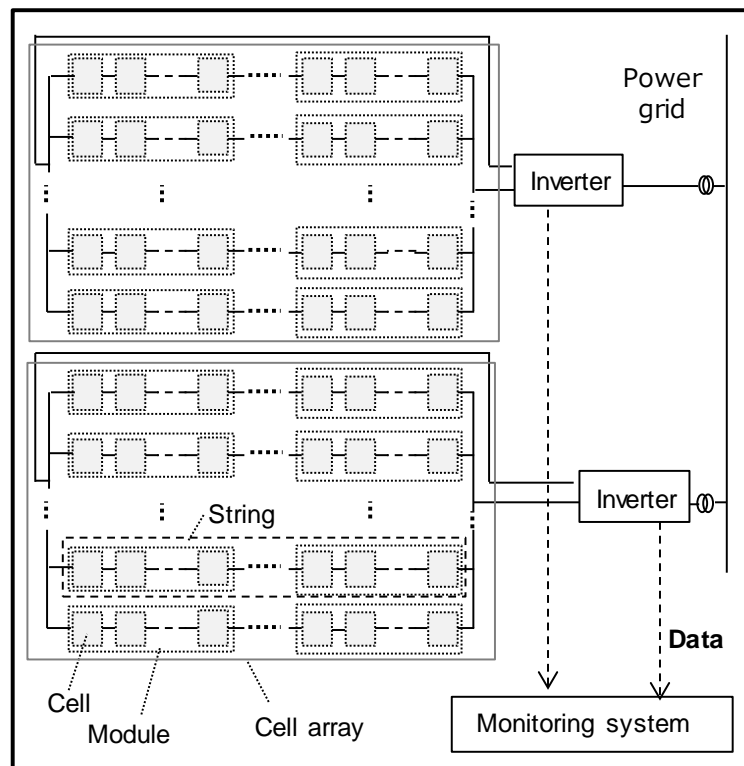
Figure 1.6. Basic configuration of PV system and storage system

1.3 Issue of a semiconductor array matrix

A significant problem for semiconductor array matrices is that the specific and critical performance of an array matrix as a whole is affected by the lowest-performance cell among numerous cells. For example, in the case of display, black spots, blob mura, and around gap mura, shown in Fig. 1.7, occur if there are cell defects. If there are some black spots or mura, even if other hundreds of thousands or millions of cells are normal, the product is judged to be commercially unacceptable [17].
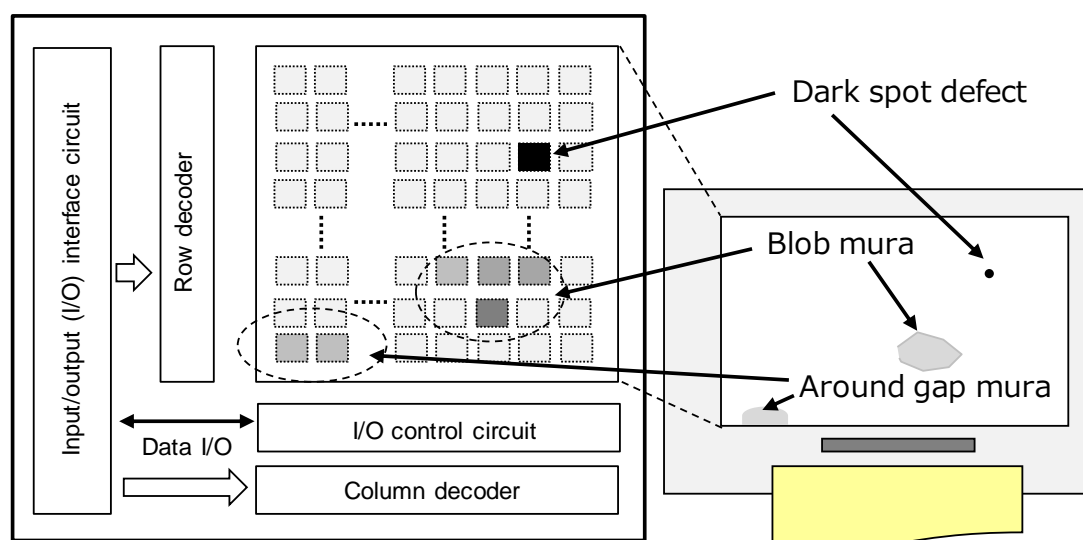
Figure 1.7. Black spot (cell defect), blob mura and around gap mura on display device (Example of performance degradation of array device as a whole influenced by the lowest performance cell)

In the case of a PV system, if one cell of tens or hundreds of thousands of modules is faulty and is left for a long time, a DC ground fault, shown in Fig. 1.8, may occur [18]. The inverter stops when detecting a ground fault. As a result, large power-loss occurs, and the PV system does not function as a power plant.
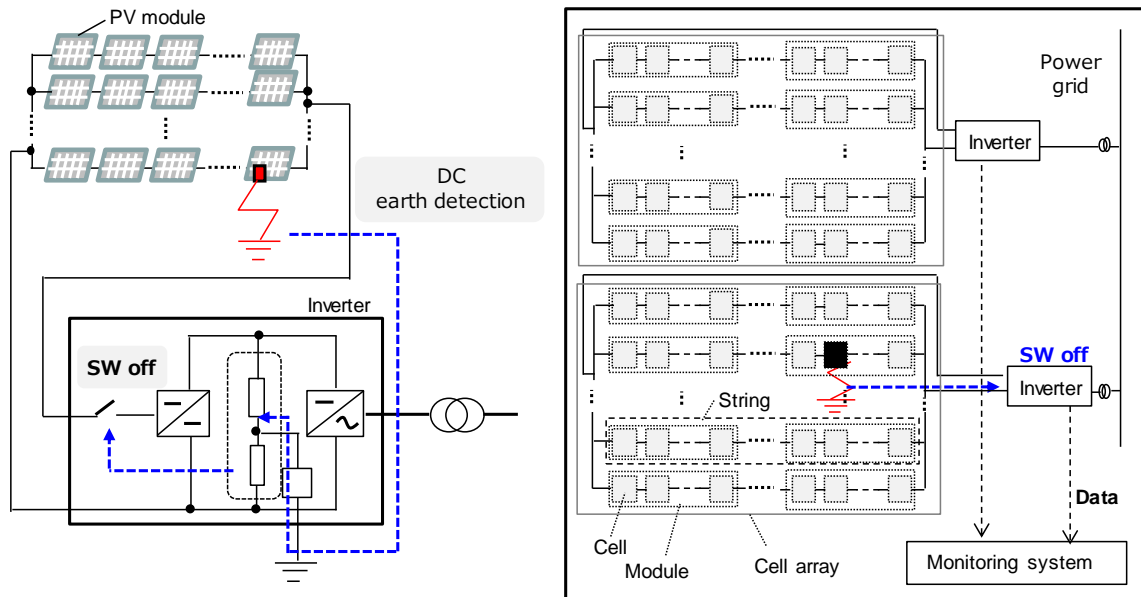
Figure 1.8. DC ground fault and large power loss of PV system
(Example of performance loss of array device as a whole influenced by the lowest performance cell)

In the production of image sensors, there is a method in which point defects are detected, and the information of neighboring normal cells is diverted as the address of the defective cell [19]. In the case of memory, defect detection such as that by parity check is executed [20]. The method of detecting defects in image sensors also establishes the erroneous locations and changes them into the nearest values. In the manufacturing process of displays, methods for detecting faulty transistors among all pixels on display have been proposed [21]. However, these methods are digital judgment. This means that mura, as shown in Fig. 1.7, cannot be detected, although black spot defects can be. Also, it is a same problem for sensing in PV systems, as shown in Fig. 1.8, because it means that small losses in the early stage caused by faults and degradation of a cell or a cell array cannot be detected until a

DC ground fault occurs, and the inverter stops.

In a passive array matrix, additional sensors may be equipped to modules or strings [30–31]. Taking a PV system as an example, it is very difficult to distinguish the state of the system until a significant change occurs in the sensing results of a plurality of modules (strings) because irradiation and temperature fluctuate, and their fluctuation is not uniform in a large site. Further, the failure rate of sensors may be higher than that of PV modules or strings, and the PV system may stop functioning due to sensor failure. This means that countermeasures that require additional measurement elements are not preferable.

Here, we focused on cell characteristic dispersion, which is the cause of blob mura and around gap mura. The best-known countermeasures against cell characteristic dispersion of displays and image sensors are circuit topologies, such as differential-pairing and usual current-mirror circuits [2][22–24], as shown in Fig. 1.9.

(a) Display   (b) Image sensor
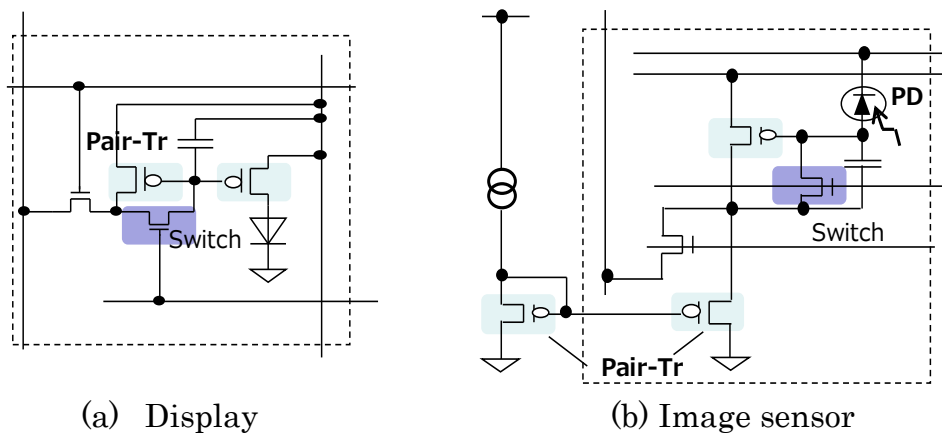
Figure 1.9. Circuit topologies for countermeasure against
cell-characteristic dispersion of display and image sensor

However, in low-temperature polysilicon (LTPS) and silicon semiconductor devices with a feature size smaller than 90 nm, circuit topologies composed of pair technologies are more complex and may not be effective [25–26]. This ineffectiveness is caused by low linearity or large characteristic variation in the transistors manufactured by these processes [27–29]. Further, as area allocated to one cell becomes smaller and smaller, countermeasures using circuit topologies that require additional elements in a cell or a cell array are inappropriate.

As described above, a major problem for semiconductor array matrices is that there is no means for effectively sensing their performance and the degradation of that performance. Therefore, our purpose is to develop a self-sensing system for cells and cell arrays in semiconductor array matrices.

1.4 Self-sensing system of semiconductor array matrix

Conventionally, additional sensors and circuits are added to each cell or each module of a semiconductor array matrix to monitor and improve performance. However, these countermeasures not only reduce the margin of cell area but also may have defects occur in the additional sensors and circuits themselves.

The purpose of the developed self-sensing system is to detect the characteristics of a semiconductor array without requiring additional sensors or with the minimal number of sensors and to improve the performance of the semiconductor array matrix itself using the detected data.

1.4.1 Block diagram of active array matrix

A block diagram of the self-sensing system for an active array matrix is shown in Fig. 1.10. First, a driver (for example, the current source or voltage source) is added to a semiconductor array device. If a driver is, for example, the current source, the voltage of a cell selected by a row decoder and column decoder is detected while applying a constant current from the current source. This detected data is defined as monitoring data.

Next, the cell's operating point on the I-V curve is controlled. Then, the manufacturing parameters (for example, Vth of the transistor) are calculated by applying the monitoring data to the device or circuit model. Finally, the calculated manufacturing parameters are transferred to the input/output interface circuit, and compensation, such as suppressing the manufacturing parameter's dispersion, is conducted. This compensation can improve the performance of a semiconductor array device.
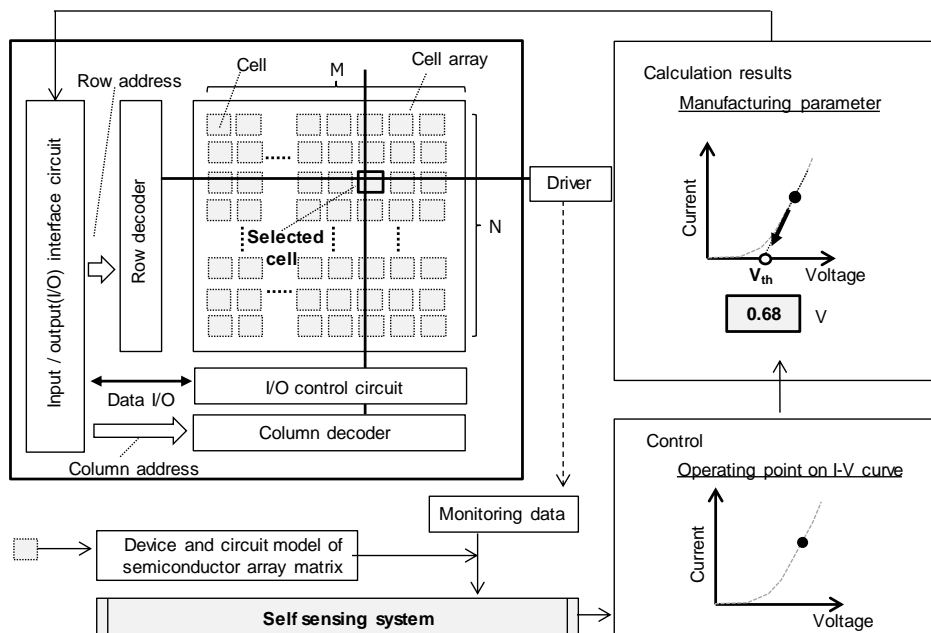
Figure 1.10. Block diagram of self-sensing system of an active array matrix

1.4.2 Block diagram of passive array matrix

A block diagram of the self-sensing system for a passive array matrix is shown in Fig. 1.11. In a passive array matrix, it is common for a measuring device such as a controller of an inverter (driver) to already be installed. Therefore, extra sensors are not installed.

The characteristics of a passive array matrix greatly fluctuate due to environmental fluctuations such as those in temperature. For example, the main element of a PV cell is a diode, and it cannot be controlled from the gate of the transistor like that of an active array matrix can. Therefore, first, calculation is performed using monitoring data and device and circuit model estimates in which a cell or cell array is operating on the I-V curve. Next, environmental parameters such as the cell's operating temperature are calculated by applying the operating point to the device and circuit models of the semiconductor array matrix at 298 K.

After that, the manufacturing parameters are estimated. If the estimated manufacturing parameters are below those of conventional dispersion, it may be determined that there are faulty cells. This makes it possible to sense small changes in a cell or cell array without requiring additional sensors.
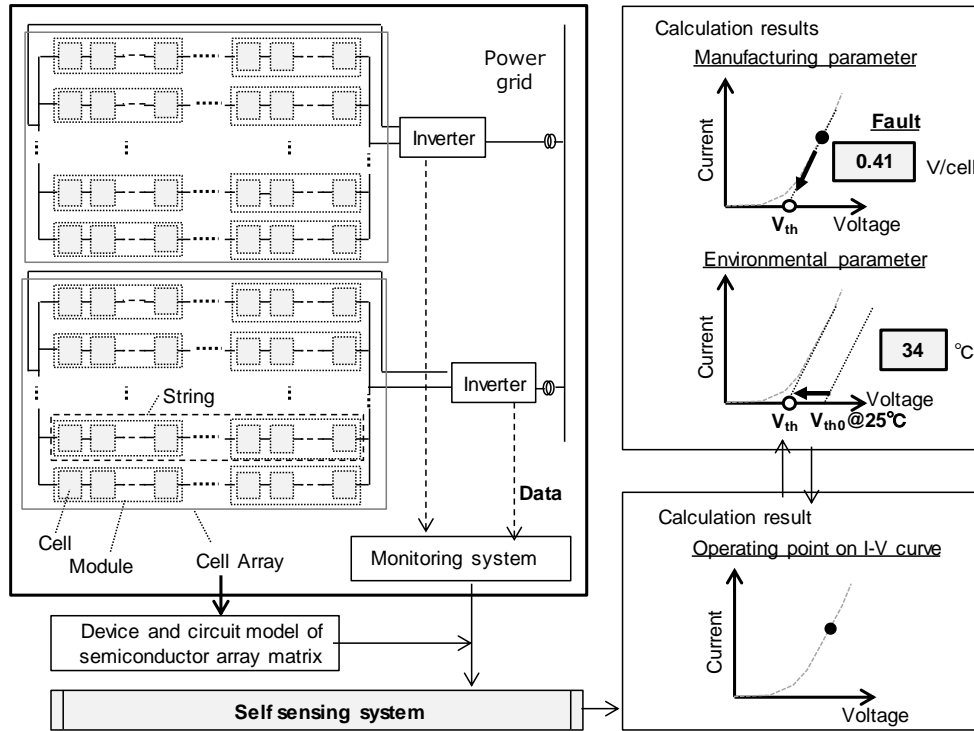
Figure 1.11. Block diagram of self-sensing system of a passive array matrix

1.5   Contents in this paper

In this paper, the self-sensing systems for semiconductor array matrices, as shown in Figs. 1.1, 1.10, and 1.11, were applied to actual commercial systems, and their effects were demonstrated. The structure of this paper is shown in Fig. 1.12, and an outline of Chapters 2 to 11 is given.

In Chapters 2, 3, 4, and 5, forming Part I, the self-sensing system is applied to an active-matrix organic light emitting diode (AM-OLED) display, an active array matrix. In Chapter 2, we describe how the performance of an AM-OLED display is significantly influenced by the dispersion V_{th} of the thin film transistor (TFT), which is the manufacturing parameter. In addition, the

technical trend for the compensation of the dispersion V_{th} is explained. In Chapter 3, the method for detecting V_{th} of the TFT for each cell is described. This method was developed by applying the self-sensing system to an AM-OLED display. In Chapter 4, the detection results for V_{th} are introduced. In Chapter 5, a summary of the self-sensing method applied to an AM-OLED display and this method's effectiveness are described.

In Chapters 6, 7, 8, and 9, forming Part II, we describe how the self-sensing system was applied to a PV system, a passive array matrix. The power generated by a PV system is influenced by the fluctuation of environmental parameters such as temperature and irradiation. In Chapter 6, the conventional methods for evaluating the performance of a PV system in a fluctuating environment are introduced. In Chapter 7, we explain the method of applying PV modeling to the self-sensing system. This method can estimate the irradiation and temperature of PV cells, faults, and degradation in semiconductor array devices without requiring additional sensors. In Chapter 8, we give the self-sensing system's detection results for faults and degradation in a PV array. In Chapter 9, we summarize the self-sensing method applied to a PV system and this method's effectiveness.

In Chapter 10, as a consideration of future work, the implementation of machine learning is discussed for further accuracy improvement and expansion of application to array matrices in which cells are not semiconductors. Finally, in Chapter 11, a summary of this paper is given.
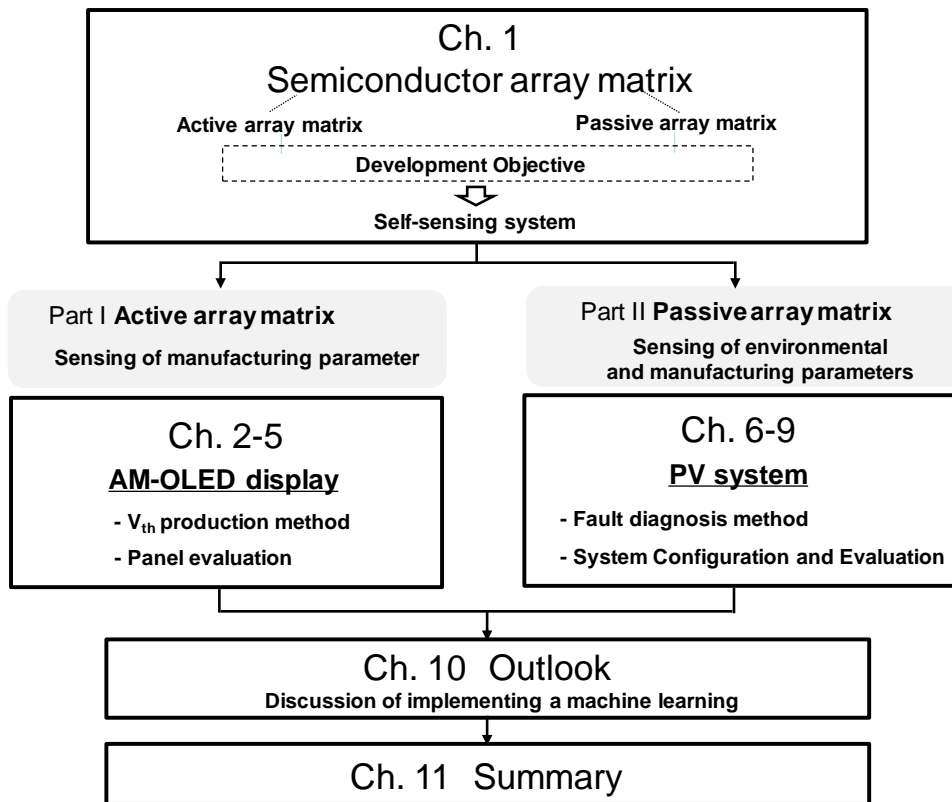
Figure 1.12. Structure of this paper and contents of each chapter

Part I

Application of a self-sensing system

of an active array matrix

(Subtitle)

A sensing system of drive TFT in two-TFTs/one-

capacitor pixel circuit of LTPS AM-OLED display

for producing high-uniformity images

Chapter 2

Introduction of AM-OLED

A self-sensing system was applied to an AM-OLED display. The image quality of an AM-OLED display is critically influenced by manufacturing parameter of each cell. Here, a cell is expressed as a pixel, and the manufacturing parameter to be sensed is the threshold value V_{th} of the TFT.

AM-OLED displays are known to achieve high performance—namely, fast response, wide viewing angle, and high contrast ratio—as a simple, thin structure. AM-OLEDs are therefore a promising candidate for the next-generation display for mobile applications.

LTPS TFTs are useful for driving OLEDs and liquid crystal displays (LCDs) because of their high mobility. An area that circuit elements can be located is restricted in the high-resolution display for mobile applications. As shown in Fig. 2.1, the pixel of LCD display is composed by only one TFT, one scan line and one signal line.
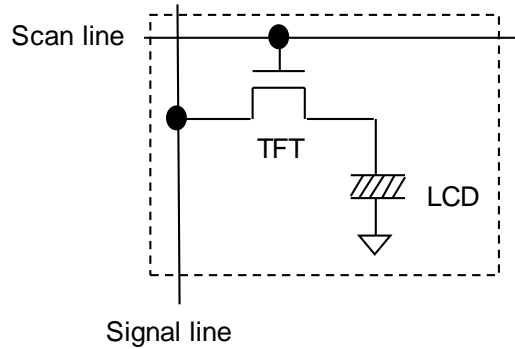
Figure 2.1 Pixel circuit of LCD display

The simplest pixel circuit of AM-OLED displays is composed of two LTPS TFTs (a drive TFT (Q1) and an address TFT(SW)), one capacitor (C), one scan line, one signal line and power live (V_{dd}) as shown in Fig. 2.2 [32]. This circuit is called "2Tr1C" configuration. A TFT of LCD display in Fig 2.1 is a switch for sending a voltage to LCD via signal line. On the other hand, a drive TFT Q1 of AM-OLED display in Fig. 2.2 generates current and drives an OLED for emitting light. Namely, a drive TFT Q1 is operating in saturation region of TFT's IV characteristic when OLED is emitting light. Therefore, inter-pixel non-uniformity caused by threshold-voltage (V_{th}) variation and hysteresis of the drive TFT Q1 is an important issue concerning high-quality AM-OLED displays.
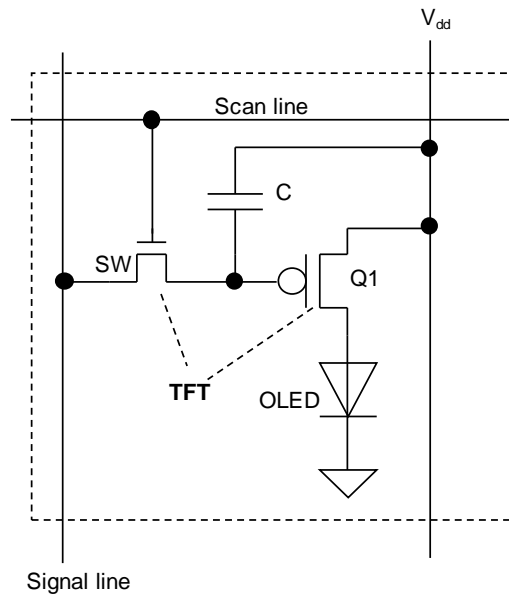
Figure 2.2 The simplest pixel circuit of AM-OLED display

Concerning this V_{th} variation, many kinds of pixel circuits have been reported. These circuits are classified to the current programmed pixel circuits [23-24] [33-34] and voltage programmed pixel circuits [35-38].

The current programmed pixel circuits are the circuit topologies composed by the pair technologies such as a current mirror as described in Chapter 1. The circuit topologies described in paper [23-24] cannot compensate sufficiently V_{th} variation. The circuit topology described in the paper [35-38] achieved compensation of V_{th} variation by storing V_{th} of the drive TFT to the capacity in the pixel circuit without the pair technology. However, circuit topology is not suitable for a high-resolution display because the parasitic capacitance must be charged before program operation and this charging takes a long time.

In high-resolution displays, many pixels should be programmed within one frame. The voltage-programmed pixel circuits are suitable for high-resolution images because the programming speed of data signal is high. As an example of the voltage programmed pixel circuit, the operation of the pixel circuit simplified to the extent of 3 TFTs, 2 scan lines, 1 signal line and 1 capacitance by the authors is explained as below. The method using this pixel circuit is called advanced-clamped-inverter (ACI) driving [36-38].

A pixel circuit is shown in Fig 2.3. It is composed of 2 TFT switches (SW1 and SW1), drive TFT (Q1), 1 capacitor, 2 scan lines (RES and ILM), and 1 signal line and can compensate TFT characteristic variation. Figure 2.4 is a diagram illustrating an entire structure of AM-OLED using the pixel circuit in Fig. 2.3. As shown in Fig. 2.4, pluralities of pixel circuits (Pixel (x0, y0), Pixel (x1, y0), Pixel(x0, y1) and Pixel(x1, y1)) are located in an array. The row decoder in Fig. 1.1, 1.2 and 1.10 corresponds to the scan circuit in Fig. 2.4. Similarly, the column decoder corresponds to the data signal driver.

Data signal lines (V2_x0, V2_x1), scan lines for reset (RES), scan lines for lighting (ILM) and a power supply line V_{dd} are provided for each pixel. The signals of scan lines for reset (RES) are determined by logical disjunction of RES_y0 (RES_y1) and RES. When RES becomes high, SW1 of all pixels in array are turned ON. The signals of scan lines for lighting (ILM) are determined by logical disjunction of ILM_y0 (ILM_y1) and ILM. When ILM becomes high, SW2 of all pixels in array are turned ON. RES_y0 (RES_y1) and ILM_y0 (ILM_y1) are connected to scan circuit. Data signals are supplied

from data signal driver.
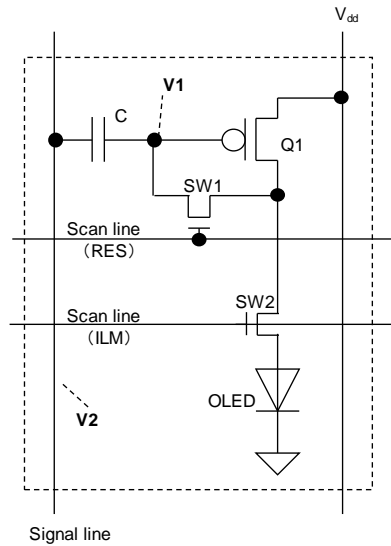
Figure 2.3 Pixel-circuit configuration with V_{th} compensation for AM-OLED
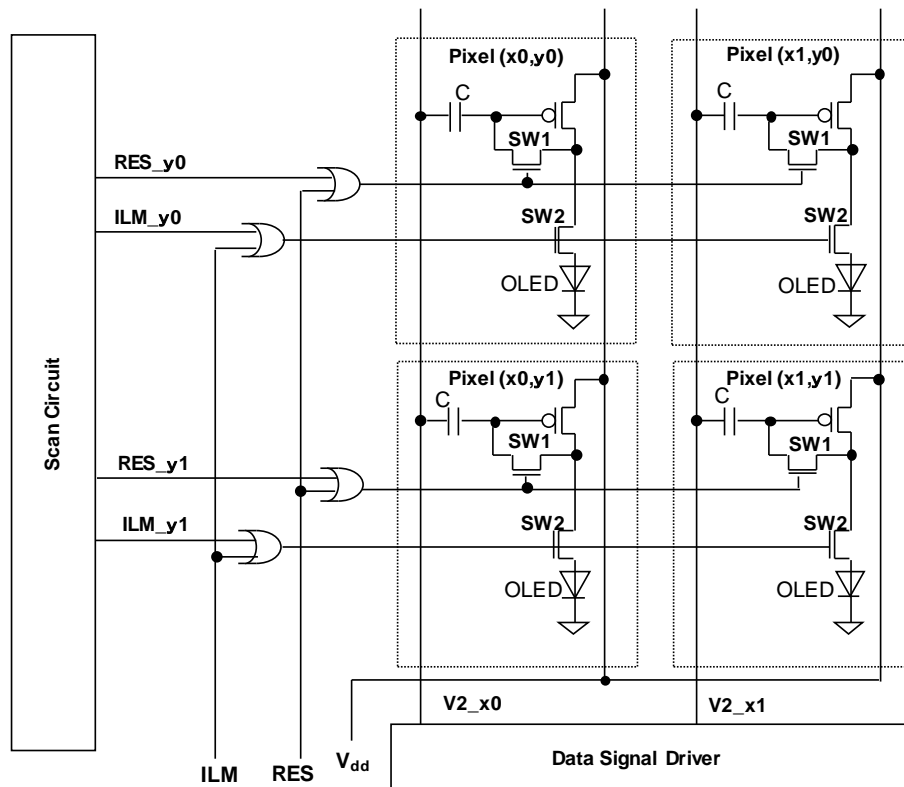
Figure 2.4 AM-OLED display equipped with pixel circuits in Fig. 2.3

As shown in Fig. 2.5, one frame is composed by a programming period and a light-emitting period. During the programming period, each row of the pixels is scanned and written with an analog data signal via the signal line (the voltage on node V2_x0 and V2_x1 in Fig. 2.4). Namely, firstly, the pixel (x0, y0) and pixel (x1, y0) in Fig. 2.3 are selected. The capacitor C of selected pixels memorizes the differential voltage of the analog data signal and threshold voltage V_{th} of Q1 when SW1 and SW2 are turned on at regular intervals and SW2 is turned off. Next, the pixel (x0, y1) and pixel (x1, y1) in Fig. 2.3 are selected, and the same memorized operation is executed. SW1 and SW2 are controlled by RES_y0 (RES_y1) and ILM_y0 (ILM_y1). Through the programming as above, variation of V_{th} can be compensated.

During the light-emitting period, SW2 of all pixels are turned on via the scan lines for emitting (ILM), a triangular sweep voltage is applied to the signal line (V2_x0 and V2_x1), and then drive TFTs (Q1) of all pixels are turned on when the triangular sweep voltage is less than the written analog data signal. The light-emitting duty from 50% to 75% during one frame time can be set. The emission period can be set longer in higher power supply voltage because the programming operation convergence can be faster depending on the power supply voltage and the program period can be shortened.

The relationship between V_{black} and V_{white} is therefore $V_{white} > V_{black}$. Here, the data voltage written to these pixels are V_{00} (pixel (x0, y0)), V_{10} (pixel (x1, y0)), V_{01} (pixel (x0, y1)) and V_{11} (pixel (x1, y1)). The relationship is $V_{10} >$

$V_{00} > V_{11} > V_{01}$. Therefore, the in order of the luminance, it is pixel (x1, y0), pixel (x0, y0), (pixel (x1, y1) and (pixel (x0, y1))
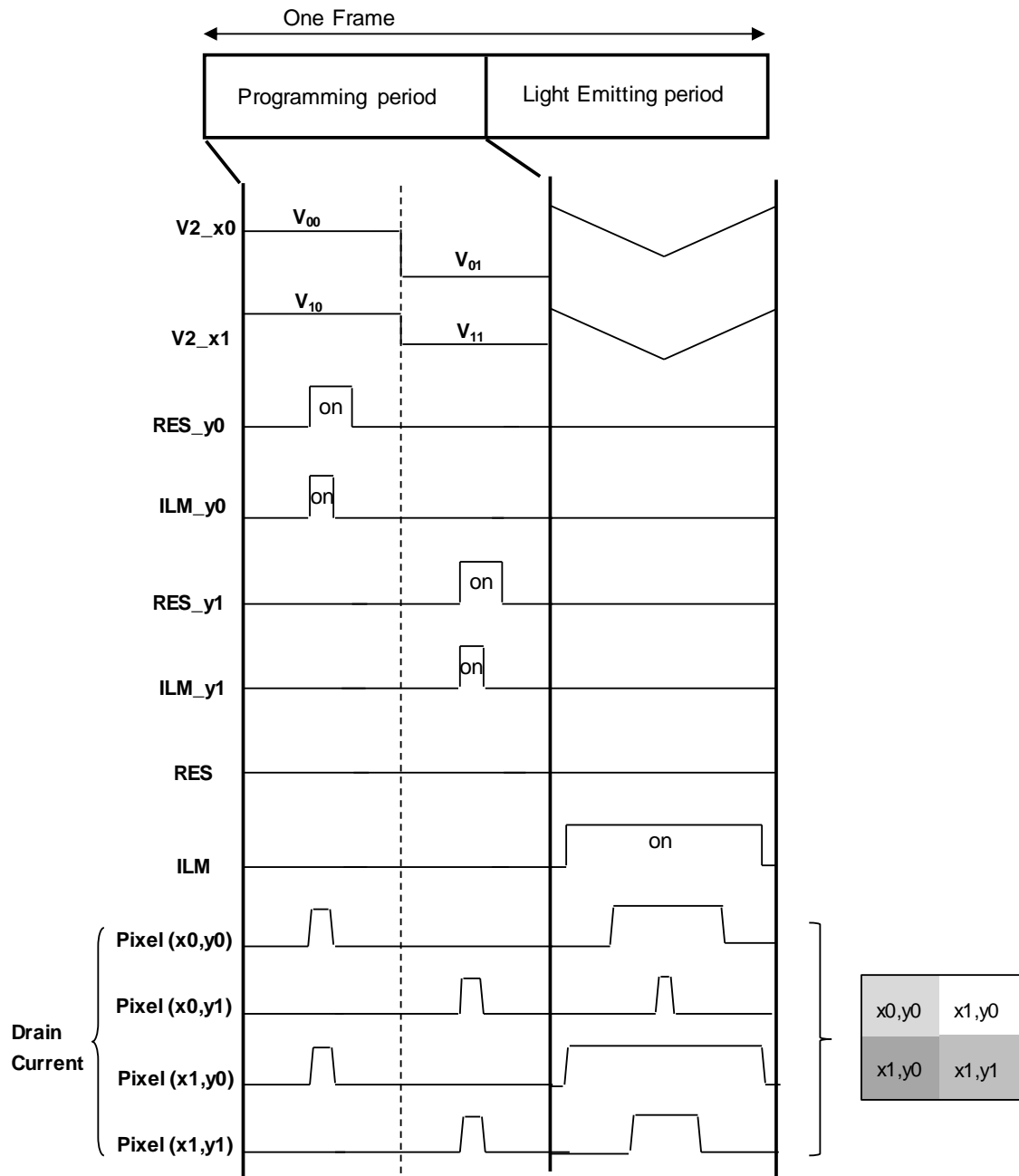
Figure 2.5 Timing chart of ACI AM-OLED panel

As mentioned above, a TFT switch at least must be added to the simplest pixel circuit in order to compensation in the internal circuit, and the area to be allocated for a pixel is restricted. Among the cell array, there are the pixels with leakage current caused by failure of gate of TFT as shown in Fig. 2.6 (a) and the subtle bright spot occurs as shown in Fig 2.6 (b). In this case, C in Fig. 2.3 must be set large so that the gate voltage of drive TFT (Q1) does not move, that is, the area for a pixel is more restricted.

(a) Leakage Current of TFT   (b) Subtle bright spot
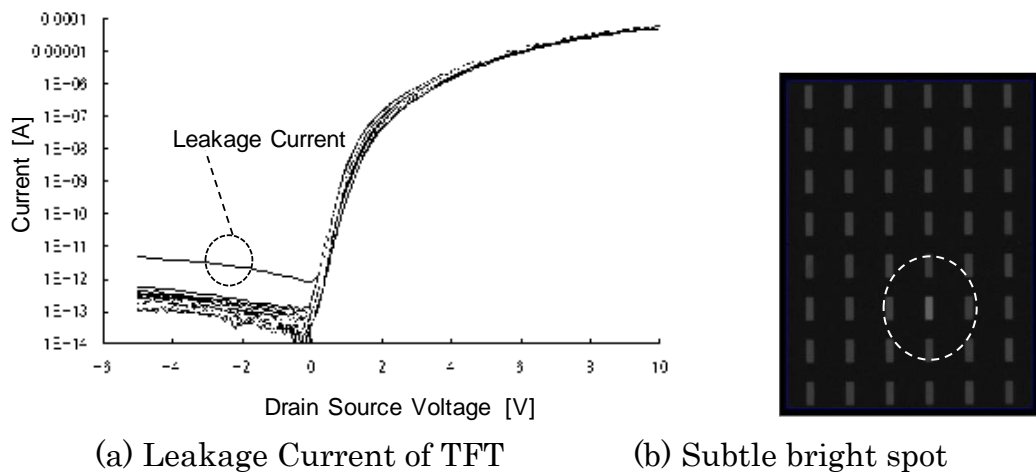
Figure 2.6 Leakage Current of TFT and Subtle bright spot

The hysteresis of the drive TFT (Q1) of the pixel circuit in Fig. 2.3 is affected by the differential voltage of the analog data signal and threshold voltage V_{th} of Q1. This means that the drive TFT (Q1) is affected by the data signal written to other addresses during the image of the one frame. For example, when the pixel (Xa, Yc), pixel (Xb, Yc) and pixel (Xc, Yc) are selected in programming period of the image as shown in Fig. 2.7, the amplitude of

the voltage applied to Q1 at (Xb, Yc) is larger than the applied voltage amplitude at (Xa, Yc) and (Xc, Yc) because V_{black} is stored on V2 side of the capacitor in the pixel (Xb, Yc). This means that holes tend to be detrapped, causing the drive TFT Q1 to be depleted [39-40]. Then, the current at (Xb, Yc) is higher than other current of the pixels at (Xa, Yc) and (Xc, Yc). That is why the crosstalk below the black box is brighter than the neighboring regions. The crosstalk appears when the luminance difference is over 1.0%. The actual occurred crosstalk on display is shown in Fig. 2.8.
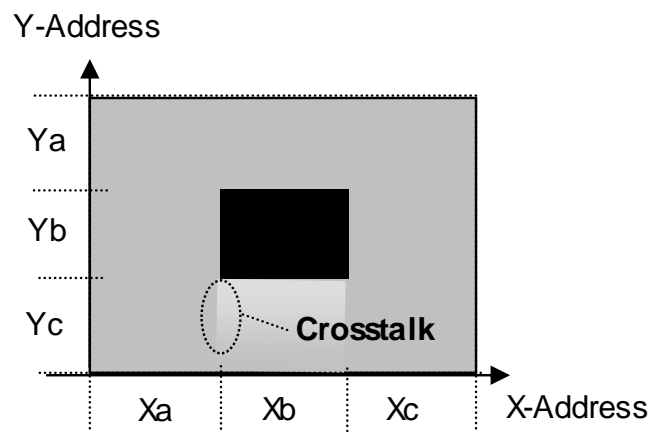
Figure 2.7 Crosstalk image caused by hysteresis of drive TFT Q1
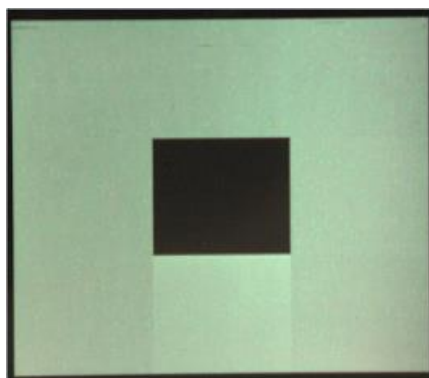
Figure 2.8 Actual crosstalk on display (Number of pixels (480(H)×RGB×480(V)))

Concerning the hysteresis, adding a reset operation to each pixel circuit has been proposed [41-43]. These circuit architectures also require more TFTs in each pixel. To apply these pixel circuits for high-end mobile applications, the most important requirement is to fabricate a display with high resolution and low power consumption.

In order to simplify the pixel circuit, there has been a new trend to use external compensation [44-48]. These circuit architectures also require more TFTs in each pixel or extra sensor such as a dummy OLED. Further, external compensation architecture including hysteresis-suppression has not been proposed. Therefore, simple and effective method is expected for the external compensation of V_{th} variation and hysteresis. In this study, a self-sensing system for avoiding characteristic fluctuation due to hysteresis and producing V_{th} distribution on AM-OELD display using the simplest 2Tr-1C pixel circuit in Fig.2.2 is proposed.

Chapter 3

V_{th} Production Method

3.1 Circuit topology

The circuit for detecting source voltage of drive TFT Q1 is shown in Fig. 3.1. As for this circuit, SW in pixel circuit is turned on, and an appropriate voltage (V_g) is applied to the gate of Q1 from the data signal driver. The source of the drive TFT Q1 is connected to a regular current source outside of the cell array on the AM-OLED panel, and source voltage (V*) can be detected. The impedance of the source of TFT, that is, the impedance of the detection line is low. Therefore, this source-voltage-detection has advantages in terms of detection speed (high) and noise (low). Detected V* is sent to the "detection process block," where thermal noise of the OLED is eliminated by a low pass filter (LPF) and is converted to a digital value by an analog-to-digital converter (ADC) in the detection process block.
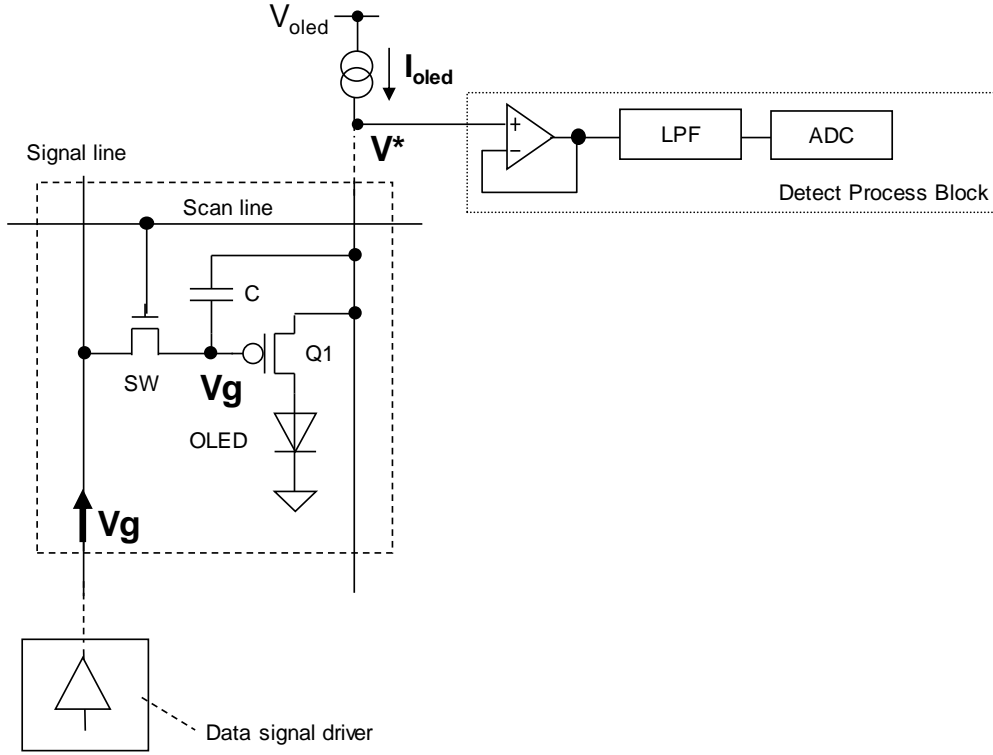
Figure 3.1 Circuit state for detecting TFT characteristic

The current of the drive TFT Q1 in Fig. 3.1 is expressed as the Eq. (3.1).

$$I_{oled} = (1/2) \cdot \mu \cdot C_{ox} \cdot (W/L) \cdot \left\{ V* - V_g - (-V_{th}) \right\}^2 \qquad (3.1)$$

Converted to V*, Eq. (3.1) is changed to Eq. (3.2)

$$V* = V_g - V_{th} - \sqrt{2 \cdot I_{oled} \cdot [1/\{\mu \cdot C_{ox} \cdot (W/L)\}]} \qquad (3.2)$$

where μ is mobility of electrons, V_{th} is threshold voltage, C_{ox} is gate-oxide capacitance per unit area, and W/L represents the device dimensions, namely,

width and length.

3.2 Detection Method

Figure 3.2 shows the V_{th} dispersion of LTPS-TFT 50 samples randomly extracted from the glass substrate. The standard deviation σ is about 110mV. Considering ± 3σ, the V_{th} variation of about 660 mV in the cell array are expected.
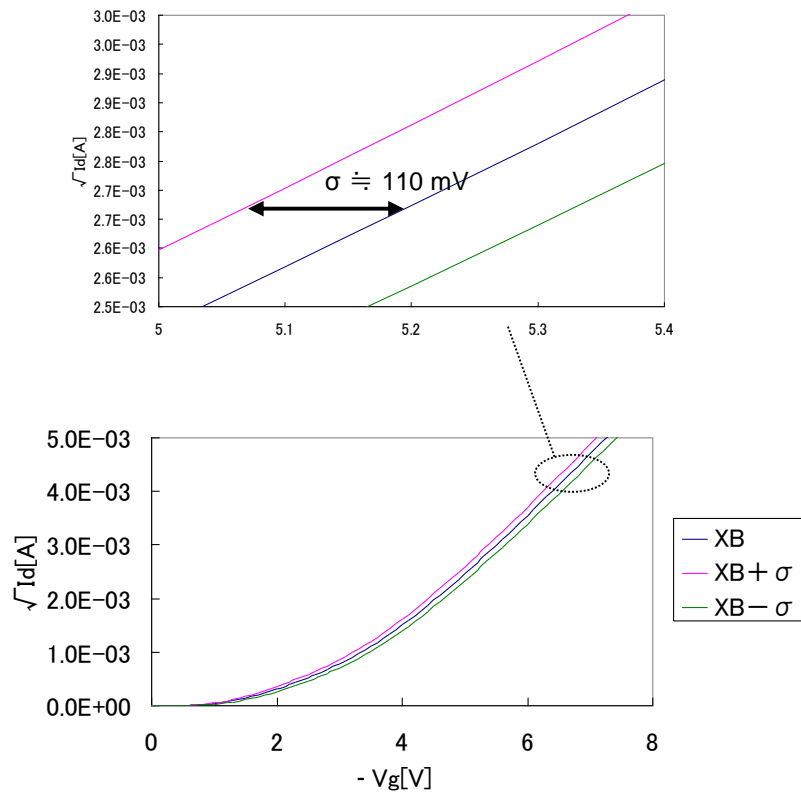
Figure 3.2 V_{th} dispersion of LTPS-TFT 50 samples

A constant voltage during the light emitting period of the ACI driving as shown in Fig.2.3, 2.4 and 2.5 was supplied to the data signal line, and the luminance of 40 pixels among the cell array were measured. As the result, the

relationship between the luminance of 40 pixels and the gate-source voltage V_{gs} of the drive TFT (Q1) is shown in Fig. 3.3. The standard deviation σ is about 20mV. This means that the high-quality image with V_{th}-compensation can be achieved if the variation of about 720 mV can be suppressed to 120 mV (± 3σ).
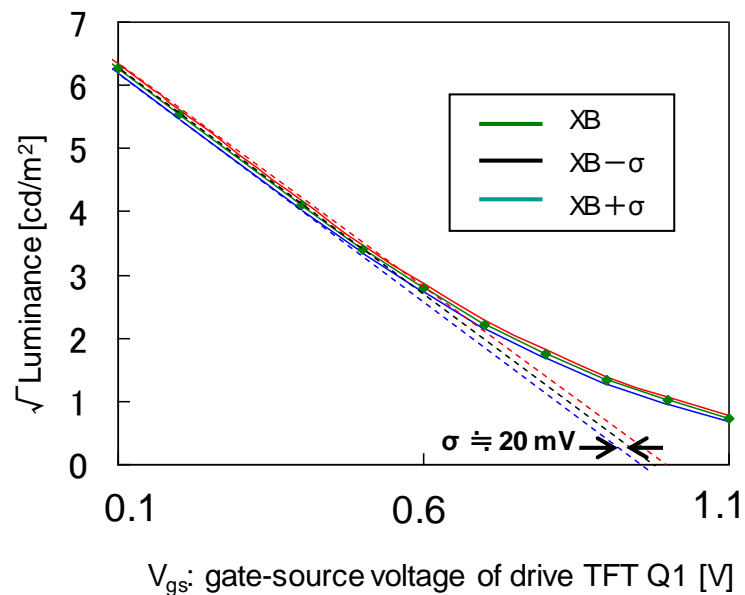
Figure 3.3　Relationship between the luminance of 40 pixels and the gate-source voltage V_{gs} of the drive TFT (Q1) in ACI driving
(Vth variation compensated by ACI driving)

The hysteresis characteristic of the drive TFT (Q1) is shown in Fig. 3.4 [39]. The hysteresis consists of a hole-trapping mode and hole-detrapping mode. Hole trapping takes place when a negative bias is applied to the gate of the drive TFT. Hole detrapping takes place when a smaller negative bias

is applied to the gate of the drive TFT [40].

In hole-trapping mode, threshold voltage (V_{th}) is "enhanced" by changing characteristic from A to B. Meanwhile, in hole-detrapping mode, V_{th} is "depleted" by changing characteristic from B to A. In the region of the drain current to be used in the AM-OLED, V_{th} shift is about 200mV as shown in Fig. 3.4. This value is too large against the V_{th} variation of about 660 mV and the suppression target 120 mV. To detect V* given by Eq. (3.2) precisely, V* detection should be executed when suppressing fluctuation caused by hole trapping and detrapping.
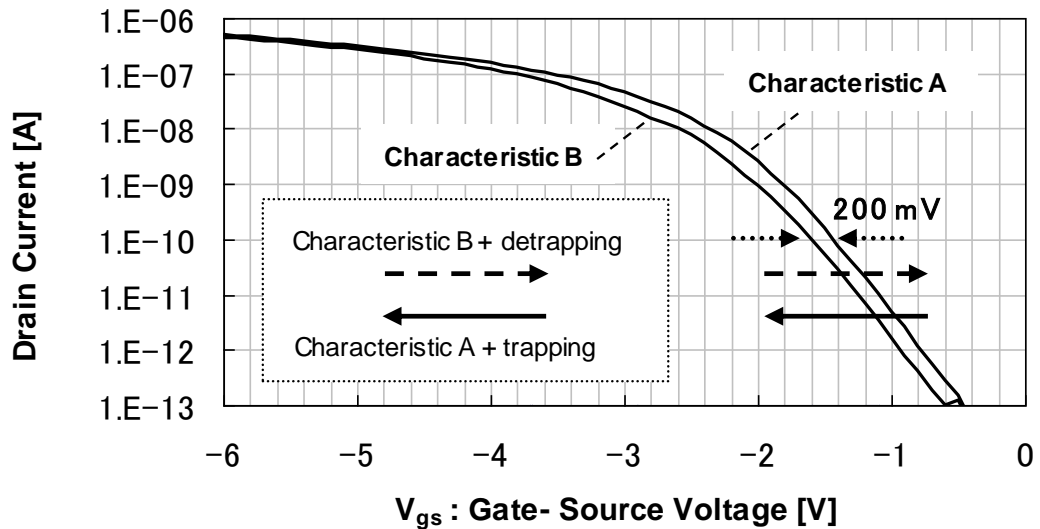
Figure 3.4 Hysteresis of TFT characteristic

Hereafter, the hole-trapping time means the time for characteristic A to converge with characteristic B, and the hole-detrapping means the time for characteristic B to converge with characteristic A. Furthermore, depletion time is much longer than enhancement time. It is reported that depletion time

is over 20 s [40].

The detection of drive-TFT (Q1) source voltage is classified to a hole-trapping mode and a hole-detrapping mode. As shown in Fig. 3.5, the V* detection method in a hole-trapping mode is consisted of three steps. In 1st step (waiting 1), the regular current source (I_{oled}) is set to zero and V_{oled}, for example, 5 V is applied to gate of drive TFT (Q1) so that a regular current is not supplied to the drive TFT (Q1). In 2nd step (waiting 2), regular current, for example, 100 nA and gate voltage, for example, 3 V are supplied to the drive TFT (Q1). In waiting 2, the drive-TFT (Q1) characteristic is in hole-trapping mode and is enhanced from A to B. The estimated enhancement time is in the order of milliseconds [39]. In 3rd step, V* detection is executed after V* converged to within quantization noise of the ADC to characteristic B. Here, quantization noise of the ADC is sufficiently set 10mV and this value is sufficient for the suppression target 120 mV. V* detection time is determined by the impedance of the detection line in Fig. 3.1 and estimated to be in the microsecond order.
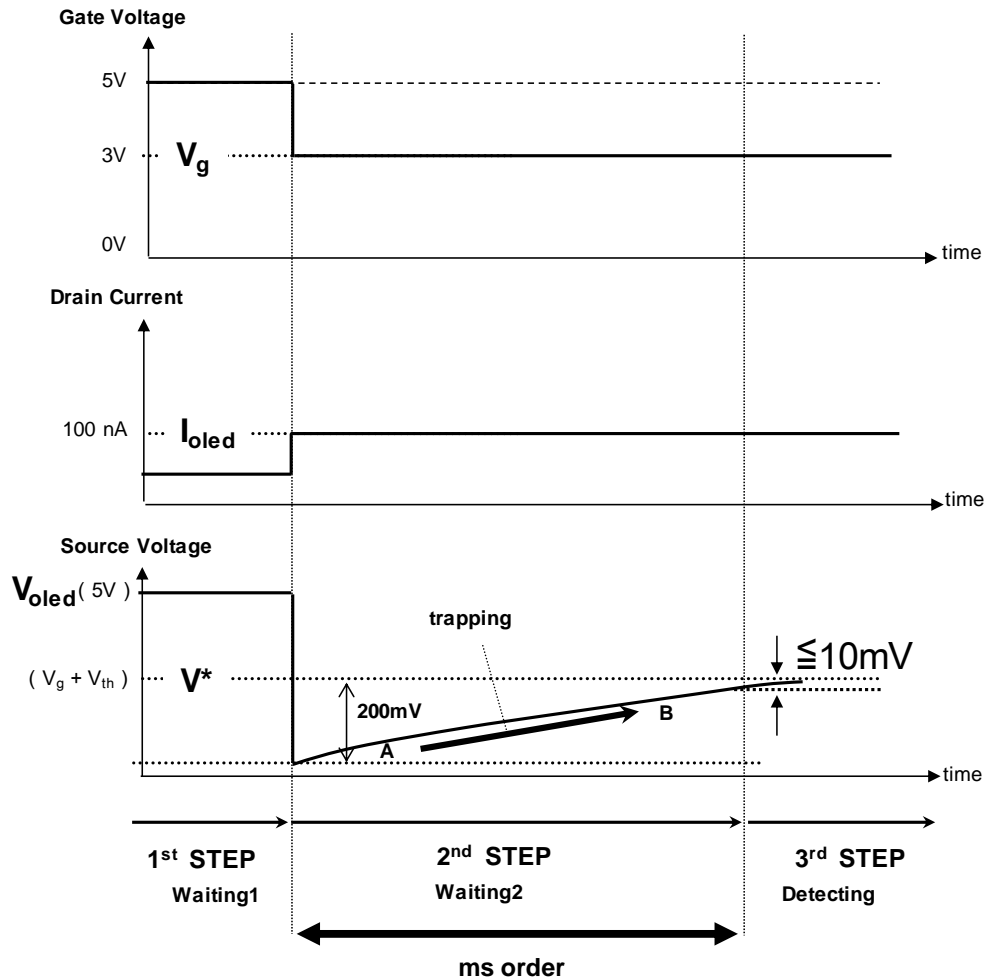
Figure 3.5 Detection method (Hole-trapping detection)

On the other hand, V* detection in hole-detrapping mode, shown schematically in Fig. 3.6. This mode is also consisted of three steps. In 1st step (waiting 1), I_{oled} is not supplied to the drive TFT (Q1). In 2nd step (waiting 2), a large regular current, for example, 800 nA is supplied to the drive TFT (Q1) and for several microseconds. In waiting 2, the drive-TFT (Q1) characteristic is enhanced rapidly from A to B by supplying large regular current. In 3rd step, smaller regular current, for example, 100 nA or 400 nA is supplied to

the drive TFT (Q1). Here, V* detection is executed in hole-detrapping mode, and the drive-TFT (Q1) characteristic is depleted from B to A. Depletion time is much longer than enhancement time. In the micro-second-order detection time of 3rd step, the fluctuation of V* can be much smaller than quantization noise (10 mV) of the ADC. V* detection can be therefore executed on the condition of suppressing fluctuation caused by the TFT-characteristic hysteresis.
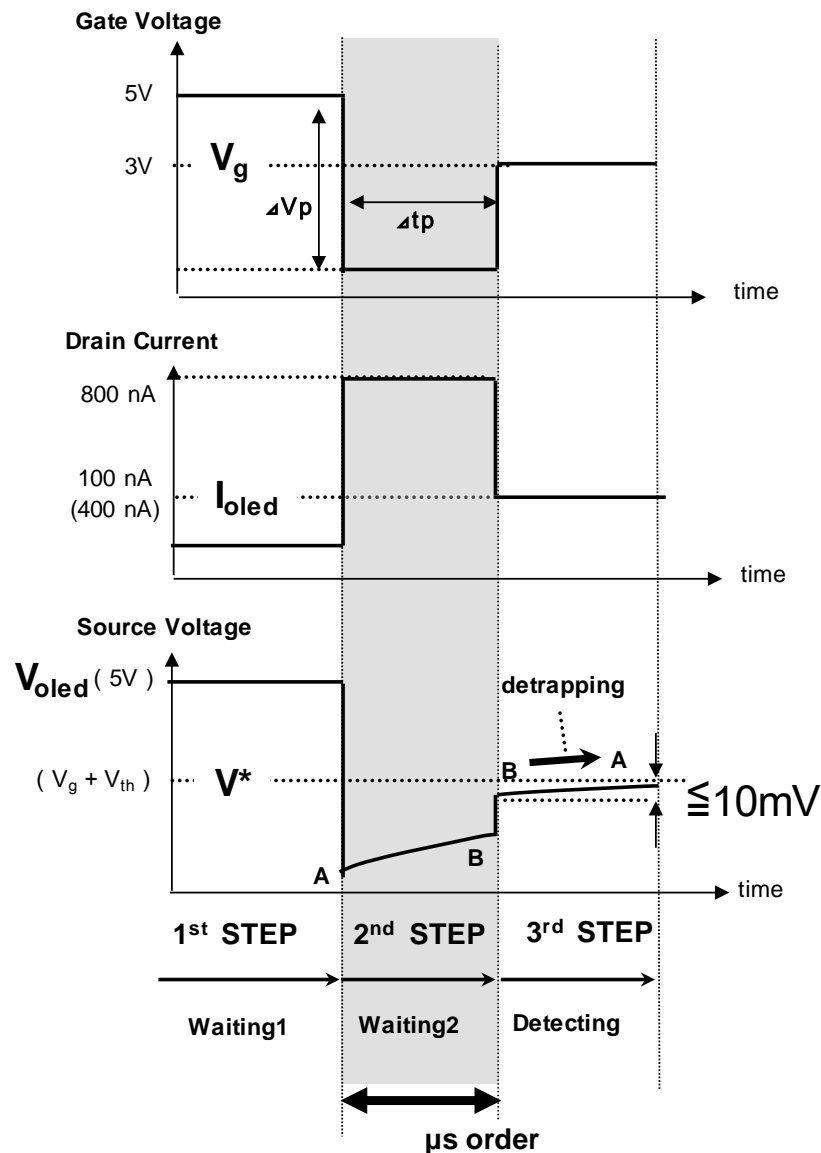
Figure 3.6 Detection method (Hole-detrapping detection)

As mentioned above, the V* detection in hole-trapping mode must be set to the millisecond order in 2nd step, on the other hand, the V* detection in hole-detrapping mode can be the microsecond order. The combination of ΔT_p (the time required 2nd step) and ΔV_p (source voltage fluctuation in 2nd step) needed to keep V* fluctuation smaller than quantization noise (10 mV) of the ADC is measured. Figure 3.7 shows the result of the combination. ΔV_p can be determined by the value of I_{oled} such as 800 nA and it becomes high when I_{oled} is high and the holes are fully trapped at the gate of the drive TFT (Q1). As shown in the Fig.3.7, when ΔV_p is higher than 2.5 V, ΔT_p, namely 2nd step (waiting 2), can be set to microsec order.
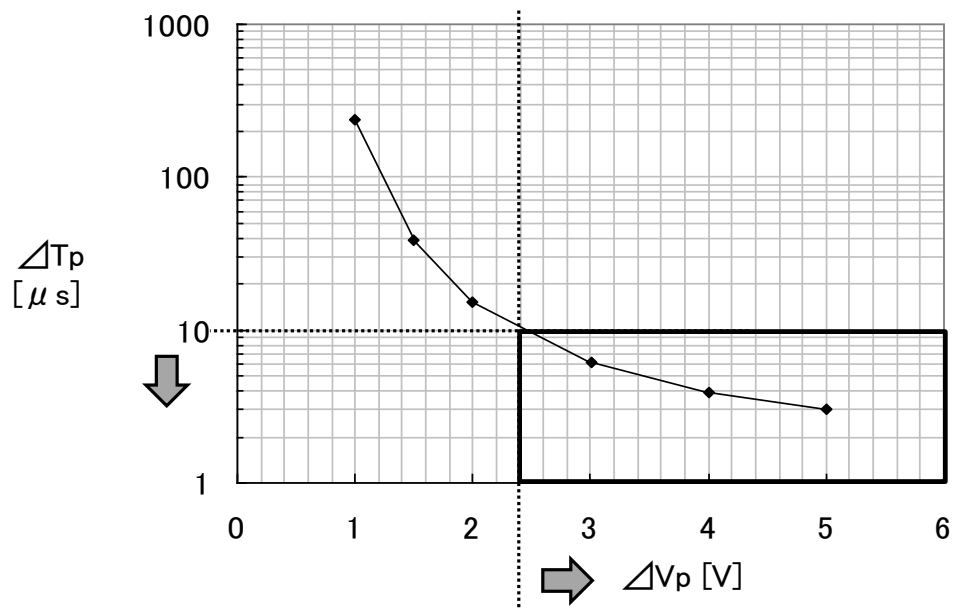
Figure 3.7   Combination of ΔT_p and ΔV_p to maintain characteristic B during detrapping period smaller than quantization noise (10 mV)

3.3 V_{th} Calculation

The drive TFT (Q1) of each pixel circuit has various values about electron mobility μ and threshold voltage V_{th} in Eq. (3.2). The purpose of this method is to generate V_{th} precisely. To improve precision of V_{th} generation, μ is eliminated. To eliminate μ as a factor in V* variation, the regular current source is set to two different values (I_{oled1} and I_{oled2}). It therefore follows that

$$V_1^* = V_g - V_{th} - \sqrt{2 \cdot I_{oled1} \cdot [1/\{\mu \cdot C_{ox} \cdot (W/L)\}]} \tag{3.3}$$

$$V_2^* = V_g - V_{th} - \sqrt{2 \cdot I_{oled2} \cdot [1/\{\mu \cdot C_{ox} \cdot (W/L)\}]} \tag{3.4}$$

Eqs. (3.3) and (3.4) are replaced by

$$V_{th} = \{(V_1^* - V_g) - K \cdot (V_2^* - V_g)\}/(K - 1) \tag{3.5}$$

where K is $\sqrt{I_{oled1}/I_{oled2}}$. Setting I_{oled1} and I_{oled2} in Eq. (3.5) to K = 2 gives

$$V_{th} = (V_1^* - V_g) - 2 \cdot (V_2^* - V_g) \tag{3.6}$$

where "2" means a 1-bit shift in digital computing. V_{th} can therefore be calculated by simple subtraction and a 1-bit-shift method, where digitally converted V*$_1$, V*$_2$, and V_g are used. Here, I_{oled1} was set to 100 nA, I_{oled2} was

set to 400 nA as shown in 3rd step of Fig. 3.6. Eq. (3.6) is formed by subtraction and the multiplication of 2. The multiplication of 2 means 1bit shift that is executed by shift register. Namely, Equation (3.6) is executed by a simple digital circuit that is constituted by a subtraction and a shift register.

3.4 System Configuration

A block diagram of a prototype AM-OLED panel and the non-uniformity compensation system are shown in Fig. 3.8. The AM-OLED display is composed of the panel, a detection board, and a signal-generation board. As illustrated in Fig 3.8, pluralities of pixel circuits (Pixel (x0, y0), Pixel (x1, y0), Pixel(x0, y1) and Pixel(x1, y1)) are provided in array. The data signal lines (V_x0, V_x1), scan lines (WR0, WR1) and a power supply line V_{dd} are provided for each pixel. During detection, SW_V_{dd} is turned off. The detection board includes LSI switches (SW_I0 and SW_I1) for selecting pixels in the x-direction.

Figure 3.9 shows the specific diagram of the detection board. The selection of the current source (I_{oled1} or I_{oled2}) and the timing of the switch-scan are controlled by the FPGA (Field-Programmable Gate Array). The voltage is adjusted (for example, 5 V → 3.3 V) by the level shifter and the switches are scanned in the x direction from address 1 to address n by the shift register. Further, the command to the scan circuit is sent from the FPGA. The V* detection results of each pixel are stored in the memory.

Figure 3.8 Block diagram of AM-OLED panel and non-uniformity-compensation system

Figure 3.9 Specific block diagram of detection board

A timing chart of the V* detection in hole-detrapping mode for the diagram in Fig. 3.7 is shown in Fig 3.10. Firstly, WR0 and WR1 become high, SW of all pixels in matrix are turned ON. High regular voltage 5V is supplied to the gate of drive TFT (Q1) from data signal driver and drive TFT (Q1) of all pixels are turned OFF. Next, WR0 becomes high and WR1 becomes low, SW of Pixel (x0, y0) and Pixel (x1, y0) in matrix are turned ON. After these SWs are turned on, Low regular voltage 0 V is supplied to the gate of drive TFT (Q1) from data signal line V_x0. When SW_I0 is turned on, large regular current (800nA) is supplied to the drive TFT of Pixel (x0, y0) and this drive-TFT characteristic is depleted from B to A. Finally, V_g (3V) in Eq. (3.6) is supplied to the gate of Pixel (x0, y0) and I_{oled} (100nA / 400nA) is supplied to the drain of drive TFT (Q1) of Pixel (x0, y0) After that, V^*_1 and V^*_2 in Eq. (3.6) on the Pixel (x0, y0) are detected. During drive TFT (Q1) of all pixels are turned OFF, V_{com} is set to V_{dd}. When large regular current (800nA) or I_{oled} (100nA / 400nA) is supplied to the drain of drive TFT, V_{com} is set to -5V in order to ensure the overdrive voltage of drive TFT. The V* detection of other pixels (Pixel (x1, y0), Pixel (x0, y1) and Pixel(x1, y1)) also are performed in the same way.

V^*_1 and V^*_2 in Eq. (3.6) on the selected pixel are sent to the buffer amplifier of the detect process block. The detected V^*_1 and V^*_2 are converted to low-noise voltage by the LPF (to eliminate thermal noise) and then converted to a digital value by the ADC as shown in Fig 3.1. The calculation result of Eq. (3.6) is exchanged with the offset signal. The offset signal is

added to the data signal, and compensated data is applied to each pixel by way of the timing controller (T-con) and data signal driver.
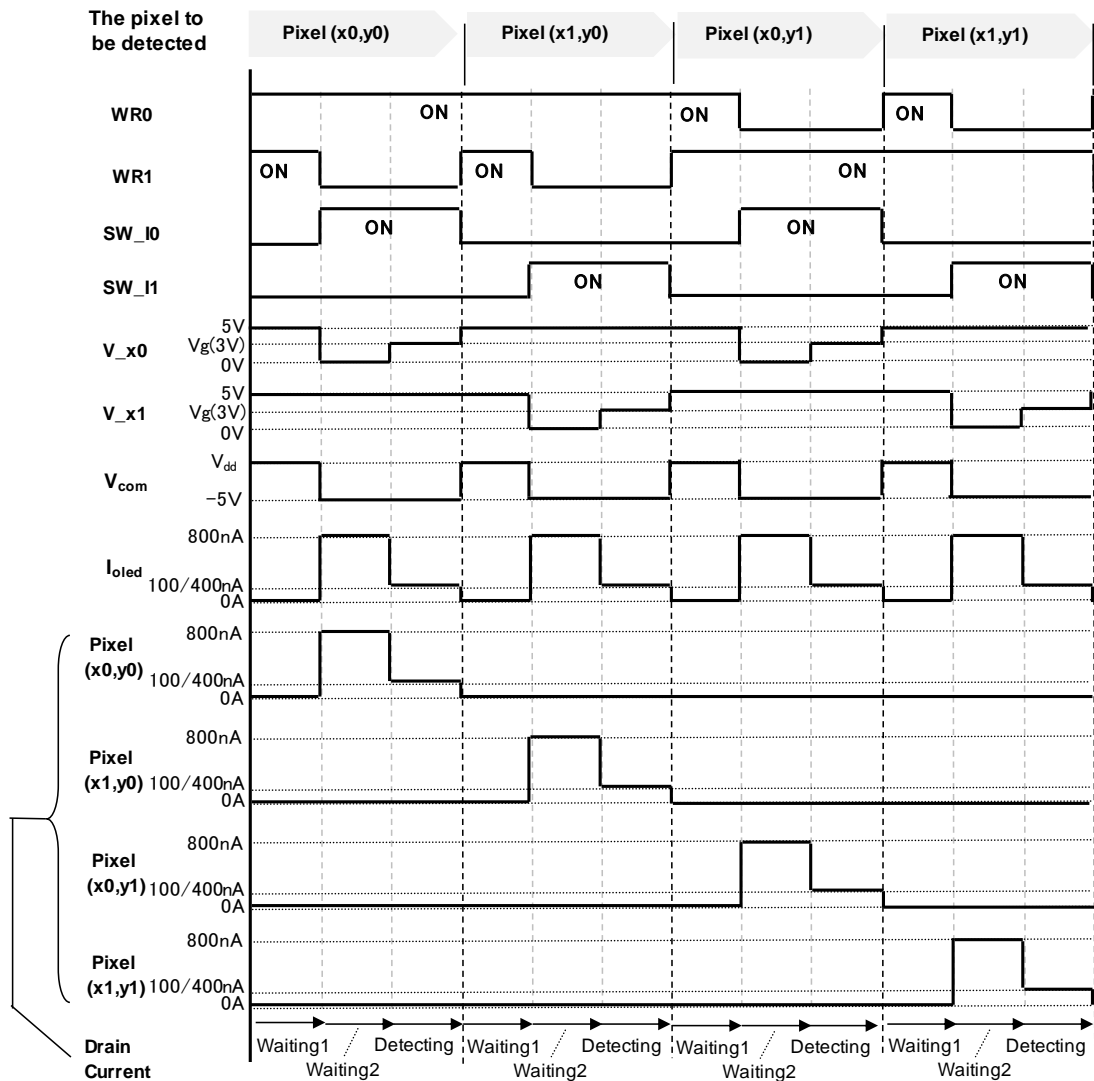
Figure 3.10 Timing chart of the V* detection for AMOLED panel

In driving OLED method, a reset period is set in one frame, which is divided into a reset period, a programming period, and a light-emitting period. In the reset period, the negative-bias precharge is applied to the drive TFTs

(Q1) of all pixels. This reset operation realized good hysteresis compensation. Furthermore, as the previous research reported [49], power-line IR drops of p-type pixel circuits can be compensated by dividing one frame to a programming period and a light-emitting period, and separating supply voltage in a programming period.

During display, SW_V_{dd} is turned on and supply voltage V_{dd} is connected to the AM-OLED panel. The detection board is separated. A timing chart of the driving method for 2Tr-1C pixel circuit is shown in Fig 3.11. One frame is divided into a reset period, a programming period and a light-emitting period. Depending on the adjustment of V_{dd}, this reset operation at 75% emitting duty ratio realized good hysteresis compensation ability at measurements [43].

In the reset period, the negative-bias precharge 0V is applied to the drive TFTs (Q1) of all pixels from data signal line V_x0 and V_x1 when SWs of all pixels are turned on by control signal WR0 and WR1 as shown in Fig 3.11. During the programming period, each row of pixels is scanned and written with an analog data signal by data signal line (the voltage on node V_x0 and V_x1 in Fig. 3.8). The analog data signal added offset signal is memorized to memory capacitor C in each pixel. In a reset period and a programming period, V_{com} is set to V_{dd} in order not to emit OLED. During the light-emitting period, V_{com} becomes 0V, and then drive TFTs (Q1) of all pixels are turned on. In this the light-emitting period, the gate of drive TFTs (Q1) of all pixels is floating and supply voltage drop doesn't occur.
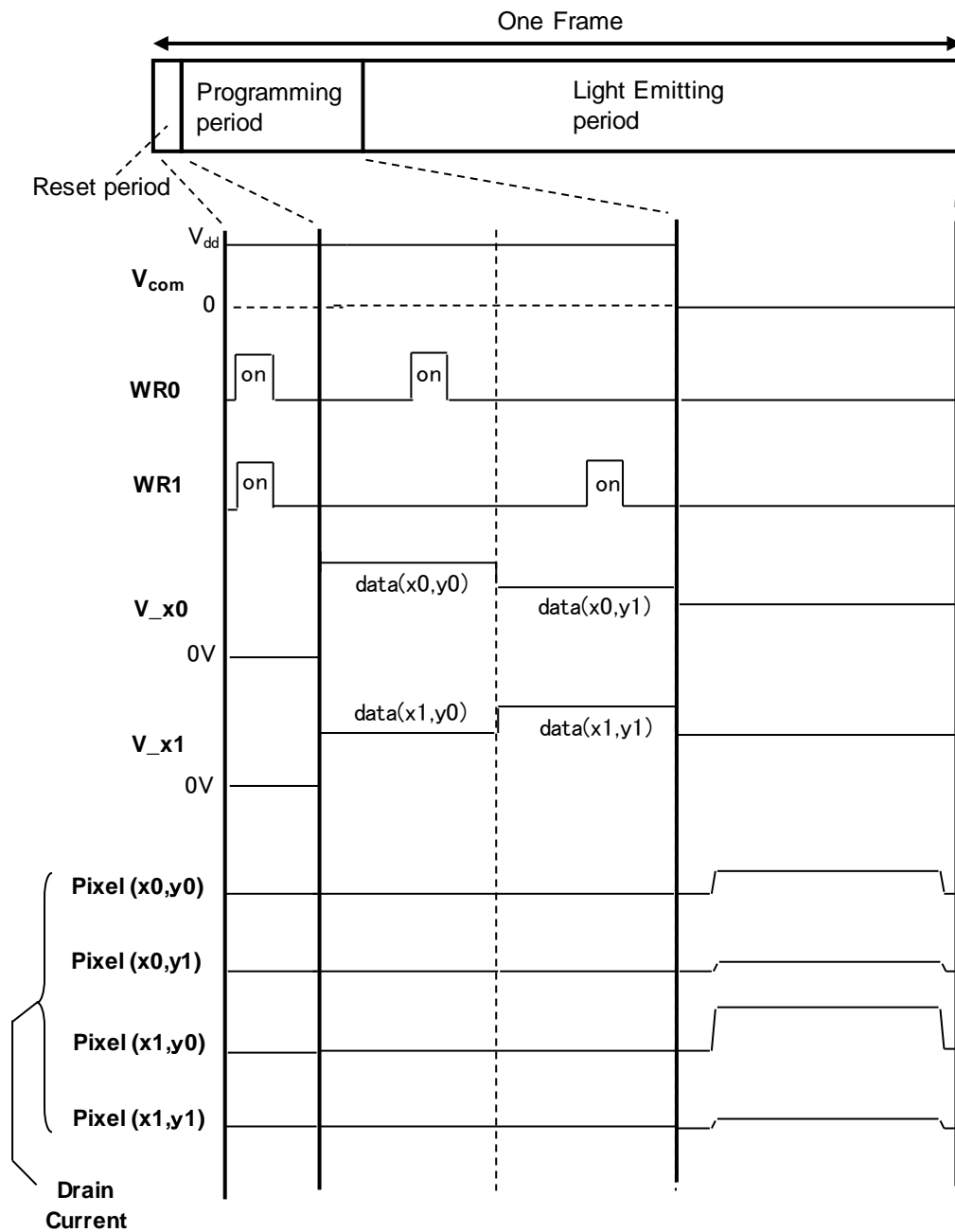
Figure 3.11 Timing chart of driving method for 2Tr1C pixel circuit

Chapter 4

AM-OLED Panel Evaluation

4.1 Prototyped Panel

A 3.8-inch RGB×480×320-pixel OLED display utilizing a conventional simple 2Tr-1C pixel circuit was made as a prototype. In Fig 3.10, Waiting1 time is set to 10 microseconds and Waiting2 time is set to 50 microseconds. Detecting time is set to 5 milliseconds because the parasitic capacitance must be charged on detection board and this charging takes a long time. Total detection time of green 480×320-pixels is about 26 minutes when I_{oled} is 100nA and 400nA. If detection board is integrated, the parasitic capacitance is much small and we estimate total detection time of green 480×320-pixels becomes about 30 seconds.

Figure 4.1 shows the schematic circuit diagram for driving this prototype OLED. The signal (High or Low) of WR0 (WR1) shown in Fig. 3.8 is generated by the logical operation of GASE, GMST, and shift register. Similarly, the analog data signal of V_x0 (V_x1) is determined by selecting the switch of R (Red), G (Green), B (Blue) or EXSEL.

Figure 4.2 shows the timing chart of driving prototype OLED. In the reset period, the signals of WR0 and WR1 shown in Fig. 3.11 become High by setting GASE and GMST to High, and the negative-bias precharge 0V from EXSEL is applied to the drive TFTs (Q1) of all pixels via signal line V_x0 and V_x1. In this prototype , 1 msec was allocated as the reset period. In the programming period, each row of the pixels is scanned by the shift register and GASE, and an analog data signal is written via the RGB signal line. In this prototype, the programming of R,G and B is respectively assigned to 3.4 µsec, and 21.5 µsec is allocated as the programming time for each row (one horizontal period). In total, the programming time of about 6.88 msec (21.5µsec×320) is required for the entire display. Therefore, the programming time was set to 7.6msec with a margin. As a result, the light emitting period became 8msec. This means that the reset period is limited to 12.5% of the light emitting period, and the light emitting period can be enough secured (about half of one frame).
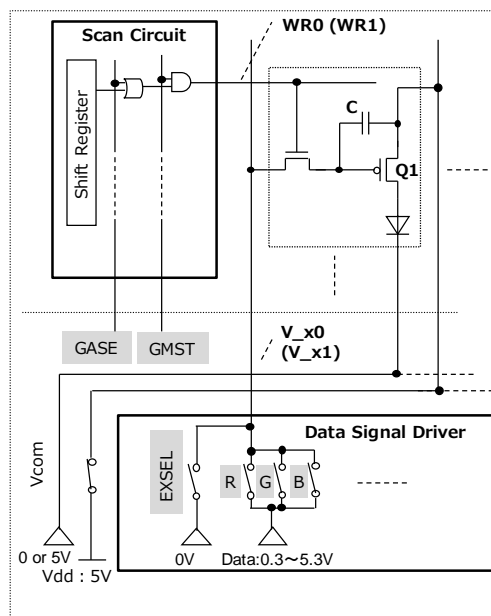
Figure 4.1 Schematic circuit diagram for driving prototype OLED

One Horizontal Period: 21.5us

GMST

R

3.4us

G

B

One Frame : 16.6ms

GMST

EXSEL

GASE

Programming
Period : 7.6ms

Light Emitting
Period : 8ms

Reset Period : 1ms
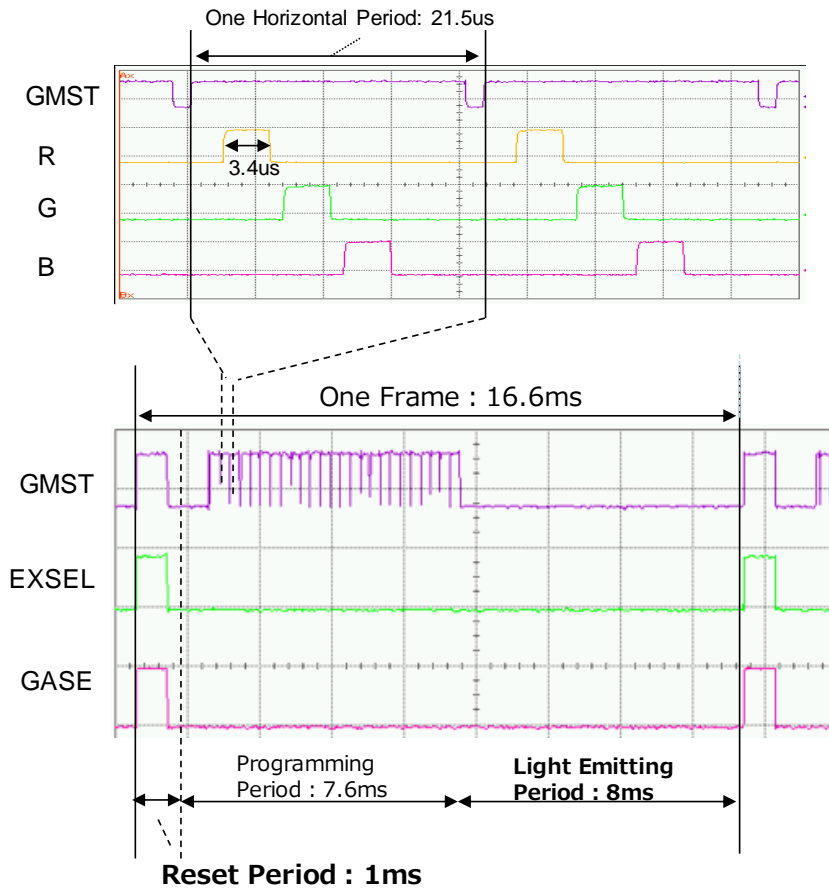
Figure 4.2 Timing chart for driving prototype OLED

4.2 Panel Evaluation

The V_{th}-distribution for all pixels of the OLED display is shown in Fig.
4.3(a). This V_{th}-distribution was calculated by using Eq. (3.6) with source
voltages V^{*}_1 and V^{*}_2 and gate voltage V_g of Q1. V^{*}_1 and V^{*}_2 were detected by
a simple circuit and the hole-detrapping detection architecture. The
calculated V_{th} was quantized by an A/D converter. The V_{th}-distribution is
640mv. This value is almost equal to the V_{th} variation (660 mV) estimated in
Fig. 3.2.

The V_{th}-distribution was converted to a V_{th}-distribution image composed of green 480×320 pixels (Fig. 4.3(b)). A green 480×320-pixel panel formed by the OLED driven by a conventional 2Tr-1C pixel circuit without V_{th} compensation is shown in Fig. 4.4. The visual characteristics of this panel and those of the V_{th} distribution image are highly correlated, indicating that the detected V^* and calculated V_{th} distributions are equal to the non-uniformity of the OLED panel. Especially, as for the mura pattern, the diagonal mura1, the X-direction mura2 and Y-direction mura3 in Fig. 4.3(b) are respectively much similar to the mura1a, the mura2a, and the mura3a in Fig. 4.4. It is therefore concluded that V_{th} distribution is a primary factor in non-uniformity of images formed by an LTPS AM-OLED.
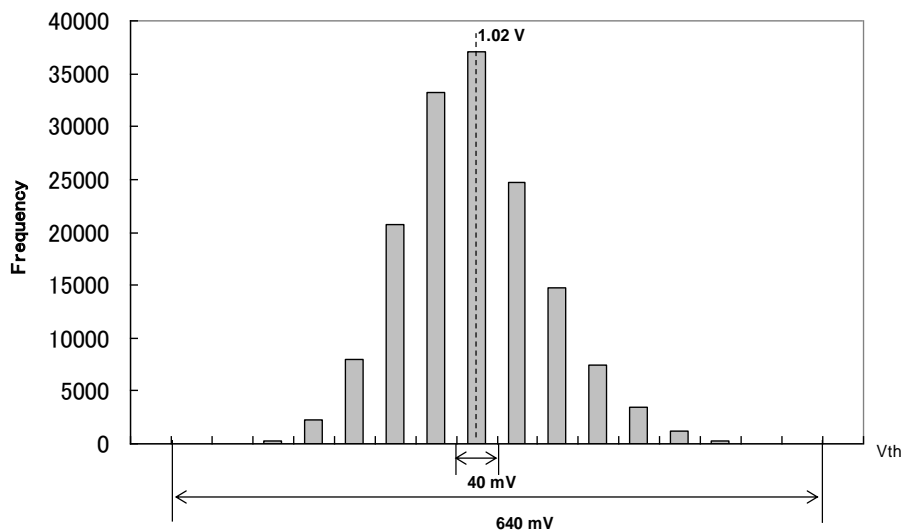
(a) V_{th} distribution map for part of a pixel image
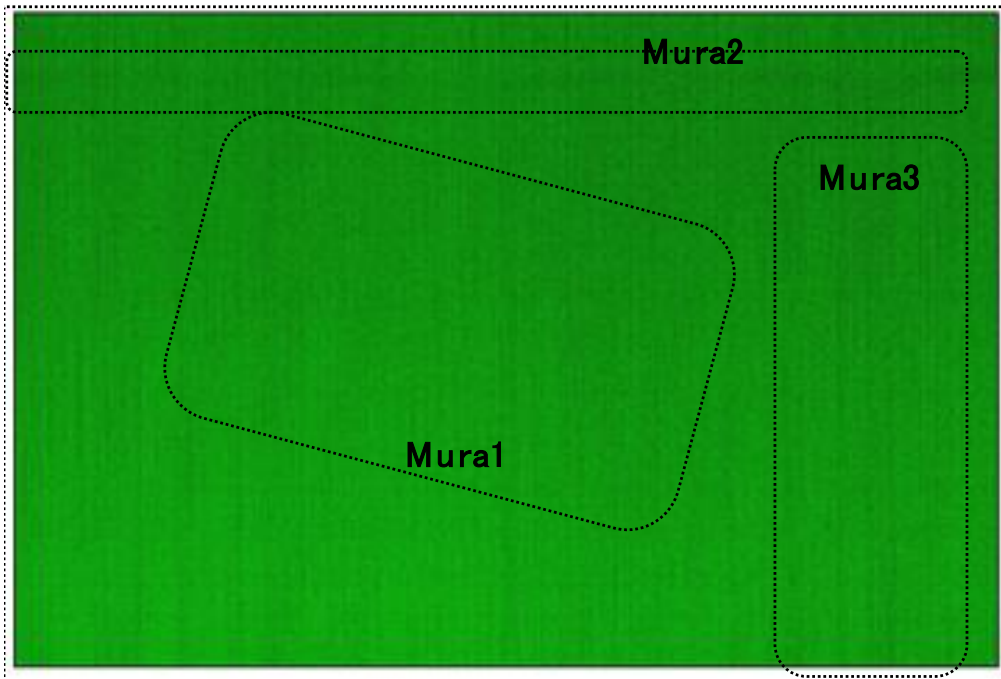
(b) Calculated V_{th} distribution image formed by 480×320 pixels

Figure 4.3 V_{th} distribution
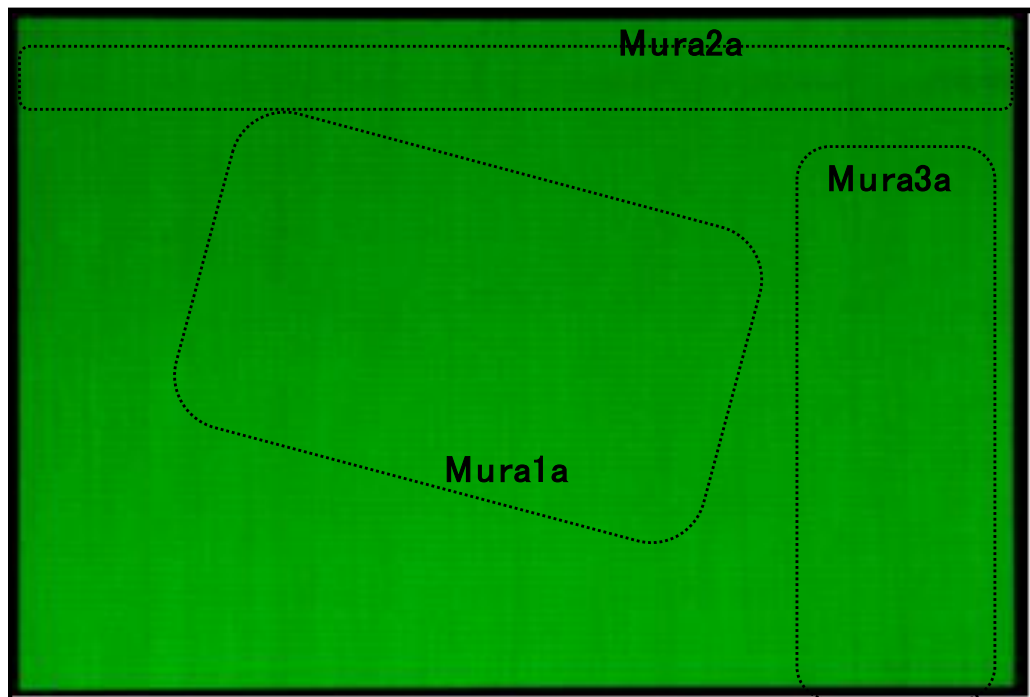
Figure 4.4 Display image formed without V_{th} compensation

The offset signal was added to data signal for each pixel and Vth-distribution was suppressed to 120 mV. A green 480×320-pixel panel formed by the OLED driven by a conventional 2Tr-1C pixel circuit with Vth compensation is shown in Fig. 4.5. The panel produces high-uniformity pictures. Each pixel's luminance of 6×4-pixel among the cell array was also observed. As shown in Fig. 4.6, the high-uniformity picture can be produced in the local region on AM-OLED display.
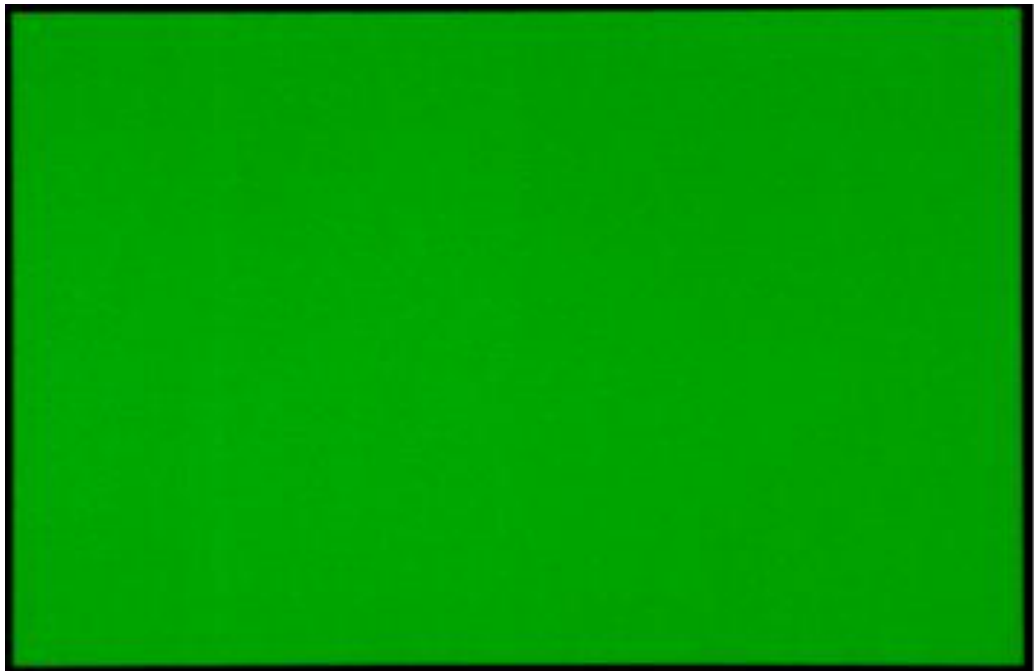
Figure 4.5 Display image formed with V_{th} compensation

Without V_{th} compensation   With V_{th} compensation
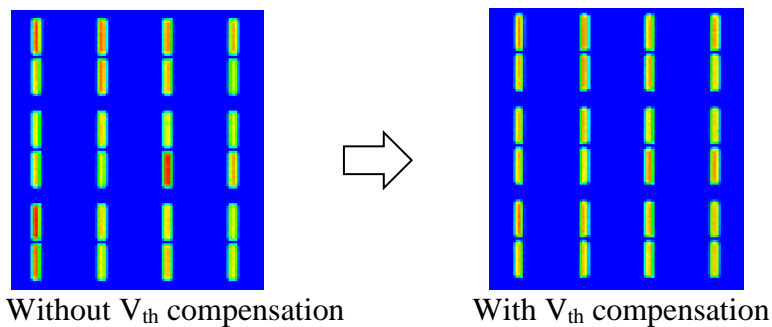
Figure 4.6 luminance of 6×4-pixel pictures among the cell array

Average and standard deviation (σ) of luminance of 6×4-pixel pictures were calculated. The luminance variation is defined in terms of average A and deviation σ as follows:

$$\text{luminance variation} = \{\sigma / A\} \times 100 \ [\%]. \qquad (4.1)$$

The luminance variation of a 6×4-pixel image is shown in Fig. 4.7, which confirms that the luminance variation is suppressed by V_{th} compensation.
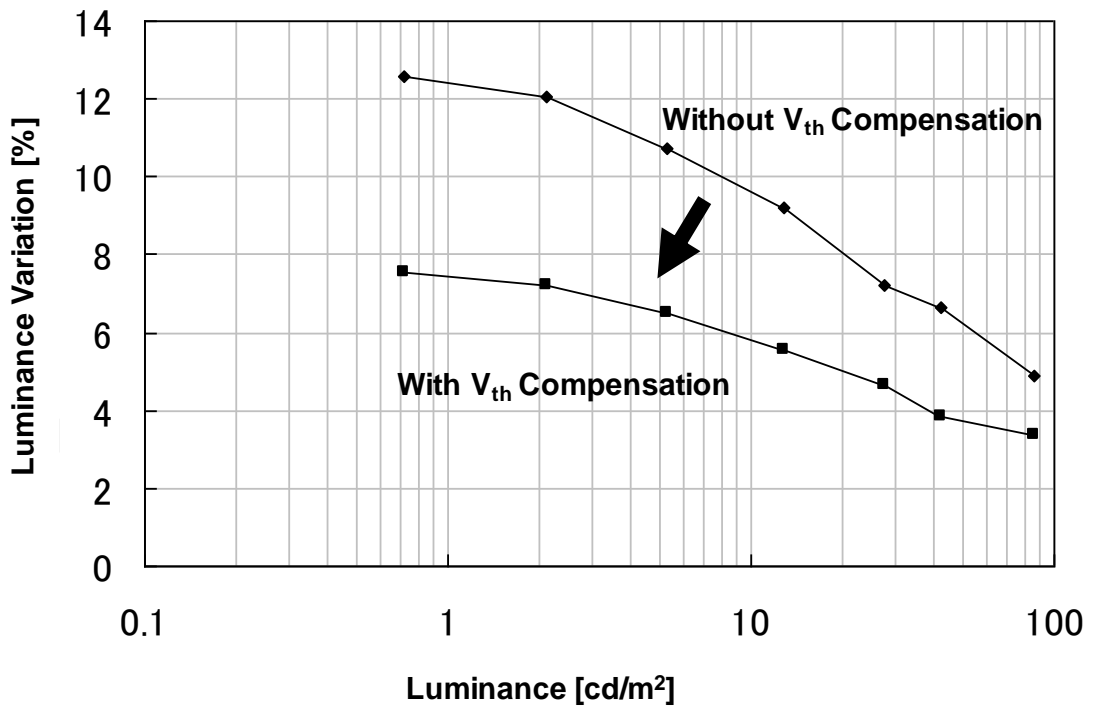
Figure 4.7 Luminance variation with and without V_{th} compensation

The result of compensation for power-line IR drops is shown in Fig. 4.8. In the conventional driving [32] using simplest pixel circuits, due to the IR drop of the power supply line V_{dd}, the current of the drive TFTs (Q1) of the pixels at address of the green pattern of the columns that exist white pattern decreases. Therefore, the smear occurred as shown in Fig. 4.8 (a). Meanwhile, in the developed driving method, the smear didn't occur as shown in Fig. 4.8 (b) by dividing one frame to a programming period and a light-emitting period, and separating supply voltage in a programming period.

(a) Conventional driving (b) Proposed driving
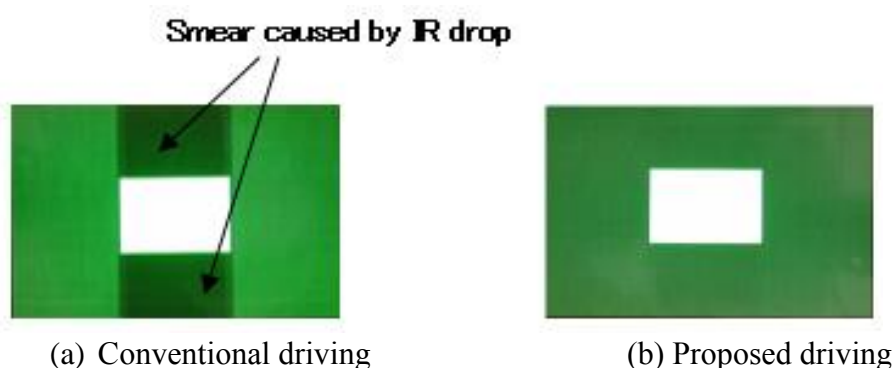
Figure 4.8 Compensation of IR drop

Fig. 4.9 shows real display images when the signal data are changed from a pattern in Fig 4.8 to green solid. As shown in Fig. 4.9 (a), If the reset period was not set in Fig. 3.11 and Fig. 4.2, the image lag occurred due to the hysteresis of the drive TFT (Q1). It was confirmed that the proposed driving method with the reset period did not cause the image lag that appears with a conventional architecture as shown in Fig. 4.9 (b).
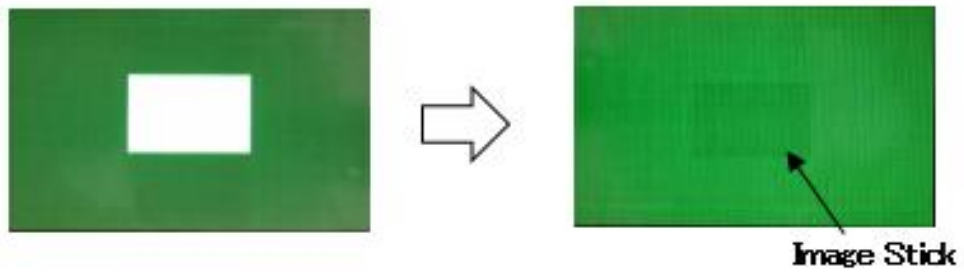
(a)　Without Reset Period in Fig. 3.11 and Fig. 4.2
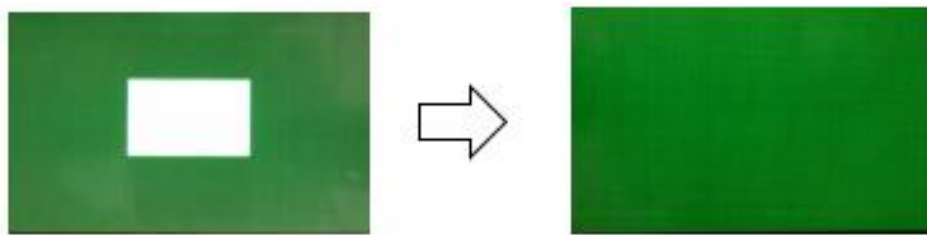
(b)　Proposed driving method in Fig. 3.11 and Fig. 4.2

Figure 4.9　Effect of Reset Period

Chapter 5

Review of Part I (Active Matrix)

In chapter 3 and 4, a self-sensing system was applied to an AM-OLED display as an active array matrix. This system is sensing of the V_{th} of TFT for a conventional the simplest pixel circuit ("2Tr1C" configuration) of AM-OLED displays. There is no extra elements and sensors inside in this pixel circuit. It involves two steps. First, source voltage of the drive TFT is quickly and precisely detected using only a current source under condition that carriers, namely holes, in the drive TFT are detrapped. Second, simple subtraction and one-bit-shift operation is executed using detected the source voltage of the drive TFT.

To evaluate the effectiveness of the proposed method, a prototype 3.8-inch 480×320-ppi OLED was built in chapter 4. From the V_{th}-distribution image, an offset signal for compensating V_{th} variation is generated, and variation of V_{th} is compensated by adding the offset signal to the data signal. It was confirmed that the OLED panel produces high-uniformity pictures when this compensation is applied.

This means that the self-sensing system can monitor not only the blob mura and around gap mura shown in Fig. 1.7 but also the analog characteristics of each cell (pixel) in cell array using the minimum sensor configuration (current source and voltage detector). That is, it was shown that a self-sensing system as shown in Fig. 1.10 was feasible.

Part Ⅱ

Application of a self-sensing system

of a passive array matrix

(Subtitle)

A sensing system for Fault-Diagnosis Architecture

for Large-scale Photovoltaic Power Plants that

does not require additional sensors

Chapter 6

Introduction of PV system

Self-sensing system was applied to the photovoltaic system that the power generated by a semiconductor array device is influenced by environmental parameters such as irradiation and temperature affect. Here, a cell, a module, a string, an array and an inverter are respectively expressed as a PV cell, a PV module, a PV string, a PV array and a PV inverter.

The environmental parameters to be sensed are irradiation and module temperature. Regarding manufacturing parameters, the number of PV cells, the series resistance and the shunt resistance in PV-array's equivalent circuit are estimated. In proposed self-sensing system, these parameters are estimated based on the difference between the measurement data and the semiconductor-array-device's ideal characteristic under sensed irradiation and temperature.

Large-scale photovoltaic (PV) system is promising power source of renewable energy. The operation of a large-scale PV power plants in Japan began with "Mega solar power generation plan" of Federation of Electric Power Companies of Japan (FEPC) in 2008. Further, Feed-in Tariff (FIT) was

enforced in 2012, the installation amount of PV has been phenomenal growth by increasing the scale of the PV power plants. In a large-scale PV power plant, PV modules are installed in units of tens of thousands.

The target of low-carbon society in SDGs is CO_2 reduction and it is required to install the many power plants of renewable energy such as the PV systems. In accelerating the amount of installation, the stable operation of the power plants over several tens to a hundred hectares for a long time is essential. The inspection of the electric power generation equipment in power plants needs much labor and large cost. However, these labor and cost cannot be sufficiently secured by the decrease the working-age population in the future. Therefore, advanced O&M management using IoT such as a remote monitoring system is expected [50].

The key issue is long-term reliability, that is, steady operation without any faults or performance degradation. For example, the overall degradation due to the increase in series resistance, reduction in power due to faulty PV modules, and potential induced degradation (PID) have been reported [51–56].

Faults that can occur at a PV power plant can be classified as PV or electrical. Many studies on these faults have been comprehensively conducted [57–59]. Techniques for preventing electrical faults have been developed and shown to be effective [58–59].

Techniques for detecting PV faults can also be classified [57]. Such techniques using sensors [60] and measurement methods [61] on PV modules

or strings are classified as output signal analysis techniques; however, implementation costs are much higher than that of simply replacing failed PV modules. Techniques [62–63] using wavelet packets are classified as machine learning techniques. More training data are needed to improve accuracy, but such data are not commonly available. To enable high-precision detection at low cost, a model-based difference measurement (MBDM) technique that compares real-time outputs with threshold values is commonly adopted, and the accuracy of PV models is important [57].

A fault-diagnosis architecture was developed that uses a new MBDM technique. As shown in Fig. 6.1, we firstly applied this architecture to PV system with sensors per two PV strings as the commercial products [64-65]. Many fault PV modules have been detected in about 5-6 years since start of the power-plant's operation. As shown in Fig. 6.2, the glass breakage of PV modules and wiring short caused by burnout etc. were timely detected in vast lands of PV power plants.
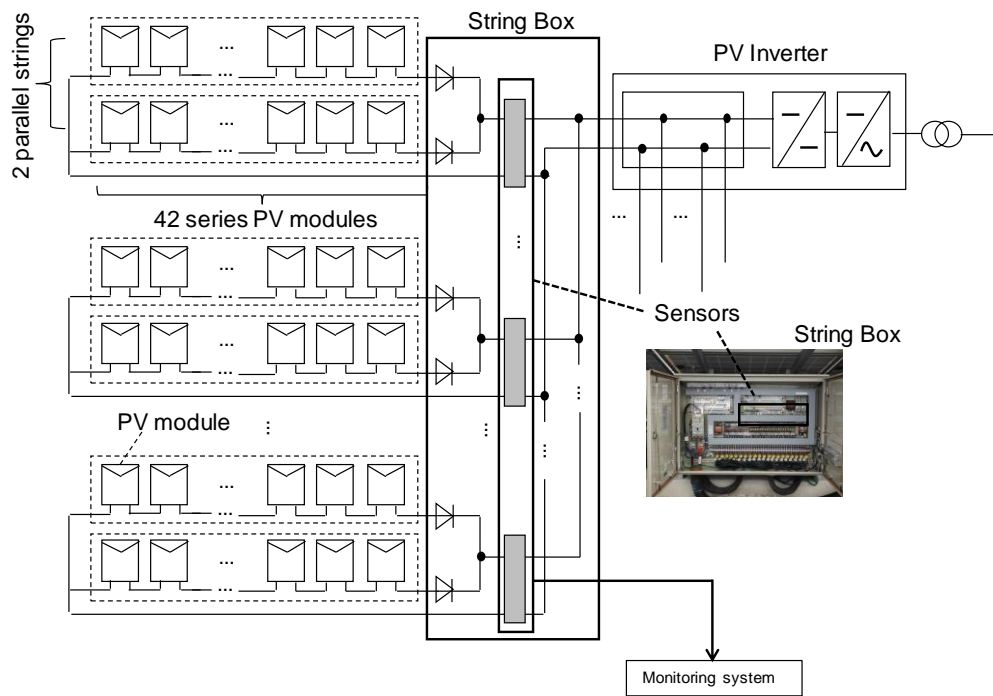
Figure 6.1 PV system with string sensors
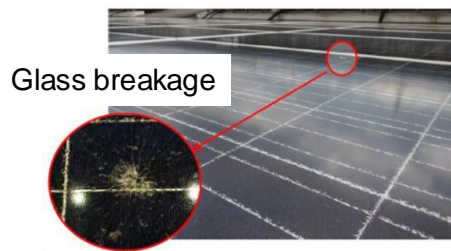
(a) Glass breakage of PV modules
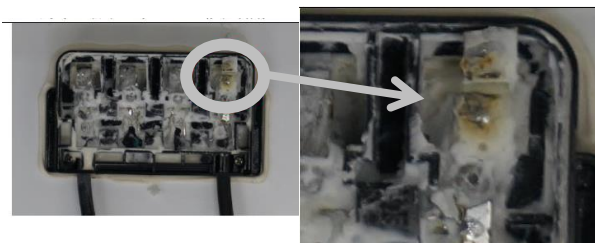
(b) Wiring short of junction box in PV module

Figure 6.2 The example of detected fault PV modules with sensors

However, in some cases, the failure rate of the equipped sensors is higher than the failure rate of PV modules. For example, all sensors in the string box are often completely failed after lightning strike. In addition, the circuit boards that equip the sensors corresponding to dozens of PV strings in string box must be exchanged at once.

In this study, the self-sensing system that does not require additional sensors shown in Fig. 1.7 was applied to PV system. It was experimentally demonstrated that this architecture can determine the number of faulty modules under maximum power point tracking (MPPT) without requiring additional sensors, i.e., by only using theoretical values for irradiation and module temperature calculated from the PV-module characteristics and measured DC voltage and current of a PV inverter.

It is common to increase power generation capacity on the DC side relative to AC side and force a PV inverter to clip of output power as shown in Fig. 6.3. In Fig. 6.3, after time0, the output is clipped and limited to 660 kW. If the output is clipped, the DC current and the DC voltage greatly changes as shown in Fig 6.3, and the point on the IV characteristic greatly changes. Therefore, the developed architecture has also a feature to calculate where the PV inverter is operating on the I-V curve when the output power of PV inverter is clipping.
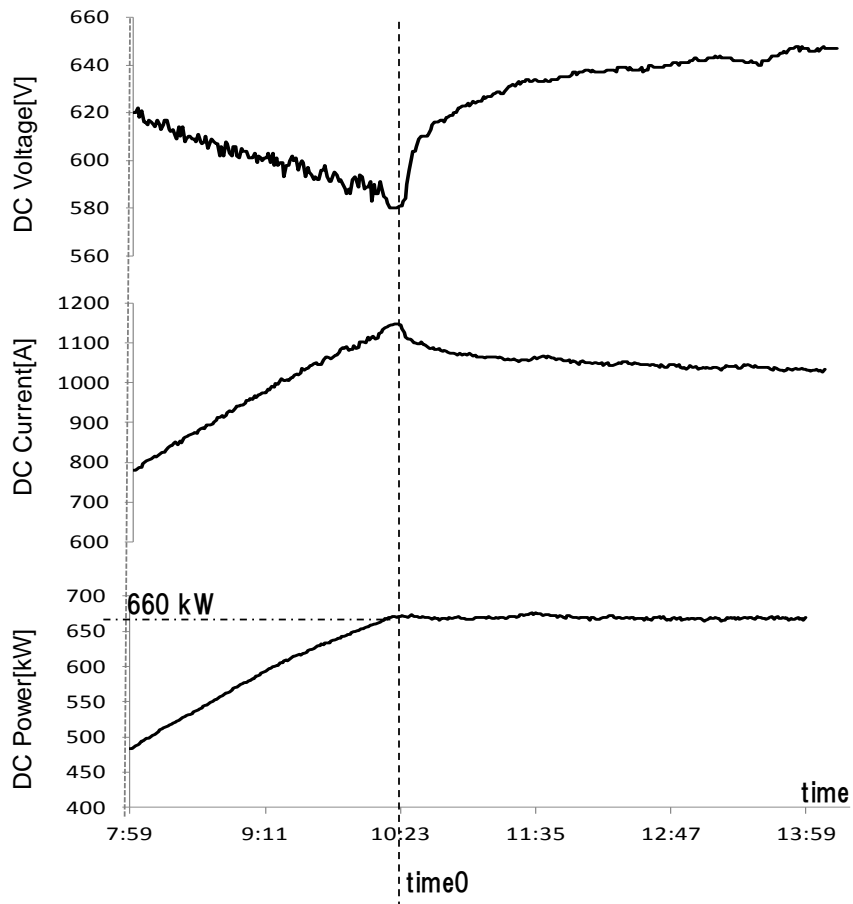
Figure 6.3 Clipping of output power of PV system

The key feature of this architecture is that solar radiation and temperature under both MPPT and clipping of output power are independently calculated from the measured DC voltage and current of a PV inverter using an improved PV model [66–69]. In other words, this is sensing architecture that the both environment parameter and the manufacturing parameter can be estimated while calculating the points on the IV characteristic of the semiconductor array device as shown in Fig. 1.11.

Chapter 7

Fault-Diagnosis Method

7.1 Schematic Diagram

A schematic of the improved architecture is shown in Fig. 7.1. The number of faulty modules in the PV array and degradation of the array's electrical performance are calculated by comparing the measured operating point of a PV inverter with that operating point estimated by improved the fault-diagnosis architecture using an analytical model [68–69]. This analytical model can accurately reproduce manufacturing variability, temperature coefficient, and power loss due to faulty modules under both MPPT and clipping of output power.

As shown in Fig. 7.2, the PV inverters are equipped in the outdoor package. Therefore, the failure of PV inverter's sensor rarely occurs against thunder strikes and typhoons.
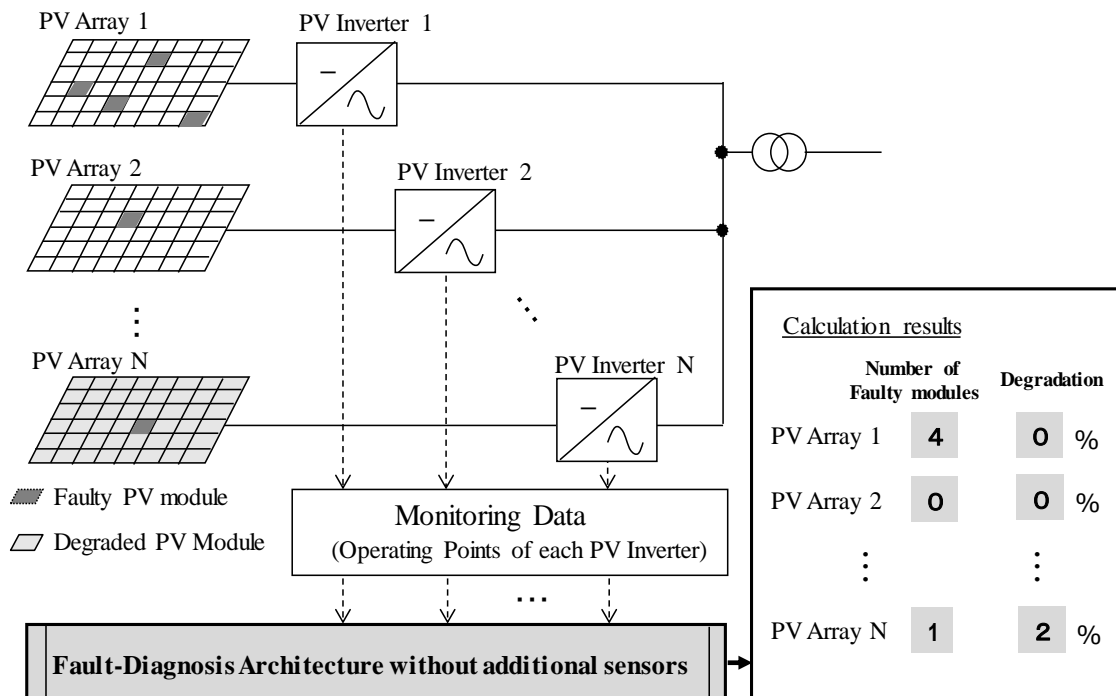
Figure 7.1 Schematic diagram of proposed architecture

Figure 7.2 Picture of outdoor package

7.2 Identification of Fault Mode

PV cells are the main components in PV module. However, these cells are not the only cause of degradation and faults in PV modules, with degradation of the cell connection wiring and filter material used in module

construction also being major factors.

Figure 7.3 shows cross sectional and bird's eye views of a PV module. The PV cells are connected in series by ribbons. Each ribbon is connected to a PV cell by soldering. PV cells are protected by filler consisting of ethylene-vinyl acetate copolymer between the glass and back sheet. The junction boxes are fitted with bypass diodes. In a commercial PV module, multiple units separated by a bypass diode are usually connected in series.
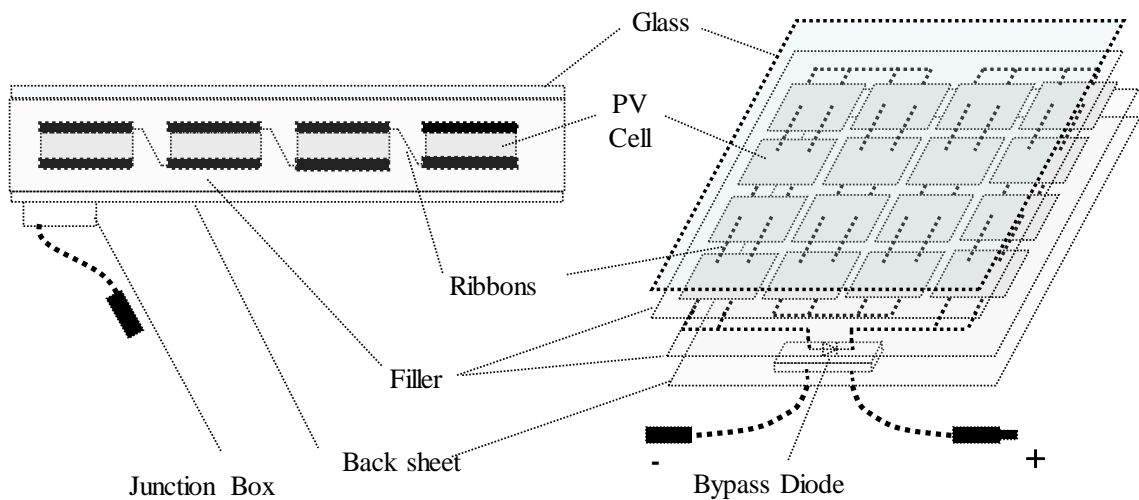
Figure 7.3 Cross sectional and bird's eye views of PV module

Because degradation or faults in these components are reflected in the equivalent circuit parameters of the PV cells, they can be identified quantitatively. An equivalent circuit of a PV module is shown in Fig. 7.4. Faults and degradation of these components are detected using the equivalent circuit parameters (series resistance: R_s, shunt resistance: R_{sh}, and bypass diode) of the PV module.
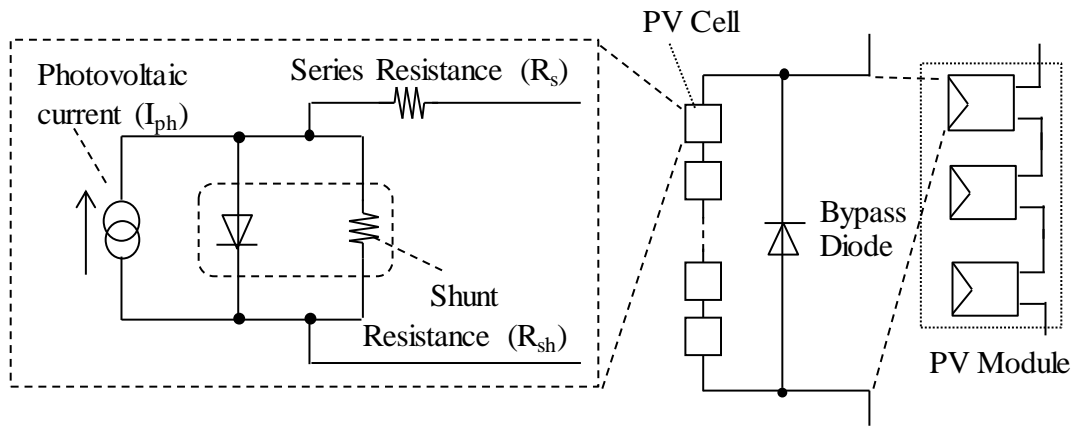
Figure 7.4　　Equivalent circuit of PV module

The PV module's faults and degradation can be roughly categorized into three fault modes. The increase in R_s reduces the fill factor [51]. This fault mode is defined as "series-resistance increase". If the p-n diode performance on the equivalent circuit decreases due to PID [53–56], the R_{sh} is equivalently reduced, resulting in electrical loss. This fault mode is defined as "shunt-resistance decrease". If the local performance deterioration is large, a bypass diode operates continuously and the voltage of the PV module is reduced to zero, also resulting in electrical loss [52]. The fault mode in which PV modules with zero voltage exist locally is defined as "bypass-diode on".

Each fault mode can occur due to multiple physical causes. The objective of this study was to determine the above-mentioned fault modes to understand the soundness of large-scale power plants during initial small power loss. For example, the I-V characteristics of a PV module with snail trails or cell microcracks caused by finger breakage increasing local series

resistance is considered a shunt-resistance decrease [70]. In our architecture, this is classified as "shunt-resistance decrease".

7.3 Calculation Method of Irradiation and Module Temperature

The key technique in proposed method is that, instead of utilizing the raw measurements from pyrheliometers and thermometers, it uses theoretical values for irradiation and module temperature calculated from the PV characteristics and measured operating points (DC voltage and DC current) of PV Inverter. This eliminates both the need to rely on an uncertain measurement from a pyrheliometer positioned at a representative location and also the need to estimate the module temperature from the air temperature. In this section, we describe the calculation methods of irradiation p_0 and module temperature T.

The distribution of the current flowing through each string connected to a PV inverter is determined by series-parallel equivalent circuit calculation [68]. If the faulty modules are set in an equivalent circuit of a PV array, the string current I_{pE} for diagnosis is determined corresponding to the fault modes and it is described in a previous study [68]. In normal state, I_{pE} is determined by dividing a DC current measured in a PV inverter by the number of PV strings.

As the DC voltage measured in a PV inverter is defined as V_{pE}, a

general equation of PV current is written as

$$I_{pE} = I_{ph} - I_s \cdot \exp\left(\frac{q \cdot \left(V_{pE} + I_{pE} \cdot (N_{cell} \cdot R_s)\right)}{N_{cell} \cdot n_f \cdot k \cdot T}\right) - \frac{\left(V_{pE} + I_{pE} \cdot (N_{cell} \cdot R_s)\right)}{R_{sh} \cdot N_{cell}} \qquad (7.1)$$

where I_{ph} is a photo current, q is elementary charge, N_{cell} is the number of cells of a PV string, n_f is the diode coefficient, k is the Boltzmann constant, I_s is the reverse saturation current, R_s is the series resistance per PV cell, and R_{sh} is the shunt resistance per PV cell.

The I_s can be expressed using Eq. (7.2) using the band gap E_{go} (= 1.205 eV).

$$I_s = A \cdot \exp\left(\frac{\left(\frac{-E_{go}}{q}\right) \cdot q}{k \cdot T}\right) \qquad (7.2)$$

where A is the saturation constant. The illuminated current and open-circuit voltage at 1 kW/m² are respectively defined as I_{ph0} and V_{oc0}. In normal state, R_{sh} can be regarded as sufficiently large, and Eq. (7.1) can be rewritten as

$$I_{ph0} = I_s \cdot \exp\left(\frac{q \cdot V_{oc0}}{N_{cell} \cdot n_f \cdot k \cdot T}\right) \qquad (7.3)$$

Solving equation (7.2) and equation (7.3), equation (7.4) can be obtained.

$$\ln(A) = \ln\left(I_{ph0}\right) + \left(\frac{q}{k} \cdot \frac{1}{T} \cdot \left(\frac{E_{go}}{q} - \frac{V_{oc0}}{n_f \cdot N_{cell}}\right)\right) \qquad (7.4)$$

The temperature coefficients of I_{ph0} and V_{oc0} are defined as α_0 (%/K) and β_0 (%/K) in the PV-module specifications, respectively. In a polycrystalline silicon PV module (for example, I_{ph0}=8.54 A, V_{oc0}=37 V, N_{cell}=60, n_f =1.8, β_0=-0.4%/K) in the temperature range -10 to 60 °C of a power plant, $\left(1/T \cdot \left(E_{go}/q - V_{oc0}/(n_f \cdot N_{cell})\right)\right)$ in Eq. (7.4) is 0.0028 mV/K and (q/k) is about 11460 K/mV; therefore, $\left(q/k \cdot 1/T \cdot \left(E_{go}/q - V_{oc0}/(n_f \cdot N_{cell})\right)\right)$ is about 32. The α_0 of I_{ph0} is 0.03–0.04 (%/K) and $\ln(I_{ph0})$ is 2.14, so the temperature dependence of $\ln(A)$ is negligibly small. We argue that the temperature characteristic due to minority-carrier injection in the p-n junction forming the semiconductor characteristics of PV is almost caused by $\exp(-E_{go}/kT)$ of Eq. (7.2) and saturation constant A can be considered as a constant.

The ratio of the DC current I_{pE} to I_{ph} can be expressed by Eq. (7.5). This ratio j can be defined as a variable indicating the location where a PV inverter is operating on the I-V curve. The advanced diagnosis during clipping of output power can be carried out by optimally setting j.

$$I_{ph} = \frac{I_{pE}}{j} \tag{7.5}$$

The third term of Eq. (7.1), namely, the current flowing through R_{sh}, is defined as I'_{pE}. By solving Eqs. (7.1), (7.2), and (7.5), T is calculated as

$$T = \frac{\frac{E_{go}}{q} - \frac{1}{n_f}\left(\frac{V_{pE}}{N_{cell}} + I_{pE} \cdot R_s\right)}{\frac{k}{q}} \cdot \left(1 \Big/ \ln\left(\frac{A}{\frac{I_{pE}}{j} - I_{pE} - I'_{pE}}\right)\right) \tag{7.6}$$

The I_{ph} under the standard condition (STC = 298 K, 1 kW/m2) is defined as I_{phs} and can be normally determined by the short-circuit current and open-circuit voltage in the module specifications and R_s as described in paper [57]. The p_0 can be expressed using I_{phs} and α_0 as

$$p_0 = I_{ph} \cdot \frac{1}{I_{phs} \cdot (1 + \alpha_0 \cdot (T-298)/100)} \qquad (7.7)$$

7.4 Calculation Method of operating point of PV inverter

In this section, we discuss the method of calculating where a PV inverter is operating on the I-V curve. Namely, the method described in this chapter can calculate where that PV inverter is operating on the current–voltage (I–V) curve when the output power of the PV inverter is clipping.

The measured V_{pE} and I_{pE} are first converted to V_{pE0} and I_{pE0} at 298 K, as shown in Fig. 7.5 (a). Then, V_{pE0} and I_{pE0} are converted to V_{p1} and I_{p1} under the STC, as shown in Fig. 7.5 (b).
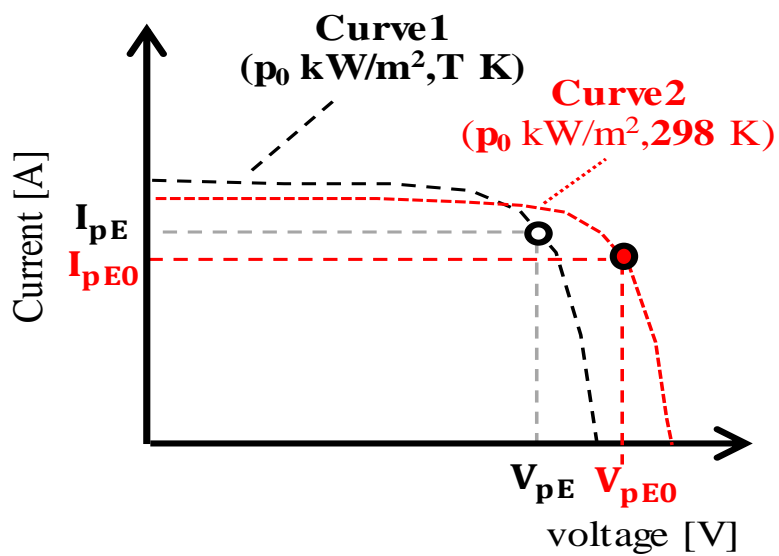
(a) Conversion to 298 K
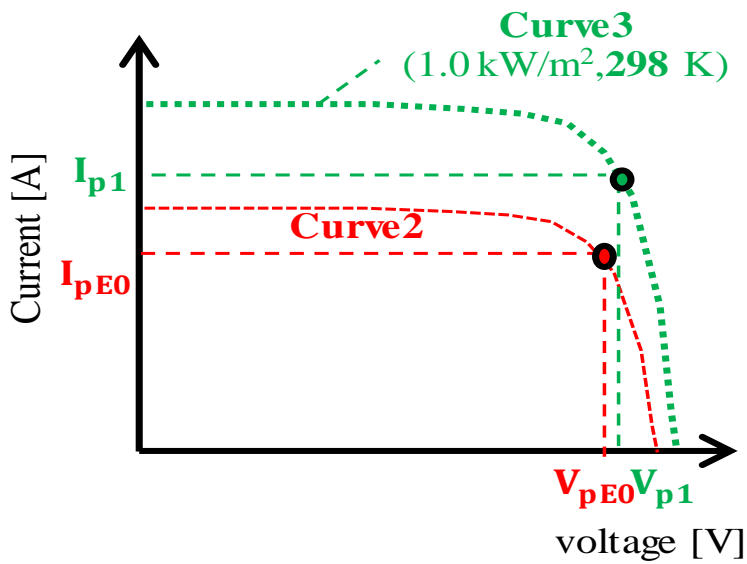
(b) Conversion to 1.0 kW/m²

Figure 7.5 Conversion of measured value of PV inverter to the point at STC

We first describe the conversion method of (V_{pE0}, I_{pE0}) of curve 2 from the measured data (V_{pE}, I_{pE}) of curve 1 in Fig. 7.5 (a). The current flowing through R_{sh} is defined as I'_{pE0}. By applying V_{pE0} and I_{pE0} to Eq. (7.6), Eq. (7.8) is written as.

$$298 = \frac{\frac{E_{go}}{q} - \frac{1}{n_f} \cdot \left(\frac{V_{pE0}}{N_{cell}} + I_{pE0} \cdot R_s \right)}{\frac{k}{q}} \cdot \left(1 / \ln \left(\frac{A}{I_{phs} \cdot p_0 - I_{pE0} - I'_{pE0}} \right) \right) \tag{7.8}$$

From Eqs. (7.6) and (7.8), considering that (k/q) is a constant, the following equation can be written.

$$\frac{\frac{E_{go}}{q} - \frac{1}{n_f} \cdot \left(\frac{V_{pE}}{N_{cell}} + I_{pE} \cdot R_s \right)}{T} \cdot \left(1 / \ln \left(\frac{A}{\frac{I_{pE}}{j} - I_{pE} - I'_{pE}} \right) \right)$$

$$= \frac{\frac{E_{go}}{q} - \frac{1}{n_f} \cdot \left(\frac{V_{pE0}}{N_{cell}} + I_{pE0} \cdot R_s \right)}{298} \cdot \left(1 / \ln \left(\frac{A}{I_{phs} \cdot p_0 - I_{pE0} - I'_{pE0}} \right) \right) \tag{7.9}$$

Here, $\left(V_{pE}/N_{cell} + I_{pE} \cdot R_s \right)$ shows the voltage of the p-n junction at T and $\left(V_{pE0}/N_{cell} + I_{pE0} \cdot R_s \right)$ shows the voltage of the p-n junction at 298 K. As shown in Fig. 7.6, the temperature coefficient ß of the p-n junction's voltage can be expressed as the voltage gradient with respect to temperature starting from E_{g0}/q. Furthermore, the voltage gradient of the value obtained by dividing the p-n junction's voltage by the diode constant can be expressed as ß'.
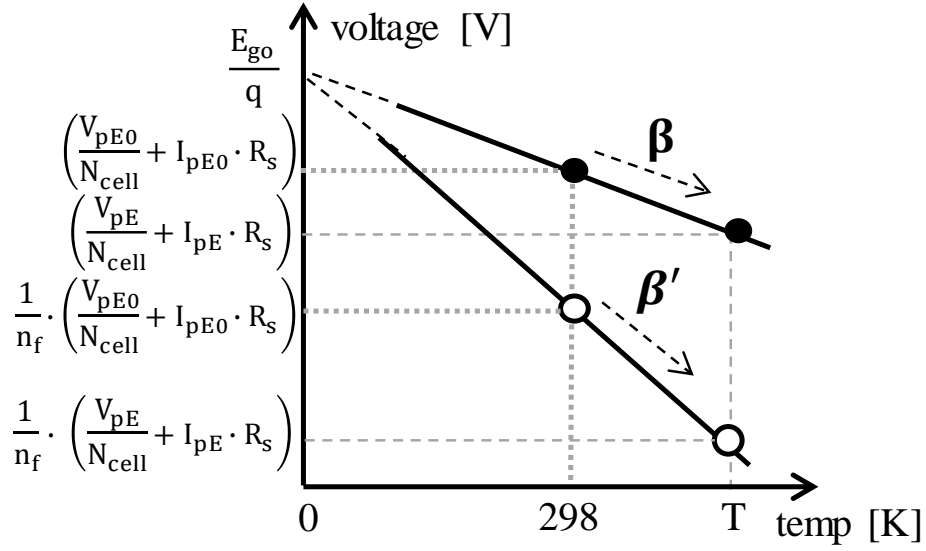
Figure 7.6   Temperature coefficient of p-n junction's voltage

Namely, β and β' of the p-n junction's voltage can be expressed by Eqs. (7.10)–(7.11).

$$-\beta = \frac{\frac{E_{go}}{q}-\left(\frac{V_{pE}}{N_{cell}}+I_{pE}\cdot R_s\right)}{T} = \frac{\frac{E_{go}}{q}-\left(\frac{V_{pE0}}{N_{cell}}+I_{pE0}\cdot R_s\right)}{298} \tag{7.10}$$

$$-\beta' = \frac{\frac{E_{go}}{q}-\frac{1}{n_f}\cdot\left(\frac{V_{pE}}{N_{cell}}+I_{pE}\cdot R_s\right)}{T} = \frac{\frac{E_{go}}{q}-\frac{1}{n_f}\cdot\left(\frac{V_{pE0}}{N_{cell}}+I_{pE0}\cdot R_s\right)}{298} \tag{7.11}$$

By substituting Eqs. (7.5), (7.7), and (7.10) into Eq. (7.9), I_{pE0} can be expressed by Eq. (7.12) and V_{pE0} can be expressed by Eq. (7.13) obtained by modifying Eq. (7.11). The third term $(I'_{pE0} - I'_{pE})$ of Eq. (7.12) may be small and negligible. To obtain the value of this term more accurately, the initial $(I'_{pE0} - I'_{pE})$ is first set to zero. The I_{pE0} and V_{pE0} calculated using Eqs. (7.12) and (7.13) are applied to Eq. (7.1) and initial I'_{pE0} is determined. Next, using calculated $(I'_{pE0} - I'_{pE})$, I_{pE0} and V_{pE0} are calculated using Eqs. (7.12) and (7.13). The I_{pE0}

and V_{pE0} are applied to Eq. (7.1), and I'_{pE0} is estimated again. By this convergence calculation, accurate I_{pE0} and V_{pE0} can be obtained.

$$I_{pE0} = \frac{I_{pE}}{j} \cdot \left(\frac{1}{1+\propto_0 \cdot (T-298)/100} - 1\right) + I_{pE} - (I'_{pE0} - I'_{pE}) \tag{7.12}$$

$$V_{pE0} = V_{pE} + N_{cell} \cdot \left(\beta \cdot (298 - T) + \left(I_{pE} - I_{pE0}\right) \cdot R_s\right) \tag{7.13}$$

Next, we describe the conversion method of (V_{p1}, I_{p1}) of curve 3 from (V_{pE0}, I_{pE0}) of curve 2 in Fig. 7.4 (b). The ratio of the DC current I_{pE0} to I_{phs} is denoted as j_0.

$$j_0 = I_{pE0}/\left(I_{phs} \cdot p_0\right) \tag{7.14}$$

Figure 7.7 (a) shows the circuit schematic for PSIM (software for power electronics simulation) to calculate the dependence of j_0 on p_0. The single diode model [57] is adopted as a PV model. The PV string model is represented by a series connection of single diode models separated by bypass diodes. While sweeping the voltage of the PV array in which multiple PV strings are connected in parallel, the current and power of the PV array are calculated.

As mentioned above, I_{phs} is normally estimated from short-circuit current, open-circuit voltage, and R_s under the STC [57]. The I_{phs} multiplied by the number of PV strings is defined as I'_{phs}. Figure 7.7 (b) shows an example of the simulation results. The ratio of the current at the maximum power point (MPP) I_{p1a} to I'_{phs} is denoted as j_{0a}, and that of the current at the point of outputting 60% of maximum power I_{p1b} to I'_{phs} is defined as j_{0b}.
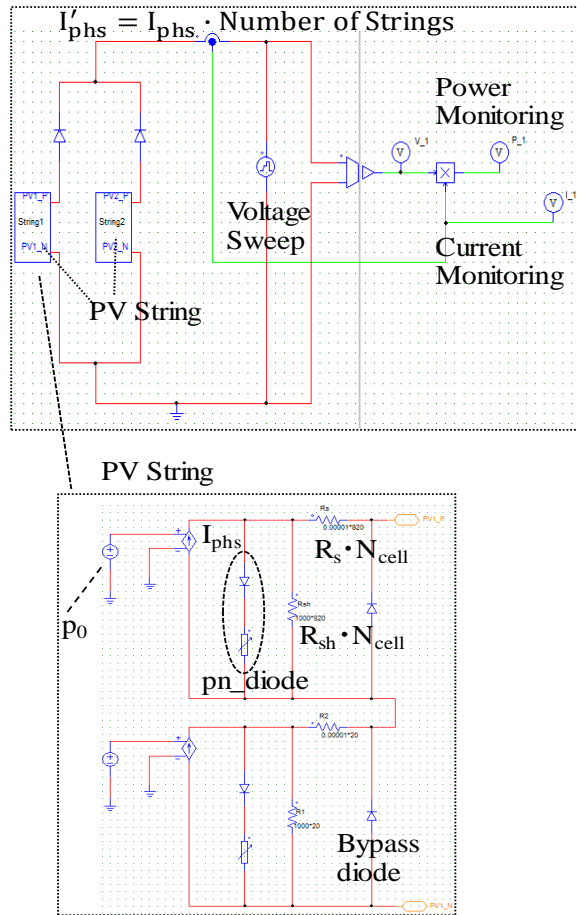
(a) Simulation circuit (PSIM)
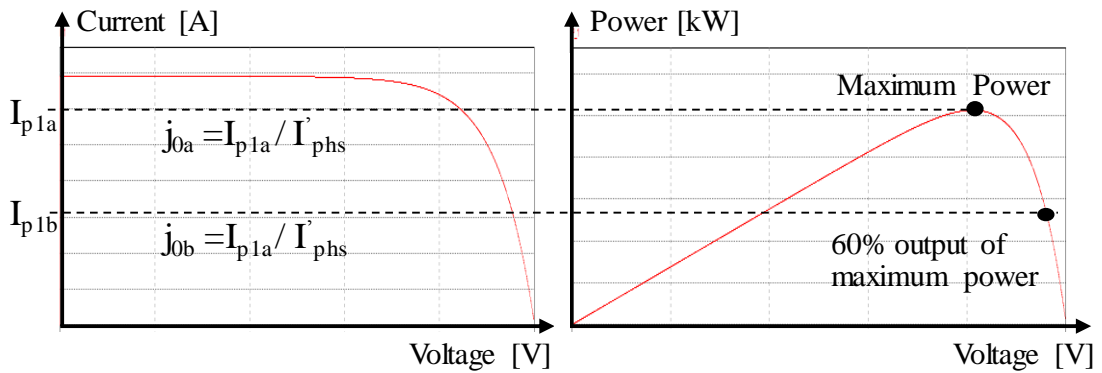
(b) Simulation result

Figure 7.7. Example of simulation circuit and results for PV model analysis

Figure 7.8 (a) shows the relationship between the j_{0a} and p_0. Similarly, Figure 7.8 (b) shows the relationship between j_{0b} and p_0. From these results, j_{0a} and j_{0b} can be regarded as a constant value if p_0 is more than 0.38 kW/m^2 at 298 K.
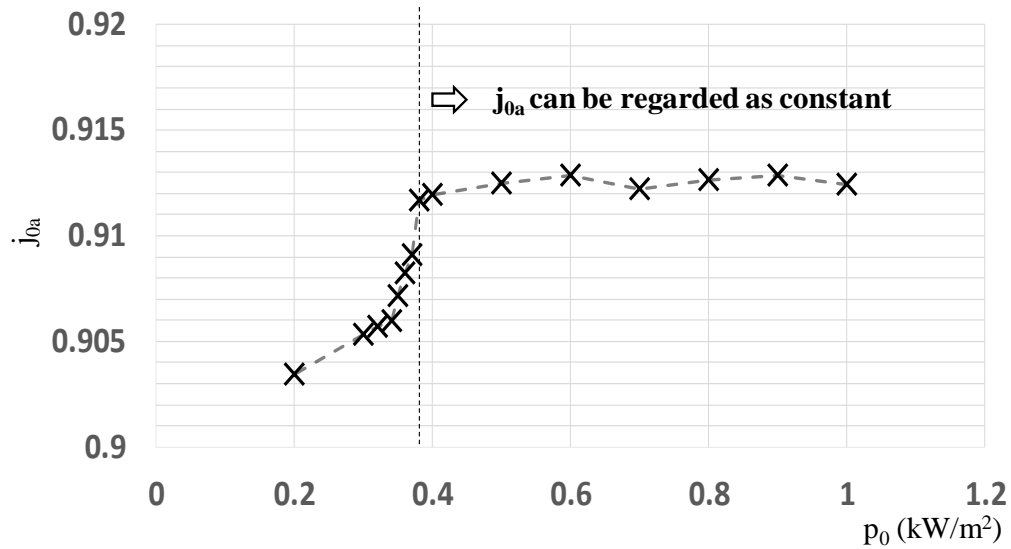
(a)　Ratio at maximum power point (MPP)
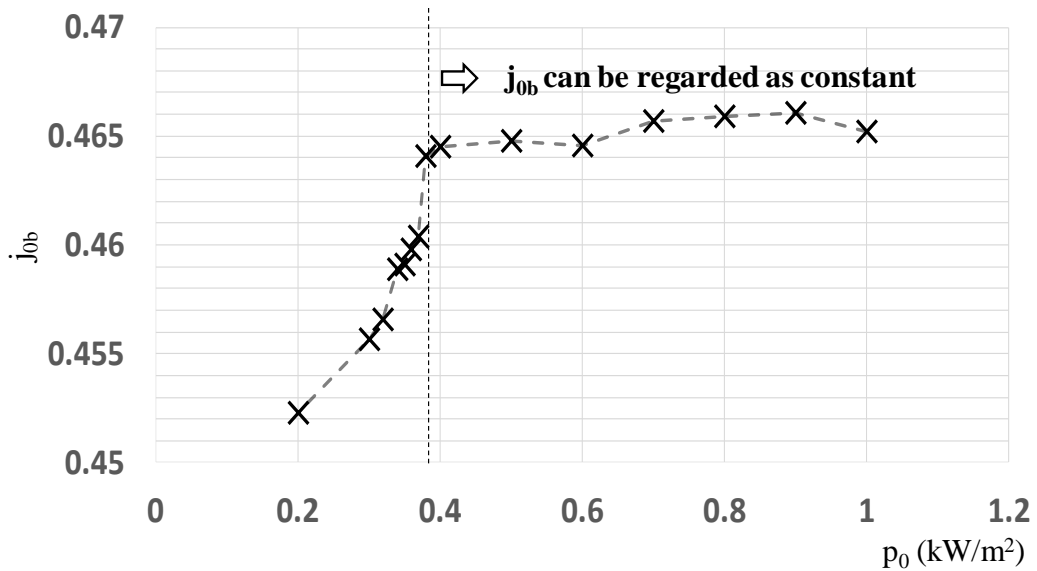
(b)　Ratio at point of outputting 60% of MPP

Figure 7.8. Dependence of ratio of DC current I_{pE0} to illuminated current I_{phs} (j_0) on irradiance p_0

Using j_0 as the constant regardless of p_0, I_{pE0} and V_{pE0} at 298 K and p_0 kW/m² are converted to I_{p1} and V_{p1} under the STC.

$$I_{p1} = I_{phs} \cdot j_0 \tag{7.15}$$

The current flowing through R_{sh} is defined as I'_{p1} expressed by Eq. (7.16). The difference between V_{p1} and V_{pE0} can be calculated by solving Eq. (7.1) regarding V_{p1} and V_{pE0}. As a result, V_{p1} is expressed by Eq. (7.17).

$$I'_{p1} = \frac{\left(V_{p1} + I_{p1} \cdot (N_{cell} \cdot R_s)\right)}{R_{sh} \cdot N_{cell}} \tag{7.16}$$

$$
\begin{aligned}
V_{p1} = {} & V_{pE0} - N_{cell} \cdot \frac{n_f \cdot k \cdot 298}{q} \cdot \ln\left(\frac{p_0 \cdot I_{phs} \cdot (1 - j_0) - I'_{pE0}}{I_{phs} \cdot (1 - j_0) - I'_{p1}}\right) \\
& + N_{cell} \cdot R_s \cdot I_{phs} \cdot j_0 \cdot (1 - p_0)
\end{aligned}
$$

$$\tag{7.17}$$

First, I'_{p1} is initialized to zero and V_{p1} is calculated using Eq. (7.17). Next, I'_{p1} is expressed by Eq. (7.16), after that V_{p1} is expressed by Eq. (7.17) again. By this convergence calculation, accurate V_{p1} can be obtained.

The voltage of the p-n junction per PV cell under the STC V_{jc} is expressed by Eq. (7.18). By substituting V_{jc} into Eqs. (7.1) and (7.2), Eq. (7.19) is written as

$$V_{jc} = \frac{1}{N_{cell}} \cdot V_{p1} + R_s \cdot I_{phs} \cdot j_0 \tag{7.18}$$

$$I_{p1} = I_{phs} - A \cdot \exp\left(\frac{\left(\frac{-E_{go}}{q}\right) \cdot q}{k \cdot 298}\right) \cdot \exp\left(\frac{q \cdot V_{jc}}{n_f \cdot k \cdot 298}\right) - \frac{V_{jc}}{R_{sh}}$$

$$= I_{phs} - A \cdot \exp\left(\frac{-q \cdot \left(\frac{E_{go}}{q} - \frac{V_{jc}}{n_f}\right)}{k \cdot 298}\right) - \frac{V_{jc}}{R_{sh}} \tag{7.19}$$

When I_{p1} is differentiated with respect to V_{jc}, Eq. (7.20) is written as

$$\frac{\partial I_{p1}}{\partial V_{jc}} = \frac{-1 \cdot q}{k \cdot 298} \cdot A \cdot \exp\left(\frac{-q \cdot \left(\frac{E_{go}}{q} - \frac{V_{jc}}{n_f}\right)}{k \cdot 298}\right) - \frac{1}{R_{sh}} \tag{7.20}$$

By defining the output power under the STC as P_{jc}, the differentiation of P_{jc} with respect to V_{jc} is calculated using Eq. (7.21).

$$\frac{\partial P_{jc}}{\partial V_{jc}} = \frac{\partial (I_{p1} \cdot V_{jc})}{\partial V_{jc}} = I_{p1} + V_{jc} \cdot \frac{\partial I_{p1}}{\partial V_{jc}} \tag{7.21}$$

The optimization function of combining j_0, $\partial I_{p1}/\partial V_{jc}$, and $\partial P_{jc}/\partial V_{jc}$ is built into the advanced fault-diagnosis flow discussed in the next section.

7.5 Diagnosis Flow

The power generated by a large PV plant in one day can be divided into two time zones, as shown in Fig. 7.9. In time zone 1, a PV inverter operates under maximum power point tracking (MPPT). In time zone 2, the DC power clips and kept constant because it is common to increase power generation capacity on the DC side relative to AC side of the PV inverter.
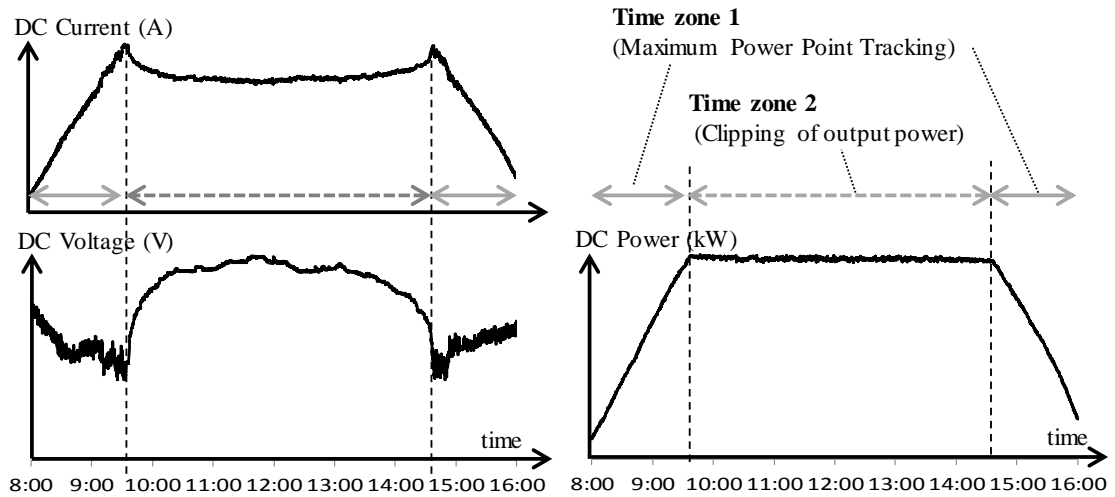
Figure 7.9. Daily PV power generation that can be divided into two time zones

The fault-diagnosis flow is shown in Fig. 7.10. The DC voltage and current measured in each PV inverter are transmitted to the monitoring system of the power plant. The DC current and voltage data in one day consists of hundreds of points corresponding to at least every minute. The time zones to be analyzed are selected as pre-processing. In a large-scale plant, the position of a building or tower's shadow is calculated beforehand. The data during the period when the loss due to shading occurs is discarded during this pre-processing. Furthermore, the data, in which the current changes in one minute is larger than the predetermined amount, are also discarded. The data in which DC power is clipping is classified as time zone 2.   The data of DC power corresponding to p_0 larger than 0.38 kW/m^2 is classified as time zone 1 from the remaining valid data.
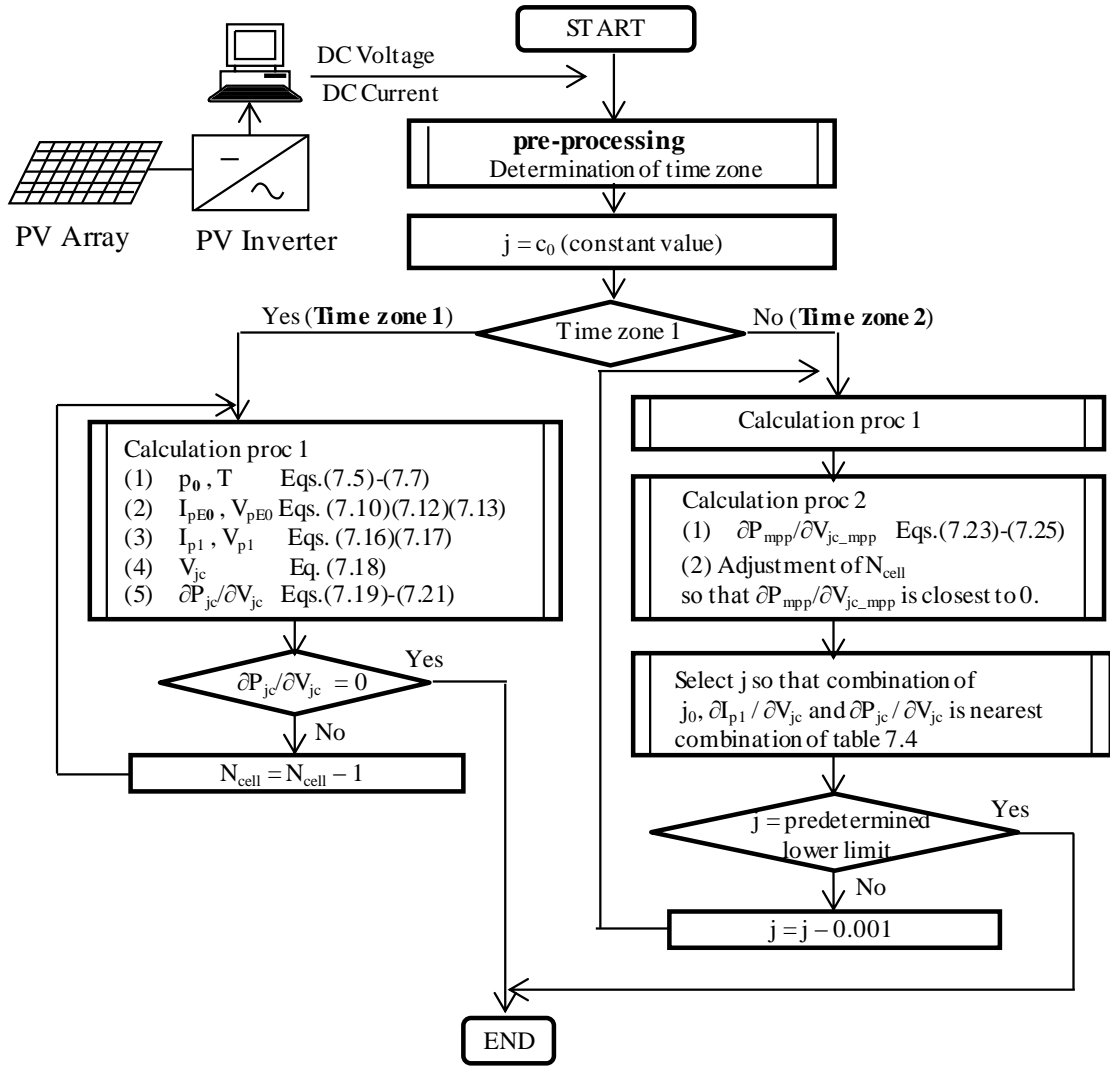
Figure 7.10. Fault-diagnosis flow for time zones 1 and 2

The fault-diagnosis flow is explained using a sample of measurement data obtained in the large-scale PV plant. Table 7.1 shows the PV-module parameters of this sample. The parameters of the polycrystalline silicon PV module are I_{ph0}=8.64 A, V_{oc0}=37.1 V, N_{cell}=60, n_f=1.73, A=1.01e+15, R_{sh}=1000 Ω, and R_s=1.5e-3 Ω. The operating current I_{op} and operating voltage V_{op} described in the specification sheet are 8.08 A and 30.3 V, respectively; thus,

the output rating of the PV module is 245 W. It was confirmed from the PSIM simulation that the parameters in Table 7.1 match those of the single-diode model in a previous study [57]. In a PV system, a PV array consisting of 100 parallel PV strings is connected to a PV inverter. A PV string consists of 14 PV modules (if the unit separated by a bypass diode is defined as a cluster, a PV strings consists of 42 series clusters.) The total output is 343 kW and clipping occurs near 259 kW. The measured data of the PV inverter at time zones 1 and 2 are listed in Table 2. To simulate faults, corrugated plastic sheets as shown in Fig. 7.11 are randomly placed on the modules in a PV array that is equivalent to faults of 100 clusters. A cluster consists of 20 PV cells. Transmittance of corrugated plastic sheets is 25%. If corrugated plastic is placed on a PV cluster, the current of this PV cluster flows through the bypass diode to simulate the "bypass diode on" mode.
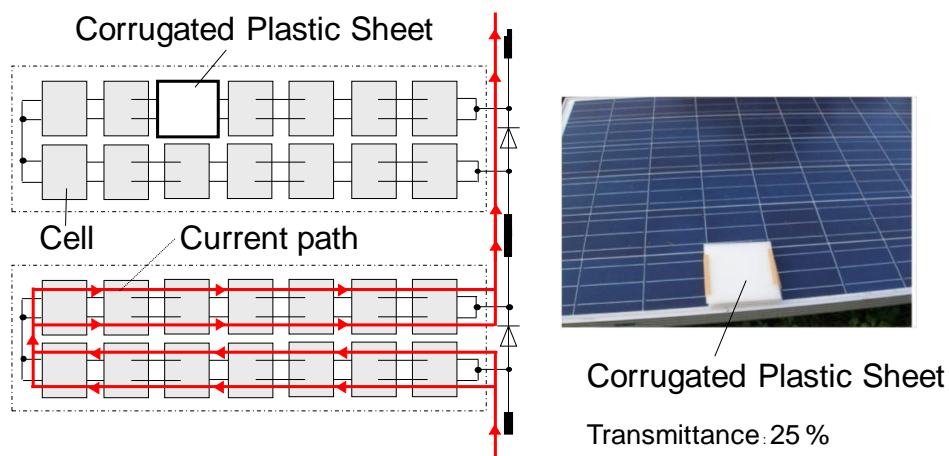
Figure 7.11 Corrugated Plastic Sheets assigned to the modules in a PV array

Table 7.1. PV module's parameter at STC

PV module's Parameters under standard condition (1.0 kW/m², 298 K)	
Illuminated current (I_{phs}) : 8.64 [A]	Saturation constant (A) : 1.01e+15
Temperature variation (α_0) : 0.04 [%/℃]	Shunt resistance (R_{sh}) : 1000 [Ω/cell]
Open circuit voltage (V_{oc}) : 37.1 [V]	Series resistance (R_s) : 0.0015 [Ω/cell]
Number of PV cells (N_{cell}) : 60	Operating current (I_{op}) : 8.08 [A]
Diode coefficient (n_f) : 1.73	Operating voltage (V_{op}) : 30.3 [V]

Table 7.2. Measured data of PV inverter

Time zone 1		Time zone 2	
DC voltage	DC current	DC voltage	DC current
378.8 V	**619.3** A	**410.4** V	**631.5** A

The V_{pE} and I_{pE} at time zones 1 and 2 are respectively (378.8 V, 6.193 A) and (410.4 V, 6.315 A). An optionally specified j is first set, and T and p_0 are calculated using Eqs. (7.5)–(7.7) by using I_{pE} and V_{pE}.

Next, I_{pE0} and V_{pE0} are calculated using Eqs. (7.10), (7.12), and (7.13), and j_0 is estimated using Eq. (7.14). As shown in Fig. 7.8 (a), j_0 at MPPT can be regarded as a constant value c_0. Therefore, at time zone 1 of MPPT, I_{p1}, V_{p1}, and V_{jc} can be estimated using Eqs. (7.16), (7.17), and (7.18) using c_0 instead of j_0.

The $\partial P_{jc}/\partial V_{jc}$ calculated using Eqs. (7.19)–(7.21) at MPPT should be zero because it is an inflection point with respect to voltage. Namely, calculation flow is repeated until $\partial P_{jc}/\partial V_{jc}$ nearly equals zero while N_{cell} is

varied. Since N_{cell} is the number of cells per PV string, the number of faulty cells applied to the PV array is equivalent to N_{cell} multiplied by the number of PV strings.

The experimental results of the sample data at time zone 1 are listed in Table 7.3. When N_{cell} is 823, $\partial P_{jc}/\partial V_{jc}$ becomes zero and the number of faulty cells can be 1700 (17×100). This corresponds to 85 (1700/20) faulty clusters, which matches the number of simulated faults (=100).

Table 7.3. Results of sample data at time zone 1

Ncell	p_0 [kW/m²]	$T[℃]$	I_{pE0} [A]	V_{pE0} [V]	I_{p1} [A]	V_{p1} [V]	$\partial I_{p1}/\partial V_{jc}$	$\partial P_{p1}/\partial V_{jc}$
840（60×14）	0.765	31.08	6.18	391.4	8.08	399.1	-14.7	**0.93**
839	0.765	30.98	6.18	391.2	8.08	398.9	-14.8	**0.88**
830	0.765	30.07	6.18	389.1	8.08	396.8	-15.6	**0.42**
825	0.765	29.55	6.18	388.0	8.08	395.6	-16.1	**0.14**
823	0.765	29.34	6.18	387.5	8.08	395.1	-16.4	**0.00**
822	0.765	29.24	6.18	387.3	8.08	394.9	-16.5	**-0.03**
821	0.765	29.13	6.18	387.1	8.08	394.6	-16.6	**-0.10**

$j_0 = 0.935$

It should be noted that the combinations of j_0, $\partial I_{p1}/\partial V_{jc}$ and $\partial P_{jc}/\partial V_{jc}$ are uniquely determined. Table 7.4 shows this combination calculated from the I-V characteristics under the STC described in the PV module specifications. Fault diagnosis at time zone 2 is executed using Table 7.4. As in the diagnosis at MPPT, T and p_0 are first calculated by setting a specified j and applying I_{pE} and V_{pE} to Eqs. (7.5)–(7.7). Next, j_0, $\partial I_{p1}/\partial V_{jc}$ and $\partial P_{jc}/\partial V_{jc}$ are calculated using Eqs. (7.10)–(7.21). The j is determined so that it is closest

to the calculated combination and the combinations in Table 7.4. While determining j, STC current I_{mpp}, STC voltage V_{jc_mpp} of p-n junction at MPPT and $\partial P_{mpp}/\partial V_{jc\_mpp}$ are obtained using V_{jc} and j_0 as

$$I_{mpp} = I_{phs0} \cdot c_0 \tag{7.22}$$

$$
\begin{aligned}
V_{jc\_mpp} &= V_{jc} + \left(V_{jc\_mpp} - V_{jc}\right) \\
&= V_{jc} + \left(\frac{n_f \cdot k \cdot 298}{q} \ln\left(\frac{I_{phs} \cdot (1-c_0)}{I_s}\right) - \frac{n_f \cdot k \cdot 298}{q} \ln\left(\frac{I_{phs} \cdot (1-j_0)}{I_s}\right)\right) \\
&= V_{jc} + \left(\frac{n_f \cdot k \cdot 298}{q} \ln\left(\frac{1-c_0}{1-j_0}\right)\right)
\end{aligned}
\tag{7.23}
$$

$$
\begin{aligned}
I_{mpp} &= I_{phs} - A \cdot \exp\left(\frac{\left(\frac{-E_{go}}{q}\right) \cdot q}{k \cdot 298}\right) \cdot \exp\left(\frac{q \cdot V_{jc\_mpp}}{n_f \cdot k \cdot 298}\right) - \frac{V_{jc\_mpp}}{R_{sh}} \\
&= I_{phs} - A \cdot \exp\left(\frac{-q \cdot \left(\frac{E_{go}}{q} - \frac{V_{jc\_mpp}}{n_f}\right)}{k \cdot 298}\right) - \frac{V_{jc\_mpp}}{R_{sh}}
\end{aligned}
\tag{7.24}
$$

$$\frac{\partial P_{mpp}}{\partial V_{jc\_mpp}} = \frac{\partial\left(I_{mpp} \cdot V_{jc\_mpp}\right)}{\partial V_{jc\_mpp}} = I_{mpp} + V_{jc\_mpp} \cdot \frac{\partial I_{mpp}}{\partial V_{jc\_mpp}} \tag{7.25}$$

Table 7.4. Combination of j_0, $\partial I_{p1}/\partial V_{jc}$ and $\partial P_{jc}/\partial V_{jc}$ calculated from STC I-V

j_0	$\partial I_{p1}/\partial V_{jc}$	$\partial P_{jc}/\partial V_{jc}$		j_0	$\partial I_{p1}/\partial V_{jc}$	$\partial P_{jc}/\partial V_{jc}$		j_0	$\partial I_{p1}/\partial V_{jc}$	$\partial P_{jc}/\partial V_{jc}$
0.94	−15.43	0.72		0.9	−25.71	−5.20		0.89	−28.29	−6.71
0.939	−15.69	0.58		0.899	−25.97	−5.35		0.889	−28.54	−6.86
0.938	−15.94	0.43		0.898	−26.23	−5.50		0.888	−28.80	−7.02
0.937	−16.20	0.29		0.897	−26.49	−5.65		0.887	−29.06	−7.17
0.936	−16.46	0.14		0.896	−26.74	−5.80		0.886	−29.32	−7.32
0.935	−16.71	0.00		0.895	−27.00	−5.95		0.885	−29.57	−7.47
0.934	−16.97	−0.15		0.894	−27.26	−6.10		0.884	−29.83	−7.63
0.933	−17.23	−0.29		0.893	−27.51	−6.26		0.883	−30.09	−7.78
0.932	−17.49	−0.44		0.892	−27.77	−6.41		0.882	−30.34	−7.93
0.931	−17.74	−0.58		0.891	−28.03	−6.56		0.881	−30.60	−8.08

where $\partial(P_{mpp})/\partial V_{jc\_mpp}$ should be also zero. Therefore, the calculation flow from the setting of j is repeated until $\partial(P_{mpp})/\partial V_{jc\_mpp}$ nearly equals zero while N_{cell} is varied.

The experimental results of the sample data at time zone 2 are listed in Table 7.5. The differences between $(\partial I_{p1}/\partial V_{jc},\ \partial P_{jc}/\partial V_{jc})$ in Table 7.4 and that in Table 7.5 are denoted as $(\Delta(\partial I_{p1}/\partial V_{jc})$ and $\Delta(\partial P_{jc}/\partial V_{jc}))$, respectively. When j and N_{cell} are set to 0.885 and 829, respectively, $\Delta(\partial I_{p1}/\partial V_{jc})$ and $\Delta(\partial P_{jc}/\partial V_{jc})$ are the lowest. Namely, the number of faulty cells at time zone 2 can be 1100 (11×100). This corresponds to 55 (1100/20) clusters, it means that simulated faults can be detected sufficiently.

Table 7.5. Result of sample data at time zone 2

j	p_0 [kW/m²]	T[℃]	I_{pE0} [A]	V_{pE0} [V]	I_{p1} [A]	V_{p1} [V]	$\partial I_{p1}/\partial V_{jc}$	$\partial P_{p1}/\partial V_{jc}$	Ncell	$\Delta(\partial I_{p1}/\partial V_{jc})$	$\Delta(\partial P_{p1}/\partial V_{jc})$
0.935	0.782	24.2	6.32	408.7	8.08	415.7	-22.72	-3.44	840	- 6.01	-3.44
0.900	0.811	28.2	6.31	416.7	7.77	422.3	-26.77	-6.00	840	- 1.06	- 0.80
0.890	0.820	28.2	6.31	416.6	7.69	421.7	-29.29	-7.50	832	- 1.01	- 0.79
0.887	0.823	28.2	6.31	416.7	7.66	421.6	-30.00	-7.92	830	-0.93	- 0.74
0.885	0.825	28.3	6.31	416.8	7.65	421.6	-30.40	-8.16	829	- 0.82	- 0.69
0.884	0.826	28.3	6.31	416.7	7.64	421.5	-30.71	-8.34	828	- 0.87	-0.71
0.883	0.827	28.2	6.31	416.6	7.62	421.4	-31.02	-8.53	827	- 0.92	-0.75

$\partial P_{mpp}/\partial V_{jc} \fallingdotseq 0$

7.6 Identification of Fault Mode

The operation of PV power plants is normally automated and unattended. Consequently, if fault or degradation occurs, it may take a long time for them to identify them, resulting in a long-term output loss and an increased risk of a more serious fault. Therefore, we developed a method for remotely determining the fault mode.

This method estimates the equivalent circuit parameter of a PV module with fault or degradation. For example, checking the decrease in R_{sh} will be effective for early detection of PID, which causes long-term performance degradation.

Figure 7.12 shows the examples of calculation result of PV string characteristics in each fault mode. Figure 7.13 shows the relationship between p_0 and calculated power loss in each faulty mode. These are the results from the PSIM simulation conducted on the circuit shown in Fig. 7.7 (a). All p_0 of normal PV-module models were swept from 0.38 to 1.0 kW/m^2, and the power loss was estimated.

If the fault mode is "bypass-diode on", p_0, namely, the current source values of the PV-module models with fault setting, are set to zero and the bypass diodes of the PV-module models with fault setting are turned on. The power loss is dependent on the number of PV cells with the bypass diodes turned on and has the same value regardless of the output power, as shown in pattern 1 and Fig, 7.12(a).

In "series-resistance increase", the R_s of all PV-module models in Fig.

7.7 (a) are set to 0.0024 Ω. A voltage drops due to R_s and corresponding current decrease causes power loss that is proportional to the current. Namely, power loss increases as the output (p_0) increases, as shown in pattern 2 and Fig, 7.12 (b).

If the fault mode is "shunt-resistance decrease", the R_{sh} of all PV-module models in Fig. 7.7 (a) are set to 3.33 Ω. The current flowing through R_{sh} is leakage current and the ratio of this leakage current to PV diode current increases with decreasing p_0. Namely, power loss increases as the output decrease, as shown in pattern 3 and Fig, 7.12(c).
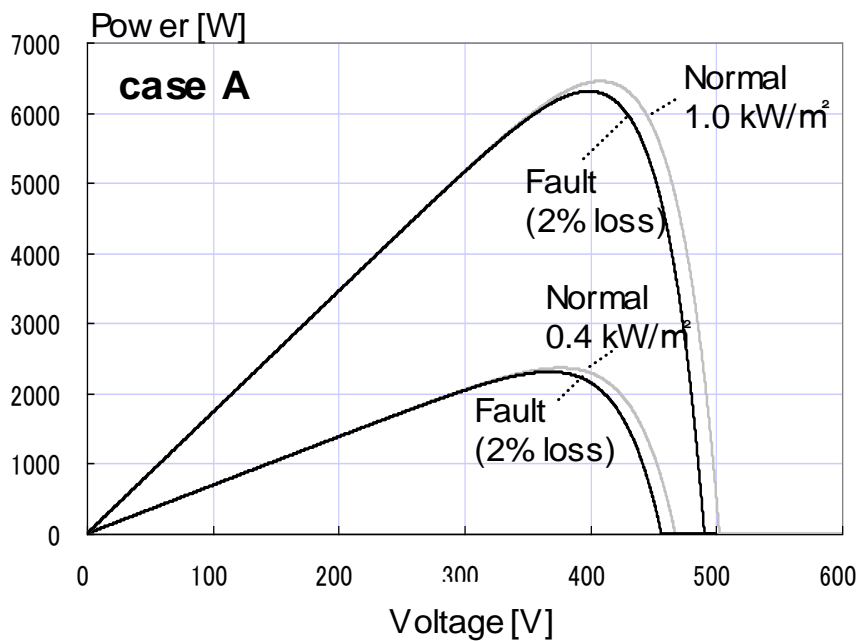
(a) bypass-diode on
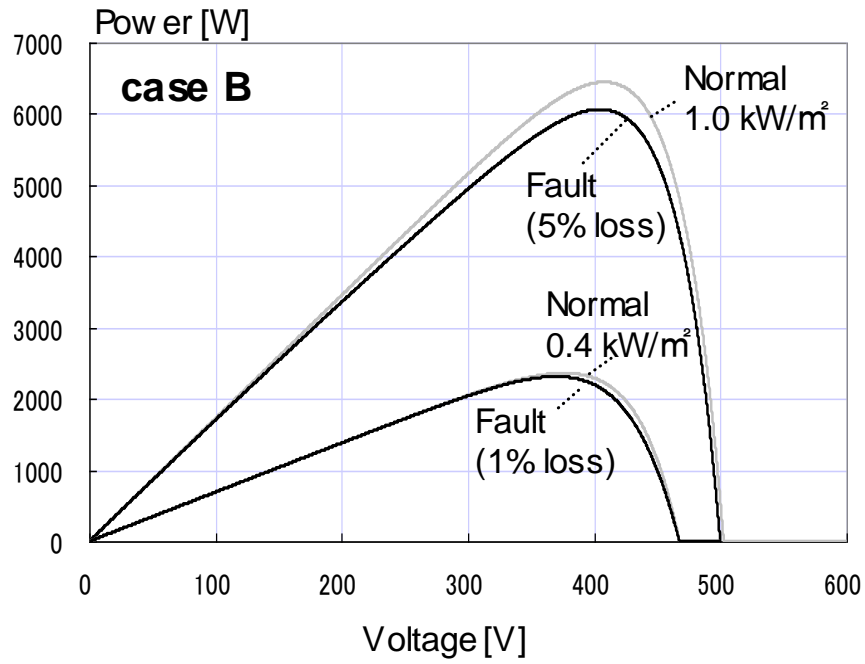
(b) series-resistance increase
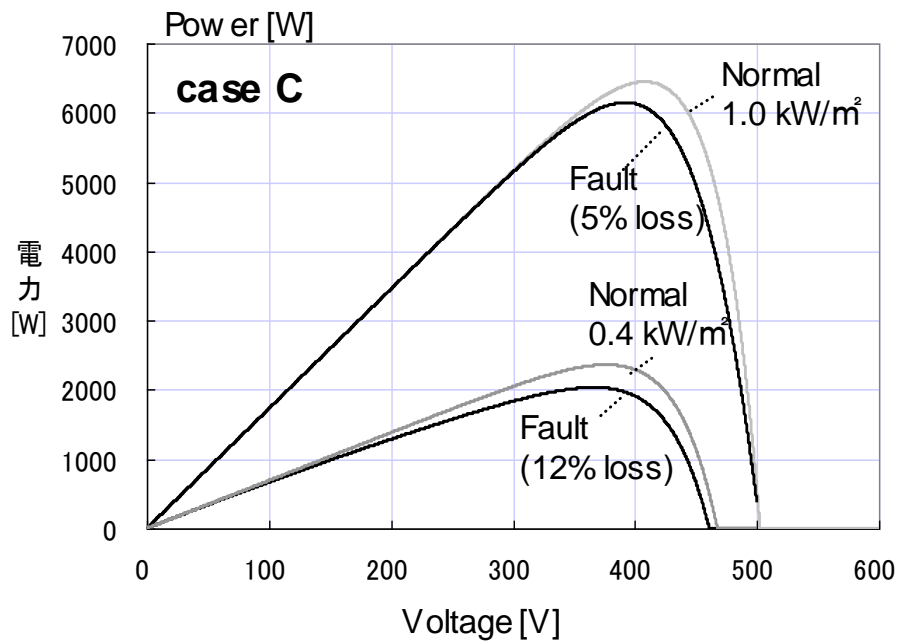
(c) shunt-resistance decrease

Figure 7.12. PV string characteristics in each fault mode
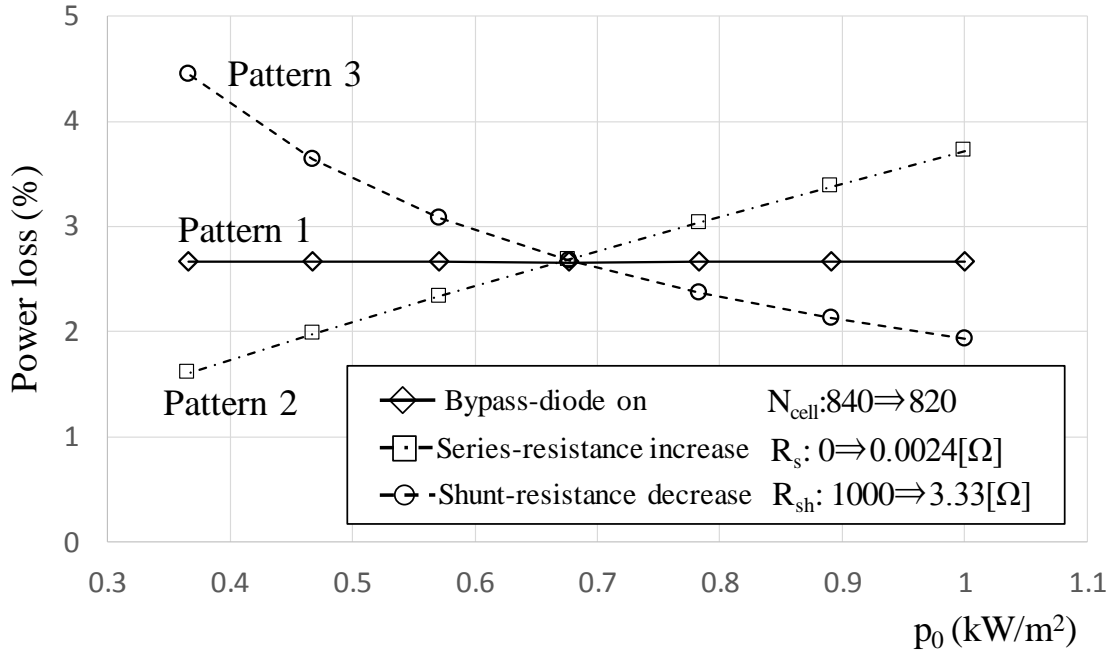
Figure 7.13.　Relationship between p_0 and power loss in each faulty mode

The initial number of normal PV cells is defined as N_{cell0} and the number of PV cells obtained in the fault-diagnosis flow in Fig. 7.10 is defined as N_{cell1}, the loss L_{cell} can be expressed by Eq. (7.26).

$$L_{cell} = (N_{cell0} - N_{cell1})/ N_{cell0} \cdot 100 \tag{7.26}$$

To identify the fault mode, a power-loss graph as a function of p_0 is first drawn using L_{cell} obtained by applying the DC current and voltage data consisting of hundreds of points in one day to the fault-diagnosis flow in Fig. 7.10. If the dependence is nearly the same as pattern 1 in Fig. 7.13, L_{cell} is estimated using Eq. (7.26).

If L_{cell} is larger than the threshold L_{cell_th}, "bypass-diode on" is determined most likely. If the dependence is nearly the same as pattern 2,

N_{cell} is returned to the initial N_{cell0} for calculating R_s. While varying Rs, the flow in Fig. 7.10 is repeated until the calculated L_{cell} pattern becomes pattern 1from pattern 2 in Fig. 13. As a result, N_{cell1} and R_s are determined. If R_s is larger than R_{s_th}, "series-resistance increase" is most likely determined. If estimated L_{cell} is larger than L_{cell_th}, "bypass-diode on" is also determined.

If the dependence is nearly the same as that in pattern 3, N_{cell1} is similarly returned to N_{cell0}. While varying R_{sh}, the fault-diagnosis flow is repeated. As a result, R_{sh} is determined. If the estimated R_{sh} is smaller than the threshold R_{sh_th}, "shunt-resistance decrease" is determined.

Chapter 8

System Configuration and Evaluation

8.1 Evaluation of Developed Architecture in a Large-scale Power Plant using Simulated Faults

To evaluate accuracy of the developed architecture, this technique is applied to the PV power plant system. The configuration of the 274.56-kW PV system used in this power plant is shown in Fig. 8.1. 220W crystal-Si products of 1248 sheets are used for this PV system. In case that the range separated by a bypass diode is defined as the PV cluster, this PV array is constituted of 3744 clusters. DC voltage and DC current is measured in PV inverter. this PV inverters is only MPPT controlled. To simulate the faults, corrugated plastic sheets as shown in fig. 7.11 are randomly put on the clusters in a PV array as mentioned above.
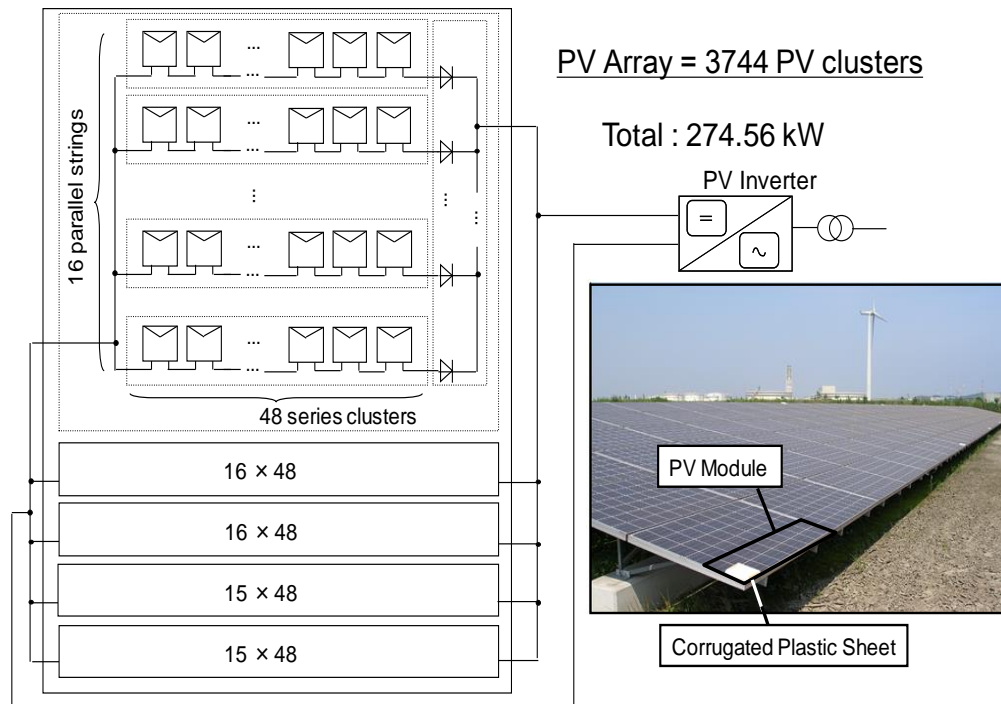
Figure 8.1 Configuration of the 274.56-kW PV system

Fig. 8.2 (a) shows the difference between estimated operating current I'_{pmax} and measured current I'_{pmaxE} when corrugated plastic sheets are set on 18 clusters in a PV array constituted of 3744 modules. The difference between I'_{pmax} and I'_{pmaxE} in Fig. 8.2 (a) is the smallest when the number of faulty modules is 16. In this case, the number of faulty modules is defined as 16. Fig 8.2 (b) shows the difference between estimated operating voltage V'_{pmax} and measured voltage V'_{pmaxE} when a corrugated plastic sheet is set on one cluster in a PV array constituted of 3744 modules. Since it is clear that the difference between I'_{pmax} and I'_{pmaxE} in Fig. 8.2 (b) is the smallest when the number of faulty clusters is 1, it is concluded that in this case, one faulty module can be detected.
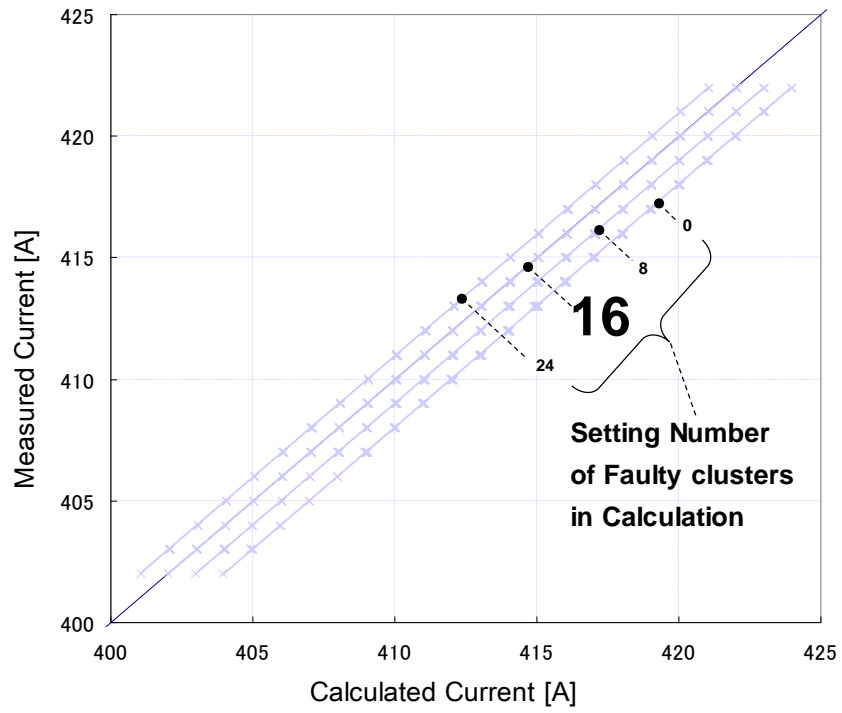
(a) Set of 18 corrugated plastic sheets
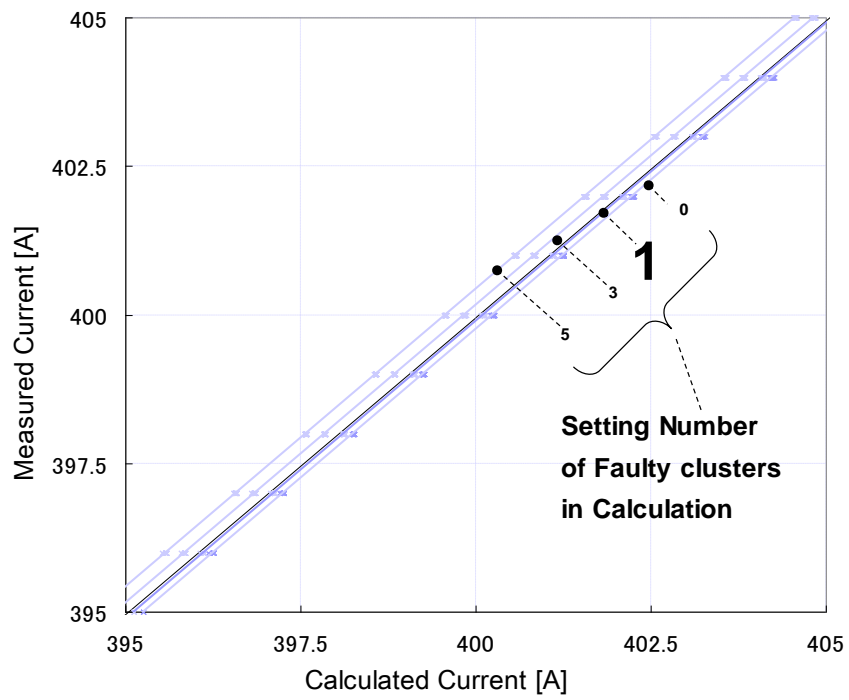
(b) Set of 1 corrugated plastic sheet

Figure 8.2 Correlation of calculated current and measured current

Fig. 8.3 shows the number of detected faulty clusters when the number of corrugated plastic sheets is varied. This result show that the developed fault-detection architecture can accurately determine the number of faulty clusters in a PV array without additional extra sensors.
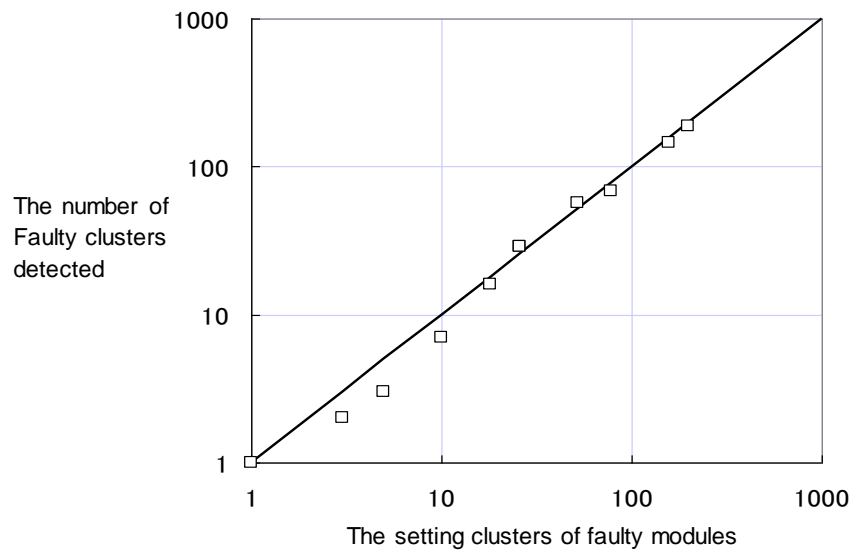
Figure 8.3 The number of faulty clusters detected in the power plant

8.2　System Configuration

The diagram of PV diagnostic system is shown in Fig. 8.4. The DC voltage and current measured in each PV inverter are transmitted to the monitoring system of the power plant. The improved architecture was executed at each power plant once a day. The DC current and voltage data acquired in one day consisted of 480 points corresponding to every minute from 8:00 to 16:00. The diagnosis results of several power plants were remotely confirmed via a virtual private network.
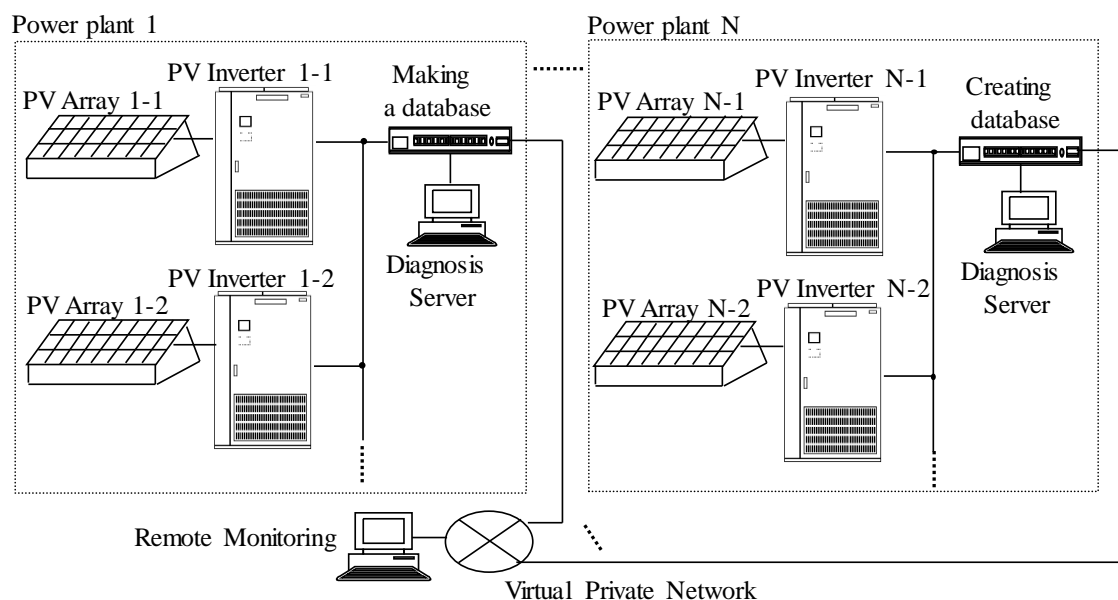
Figure 8.4　Diagram of PV diagnostic system

Figure 8.5 shows the DC power data in a predetermined PV inverter of each power plant. At power plant 1, the 245-W crystal-Si products of 1400 PV modules are connected to the PV inverter (all strings consist of 14 series PV modules, and the PV array consists of 100 parallel PV strings.). At power

plant 2, the 230-W crystal-Si products of 225 PV modules are connected to the PV inverter. At power plant 3, 192-W crystal-Si products of 1314 PV modules are connected to the PV inverter.

Figure 8.6 shows the j_0 and p_0 at power plant 1. For this power plant, time zones 1 and 2 are set, as shown in Fig. 8.3. It was found that j_0 and p_0 can be determined by calculating time zone 2 following the fault-diagnosis flow in Fig. 7.10.
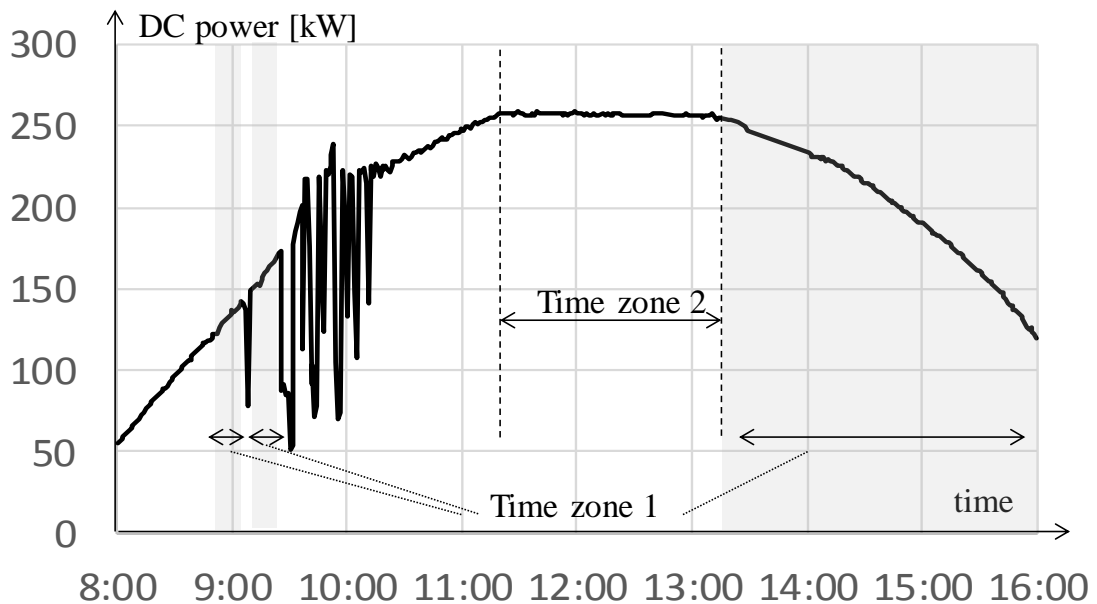
(a) Power plant 1
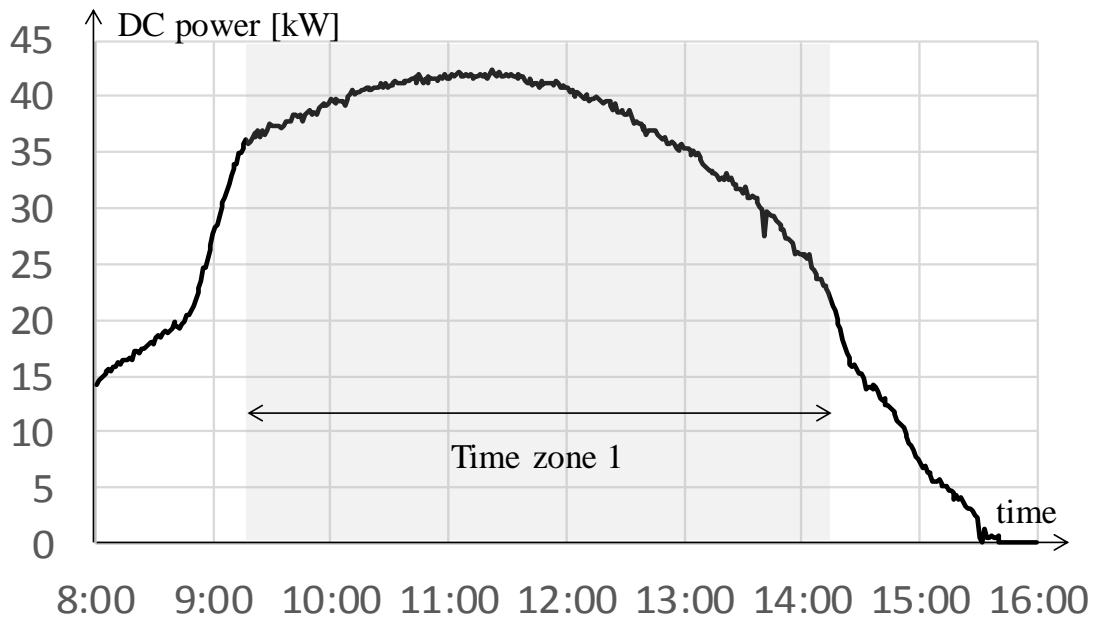
(b) Power plant 2
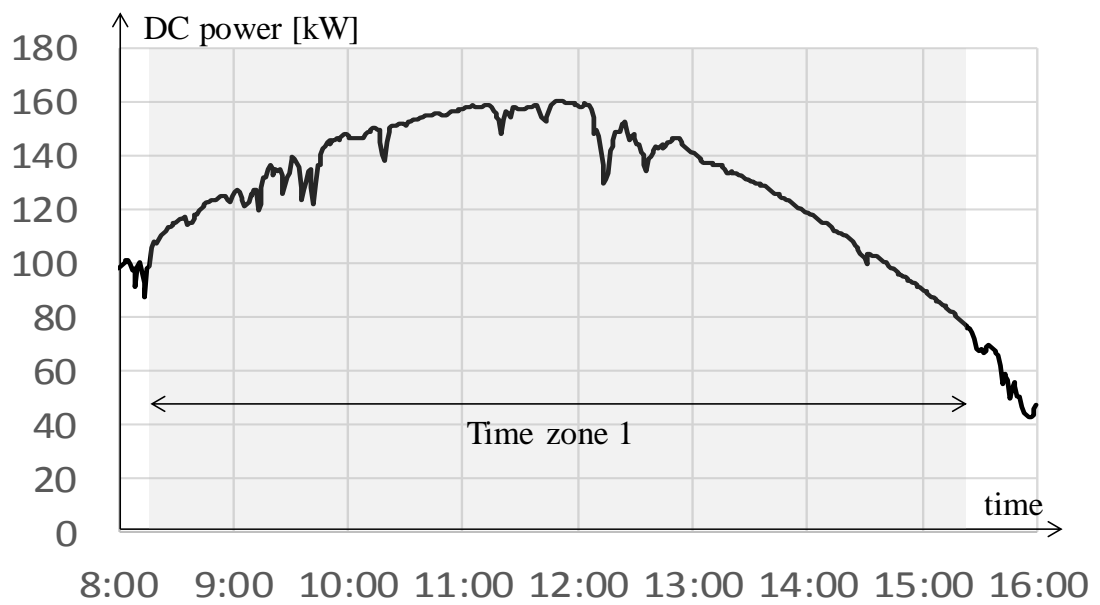
(c) Power plant 3

Figure 8.5 DC power data acquired every minute in PV inverter
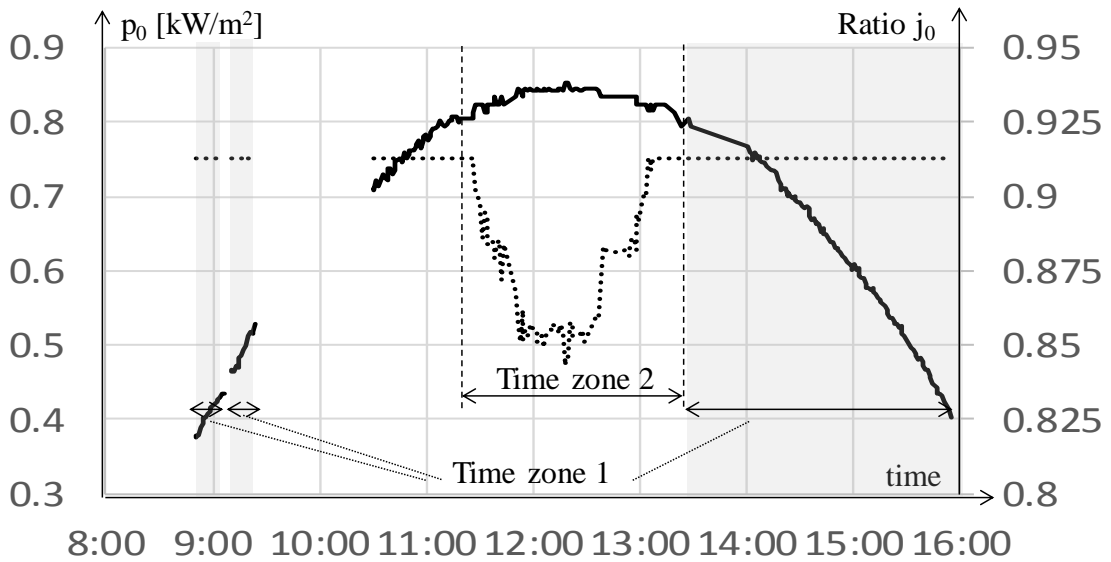
Figure 8.6. Calculated p0 and j0 at power plant 1

8.3 Evaluation Results

The actual diagnosis results at each power plant are shown in Figs. 8.7 and 8.8. At power plant 1, the relationship between p_0 and power loss was nearly the same as pattern 1 in Fig. 7.13, "bypass-diode on" of 0.1-0.2% loss was thus determined. When the I-V characteristics of the PV strings in the area of the PV inverter were measured during on-site inspection, the voltage drop caused by bypass-diodes being turned on was confirmed in some of the PV strings, as shown in the string I-V characteristic in Fig. 8.9(a). During visual inspection for some of the PV strings with voltage drop, the glass of a few PV modules was found to be, as shown in Fig. 8.9 (b).

The relationship between p_0 and power loss was nearly the same as pattern 2 at power plant 2, "series-resistance increase" was thus determined.

When the I-V characteristics of the PV strings in the area of the PV inverter were measured during on-site inspection, the increase in R_s was confirmed in almost all PV strings. For several randomly chosen PV modules, an increase in R_s and about 4% power loss were confirmed under STC (298 K, 1.0 kW/m2). The I-V and PV characteristics of one of these PV modules are shown in Fig.8.9 (c) and Fig.8.9 (d).

The output performance at power plant 3 further decreased for 2 months after the diagnosis, as shown in Fig. 8.8; therefore, the I-V characteristics of all PV strings at power plant 3 were measured. In this on-site inspection two months after diagnosis, the decrease in R_{sh} was confirmed from the I-V characteristics measurement of almost all PV strings. For the randomly chosen PV module after the on-site inspection, the decrease in R_{sh} and large power loss of over 40% were confirmed, as shown from the I-V characteristic in Fig. 8.9 (e). The emission of some PV cells also disappeared, as shown in the EL image of Fig. 8.9 (f). This decrease in output power is due to PID [5–6]. These results indicate that the improved architecture can determine "shunt-resistance decrease" at the early stage of low power loss of about 5% even for events that cause serious power loss such as PID.
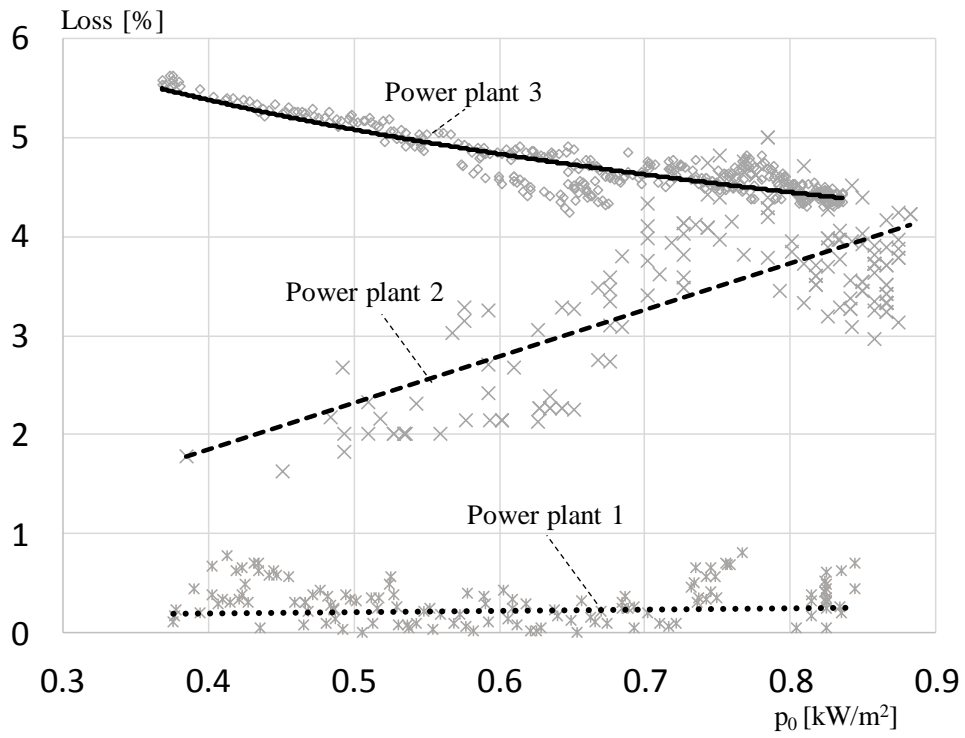
Figure 8.7. Actual diagnosis results at each power plant
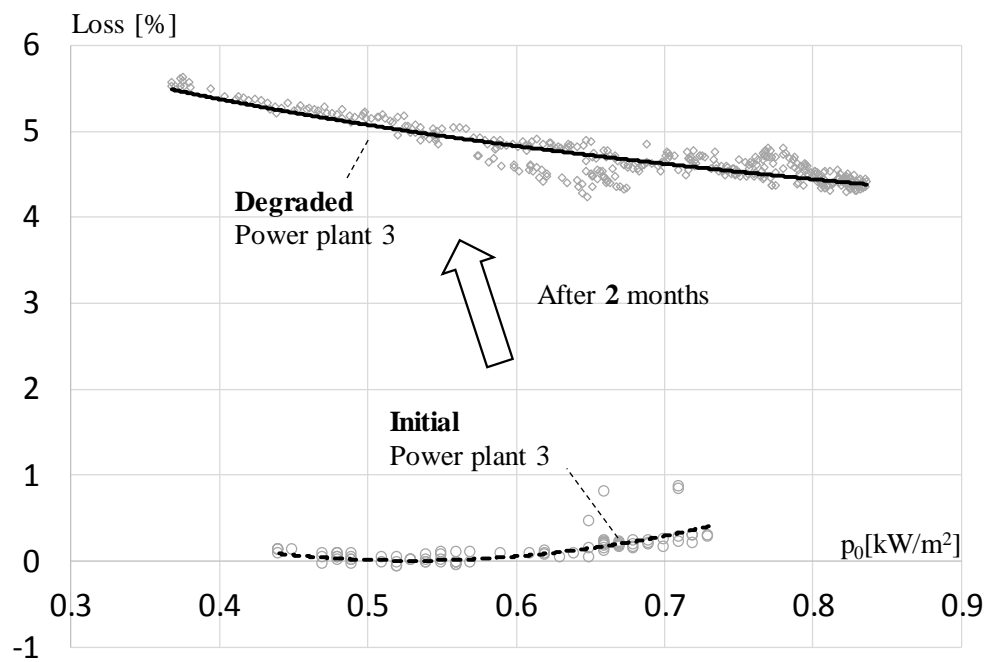
Figure 8.8. Comparison of diagnosis results
between initial and degraded output power at power plant 3
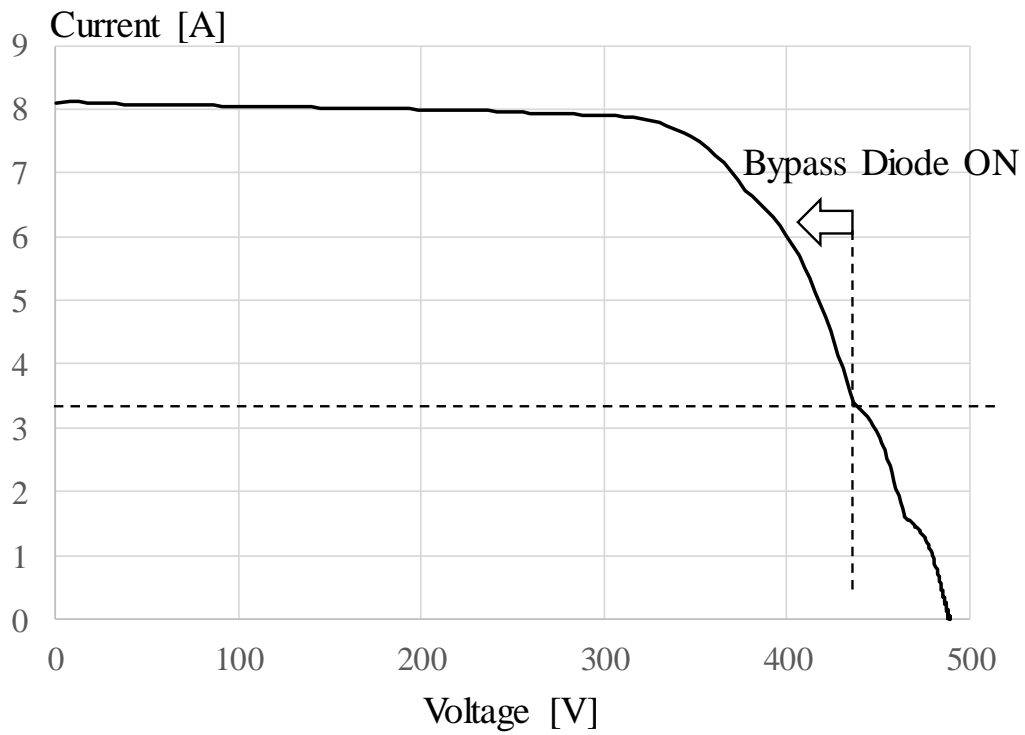
(a) Detected string's IV at power plant 1 (pattern1: broken wire)

(b) Detected Glass breakage (pattern1: broken wire)
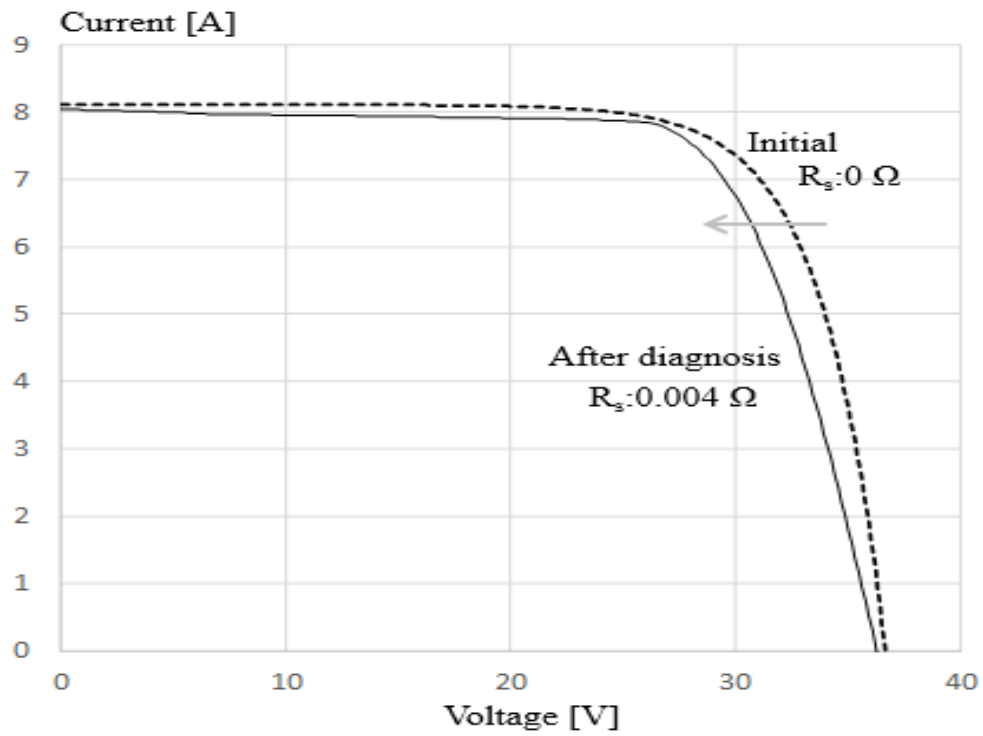
(c) Measured module's IV characteristics (pattern2: series-resistance increase)
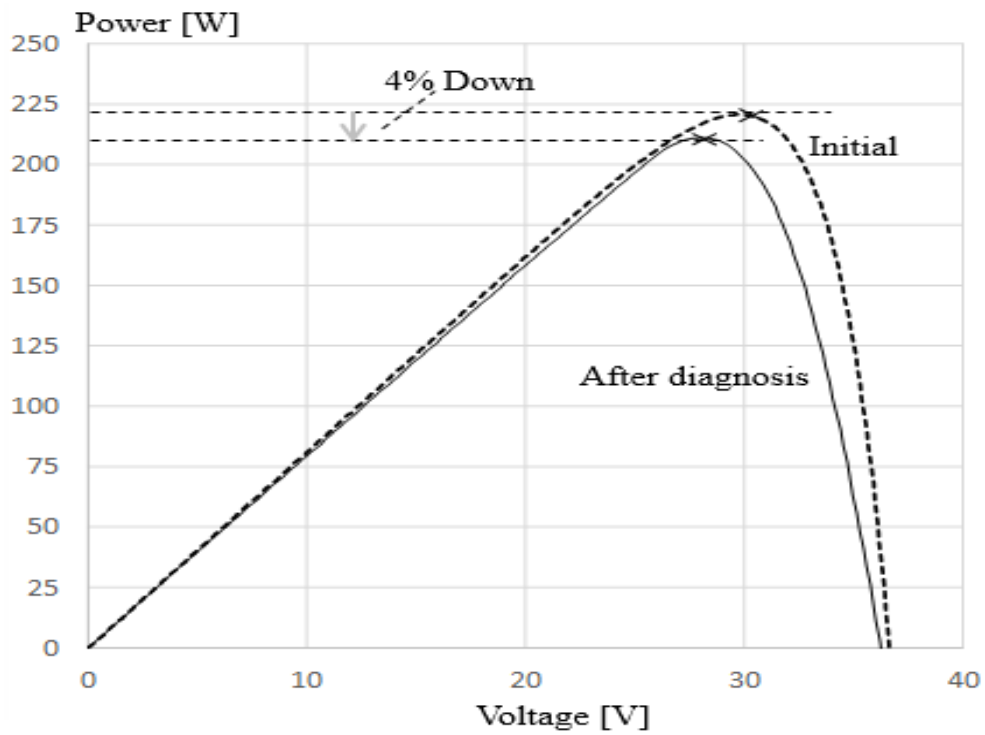
(d) Measured module's PV characteristics (pattern2: series-resistance increase)
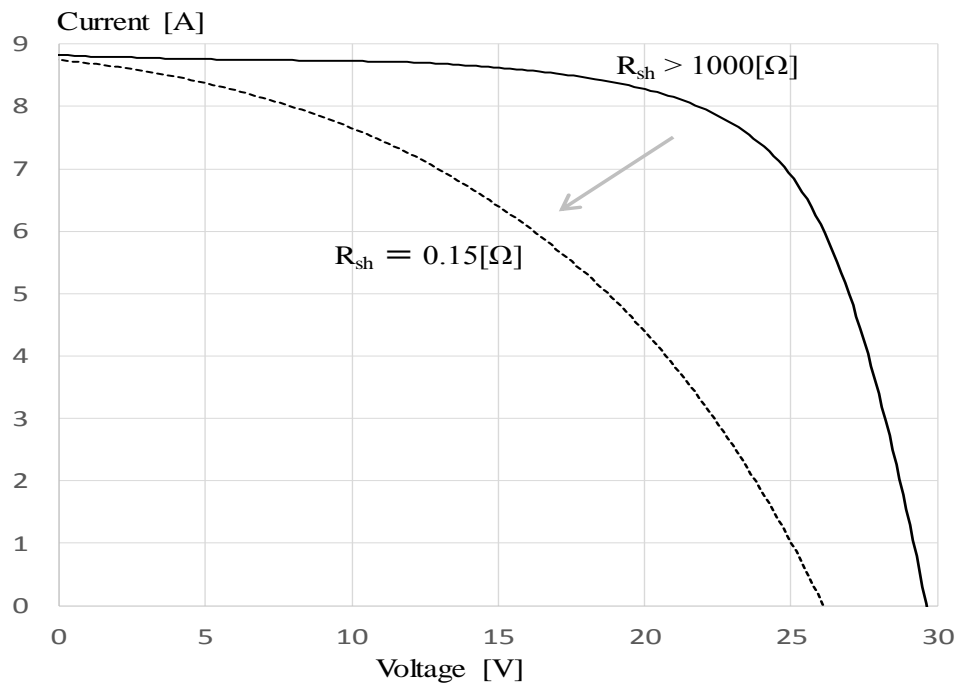
(e) Measured PV module's IV characteristics (pattern3: shunt-resistance decrease)

Degraded Cell

Normal Cell
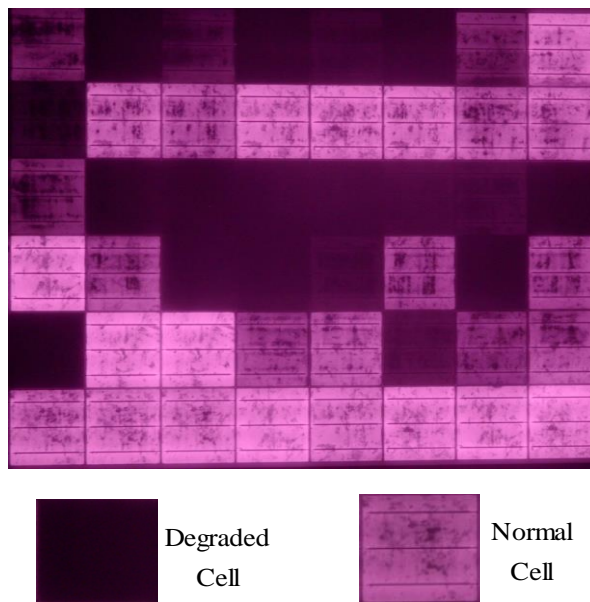
(f) Measured module's EL images (pattern3: shunt-resistance decrease)

Figure 8.9. The performance of PV module or string investigated after diagnosis

Chapter 9

Review of Part II (Passive Matrix)

In chapter 7 and 8, a self-sensing system was applied to a large-scale PV system as an electric power system. This system can calculate the number of faulty modules in a PV array and determine the cause of failure and degradation using the operation point of both MPPT and clipping of output power. The key technique in this architecture is that, instead of using the irradiation and module temperature measured using pyranometers and thermometers, respectively, their theoretical values are calculated from the PV-module characteristics and measured DC voltage and current of a PV inverter.

A PV diagnostic system connected via a virtual private network was constructed to apply this architecture to three large-scale PV power plants. It was experimentally demonstrated that this architecture can determine the number of fault modules even for a loss of less than 0.2% and accurately determine the cause of failure and degradation, namely, "series-resistance increase", "shunt-resistance decrease", or "bypass-diode on" even for a loss of less than 5–6%.

This means that not only the faulty module can be replaced before the DC ground fault as shown in Fig. 1.8, but also the timing of the maintenance can be remotely monitored and the labor and the cost are greatly reduced. That is, it was shown that a self-sensing system as shown in Fig. 1.11 was feasible.

Chapter 10

Outlook

10.1   Implementation of machine learning

In the application of the self-sensing system discussed above, high-precision detection of manufacturing and environmental parameters can be achieved without additional sensors or with minimal configuration. However, existing sensors and installed minimal configuration sensors are not always measurable with sufficient accuracy and resolution.

In the future, machine learning will be embedded in the self-diagnosis system to achieve more accurate sensing. As shown in Fig. 10.1, first, the reference data are prepared. Next, clustering of the relationship between the reference and self-sensing results is executed. After that, selection or modification of the monitoring data is performed, and the processed data is applied to the self-sensing system of the semiconductor array matrix. By modifying the data, the complex calculation of environmental parameters can be simplified. Further, by implementing machine learning, the sensing of parameters of an array matrix composed of non-semiconductor cells, such as a LIB system and a medical sensor system, can be accomplished.
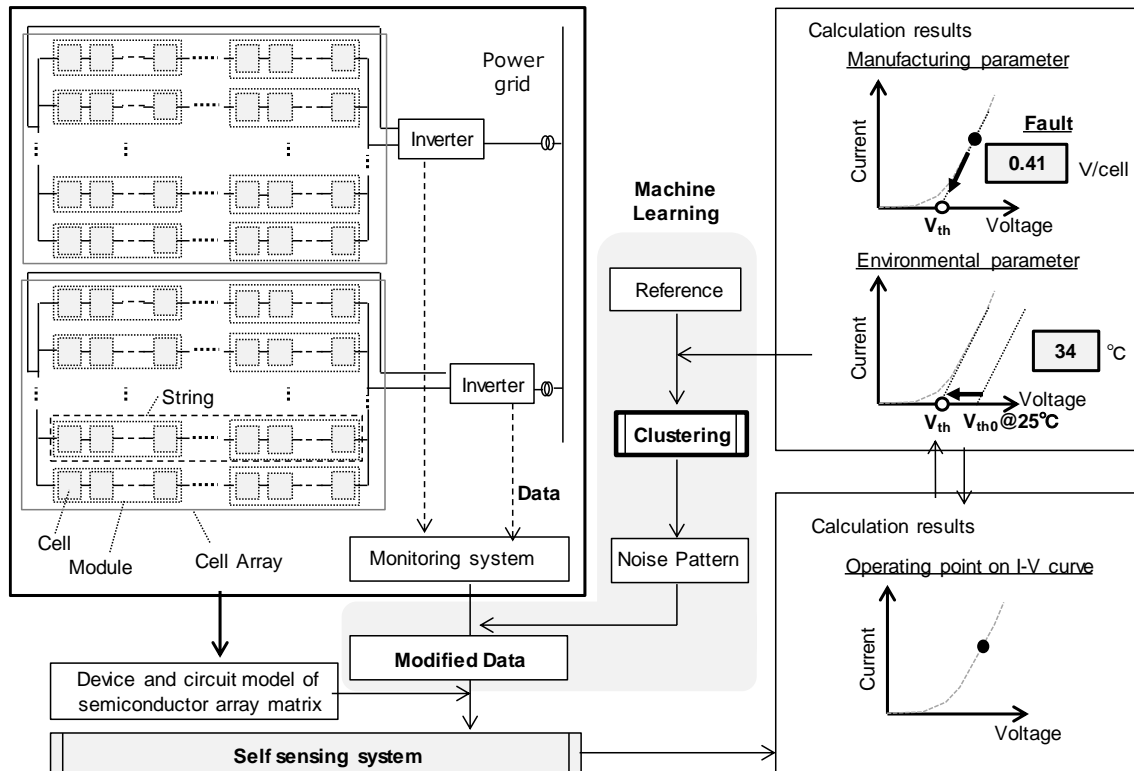
Figure 10.1. Concept of self-sensing system in semiconductor Array Device with machine learning

10.2 Example of application

10.2.1 Example of application to a PV system

The sensing in the large-scale PV system described in Part II (Chapter 6–9) can be cited as a simple application example of clustering. If the fault diagnosis is executed on a day with large power fluctuation, such as that which occurs at the time from 8:30 to 11:00 in Fig. 10.2 (a), the results of regression analysis will have a large variation, as shown in Fig 10.2 (b). Therefore, the diagnostic accuracy is low, and the fault modes cannot be analyzed. This variation is caused by an insufficient response from the MPPT

control of the PV inverter to the fluctuation in irradiation. (The constant value c0, such as 0.914 and 0.935 mentioned in Fig. 7.10 (Chapter 7), cannot be secured.)

(a) DC power vs time   (b) the result of regression analysis
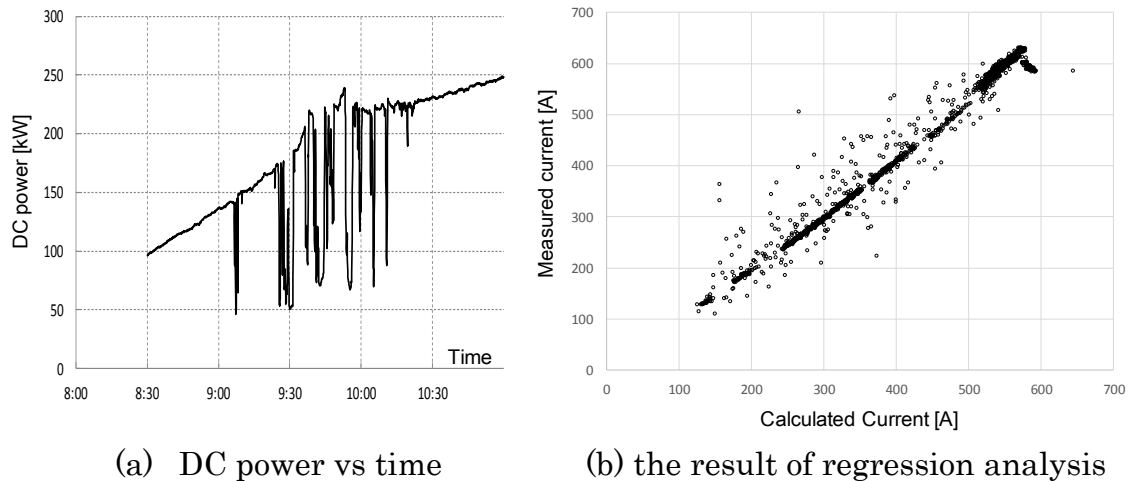
Figure 10.2. DC power on day with large fluctuation and regression analysis of the diagnostic results

Here, machine learning is implemented. In a large-scale PV power plant, a few pyranometers are installed in a large area to provide reference data. First, the results of regression analysis between the measured irradiance and the irradiance calculated by the calculation process in Fig. 7.10 are recorded daily. The response speeds of a PV and pyranometer are very different, so the results of the regression analysis shown in Fig. 10.3 are obtained. Assuming that the dispersion is σ and the sample number is n, the total diagnostic accuracy becomes $\sigma/\sqrt{n}$. Next, the upper and lower limits corresponding to the target of the diagnostic accuracy as shown in Fig. 10.3 are determined using clustering, and unnecessary measurement data are removed.
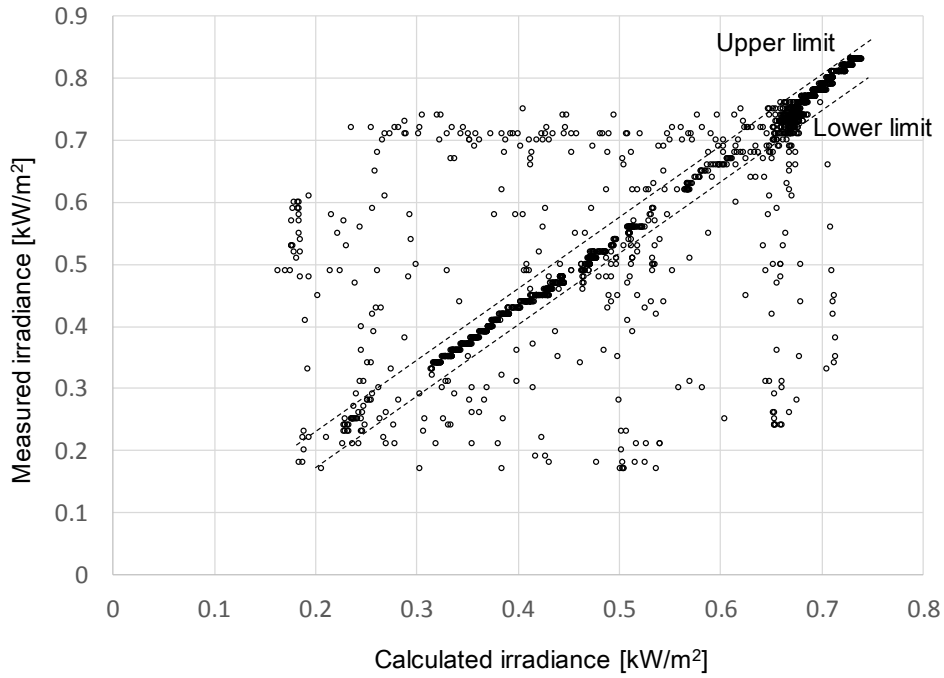
Figure 10.3. Data selection for diagnosis by machine learning based on reference data

(measured irradiation by pyranometer)

Figure 10.4 shows the selected DC power data and the regression line of the diagnostic results after rejecting unnecessary data. These results show that high-precision sensing can be performed even under large fluctuations caused by partial shade or the like by monitoring the measurement performance of the PV inverter using clustering.
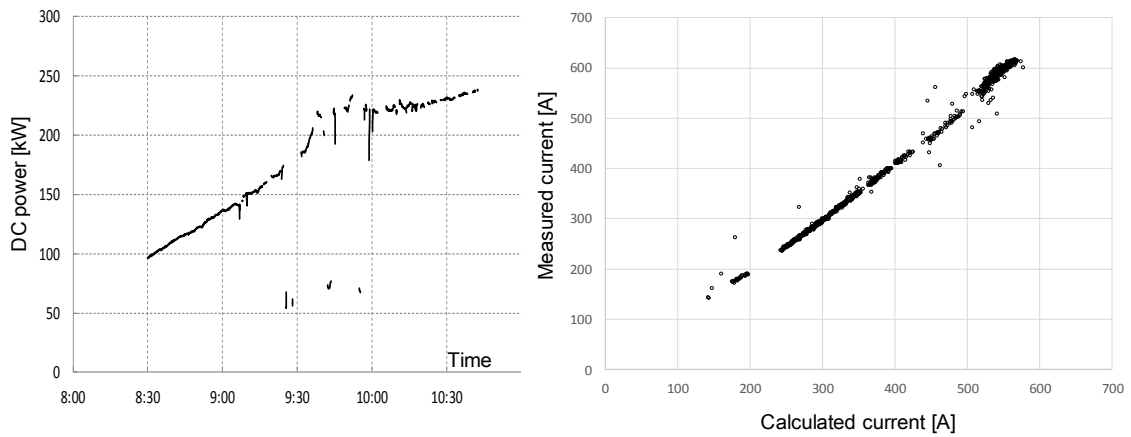
Figure 10.4. Selected DC power on day by machine learning and regression analysis of diagnostic results

10.2.2　Example of application to a storage battery system

Next, we examine an example of application to a storage battery system. A storage battery cell such as a LIB is not a semiconductor device. However, a cell array consists of battery cells arranged in series and parallel, and it is controlled by an inverter, the same way a PV array is. Therefore, a storage battery system can be considered a passive array matrix.

The configuration of a storage battery system is shown in Fig. 10. 5. The system is composed of submodules consisting of series- and parallel-connected battery cells, modules consisting of series- and parallel-connected submodules, and packages consisting of series- and parallel-connected modules. The packages are connected to a battery management unit (BMU).

The information of the battery cells' maximum voltage V_{max}, minimum voltage V_{min}, maximum temperature T_{max}, and minimum temperature T_{min} are available in the submodules. The modules have a cell-balance controller to control the charge distribution during charge and discharge.
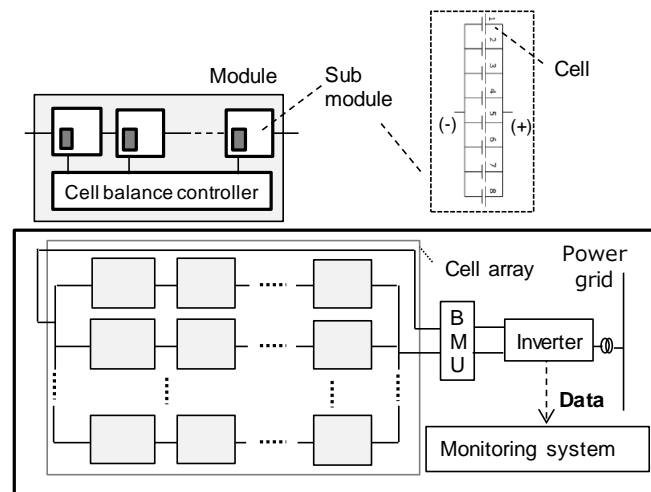
Figure 10.5. Configuration of lithium ion battery storage system

If a battery cell degrades, its voltage increases at low state of charge (SOC), as shown in the Fig. 10.6. As shown in Fig. 10.5, the cell balance is controlled by a cell-balance controller in a submodule, and the voltage of the modules is balanced by the BMU. The lifetime of a LIB storage system is determined by the cell with the shortest lifetime. Therefore, sensing the characteristics of the cell with the worst performance is very important.
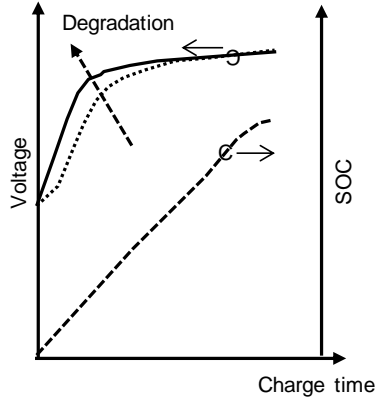
Figure 10.6. Degradation characteristic of LIB storage cell

However, due to cell-balance control and the balancing of the BMU, variations in measured voltage data are usually suppressed. This means that it is difficult to distinguish the voltage of the cell with the shortest lifetime among the measured voltage data.

Here, machine learning is implemented. First, a battery's thermal activation energy E_a and acceleration factor AF are set. E_a is estimated using an acceleration test or similar method. AF is calculated with the Arrhenius equation using E_a, T_{max}, T_{min}, and Boltzmann's Constant k, as below.

$$AF = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_{min}} - \frac{1}{T_{max}}\right)\right) \qquad (10.1)$$

Next, the variation of the voltage V_{ref} in the acceleration test is set as a reference. V_{ref} can be regarded as (V_{max}-V_{min}) corresponding to the cycle numbers of the charge/discharge and acceleration factor AF.

Then, the charge/discharge patterns in the inverter's

operation are classified using clustering. The patterns in which (V_{max}-V_{min}) and V_{ref} are the closest are grouped. After grouping, the largest voltage-variation value among the selected data is plotted on the graph in Fig. 10.7. The upper limit in Fig. 10.7 is adjusted using machine learning in the same way as in the application to the PV system. In the example of Fig. 10.7, the voltage variation exceeded the upper limit at the N1 cycle; it is considered that the AF changed, that is, that the E_a of the cell with the shortest lifetime greatly changed. This means that a cell's operating point on the I-V curve can be presumed, and a degraded cell can be sensed even if the cell is not a semiconductor device, by implementing machine learning to the self-sensing system.
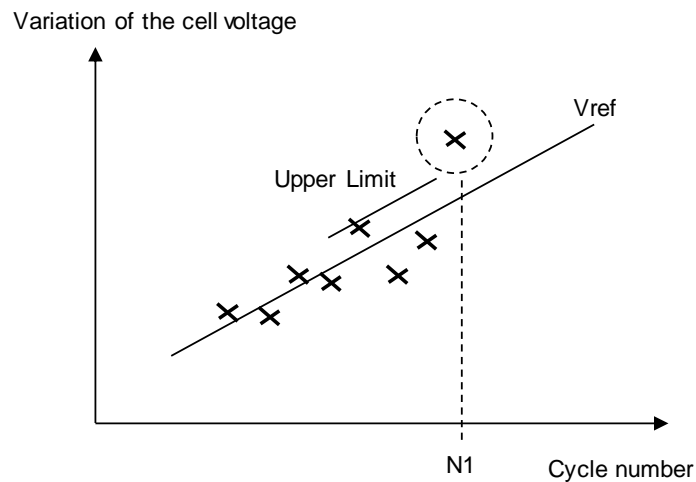
Figure 10.7. Sensing of fault cell by introduction of machine learning

10.2.3 Example of application to medical imaging

We also consider an application of the self-sensing system implementing machine learning to medical imaging. Imaging of the elements of protein and the brain, which medical devices do, requires precise measurements of magnetic fields.

Recently, diamond crystals containing nitrogen-vacancy pairs, i.e. diamond nitrogen-vacancy (NV) centers, have been studied as high-sensitivity magnetic-field measurement devices for use at room temperature [71]. A conceptual depiction of the neuromagnetic sensing of brain function using a diamond NV center is shown in Fig. 10.8. Many diamond NV centers can be installed around the brain; installing diamond NV centers in this way is expected to achieve high-areal-density sensing. A microwave with a high frequency of 2 to 3 GHz irradiated the diamond crystal of a diamond NV center. Regarding the intensity of red fluorescence obtained by sweeping the frequency of the microwave, the magnetic field is measured at the frequency at which the intensity of fluorescence intensity is the minimum. A green laser light is used as a blue-green light source that irradiates the diamond crystal with excitation light. An image sensor is used to detect the red fluorescent output from the diamond crystal in pixel units. A diamond NV center is composed of a diamond substrate and NV center layer. The NV center layer is formed using chemical vapor deposition (CVD). The measurement target for a diamond NV center is neuromagnetic signals of brain function. A microwave source, light source, and image sensor are controlled by a control

block. The signal in the brain is sensed in a pixel unit of the image sensor. The resolution of the signal in the brain is usually higher than that of the image sensor. This system, shown in Fig. 10.8, can be regarded as an array matrix composed of the measurement target, diamond NV center, and image sensor if the brain signal's unit of the measurement target is regarded as a cell.
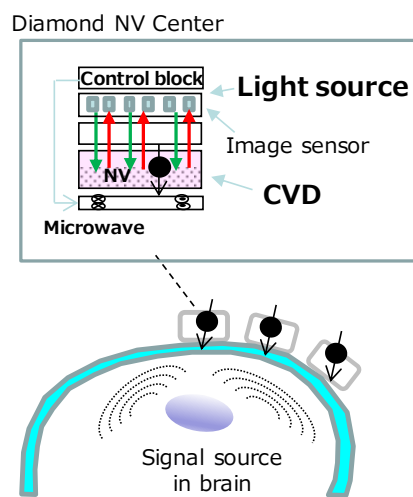
Figure 10.8. Neuro-magnetic sensing of brain function using diamond NV center

Regarding the high sensitivity of the magnetic sensor, that is, handling the depth, as described in existing research [71], highly sensitive magnetic-field measurement without restriction on the evolution time was accomplished with dynamic decoupling. As for miniaturization, the microwave source and control block in Fig. 10.8 are composed of electronic components such as a synthesizer and FPGA board, respectively, as shown in Fig 10.9. In this way, a compact configuration was achieved.
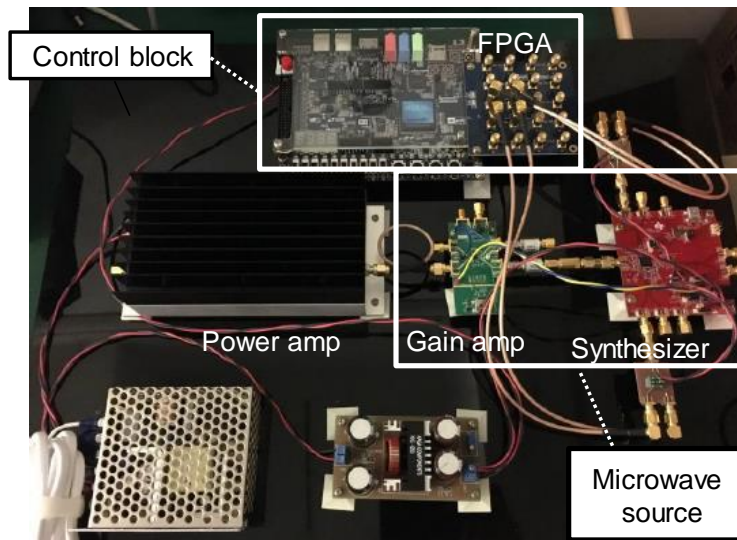
Figure 10.9. Miniaturization of control block and microwave source

To develop the neuromagnetic sensing system for brain function as shown in Fig 10.8, technologies must be developed from the viewpoints of spatial and temporal resolution.

For spatial resolution, the noise pattern is removed by clustering. First, a method to detect image-sticking that cancels deposition unevenness in OLED, as described in other work [72], is applied, canceling the signal fluctuation caused by vapor deposition unevenness in CVD.

Next, the multi-stage analog-to-digital converter (ADC), shown in Fig. 10.10, is used to suppress the quantization error restricted by shot noise from the light source. The multi-stage ADC is composed of a standard ADC and level-shift ADC. As shown in Table 10.1, numerical value with V_{th_det} as one unit determined by quantization error is suppressed to $V_{th\_det}/2$ by combining

the standard ADC's data and level-shift ADC's data. The level-shift ADC was also used for sensing V_{th} of a drive TFT on the AM-OLED display in Chapter 3.
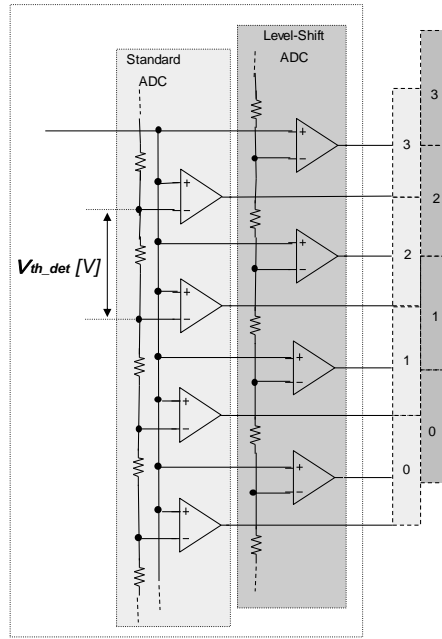
Figure 10.10. Multistage Analog Digital Converter (ADC)

Table 10.1. Suppressed quantization error by multistage ADC

Data of standard ADC Data of level-shift ADC	Value with suppressed quantization error
(0 0),	0
(0 1), (1 0)	1
(1 1),	2
(1 2), (2 1)	3
(2 2),	4
(2 3), (3 2)	5
(3 3)	6
⋮	⋮

Numerical value with V_{th_det} as one unit   Numerical value with $V_{th\_det}/2$ as one unit

The signal fluctuation caused by vapor deposition unevenness in CVD and the quantization error restricted by the shot noise from the light source are quantified. By introducing clustering and separating periodic fluctuation caused by the light source, all of the noise caused by the structure of the diamond NV center can be removed.

For temporal resolution, we need the solution of the inverse matrix to convert the M pcs data measured by the image sensor into the information of the voxels separated by N finite elements. However, the inverse matrix calculation may only be performed with a sensor if there is a large change among the sensors around the NV center in Fig. 10.8 because fluctuating components other than the signals in the brain are removed by the above method. For this reason, machine learning is made to select the sensor to perform the inverse matrix calculation. This implementation of machine learning will reduce the amount of computation and contribute to the creation of a compact neuromagnetic sensing system for brain function.

Chapter 11

Conclusion

The self-sensing system was developed for semiconductor array matrices, in which semiconductor elements such as transistors and diodes are arranged in an array. Semiconductor array matrices can be classified as active or passive matrix arrays. In this study, the system was equipped to both passive and active array matrices. An array matrix possessing a cell with a transistor, as discussed above, is defined as an active array matrix, and an array matrix possessing a cell in which the main element is a diode is defined as a passive array matrix.

In an active array matrix, peripheral circuits and transistors control an operating point on the I-V curve before manufacturing parameters are calculated. In contrast, in a passive array matrix, environmental parameters that indicate an operating point on the I-V curve, such as operating temperature of the array matrix, are estimated by a circuit model, device model, and sensed data.

In Chapters 2, 3, 4, and 5, forming Part I, the self-sensing system was applied to an AM-OLED display, an active array matrix. Peripheral circuits

and transistors in an active matrix array control an operating point of a drive TFT on an AM-OLED. Each pixel's V_{th} of the drive TFT on the AM-OLED is sensed as a manufacturing parameter. To evaluate the effectiveness of the proposed method, a prototype 3.8-inch 480×320-ppi OLED was built in Chapter 4. From the V_{th}-distribution image, an offset signal for compensating V_{th} variation was generated, and the variation of V_{th} was compensated for by adding the offset signal to the data signal. We found that the OLED panel produces highly uniform pictures when this compensation is applied.

In Chapters 6, 7, 8, and 9, forming Part II, the application of the self-sensing system to a PV system, a passive array matrix, is described. The power generated by a PV system is influenced by fluctuations in environmental parameters, such as temperature and irradiation. First, environmental parameters were estimated using a circuit model, device model, and sensed data. Environmental parameters indicated an operating point on the I-V curve, e.g., operating temperature, of the PV system. Next, faults and degradation were calculated as the manufacturing parameters using the estimated environmental parameters. A PV diagnostic system connected by a virtual private network was constructed to apply this architecture to three large-scale PV power plants. We experimentally demonstrated that this architecture can determine the number of faulty modules even for a loss of less than 0.2%. We also experimentally found that it can accurately determine the cause of failure and degradation, namely, series-resistance increase, shunt-resistance decrease, or bypass diode on,

even for a loss of less than 5–6%.

In Chapter 10, as considerations for future work, we discussed the implementation of machine learning for further accuracy improvement and expansion of application to array matrices with cells that are not semiconductors. By implementing machine learning, the sensing of parameters of an array matrix composed of non-semiconductor cells such as a LIB system and a medical sensor system may be accomplished.

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Award

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[2] 平成 30 年度関東地方発明表彰 "太陽光発電システムの高感度故障診断技術（特許第 6075997 号）"

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