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A Study of High-Linearity High-Data-Rate Millimeter-Wave CMOS Transceiver Design

by

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A Ph.D. dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

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in the

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of

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Supervised by

Professor Kenichi Okada

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To my family

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Abstract

This dissertation presents a study of millimeter-wave transceiver targeting high data rate by improving spectrum efficiency with high linearity and high-order modulation scheme in CMOS technology.

The dissertation starts from CMOS millimeter-wave devices modeling and wireless transceiver system analysis. Passive and active devices modeling and characterization is usually required for highly accurate design at millimeter-wave frequencies. For a given channel bandwidth, the communication data rate can be increased by using high-order modulation schemes, which require high system linearity.

The power amplifier design has a dominant effect on wireless transceiver system linearity. The power amplifier is designed to handle large output power before emitted from transmitter antenna, the higher linear output power leads to the longer communication distance. To achieve a high linearity with adequate gain on the millimeter-wave power amplifier design, optimized transistor and output transformer are utilized. The power combined solution is provided by using modeled transmission line to further improve output power and overall linearity. Designed for 5G New Radio 28GHz and 39GHz bands, a 28 GHz power amplifier and a 39 GHz power amplifier are introduced. By using high quality factor 1:1 ratio transformer and high-accuracy output matching technique, the proposed 28 GHz power-combining PA achieves 20.2dBm P_{SAT} and 11.4dBm output power with 2500MHz 64QAM modulated signal. A single path 39 GHz PA with transmitter/receiver switch is proposed, it achieves 15.5 dBm P_{SAT} and 8.6 dBm output power with 3000MHz 64QAM modulated signal.

Due to relatively higher free-space path loss (FSPL) at millimeter-wave frequencies, it is necessary to overcome high FSPL when establishing a long distance millimeter-wave wireless link. The link distance can be enhanced by further improving transmitter output power, however, the power amplifier designed in CMOS has a limited performance due to the technology limitation and feasibility. The phased-array architecture with controlled sub-array element can enhance the transceiver signal strength therefore enhance the link distance. Targeting several hundred meter millimeter-wave link distance, the estimated array element for transmitter is over 1000. Highly accurate sub-array element phase

and gain control are required for high quality beamforming. 28GHz and 39GHz phased-array transceiver are implemented with the characteristic of high linearity. The measured 1-channel transmitter peak error vector magnitude (EVM) for 28GHz transceiver and 39GHz transceiver are -37dB and -34dB, respectively. The measured 1-channel receiver peak signal to noise and distortion ratio (SNDR) for 28GHz transceiver and 39GHz transceiver are 39dB and 40dB, respectively. Built-in phase gain calibration mechanisms are proposed to enhance the beamforming quality. The proposed phase gain calibration extracts the phase and gain information in each sub-array transmitter and receiver path. An analog-to-digital convertor (ADC) and a phase-to-digital convertor (PDC) are used for gain and phase quantization. The built-in calibration has a measured accuracy of 0.08-degree RMS phase error and 0.01-dB RMS gain error. Thanks to the highly-accurate phase gain control, the 8TX-8RX phased-array transceiver module 1-m OTA measurement supports 5G NR 400MHz 256QAM OFDMA modulation with -30.0dB EVM. The 64-element transceiver has a EIRP MAX of 53dBm.

Furthermore, for indoor high data rate high portability wireless, a novel BPOOK modulation is proposed to realize the ultra low power consumption with improved spectrum efficiency. Conventionally, to realize a low power wireless transceiver at millimeter-wave frequencies, the on-off-keying (OOK) modulation is used due to its simplicity. However, the OOK modulation has the intrinsic issues of low spectrum efficiency and high LO feedthrough (LOFT). In order to solve the issues in OOK modulation, a binary-phase-OOK (BPOOK) is proposed. The BPOOK wireless transceiver transmits radio frequency (RF) signal with amplitude modulated on and off by input baseband data, and meanwhile phase is changing between 0° and 180°. The BPOOK transceiver achieves doubled spectral efficiency compared with OOK modulation and binary-phase-shift keying (BPSK) modulation. It also cancels the intrinsic LOFT in the OOK modulation. The 60GHz BPOOK transceiver achieves 3.0Gb/s data rate while consuming a power of 100mW. The 60GHz BPOOK transceiver is compliant with spectrum mask in IEEE 802.11ad standard.

At last, this dissertation concludes the millimeter-wave transceiver design towards high data rate by improving spectrum efficiency with proposed high linearity power amplifier, high accuracy phased-array transceiver and spectrum efficient BPOOK modulation scheme. Future researches are also discussed in the end of the dissertation.

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Chapter 1

Introduction

The electrical and electronic technology has changed human society tremendously in the recent hundred years. One of the most significant impacts on human daily life is the communication system. In the past thousands of years, people have been using visual signals for transferring information, such as smoke signals, signal flags and semaphores. Until the 1830s, the electrical telecommunication systems started to appear with the invention of telegraph. The telephone was invented in the 1870s, which enables people to realize voice transmission over a wire with a distance of thousands of miles. The first communication through radio waves are established in 1901 by Guglielmo Marconi, who shared the 1909 Nobel Prize in physics with Karl Ferdinand Braun, in recognition of their contributions to the development of wireless telegraphy. Over more than a hundred yearsą́ improvement and development, the modern wireless communication has been specified and dedicated for different purposes, such as WiFi, Bluetooth, ZigBee, NB-IoT, 2/3/4/5G etc.

Nowadays, wireless communication has been involved in high data rate applications, for supporting interactive video services, massive connections, virtual reality, augmented reality and so on. However, with the increasing demand on wireless communication speed, the frequency band allocation is becoming more and more crowded than ever before. Meeting the demand is a formidable task by utilizing the today's cellular network frequency bands (below 10 GHz). To address the challenge, millimeter-wave bands (30 GHz to 300 GHz) has been raised great interest in it, where the bandwidth is tens to hundreds of times wider than low frequency bands [1–4]. Moreover, with the increasing of electronic device operation frequency, the wavelength is becoming smaller, which makes the circuits area efficient and low cost.

The CMOS technology provides high integration and low cost solution for integrated circuits implementation. The peak f_{t} and f_{max} of over 500 GHz in standard CMOS tech-

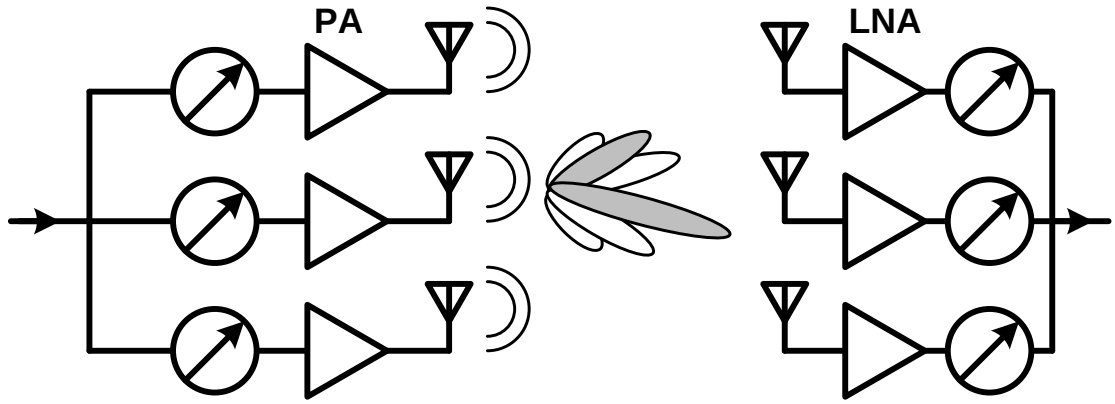


Figure 1.1: Simplified phased-array transceiver.

nology are predicted with the improvement of technology scaling. However, due to the low electron mobility, low breakdown voltage and low passive device quality factor, there are still a lot of improvements needed for realizing as good performance as GaAs or InP, such as local oscillator phase noise and power amplifier linearity.

1.1 Millimeter-Wave Wireless

The millimeter-wave band is the frequency band from 30 GHz to 300 GHz with its wavelength from 10 mm to 1 mm. The bandwidth that provided in a millimeter-wave band is much wider than current popular bands for cellular network and wireless local area network. In principle, the data rate a transceiver can achieve is limited by its channel capacity, which is related to the channel bandwidth and signal-to-noise ratio (SNR). The Shannon channel capacity theorem is expressed as:

$$C = BW \cdot \log_2(1 + SNR) \tag{1.1}$$

The system SNR is related to transceiver noise figure, linearity and local oscillator phase noise. However, due to high freespace propagation loss at millimeter-wave frequencies, the communication distance is relatively short and makes the millimeter-wave application limited within the short-distance communication. The phased-array technique enables transceiver to achieve a longer distance. The phased-array technique is reasonable in millimeter-wave bands since the antenna size is proportional with the wavelength. Figure 1.1 illustrates a phased-array transceiver mechanism. The received signal strength

is described in the Friis transmission equation:

$$P_r = P_t \cdot G_t \cdot G_r \cdot \left(\frac{\lambda}{4\pi \cdot d}\right)^2 \tag{1.2}$$

where P_t is the total transmitter output power, G_t, G_r are the transmitter and receiver antenna gain, respectively. For a phased-array transceiver with transmitter element of N_t and receiver element of N_r, the total output power is

$$P_t = P_{\text{t\_single}} + 10 \cdot \log_{10}(N_t) \tag{1.3}$$

the transmitter and receiver antenna gain are

$$G_t = G_{\text{t\_single}} + 10 \cdot \log_{10}(N_t) \tag{1.4}$$

$$G_r = G_{\text{r\_single}} + 10 \cdot \log_{10}(N_r) \tag{1.5}$$

the total received signal in dBm is

$$P_r(dBm) = P_{\text{t\_single}} + G_{\text{t\_single}} + G_{\text{r\_single}} + 20 \cdot \log_{10}\left(\frac{\lambda}{4\pi \cdot d}\right) + 20 \cdot \log_{10}(N_t) + 10 \cdot \log_{10}(N_r) \tag{1.6}$$

By employing phased-array technique, the millimeter-wave band is promising for an evolutionary improvement on wireless communication. Recently deployed 5G new radio (5G NR) are located at 28GHz band and 39GHz band, which makes millimeter-wave a reality.

1.2 Millimeter-Wave Circuits in CMOS Technology

The silicon technologies, especially CMOS technology, has a great advancement, which improves the performance of digital computation and signal-processing integrated circuits. Specifically, the digital circuits benefit most from technology scaling. The speed is increased and power consumption is decreased due to the technology scaling. The CMOS technology enables most of the RF functions in wireless system since 1990s thanks to the ground breaking research. The wireless system-on-chip (SoC) realized in the digital CMOS technology enables compact solution for mobile devices. The SoCs implemented in CMOS technology shows reduced cost, system complexity and power consumption compared with the traditional multi-chip-module (MCM) approaches. The CMOS SoCs can also enhance the system robustness thanks to on-chip calibration, built-in self-test

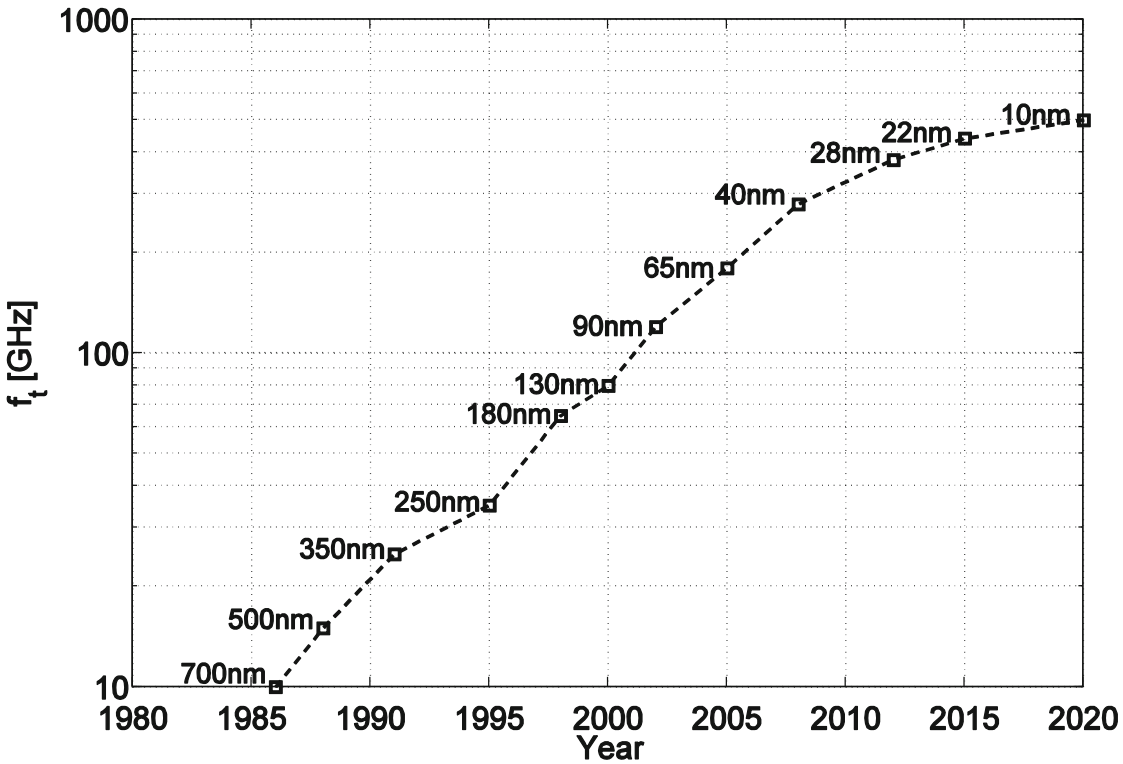


Figure 1.2: CMOS ft of technology nodes over the years.

(BIST), and self-healing schemes with assistance of monolithically integrated digital circuits. Furthermore, new system architectures and topologies with better performance over the conventional integration methods are enabled due to the availability of digital functions.

It has been researched and developed for two decades that the silicon technologies can be used for integrating large-scale complex millimeter-wave wireless systems. The early works to realize integrated complex millimeter-wave transceivers with standard silicon technologies [5–8] are done by California Tech, [9, 10] by IBM, [11, 12] by UC-Berkeley, [13, 14] by UCLA at the years around the middle 2000s. In recent decade, many other works from more groups are published like [15] by Georgia Tech, [16–19] by UCSD, [20, 21] by National Taiwan University, [22] by Intel, and [23–28] by Tokyo Institute of Technology. With the significant contributions and developments made by research groups, the feasibility of monolithic integrated millimeter-wave wireless transceiver in deep micron silicon technology is greatly demonstrated.

Figure 1.2 shows a graph of the evolution of the gate length and the maximum frequency of current gain (ft) of CMOS technologies over the years. Note that the ft is increased from several gigahertz in the 1980s up to hundreds of gigahertz for todayąŕs

nanometer-scale CMOS technologies. This speed increase of the transistors enables the implementation of millimeter-wave circuits in a standard CMOS technology.

The ability to design millimeter-wave front ends in a CMOS process creates numerous advantages. Integration of the front end together with digital processing circuits enables the design of new millimeter-wave architectures with direct digital modulation schemes. This reduces system complexity, power consumption, and it avoids the high-speed digital interface between a digital chip and a millimeter-wave chip implemented in a III-V RF technology. These single CMOS chip solutions also reduce the production cost for mass-market consumer applications, which perfectly fits the exponential growth of the wireless data communication market for consumer applications. Although the ft and $f_{\max}$ of CMOS technologies have increased toward several hundreds of gigahertz, it will still be a challenge to implement high-performance and efficient millimeter-wave front ends.

1.3 Overview of this Thesis

As shown in Figure 1.3, this thesis focuses on achieving high speed wireless communication using CMOS technology in the millimeter-wave frequency bands. In order to achieving high data rate, the millimeter-wave frequency bands are attractive due to the multi-GHz bandwidth can be allocated for wireless communication. In addition to wider bandwidth, the spectral efficiency is also one of the most important consideration in the system design. Employing high order modulation scheme can achieve higher data rate within the same bandwidth, however, it also requires high SNR as given by equation (1.1), where SNR represents high order modulation scheme. Therefore, high SNR transceiver design is the key point of the whole system plan. Another way to increase the signal spectral efficiency is to reduce the signal bandwidth without reducing the data rate. This thesis focuses on this two direction and gives detailed analysis and discussion.

The Chapter 2 of the thesis starts the design consideration of the wireless transceiver in millimeter-wave bands. It includes widely used device modeling and basic function of each building blocks in the transceiver. Chapter 3 includes millimeter-wave power amplifier design targeting high linearity and high output power, which is to be used in Chapter 4. The Chapter 4 introduces phased-array transceiver design for 5G New Radio 28 GHz and 39 GHz bands with calibration consideration. Chapter 5 explains the bandwidth reduction technology which enables doubled data rate and low power consumption at 60 GHz. Conclusion and future works are included in the final chapter.

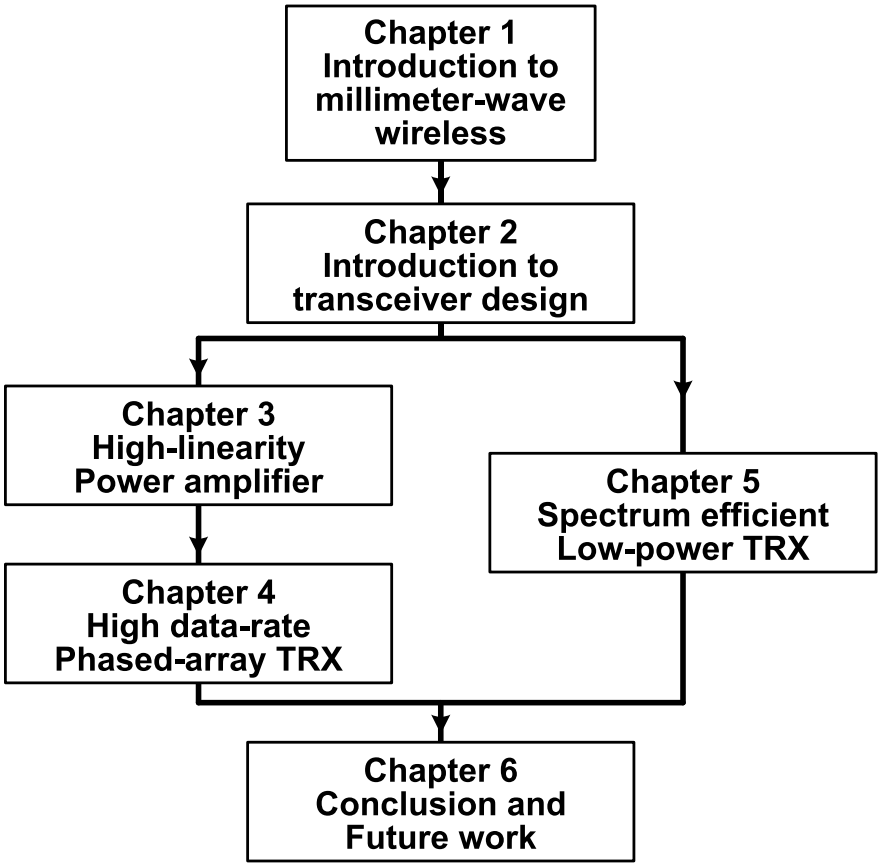


Figure 1.3: Thesis organization.

Chapter 2

Millimeter-Wave Transceiver Design

The CMOS millimeter-wave transceiver design usually starts with device modeling, since the process design kits (PDKs) provided by foundry are modeled up to around 20 GHz. Due to the parasitic components effect, the transistor maximum available gain will drop inversely proportional to the operation frequency; the inductor and capacitor will easily enter the self-resonant frequency. Therefore, it is quite difficult to obtain certain high gain, capacitance and inductance value, not to mention the accuracy. Fortunately, thanks to the short wavelength at millimeter-wave frequency, the on-chip transmission lines are feasible to be integrated monolithically. This chapter will introduce the measurement-based in-house PDKs including transmission line and customized-layout transistor.

The millimeter-wave transceiver building blocks design requirements and challenges are discussed in this chapter. To achieve high data rate, the RF front-ends need to be designed with wideband characteristic. The LO synthesizer is required to cover the entire operation band with low phase noise. The power amplifier needs to provide high linearity and high output power.

In order to evaluate the overall millimeter-wave transceiver system performance, the signal-to-noise-and-distortion ratio (SNDR) is analyzed based on RF front end characteristics. The key challenges of millimeter-wave transceiver design are given in this chapter.

2.1 Devices Modeling and Characterization

2.1.1 Transmission line models

The passive components play important roles in the RF circuit impedance matching blocks. For example, the LNA first stage source impedance matching will contribute the most on the receiver overall noise figure. However, the PDK models of on-chip passive com-

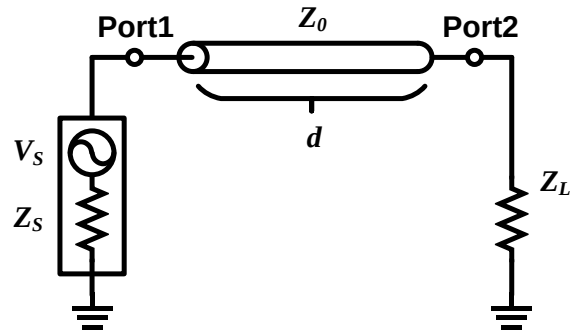


Figure 2.1: Transmission line model.

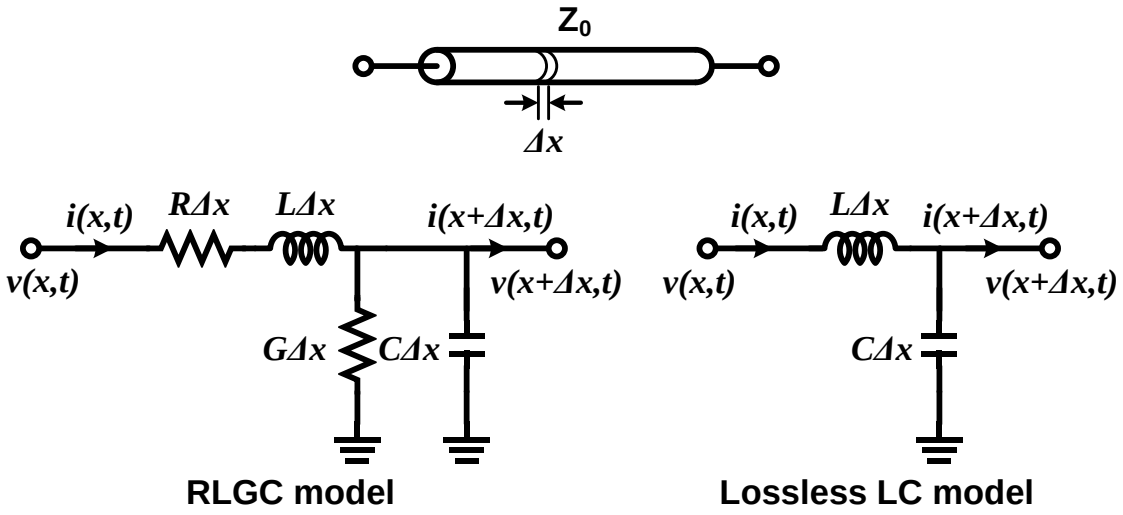


Figure 2.2: Transmission line distributed circuit model.

ponents, especially the inductor, provided by the foundry are less accurate at millimeter-wave frequency bands. Impedance matching using LC network is the most common way in the low-frequency RF circuit design, and it is becoming challenging with the frequency increase to millimeter-wave band.

An alternative way to accomplish the impedance matching is by using transmission line [29]. The transmission line is popular in RF integrated circuit design due to its fixed on-chip physical structure and accurate impedance transforming. The transmission line model is shown in Figure 2.1. The transmission line is a two-port network with a characteristic impedance of Z_0. The transmission line port 1 is connected to a source input with its source impedance of Z_S. The transmission line port 2 is connected to output with its load impedance of Z_L. A distributed circuit model is analyzed to characterize the transmission line. As shown in Figure 2.2, the transmission line distributed circuit model can

be expressed using RLGC model. Due to the transmission line R and G are negligible, a simplified lossless LC model is used for ideal transmission line with $R = G = 0$. The voltage and current along the transmission line are given

$$v(x,t) = Re\left[V(x)\,e^{j\omega t}\right] \tag{2.1}$$

$$i(x,t) = Re\left[I(x)\,e^{j\omega t}\right] \tag{2.2}$$

The equations gives

$$\frac{d^2V(x)}{dx^2} = \left(-\omega^2 LC\right)V(x) = -\beta^2 V(x) \tag{2.3}$$

where $\beta = \omega\sqrt{LC}$ is known as propagation constant. The general solution $I(x)$ can be derived as

$$I(x) = \frac{\beta}{\omega L}\left[Ae^{-j\beta x} - Be^{j\beta x}\right] \tag{2.4}$$

Defining the transmission line characteristic impedance as

$$Z_0 = \frac{\omega L}{\beta} = \sqrt{\frac{L}{C}} \tag{2.5}$$

It can be observed that the transmission line characteristic impedance value is real.

A transmission line with characteristic impedance of Z_0 and length of d in the matching network is shown in Figure 2.3. The input impedance of transmission line at any distance d is defined as:

$$Z_{IN}(d) = \frac{V(d)}{I(d)} = Z_0\frac{(Z_L + Z_0)\,e^{j\beta d} + (Z_L + Z_0)\,e^{-j\beta d}}{(Z_L + Z_0)\,e^{j\beta d} - (Z_L + Z_0)\,e^{-j\beta d}} \tag{2.6}$$

$$= Z_0\frac{Z_L + jZ_0\tan\beta d}{Z_0 + jZ_L\tan\beta d} \tag{2.7}$$

In a short terminated transmission line ($Z_L = 0$), the input impedance is given by

$$Z_{IN}(d) = jZ_0\tan\beta d \tag{2.8}$$

In an open terminated transmission line ($Z_L = \infty$), the input impedance is given by

$$Z_{IN}(d) = \frac{Z_0}{j\tan\beta d} \tag{2.9}$$

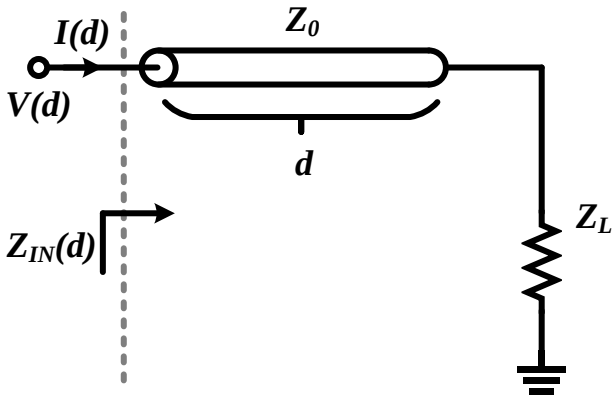


Figure 2.3: Transmission line input impedance at any distance d.

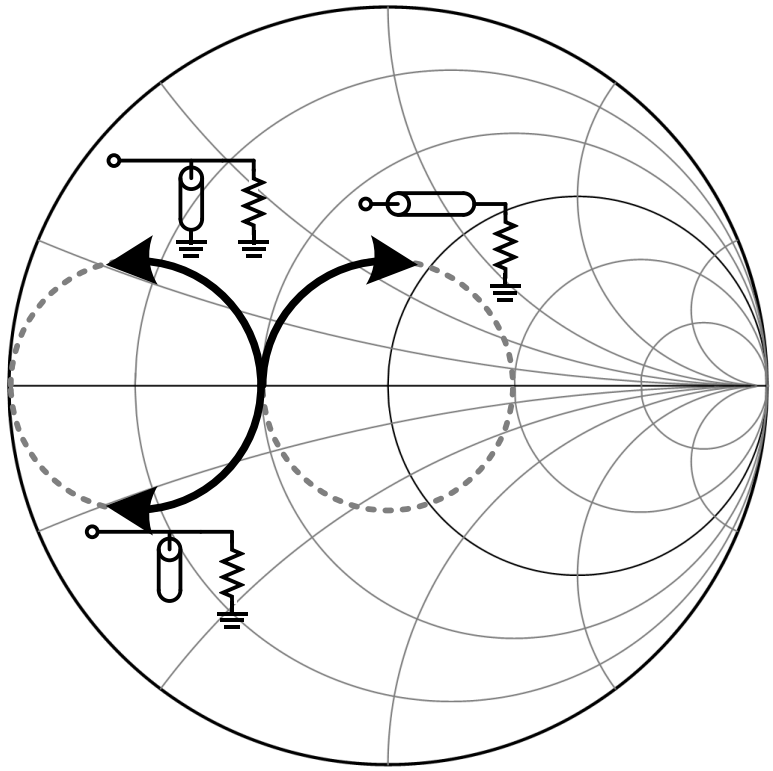


Figure 2.4: Transmission line matching networks.

The short and open terminated transmission lines are useful in RF matching networks. The short transmission line stub can be regarded as a shunt inductor, and the open transmission line stub can be regarded as a shunt capacitor.

The transmission line matching can be demonstrated in a Smith chart. Figure 2.3 shows the input impedance of the series, short stub and the open stub transmission line

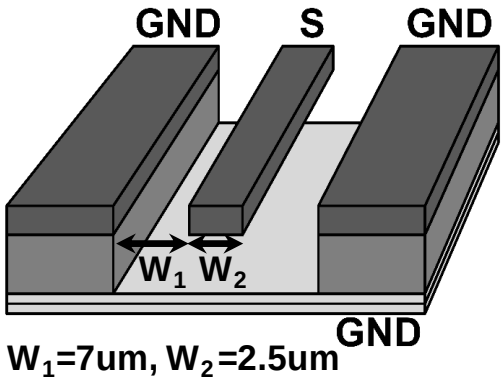


Figure 2.5: Transmission line CPWG structure cross view.

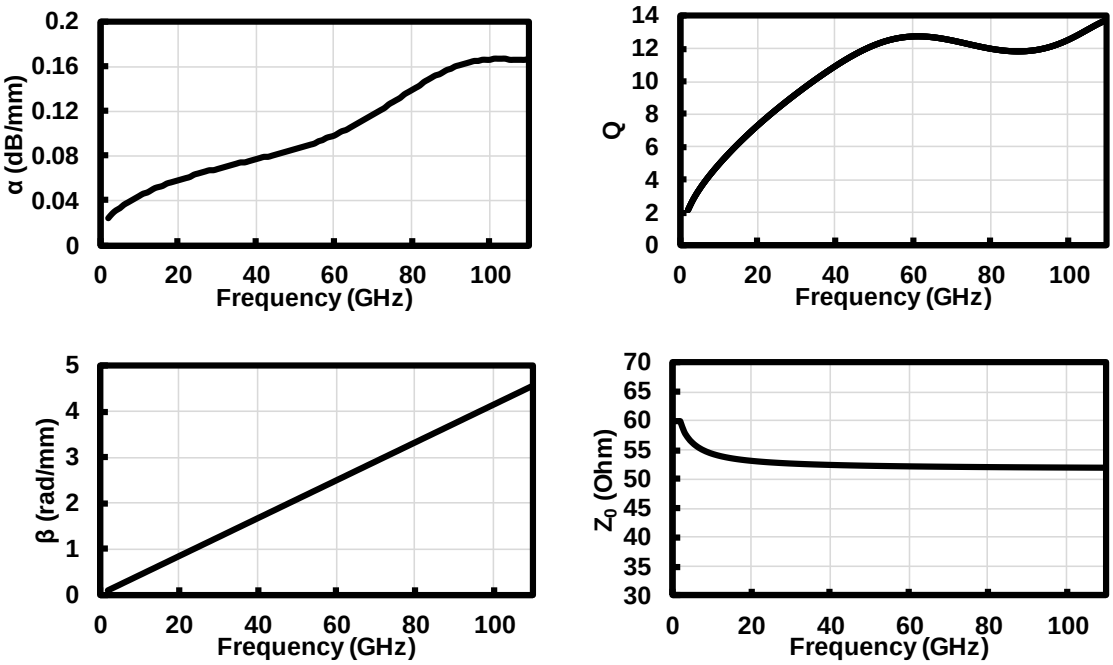


Figure 2.6: Transmission line measured and de-embedded attenuation constant (α), phase constant (β), quality factor (Q), and characteristic impedance (Z_0)..

transforming the load impedance of Z_L. By using transmission line, the RF matching LC components can be replaced, except the DC-cut capacitor.

Another important transmission line is the quarter-wave transmission line, with $d = \lambda/4$. The quarter-wave transmission line can be used for electrostatic discharge (ESD) and supply circuits.

It can be cleared observed in Figure 2.4 that the transmission line can match the load impedance to any desired impedance by employing series, short stub and open stub.

It will be extremely useful to realize the matching networks by using the on-chip transmission line, especially at the millimeter-wave frequency. With the frequency increase, the required transmission line length d for matching also shrinks. Therefore, the on-chip transmission line matching benefits from the following features: The fixed physical structure, which is invariant with PVT conditions, the highly-accurate impedance matching, and the flexible layout.

The measurement-based in-house transmission line PDK is developed. Figure 2.5 shows the cross view of the in-house transmission line structure. The transmission line is coplanar-waveguide-with-lower-ground-plane (CPWG) structure with top metal width of 2.5um and coplanar gap distance of 7um. The coplanar ground and the lower ground are connected through via. The transmission line size is optimized to 50-Ohm for compatibility with 50-Ohm design system.

The transmission line standalone test element groups (TEGs) with different lengths are implemented for characterization. L-2L method is used for de-embedding the transmission line characteristics in unit length. The measured and de-embedded transmission line unit length attenuation constant (α), phase constant (β), quality factor (Q), and characteristic impedance are shown in Figure 2.6 [30]. The transmission line is modeled up to 110 GHz which covers the 5G NR band and 802.11ay 60GHz band. With the in-house transmission line model, a compact and accurate matching network can be realized at millimeter-wave frequency without using LC components.

2.1.2 Transistor models

The transistor model provided by foundry PDK also lacks of accuracy at high frequency as well as models for inductor and capacitor. The in-house transistor modeling method

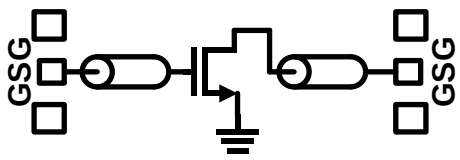


Figure 2.7: TEG for transistor modeling.

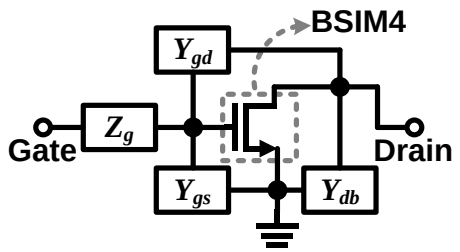


Figure 2.8: Transistor model with parasitic parameters.

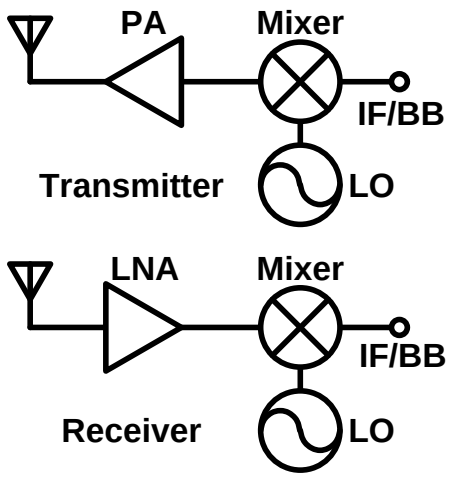


Figure 2.9: Simplified wireless transceiver architecture.

is introduced in [31]. The transistor model consists of a BSIM4 model from foundry, Y parameters for C_{gs}, C_{gd} and C_{db}, and Z parameter for gate resistance Z_g. The advantage of the modeling method is that it takes the gate parasitic into account to accurately predict the linearity and noise performance against different frequency and bias conditions. The implemented TEG for transistor modeling is shown in Figure 2.7. The gate bias and VDD supply are provided externally by bias junction. The transmission line is used to connect transistor gate and drain to pads. The transistor model measurement data can be obtained de-embedding the transmission line and pads. The detailed transistor model with parasitic parameters is shown in Figure 2.8. The in-house transistor PDK contains variant transistor sizes with their width from 12 um to 120 um for different drive abilities.

2.2 Building Blocks in Millimeter-Wave Transceiver

The main building blocks in a wireless transceiver as shown in Figure 2.9 are introduced in this section, containing power amplifier (PA), low noise amplifier (LNA) and local oscillator (LO). The fundamentals of the building blocks are described here.

2.2.1 Power Amplifier

The power amplifier is usually at the last stage of a transmitter, and it amplifies the RF signal large enough to be emitted by an antenna. The power amplifier design is one of the most critical part in a transmitter. A power amplifier can be Evaluated by the saturate output power (P_{SAT}), 1-dB compression point (P_{1dB}), peak efficiency, back-off efficiency,

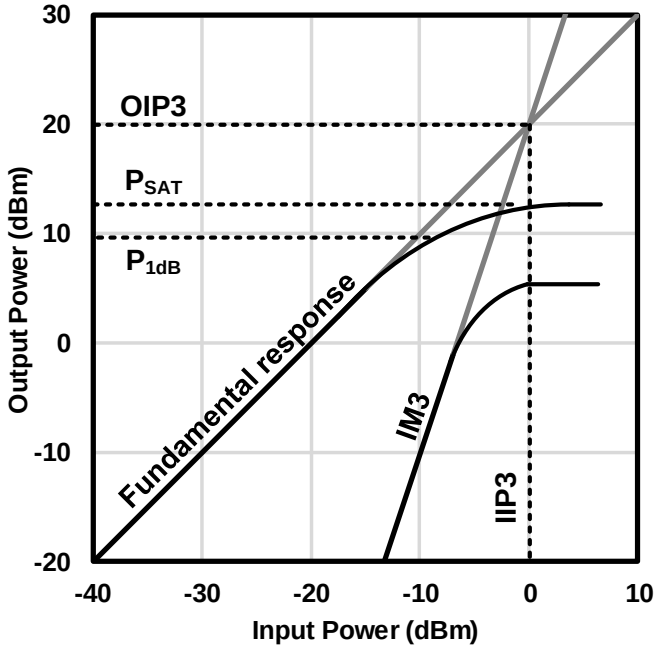


Figure 2.10: Power amplifier linearity.

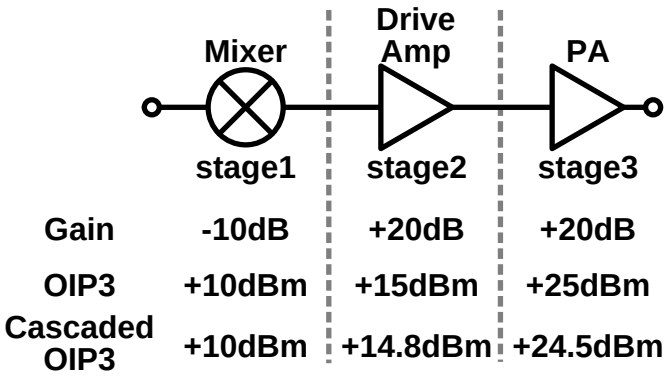


Figure 2.11: Transmitter cascaded OIP3.

linearity, gain, frequency response, stability, power consumption, etc. The transmitter system overall linearity is usually limited by the power amplifier, since the transmitter always try to drive the power amplifier into the edge of linear region. As illustrated in the Figure 2.10, the power amplifier linearity can be represented by output third-order intercept point (OIP3). The power amplifier third-order intermodulation (IM3) tone is produced by the non-linear effect. It can be observed that the higher OIP3 leads to the smaller IM3, which means the amplifier output contains less non-linear tones and high linearity. The transmitter three-stage cascaded OIP3 can be expressed as:

$$\frac{1}{OIP3} = \frac{1}{OIP3_1 \cdot G_2 \cdot G_3} + \frac{1}{OIP3_2 \cdot G_3} + \frac{1}{OIP3_3} \tag{2.10}$$

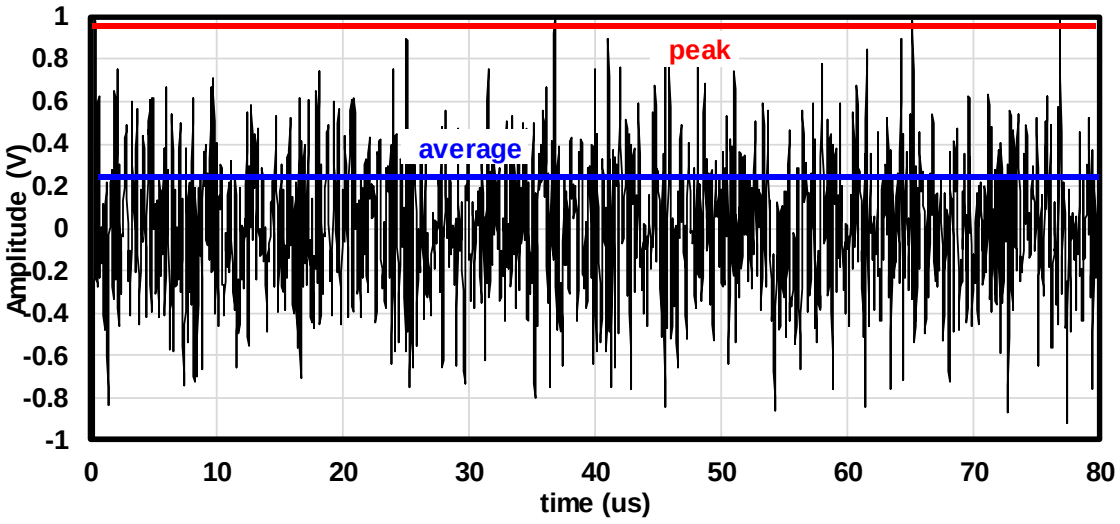


Figure 2.12: Non-constant envelope 64QAM OFMD signal waveform.

Table 2.1: Constellation PAPR for different modulation schemes

Modulation Scheme	PAPR of ideal constellation (dB)	PAPR of signal after SRRC filter (α=0.35) (dB)
QPSK	0	4
8PSK	0	4
16QAM	2.6	6.6
64QAM	3.7	7.7
256QAM	4.2	8.8

where $OIP3_N$ and G_N denote the OIP3 and gain in each stage. From Eq. (2.10), it can be observed that the final stage $OIP3_3$ has a dominant contribution on the system cascaded overall OIP3. In other words, the power amplifier linearity performance decides the entire transmitter linearity performance. On the other hand, a high-output-power high-linearity power amplifier is usually power hungry, which makes the efficiency to be a more critical parameter than in other building blocks.

The power amplifier design differs from the input signal applied to it. Mainly there are two kinds of signal needs to be taken into account: constant envelope signal, non-constant envelope signal. For constant envelope signal, the switching power amplifier and saturated power amplifier can be employed, since the magnitude and phase distortion cause less degradation on constant envelope signal quality.

Figure 2.12 shows a general non-constant envelope signal waveform. The linearity performance of a power amplifier is of great concern when amplifying a non-constant

envelope signal. The signal envelope fluctuation is quantified by peak-to average power ratio (PAPR), which is defined as the ratio of signal peak power and average power. The constellation PAPR of some well-known modulation schemes are shown in Table 2.1. The power amplifier must be at least linear when the peak power is applied, which requests the power amplifier operates at a certain output power level back-off from the saturated output power.

2.2.2 Low Noise Amplifier

The low noise amplifier is the device amplifying extremely small signal to be large enough power level before processing to the next block. Therefore, the low noise amplifier is the first building block after antenna in a receiver system. The additive white Gaussian noise (AWGN) will be added to the received small signal after amplifier. Noise factor (F) is used to quantize the signal quality degraded by noise introduced in any components, and it is defined as below:

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_i}{SNR_o} \tag{2.11}$$

where S_i, So denotes the input and output signal power, N_i, N_o denotes the input and output signal power. The noise figure (NF) is defined as the noise factor in dB:

$$NF = 10 \cdot \log_{10}(F) \tag{2.12}$$

The three-stage cascaded noise figure of a system can be found with Friisą́ formular for noise:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} \tag{2.13}$$

The receiver cascaded noise figure is demonstrated in Figure 2.13. It can be observed that, with sufficient high gain, the receiver overall noise figure is dominated by first stage low noise amplifier. Therefore, a low noise amplifier is required to obtain low noise and its gain needs to be high enough to minimize the receiver overall noise figure. The noise figure of the receiver is directed related with the receiver sensitivity, which is a fundamental limit of the transceiver link distance.
The noise factor of a two-port amplifier can be obtained with:

$$F = F_{min} + \frac{4r_n \left|\Gamma_s - \Gamma_{opt}\right|^2}{\left(1 - |\Gamma_s|^2\right)\left|1 + \Gamma_{opt}\right|^2} \tag{2.14}$$

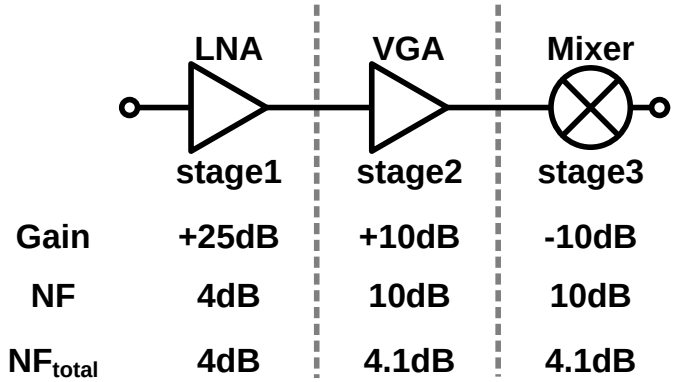


Figure 2.13: Receiver cascaded noise figure.

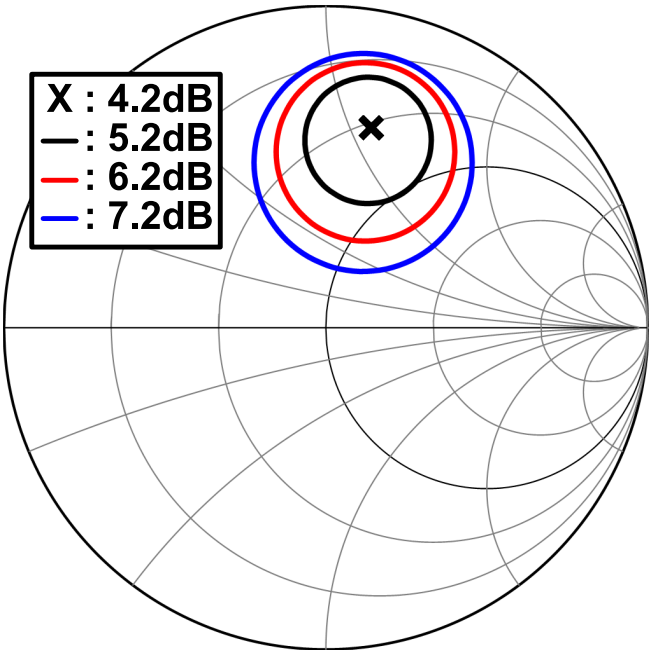


Figure 2.14: LNA typical noise figure circles in the Γ_s plane .

where r_n is the equivalent normalized noise resistance of the input port, F_{min} can be determined using a network analyzer, and Γ_s is defined as the source matching reflection coefficient with source impedance of Z_s:

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{2.15}$$

and Γ_{opt} is associated with F_{min}, represents the optimal source matching reflection coefficient with optimal impedance of Z_{opt}:

$$\Gamma_{opt} = \frac{Z_{opt} - Z_0}{Z_{opt} + Z_0} \tag{2.16}$$

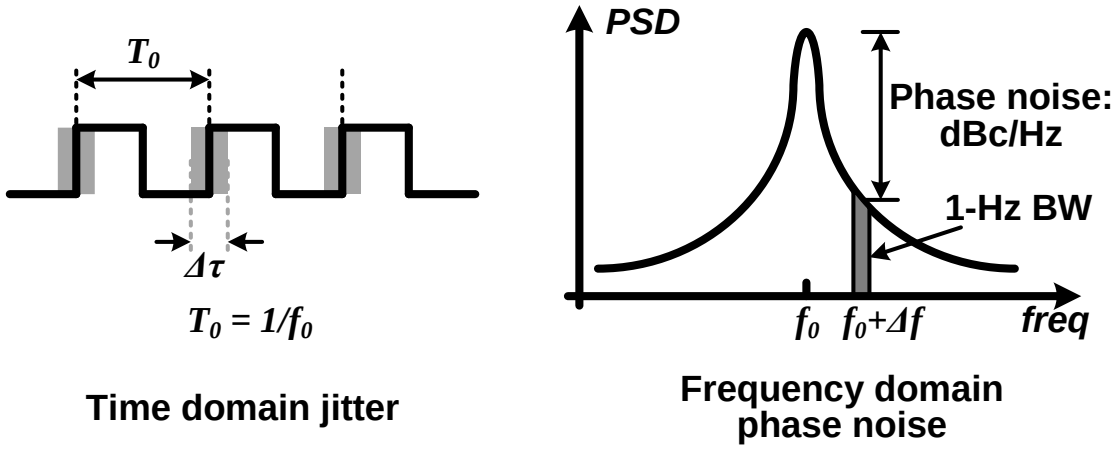


Figure 2.15: Local oscillator phase noise effects.

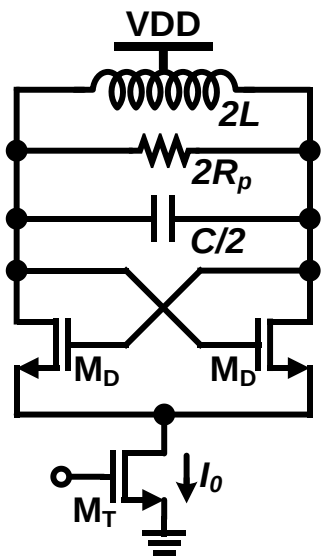


Figure 2.16: Tail-current biased differential LC VCO.

Figure 2.14 shows a typical noise figure circles of a low noise amplifier, with its F_{min} = 4.2dB and 1-dB noise circle step. The low noise amplifier matching is required with impedance around optimal impedance, and leads to the minimum noise figure.

2.2.3 Local Oscillator

The role of a local oscillator is to provide a common reference frequency signal for frequency conversion or synchronization. An ideal local oscillator is a single tone sinusoid wave with constant amplitude and phase. However, the practical local oscillator cannot be

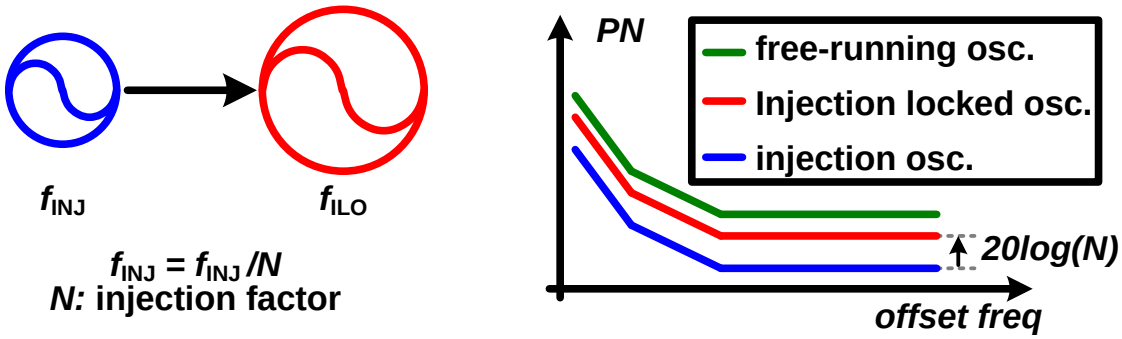


Figure 2.17: Injection locked oscillator mechanism.

designed with pure single tone output due to the additive noise in any electronic circuits. Noise contains components at many frequencies, so its phase with respect to the main tone is random, and its amplitude is also random. The noise phase component and amplitude component are phase modulation (PM) and amplitude modulation (AM) applied to the ideal tone. Generally, the AM can be removed by applying a limiting amplifier which clips the voltage. However, since it cannot clip the time information, the noise PM component is unaffected. Phase noise is used to quantify the noise PM effect on a local oscillator. As illustrated in Figure 2.15, the phase noise is defined as the 1-Hz bandwidth noise power ratio at offset frequency to the carrier power ratio. A tail-current biased differential LC voltage controlled oscillator (VCO) is the dominant local oscillator in RF application owing to its robust operation. The differential LC oscillator phase noise performance has been well analyzed by many papers, the total phase noise can be expressed as

$$\mathfrak{L}(\omega_m) = \frac{4kTR_p}{V_1^2}\left[1 + \frac{2\gamma I_0 R_p}{\pi V_1} + \frac{\gamma I_0 R_p}{2V_{eff}}\right]\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \tag{2.17}$$

where the R_p, V_1, V_{eff}, Q, ω_0 and ω_m denotes resonator parallel resistor, fundamental voltage, effective voltage including harmonics, resonator quality factor, center frequency and offset frequency. It can be observed that the oscillate voltage and resonator quality has the highest improvement on phase noise due to their square law effect. However, the oscillate voltage is limited by supply voltage, the differential oscillator is usually designed to operate at supply limit region for lower phase noise. The resonator quality factor Q is critical in an oscillator design, especially at millimeter-wave frequencies.

The on-chip resonator at millimeter-wave frequencies cannot achieve high quality factor due to the parasitic components, thus a VCO designed with its fundamental frequency running at millimeter-wave bands always suffers from the noise figure performance. The

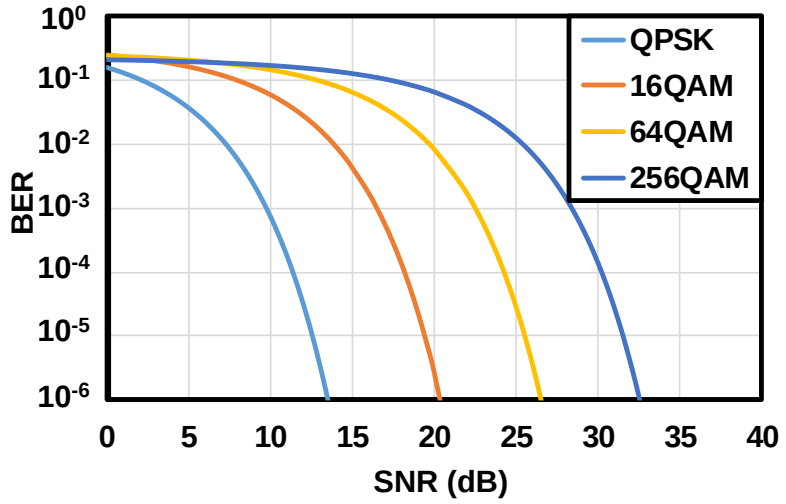


Figure 2.18: SNR requirement on different modulation scheme.

injection locked oscillator (ILO) is one of the best solution for implementing a millimeter-wave local oscillator by using a sub-harmonic oscillator running at lower frequency inject to a millimeter-wave oscillator [32–34]. The injection locked oscillator mechanism is shown in Figure 2.17. The injection locked phase noise is related with the sub-harmonic injection oscillator:

$$PN_{\mathrm{ILO}} = PN_{\mathrm{INJ}} + 20 \cdot \log_{10}(N) \tag{2.18}$$

where N is the injection factor. The higher N leads to the lower injection oscillator phase noise and narrower locking range.

2.3 System Signal-to-Noise Ratio Analysis

This section discussed the system requirements on each building blocks' design. The wireless communication channel capacity is theoretically limited by the bandwidth of the signal. For a given bandwidth, the maximum data rate R_b that can be achieved is expressed as:

$$R_b = BW \cdot \log_2(M) \cdot \frac{1}{(1+\alpha)} \tag{2.19}$$

where M denotes M-QAM modulation order, ęÁ is the roll-off factor. The higher data rate can be achieved when employing higher order QAM modulation, which also increases

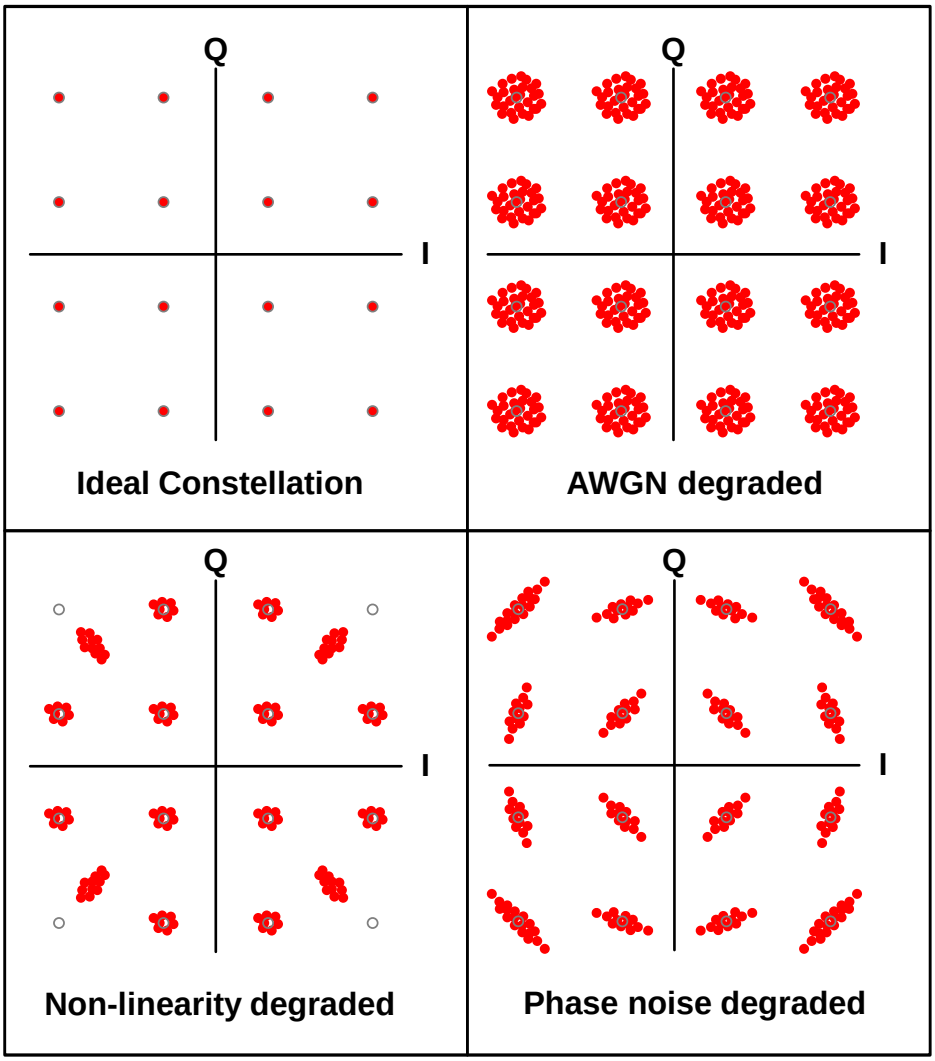


Figure 2.19: 16QAM modulation constellation EVM degraded by AWGN, non-linearity and phase noise.

higher requirements on the each building blocks. The required system signal-to-noise ratio (SNR) for certain bit-error-rate (BER) and the different modulation orders can be approximately expressed as:

$$BER \approx \frac{4}{\log_2(M)}\left(1-\frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3}{M-1}\cdot SNR}\right) \tag{2.20}$$

where Q is the Q-function. Figure 2.18 plots the SNR requirement for modulation scheme QPSK, 16QAM, 64QAM and 256QAM.

As we discussed in previous section, each individual building block has its design require-

ment, the system SNR should be considered including the critical blocks such as power amplifier and local oscillator. Constellation EVM is usually used to evaluate a system overall performance with complex modulation scheme. The main factors that degrade the system overall EVM are the linearity, noise figure and LO phase noise. The system overall EVM can be expressed as:

$$EVM_{\text{system}} = \sqrt{\frac{1}{SNR^2_{\text{system}}}} = \sqrt{\frac{1}{SNR^2_{\text{AWGN}}} + \frac{1}{SDR^2} + \varphi^2_{\text{PN,RMS}}} \tag{2.21}$$

where SNR_{AWGN} is the signal-to-AWGN-noise ratio, SDR is the signal-to-distortion ratio which represents the non-linearity. The $\varphi^2_{\text{PN,RMS}}$ is the integrated phase noise of the local oscillator.

Figure 2.19 shows the 16QAM modulation constellation EVM degraded by AWGN, non-linearity and phase noise in comparison with the ideal constellation. The AWGN noise degrades the EVM by introducing random noise on each mapping point, so that the constellation mapping points are scatter from the ideal point. The higher system noise figure leads to the bigger scattering constellation mapping points. Once the noise figure is large enough to scatter the points jump to the neighbor mapping points, the demodulation bit error occurs. The non-linearity degradation happens when the system drives modulation signal into non-linearity region; in this case, the constellation will collapse from the edge. The higher modulation order requires the higher SDR to overcome the non-linearity degradation on constellation. The phase noise degradation makes the constellation mapping points rotates randomly around the origin. If the phase noise is large enough, the points will move to another neighbor mapping region and create bit error.

Chapter 3

High-Power High-Linearity Millimeter-Wave Power Amplifier

This chapter discusses the high-power high-linearity power amplifier design for 28GHz and 39GHz 5G NR bands. The millimeter-wave power amplifier design consideration is discussed at first including amplifier introduction, operation classes. Secondly, power amplifier architectures are discussed for picking suitable architecture for PA operating at millimeter-wave frequencies. Next, the amplifiers designed targeting 28 GHz and 39 GHz 5G NR bands are simulated and implemented. The measurement results of proposed power amplifiers are compared with the state-of-the-art millimeter-wave amplifiers in literature for 5G application. Finally, a conclusion is briefly presented.

3.1 Millimeter-Wave Power Amplifier Design Consideration

3.1.1 Power Amplifier Introduction

As briefly discussed in chapter 2, the power amplifier is one of the most important component in a wireless transceiver. The one stage power amplifier structure with 50Ω source impedance and 50Ω load impedance is shown in Figure 3.1. The output matching block transforms the 50Ω real impedance to complex conjugate value of the transistor output impedance.

The power transistor in shown in Figure 3.1 is the core component of the power amplifier. The 65-nm CMOS transistor f_t and f_{max} are about 200GHz, which makes it challenging to provide a high output power and a reasonable gain. With the transistor size increasing, the parasitic capacitance also increases and the operation frequency drops due

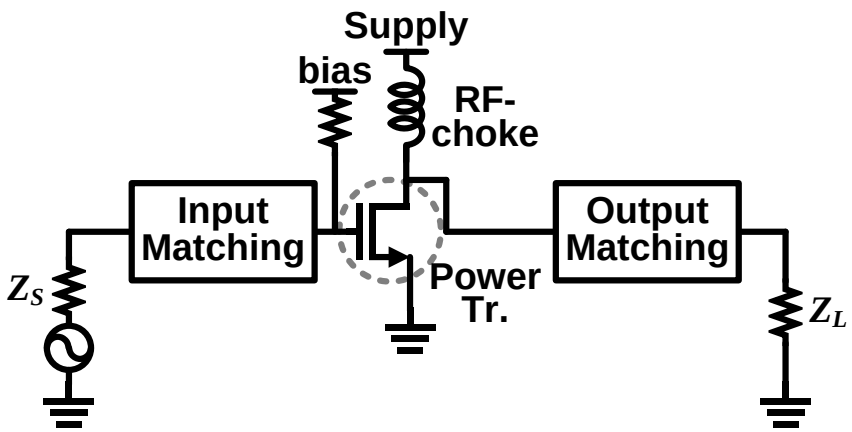


Figure 3.1: Generic power amplifier structure.

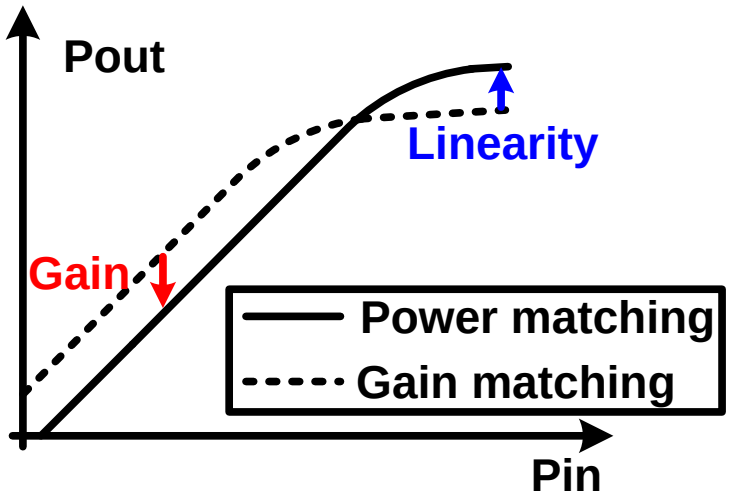


Figure 3.2: Typical relationship of power matching and gain matching.

to the large parasitic capacitance. Therefore, the transistor size need to be optimized for gain, output power. The power amplifier bias circuit sets the amplifier operation class, the VDD supply uses RF-chock inductor. At millimeter-wave frequency, the RF-chock inductor is also a part of matching block due to its lower low inductance.

3.1.2 Power Matching and Operation Class

The matching blocks transforms the source or load impedance to the desired impedance that extracted from power transistor. The ideal LC or transmission line matching is lossless, however, due to the low quality factor at high frequency, the matching block typically introduce 1-dB insertion loss. A complex high loss matching network at millimeter-wave frequencies has no improvement on power amplifier overall performance even the power transistor delivers higher output power. The power amplifier matching network prefers the

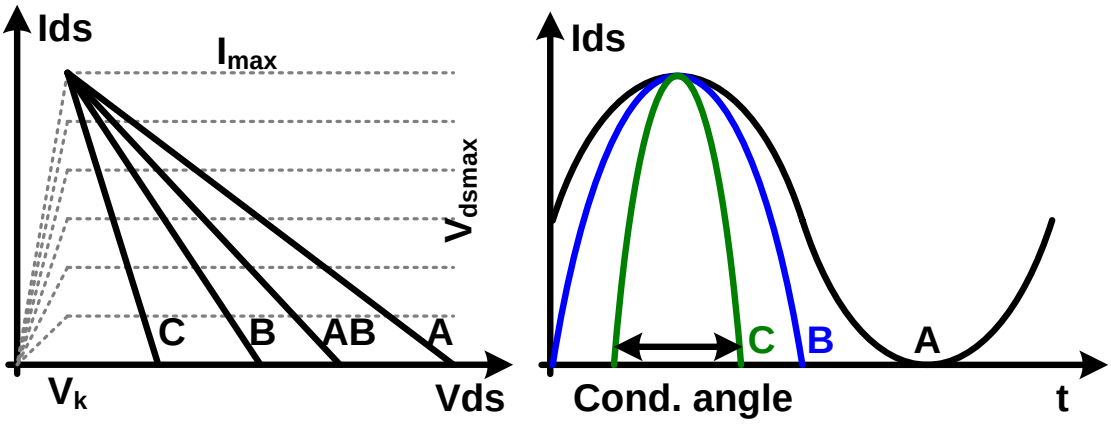


Figure 3.3: Power amplifier operation class load line and conduction angle.

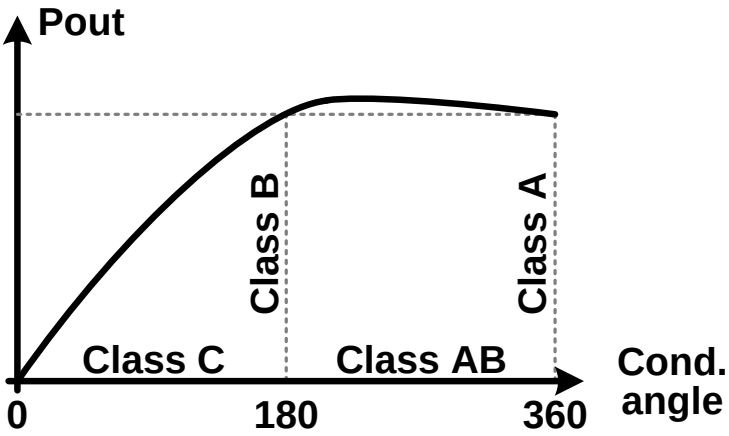


Figure 3.4: Power amplifier fundamental frequency output versus conduction angle.

power matching than the gain matching. The maximum gain impedance matching delivers the highest gain, when the amplifier is operating in a low-signal mode, it is encouraged to increase the gain in the design regardless of the amplifier linearity. However, when the amplifier is operating in a large-signal mode, the matching blocks have a great influence on linear region. Usually the gain matching and the power matching are not with the same impedance, it makes a tradeoff between the amplifier gain and linearity. Figure 3.2 shows the typical relationship of the amplifier power matching and gain matching. Figure 3.3 shows the power amplifier operation class versus the conduction angle. The power amplifier maximum efficiency improves when decreasing the conduction angle, on the other hand, the harmonic tones are generated with smaller conduction angle. The class A amplifier has the lowest harmonic tones and the lowest efficiency. Figure 3.4 shows the output power versus the conductional. Class AB amplifier generates highest fundamental tone output power with reasonable maximum efficiency. Due to the speed constrains, it is challenging to design the switch mode power amplifier at millimeter-wave frequencies.

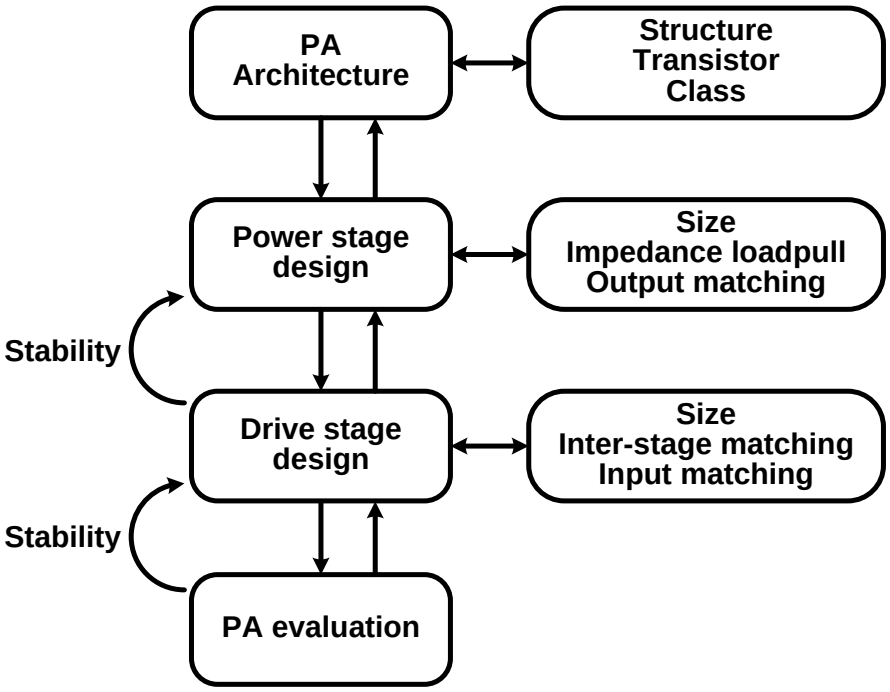


Figure 3.5: PA design process flow.

Therefore, millimeter-wave power amplifiers mostly operate at class AB mode for high linearity and maximum efficiency. The power amplifier design process is illustrated in Figure 3.5. Starting from the power amplifier architecture such as single-ended, differential, Doherty, stacked and power combined. The transistor topologies also need consideration for gain and linearity optimization. The power amplifier classes for high linearity is usually class AB at millimeter-wave frequencies. The power stage design is secondly focused, including transistor sizes, extracted load optimal impedance and the matching block design. The drive stage design concerns mainly the inter-stage matching with the power stage. The power amplifier should be designed unconditionally stable since it is easy to be oscillating at millimeter-wave frequencies.

3.2 Power Amplifier Architectures

The power amplifier architectures are introduced in this section. In order to obtain high output power and high efficiency, different architectures are used in PA design. However, the due to the low breakdown voltage, low available gain, and low quality factor of on-chip passive devices. The relationship between the breakdown voltage limitation and the CMOS technology node is discussed below. Figure 3.6 (a) and Figure 3.6 (b) show the

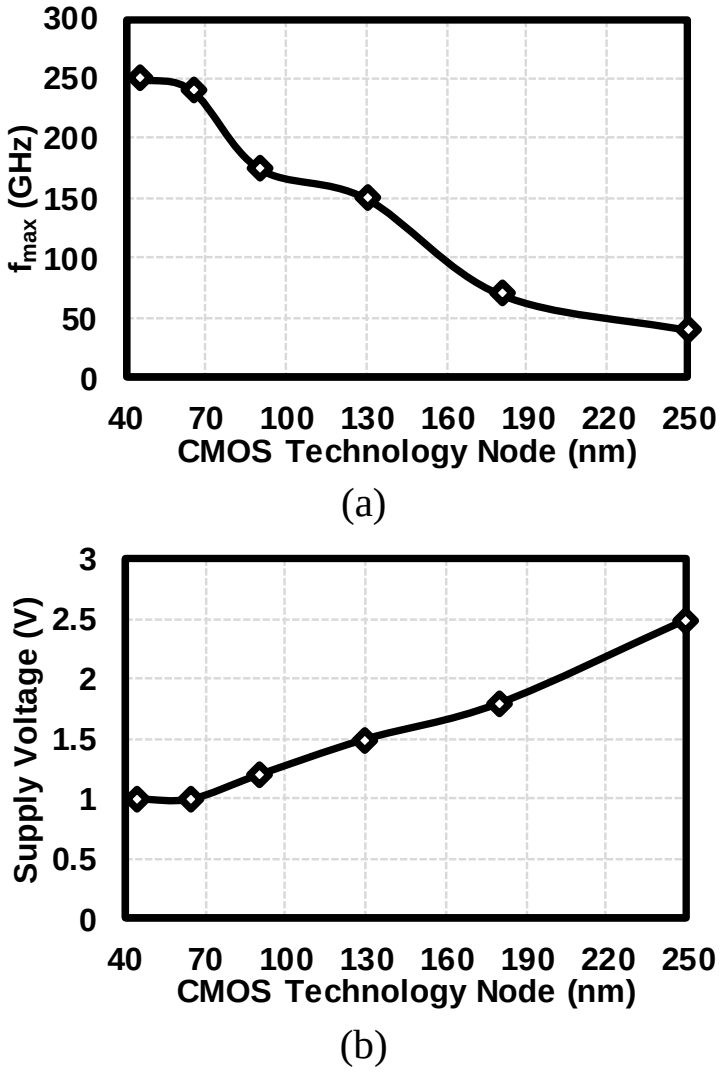


Figure 3.6: 28-GHz single-path differential power amplifier architecture.

$f_{\max}$ improvement and voltage supply with technology scaling. $f_{\max}$ is the characteristic of extrinsic device which includes series source, drain, input, and gate resistances, R_s, R_d, R_i, and R_g. $f_{\max}$ is defined as the frequency at which the power gain of the transistor is equal to unity under optimum matching conditions. The dominant factor of the series resistances is the gate resistance R_g, which can be minimized by using gate fingers. The RF amplification circuit usually operates at up to 1/2 of $f_{\max}$, and for high intrinsic gain, the amplifier usually operates at 1/5 of $f_{\max}$.

It can be experimentally found that with the technology scaling, the $f_{\max}V_{DD}^2$ is almost fixed to 250 GHzV^2. Assuming an amplifier is designed at $f_c = 1/5\ f_{\max}$, with 0V knee voltage and twice VDD peak-to-peak swing. Given

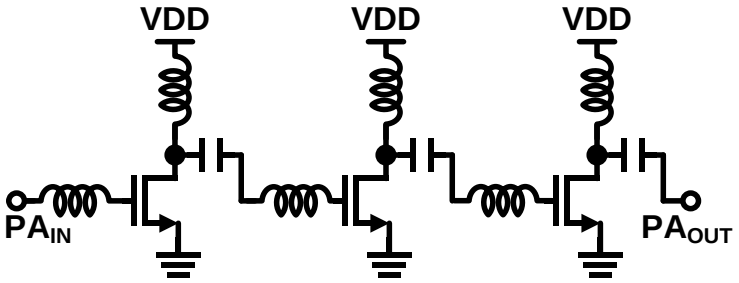


Figure 3.7: Three stage single-ended power amplifier.

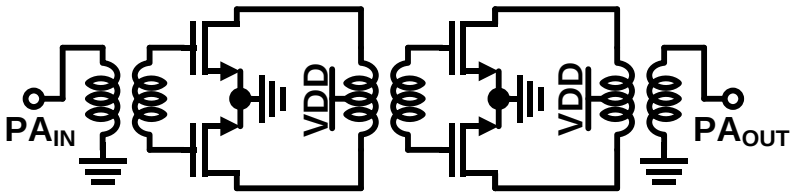


Figure 3.8: Two-stage differential power amplifier.

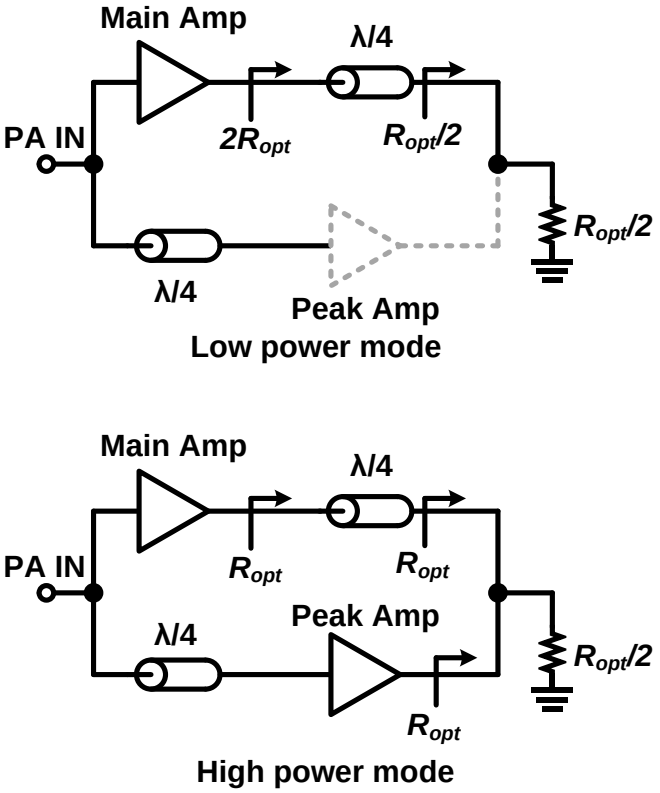


Figure 3.9: Doherty power amplifier.

$$f_{\max} V_{\mathrm{DD}}^2 = 250 \text{ GHzV}^2 \tag{3.1}$$

The power amplifier output power with 50-Ω P_{out} can be estimated as:

$$P_{\text{out}} = \frac{V_{\text{DD}}^2}{2 \cdot R_{\text{L}}} = \frac{250/f_{\max}}{2 \cdot 50} = \frac{250}{2 \cdot 50 \cdot 5 f_{\text{c}}} \tag{3.2}$$

$$= \frac{500}{f_{\text{c}}} \cdot \frac{\text{mW}}{\text{GHz}} \tag{3.3}$$

For operation frequency f_{c} around 1 GHz, the power amplifier can reach watt-class output power. However, when the operation frequency increases to millimeter-wave, the typical output power is around 12dBm at 30GHz. The power amplifier load can be reduced to an relatively low impedance to enable a higher output power, however, the matching network that transform the 50-Ω impedance to low impedance is lossy in CMOS process due to the poor quality factor of passive devices. There are several architectures can improve the power amplifier output ability.

3.2.1 Power Amplifier Architecture Introduction

Starting from the basic single-ended common-source architecture. The single-ended common source power amplifier is most common seen architecture due to its simplicity. Figure 3.7 shows the three stage single-ended power amplifier architecture. The amplifier stages are cascaded to obtain high enough gain. The number of stages depends on the gain requirement, however, the stages should be designed with increasing drive ability to avoid pre-saturation. The use of LC components for matching network offers high quality factor and low loss matching. The single-ended architecture output power is limited by the single transistor.

A differential architecture power amplifier can achieve higher output power. As shown in Figure 3.8, the two-stage power amplifier has symmetric two path for differential signal. The single-ended input is converted to differential by using the input balun, the inter-stage matching uses a transformer, which also provides VDD supply at the center tap of the transformer. The output impedance matching also employs a balun for converting the load impedance to desired impedance. In general, the differential power amplifier is 3-dB higher than a single-ended one. However, due to the higher insertion loss of the balun and unbalance of differential signal, the differential power amplifier linearity may be degraded.

Figure 3.9 shows the circuit architecture of the Doherty power amplifier. The Doherty power amplifier is a type of power backoff efficiency enhanced technique. The main amplifier is biased in class AB and the peak amplifier is biased in class C. When a Doherty amplifier operates in the low power mode, the main amplifier turns on and achieves the

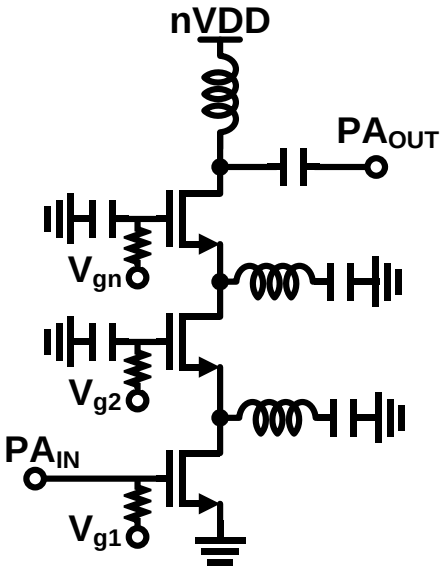


Figure 3.10: n-stacked power amplifier.

first peak efficiency with input power increase. Further increase the input power will turn on the peak amplifier, with 6-dB power increase, the Doherty amplifier reaches the second efficiency peak. The key technique to achieve such efficiency enhancement is to use the quarter-wave transmission line converting the impedance seen by the carrier amplifier go down from the ($2R_{\text{opt}}$) to (R_{opt}) as the peaking amplifier current increases. The main drawback of a Doherty power amplifier is the passive network which occupies large area and causes high loss.

In order to further increase the output power, stacking the transistors and power combining are the popular ways. Observing the load line of the power amplifier, the maximum output power can be improved by series stacking multiple devices to increase the load voltage swing. The increased voltage can be shared by the multiple devices. Thus, by stacking N transistor, the output node voltage swing is N times increased than a single common source device. One more benefit is that the optimal load impedance is also N times increased than before stacking, which is a great convenient for impedance matching. However, the CMOS devices junction drain-bulk and source-bulk limitation are not alleviated by stacking more devices, thus the number of stacked devices is limited to three or four in bulk CMOS.

The architecture of a n-stacked power amplifier is shown in Figure 3.10, where n is 3. The input transistor is common-source and the stacked transistor is common gate. An inductor is used for inter-stage matching. The VDD supply can be three times of standard VDD for single transistor. The followings are the main advantages of the stacked

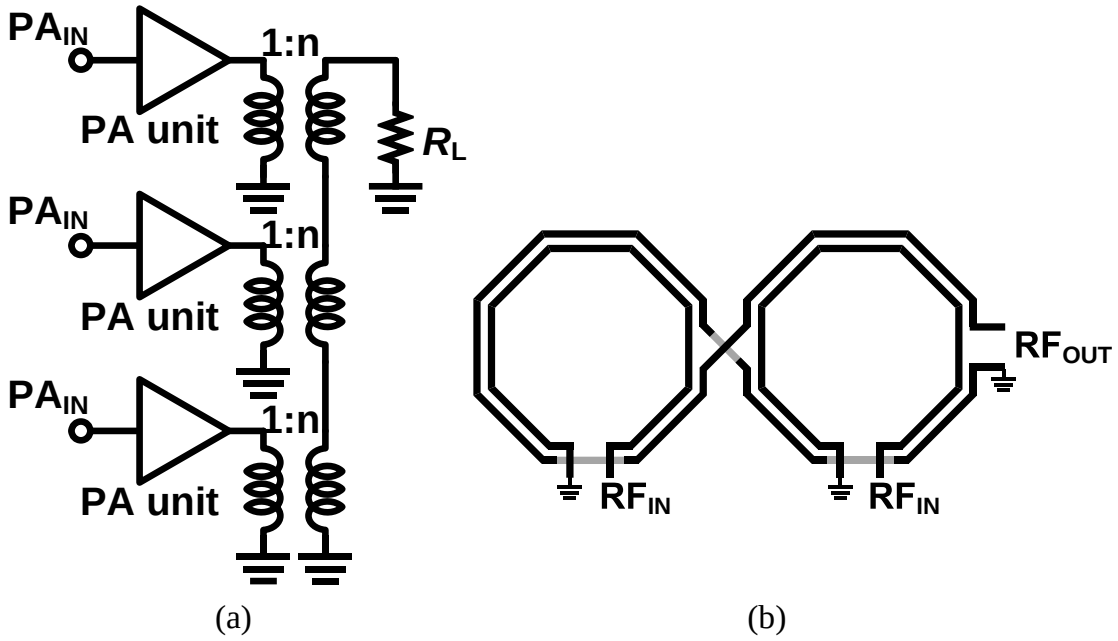


Figure 3.11: (a) m-element voltage combining power amplifier architecture. (b) 2-element voltage combining transformer with turn ratio of 1:1.

power amplifier. 1) Maximum voltage that the amplifier can handle is increased. 2) Saturated output power is increased due to increased maximum voltage. 3) The amplifier gain is increased by factor of n. 4) Optimal load impedance is increased by factor of n. 5) Drain efficiency and PAE are increased in general due to the higher gain and higher load impedance matching. The stacked power amplifier requires custom voltage supply which is n times higher than a system voltage supply, which degrades the system overall integration level and efficiency. Another main issue is that low junction drain-bulk and source-bulk limitations in bulk CMOS, which limits the total stacking number. In solicon-on-insulator (SOI) CMOS, since the body of each device can be isolated, the SOI CMOS can eliminate the junction limitations and enable stacked supply voltage over 5V. Therefore, the stacked power amplifier architecture is usually applied in SOI CMOS technology.

The power combining power amplifier directly sums the many paths' output to achieve high output power without stacking to a high voltage supply. There are mainly two types of power combining methods, one is the voltage summation, and another is the current summation. Figure 3.11 and 3.12 illustrate the mechanism of voltage combining and current combining. The transformer is compulsory for a voltage combining topology.

Instead of stacking transistors and increasing the supply voltage to improve output power, the power combining technique sums the single amplifier outputs to obtain high

output power. The voltage combining architecture is shown in Figure 3.11 (a). Assuming an infinite coupling coefficient, the output power of the voltage combiner can be n times of unit PA output power. The transformers provide power combining and impedance matching at the same time. Since it is voltage combining through transformer, the amplifier individual elements have light influence on another element, therefore the voltage combining power amplifier can adaptively turn on or off the sub elements based on output power requirements and keeps a good efficiency. The output impedance seen by individual PA unit in a m element voltage combining PA is

$$R_{\mathrm{ov}} = \frac{1}{m} \cdot \frac{1}{n^2} R_{\mathrm{load}} \tag{3.4}$$

In order to to achieve high output power, the R_{ov} is required to be low. It can be seen that the voltage combining method has the intrinsic benefit of achieving low R_{ov}. The main drawback of the voltage power combining technique is that in a practical design, the output combining transformer size become very long. The large size inductor will suffer from low quality factor and low resonance frequency, which is not preferred for large numbers of PA units at millimeter-wave frequencies. Figure 3.11 (b) shows a 2-element voltage combining transformer with turn ratio of 1:1.

The current combining architecture is shown in Figure 3.12, it combines the individual amplifiers current instead of their voltage. The output combining network employs zero-degree power combiner for the output. The current combining power amplifier ensures good reliability since it does not require large size transformer. The main drawback of the current combining technique is the output impedance matching. This method is based on summation each unit amplifier current, therefore, the output matching network should realize the impedance transformation from high impedance to the output low load impedance. The output impedance seen by individual PA unit in a m element current combining PA is

$$R_{\mathrm{oi}} = m \cdot R_{\mathrm{load}} \tag{3.5}$$

For achieving high output power, the R_{oi} is required to be low. However, it can be seen that, with a large number of current combining, the R_{oi} is intrinsically high. In order to transform R_{oi} to low impedance, additional matching network is required in each PA unit. A solution is to employ differential architecture in current combining network.

The current combining network with differential unit PA architecture employing 1:n turn ratio transformer is shown in Figure 3.13. Assuming the current combining PA consists of m PA units, and an infinite coupling coefficient. The output impedance seen

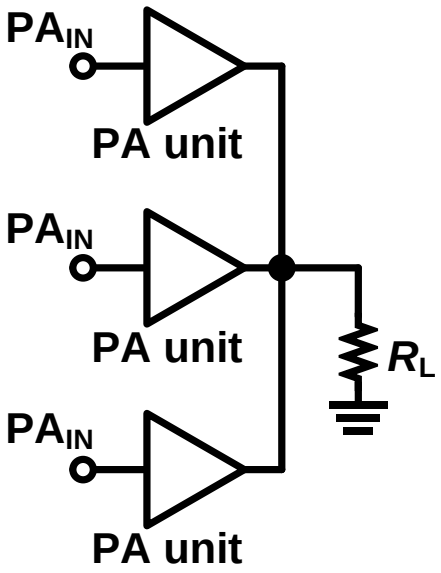


Figure 3.12: m-element single-ended current combining power amplifier.

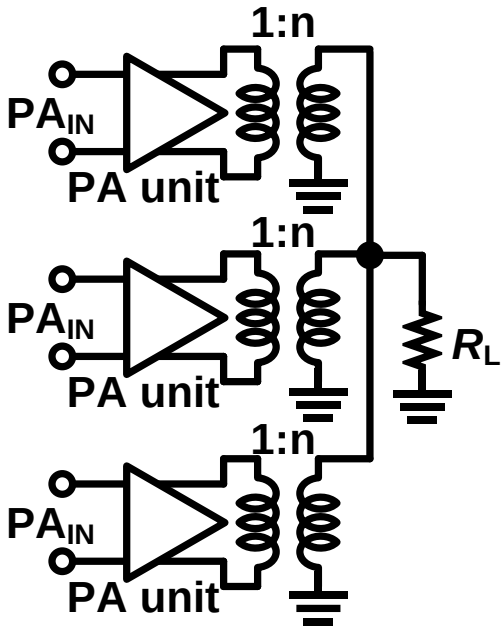


Figure 3.13: m-element differential current combining power amplifier.

by individual PA unit in a m element voltage combining PA is

$$R_{\text{oi\_diff}} = \frac{1}{2} \cdot m \cdot \frac{1}{n^2} R_{\text{load}} \tag{3.6}$$

Compared with the single-ended current combining power amplifier, the differential current combining power amplifier can lower the output impedance $R_{\text{oi\_diff}}$ by increasing

transformer turn ratio n. Same with voltage combining method. A large turn ratio n of the transformer will lead to other problems, such as low self-resonance frequency and low passive power transferring efficiency of the transformer, especially for millimeter-wave PA design. In addition, the appropriate turn ratio of the transformer for m-parallel combining transformers may not be an integer number, which is also a design issue for practical implementation.

3.2.2 Power Amplifier Architecture decision

Various types of power amplifier are introduces in section above. In a typical phased array transmitter for 5G NR in bulk CMOS technology, the power amplifier design has the following considerations: 1) High area efficiency for larger array scales. 2) Unified VDD supply for high system integration level. 3) High linearity for wideband and high-PAPR modulation signal transmission. 4) Providing sufficient gain of more than 15dB. 5) Peak PAE of higher than 30% for less power consumption while producing high output power. Figure 3.14 shows the output power of the reported state-of-the-art mm-wave PAs in CMOS, CMOS SOI, and SiGe at 30GHz to 60GHz. It can be seen that stacking devices are preferred in CMOS SOI technology for high junction limitation voltage. There is a lim-

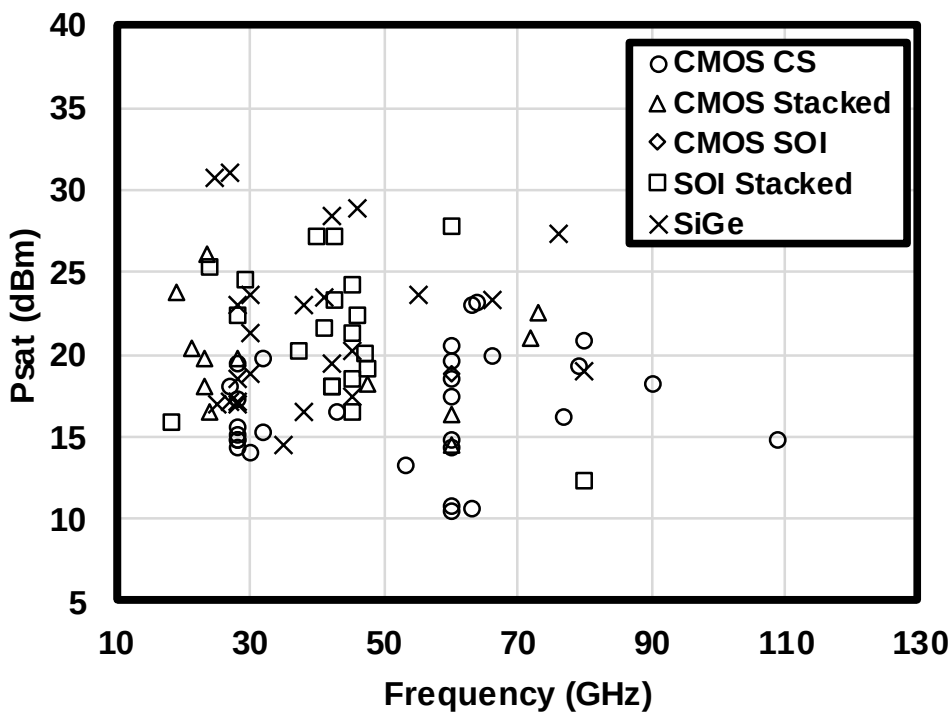


Figure 3.14: Output power of the reported state-of-the-art mm-wave PAs in CMOS, CMOS SOI, and SiGe at 30GHz to 60GHz.

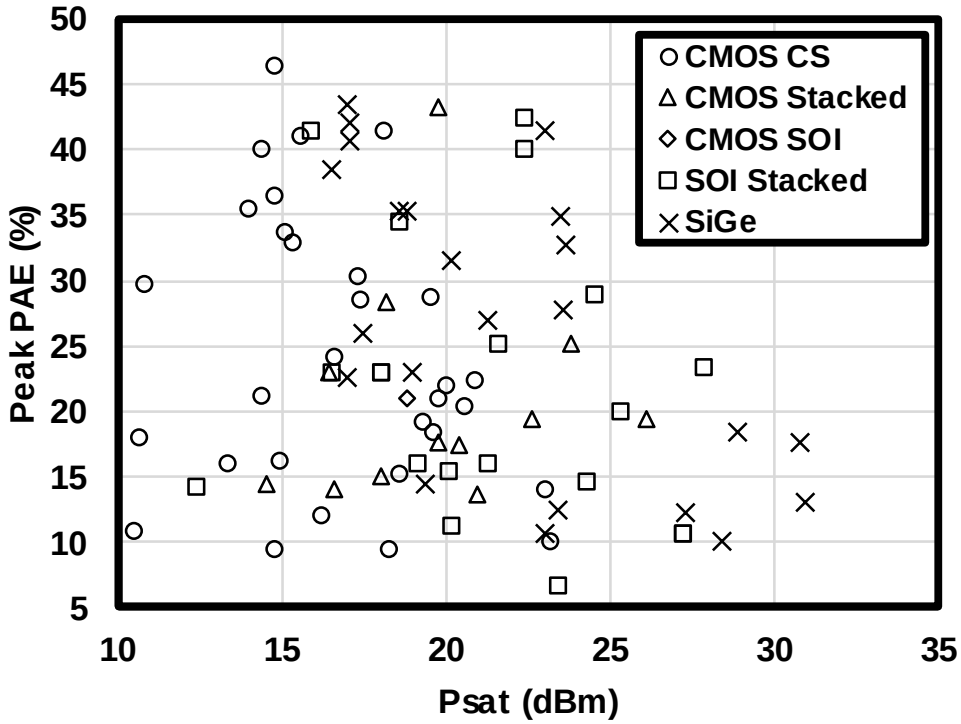


Figure 3.15: Peak PAE against Psat of the reported state-of-the-art mm-wave PAs in CMOS, CMOS SOI, and SiGe.

ited improvement by stacking bulk CMOS devices due to stacking device number cannot exceed three. The average saturate output power in bulk CMOS is around 16 dBm at 28 GHz.

Figure 3.14 shows the Peak PAE against Psat of the reported state-of-the-art mm-wave PAs in CMOS, CMOS SOI, and SiGe technology. It can be seen that the stacked architecture has higher efficiency. The stacked architecture efficiency is increased in general because the impedance transformation between overall R_o and 50 Ω is less challenging. Due to the high system integration level requirement for 5G transceiver, the system voltage supply constrains PA design to common source architecture. As shown in the Figure, the common source PA in bulk CMOS technology has an average PAE_{peak} of 30%. The PAE_{peak} can be achieved higher by reducing output power to maintain a low-loss matching network. The combining network can increase output power by summing more unit PA paths, on the other hand, the power combining network has an insertion loss and impedance transforming characteristic. The insertion loss will directly lower the output power which means the degraded PAE.

The PAs introduced in the following sections are designed in 65nm bulk CMOS technology, and the common source transistor structure is employed for 1V voltage supply. In order to achieve highest linearity and output power under low-voltage supply, the tran-

sistor size is as large as possible with differential architecture, which is used to combine two transistors' output power through a transformer. Due to limited area and high signal distribution path loss, four-path power combining PA is implemented to achieve 20dBm output. Further increasing output power will make the input an output signal distribution path more complex and lower the benefits of power combining.

3.3 Power Amplifier Design for 5G NR 28 GHz Band

The fifth generation (5G) wireless communication will be deployed by 2020 since the rapid expansion on internet of everything (IoE). Employing millimeter-wave including 28-GHz band and 39 GHz band is one of the key features of 5G NR that provides a wireless performance of multi-gigabits per second. Owing to the recent advancement in CMOS RF technology, RF front-end implemented in CMOS improves system integration level, millimeter-wave System-on-Chip (SoC) phased-array radio transceivers have been demonstrated for high integration level, high equivalent isotropically radiated power (EIRP) and low cost [35, 36].

In general, as discussed above, the linearity performance of a wireless transmitter is mainly dominated by the power amplifier (PA) as illustrate in chapter 2, since the PA will be driven into high power and non-linear region. In a CMOS transceiver SoC, the PA is limited by low breakdown voltage and low power supply, which leads to a limitation on overall system signal-to-noise-distortion-ratio (SNDR). The PA design is required to push the output power and linearity to the performance limitation with good area efficiency. Thanks to the phased-array beamforming characteristic, the sub-array PA is not required to combine large number path output, and the area can be saved for more array elements.

Frequency band for 5G NR are being separated into two different frequency ranges. First there is Frequency Range 1 (FR1) that include sub-6GHz frequency bands. The other is Frequency Range 2 (FR2) that include frequency bands in the millimeter-wave range. This section focus on the design of power amplifier for 5G NR transmitter at 28 GHz band. It presents two power amplifier realization with different topologies: 1) single-path differential power amplifier, 2) two-path power combining power amplifier. For each PA, the simulation and experimental results are shown.

3.3.1 28 GHz Single Path Differential Power Amplifier

As discussed in Section 3.2.2, the architecture is chosen common source with differential transistor topology. Figure 3.16(a) shows the circuit schematic of the single-path 28-GHz

differential power amplifier. The PA has a differential input since the differential transmitter architecture provides intrinsic 3dB higher power than that of a single-ended one. The power amplifier consists of two stages: drive stage and power stage. The transistor sizes are 132um/0.065um and 308um/0.065um for drive stage (DA) and power stage (PA), respectively. The input matching network uses the series transmission line and shunt capacitor for transforming the source 50Ω impedance to drive amplifier input conjugate impedance. A series capacitor is placed for DC-cut and transistor bias. A shunt inductor and a series transmission line are used for the inter-stage matching; the shunt inductor is also connected to VDD supply from its center tap due to the differential operation. The power stage differential signal is converted to single-ended using an on-chip balun. The balun is carefully designed for low-loss impedance matching.

The power cell detailed architecture is shown in Figure 3.16(b). The gate-drain capacitance miller effect of a common-source stage at millimeter-wave frequency will cause gain degradation. The differential architecture can neutralize the capacitance by cross connecting the one output to another input through a capacitor, which is equivalent to the

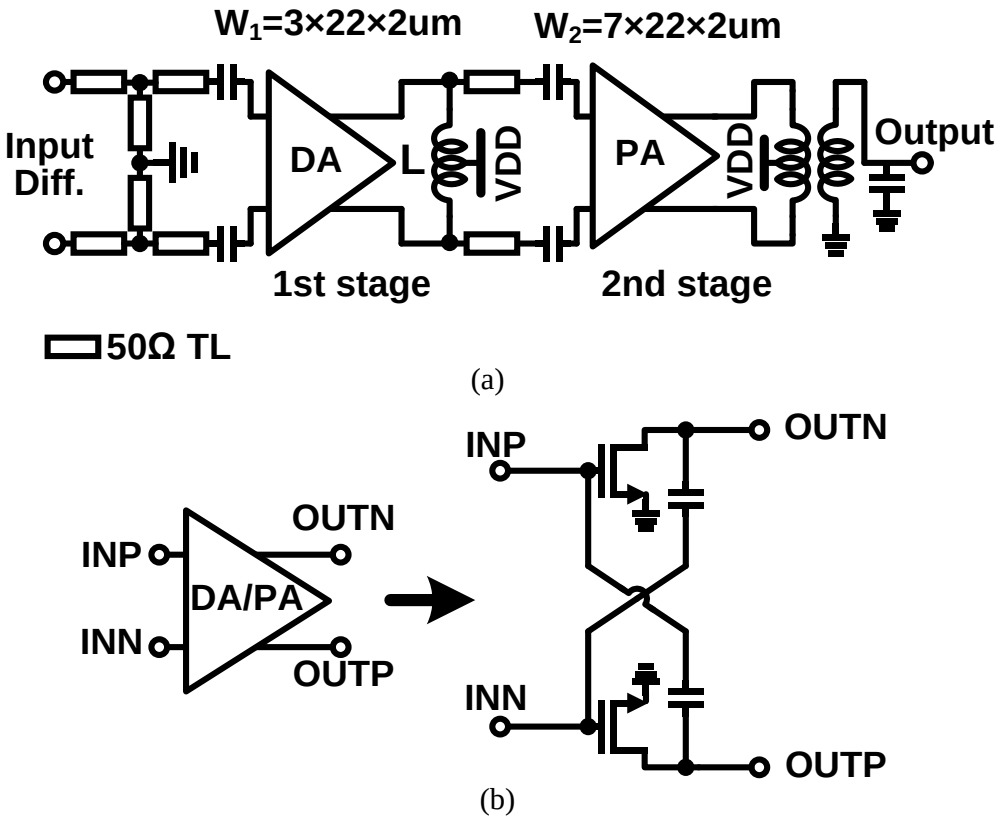


Figure 3.16: 28-GHz single-path differential power amplifier architecture.

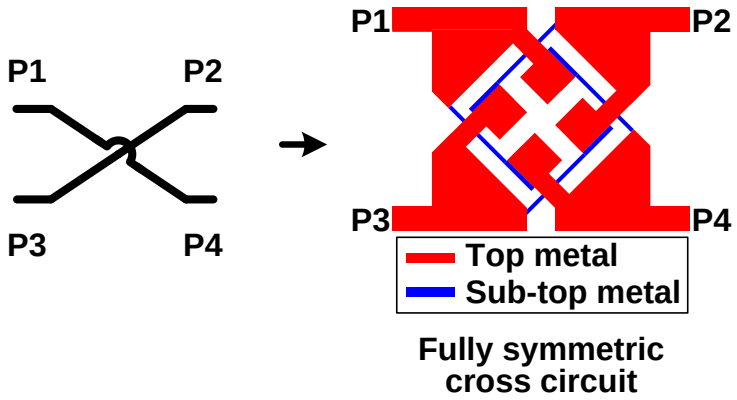


Figure 3.17: Fully symmetric cross circuit.

gate-drain capacitance. Since the differential phase mismatch may cause gain and power degradation, the differential circuit is designed and do layout fully symmetrically [37]. Figure 3.17 shows the fully symmetric cross circuit used in capacitive neutralization circuit. It consists of two layers and four ports, each port can cross to the opposite port through the same physical path. Detailed modeling and analysis can be found in [38, 39].

The power amplifier optimal impedance matching is the first step to estimate the transistor capability and efficiency. Figure 3.18 shows the simulation setup of load pull for optimal impedance extraction. Since the differential architecture power is used in this design, the setup uses two ideal baluns to convert the single-ended test signal to differential. Biased in class AB mode, by tuning the tuner impedance, the output power keeps changing and the optimal impedance can be extracted. Usually there will be two types of optimal impedance: impedance for highest saturated output power (Psat), and impedance for highest power added efficiency (PAE). Most of the transistor optimal impedance for Psat and peak PAE are not the same, thus there is a trade-off between the power matching and PAE matching. In this dissertation, our design prefers the impedance matching for high Psat which leads to higher linearity.

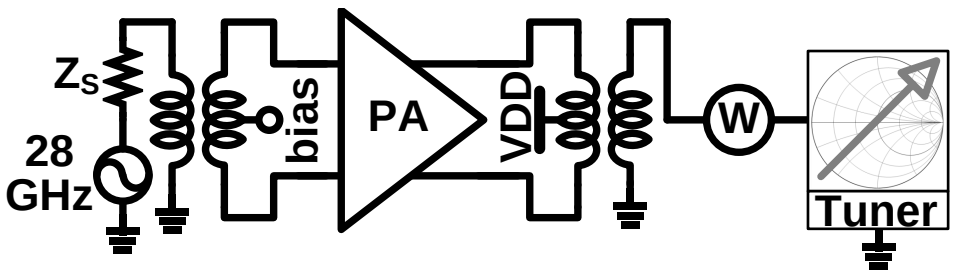


Figure 3.18: Power stage load pull.

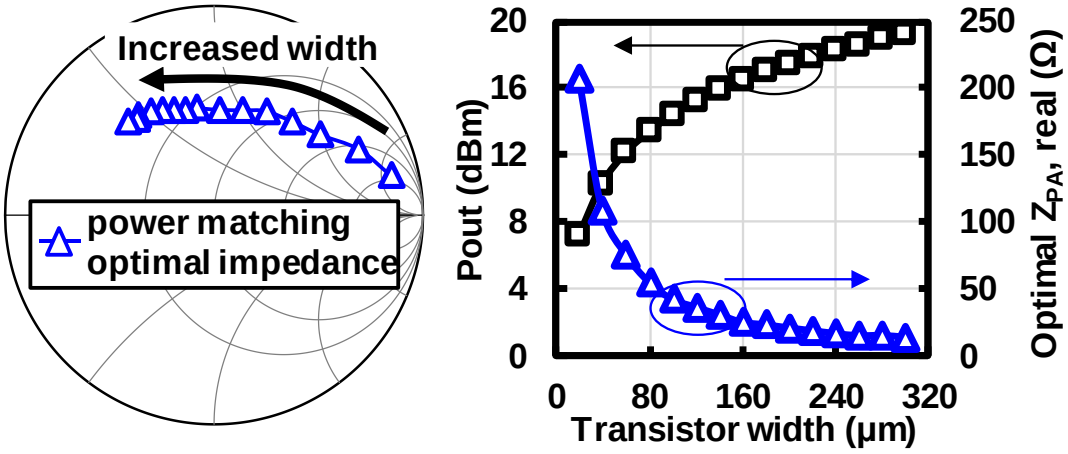


Figure 3.19: Simulated Pout and optimal impedance with respect to transistor width.

The power stage differential transistor pair output power and corresponding optimal impedance with respect to transistor width is simulated as shown in Figure 3.19. It can be found that the required impedance for PA optimal matching is decreasing with the transistor size increasing. The optimal transistor size is 80um for a 50 Ω load impedance, and the corresponding output power is around 13 dBm. Further increase the transistor size, the output power will improve to near 20 dBm, in this case, the optimal impedance is around 10 Ω. In this design, the power stage transistor size is 308um, which can deliver maximum 19dBm output power with ideal transformer.

The transformer design is the second step. After extracting the optimal impedance, the output transformer should be designed to convert the differential signal to single-ended and provide the optimal impedance for the transistor output with a low insertion loss. The transformer is designed in the electromagnetic (EM) simulator with 3D modeling and finite element method (FEM) solver. The transformer 3D model views are shown in Figure 3.20. The transformer is single turn with vertical structure for high coupling coefficient and friendly layout. The simulated insertion loss is 0.8 dB at 28 GHz. The transformer simulated efficiency and quality factor is shown in Figure 3.21.

The implemented 28 GHz differential power amplifier is shown in Figure 3.22, the amplifier occupies a core area of 0.17 mm^2. This section discusses the measured small signal performance and large signal performance. The PA performance is characterized in 50 Ω on-wafer measurement setup under 1-V supply voltage with fixed class AB bias. The PA small signal measurement uses Keysight PNA-X. Figure 3.23 shows the measured S-parameter results. The PA has a peak gain of 15.0 dB, and 3-dB bandwidth from 25.1 GHz to 28.9 GHz. The PA large signal measurement uses Keysight signal generator and power meter. The measured results are shown in Figure 3.24. The amplifier achieves

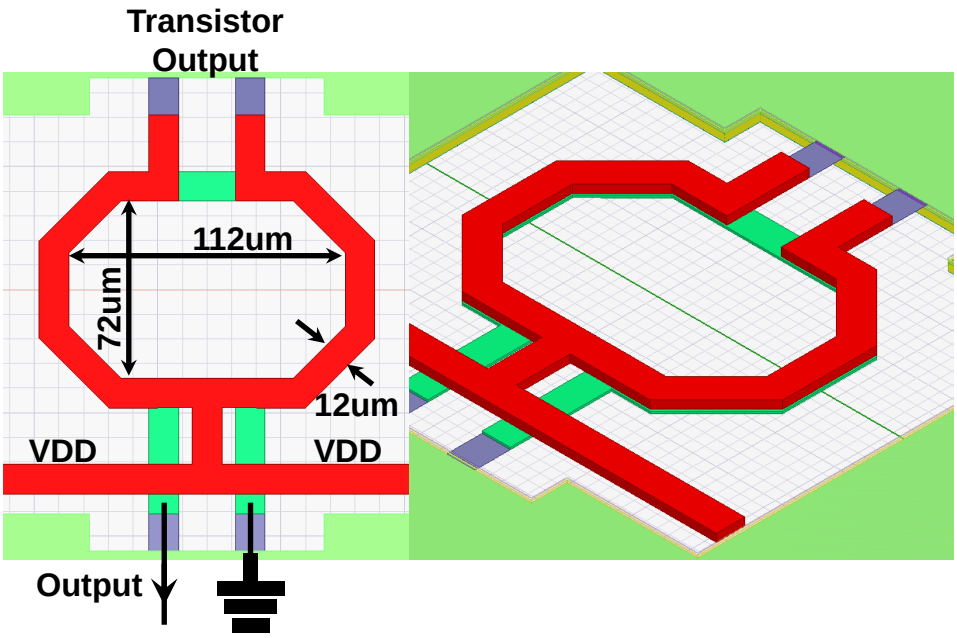


Figure 3.20: Output transformer 3D model.

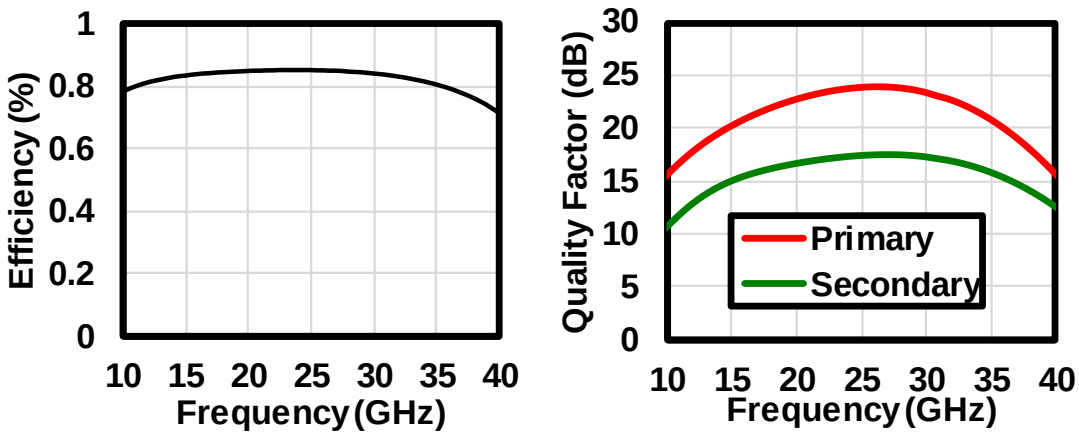


Figure 3.21: Transformer simulated efficiency and quality factor.

17.6 dBm saturated output power and 16.2 dBm 1-dB compression point at 28 GHz. The peak power added efficiency is 30.3 % and PAE at P1dB is 23.2%. This PA exhibits high performance linearity and power delivery, the peak PAE is achieved 30 %. The PA is integrated in the phased-array transceiver, and the modulation performance is evaluated with the transceiver introduced in chapter 4 section 4.2.1.

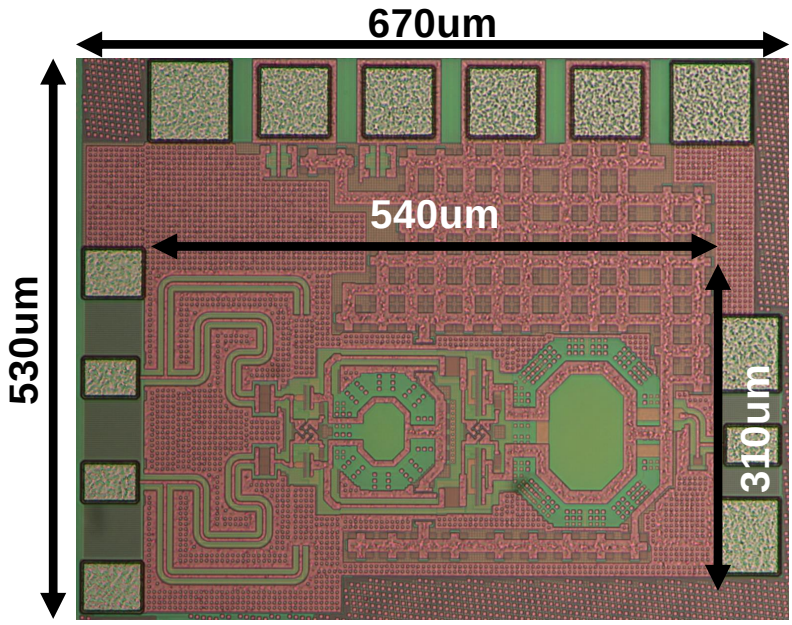


Figure 3.22: Chip micrograph of 28 GHz differential power amplifier.

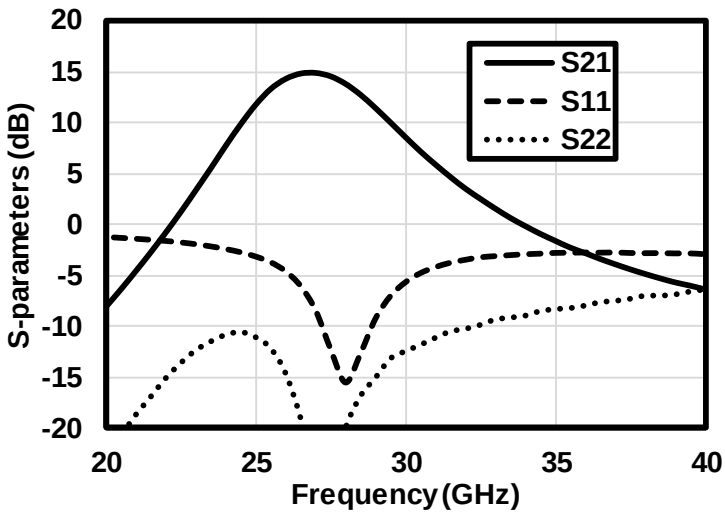


Figure 3.23: S-parameter measurement of 28 GHz differential PA.

3.3.2 28 GHz Power-Combining Power Amplifier

As introduced in Section 3.2, in order to further increase the output power and linearity, a 28 GHz power amplifier with current combining is introduced in this section. As shown in Figure 3.25, the power combining PA consists of two identical paths with both driving stage and power stage. The driving stage and power stage in each path is reusing the PA described in section 3.3.1. The driving stage and power stage transistors have the total

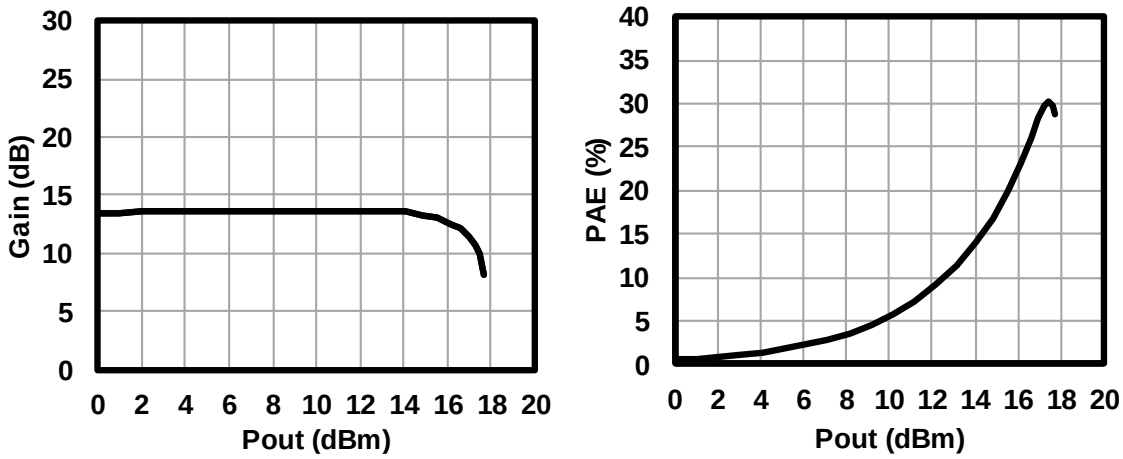


Figure 3.24: Large signal measurement of 28 GHz differential PA.

width of 132um and 308um with 50 fF and 80 fF neutralization capacitor, which is the same with 28 GHz differential power amplifier introduced in section 3.3.1. Both the PA single path layout and the power-combining network layout are fully symmetric. The transmission line input matching network is replaced by an input transformer. The upper path and the lower path are connected to the differential input positive and negative ports respectively. The outputs from each unit PA path added together through zero-degree power combiner. The zero-degree combiner uses transmission line for low-loss and high accuracy.

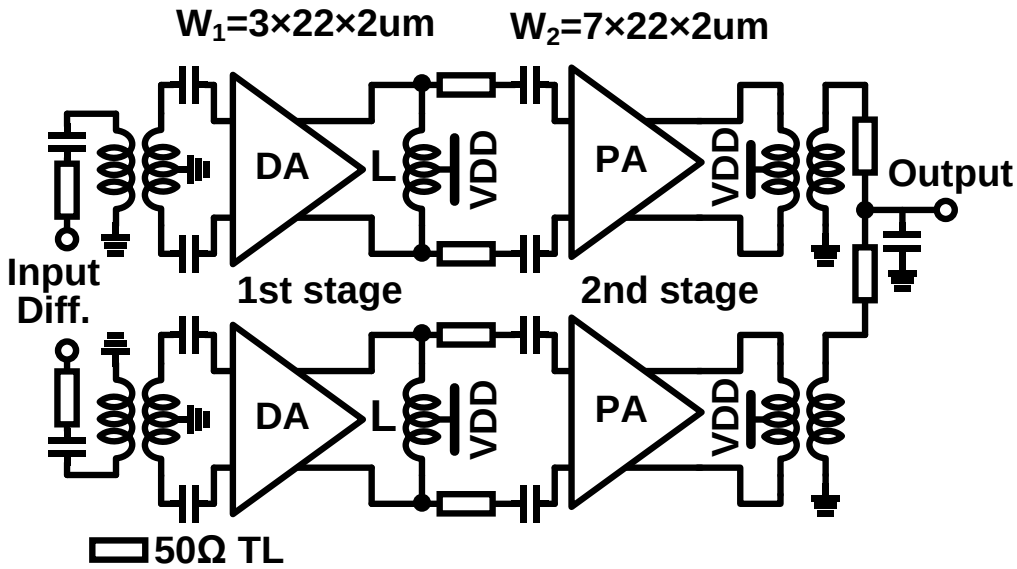


Figure 3.25: 28-GHz two-path power combining differential power amplifier architecture.

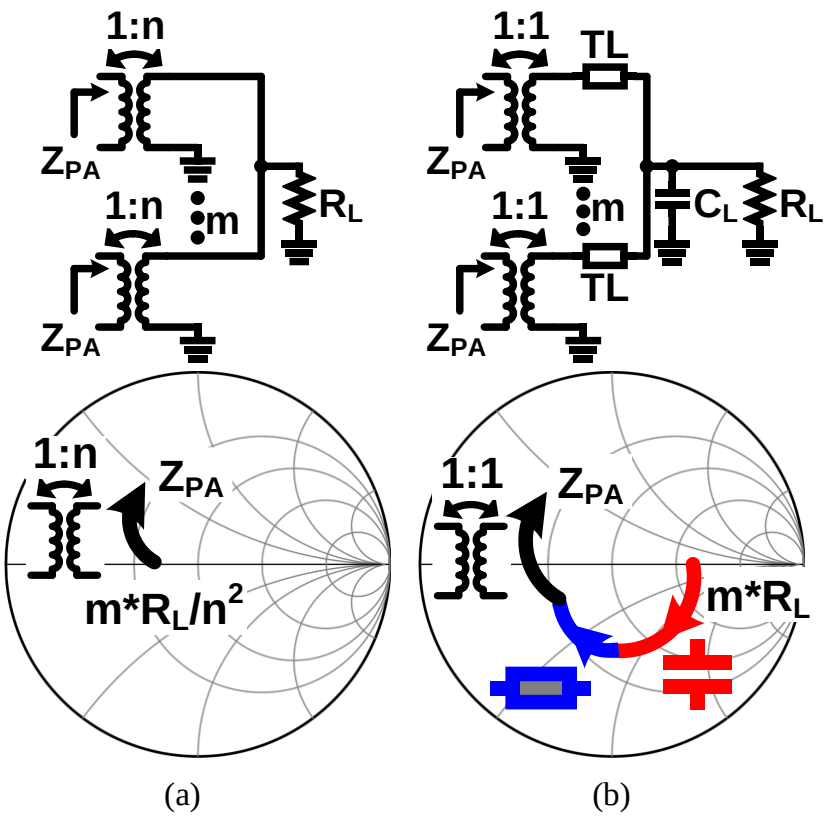


Figure 3.26: (a) current combining network with multi-turns output transformer, (b) current combining network with high-Q single-turn output transformer.

More detailed circuit design shown in Figure 3.25 is introduced below. The input transformer converts the driving stage transistor pair input impedance to inductive, and a 50 fF series capacitor is used for matching to 50 Ω source impedance. The inter stage matching uses a 100-pH shunt inductor and a series transmission line to match the impedance between optimal driving stage load impedance and power stage source impedance. The driving stage supply is fed through the inductor virtual ground center tap. The power combining network is required to sum the power as well as provide impedance matching as discussed in section 3.2.1.

The power stage output impedance matching is carefully considered, since it has high impact on PA linearity and saturation power. A current power-combining network is preferred at millimeter-wave PA design [40]. However, due to the current summation, a high loss matching is mandatory to transform the high load impedance to the PA optimal impedance. As shown in Figure 3.26 (a), the conventional way to transform the current combining network high load impedance $m * R_L$ to desired PA load impedance is by employing a transformer, where m indicated the m-way current combining. The high load

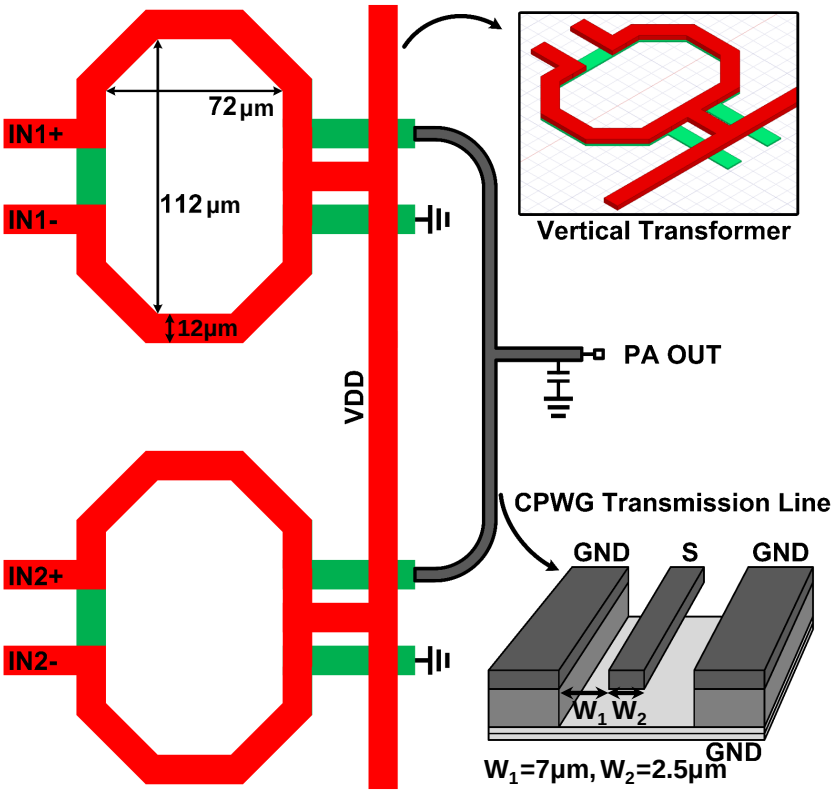


Figure 3.27: Current power combining network.

impedance can be transformed to $m * R_L/n^2$ when applying the transformer turns ratio to 1:n. However, at millimeter-wave frequencies, the transformer number of turns n increases will lead to higher insertion loss and complex modeling. For reliable EM simulation and modeling, the proposed PA output current power combiner consists of 1:1 turn ratio transformers, transmission lines and a shunt capacitor as shown in Figure 3.26 (b). The high load impedance $m * R_L$ is transformed to low impedance through a shunt capacitor and a series transmission line. In this section, a 2-way current combining network is implemented as shown in Figure 3.27. Each transformer has a simple vertical structure for high quality factor and accurate EM modeling. The transformer has an octagon structure with horizontal size of 72 um, vertical size of 112 um, and 12 um metal width. The power stage supply is fed through transformer top metal center tap. The simulated transformer efficiency is 83.1 %. The 50 Ω transmission line is based on coplanar waveguide with lower ground plane (CPWG) structure introduced in chapter 2, and the measurement-based model up to 110 GHz is introduced in [41].

Simulation shows the entire output power-combining network has a loss of 1.0 dB. Power matching is used in this PA design instead of conjugate matching for high linearity.

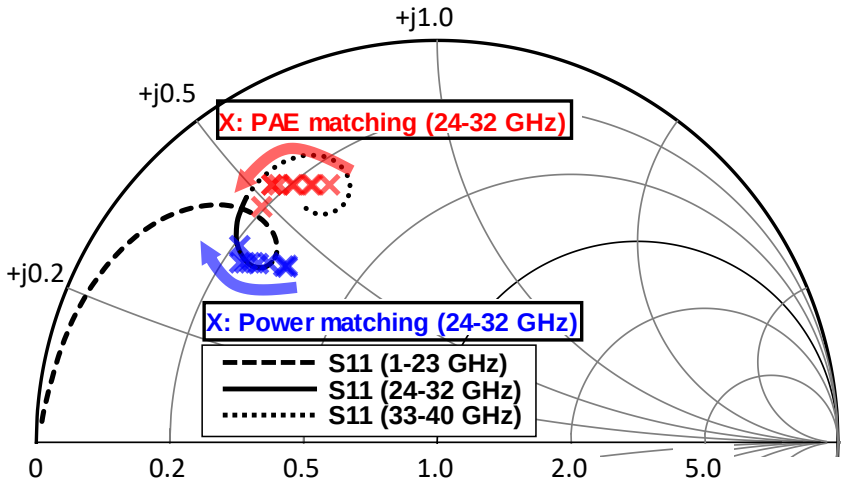


Figure 3.28: Simulated load impedance seen at power-combining network in Smith Chart, and load-pull extracted optimal impedance for power matching and efficiency matching.

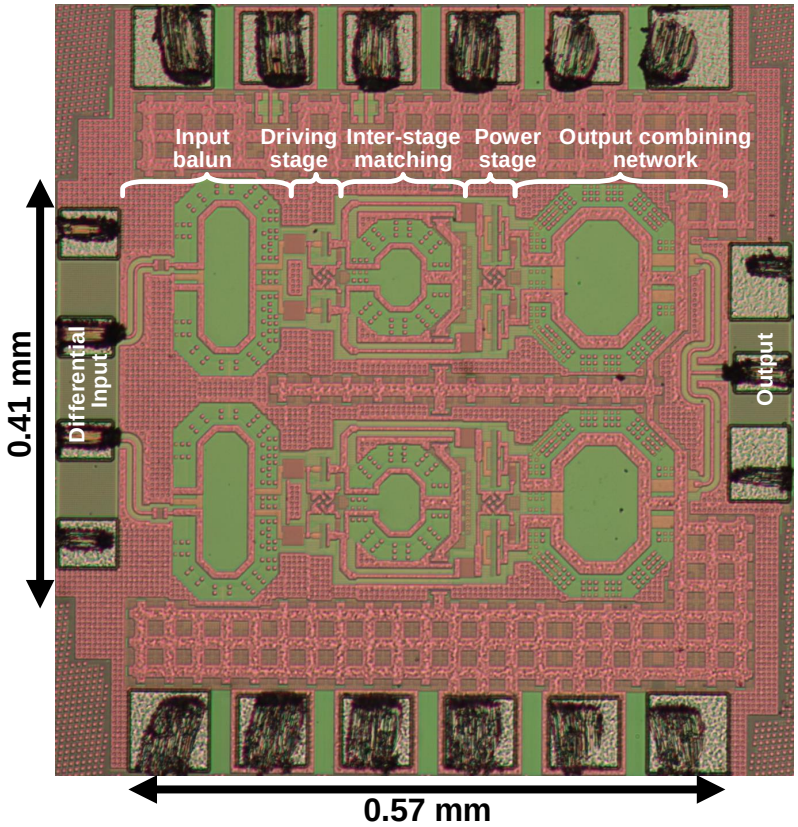


Figure 3.29: Chip micrograph.

Figure 3.28 shows the PA power stage differential pair simulated load-pull optimal load impedances for power delivery and efficiency. The simulated load impedances presented at power-combining network is also shown in Figure 3.28. It can be seen that the PA has an optimal power matching impedance at 28 GHz.

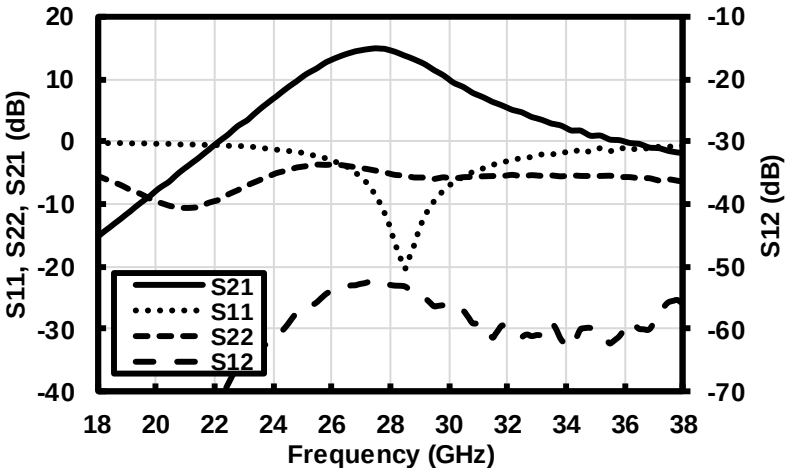


Figure 3.30: Measured small signal performance.

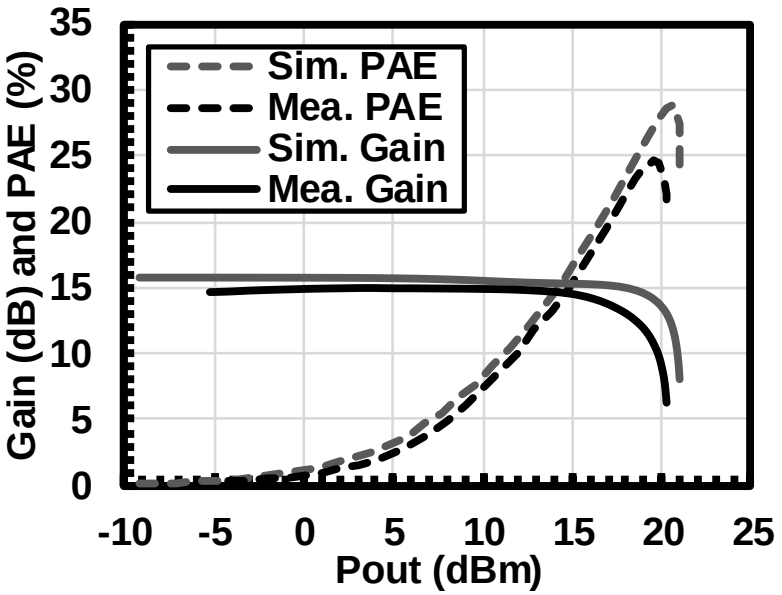
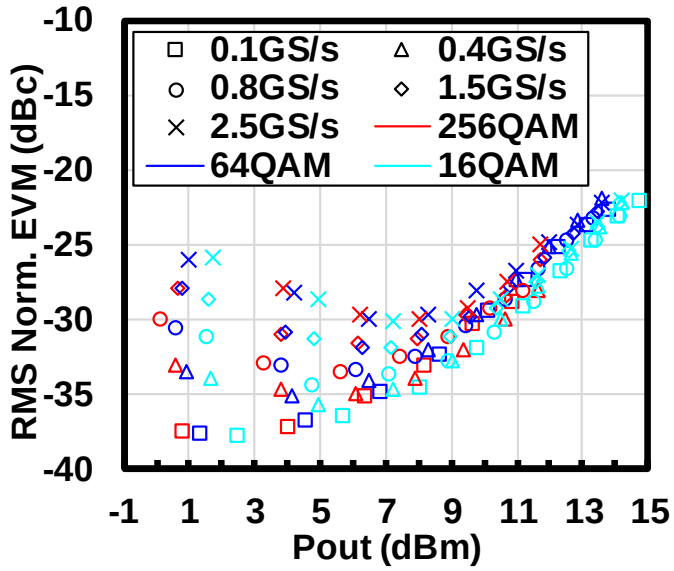
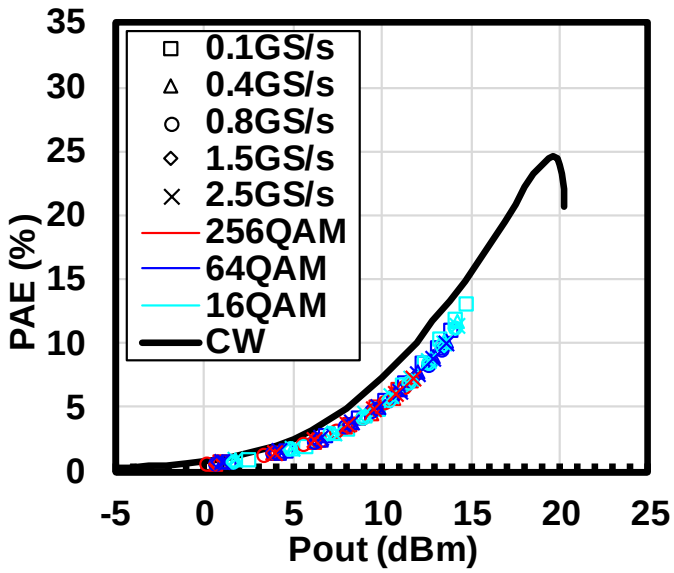


Figure 3.31: Measured large signal performance.

Figure 3.29 shows the PA chip micrograph with a core area of 0.23 mm^2. The PA is fabricated in standard 65-nm CMOS technology. The PA performance is characterized in 50-Ω on-wafer measurement setup under 1.1-V supply voltage with fixed class AB bias. The PA small signal measurement uses Keysight PNA-X E8361A. Fig. 6 shows the measured S-parameter results. The PA has a peak gain of 15.0 dB, and 3-dB bandwidth from 25.6 GHz to 29.3 GHz. The PA large signal measurement uses Keysight signal generator E8257D and power meter E4417A. The measured results are shown in Figure 3.31. The amplifier achieves 20.2 dBm saturated output power (P_{sat}) and 17.0 dBm 1-dB compression point (P_{1dB}) at 28 GHz. The peak power added efficiency (PAE) is 24.5% and PAE at P1dB is 20.7%. The measured linearity is 2-dB degraded from simulation.



(a)



(b)

Figure 3.32: Measured (a) EVM performance and (b) average PAE.

The PA performance with modulation signal is measured using a Keysight AWG M8195A, oscilloscope DSO91304A and external mixer. The single carrier modulation signal is applied to PA. After calibrating LO power, the PA output average power versus the PAE and average RMS power normalized EVM performance is shown in Figure 3.32. For 2500MHz 64QAM modulation, the PA has an average output power of 11.4 dBm with 6.8% PAE at -26dBc RMS power normalized EVM, and an average output power of 13.6 dBm with 10.0% PAE at -26dBc peak power normalized EVM.

A current type 2-way power-combining 28-GHz PA using vertical transformer and transmission line for impedance matching is discussed in this section. Experimental result shows the PA achieves 20.2 dBm P_{sat} and 11.4 dBm average output power for transmitting 2500MHz 64QAM modulation signal, which is suitable for 5G millimeter-wave phased array in CMOS technology.

3.4 Power Amplifier Design for 5G NR 39 GHz Band

This section presents power amplifier design for 5G NR 39 GHz band. The 39 GHz band provides 3-GHz contiguous spectrum, with sub-channel width of 100 MHz. As shown in Figure 3.33, the 5G NR n260 band combines the two frequency bands of 37-38.6 GHz and 38.6-40 GHz. The 39 GHz band frequency is 40% higher than 28 GHz band frequency, which results in a higher propagation losses and shorter communication distances. The short communication distances and high propagation losses also provides advantages of spectrum re-use in cellular deployment with limited interference between adjacent cells. For realizing longer communication distance, it is feasible to employ small size antenna phased-array to concentrate the signal strength forming a beam with enough gain to compensate the propagation losses.

Different with the 28 GHz bands, the 39 GHz band is preferred to license a portion of the band on a nonexclusive basis and to license the remainder of the band by geographic area. As shown in Figure 3.34, for example in USA, EU, Japan and China, the 28 GHz bands are all allocated to carriers exclusively. By contrast, the 39 GHz band is planed to be shared and non-exclusive, which will allow for a sufficient acquisition of spectrum by smaller users while still allowing for aggregation by larger entities.

This section introduces power amplifiers design for 5G NR 39 GHz band, the amplifiers include single-path differential PA, power-combining PA and TRX switch integrated PA.

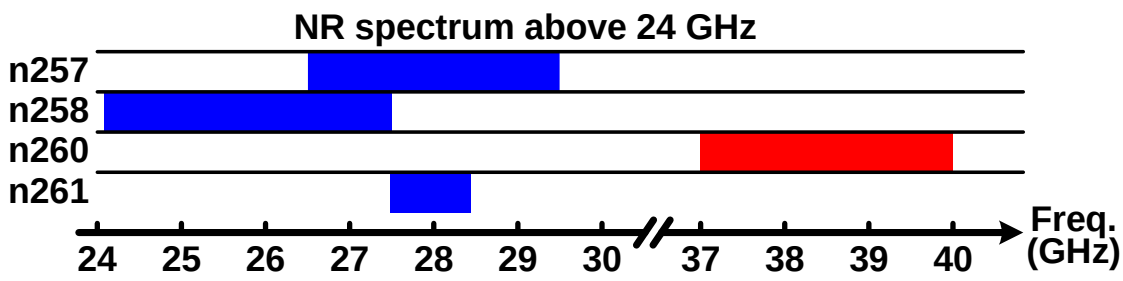


Figure 3.33: 5G NR bands spectrum plan by country or region.

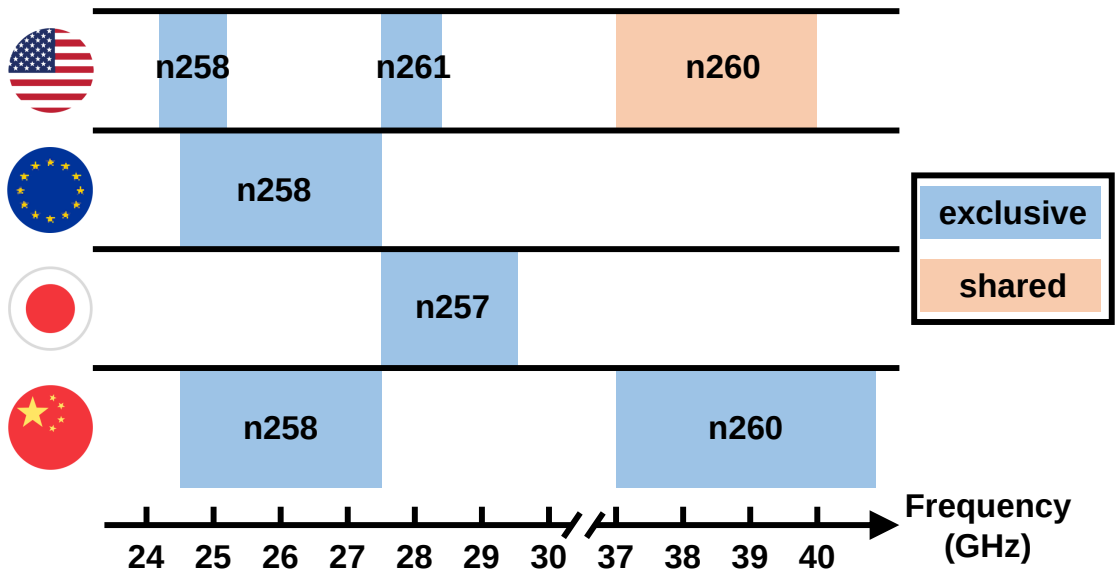
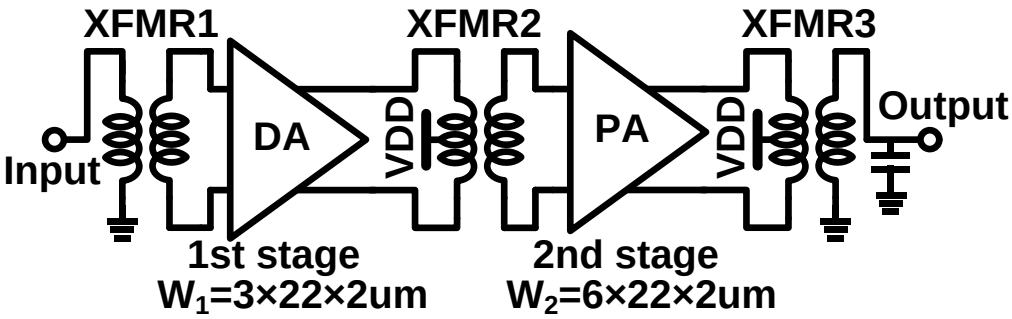


Figure 3.34: 5G NR bands above 24 GHz.

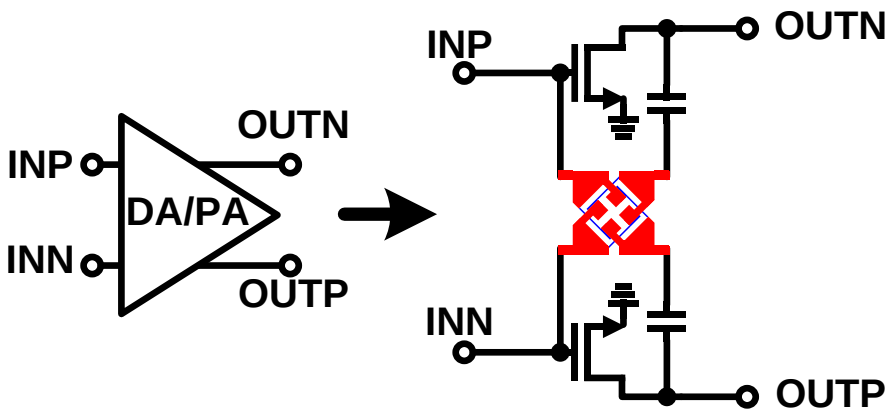
3.4.1 39 GHz Single Path Differential Power Amplifier

The differential architecture is also used in 39 GHz power amplifier design. Similar with power amplifier at 28 GHz, the 39 GHz power amplifier employs a transformer to combine the differential signal to single-ended. The detailed architecture is shown in Figure 3.35 (a), the PA input is single-ended including a transformer (XFMR1) converting the put to differential with 50Ω input impedance. The power amplifier consists of two stages: drive stage and power stage. The transistor sizes are 132um/0.065um and 264um/0.065um for drive stage and power stage, respectively. Figure 3.35 (b) shows the differential pair transistor topology. The differential architecture can neutralize the capacitance and improve gain by cross connecting the one output to another input through a capacitor, which is equivalent to the gate-drain capacitance.

The inter-stage matching network between drive stage and power stage uses a transformer to replace the transmission line matching network introduced in section 3.3.1. The transformer XFMR2 separates the drive stage VDD and power stage bias without using DC-cut capacitor. The benefits of employing transformer in the inter-stage matching are below. At first, the transformer has much wider metal width, therefore, the quality factor and insertion loss of the matching network is better than the transmission line. Second, the inductor L used in Figure 3.16 is already with the smallest radius that a foundry can provide. For 39 GHz matching network, the inductor should scaled 40% smaller than in 28 GHz matching network. The inductor size will be extreme small and infeasible to be implemented by the foundry. Therefore, the transformer is employed due to the cus-



(a)



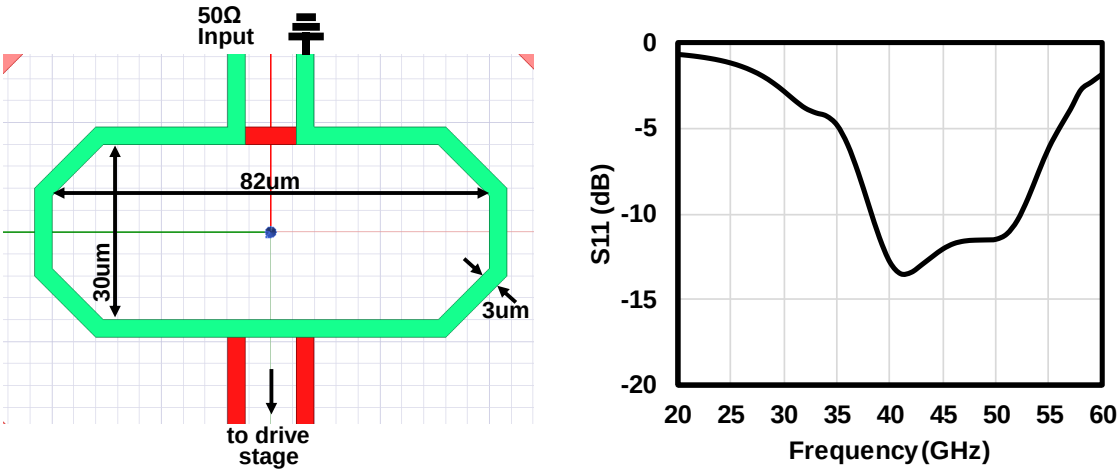
(b)

Figure 3.35: 39-GHz single-path differential power amplifier architecture.

tomized shape and wide metal width.

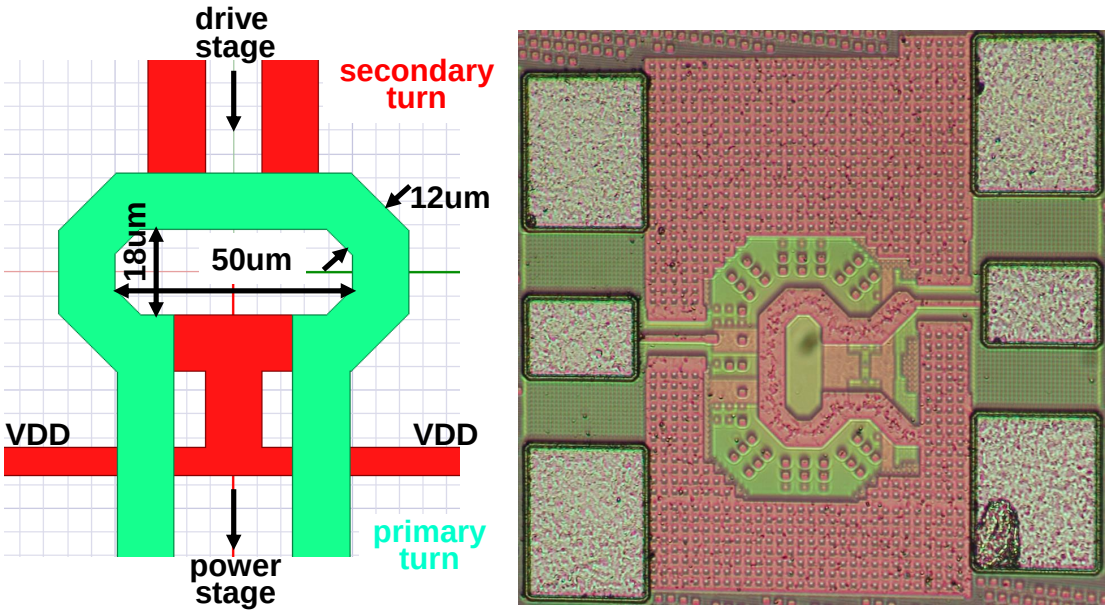
Compared with the 28 GHz power amplifier, another difference is the power stage transistor size. The larger transistor size leads to higher power delivery ability. However, because of that the parasitic components will not scale down with the size of a multi-finger CMOS device, the larger transistor size will lead to low maximum available gain at higher frequency. In addition, the large parasitic capacitance will make the matching network difficult to achieve high quality factor at the desired frequency. Therefore, for maintaining adequate power gain and low-loss matching network, the power stage transistor is decided 264um/0.065um. The drive stage transistor size is not critical for the frequency characteristic due to the relatively smaller size.

The transformers for input, inter-satge, and output are designed and simulated using electromagnetic (EM) simulator. For testing and evaluating the accuracy of transformer, the standalone test element groups (TEG) for the transformers are implemented. Figure 3.36 (a) shows the power amplifier input transformer (XFMR1) top view. By adjusting the transformer size, the power amplifier has a input impedance of 50 Ω without employing additional LC components. Figure 3.36 (a) shows the simulated power amplifier input matching reflection coefficient.



(a) (b)

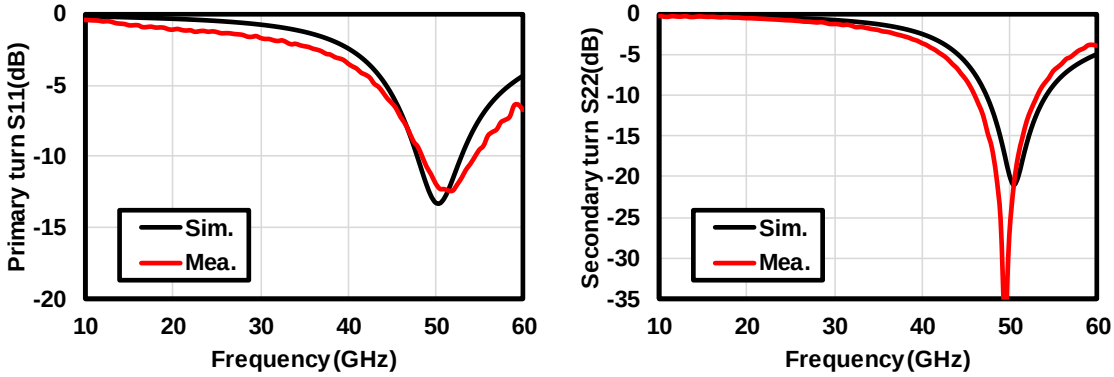
Figure 3.36: (a) Power amplifier input transformer (XFMR1), (b) Simulated power amplifier input matching reflection coefficient.



(a) (b)

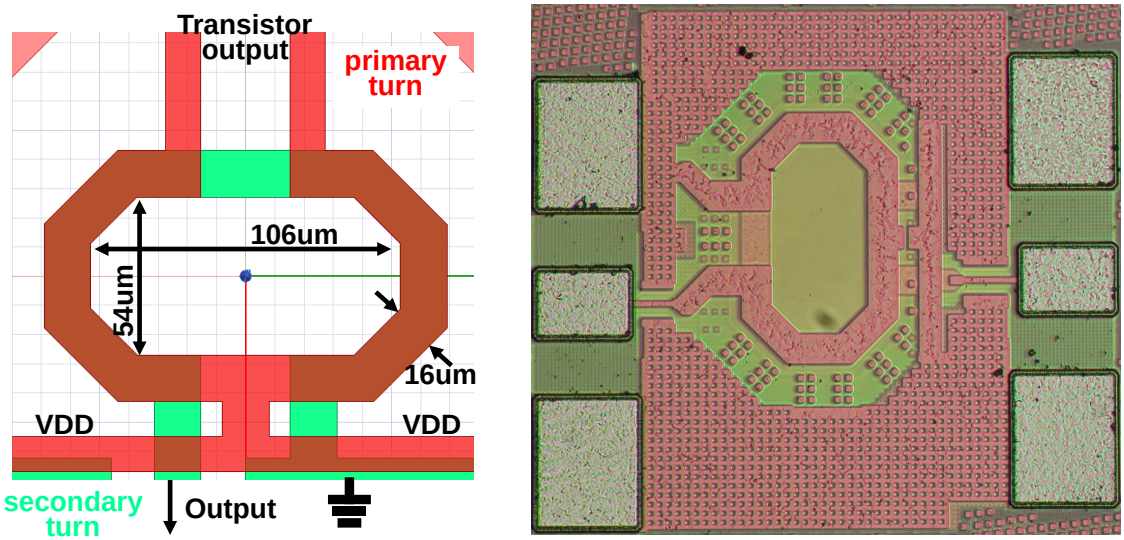
Figure 3.37: (a) Power amplifier inter stage transformer (XFMR2) top view, (b) standalone TEG for XFMR2 characterization.

The inter-stage transformer (XFMR2) is designed to match the impedance between the drive stage output and the power stage input. Since the power amplifier linearity performance is mainly dominated by the power stage, the matching network in the inter stage provides conjugate impedance matching for high gain. Figure 3.37 (a) shows the



(a) (b)

Figure 3.38: Inter-stage transformer XFMR2 simulated and measured reflection coefficient (a) primary turn, (b) secondary turn.



(a) (b)

Figure 3.39: Output transformer XFMR3 (a) top view, (b) standalone TEG for XFMR3 characterization.

inter stage transformer (XFMR2) 3D view. The transformer shape and size are highly customized to save the area. It can be found that the inter stage transformer is very compact with its radius of 9um, which is infeasible beyond the lower limit that the foundry PDK can provide. The customized transformer is simulated and measured to verify its characteristic. Figure 3.37 (b) shows the inter stage transformer standalone TEG microphotograph. Figure 3.38 shows the inter-stage transformer simulated reflection coefficient in comparison with measurement results. It shows simulation has good match with the measured results.

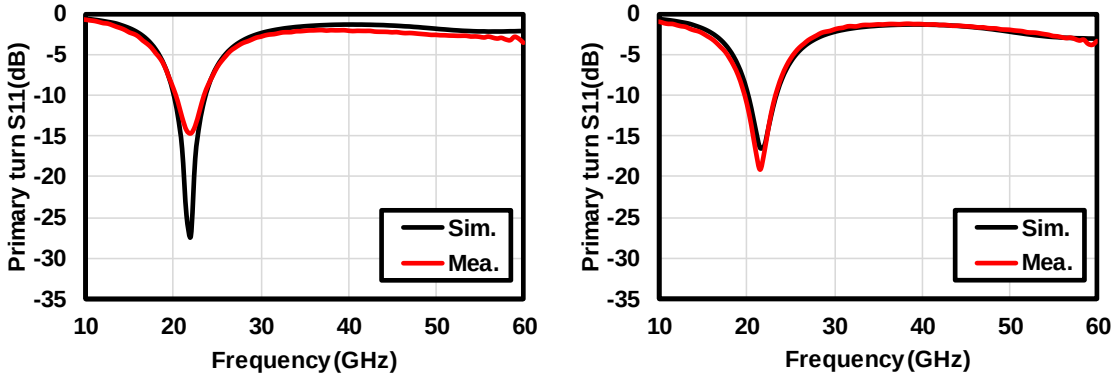


Figure 3.40: Output transformer XFMR3 simulated and measured reflection coefficient (a) primary turn, (b) secondary turn.

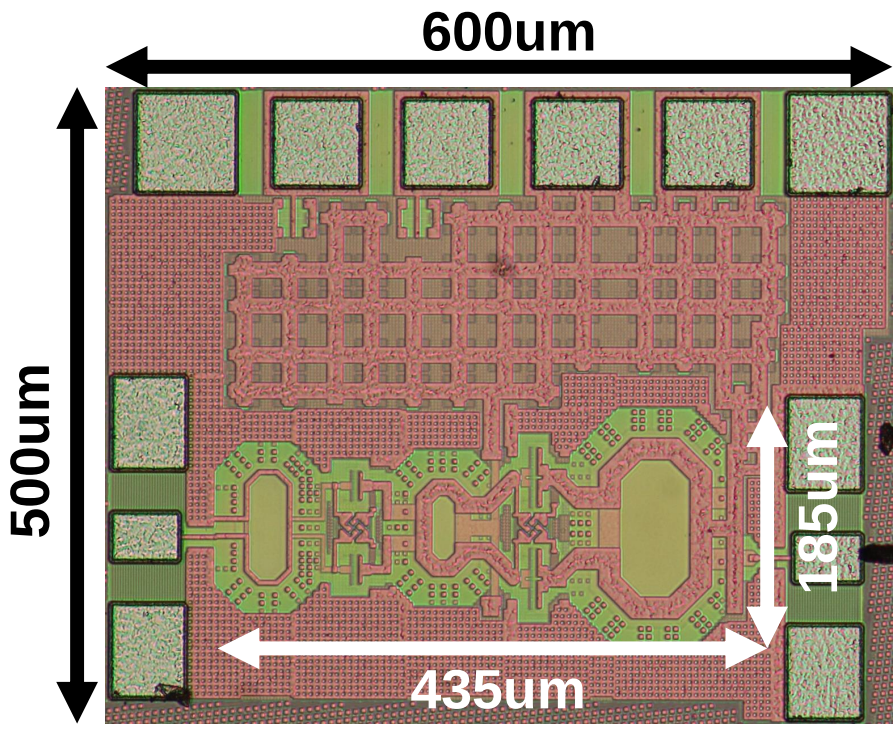


Figure 3.41: 39 GHz single path differential power amplifier chip micrograph.

The output transformer (XFMR3) is also characterized by using a standalone TEG. Figure 3.40 shows the output transformer simulated reflection coefficient in comparison with measurement results. It can be observed that the transformer modeling is highly matched with the measurement result, which ensures the design accuracy.

The implemented 39 GHz single path differential power amplifier is shown in Figure 3.41, the amplifier occupies a core area of 0.081 mm^2. The measurement firstly evaluates

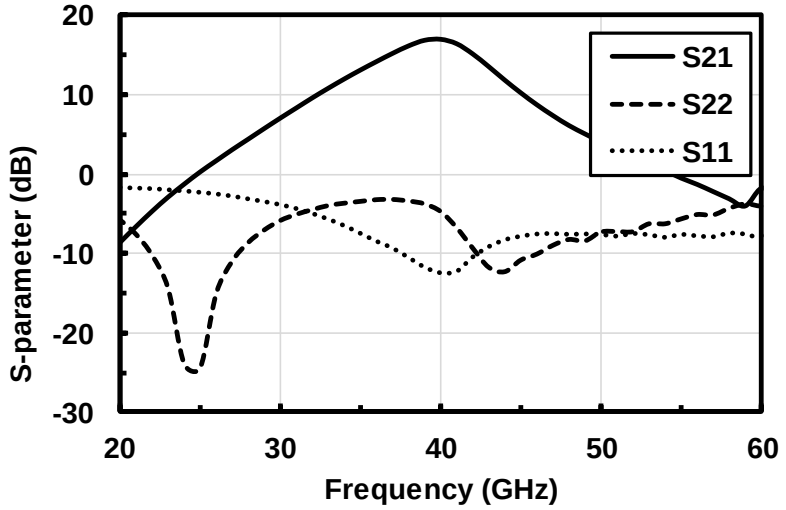
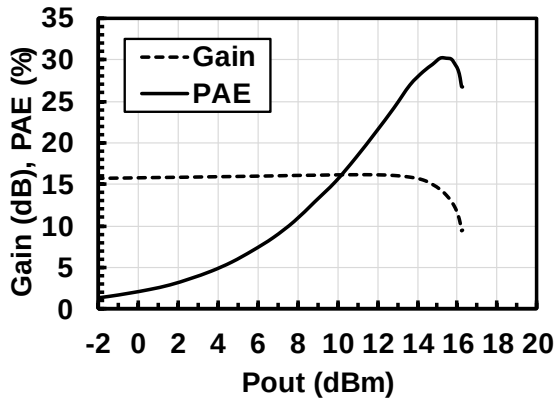
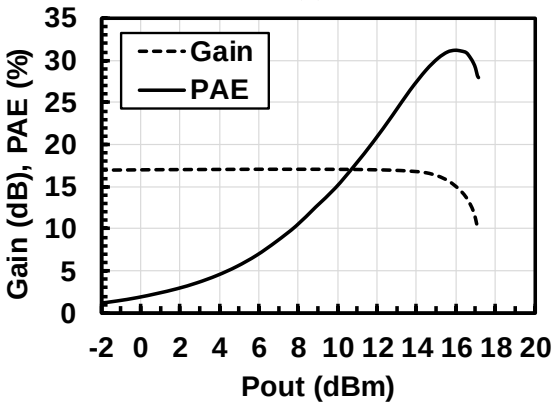


Figure 3.42: Measured s-parameters of 39 GHz single path differential power amplifier.



(a)



(b)

Figure 3.43: Measured 39 GHz single path differential PA linearity and PAE under (a) 1-V supply and (b) 1.1-V supply.

the PA small signal performance and large signal performance. The PA performance is characterized in 50 Ω on-wafer measurement setup under 1-V and 1.1-V supply voltage

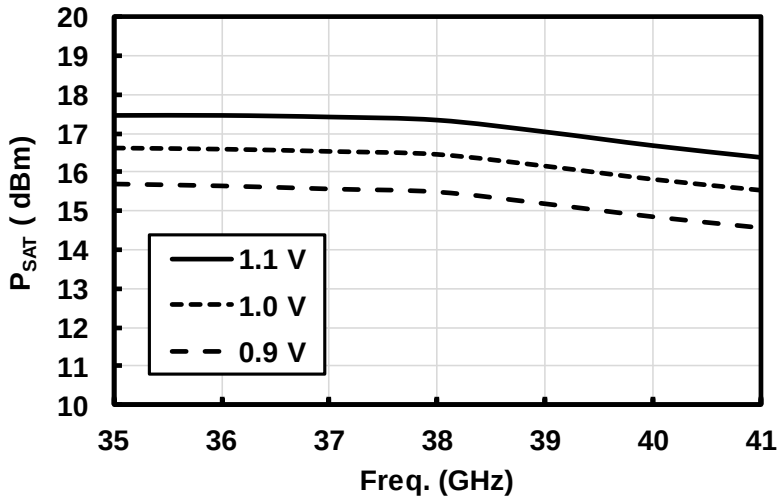
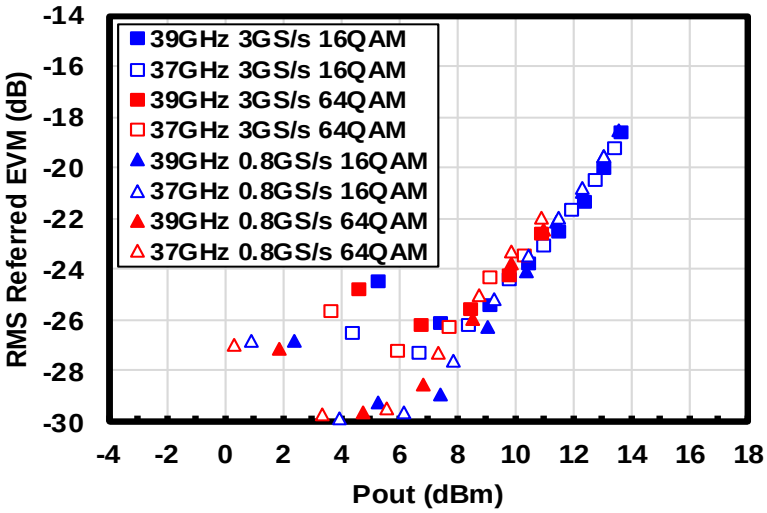


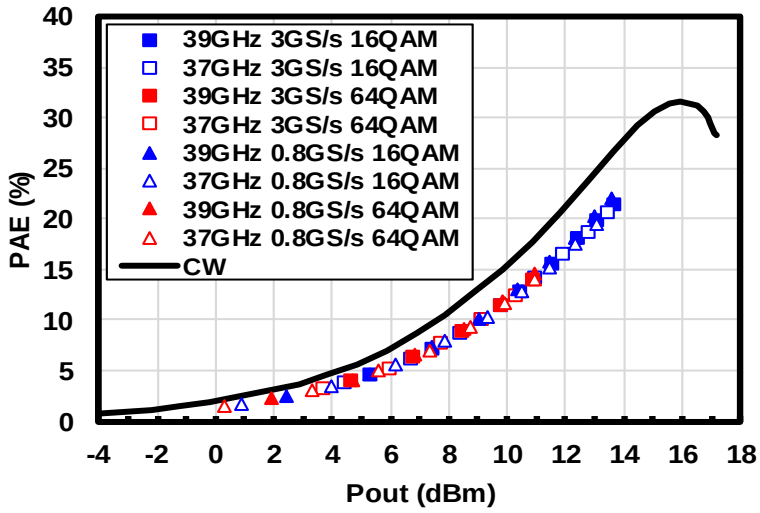
Figure 3.44: Measured 39 GHz single path differential PA P_{SAT} flatness under different supply voltages.

with class AB bias. The PA small signal measurement uses Keysight PNA-X. Figure 3.42 shows the measured S-parameter results. The PA peak gain is 16.2 dB at 39 GHz, and 3-dB bandwidth from 37 GHz to 42 GHz. The 3-dB bandwidth covers 37-GHz band and 39-GHz band for 5G NR in millimeter-wave. Figure 3.43 shows measurement results of the amplifier linearity and efficiency at 39 GHz. The 39 GHz PA achieves 16.3 dBm P_{SAT} 30.3 % maximum power added efficiency (PAE_{MAX}) 14.9 dBm 1dB compression point (P_{1dB}) and 29.5 % power added efficiency at 1dB compression point (PAE_{P1dB}) under 1-V supply. Under 1.1-V supply, the PA achieves 17.2 dBm P_{SAT} 31.2 % maximum power added efficiency (PAE_{MAX}) 15.5 dBm 1dB compression point (P_{1dB}) and 30.2 % power added efficiency at 1dB compression point (PAE_{P1dB}). Figure 3.44 shows the amplifier measured P_{SAT} has 1-dB power variance over the frequency from 35 GHz to 41 GHz. This PA exhibits high performance linearity and power delivery at 39 GHz.

The PA performance with modulation signal is measured using a Keysight AWG M8195A, oscilloscope DSO91304A and external mixer. The single carrier modulation signal is applied to PA, the mixer converts the modulated signal to 39 GHz. After calibrating LO power, the PA output average power versus the PAE and average RMS power normalized EVM performance are measured and shown in Figure 3.45. For 39 GHz 3000MHz 64QAM modulation, the PA has an average output power of 9.0 dBm with 10.0% PAE at -25dBc RMS power normalized EVM under 1.1-V supply, and an average output power of 8.2 dBm with 9.2% PAE at -25dBc RMS power normalized EVM under 1.0-V supply. At 37GHz, with the same 3000MHz 64QAM modulation, the PA has an average output power of 8.5 dBm with 9.3% PAE at -25dBc RMS power normalized EVM



(a)



(b)

Figure 3.45: Measured 39 GHz single path differential PA performance with modulation signal under 1.1-V.

under 1.1-V supply, and an average output power of 8.5 dBm with 8.6% PAE at -25dBc RMS power normalized EVM under 1.0-V supply

The 39 GHz differential amplifier is also power combined using current type power combiner as introduced in section 3.3.2, the detailed 39 GHz power combining power amplifier is discussed in the following section 3.4.2.

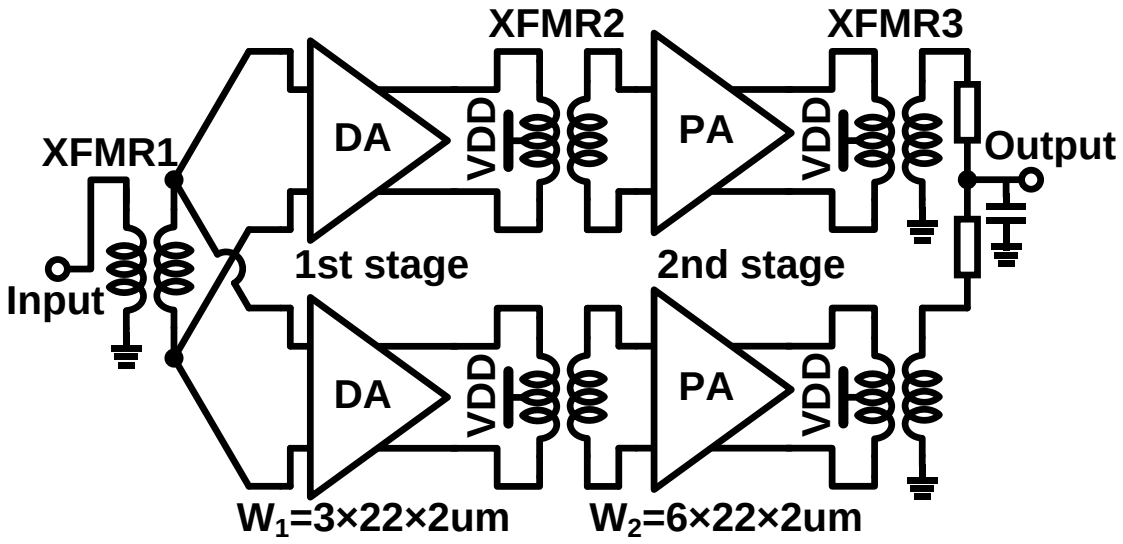


Figure 3.46: 39-GHz two-path power combining differential power amplifier architecture.

3.4.2 39 GHz Power-Combining Power Amplifier

The 39 GHz power combining PA is designed and implemented in order to further increase the output power and linearity, the design detail and measurement results are introduced in this section. As shown in Figure 3.46, the power combining PA consists of two identical paths with both driving stage and power stage. The PA input is single-ended instead of differential due to higher measurement accuracy. Compared with the 1-port or 2-port calibration, the multi-port calibration in vector network analyzer is usually unbalanced and less accurate. The single-ended input is firstly transformed to differential, then transformer (XFMR1) positive and negative outputs are connected to two identical PA paths. The driving stage and power stage in each path is reusing the PA described in section 3.4.1. The driving stage and power stage transistors have the total width of 132um and 264um with 50 fF and 70 fF neutralization capacitor. The outputs from each unit PA path added together through zero-degree power combiner. The zero-degree combiner uses transmission line for low-loss and high accuracy.

Figure 3.47 shows the PA chip micrograph, with a core area of 0.20 mm^2 and TEG area of 0.47 mm^2. The transmission line zero-degree combiner can also be seen in Figure 3.47, the transmission line length is adjusted to provide optimal impedance for power stage transistors. The transformer sizes are exactly the same with 39 GHz single path PA introduced in section 3.4.1. The VDD supply is applied from both upper path and lower path for balanced VDD in differential architecture.

The PA chip is nodnot delivered, therefore here shows simulated small signal performance and large signal performance. Under 1-V supply voltage with class AB bias, the

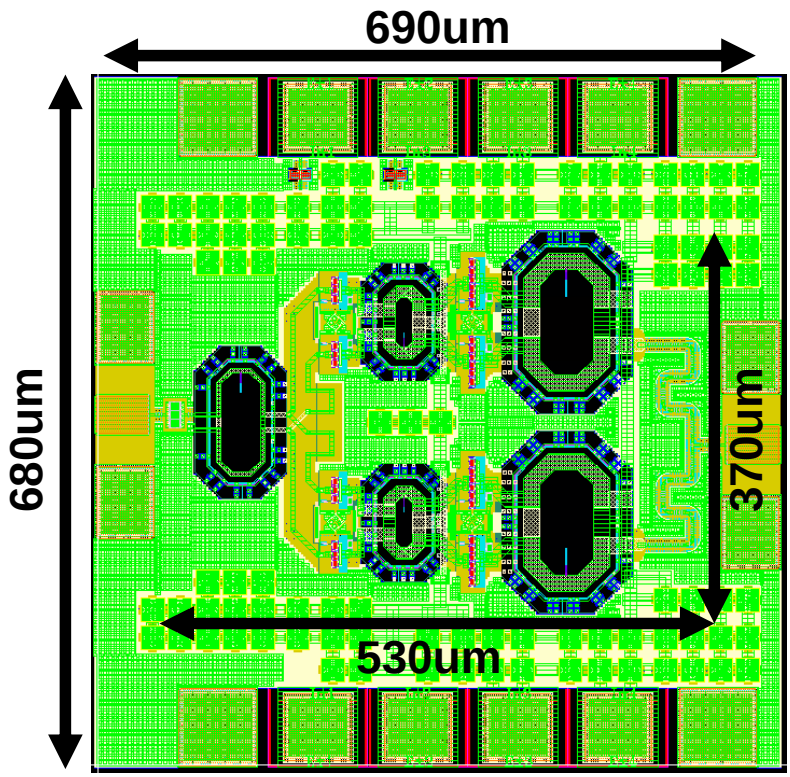


Figure 3.47: Chip layout.

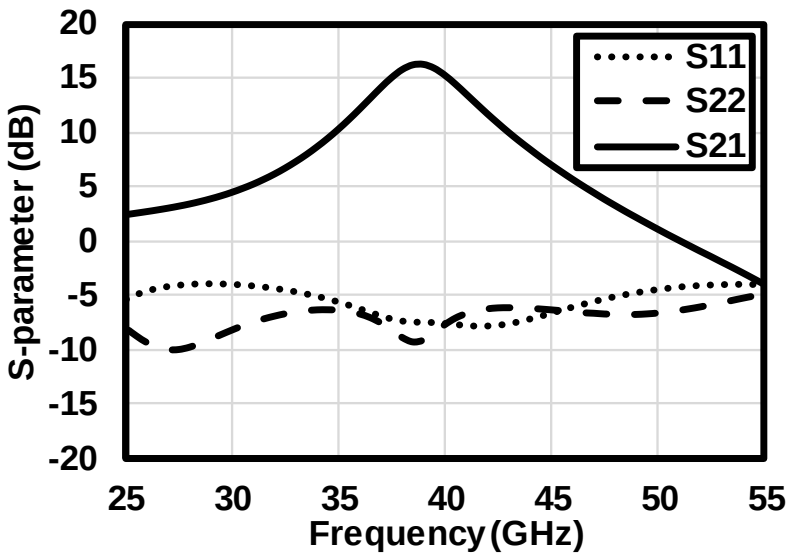


Figure 3.48: Simulated s-parameters of 39 GHz power combining PA.

PA is simulated to obtain s-parameter and large signal performance. Figure 3.48 shows the simulatedd S-parameter results. The PA peak gain is 17.0 dB at 39 GHz, and 3-dB bandwidth from 36.6 GHz to 41.2 GHz. The 3-dB bandwidth covers 37-GHz band and

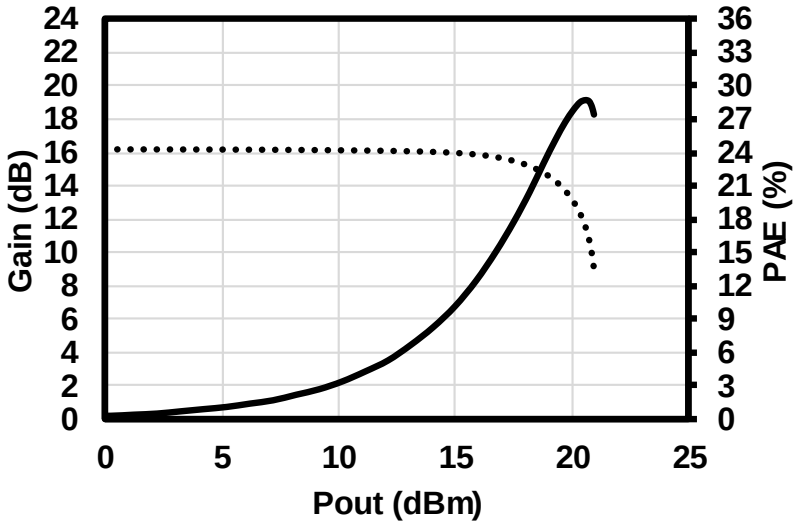


Figure 3.49: Simulated large signal gain and PAE of 39 GHz power combining PA.

39-GHz band for 5G NR in millimeter-wave.

Figure 3.49 shows simulated results of the amplifier linearity and efficiency at 39 GHz. The 39 GHz PA achieves 20.9 dBm P_{SAT} 28.8 % maximum power added efficiency (PAE_{MAX}) 18.2 dBm 1dB compression point (P_{1dB}) and 20.5 % power added efficiency at 1dB compression point (PAE_{P1dB}) under 1-V supply. This PA exhibits high performance linearity and power delivery at 39 GHz.

3.4.3 39 GHz Power Amplifier with TRX Switch

The transmitting/receiving (TRX) switch is widely used for switching between the transmit and receive mode. For a transceiver with its transmitting RF frequency close to receiving RF frequency, the RF antenna can be shared for both transmit mode and receive mode. Figure 3.50 shows the transceiver without TRX switch, in the transmit mode, the transmitter part in the RF front-end is enabled and the antenna connected with PA is used to emit RF signal to the air. In the receiver mode, the receiver part in the RF front-end is enabled and the antenna connected with LNA is used to receive RF signal from the air. It can be found that the total antenna number in a phased-array transceiver is two times of the sub-transceivers number. For a large scale phased-array transceiver, the antenna distribution is one of the main concerns in the implementation. The doubled antenna number will increase the implementation size, cost and complexity. Usually, the transmitting RF frequency and receiving RF frequency is the same for time division duplexing (TDD), the antennas for transmitting and receiving can share the same design specification. In other words, the antenna can be used for both transmitter and receiver. The conceptual

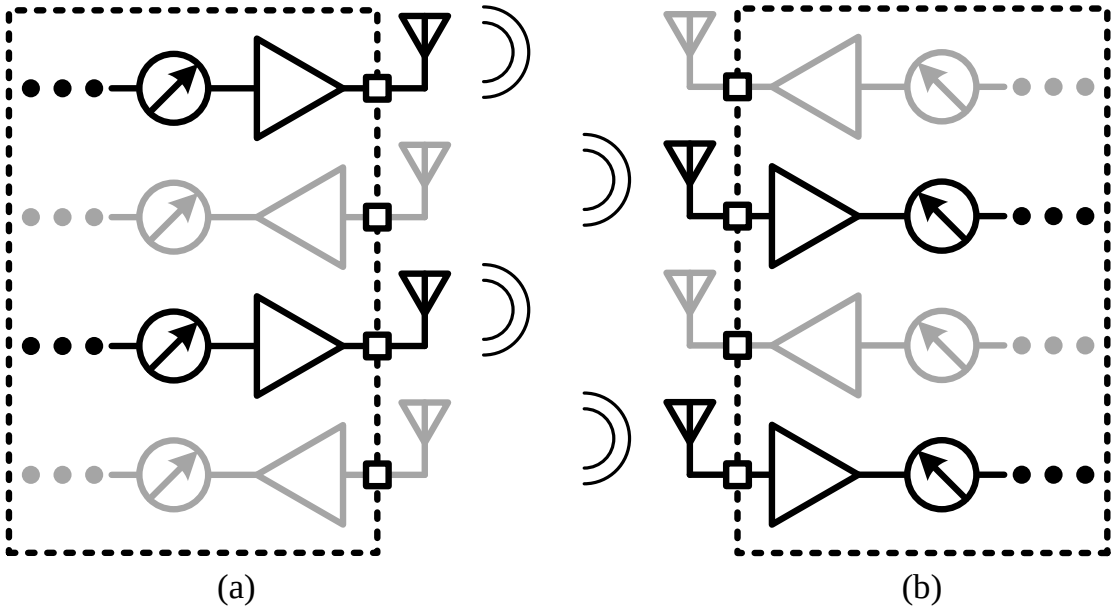


Figure 3.50: Transceiver without TRX switch. (a) TX mode, (b) RX mode.

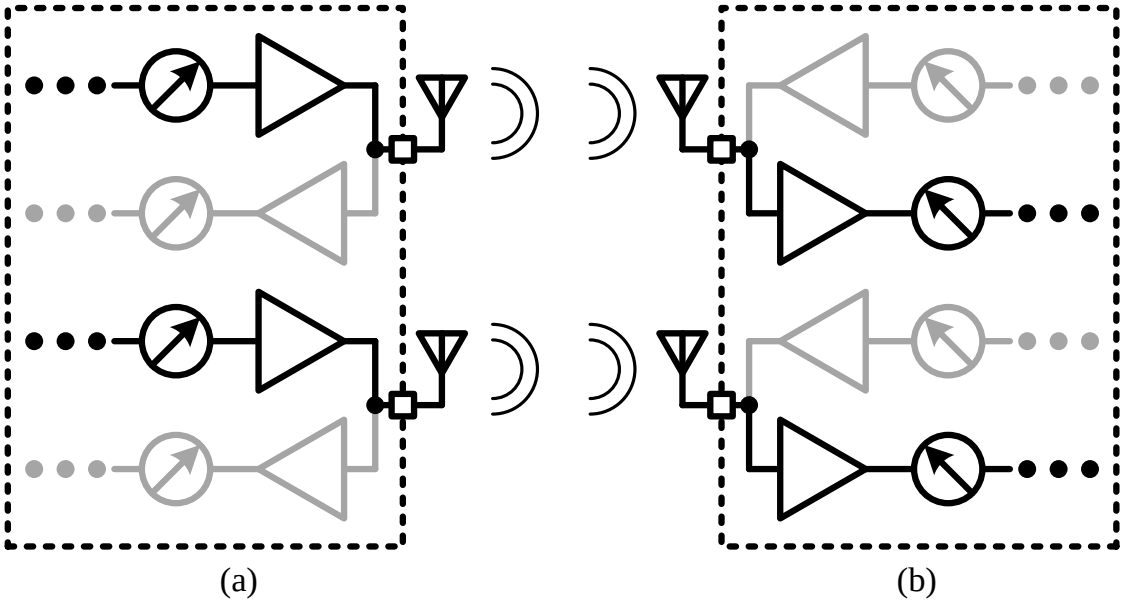


Figure 3.51: Transceiver with TRX switch. (a) TX mode, (b) RX mode.

transceiver with TRX switch shared antenna is shown in Figure 3.51. The antenna is connected to both transmitter PA output and receiver LNA input. On TX mode, the antenna is switched to transmitter PA output, on RX mode, the antenna is switched to receiver LNA input. By sharing antenna, the phased-array transceiver can be implemented compact, low-cost and low-complexity.

The shared antenna by using TRX switch is designed to match the impedance for both

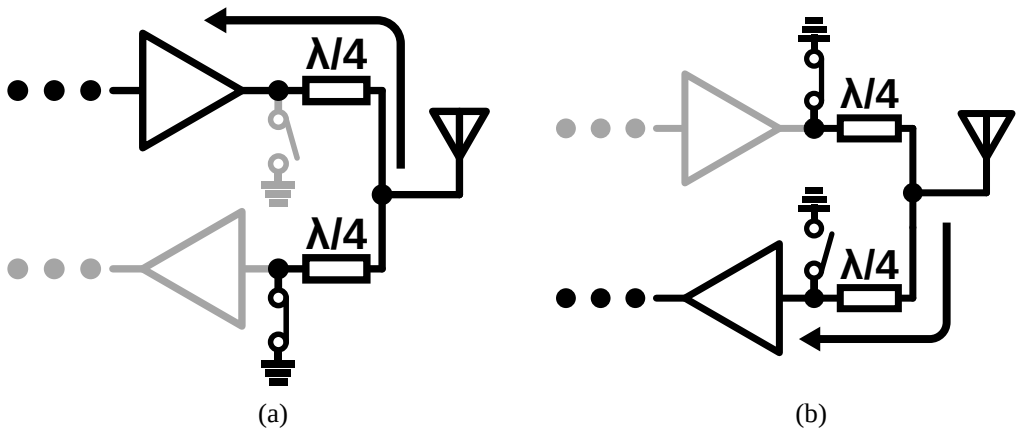


Figure 3.52: Conventional TRX switch using quarter-wave transmission line. (a) TX mode, (b) RX mode.

transmitter PA and receiver LNA. There are mainly three issues in the TRX switch design. 1) impedance mismatch for antenna. 2) optimal impedance matching for PA output and LNA input. 3) insertion loss of the TRX switch.

Figure 3.52 shows a conventional TRX switch using quarter-wave transmission line [42]. As introduced in section 2.1.1, the quarter-wave transmission line is mostly used to transfer impedance between open and load: the impedance see at an open quarter-wave transmission line is short; and the impedance see at a short quarter-wave transmission line is open. In Figure 3.52 (a), the TX mode is enabled by connecting the receiver quarter-wave transmission line to ground and turning off the quarter-wave transmission line switch in the transmitter. The receiver path will show open impedance seen at the antenna, and the transmitter RF signal will be delivered to antenna through a quarter-wave transmission line. For a 50 Ω characteristic impedance antenna, the quarter-wave transmission line at transmitter side has no influence on the PA load impedance. In Figure 3.52 (b), the RX mode is enabled by connecting the transmitter quarter-wave transmission line to ground and turning off the quarter-wave transmission line switch in the receiver. The transmitter path will show open impedance seen at the antenna, and the antenna received RF signal will be delivered to LNA through a quarter-wave transmission line. For a 50 Ω characteristic impedance antenna, the quarter-wave transmission line at transmitter side has no influence on the LNA source impedance. In this architecture, TX-to-RX isolation depends on switch on and off resistances. For a non-ideal switch, both the insertion loss and isolation will be degraded.

Figure 3.53 shows the proposed 39 GHz PA and LNA circuit schematic with shared antenna using stacked transformer. It consists of a 39 GHz PA, a 39 GHz LNA and a stacked transformer. The 39 GHz PA input, drive stage and the power stage are introduced in section 3.4.1. The only difference is the power stage output network, the PA in

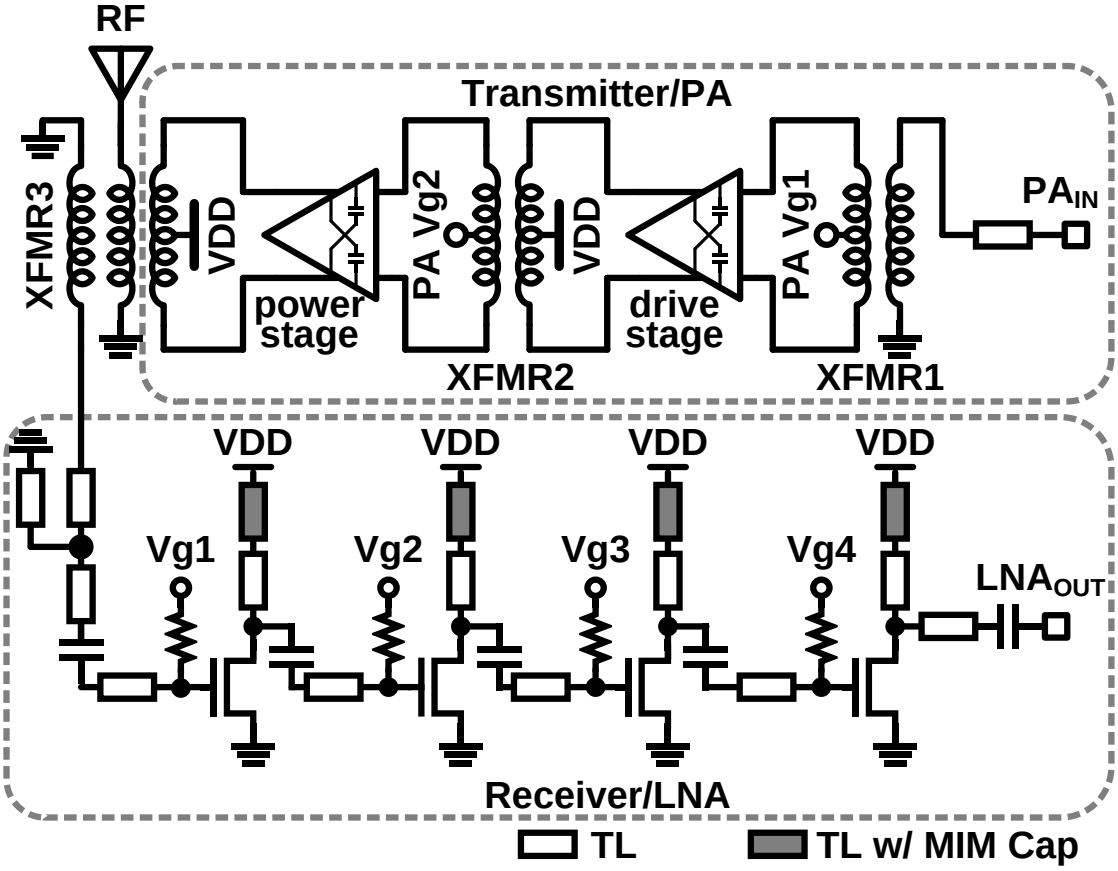


Figure 3.53: 39 GHz PA and LNA circuit schematic with shared antenna using stacked transformer.

section 3.4.1 uses a two-layer vertical transformer as the output network for power stage transistor pair. By contrast, the PA in Figure 3.53 employs a three-stacked transformer (XFMR3) as the load. The three-stacked transformer has three ports: the top layer is connected to PA transistor pair output, the middle layer is connected to antenna with 50 Ω characteristic impedance, the bottom layer is connected to LNA input. The PA power supply is applied at the center tap of the transformer top turn metal. The transformer middle turn and bottom turn are single-ended. The receiver LNA consists of four common stages with matching blocks using transmission line. Two types of transmission line are used, 50 Ω transmission lien and Metal-Insulator-Metal transmission line (MIMTL). The MIM transmission line is the transmission line connected with parallel Metal-Insulator-Metal capacitors. The parallel capacitor is used for two purposes: one is VDD supply decoupling, and another is to provide low impedance to ground for RF signal, which is part of the matching network.

The stacked transformer is modeled and simulated in 3D electromagnetic (EM) simu-

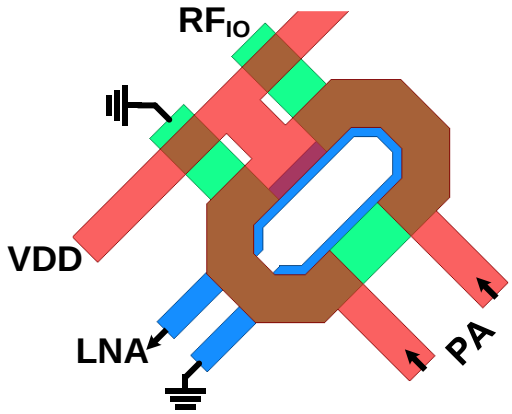


Figure 3.54: Stacked transformer EM model.

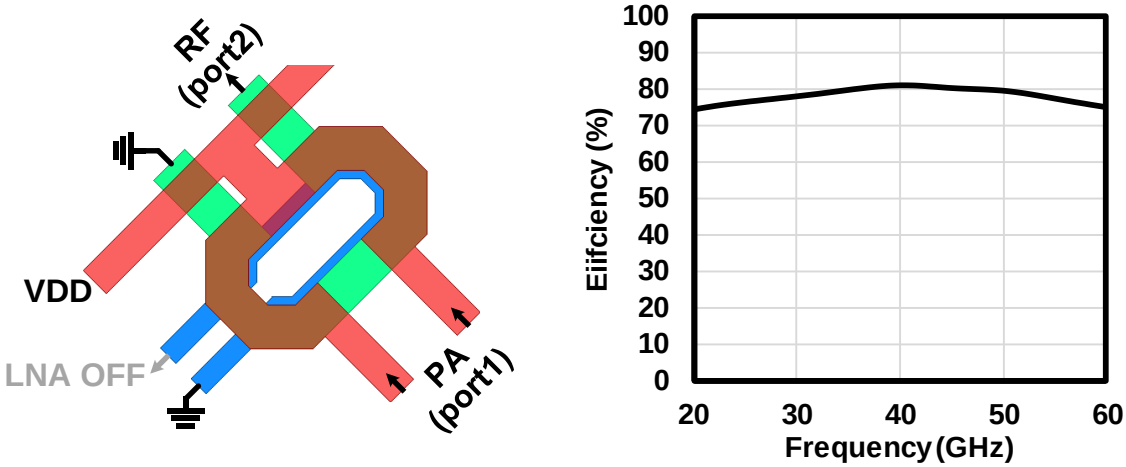


Figure 3.55: PA mode transformer signal path and transformer efficiency.

lator. Figure 3.54 shows the top view of the three-stacked transformer for shared antenna. The red color metal layer is at the top, it is connected to the PA output. The PA VDD supply is also at the top layer connected to the center tap. The meddle metal layer is green color, it couples PA output signal electromagnetically and converts differential signal to single-ended, which is connected to 50 Ω impedance antenna. The bottom metal layer is blue colored with single-ended output connected to LNA. The individual PA mode and LNA mode transformer simulation results are given below.

Figure 3.55 shows the PA mode transformer signal path and transformer efficiency. On PA mode, the LNA is turned off, so that the impedance see to the LNA is high. The top two layers are used, the PA differential signal (port1) is converted to single-ended for transmitting using antenna. The EM simulation result shows that, when LNA is off, the transformer efficiency from PA output to antenna input is 80 % at 39 GHz.

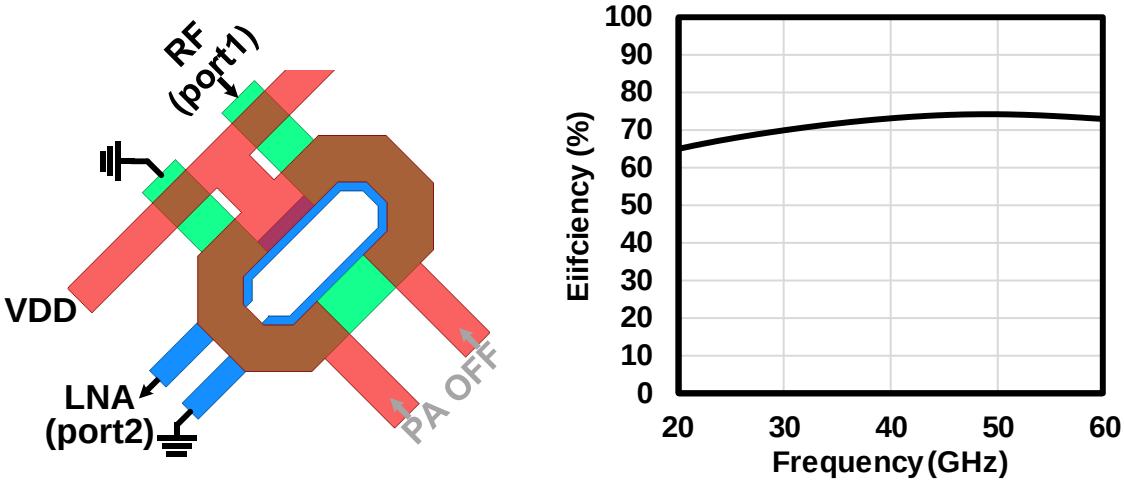


Figure 3.56: LNA mode transformer signal path and transformer efficiency.

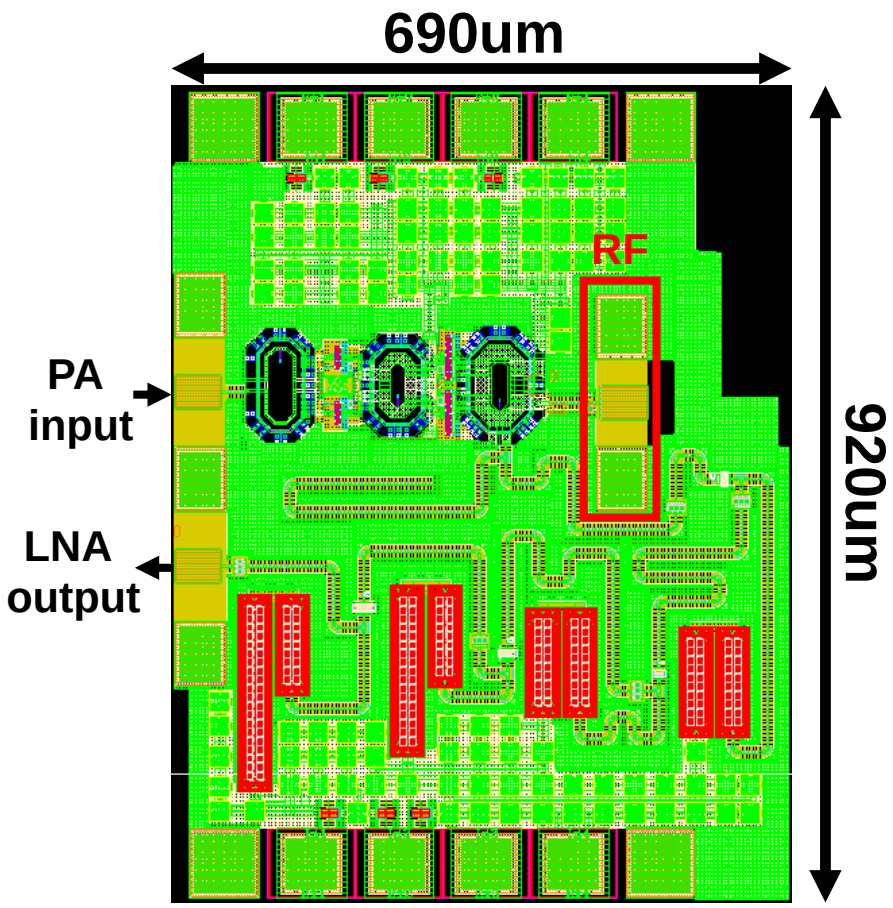


Figure 3.57: Implemented chip micrograph of PA and LNA with shared antenna.

Figure 3.56 shows the LNA mode transformer signal path and transformer efficiency. On LNA mode, the PA is turned off, so that the impedance see to the PA is high. The

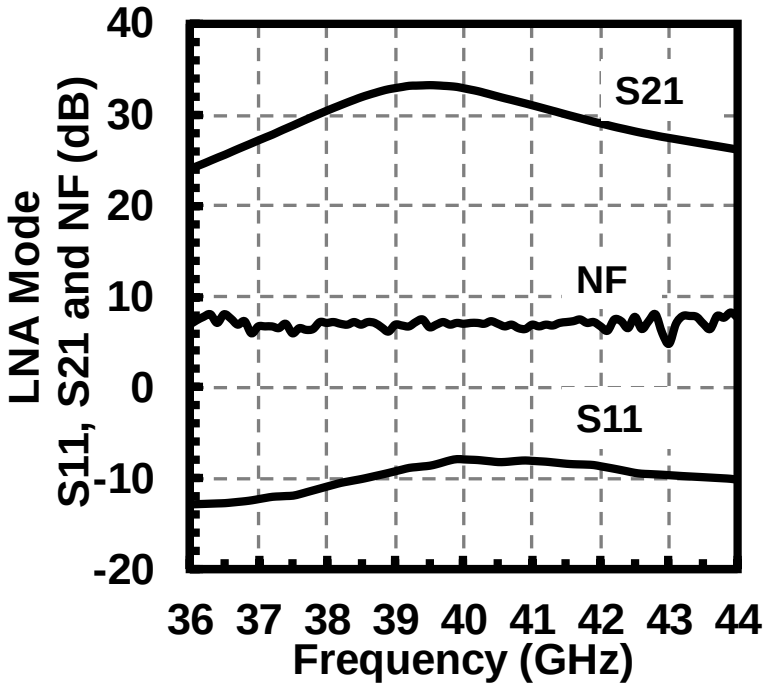


Figure 3.58: LNA mode small signal and NF measurement results.

middle layer and bottom layer are used, the antenna received signal is coupled to LNA electromagnetically. Both the antenna and the LNA input are single-ended. The EM simulation result shows that, when PA is off, the transformer efficiency from antenna (port1) to the LNA input (port2) is 73 % at 39 GHz. The transformer efficiency on LNA mode is relatively lower than the PA mode due to the bottom layer metal lower thickness.

The proposed PA and LNA is implemented and measured using a standalone TEG, as shown in Figure 3.57. The PA and LNA TEG is fabricated in standard 65-nm CMOS technology. The LNA mode is enabled by turning off the PA biases and turning on the LNA biases. The LNA mode measurement results are shown below. The LNA performance is characterized in 50-Ω on-wafer measurement setup under 1-V supply voltage with fixed class 0.5 V bias at all stages. The LNA small signal measurement uses Keysight PNA-X E8361A. There are two RF PADs for probe measurement, one is a ground-signal-ground-signal-ground (GSGSG) type, another is ground-signal-ground (GSG) type. The LNA is measured by two-port network configuration, and the GSGSG pad uses GSG type RF probe, which means the PA input with high impedance. Figure 3.58 shows the LNA mode measured noise figure (NF), small signal gain (S21), input reflection coefficient (S11). The LNA achieves a small signal gain of 33 dB at 39 GHz and a noise figure of 7 dB over 37 GHz to 41 GHz. The reflection coefficient is -9 dB at 39 GHz for 50 Ω antenna impedance.

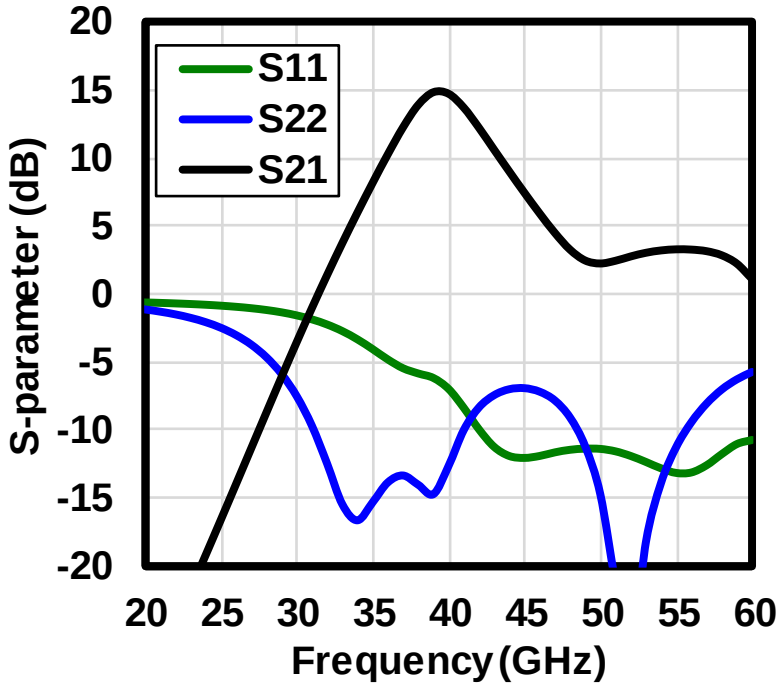


Figure 3.59: PA mode small signal measurement results.

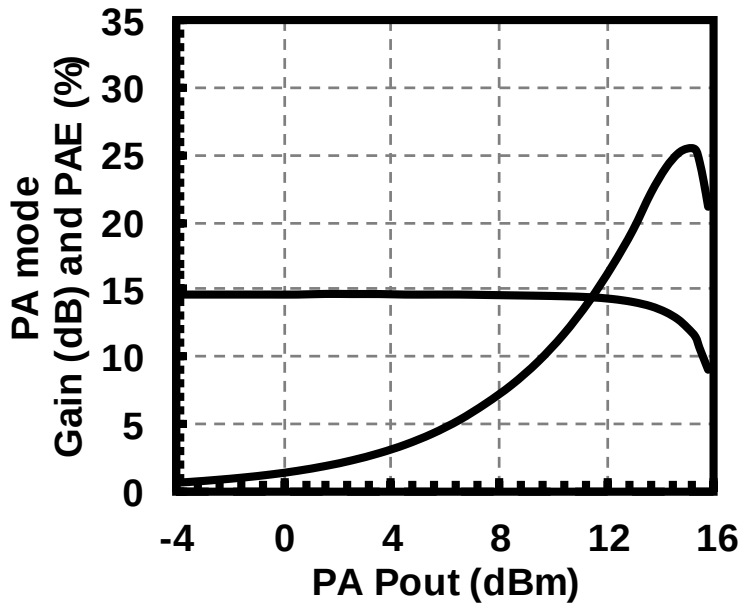


Figure 3.60: PA mode large signal measurement results.

The PA performance is also characterized in 50-Ω on-wafer measurement setup under 1-V supply voltage. The biases are 0.3 V for first stage and 0.6 V for second stage. The PA input port uses GSG type RF probe, which mheans the LNA output is with high impedance. Due to the off state isolation, the LNA output impedance has no influence on

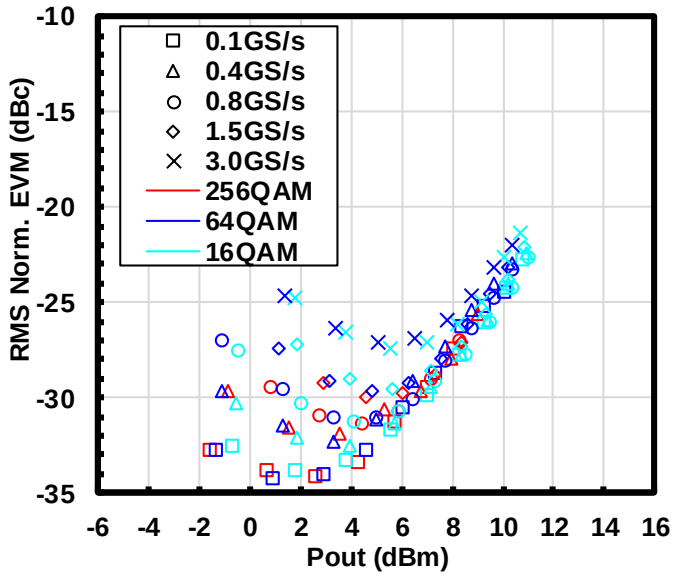


Figure 3.61: Measured EVM performance with modulation signal.

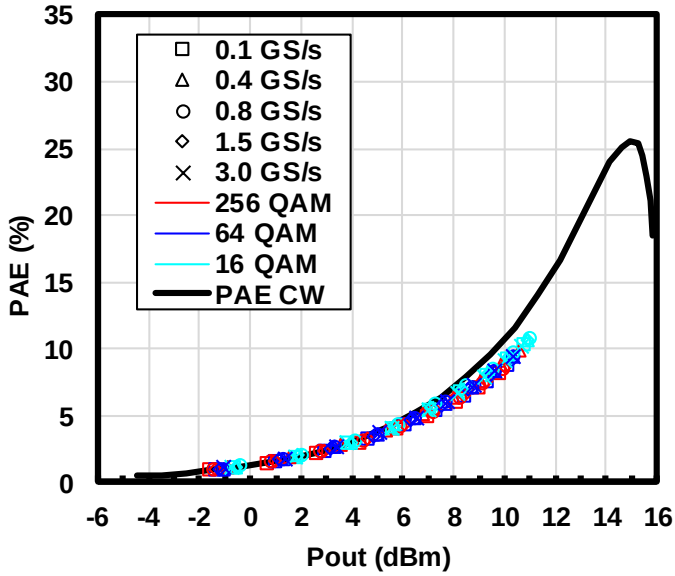


Figure 3.62: Measured PAE performance with modulation signal.

the PA performance. Figure 3.59 shows the PA mode measured small signal gain (S21), input and output reflection coefficient (S11, S22). The PA achieves a small signal gain of 14.7 dB at 39 GHz and a 3-dB bandwidth from 36.7 GHz to 42.5 GHz.

Figure 3.60 shows measurement results of the amplifier linearity and efficiency at 39 GHz. The 39 GHz PA mode achieves 15.5 dBm P_{SAT} 25.5 % maximum power added efficiency (PAE_{MAX}) 13.6dBm 1dB compression point (P_{1dB}) and 22.7 % power added efficiency at 1dB compression point (PAE_{P1dB}) under 1-V supply. This PA shows 0.8 dB degradation from PA without antenna switch introduced in Section 3.4.1.

Table 3.1: Performance comparison with state-of-the-art PAs for 5G millimeter-wave.

	This Work								
	28 GHz	28GHz combine	39GHz	39GHz combine	39GHz w/SW	[43]	[44]	[45]	[46]
Technology	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS	40-nm CMOS	40-nm CMOS	65-nm CMOS	130-nm SiGe
Frequency (GHz)	28	28	39	39**	39	27	27	28	37
Gain (dB)	15.0	14.7	17.0	16.2**	14.7	22.4	20.5	15.8	17.1
P_{SAT} (dBm)	17.6	20.2	17.2	20.9**	15.5	15.1	18.1	15.6	17.1
P_{1dB} (dBm)	16.2	17.0	15.5	18.2**	13.6	13.7	16.8	14	15.5
PAE_{MAX} (%)	30.3	24.5	31.2	28.8**	25.5	33.7	41.5	41	22.6
PAE_{P1dB} (%)	23.2	20.7	30.2	20.5**	22.7	31.1	37.6	34.7	21.6
64QAM Mod. BW	0.8 GS/s	2.5 GS/s	3 GS/s	-	3 GS/s	0.8 GHz	1 GS/s	0.34 GS/s	0.5 GS/s
EVM (dBc)	-26$	-26	-25	-	-25	-25	-25	-26.4#	-27#
Pout (dBm)@ EVM	11.7$	11.4	9.0	-	8.4	6.7	8.4	9.8#	9.3#
PAE (%)@ EVM	-	6.8	10.0	-	7.5	11	8.8	18.2#	-
Supply (V)	1	1.1	1.1	1	1	1.1	1	1.1	1.5
Area (mm^2)	0.167	0.23	0.081	0.196	0.08	0.23	0.36	0.24	1.76

*estimated graphically #constellation peak power referred EVM **simulation data $evaluated using 28 GHz transceiver

The PA mode performance with modulation signal is measured using a Keysight AWG M8195A, oscilloscope DSO91304A and external mixer. The single carrier modulation signal is applied to PA, the mixer converts the modulated signal to 39 GHz. After calibrating LO power, the PA output average power versus the PAE and average RMS power normalized EVM performance are measured and shown in Figure 3.61 and 3.62. For 39 GHz 400MHz 64QAM modulation, the PA has an average output power of 9.1 dBm with 7.5% PAE at -25dBc RMS power normalized EVM under 1-V supply.

3.5 Performance Summary

Table 3.1 shows the performance summary table of state-of-the-art millimeter-wave power amplifier. The proposed power amplifier with high quality-factor transformer achieves high linearity and high output power at both 28 GHz and 39 GHz. From the table 3.1, it can be seen that the proposed power amplifier achieves highest P_{SAT} and highest average output power with decent constellation among the PAs for 5G millimeter-wave.

3.6 Conclusion

This chapter presents the detailed design of power amplifiers for 5G NR 28GHz 39GHz band. In order to achieve highest P_{SAT} without increasing supply voltage or stacking transistors, the proposed power amplifiers employ high quality-factor vertical transformer

for impedance matching. Current-type power-combining power amplifier and a 39 GHz antenna switch PA/LNA are implemented. The amplifiers are implemented and evaluated by using wideband modulated signal. The proposed amplifiers achieves highest P_{SAT} and highest average output power with modulation signal.

Chapter 4

Millimeter-Wave Phased-Array Transceiver For 5G New Radio

This chapter discusses the high linearity millimeter-wave phased array transceiver implementation. Starting with the basic of the phased-array transceiver architecture and challenge, detailed 39GHz transceiver front-end are introduced and discussed. The phased-array transceiver is implemented and evaluated with 5G New Radio signal.

4.1 5G Phased-Array Transceiver Introduction

Phased array systems play an important role in communication systems that will be deployed on the next generation cellular network (fifth generation, 5G). The phased-array mechanism is illustrated in Fig. 4.1. For an ideal isotropic element antenna, its radiation strength is constant in any direction. By employing 3-isotropic-element antenna array, the radiation strength is centralized to a certain direction, while the radiation strength cannot stay constant. Besides the beam main direction, the radiation strength in the rest of direc-

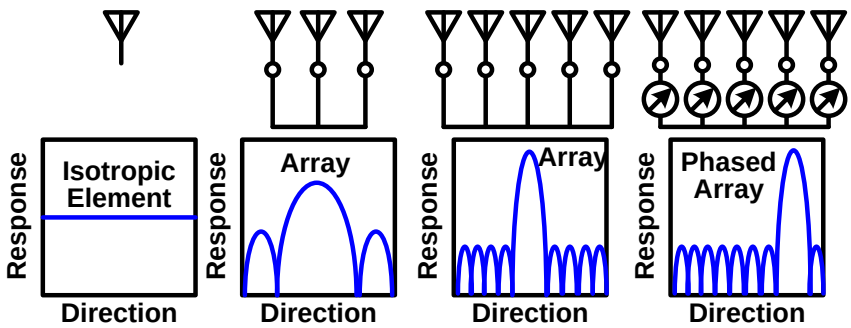


Figure 4.1: Phased-array mechanism.

tions are suppressed with small sidelobes. Further increasing the antenna array elements can enhance the radiation strength with a narrower main beam direction. The phased-array is realized by introducing constant phase difference between each antenna elements. By introducing the phase difference, the antenna array radiates signal with a controlled direction. Usually a linear phased-array architecture is used for beamforming. As shown in Fig. 4.2, the linear phased array consists of a number of antenna elements with equal distance and phase difference between each antenna element. The phased-array beamforming direction relationship with the antenna element distance and the initial phase can be expressed as:

$$\Delta\varphi = \frac{2\pi}{\lambda} d \sin(\theta) \tag{4.1}$$

where $\Delta\varphi$ is the phase difference between the antenna elements, d is the equal distance between the antenna elements, θ is the beam steering angle shift from 0 degree phased array beam direction [47].

Recently, there have been several demonstrations of phased-array-based data links in the mm-wave bands [48–51]. The phased-array transceiver architecture can be divided into two main types: phase shift in the RF path, and phase shift in the LO path. Fig. 4.3 and 4.4 shows the two types of phase shifting transmitter architecture. The RF phase

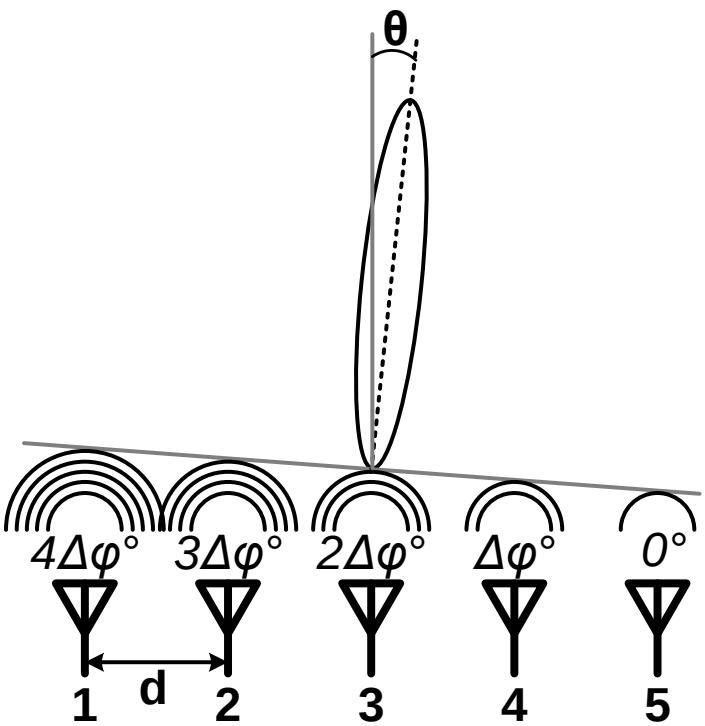


Figure 4.2: A equal spaced linear array transmitter with 5 elements.

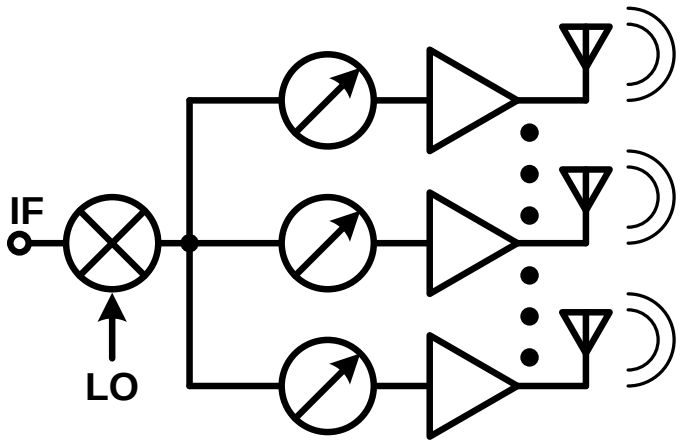


Figure 4.3: RF phase shifting transmitter architecture.

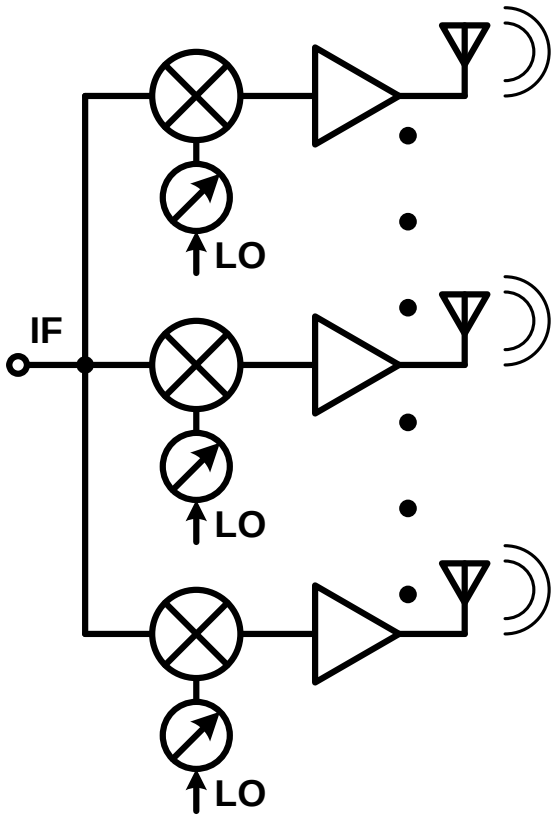


Figure 4.4: LO phase shifting transmitter architecture.

shifting transmitter contains one mixer for all the RF paths, the phase is shifted in each sub-transmitter. The benefits and disadvantages of this architecture are as follow. The RF phase shifting architecture contains less components than a LO phase shifting architecture, thus it occupies less area. The RF phase shifting also has a simpler layout

architecture due to the single LO distribution [52–57]. However, realizing constant gain phase shifter in the RF path is difficult, which degrades the beamforming quality. Also the RF phase shifting requires large RF drive power to enable more elements, which is challenging to design the high linearity RF amplifier.

The LO phase shifting architecture, as mentioned, has more components and complex LO distribution. On the other hand, it can realize constant-gain phase shifting characteristic, and driving the phased-array transceiver in low frequency IF is easier than driving in the RF frequency. The phased-array transceiver presented in this dissertation chooses LO phase shifting to target the low phase and gain error for high quality beamforming in large array [36].

By employing the phased-array architecture, the communication distance can be extended with the enhanced equivalent isotropic radiated power (EIRP). The EIRP is the measured radiated power of an antenna in a specific direction. For an isotropic antenna or an ideal antenna, the power is radiated uniformly in all directions. An isotropic antenna is often used as a reference antenna for the antenna gain, the gain for isotropic antenna is 0dBi. The EIRP is defined as the RMS power input in watts required to a lossless isotropic antenna to give the same maximum power density far from the antenna as the actual transmitter. It is equal to the power input to the transmitter's antenna multiplied by the isotropic antenna gain. The single transmitter EIRP can be expressed as:

$$EIRP_{1\mathrm{TX}} = P_{\mathrm{OUT\_1TX}} + G_{\mathrm{A\_1TX}}\ (dBm) \tag{4.2}$$

where $P_{\mathrm{OUT\_1TX}}$ denotes the one transmitter excitation power at antenna input port, $G_{\mathrm{A\_1TX}}$ denotes the transmitter antenna gain.

The N-element phased array transmitter EIRP can be expressed as:

$$\begin{aligned} EIRP_{\mathrm{NTX}} &= P_{\mathrm{OUT\_NTX}} + G_{\mathrm{A\_NTX}}\ (dBm) && (4.3)\\ &= (P_{\mathrm{OUT\_1TX}} + 10\log_{10}(N)) + (G_{\mathrm{A\_1TX}} + 10\log_{10}(N)) && (4.4)\\ &= P_{\mathrm{OUT\_1TX}} + G_{\mathrm{A\_1TX}} + 20\log_{10}(N) && (4.5) \end{aligned}$$

As illustrated in Fig. 4.5, for both single transmitter and phased array, the communication distance depend on the RX sensitivity. For single TX, the EIRP is lower and the distance $d1$ is short. With the same RX, by employing N-element phased-array, the transmitted EIRP is increased by the power summation and beamforming effect, which is $20\log_{10}(N)$. It can be observed that the phased array communication distance $d2$ is proportional to the array element N with the same sub-array transmitter output power.

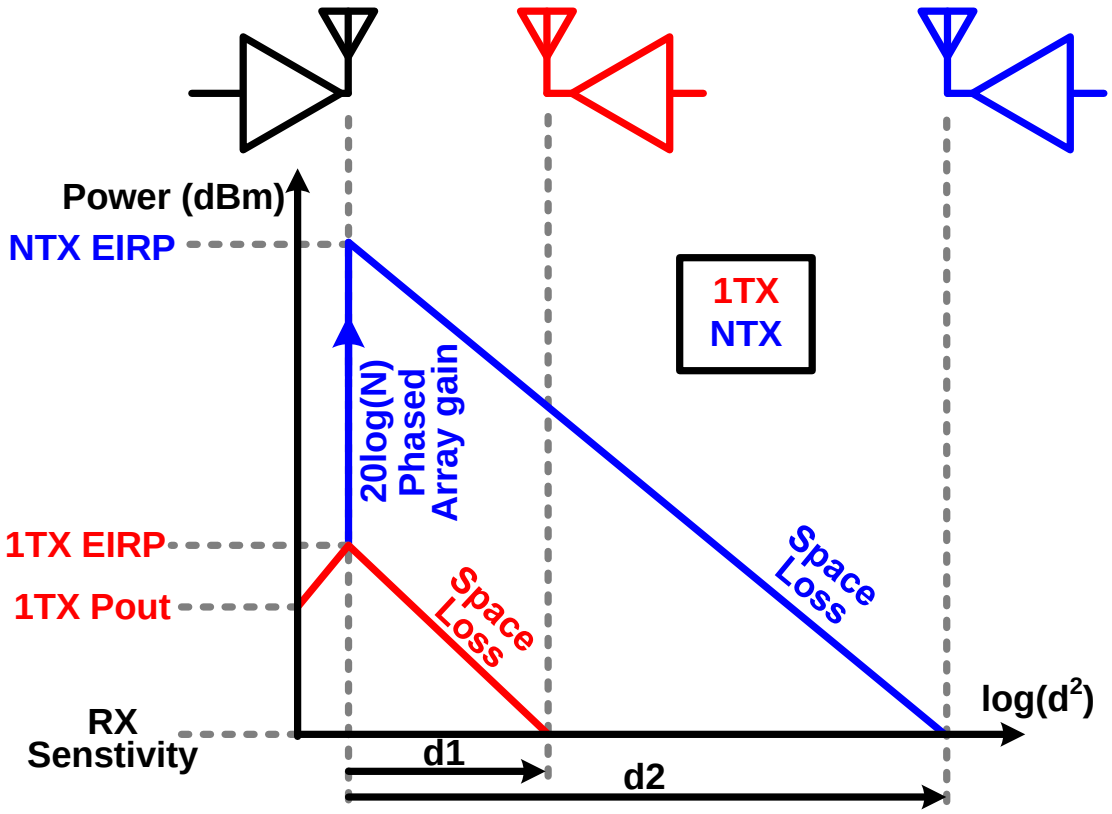


Figure 4.5: Phased-array transmitter with isotropic RX antenna.

4.2 Phased-Array Transceiver for 5G NR 28GHz Band

A phased-array transceiver for 5G NR 28 GHz band is introduced in this section. The monolithic phased-array transceiver consists four sub-array TRXs in a chip. The LO phase shifting architecture is decided in the transceiver design. The power amplifier introduced in section 3.3.1 is employed in the transmitter. This section introduces the detailed transceiver architecture and calculated level diagram in section 4.2.1. The measurement results are also introduced in section 4.2.2.

4.2.1 Transceiver Front-End Design

This section introduces the 28 GHz phased-array transceiver front-end design. It includes the system design, sub-TRX circuit design, LO phase shifter and calculated link level diagram.

The sliding IF transceiver architecture is chosen in this design due to less number of LO generation circuits. The sliding IF phased-array transmitter architecture is shown in Figure 4.6, the baseband signal (BB) frequency is at DC, the external LO (LO_{EX}) and

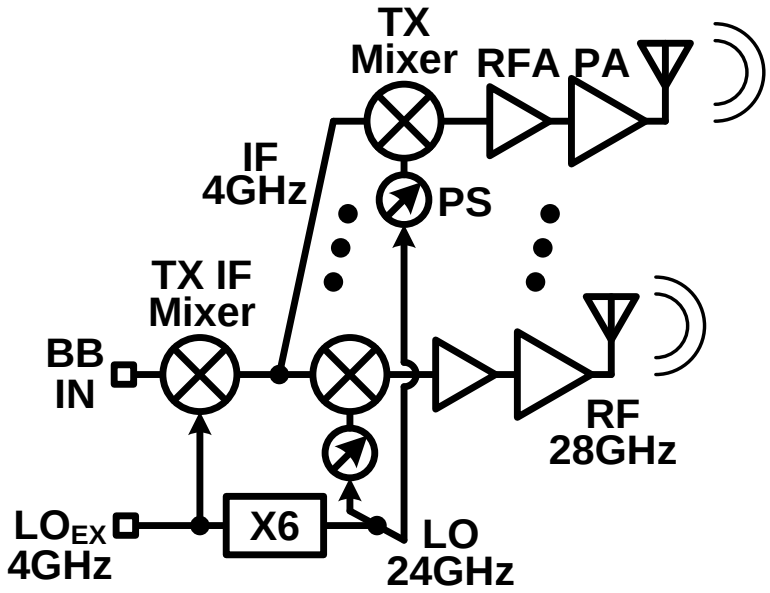


Figure 4.6: Sliding IF 28 GHz phased-array transmitter architecture.

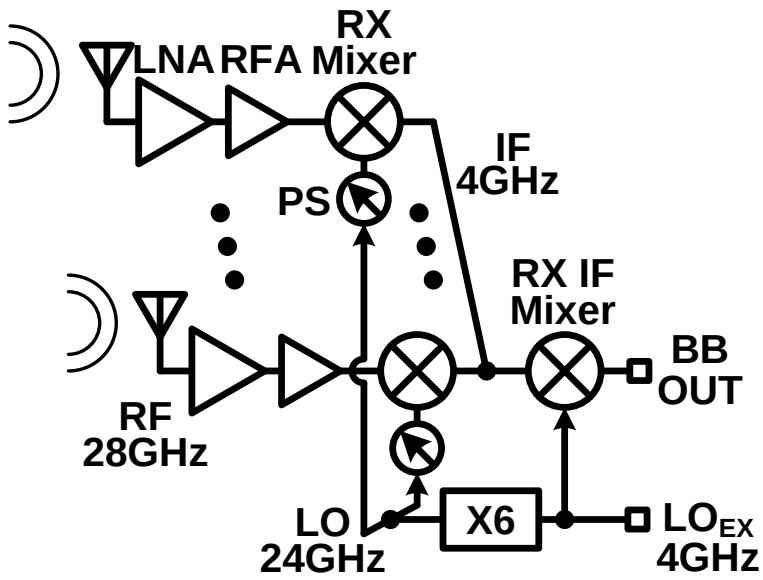


Figure 4.7: Sliding IF 28 GHz phased-array receiver architecture.

intermediate frequency (IF) is at 4 GHz, the radio frequency (RF) is then at 28 GHz. The sliding IF architecture with a frequency multiplier or a frequency divider can share one frequency generator in the IF stage and the RF stage. In this design, the IF and LO_{EX} frequency are chosen at 4 GHz. To set the RF frequency at 28 GHz, the ×6 LO multiplier is required. Figure 4.7 shows the sliding IF phased-array receiver architecture. The same with transmitter architecture, the sliding IF receiver has RF at 28 GHz, IF and LO_{EX} at 4

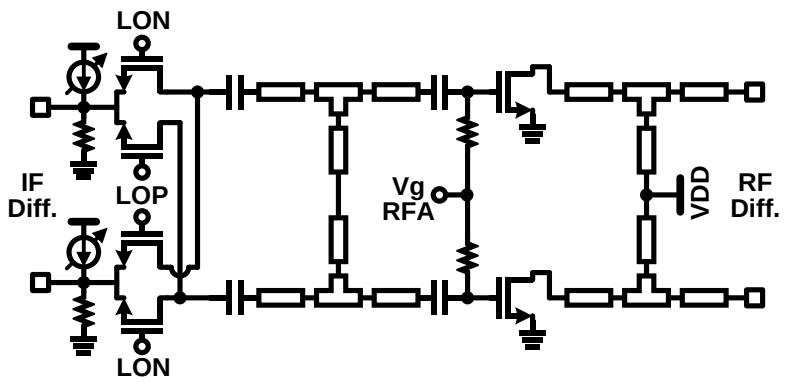


Figure 4.8: Double-balanced mixer and RF-amplifier.

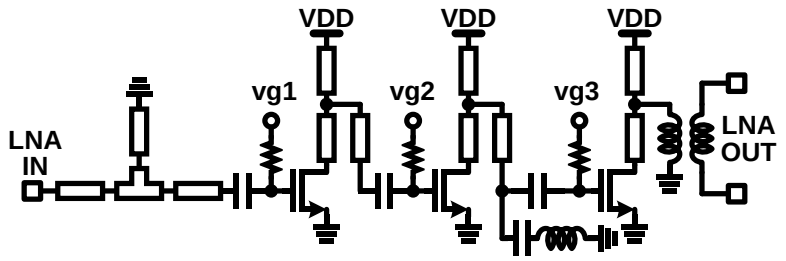


Figure 4.9: LNA circuit schematic.

GHz with a ×6 LO multiplier.

As introduced in [36], the 28 GHz RF transceiver IF signal is not integrated monolithically, an external IF circuit is used in the 28 GHz wireless system. The RF transceiver consists of sub-array transmitter, receiver and LO chain. The LO chain includes frequency multiplier, poly-phase-filter (PPF) and phase shifter. The RF interfaces are single-ended for PA RF output and LNA RF input due to simple connection with antenna. For higher power delivery and noise immunity, the RF front-end circuits are differential except in LNA and LO buffer.

The LO chain detail is described in [36] which demonstrates a 0.04° fine tuning step and less than 0.2 dB gain variation.

In the transmitter side, a double-balanced mixer converts the input IF signal to RF followed by a RF-amplifier. The mixer and RF-amplifier detailed circuit schematic is shown in Figure 4.8. The DC-offset of mixer input positive and negative paths can be adjusted for further local-oscillator feed through (LOFT) cancellation [28]. The RF amplifier provides 10 dB power gain. The double-balanced mixer has 7dB conversion loss, therefore the total gain of mixer and RF-amplifier is 3 dB. The RF amplifier is followed by a differential power amplifier introduced in section 3.3.1.

In the receiver side, the LNA is single-ended due to the antenna interface type. Figure

4.9 shows the 28 GHz LNA circuit schematic. The LNA consists of three common source stages with a notch filter at the inter-stage of second transistor and third transistor, a short stub is used in the LNA input for low-noise matching. The notch filter is centered at 20 GHz, which is frequency of the transmitter image signal. Without suppressing image signal at receiver side, the receiver system overall noise figure will be 3 dB worse, because the image noise appears at the output along with noise associated with the desired received frequency, this effectively doubles the noise power (3 dB) at the output of the IF. The LNA single-ended output is converted to differential for double-balanced mixer through a balun. From simulation, the LNA provides a small signal gain of 19 dB and a noise figure of 5 dB. The RF mixer and RF-amplifier in receiver side reuses the mixer and RF-amplifier in transmitter side.

The transmitter linearity and receiver noise figure are the dominant factors of communication distance. In transmitter side, when the saturate output power and system linearity are high, the transmitter can emit high output power high-order modulation signal. Usually, in order to emit high-order modulation signal, the output power is required to backoff from 1dB compression point into linearity region. When the transmitter system linearity is low, for linear amplification, the output power is also low. The low linearity has mainly two issues. One is the low output power, it directly decides the wireless communication distance. Another is the SNR limitation due to the low signal input power at the backoff

Table 4.1: Characteristics of each building blocks on simulation.

TX	Gian [dB]	Noise figure [dB]	OIP3 [dBm]
IF Div.	-8	12	∞
RF Mixer	-7	9	10
RF amp.	10	11	13
PA	15	12	27
TX Cumulative	10	31	24

RX	Gian [dB]	Noise figure [dB]	IIP3 [dBm]
LNA	19	5	-11
RF amp.	9	5	4
RF Mixer	-7	9	17
IF combine	-2	1	∞
RX Cumulative	19	5.2	-17

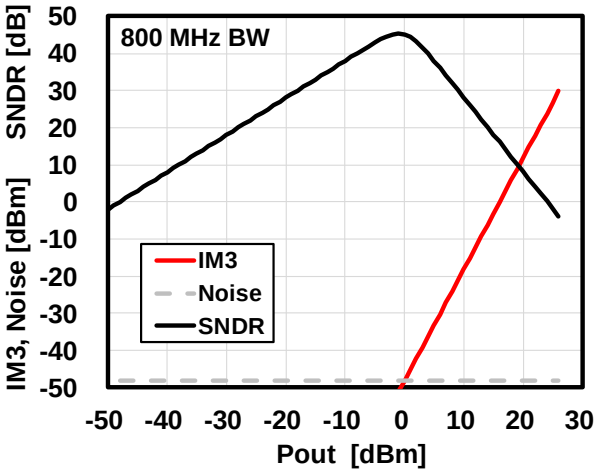


Figure 4.10: TX one channel 800MHz BW calculated SNDR vs TX output power.

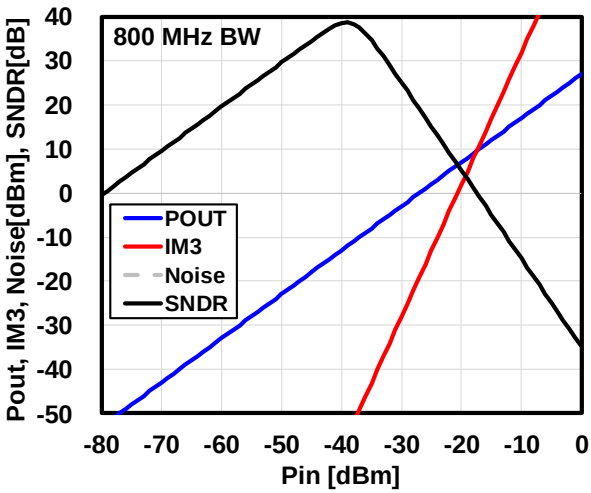


Figure 4.11: RX one channel 800MHz BW calculated SNDR vs RX input power.

point. In the receiver side, the linearity issue is much relaxed since it will not push the receiver output signal as high as possible. The noise figure in a receiver system has a direct impact on its sensitivity. The specifications of each building block in transceiver RF system is discussed below.

The design specifications of each blocks in the 4-element phased-array transceiver are listed in table 4.1. In the TX, the IF divider represents the IF input signal distributed to four sub-array TX, and the power divided loss is 8 dB. The IF input signal distribution path is designed fully symmetric for each TX, therefore the IF divider loss is relatively higher. Because the IF power divider is uses transmission line only, the OIP3 is thus infinity. The same with the IF combiner in the RX. The IF combiner shows 2 dB loss when one channel RX is enabled. The sub-array receiver IF output is 0-degree power combined through transmission line.

Figure 4.10 and Figure 4.11 show the calculated one channel TX and RX signal-to-noise-and-distortion ratio (SNDR) in respect with RF power. For one channel TX with 800 MHz signal bandwidth, the maximum achievable SNDR is 45 dB at -1 dBm TX output power. As discussed in Figure 2.18, the SNDR > 26dB is regarded as requirements of TX or RX which is capable of 64 QAM modulation with a BER of 10^{-3}. It can be seen that the TX has 30 dB dynamic range of SNDR > 26 dB. For one channel RX with 800 MHz signal bandwidth, the sensitivity of RX with SNDR > 26 dB is -55 dBm. The RX peak SNDR is 39.5 dB with input power at -40 dBm.

From above calculation, it can be seen that, for one channel TX and RX, the optimal TX output power is -1 dBm and the optimal RX input power is -40 dBm. Assuming no cable loss from the RF ports connecting to antenna, and isotropic antenna is employed for both TX and RX. The free space propagation loss from TX to RX with distance of d is expressed using Friis transmission formula:

$$\frac{P_r}{P_t} = D_t \cdot D_r \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \tag{4.6}$$

where $P_r = -40$ dBm, $P_t = -1$ dBm, $D_t = D_r = 1$, $\lambda = 10.7$ mm for 28 GHz. One channel communication optimal distance d for highest system SNDR is then calculated as:

$$d = \frac{\lambda}{4\pi} \cdot \sqrt{D_t \cdot D_r \cdot \frac{P_t}{P_r}} \tag{4.7}$$

$$= \frac{0.0107}{4\pi} \cdot \sqrt{\frac{10^{-1/10}}{10^{-40/10}}} \tag{4.8}$$

$$= 0.076 \text{ m} \tag{4.9}$$

The calculation above is the link of one channel TX to one channel RX. The communication down link considers TX as the base station (BS) and RX as the user equipment (UE). Usually the array size of a base station is much larger than the size of a user equipment. The up link is using UE as TX and BS as RX. Therefore, the EIRP of down link can be much higher than the EIRP of uplink because of more transmitter elements are used in down link. Figure 4.12 shows the phased-array transceiver down link calculated SNDR as a function of distance d with signal bandwidth of 800 MHz. Different array scales are used in the calculation. Figure 4.12 (a) shows the 1TX and 1RX case, the highest SNDR is around 0.1m, which matches the optimal distance derived in equation (4.8). Figure 2.18 shows the system required SNR for various modulation schemes. SNR > 23 dB can be regarded as capable of 64 QAM modulation, which is most commonly used in high data rate wireless communication. By using 1024 TX elements in base station and 8 elements

in user equipment, the longest communication distance is 800 m with SNDR higher than 23 dB for 64 QAM modulation capability. By scaling down the TX array size to 256 elements, the communication distance is 200 m.

In the internet communication scenario, the up link usually occupies less resources than the down link due to the majority of the users are enjoying multi-media from the internet. The bandwidth of the down link and the uplink are usually unequal, one reason is the above stated that users are downloading more information than they uploading. Another is that the down link from base station are sending the data to a group of users, which data are orthogonal frequency-division multiplexing (OFDM) modulated to separate the different users in different sub-channel. In this case, the base station output signal is wideband. By contrast, the up link is the link from user equipment to base station, the user equipment is infeasible to implement very large array such as 2014 elements array. Therefore, the up link transmitted signal EIRP is much lower than the down link. To

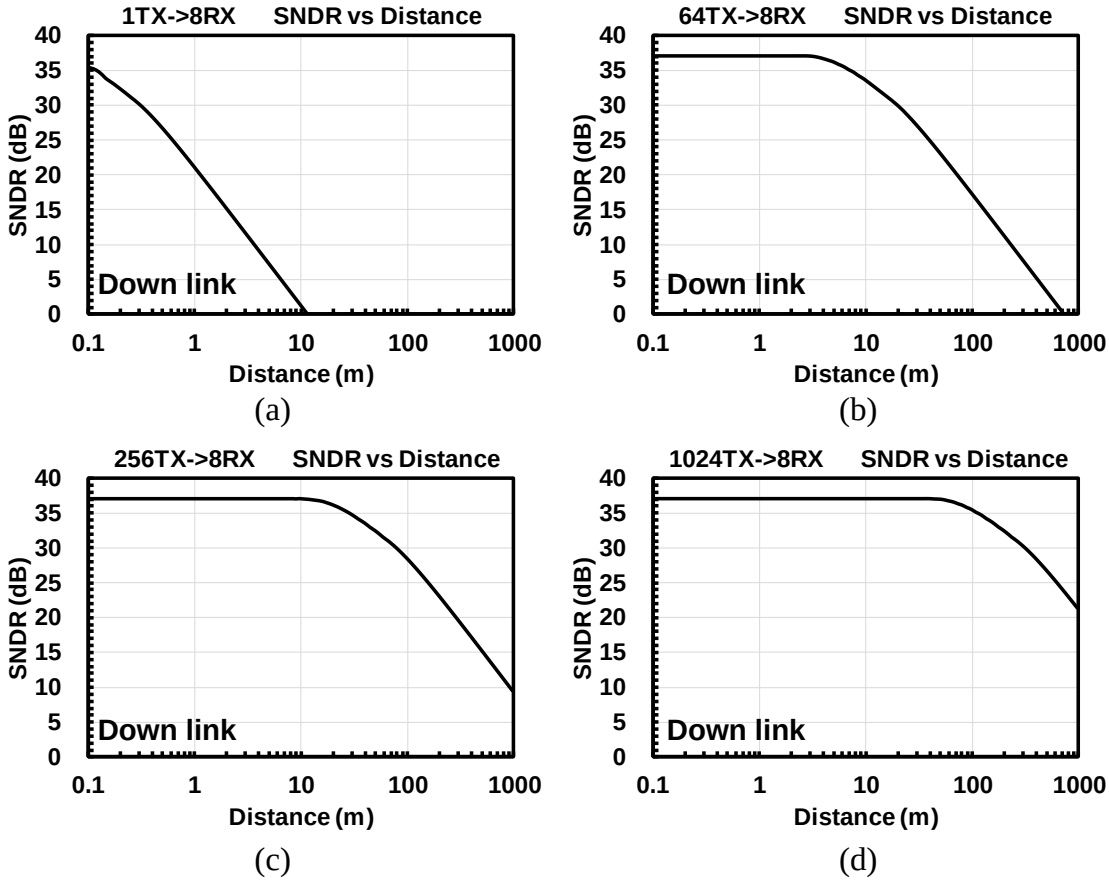
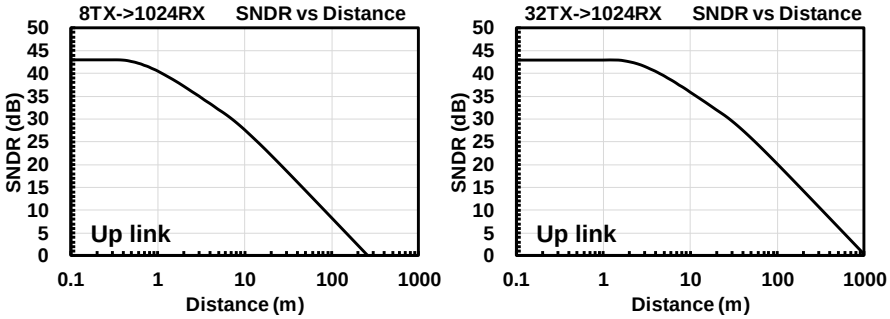


Figure 4.12: 800MHz BW phased-array transceiver down link calculated SNDR vs communication distance (a) 1TX to 8RX, (b) 64TX to 8RX, (c) 256TX to 8RX, (d) 1024TX to 8RX.



(a) (b)

Figure 4.13: 100MHz BW phased-array transceiver up link calculated SNDR vs communication distance (a) 8TX to 1024RX, (b) 32TX to 1024RX.

maintain the same communication distance for down link and up link, the up link signal bandwidth is reduced to 100 MHz. With the reduced signal bandwidth, the maximum achievable SNDR is increased due to the lower system noise floor. In a practical user equipment such as a mobile phone, the largest array size is assumed as 32. Figure 4.13 shows the phased-array transceiver up link calculated SNDR as a function of distance d with signal bandwidth of 100 MHz. Differs from the modulation scheme used in the down link, the up link employs simpler modulation scheme such as 16 QAM and QPSK for long distance wireless. Figure 2.18 shows the system required SNR for various modulation schemes. System SNR > 10 dB and SNR > 16 dB can be regarded as capable of QPSK and 16 QAM. It can be seen that the user equipment with 32 TX array can establish a up link with base station in several hundred meters while maintaining SNDR higher than 10 dB. Assuming QPSK modulation is used, the up link communication distance is 320 m with 32 UE TX array, and the up link communication distance is 80 m with 8 UE TX array.

This section discussed the phased-array transceiver system and circuit design for 5G NR 28 GHz band. The system topology and building blocks circuit schematic are including for detailed discussion. The one channel transmitter and receiver SNDR performance specification is calculated to verify system capability. The practical scenario of base station and user equipment using proposed phased-array transceiver is discussed, both the down link and the up link can establish several hundred miter communication distance. The following section will discussed the implemented transceiver measurement results.

4.2.2 Measurement Results

The proposed 28GHz 4-element phased-array transceiver is fabricated in a standard 65-nm CMOS process. The chip occupies an area of 3mm × 4mm, four sub-array transceivers are placed symmetrically. Table 4.2 denotes the core area breakdown of the key building

Table 4.2: Core area of building blocks.

Blocks	Core Area [mm^2]
PA	0.18
RF Buf. & Mixer	0.16
LO Phase Shifter & Buf.	0.25
LNA	0.24
Multiplier	0.3
LO SW &Buf.	0.27
Logic	0.64

Table 4.3: Power breakdown of each building blocks.

	Blocks	P_{DC} [mW]
TX	PA	179.8
	RF Buf.	31.6
	Mixer	0.6
RX	LNA	30.6
	RF Buf.	19.5
	Mixer	0.7
LO	Multiplier	37.1
	LO Switch & Buf.	28.0
	PPF Buf.	44.4
	LO Phase Shifter	10.3
	2-Stage LO Buf.	16.6

blocks. The sub-array single-element transceiver occupies an area of 1.85 mm^2.

The evaluation PCB board is implemented to characterize the proposed transceiver. The DC power breakdown of each building block is measured at first. Table 4.3 shows the power consumption breakdown of the proposed phased-array transceiver. The measured power consumption in transmitter mode for the whole chip is 1.2W with an output power of 11dBm per path. In receiver mode, the power consumption is 0.59W.

Figure 4.14 shows the measured transceiver characteristics. The small signal characteristics, including conversion gain, noise figure, are measured by using network analyzer Keysight PNA-X E8361A. The large signal measurement is measured by using power meter Keysight E4417A. Figure 4.14 (a) shows the TX conversion gain, the TX has a peak conversion gain of 12 dB. Figure 4.14 (b) shows the TX large signal measurement result at 28 GHz. The one channel achieves a saturated output power of 18 dBm and a P_{1dB} of 15.7 dBm. Figure 4.14 (c) shows the receiver conversion gain, the receiver has a

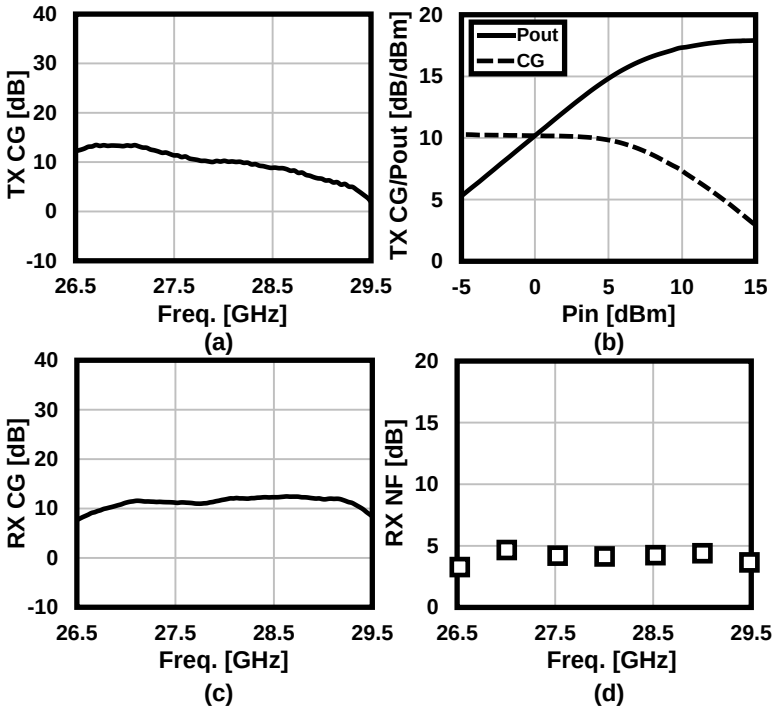


Figure 4.14: Measured transceiver characteristics: (a) transmitter-mode conversion gain, (b) transmitter-mode output power, (c) receiver-mode conversion gain and (d) receiver-mode noise figure.

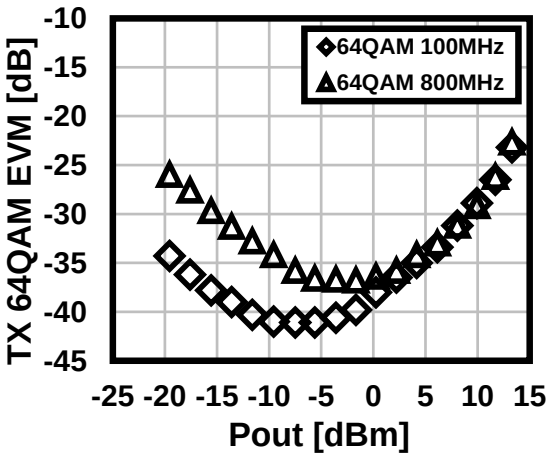


Figure 4.15: One channel TX measured EVM performance.

flat conversion gain of 11 dB over 27 GHz to 29 GHz. Figure 4.14 (d) shows the receiver measured noise figure, the noise figure is measured below 5 dB over 26.5 GHz to 29.5 GHz.

After measuring the small signal and large signal characteristics of the one channel TX and RX, the EVM or SNR performance is evaluated for one cannel TX and RX. The TX EVM is measured by using an arbitrary waveform generator (AWG) as an ideal modulation signal source. The TX transmitted signal EVM is down converted and demodulation

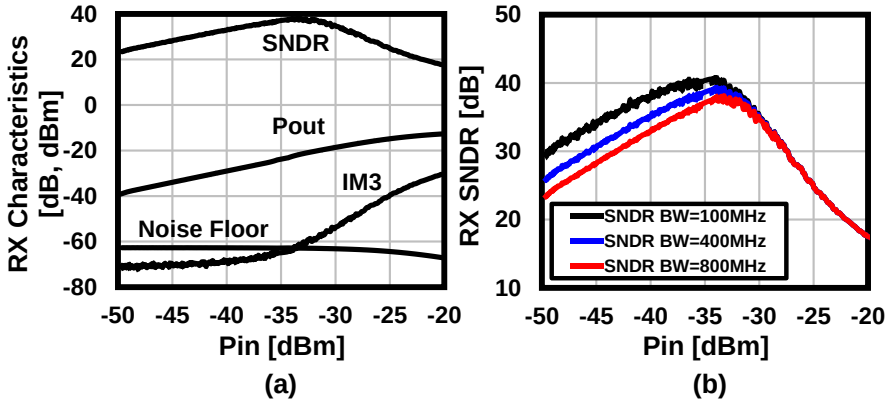


Figure 4.16: One channel RX measured SNDR performance.

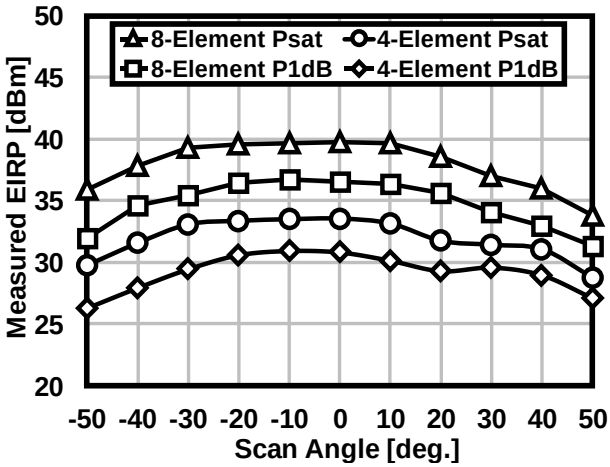
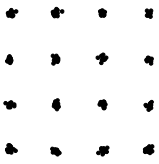
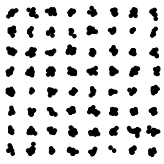
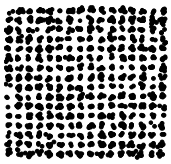


Figure 4.17: Measured TX beam pattern with steering beam angel.

by an oscilloscope. The AWG and oscilloscope are Keysight M8195A and DSO91304A respectively. Figure 4.15 shows the measured TX EVM performance in 64 QAM modulation with 100 MHz and 800 MHz signal bandwidth. The peak EVM is at output power of -2 dBm, which matches the calculation shown in Figure 4.10.

The RX EVM performance is evaluated by calculating its SNDR. The noise floor is measured above, then the remaining measurement is the nonlinearity. Two tone signal are generated by signal generator Keysight E8257D. Figure 4.16 (a) shows measured Pout, IM3, noise floor and calculated SNDR for 800 MHz signal bandwidth. By decreasing the signal bandwidth, the SNDR and sensitivity are improved. For 100 MHz signal bandwidth, the peak SNDR is 40 dB at -36 dBm, which is 4 dB degraded from calculation based on simulation data as shown in Figure 4.11.

After evaluating one channel TX and RX, the phased-array transceiver is connected with antenna for over-the-air (OTA) communication measurement. Two chip, four sub-array transmitters are connected to eight antennas with same length transmission lines. The measured EIRP against the beam scan angle for an 8-element array and a 4-element array are shown in Figure 4.17. The achieved saturated EIRP is 39.8dBm for an 8-element

5m OTA Measurement	Modulation	QPSK	16QAM	64QAM	256QAM
	Data rate	5Gb/s	10Gb/s	15Gb/s	12.8Gb/s
	Beam direction	0°	0°	0°	0°
	Constellation**				
	TX EVM (RMS)**	-28.8dB (3.6%)	-28.7dB (3.7%)	-27.9dB (4.0%)	-30.9dB (2.9%)
	TX-to-RX EVM (RMS)***	-25.5dB (5.3%)	-25.1dB (5.6%)	-25.2dB (5.5%)	-29.3dB (3.4%)

*The roll-off factor is 0.25.
**Constellation, and TX EVM are measured with an external downconverter.
***TX-to-RX EVM(RMS) is measured through TX and RX, which is equivalent to −SNR(MER).

Figure 4.18: Measured EVM performance.

array and 33.6dBm for a 4-element array at 0° scan, respectively. The observed 6dB difference in EIRP matches with the theory. The measured EIRPs at P_{1dB} are 36.5dBm and 30.8dBm for the 8-element array and the 4-element array, respectively.

Figure 4.18 shows the over-the-air (OTA) constellation and performance summary of the proposed 8-element ransceiver module. For measuring the constellation and EVM RMS of the 8-TX, one module operating in TX mode is measured together with a 15-dBi horn antenna and an external down-converter. The carrier frequency is 28GHz in this measurement. The constellations at 0° beam direction are measured in QPSK, 16 QAM, 64 QAM with 2.5 Gsymbol/s and in 256 QAM with 1.6 Gsymbol/s, respectively. One module operates in TX mode and the other operates in RX mode. The distance between two modules is 5m. For 0° beam direction, the measured TX-to-RX EVM RMS is 5.3 %, 5.6 %, 5.5 % and 3.4 % for QPSK, 16 QAM, 64 QAM and 256 QAM, respectively. The data rate of 5 Gb/s for QPSK, 10 Gb/s for 16 QAM, 15 Gb/s for 64 QAM and 12.8 Gb/s for 256 QAM is achieved. 6.4 Gb/s wireless communication in 256 QAM is realized over the whole beam angle of ±50° at 5 m distance.

4.3 Phased-Array Transceiver for 5G NR 39GHz Band

This section introduces a phased-array transceiver for 5G 39 GHz band. The 39 GHz phased-array chip also consists of four sub-array transceiver elements and it is also LO phase shifting architecture. The phased-array transceiver introduced in this section integrates phase and gain detection and calibration block. The power amplifier and LNA is discussed in section 3.4.3. This section includes detailed transceiver architecture, system level diagram in section 4.3.1, and the calibration algorithm in section 4.3.2. The

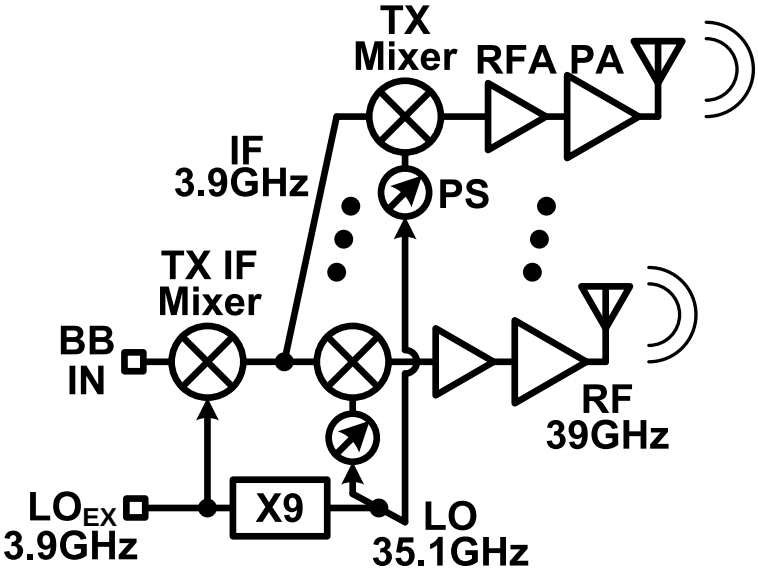


Figure 4.19: Sliding IF 39 GHz phased-array transmitter architecture.

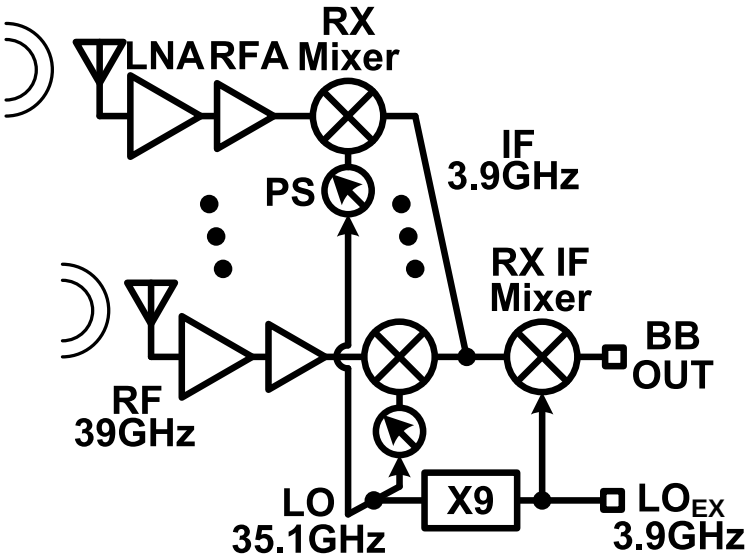


Figure 4.20: Sliding IF 39 GHz phased-array receiver architecture.

measurement results are shown in section 4.3.3.

4.3.1 Transceiver Front-End Design

This section introduces the 39 GHz phased-array transceiver front-end design. It includes the system design, sub-TRX circuit design, LO phase shifter and calculated link level diagram.

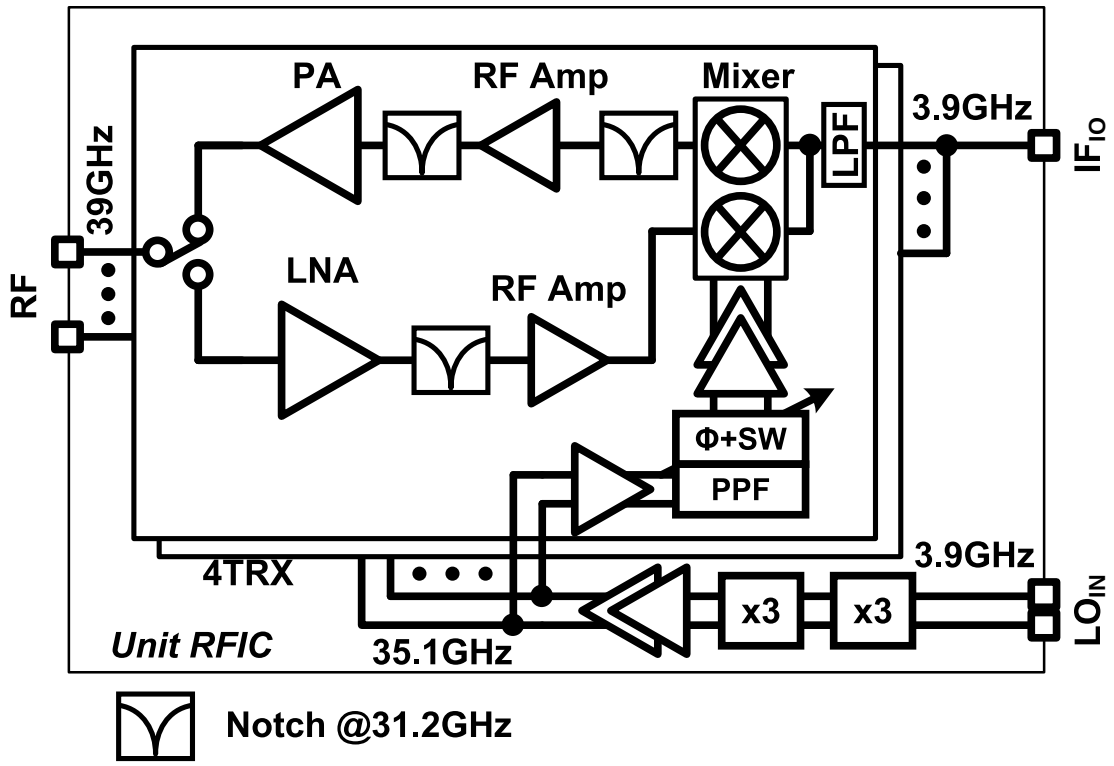


Figure 4.21: 4-element 39 GHz phased-array RF transceiver block diagram.

The 39 GHz transceiver has the same sliding IF architecture as in 28 GHz transceiver introduced in above section. The sliding IF architecture requires less number of LO generation circuits. The sliding IF 39 GHz phased-array transmitter architecture is shown in Figure 4.19, the baseband signal (BB) frequency is at DC, the external LO (LO_{EX}) and intermediate frequency (IF) is at 3.9 GHz, the radio frequency (RF) is then at 39 GHz. The sliding IF architecture with a frequency multiplier or a frequency divider can share one frequency generator in the IF stage and the RF stage. In this design, the IF and LO_{EX} frequency are chosen at 3.9 GHz. To set the RF frequency at 39 GHz, the ×9 LO multiplier is required. Figure 4.20 shows the sliding IF phased-array receiver architecture. The same with transmitter architecture, the sliding IF receiver has RF at 39 GHz, IF and LO_{EX} at 3.9 GHz with a ×9 LO multiplier.

Figure 4.21 shows the detailed block diagram of the 39 GHz RF transceiver. The IF signal is not integrated monolithically, an external IF circuit is used in the 39 GHz wireless system. The RF transceiver consists of sub-array transmitter, receiver and LO chain. The LO chain includes frequency multiplier, poly-phase-filter (PPF) and phase shifter. The RF interfaces are single-ended for PA RF output and LNA RF input due to simple connection with antenna. The IF port of TX and RX are combined to save the area and make

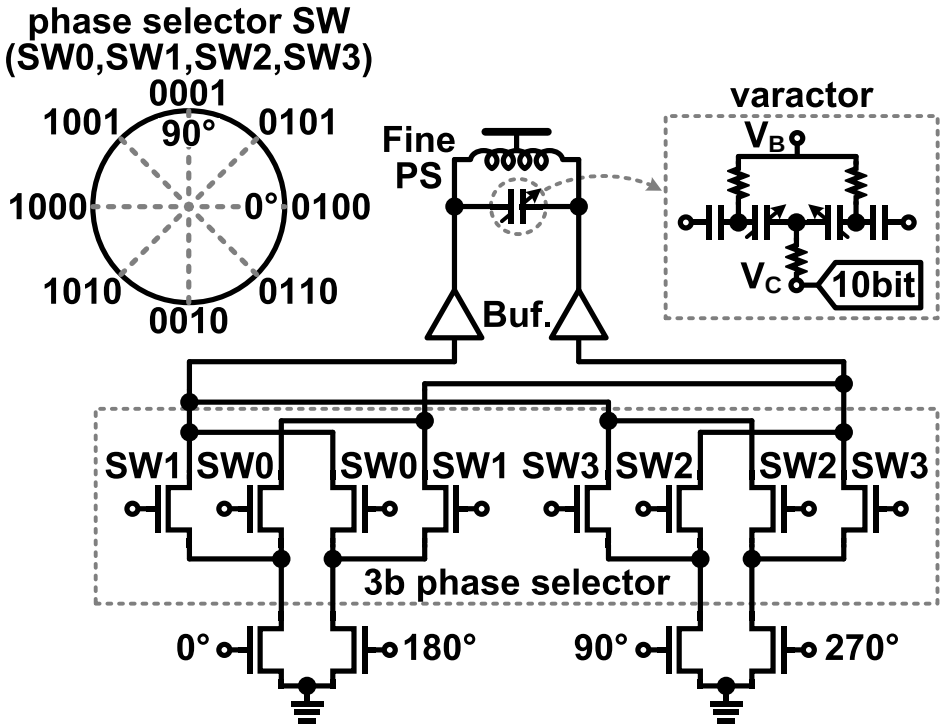


Figure 4.22: Circuit schematic and phase mapping of phase selector and phase shifter.

the layout simpler. Passive mixer is used for both up-conversion and down-conversion. Instead of sharing mixer RF port for transmitter and receiver, a pseudo-single-balanced mixer is proposed in this work. A low-pass-filter is added at the IF port of the mixer in each sub-array TRX. The LPF is added to enhance the LO isolation between each sub-array transceivers. Two notch filters are added in the transmitter to filter the RF image signal, which may be a big interference signal for other wireless devices operating at 31 GHz.

The LO chain plays the same role as in the 28 GHz transceiver. In stead of increase LO_{EX} and IF frequency, a simpler way is to increase the multiplication frequency from 6 to 9. The ×9 multiplier consists of two stage of ×3 multipliers, which has been presented in section 4.2.1. The poly-phase filter is RC based to convert the differential signal to be quadrature.

Figure 4.22 shows the detailed circuit schematic and phase mapping of phase selector and phase shifter. The phase selector in 39 GHz transceiver has 3-bit resolution, the 2-bit basic phase selection is 0°, 90°, 180°, and 270°. The additional phase selection sums two phases to produce the 45° resolution step. Compared with the 90° quadrant phase selector, the proposed phase selector has a smaller phase step. Therefore, the fine phase shifter can be designed with a relaxed phase coverage, which improves the gain consistency over the

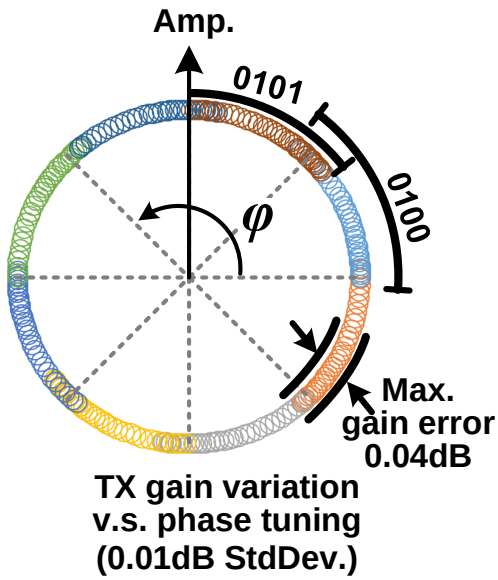


Figure 4.23: Measured phase map and gain variance over full tuning range.

varactor tuning range. With the benefits of the small step phase selector, the switch capacitor bank is removed and only a 10-bit DAC controlled varactor is used for fine phase tuning. The fine phase tuning step is 0.05°. As shown in Figure 4.23, the transceiver has a measured maximum gain variation of 0.04 dB, the other detailed measurement result will be shown in section 4.3.3.

The pseudo-single-balanced mixer used in the 39 GHz transceiver is shown in Figure 4.24. The pseudo-single-balanced mixer works in two modes, one is the up-conversion mode, one is the down-conversion mode. On up-conversion mode, the mixer combines the signal path (LO+) and a dummy path (LO-) for the TX. The LOFT can be further reduced by adjusting the bias voltage at the LO port, IF port, and dummy IF port. In addition, the proposed mixer mitigates the issue of LO leakage to IF path, which causes LO phase shifters affecting on each other when tuning the phase. The mitigation of the LO leakage to IF path is realized by summing the LO signal in opposite phase. An R-C low-pass filter (LPF) at the mixer IF port is added to further enhance the LO isolation. Therefore, on both the up-conversion mode and the down-conversion mode, the mixer transistors are turned on. The measured phase variation of one TX path at different phase control code shows a maximum standard deviation of 0.5°. The phase variation is measured by sweeping the phase of other TXs over 360°.

The PA/LNA with antenna switch is reuses the same circuit introduced in section 3.4.3. On PA mode, the PA has a small signal gain of 14.7 dB, a P_{SAT} of 15.5dBm, P_{1dB} of 13.5dBm, and peak PAE of 25.5% at 39 GHz. On LNA mode, the LNA provides a small signal gain of 33 dB and has a noise figure of 7.0 dB at 39 GHz.

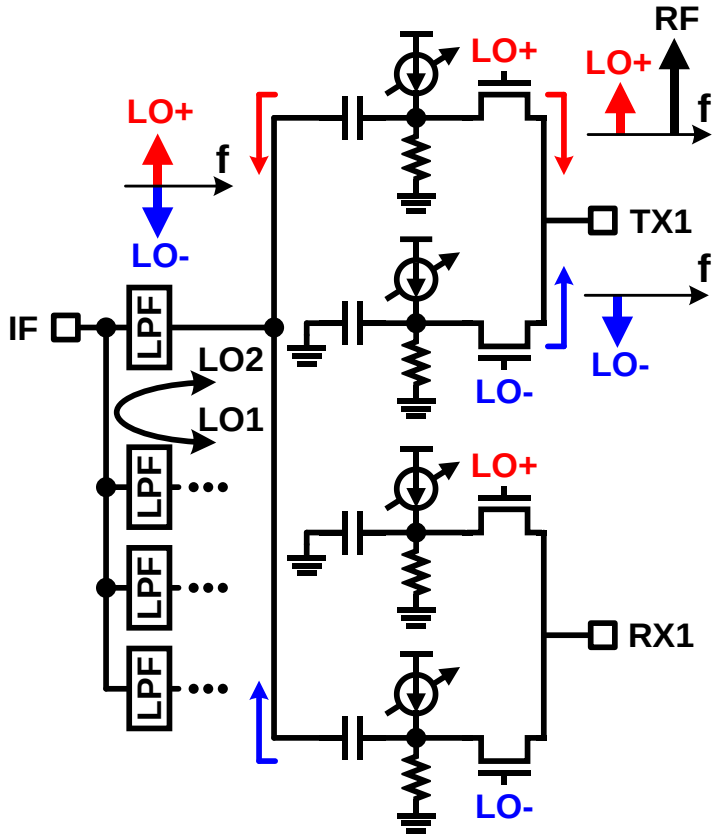


Figure 4.24: Circuit schematic of the pseudo single-balanced mixer.

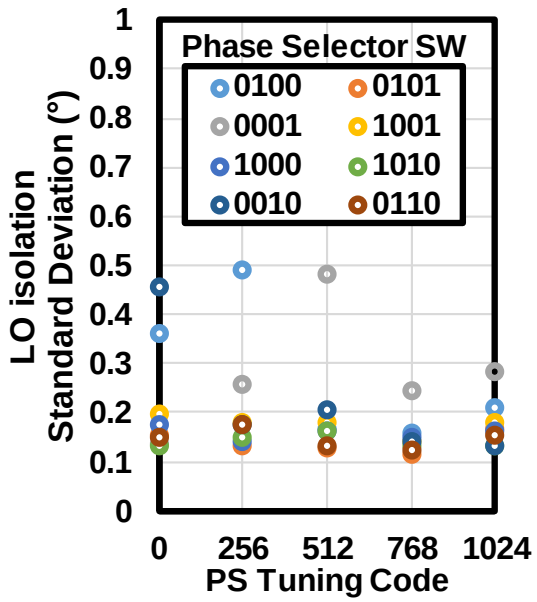


Figure 4.25: Measured LO isolation.

The design specifications of each blocks in the 4-element phased-array transceiver are listed in table 4.4. Due to the single-ended architecture, the system overall linearity is

degraded. The TX and RX link budget are designed carefully to keep high system SNR.

Figure 4.26 and Figure 4.27 show the calculated one channel TX and RX SNDR in respect with RF power. For one channel TX with 1400 MHz signal bandwidth, the maximum achievable SNDR is 40.5 dB at -3 dBm TX output power. As discussed in Figure 2.18, the SNDR > 26dB is regarded as requirements of TX or RX which is capable of 64 QAM modulation with a BER of 10^{-3}. It can be seen that the TX has 25 dB dynamic range of SNDR > 26 dB. For one channel RX with 1400 MHz signal bandwidth, the sensitivity of RX with SNDR > 26 dB is -49 dBm. The RX peak SNDR is 32.2 dB with input power at -41 dBm.

The phased-array transceiver down link and up link are calculated based on one channel characteristics. Figure 4.28 shows the phased-array transceiver down link calculated SNDR as a function of distance d with signal bandwidth of 1400 MHz. Different array scales are used in the calculation. By using 1024 TX elements in base station and 8 elements in user equipment, the longest communication distance is 800 m with SNDR higher than 23 dB for 64 QAM modulation capability. By scaling down the TX array size to 256 elements, the communication distance is 200 m.

Figure 4.29 shows the phased-array transceiver up link calculated SNDR as a function

Table 4.4: Characteristics of each building blocks on simulation.

TX	Gian [dB]	Noise figure [dB]	OIP3 [dBm]
IF Div.	-10	10	∞
RF Mixer	-17	17	-3.4
RF amp.	16	5.7	10.8
PA	15	8	21
TX Cumulative	4	32.8	19.1

RX	Gian [dB]	Noise figure [dB]	IIP3 [dBm]
LNA	20	6.9	-14
RF amp.	8	9	2
RF Mixer	-17	17	9
IF combine	-10	10	∞
RX Cumulative	1	7.6	-21.2

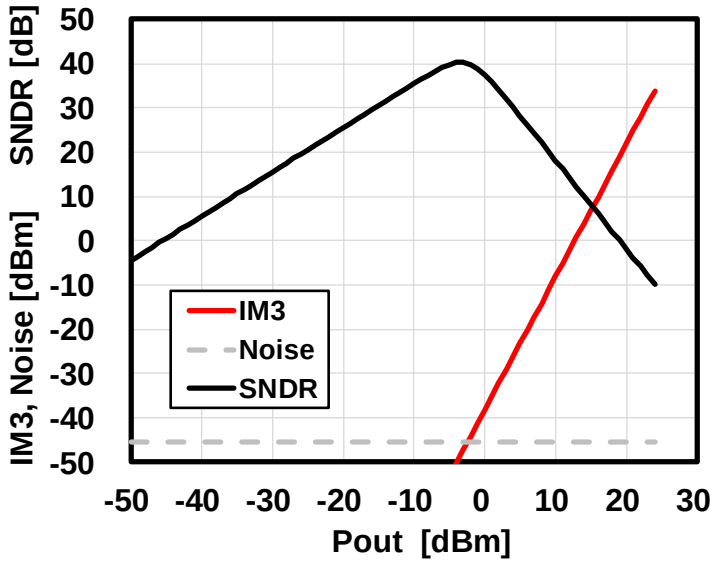


Figure 4.26: TX one channel 1400MHz BW calculated SNDR vs TX output power.

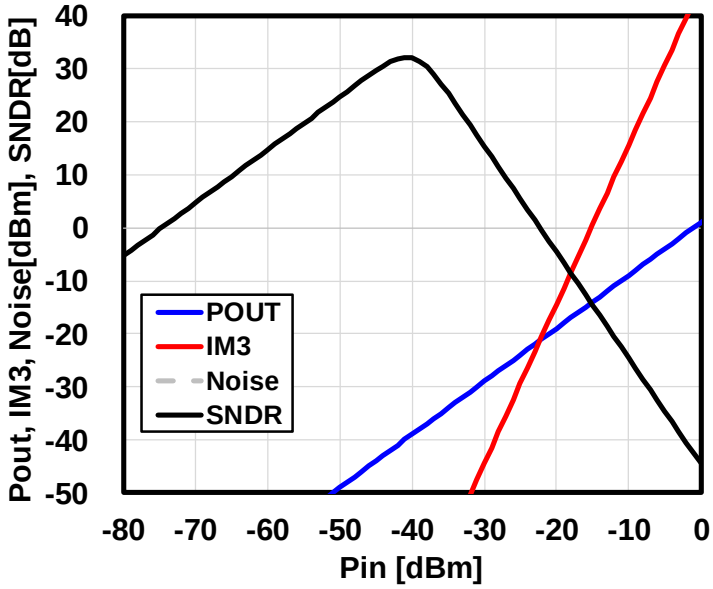


Figure 4.27: RX one channel 1400MHz BW calculated SNDR vs RX input power.

of distance d with signal bandwidth of 100 MHz. Differs from the modulation scheme used in the down link, the up link employs simpler modulation scheme such as 16 QAM and QPSK for long distance wireless. Figure 2.18 shows the system required SNR for various modulation schemes. System SNR > 10 dB and SNR > 16 dB can be regarded as capable of QPSK and 16 QAM. It can be seen that the user equipment with 32 TX array can establish a up link with base station over 50 meters while maintaining SNDR higher than 10 dB. Assuming QPSK modulation is used, the up link communication distance is

200 m with 32 UE TX array, and the up link communication distance is 50 m with 8 UE TX array.

This section discussed the phased-array transceiver system and circuit design for 5G NR 39 GHz band. The system topology and building blocks circuit schematic are including for detailed discussion. The one channel transmitter and receiver SNDR performance specification is calculated to verify system capability. The practical scenario of base station and user equipment using proposed phased-array transceiver is discussed, both the down link and the up link can establish several hundred miter communication distance. The following section will discussed the proposed gain and phase calibration mechanism and transceiver measurement results.

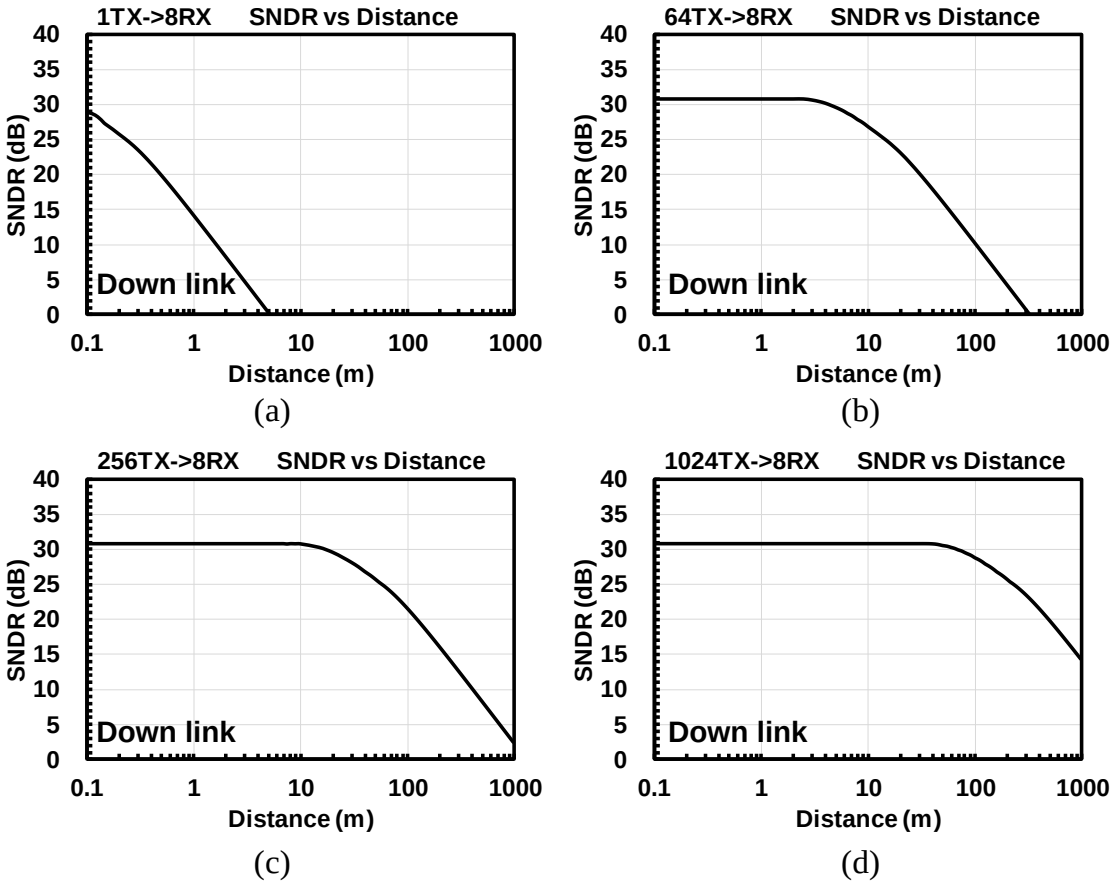
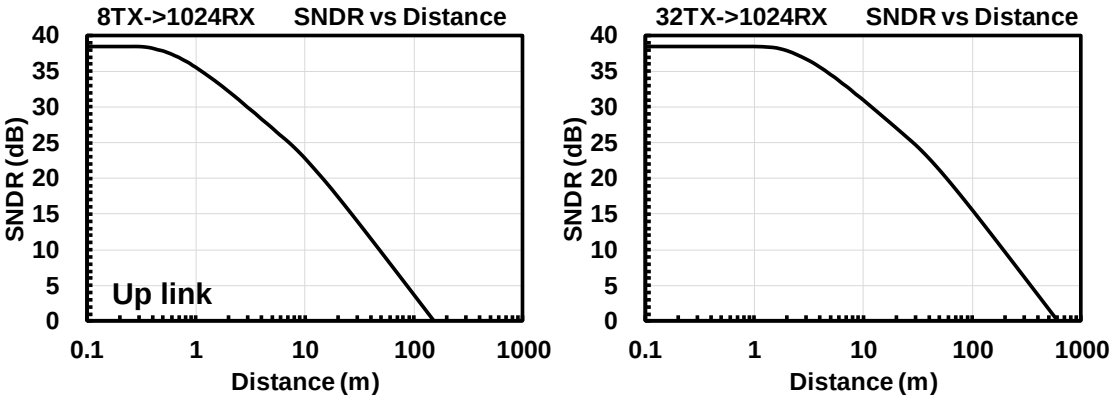


Figure 4.28: 1400MHz BW 39 GHz phased-array transceiver down link calculated SNDR vs communication distance (a) 1TX to 8RX, (b) 64TX to 8RX, (c) 256TX to 8RX, (d) 1024TX to 8RX.



(a) (b)

Figure 4.29: 100MHz BW 39 GHz phased-array transceiver up link calculated SNDR vs communication distance (a) 8TX to 1024RX, (b) 32TX to 1024RX.

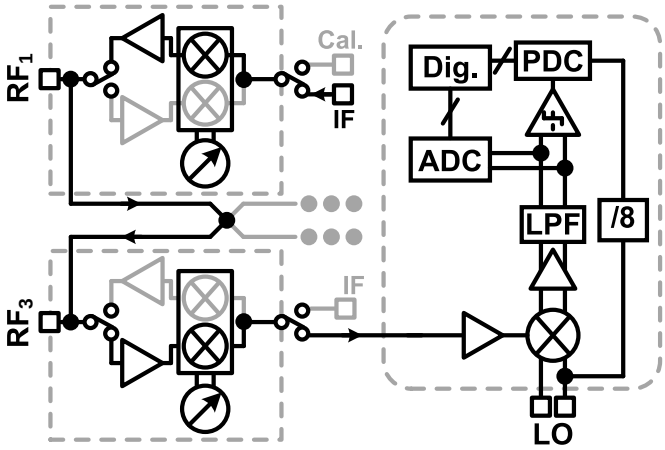


Figure 4.30: Simplified phase gain calibration method.

4.3.2 Calibration Algorithm

The proposed 39 GHz phased-array transceiver integrates phase gain calibration monolithically. The simplified calibration idea is illustrated in Figure 4.30. Directly calibrate the RF signal gain phase information are researched in [58, 59], however, these methods cannot calibrate both TX and RX simultaneously. In addition, the conventional methods quantize phase gain information using ADC, which lacks the quantization accuracy especially for phase. The proposed method for phase gain calibration operates as follow. First, turn on a TX and a RX in two different sub-array transceiver. Second, the IF signal used for calibration is up-converted to RF at the TX side, The RF_1 carries the TX1 phase gain information. Third step is connecting the RF_1 with RF_3, RX3 will down-convert the RF_3 to IF, which carries the RX3 phase gain information. Therefore, the RX3 down-converted IF signal contains both TX1 and RX3 phase gain information. The final step is to quantize the the down-converted IF signal at low frequency. Thanks to the sliding IF architecture,

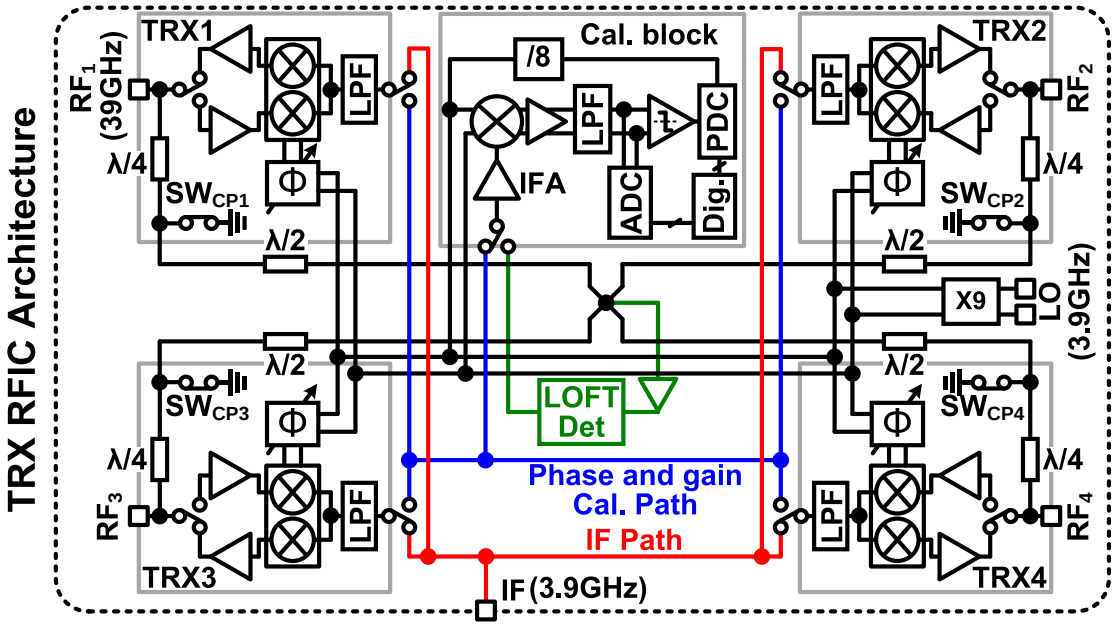


Figure 4.31: Transceiver block diagram with built-in calibration.

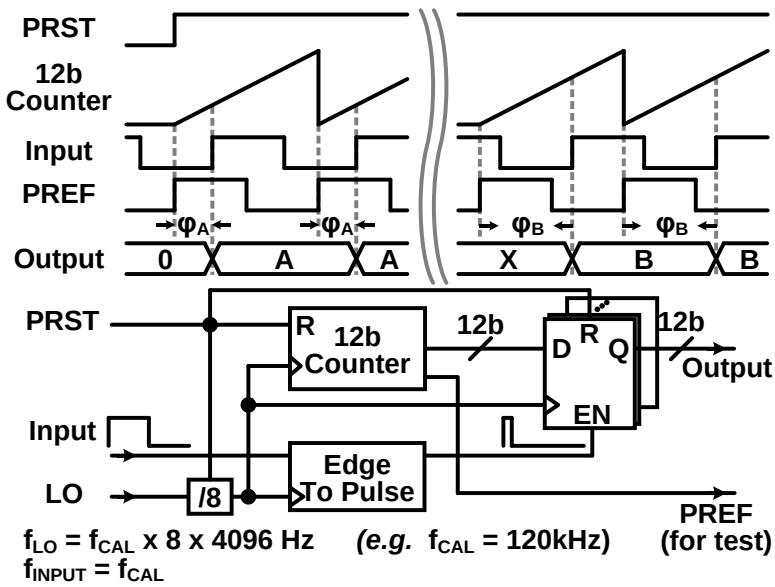


Figure 4.32: PDC timing diagram.

the IF and LO are with the same frequency, so that the IF can be further down-converted to DC. However, the DC signal usually suffers from DC-offset issue, so in this design, a very low frequency offset is used. The gain information is quantized by ADC and the phase information is quantized by phase-to-digital convertor (PDC). For calibrating the each sub-array TXs, one of the RX is used. Due to the same RX, each TX can be calibrated with same gain and same phase difference. And for calibrating RX, vice versa.

The full transceiver block diagram with calibration blocks and signal path is shown

in Figure 4.31. The transceiver consists of four sub-array transceiver. The transceiver IF signal and calibration path are separated with switch, the red line denotes the IF path on TX mode or TX mode. The blue line denotes the phase gain calibration path, which is connected to sub-array RX by switch. All the sub-array TRXs are connected through transmission line symmetrically, which guarantee the path loss and phase shifting between each RF node are the same. A quarter-wave ($\lambda/4$) transmission line with switch is added in the RF calibration path. On the TRX mode, the calibration block is off, the quarter-wave transmission line switches are connect to ground to provide high impedance at the RF node see to the calibration path. At the center cross point of the RF calibration path, an square-law detector is added to detect LO feed through (LOFT) leaked from each TX.

In calibration block, a 12-bit phase-to-digital converter (PDC) will quantize the phase value. Figure 4.32 shows the PDC timing diagram, the phase input signal is quantized by a 12-bit counter, which results in a qantization resolution of 0.09°. The proposed on-chip phase quantization technique achieves a very high resolution at millimeter-wave frequency, and it is 30 times improved compared with the analog solution in [58,60]. The detailed phase gain LOFT calibration procedure and measurement is introduced below.

Figure 4.33 (a) shows the detailed phase gain calibration mechanism. The f_{IF} and f_{LO} has a small frequency offset f_{CAL}, which is the signal frequency in calibration block. Figure 4.33 (b) shows the phase gain quantization procedure. In the first loop, the PDC mode is enabled and phase shifter is tuning 360° to map the real phase with the phase control code. The second loop is to quantize the amplitude in ADC mode, the amplitude variation while phase tuning is quantized and saved to register. The quantized phase and amplitude map is shown in Figure 4.23. The phase quantization error is measured by comparing the PDC phase readout value with the external oscilloscope readout value. The measured phase quantization error is shown in Figure 4.33 (c). The RMS phase quantization error is 0.08° in the phase shifter full tuning range.

The LOFT issue in the sliding IF TX architecture will create a interference signal at the LO frequency, which should be eliminated. The proposed transceiver detects the LOFT signal at the RF output node and eliminates it by automatic tuning the mixer DC-offset level. Figurefig:trx:ch4f39 (a) shows the LOFT calibration mechanism. The proposed LOFT calibration circuit has the same IF input signal with phase gain calibration mode. The IF input has a low offset frequency with LO as denited in Figure 4.34 (a). The up-converted RF signal is then $f_{\mathrm{RF}} = 9 * f_{\mathrm{LO}} + f_{\mathrm{CAL}}$, and the LOFT frequency is $f_{\mathrm{LOFT}} = 9 * f_{\mathrm{LO}}$. The RF and LOFT consist a two-tone signal at the RF node. The sub-array TXs are turned on and calibrated by order. The two-tone signal is amplified and detected by a square-law detector. The square-law detector output frequency is $f_{\mathrm{LOFTDET}} = f_{\mathrm{LO}} + f_{\mathrm{CAL}}$. The ADC

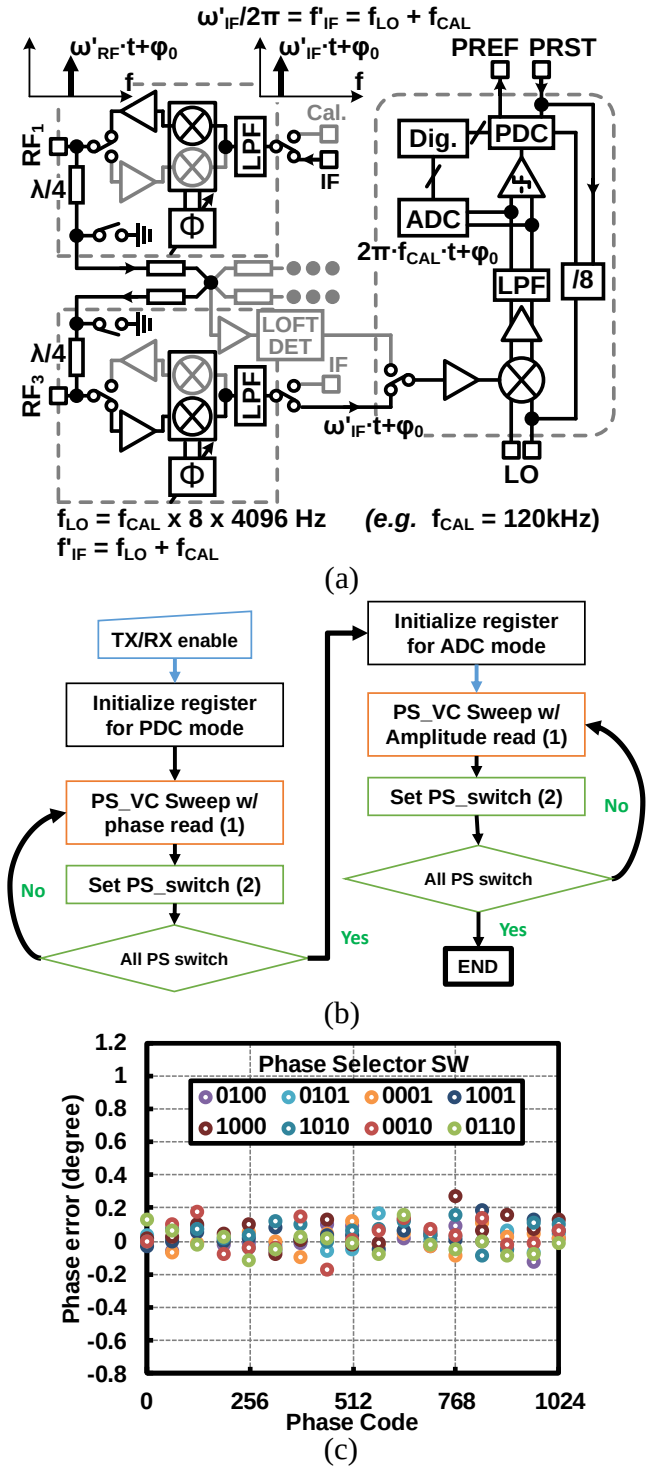


Figure 4.33: (a) Phase gain calibration mechanism, (b) quantization procedure, (c) phase quantization accuracy.

in calibration block is used to quantize the LOFT detected signal amplitude. Figure 4.34 (b) shows the LOFT calibration procedure. The TXs are calibrated one by one, the mix-

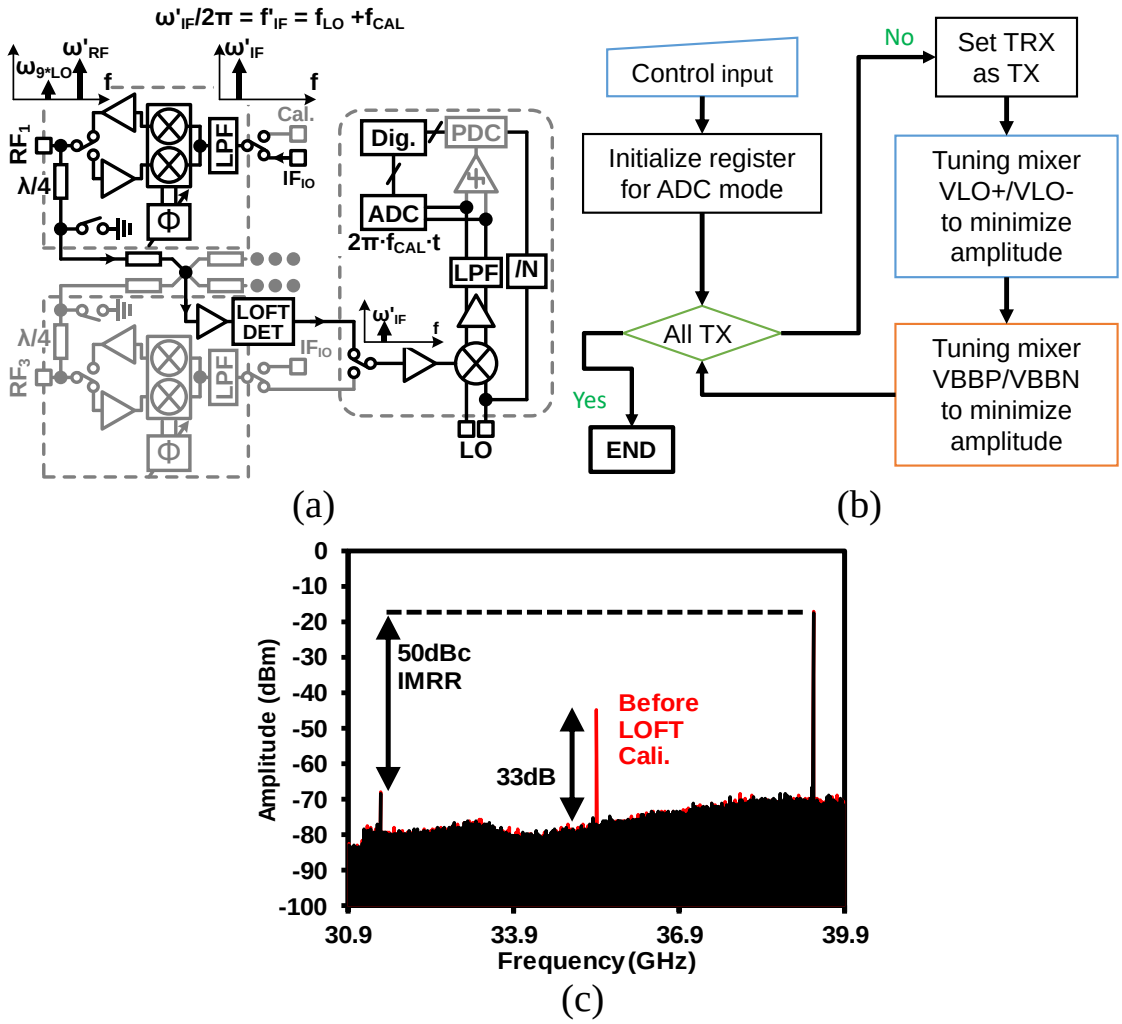


Figure 4.34: (a) LOFT calibration mechanism, (b) calibration procedure, (c) auto-calibration result.

er biases are fully tuned to find the minimum amplitude, which represents the minimum LOFT. Figure 4.34 (c) shows the measured auto-calibrated LOFT results. The measurement shows a -70 dBm LOFT cancellation and a 50 dBc image signal suppression.

4.3.3 Measurement Results

The proposed 39 GHz 4-element phased-array transceiver is fabricated in a standard 65-nm CMOS process. Figure 4.35 shows the die micrograph of the chip. The chip occupies an area of 3mm × 4mm, four sub-array transceivers are placed symmetrically. Figure 4.36 shows the implemented 39 GHz phased-array transceiver module. Each transceiver PCB module has four chips 16 antenna elements, as shown in the front view, the LO signal input is at the upper side of chips and the IF signal is at the bottom side of the chips.

Table 4.5: Power breakdown of 39 GHz transceiver building blocks per chip.

Blocks	P_{DC} [mW]
PA	650
RFAMP	390
LNA	130
X9 multiplier	140
Phase shifter	240
Cal. Blocks	30
LOFT det.	50
SPI	30

The LO and IF are connected to chips with Wilkinson power divider. The transceiver one channel RF front-end characteristic is measured at first. Figure 4.37 shows the measured the one-path TX EVM performance evaluated using 5G NR 400MHz bandwidth MC-S10/19/27 modulated signal (OFDMA). The TX 5G NR OFDMA IQ modulation signal is up-converted to IF by Keysight signal generator (E8267D) with vector modulation at 3.9 GHz. The RF output signal is down-converted by an external mixer and demodulat-

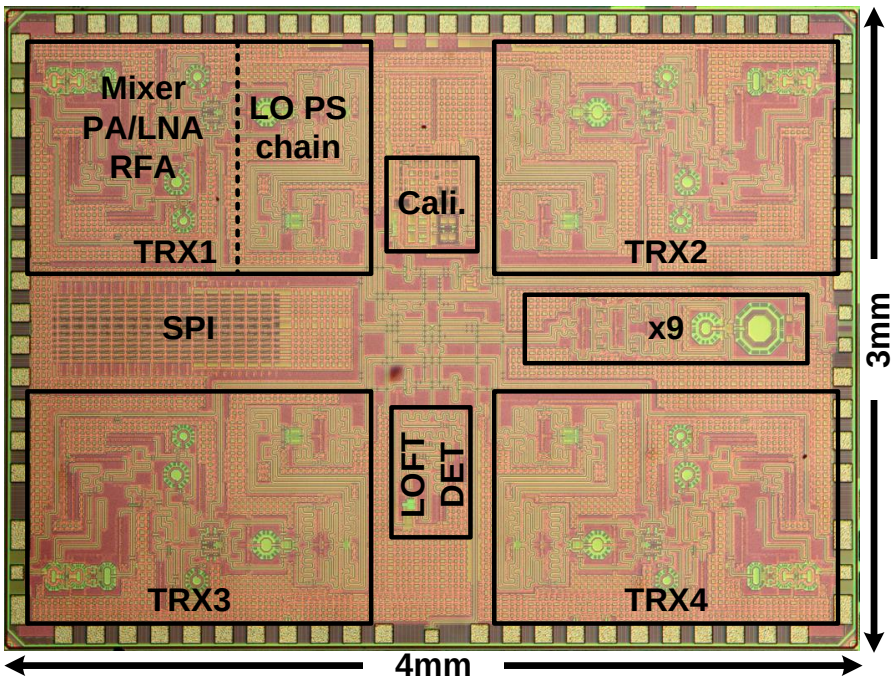


Figure 4.35: Chip micrograph of 39 GHz 4-element phased-array transceiver.

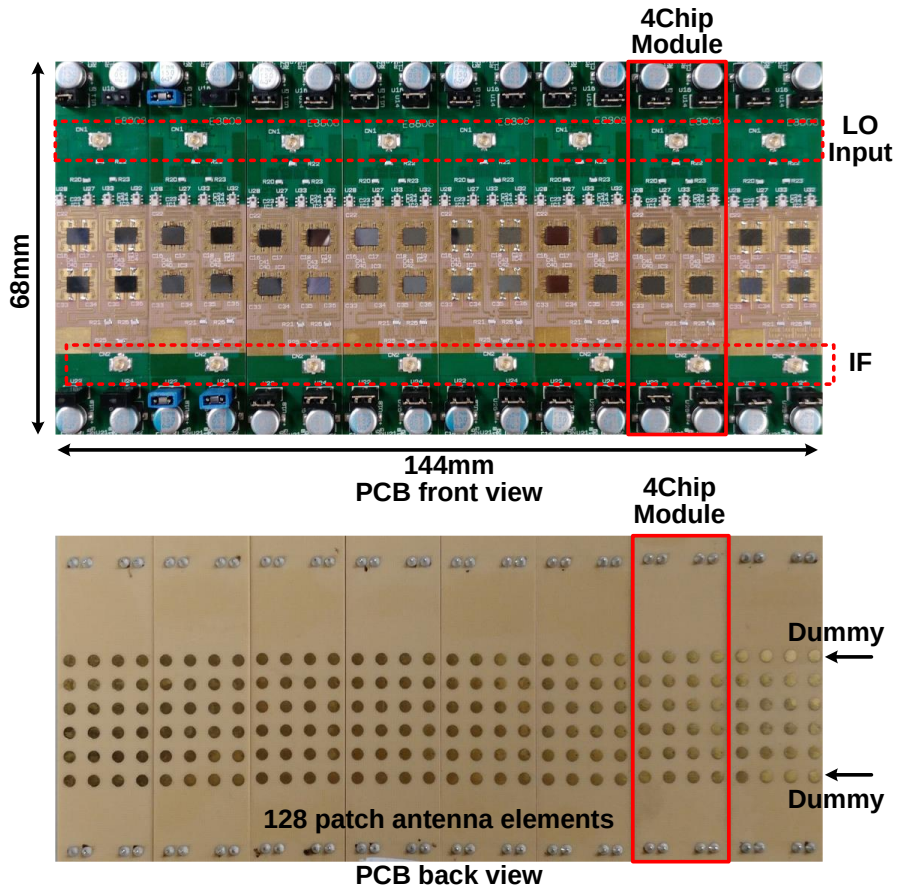


Figure 4.36: The 39GHz phased-array transceiver module.

ed by keysight digitizer (M9703B). After de-embedding LO and image signal, the TX achieves an average output power of 3.6dBm at -24.6dB EVM while transmitting MCS19 64QAM modulation signal. Figure 4.38 shows the calculated one channel RX SNDR performance. The RX achieves a peak SNDR of 40dB. The RX SNDR with 400MHz signal bandwidth is calculated from the measured RX gain, IM3 and noise figure. The transceiver module with 128-element (4x32) patch antenna is implemented as shown in Figure 4.36. The maximum EIRP is measured by driving the TX element to maximum gain and output power. A receiver horn antenna is used to receiver emitted RF signal and a power meter is used to observe the received signal strength. A number of TX elements are used from 4TX to 32TX. The measured maximum EIRP is 46 dBm for a 32-element (4×8) TX. With the doubled TX elements, the EIRP shows good compliance with theoretically calculated 6 dB step. The maximum EIRP has a good match with the TX P_{SAT} and the antenna elements.

The radiation pattern of 1x4 TX array with and without calibration is measured at 0-degree and 20-degree beam steering angle. As shown in Figure 4.40, at 20-degree an-

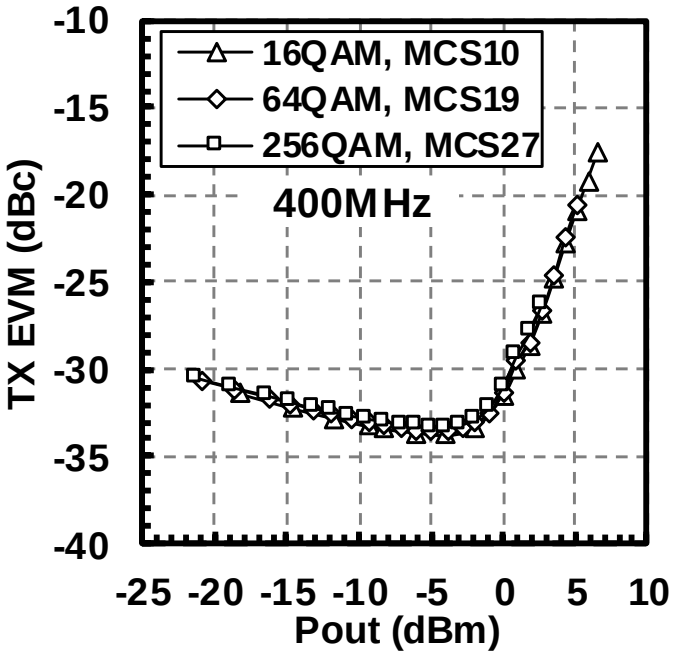


Figure 4.37: Evaluated one channel TX EVM performance.

gle, the main lobe strength is 3dB improved after calibration and side lobe is suppressed more than 5dB. After calibration, the radiation pattern with beam steering angle in +/-40-degree is demonstrated.

Figure shows the measured OTA constellation and EVM performance. Both TX and RX utilize 8-element (2×4) array. The TX 5G NR OFDMA IQ modulation signal is up-converted to IF by Keysight signal generator (E8267D) with vector modulation. The RX IF output signal is down-converted by an external mixer and demodulated by keysight digitizer (M9703B). The transceiver is evaluated with 400MHz QPSK, 16QAM, 64QAM and 256QAM modulation signal. At 1m OTA distance and 0-degree beam direction, the measured TX to RX RMS power normalized EVM are -30.7dB, -30.3dB, -30.2dB and -30.0dB in QPSK, 16QAM, 64QAM and 256QAM, respectively. At 20-degree and 40-degree beam direction, the measured EVM are -30.1dB and -28.6dB in 64QAM.

4.4 Performance Summary

Figure 4.6 summarizes the performance summary and shows the comparison table of millimeter-wave phased-array transceivers for 5G and beyond. The proposed LO phase shifting based transceiver chip achieves a measured RMS gain and phase errors of less than 0.04dB and 0.3°, respectively. In the 5-m OTA measurement, the proposed 8-element module reports the constellations with 64QAM and 256QAM. 12.8Gb/s in 256QAM with

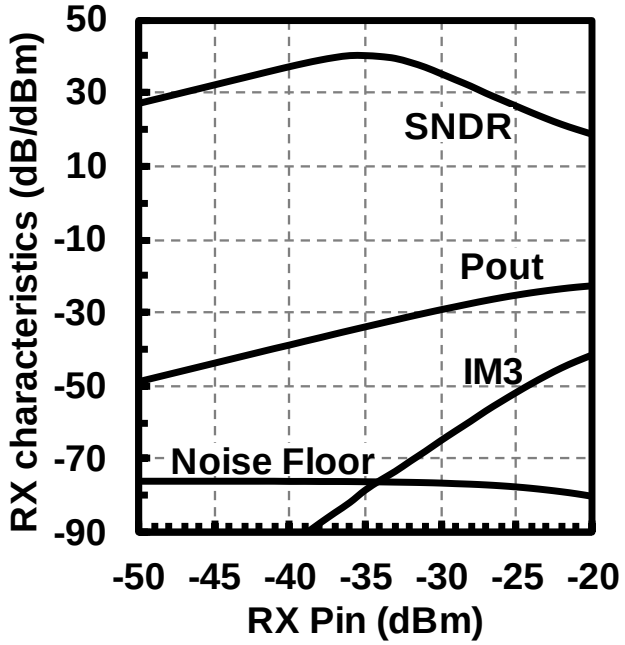


Figure 4.38: Calculated one channel RX SNDR performance.

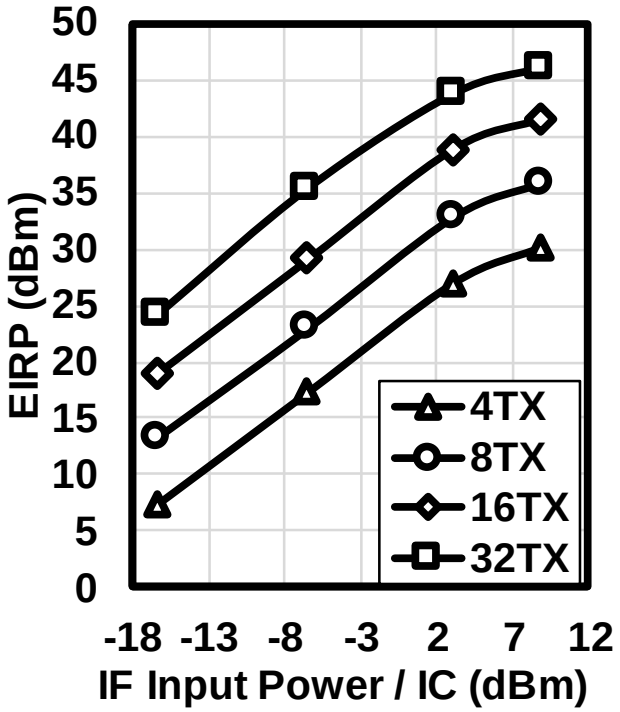


Figure 4.39: Measured EIRP performance up to 32 TX element.

3.4% TX-to-RX EVM RMS is realized at 5m distance. Data rate of 6.4Gb/s in 256QAM can be achieved within the beam angle of ±50°.

The 39 GHz phased-array transceiver demonstrates a 39GHz phased-array transceiver

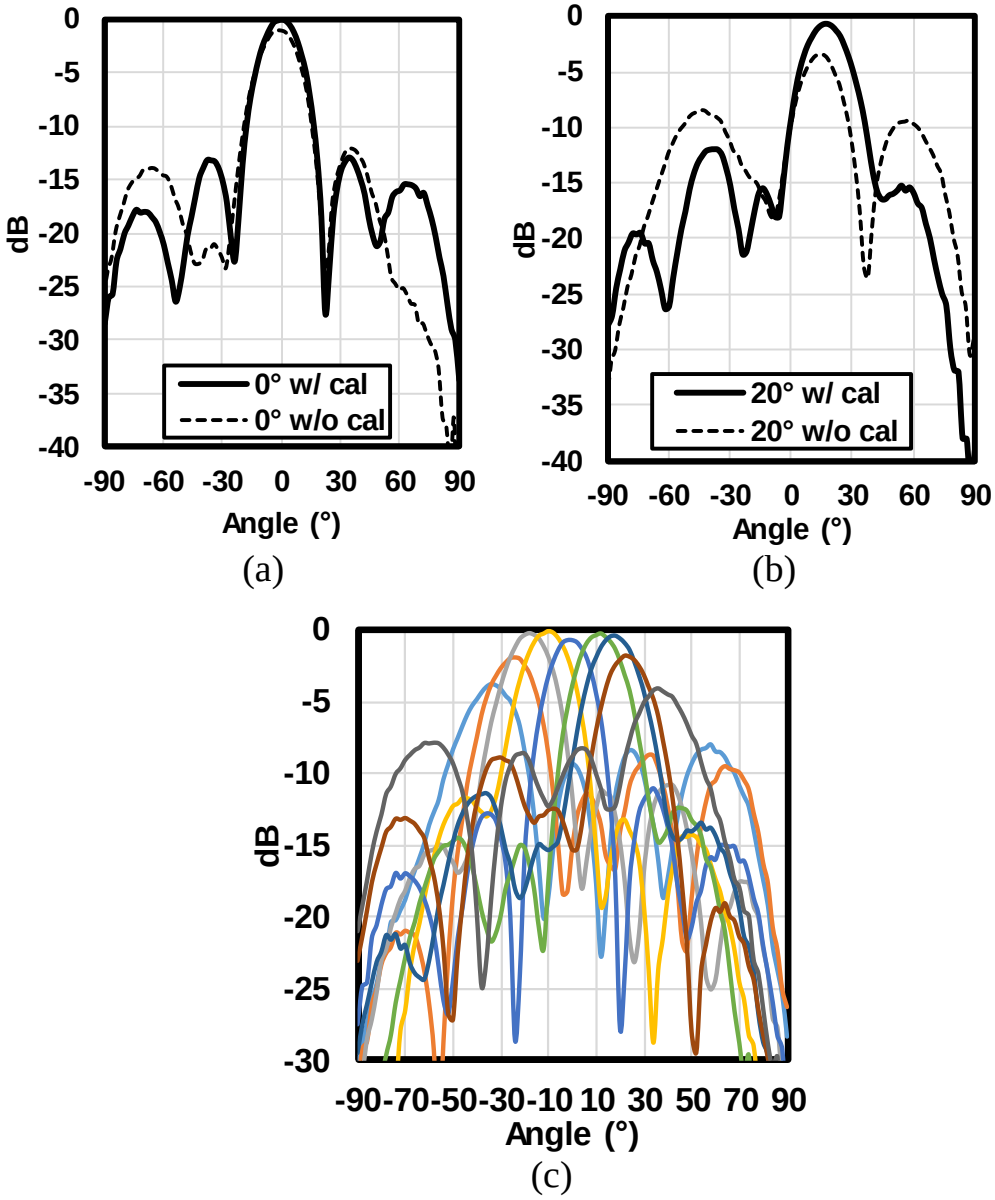
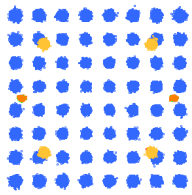
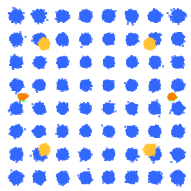
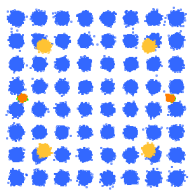
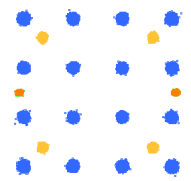
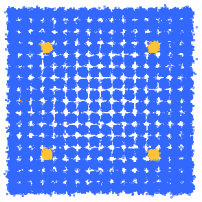


Figure 4.40: Measured beam pattern (a) 0°, (b) 20°, (a) beam steering.

with built-in phase, gain and LOFT calibration, which can ease the deployment of the large array. The on-chip calibration is integrated to calibrate phase gain and LOFT. The RMS phase and gain quantization error are 0.08° and 0.01 dB. A 1-m OTA link is achieved with 5G NR 400MHz bandwidth MCS19 64QAM modulation signal. The LOFT is auto-calibrated to -70dBm, and image signal is 50dBc suppressed.

1m OTA Measurement	Modulation	64QAM MCS19	64QAM MCS19	64QAM MCS19
	BW	400MHz	400MHz	400MHz
	Beam direction	0 °	20 °	40 °
	TX to RX Constellation			
	TX to RX EVM*	-30.2dB	-30.1dB	-28.6dB

1m OTA Measurement	Modulation	QPSK MCS4	16QAM MCS10	256QAM MCS27**
	BW	400MHz	400MHz	400MHz
	Beam direction	0 °	0 °	0 °
	TX to RX Constellation			
	TX to RX EVM*	-30.7dB	-30.3dB	-30.0dB

*RMS power normalized EVM, measured with external down-conversion mixer
**MSCs are defined in Table 5.1.3.1-2 table 2 for PDSCH in 3GPP TS 38.214 V15.1.0

Figure 4.41: Measured OTA performance for 8TX-8RX module.

4.5 Conclusion

The Chapter introduces phased-array transceivers design for 5G NR 28 GHz band and 39 GHz band. Both transceivers show high linearity and high data rate capability. The 28-GHz 4-element phased-array transceiver utilizing a gain-invariant LO phase shifter. 0.1° beam-steering resolution is realized with an 8-element phased-array transceiver. At 5m distance, 6.4Gb/s data-link in 256QAM is achieved over beam angle of ±50° with the maximum data rate of 15Gb/s in 64QAM. The 39 GHz phased-array transceiver with large antenna array integrates on-chip phase gain and LOFT calibration, the calibration has the RMS phase and gain quantization error are 0.08° and 0.01 dB. The LOFT is auto-calibrated to -70dBm, and image signal is 50dBc suppressed. A 1-m OTA link is achieved with 5G NR 400MHz bandwidth MCS19 64QAM modulation signal.

Table 4.6: Performance summary.

	This work 39 GHz	**This work 28 GHz**	[50] Qualcomm	[57] Broadcom
Frequency (GHz)	39 (n260)	28	28	60
Process	65nm CMOS	65nm CMOS	28nm LP CMOS	28/40nm CMOS
Architecture	LOPS	LOPS	RFPS	RFPS
PS resolution	3+10 bit / 0.05º	2+3+10 / 0.04º	3 bit -	6bit / 6º
TX Psat/path (dBm)	15.5	18	14	6.5
Chip power dissipation (W)	1.5 / 4TX 0.5 / 4RX	1.2 / 4TX 0.6 / 4RX	0.36 / 4TX 0.17 / 4RX	8.4 / 144TX 6.6 / 144RX
Chip area (mm^2)	12	12	28	292 (full radio)
calibration	phase, gain, LOFT	N/A	N/A	N/A
Max gain variation (dB)	0.04	0.03 (RMS)	-	1.5
RMS phase error (◦)	0.08	0.28	-	-
TX LOFT (dBm)	< -70	-	-	-
Array size	128	8	24	288
$EIRP_{MAX}$ (dBm)	46 (32 ele.)	39.8	35 (8 ele.)	51
OTA TX to RX EVM (dB)	-30.2 400MHz 64QAM	-35 800MS/s 64QAM	-41 (TX only) 100MHz 64QAM	-24 (TX only) 1150MS/s 16QAM

Chapter 5

Low-Power High-Spectral-Efficiency Transceiver

This chapter presents a 60-GHz transceiver for low-power high-speed short-range wireless using proposed binary-phase on-off keying (BPOOK) modulation scheme. The proposed BPOOK wireless transceiver transmits radio frequency (RF) signal with amplitude modulated on and off by input baseband data, and meanwhile phase is changing between 0° and 180°. The BPOOK transceiver achieves doubled spectral efficiency compared with on-off keying (OOK) modulation and binary-phase-shift keying (BPSK) modulation. It also cancels the intrinsic local-oscillator feed through (LOFT) issue in the OOK modulation. The BPOOK RF signal can be demodulated by employing low-power square-law envelope detector incoherently. The transceiver is fabricated in a standard 65-nm CMOS technology. A data rate of 3.0 Gb/s is achieved while consuming a power of 100 mW from 1-V supply. The incoherent receiver has a sensitivity of -46 dBm. The core area of the transceiver is 1.56 mm^2.

5.1 Millimeter-wave Low-Power Transceiver Considerations

The growing demand for high-speed wireless communication, such as syncing personal cloud, streaming 4K videos, and enabling wireless augmented reality (AR)/ virtual reality (VR) headsets, makes 60-GHz frequency band a great candidate owing to its 9-GHz bandwidth [62–64]. There are several standards defining specification of physical layers (PHY) and media access control layer (MAC) that enables multi-gigabit per second speed wireless communication operating at 60-GHz frequency band. For example, the IEEE 802.11ad standard defines four 2.16-GHz-bandwidth channels at 60-GHz frequency band.

Other technical advancements have been used to enhance the communication speed and distance, including multi-channel bonding [65], phased array beamforming transceivers [66]. However, in addition to high data-rate, the mobile devices also desire lower power consumption, since it leads to higher portability and smaller battery size. Therefore, it makes room for developing a 60-GHz wireless transceiver with characteristics of both high speed and low power.

Recently reported 60-GHz wireless transceivers mainly employ quadrature modulation schemes, such as quadrature phase-shift keying (QPSK) and quadrature amplitude modulation (QAM), due to their high spectral efficiency and channel capacity. High level integrated 60-GHz transceivers employing quadrature modulation scheme with baseband circuity have been demonstrated in [35, 67, 68]. 64-QAM RF transceivers are introduced in [25, 27], which use channel bonding and frequency interleaving to achieve a data rate of 42.24 Gb/s. However, the above 60-GHz transceivers with analog and digital baseband circuitry usually consume a power of over 1000 mW. The on-off-keying (OOK) modulation scheme is widely used in low-power wireless communication system due to its simplicity of RF signal modulation and demodulation [69, 70]. OOK transceiver requires no analog-to-digital converters (ADC) and digital-to-analog converters (DAC) in baseband circuity design, which makes the system achieve lower power consumption. Integrated 60-GHz OOK transceivers have been demonstrated in [20, 71], the overall power consumption is controlled within 300 mW. However, the OOK modulation spectral efficiency is only half of QPSK, which leads to lower communication speed in a limited bandwidth. In addition, OOK transceiver suffers from intrinsic local-oscillator feed through (LOFT), which shares half of total transmission power. OOK spectrum with LOFT can hardly comply with the transmission spectrum mask.

In this chapter, a low-power spectrum efficient LOFT-free 60-GHz CMOS transceiver is presented. A binary-phase on-off keying (BPOOK) modulation scheme is proposed to eliminate the LOFT issue in OOK spectrum and to double the spectrum efficiency than that of the OOK modulation [72]. Fabricated in a 65-nm CMOS process, the transceiver achieves 3.0 Gb/s data rate, and the spectrum occupies a bandwidth of 3 GHz. The transceiver consumes 78 mW while transmitting, and 22 mW while receiving, from a 1-V supply. The core area of the transceiver is 1.56 mm2.

5.2 Proposed BPOOK Modulation

In order to realize a system with low power consumption and improved spectrum efficiency, this paper starts with the OOK modulation scheme, since the OOK has the simplest structure among the digital modulation schemes. Fig. 5.1 shows the conceptual OOK

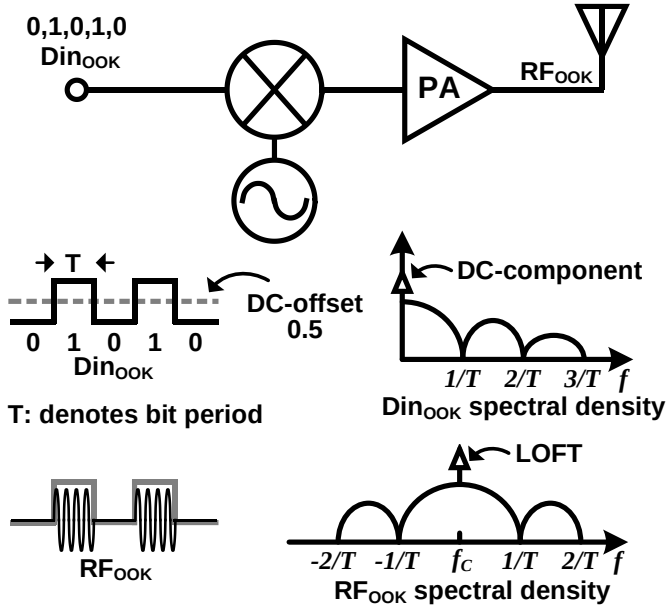


Figure 5.1: OOK modulation and its LOFT issue.

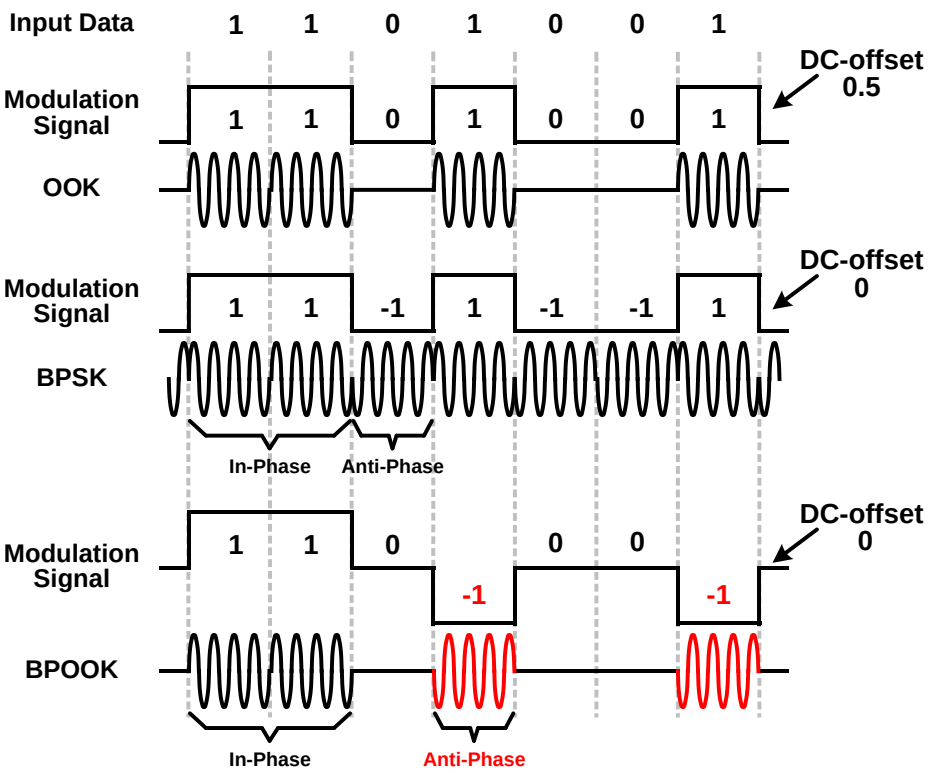


Figure 5.2: BPOOK modulation in comparison with OOK and BPSK.

transmitter and its transmitting power spectral density. The OOK input modulation signal has two levels: “0” and “1”. For a random input data with bit period of T, the input signal

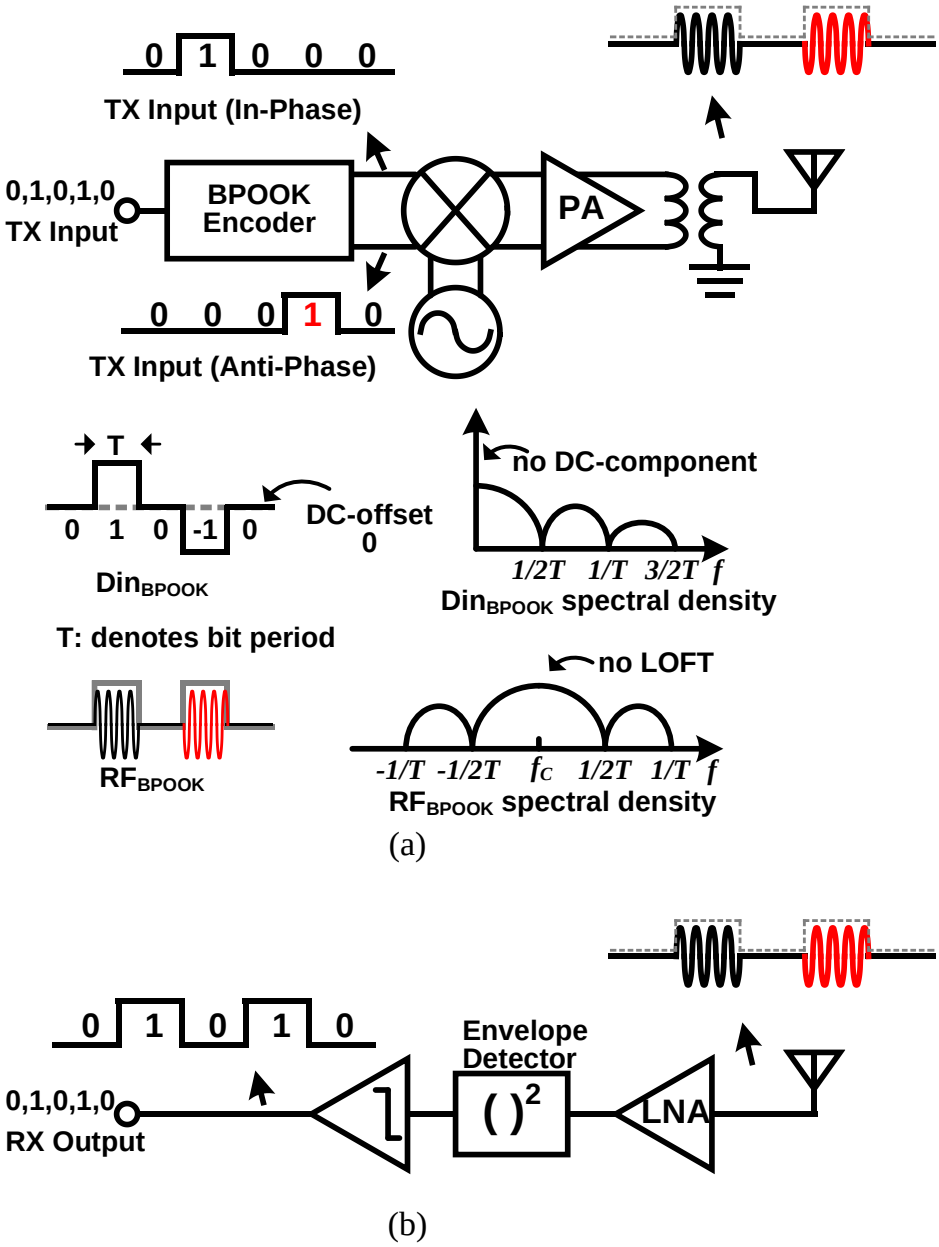


Figure 5.3: BPOOK incoherent demodulation.

power spectral density can be expressed as

$$S_{DinOOK}(f) = \frac{T}{8}\frac{sin^2(\pi T f)}{(\pi T f)^2} + \frac{\pi}{4}\delta(2\pi f) \tag{5.1}$$

The first term in (5.1) denotes the signal bandwidth of *Din*. It can be seen that the main lobe occupies a bandwidth of $1/T$. The second term in (5.1) denotes a DC-component appearing at the spectrum of the input signal. The DC-component can be easily observed

in time domain by calculating the DC-offset of input signal *Din*. The OOK RF signal is generated by switching on and off the local oscillator according to the input signal *Din*. The OOK RF signal power spectral density can be expressed as

$$S_{RFOOK}(f) = \frac{T}{8}\frac{sin^2(\pi T(f-f_c))}{(\pi T(f-f_c))^2} + \frac{\pi}{4}\delta(2\pi(f-f_c)) \tag{5.2}$$

An intrinsic LO feed through signal is observed in OOK spectrum from (2), which is an undesired component for wireless transmitting. A comparison can be made between OOK and binary phase shift keying (BPSK). As shown in Fig. 5.2, for OOK and BPSK, both modulation signals have only two levels, which are "1" and "0" for OOK and "1" and "-1" for BPSK. The BPSK modulation has no intrinsic LOFT issue since the DC-offset of BPSK modulation signal is 0. The bandwidth occupied by OOK and BPSK are the same, which is $2/T$. Therefore employing OOK and BPSK leads to a relative low spectrum efficiency. The spectrum efficiency can be improved by introducing more levels on the modulation signal and also by employing IQ modulator. However, both the methods are power consuming. The multi-level input and output need ADCs and DACs for level generation and decision. The IQ modulator requires quadrature local-oscillator for transmitter and receiver. In order to improve spectrum efficiency without consuming large power, the BPOOK modulation scheme is proposed in this paper. The basic operation principle of the BPOOK modulation is shown in Fig. 5.2. The BPOOK modulation signal has three levels: "1", "0", and "-1". When the input data is "1" the modulation signal is encoded to either "1" or "-1", the corresponding modulated RF signal is "on" status. When the input data is "0" the modulation signal is kept "0", the corresponding modulated RF signal is "off" status. Therefore, the BPOOK modulated RF signal has exactly the same envelope with the RF signal of a conventional OOK. Since the "on" status has two phases: in-phase and anti-phase, in other words the DC-offset of modulation signal is 0, the proposed BPOOK has no LOFT on its transmitting spectrum.

The conceptual modulation and demodulation architecture for BPOOK transceiver is shown in Fig. 5.3. As discussed before, the BPOOK modulation signal has three levels: "1", "0", and "-1". Conventionally it requires DAC and an additional negative voltage supplier to generate the desired three-level signal, which makes the modulator complex and impractical. Fortunately, a differential architecture can provide virtual negative voltage. As shown in Fig. 5.3, with the benefit of differential architecture, positive and negative modulation signal can be easily realized by employing a double-balanced mixer and a differential local oscillator. The input data is encoded by a BPOOK encoder, separating input data into two parallel sequences for differential input of mixer. The BPOOK encoder encodes input data with a rule as follow: when a sequence of "1" is followed by

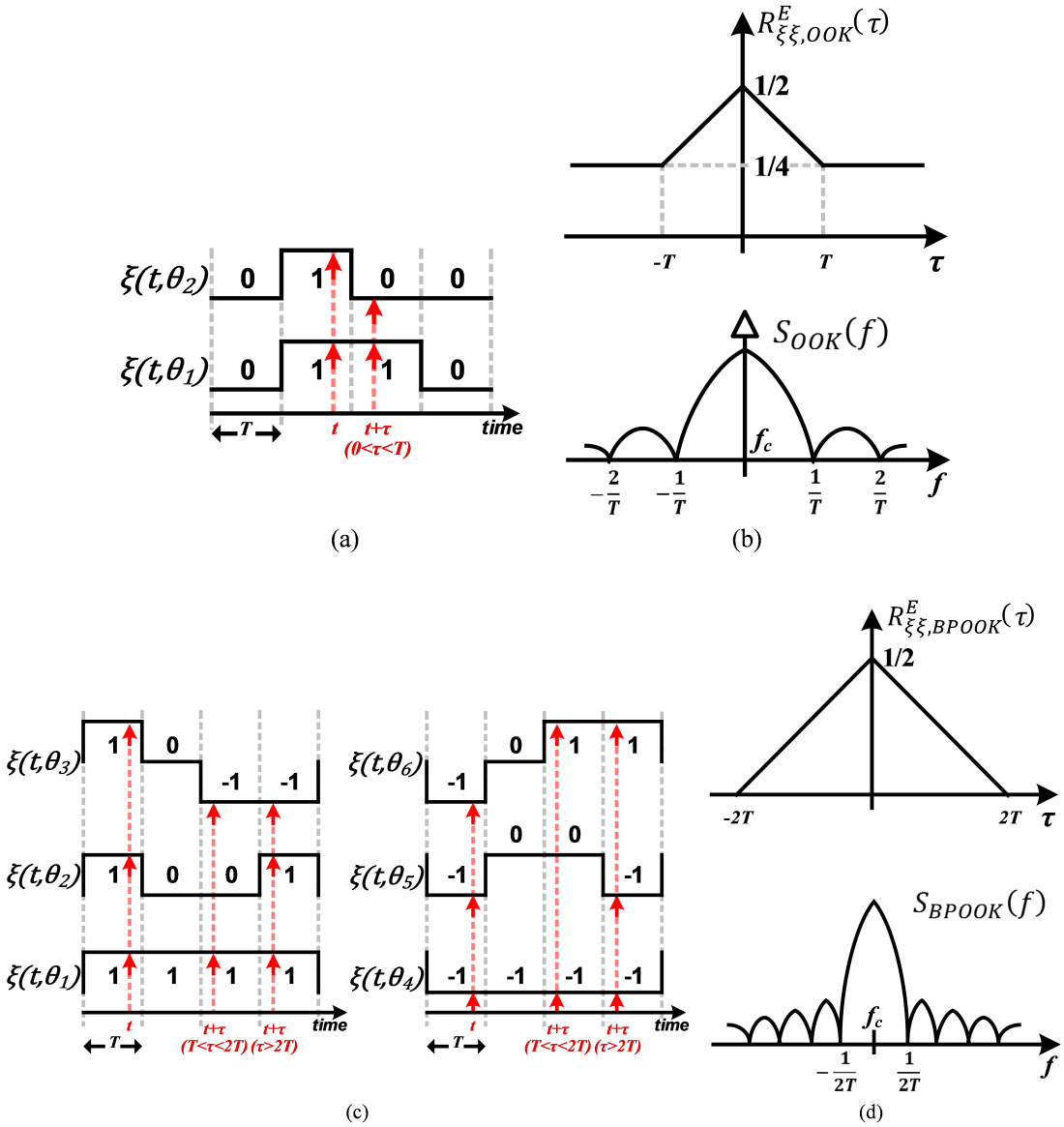


Figure 5.4: Power spectral density of OOK in comparison with BPOOK. (a) Selected repeated trials of OOK modulation signal, (b) OOK ensemble auto-correction and power spectral density, (c) Selected repeated trials of BPOOK modulation signal, (b) BPOOK ensemble auto-correction and power spectral density.

odd number of “0”s, the next sequence of “1” changes to “-1”; when a sequence of “1” is followed by even number of “0”s, the next sequence of “1” keeps “1”. The same polarity changes apply to a sequence of “-1”. Finally, “1” sequences and “-1” sequences are separated for mixer differential input. The concept of BPOOK modulation signal is similar with duobinary modulation, which is widely used in wireline communication [73–75]. In [76], a wireless transceiver employing duobinary modulation is presented. The duobinary wireless transceiver controls carrier amplitude with three levels: “0”, “1”, and “2”,

which requires a linear amplitude modulator for transmitter and a multi-level comparator for receiver. System complexity and power consumption is increased compared with the BPOOK transceiver. The duobinary wireless transceiver also suffers from LOFT issue since the DC-offset is non-zero. In [77], a TSSS-OOK is proposed for cancelling the LOFT. However, the TSSS-OOK spectrum is spread and high sampling rate is required, which makes it difficult to operate at high data rate. In [78], a BPSK-pulse-amplitude-modulation (BPSK-PAM) modulated transmitter for ultra-low-power impulse radio ultra-wideband (IR-UWB) is implemented. Although the BPOOK modulated signal and the BPSK modulated IR-UWB signal have similar waveform, there are differences on spectral efficiency and demodulation scheme between them. The BPSK based IR-UWB uses in-phase and anti-phase for representing "0" and "1", and the waveform carries no information during "off" status. By contrast, the BPOOK uses "off" and "on" to represent "0" and "1", and changing the phase for bandwidth reduction. Moreover, the BPSK based IR-UWB requires coherent demodulator which consumes more power.

For BPOOK demodulation, the RF signal can be in-coherently demodulated as shown in Fig. 5.3. The BPOOK modulated RF signal has exactly the same envelope with the OOK modulated RF signal. The low-power incoherent envelope detector can be utilized for BPOOK demodulation.

The OOK power spectral density and BPOOK power spectral density can be derived as follow. The selected repeated trials of the OOK modulation signal random process is shown in Fig. 5.4, the ensemble auto-correction of the trials can be expressed as

$$R^{E}_{\xi\xi,OOK}(\tau) = \int \xi(t,\theta)\xi(t+\tau,\theta)p(\theta)d(\theta) \tag{5.3}$$

$$= p(\xi(t) = 1, \xi(t+\tau) = 1) \tag{5.4}$$

For $|\tau| > T$, $\xi(t)$ is independent with $\xi(t+\tau)$, so that

$$R^{E}_{\xi\xi,OOK}(\tau) = p(\xi(t) = 1, \xi(t+\tau) = 1) \tag{5.5}$$

$$= p(\xi(t) = 1) \times p(\xi(t+\tau) = 1) \tag{5.6}$$

$$= \frac{1}{2} \times \frac{1}{2} = \frac{1}{4} \tag{5.7}$$

For $0 \leq |\tau| \leq T$, the transition probability from "1" to "0" during the interval τ is $\frac{1}{2}\left(\frac{\tau}{T}\right)$, so that

$$R^{E}_{\xi\xi,OOK}(\tau) = p(\xi(t) = 1) \times p(\xi(t+\tau) = 1) \tag{5.8}$$

$$= \frac{1}{2} \times \left(1 - \frac{1}{2}\left(\frac{\tau}{T}\right)\right) = \frac{1}{2} - \frac{\tau}{4T} \tag{5.9}$$

Then $R^{E}_{\xi\xi,OOK}(\tau)$ can be expressed as

$$R^{E}_{\xi\xi,OOK}(\tau) = \begin{cases} \frac{1}{2} - \frac{|\tau|}{4T}, & |\tau| \leq T \\ \frac{1}{4}, & |\tau| > T \end{cases} \tag{5.10}$$

Applying Wiener-Khinchin Theorem, the OOK spectral density is convolution of $R^{E}_{\xi\xi,OOK}(\tau)$ Fourier Transform and carrier signal $\cos(2\pi f_c t)$ Fourier Transform, expressed as

$$S_{OOK}(f) = \mathcal{FT}\left[R^{E}_{\xi\xi,OOK}(\tau)\right] * \mathcal{FT}\left[\cos(2\pi f_c t)\right] \tag{5.11}$$

$$= \frac{T}{8}\frac{sin^2(\pi T(f - f_c))}{(\pi T(f - f_c))^2} + \frac{\pi}{4}\delta(2\pi(f - f_c)) \tag{5.12}$$

The repeated trials of the BPOOK modulation signal random process is shown in Fig. 5.4 (c), the ensemble auto-correction of the trials can be expressed as

$$R^{E}_{\xi\xi,BPOOK}(\tau) = \int \xi(t,\theta)\xi(t+\tau,\theta)p(\theta)d(\theta) \tag{5.13}$$

$$\begin{aligned} &= p(\xi(t) = 1, \xi(t+\tau) = 1) \\ &+ p(\xi(t) = -1, \xi(t+\tau) = -1) \\ &- p(\xi(t) = 1, \xi(t+\tau) = -1) \\ &- p(\xi(t) = -1, \xi(t+\tau) = 1) \end{aligned} \tag{5.14}$$

For $0 \leq |\tau| \leq T$, there is no probability for "1" transit to "-1", or "-1" transit to "1". So that

$$\begin{aligned} R^{E}_{\xi\xi,BPOOK}(\tau) &= p(\xi(t) = 1) \times p(\xi(t+\tau) = 1) \\ &\quad + p(\xi(t) = -1) \times p(\xi(t+\tau) = -1) \qquad (5.15) \\ &= \frac{1}{4} \times \left(1 - \frac{1}{2}\left(\frac{\tau}{T}\right)\right) + \frac{1}{4} \times \left(1 - \frac{1}{2}\left(\frac{\tau}{T}\right)\right) \\ &= \frac{1}{2} - \frac{\tau}{4T} \qquad (5.16) \end{aligned}$$

For $T < |\tau| \leq 2T$, there are two transitions during the interval τ. In case of the transitions from "1" to "0" then to "-1", the probability of first transition "1" to "0" is $\frac{1}{2}$, and the probability of second transition "0" to "-1" is $\frac{1}{2}\frac{\tau - T}{T}$, so that

$$\begin{aligned} R^{E}_{\xi\xi,BPOOK}(\tau) &= p(\xi(t) = 1, \xi(t+\tau) = 1) \\ &\quad + p(\xi(t) = -1, \xi(t+\tau) = -1) \\ &\quad - p(\xi(t) = 1, \xi(t+\tau) = -1) \\ &\quad - p(\xi(t) = -1, \xi(t+\tau) = 1) \qquad (5.17) \\ &= \frac{1}{4} \times \frac{1}{2}\left(1 - \frac{1}{2}\frac{\tau - T}{T}\right) + \frac{1}{4} \times \frac{1}{2}\left(1 - \frac{1}{2}\frac{\tau - T}{T}\right) \\ &\quad - \frac{1}{4} \times \frac{1}{2}\left(\frac{1}{2}\frac{\tau - T}{T}\right) - \frac{1}{4} \times \frac{1}{2}\left(\frac{1}{2}\frac{\tau - T}{T}\right) \\ &= \frac{1}{2} - \frac{\tau}{4T} \qquad (5.18) \end{aligned}$$

For $|\tau| > 2T$, the polarity of non-zero $\xi(t)$ and $\xi(t+\tau)$ only depends on total number of "0" between them, so that

$$\begin{aligned} &R^{E}_{\xi\xi,BPOOK}(\tau) \\ &= p(\textit{even number } 0) \times (p(\xi(t) = 1) \times p(\xi(t+\tau) = 1)) \\ &\quad + p(\textit{even number } 0) \times (p(\xi(t) = -1) \times p(\xi(t+\tau) = -1)) \\ &\quad - p(\textit{odd number } 0) \times (p(\xi(t) = 1) \times p(\xi(t+\tau) = -1)) \\ &\quad - p(\textit{odd number } 0) \times (p(\xi(t) = -1) \times p(\xi(t+\tau) = 1)) \\ &= \frac{1}{2} \times \left(\frac{1}{4} \times \frac{1}{4}\right) + \frac{1}{2} \times \left(\frac{1}{4} \times \frac{1}{4}\right) - \frac{1}{2} \times \left(\frac{1}{4} \times \frac{1}{4}\right) - \frac{1}{2} \times \left(\frac{1}{4} \times \frac{1}{4}\right) \\ &= 0 \qquad (5.19) \end{aligned}$$

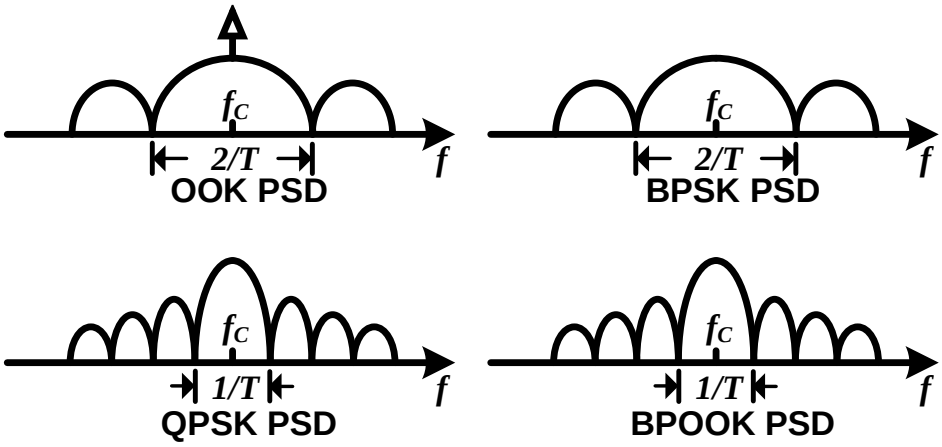


Figure 5.5: Power spectral density of OOK, BPSK, QPSK and BPOOK.

Then $R^{E}_{\xi\xi,BPOOK}(\tau)$ can be expressed as

$$R^{E}_{\xi\xi,BPOOK}(\tau) = \begin{cases} \frac{1}{2} - \frac{|\tau|}{4T}, & |\tau| \leq 2T \\ 0, & |\tau| > 2T \end{cases} \tag{5.20}$$

the BPOOK power spectral density can be expressed as

$$S_{BPOOK}(f) = \mathcal{FT}\left[R^{E}_{\xi\xi,BPOOK}(\tau)\right] * \mathcal{FT}\left[\cos(2\pi f_c t)\right] \tag{5.21}$$

$$= \frac{T}{2}\frac{sin^2(2\pi T(f - f_c))}{(2\pi T(f - f_c))^2} \tag{5.22}$$

Fig 5.5 and table 5.1 shows the comparison of the BPOOK modulation with OOK, BPSK, and QPSK. The BPOOK modulation eliminates the intrinsic LOFT issue in OOK modulation. Moreover, the BPOOK modulation can realize as high spectrum efficiency as QPSK, while avoid using power-consuming IQ modulator and coherent demodulator. The OOK and BPSK can also reduce transmitting spectrum bandwidth by employing finite impulse response (FIR) filter. However, the FIR filter requires high oversampling clock and accurate resistor-DACs (R-DAC) or current-DACs (I-DAC) for good filtering quality. As the data-rate increases, the design challenge of the oversampling circiut and DACs will also increase, which limits the data-rate and low-power application. From the above comparison, it can be summarized that the proposed BPOOK modulation scheme is suitable for low-power high-speed short-range wireless application at 60GHz.

Table 5.1: COMPARISON OF OOK, BPSK, QPSK, AND BPOOK

	OOK	**BPSK**	**QPSK**	**BPOOK**
LO	Single-ended	Differential	Quadrature	Differential
BW	2/T	2/T	1/T	1/T
LOFT issue	YES	NO	NO	NO
Demodulation	Incoherent	Coherent	Coherent	Incoherent

5.3 Low-Power High-Speed BPOOK Transceiver Design

5.3.1 Transceiver Architecture

Fig. 5.6 shows the entire block diagram of the 60-GHz BPOOK transceiver. The transmitter consists of a BPOOK encoder, a double-balanced mixer, a differential pre-amplifier, and a 5-stage power-amplifier (PA). For satisfying the out-of-band suppression requirement in IEEE 802.11 ad, an RC low-pass filter is used for spectrum sideband suppression. The 60-GHz local synthesizer consists of a 60-GHz injection locked oscillator (ILO) and a 20-GHz phase-locked loop (PLL) for subharmonic injection. On received side, the received RF signal is firstly amplified by a 5-stage low-noise amplifier (LNA), and then it is demodulated by a differential envelope detector. The demodulated baseband signal is amplified to rail-to-rail by a baseband amplifier. Both the transmitter input and the receiver output interfaces are digital. For comparison with the conventional OOK transceiver, an input for OOK modulation is also reserved in the transmitter without encoding.

5.3.2 BPOOK Encoder

Details of the BPOOK encoder design and operation timing diagram are illustrated in Fig. 5.7. Input data D_{in} is firstly encoded and separated to be positive input data D_{in_P} and negative input data D_{in_N}. An RC low-pass filter is employed to suppress spectrum sidelobe instead of a power-consuming FIR filter. The RC low-pass filter contains a 3-bit capacitor bank for enabling variable 3-dB cut-off frequency. The LPF highest cut-off frequency is 1.7GHz. However, there is trade-off between bandwidth efficiency in the frequency domain and intersymbol interference (ISI) in the time domain. By using the RC-filter to suppress the sidelobe, the ISI will be introduced and degrade the system S-NR and the receiver sensitivity. The RC-filter is followed by a double-balanced mixer,

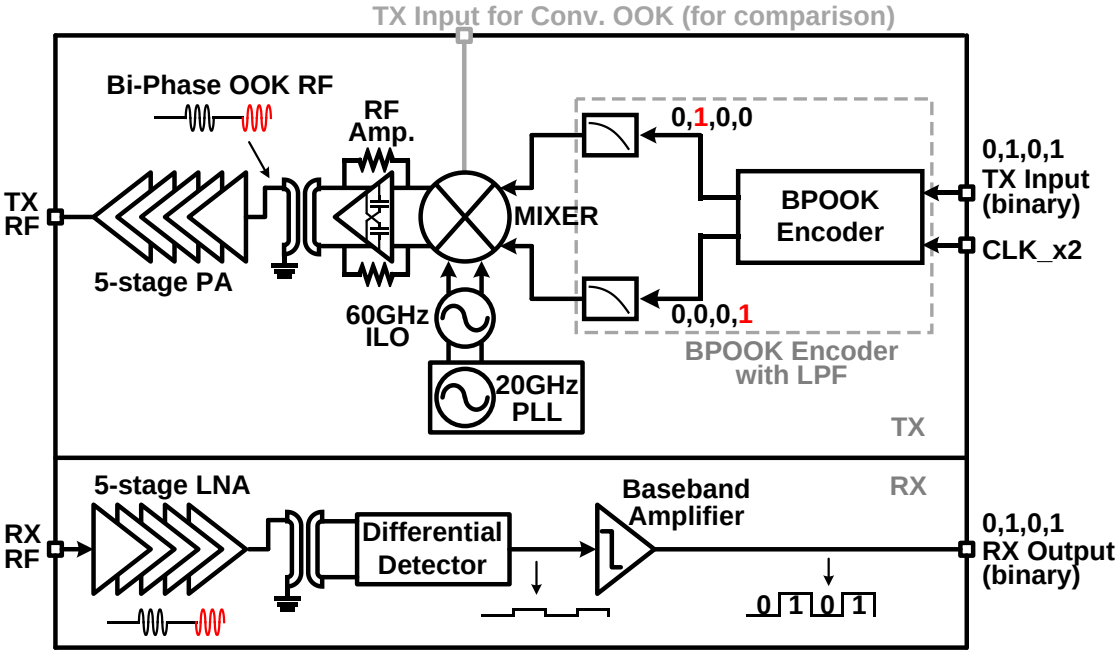


Figure 5.6: Block diagram of BPOOK transceiver.

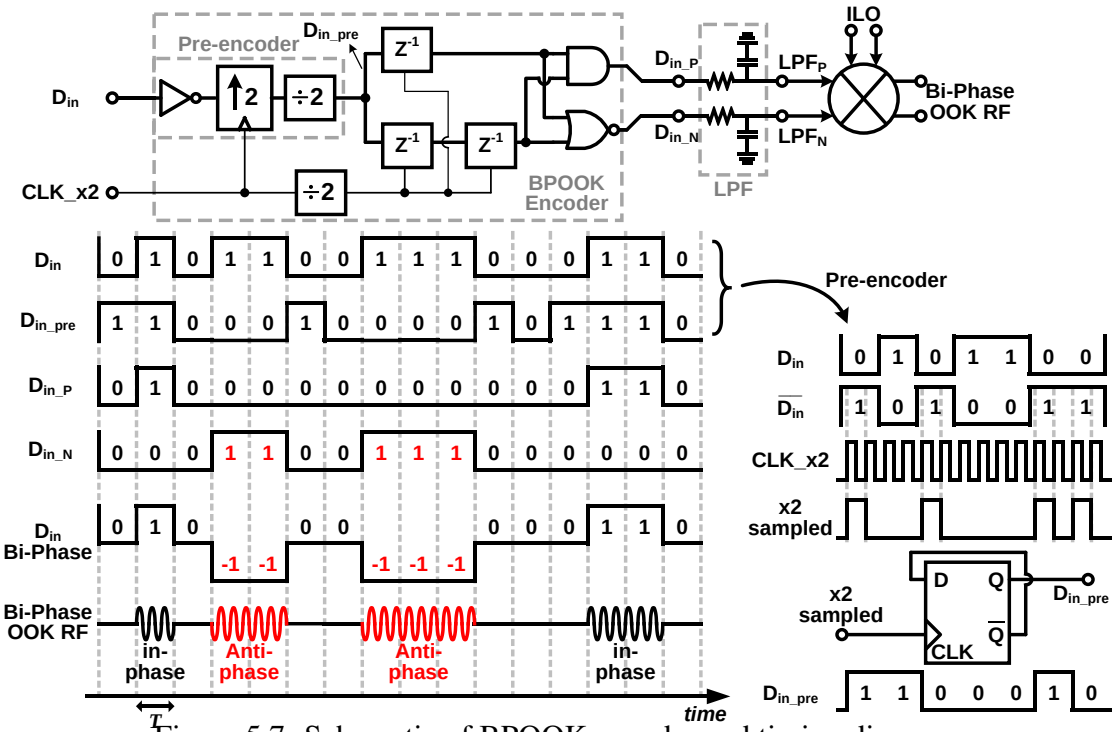


Figure 5.7: Schematic of BPOOK encoder and timing diagram.

which generates in-phase (0°) and anti-phase (180°) RF signal according to its positive and negative input data. The BPOOK encoder concept is following a design of duobinary encoder [74–76]. The input data D_{in} is firstly pre-encoded to D_{in_pre}. For wireline duobinary case, the D_{in_pre} is filtered by a 2-tap FIR filter to generate three-level signal during

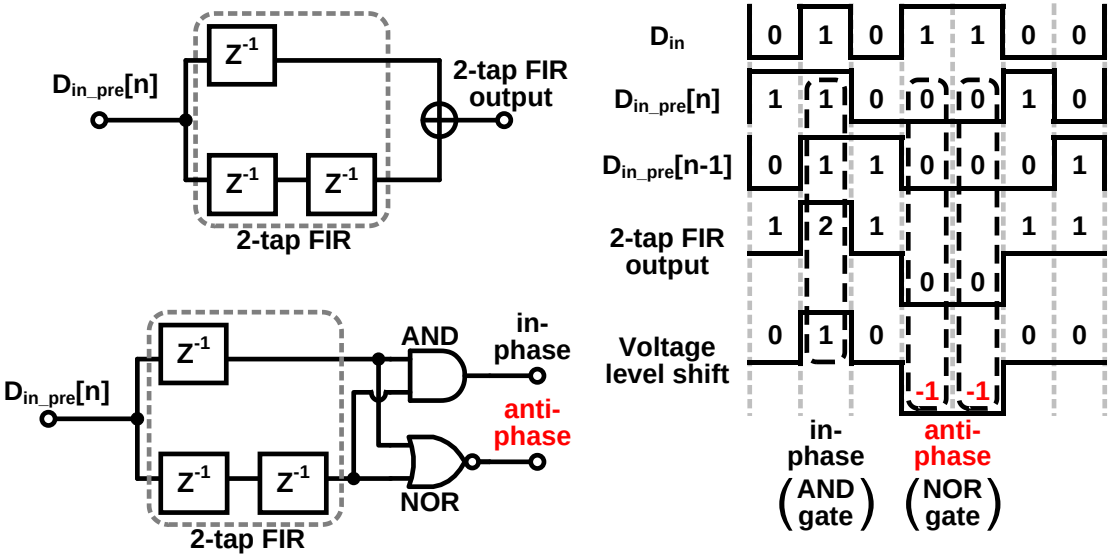


Figure 5.8: Principle of binary-phase generation for encoder.

transmission. In this work, D_{in_pre} is encoded to generate desired positive and negative modulation signal. The D_{in_pre} can be expressed in Boolean notation as:

$$D_{in\_pre}[n] = D_{in\_pre}[n-1] \oplus \overline{D_{in}[n]} \tag{5.23}$$

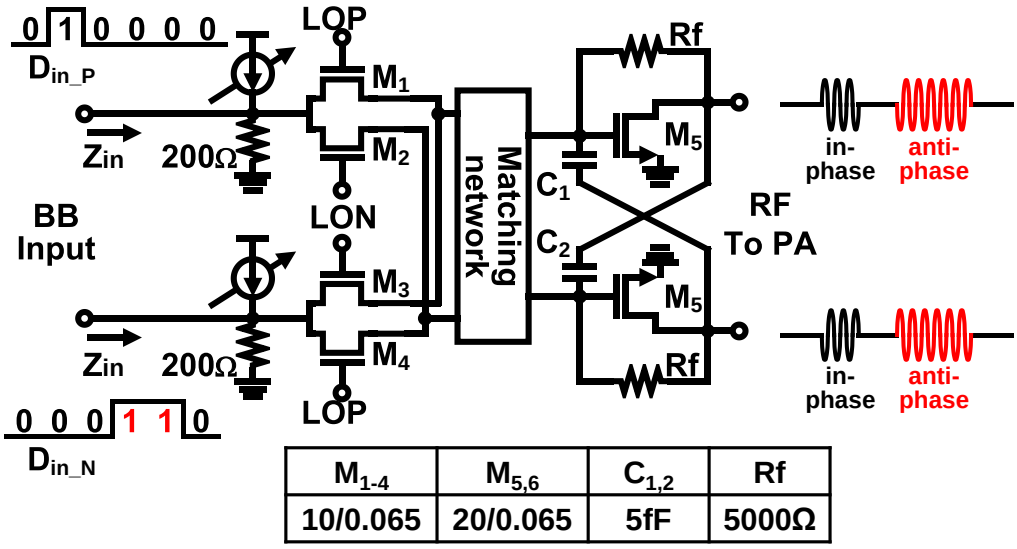
Fig. 5.7 also shows the detailed timing diagram of pre-encoder. Since previous pre-encoder in work [74–76] should satisfy a timing requirement, which requires fixed phase relationship between the input data and input clock. An up-sampling by 2 circuit is used in this work to replace the AND gate, without requirement on input clock phase.

Fig. 5.8 shows the operation principle for the BPOOK encoder. The pre-encoded input $D_{in\_pre}[n]$ generates a unit-delayed $D_{in\_pre}[n-1]$. If they are physically added, a three-level 2-tap FIR signal will be generated, which is usually for duobinary case. The desired BPOOK modulation signal can be produced by shifting the 2-tap FIR signal DC-offset to 0. Then it can be observed that the BPOOK positive input D_{in_P} can be expressed in Boolean notation as:

$$D_{in\_P}[n] = D_{in\_pre}[n] \bullet D_{in\_pre}[n-1] \tag{5.24}$$

and negative input D_{in_N} can be expressed as:

$$D_{in\_N}[n] = \overline{D_{in\_pre}[n] + D_{in\_pre}[n-1]} \tag{5.25}$$



$M_{1\text{-}4}$	$M_{5,6}$	$C_{1,2}$	Rf
10/0.065	20/0.065	5fF	5000Ω

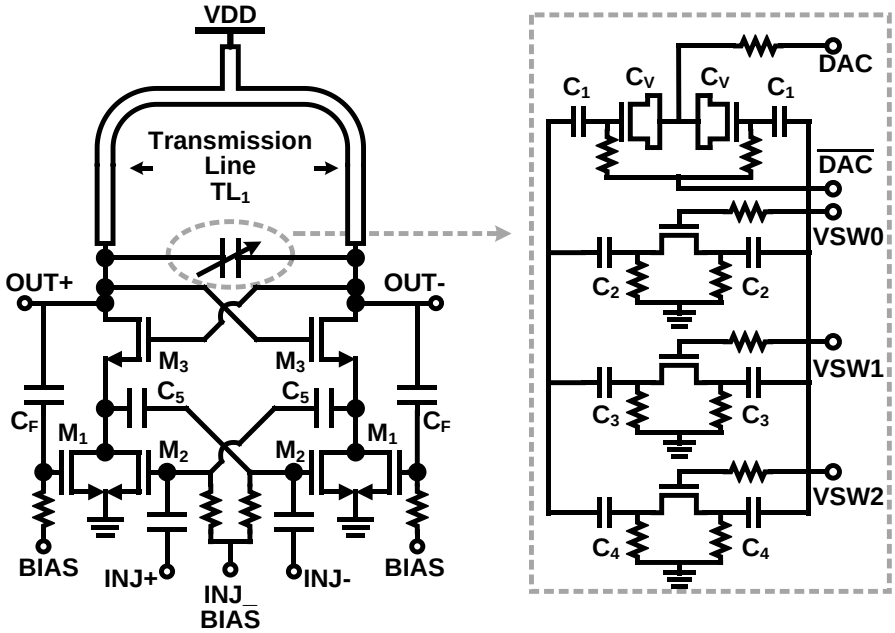
Figure 5.9: Schematic of double-balanced mixer and differential pre-amplifier.

Thus, the D_{in_P} and D_{in_N} encoder circuit can be practically implemented by an AND gate and a NOR gate.

5.3.3 Transmitter

Fig. 5.9 shows the detailed circuits of the double-balanced mixer and RF pre-amplifier in transmitter. A mixer first transmitter architecture is adopted due to its wideband characteristics. The mixer is followed by a resistive-feedback differential amplifier with capacitive-cross-coupling neutralization for flat gain characteristic. The double-balanced mixer consists of two single-balanced mixers. The modulated BPOOK RF signal is produced by alternatively turning on the single-balanced mixer with positive and negative baseband input. The differential amplifier output is connected to the power amplifier through a parallel-line transformer.

This 60-GHz transceiver employs a 60-GHz ILO and a 20-GHz sub-harmonic PLL for local synthesizer. The phase noise of the 60-GHz ILO is determined by the 20-GHz PLL, thus a better jitter performance can be achieved than a 60-GHz PLL with VCO oscillating at fundamental frequency [79]. According to IEEE standards, the 60-GHz I-LO should cover center frequencies at four channels, which are 58.32, 60.48, 62.64, and 64.80 GHz. However, it is challenging to design a millimeter-wave oscillator operating at target frequency due to parasitic parameters and RF device model accuracy. Fortunately, electromagnetic (EM) simulation and post-layout parasitic extraction can provide designers helpful estimation. The core part layout of the ILO includes capacitor bank



M_1	M_2	C_1	C_2	C_3	C_4	C_5	C_V	C_F	TL_1
24/0.065	16/0.065	47fF	15fF	30fF	45fF	53fF	30~140fF	10fF	135um

Figure 5.10: Schematic of ILO and variable capacitor.

and transistors is very compact, and the RC parasitic parameters can be extracted for post-layout simulation. The inductor RF model provided by foundry is usually optimized for low-gigahertz application, thus the inductor value and quality factor at millimeter-wave frequency becomes inaccurate even with the assistance of EM simulation. This paper propose an ILO using modeled transmission line (TL) as inductor to achieve accurate free running frequency. As shown in Fig. 5.10, The ILO contains a LC tank, a cross-coupled pair, a pair of tail transistors, and a pair of injection tail transistors with g_m-enhancement [80]. Measurement-data modeled transmission line is popular in millimeter-wave matching blocks due to high accuracy and flexible layout. The transmission line can be modeled accurately up to 110 GHz with measurement using multi-line de-embedding method [41]. The transmission line Q is relatively lower than that of inductor, since the transmission line is optimized for characteristic impedance. Therefore, the overall LC tank Q is degraded. However, since the phase noise of the 60-GHz ILO is determined by that of the 20-GHz PLL, we can focus on the frequency coverage in ILO design regardless of Q degradation. A measurement-data based RLGC transmission line model is generated for ILO periodic steady state (PSS) simulation. Fig. 5.11 shows the simulated 60-GHz ILO free-running frequency coverage and the measured values. It shows up to

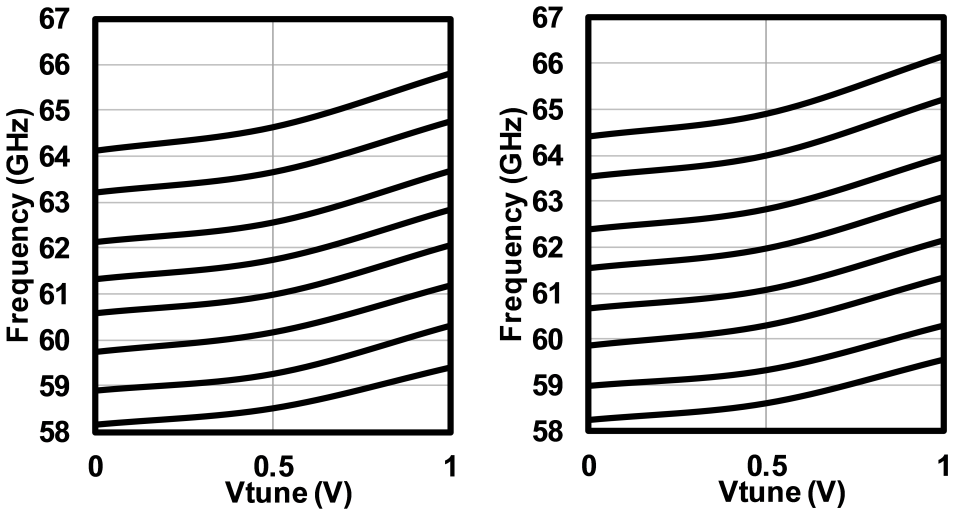
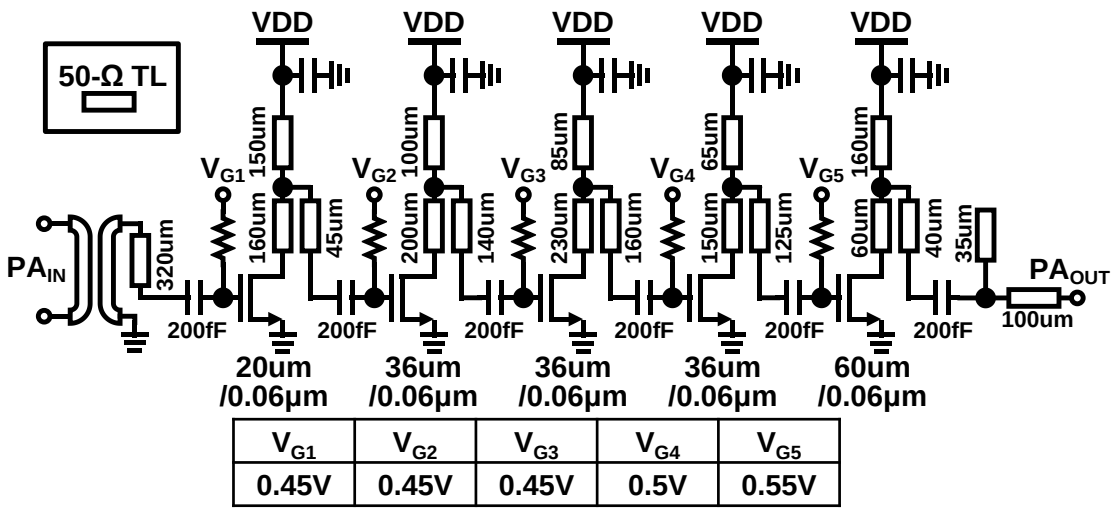


Figure 5.11: ILO free-running frequency coverage (a) simulation (b) measurement.



V_{G1}	V_{G2}	V_{G3}	V_{G4}	V_{G5}
0.45V	0.45V	0.45V	0.5V	0.55V

Figure 5.12: Schematic of the PA.

500 MHz frequency shifting between simulation and measurement. Fig. 5.12 shows the circuit schematic of the five-stage common-source PA. Transmission lines and 200-fF DC-cut capacitors are used for PA impedance matching. The 200-fF DC-cut capacitors are measured and modeled for reuse and high accuracy simulation. The PA first three stages are optimized with higher gain characteristics, and final two stages are matched for high output power with large transistor width. The PA has simulated 30 dB Gain and 5 dBm saturated output power. The PA differential input is converted to single-ended using

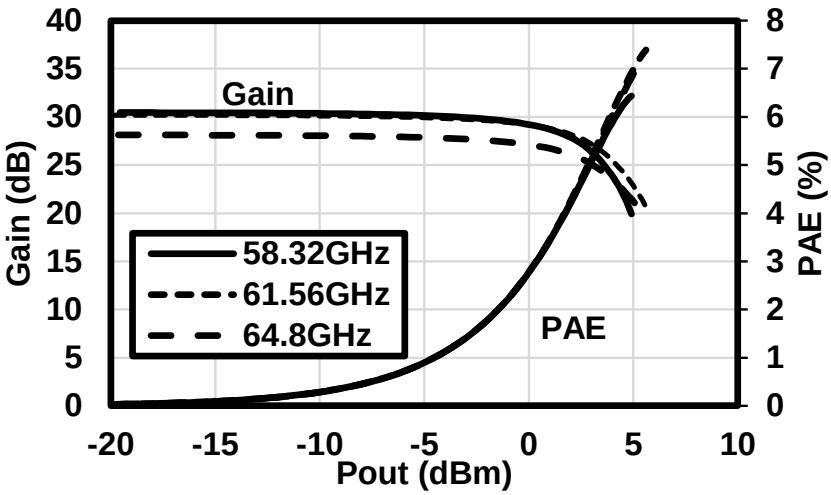


Figure 5.13: Simulated PA large-signal performance.

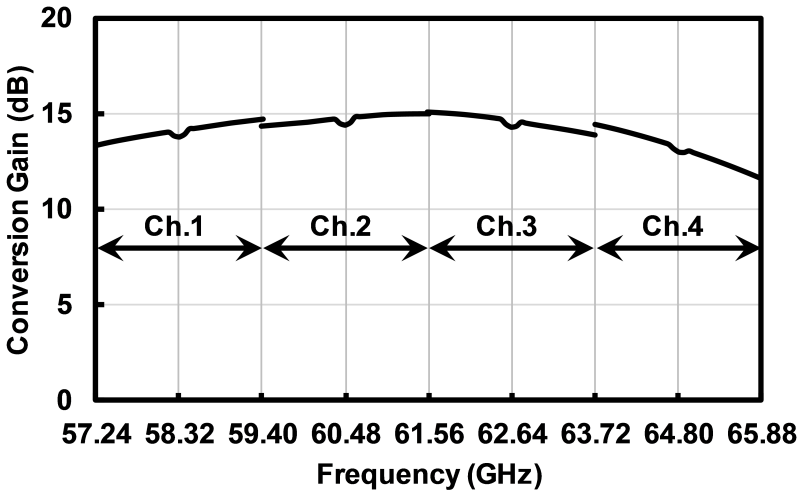
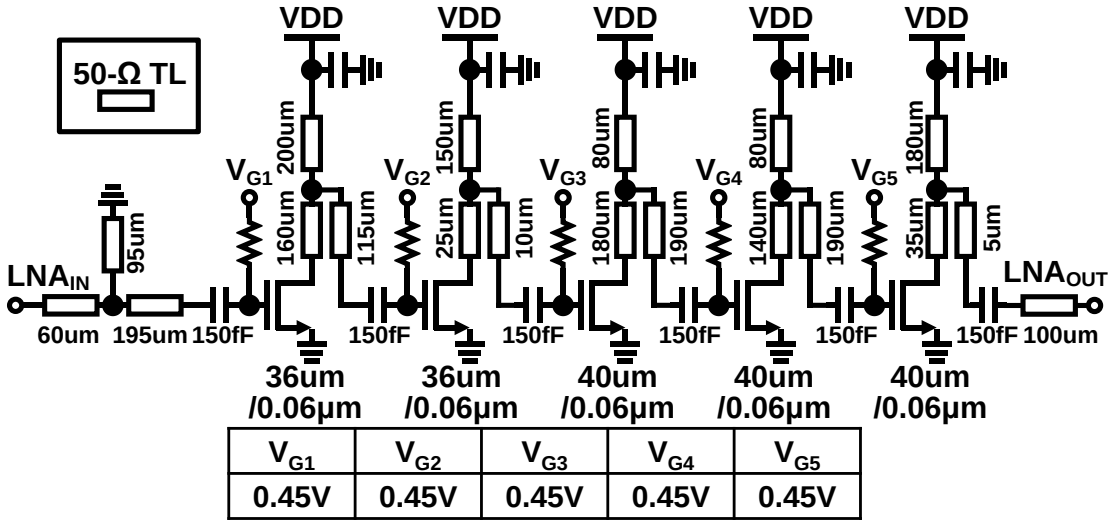


Figure 5.14: Simulated transmitter conversion gain.

a parallel line transformer, and the PA output is matched 50-Ohm for connecting with antenna. Fig. 5.13 shows the simulated PA large-signal performance. Fig. 5.14 shows the simulated transmitter conversion gain for each channel with LO frequencies at 58.32, 60.48, 62.64, and 64.80 GHz. The transmitter covers four channels with a conversion gain flatness in 3 dB.



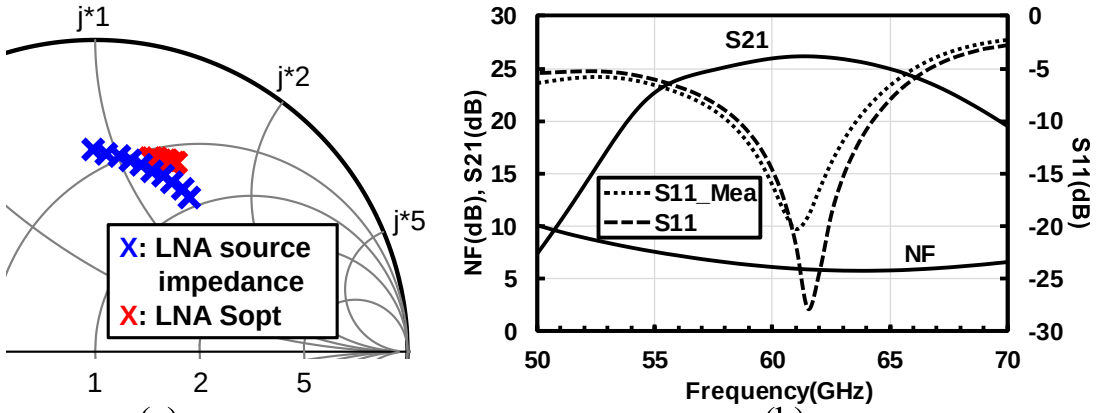
V_{G1}	V_{G2}	V_{G3}	V_{G4}	V_{G5}
0.45V	0.45V	0.45V	0.45V	0.45V

Figure 5.15: Schematic of the LNA.

5.3.4 Receiver

The BPOOK modulated RF signal can be demodulated using both coherent demodulator and incoherent demodulator. The coherent demodulator has higher sensitivity [81] and higher power consumption. A three-level comparator is also required by using coherent demodulator. For low-power short-range communication, this work employs incoherent demodulator due to its simplicity. The receiver consists of a five-stage LNA, a differential envelope detector, and a limiting amplifier, as shown in Fig. 5.6. Fig. 5.15 shows circuit schematic of the five-stage common-source LNA. The LNA matching uses transmission line and capacitors as used in PA design. The LNA first and second stages contribute most on the overall noise figure (NF), and the first and second stages are matched to get minimum NF and the other stages are designed for gain optimization. The single-ended LNA output is connected to a differential detector through parallel-line transformer. Fig. 5.16 shows the LNA simulated source impedance, NF, small signal gain, input reflection coefficient and cascaded NF.

The circuit schematic of differential envelope detector and baseband limiting amplifier is shown in Fig. 5.17. The differential envelope detector employs cross-coupled-capacitor gain-boosted architecture [70]. The matching blocks use modeled transmission line and parallel-line transformer for reliable simulation. The input RF signal is converted to differential and connected to both gate and drain of the transistor pair. The quarter-wave transmission line is used to provide RF high impedance at the transistor pair source node. The conversion gain of the differential envelope detector under class-B biasing can be

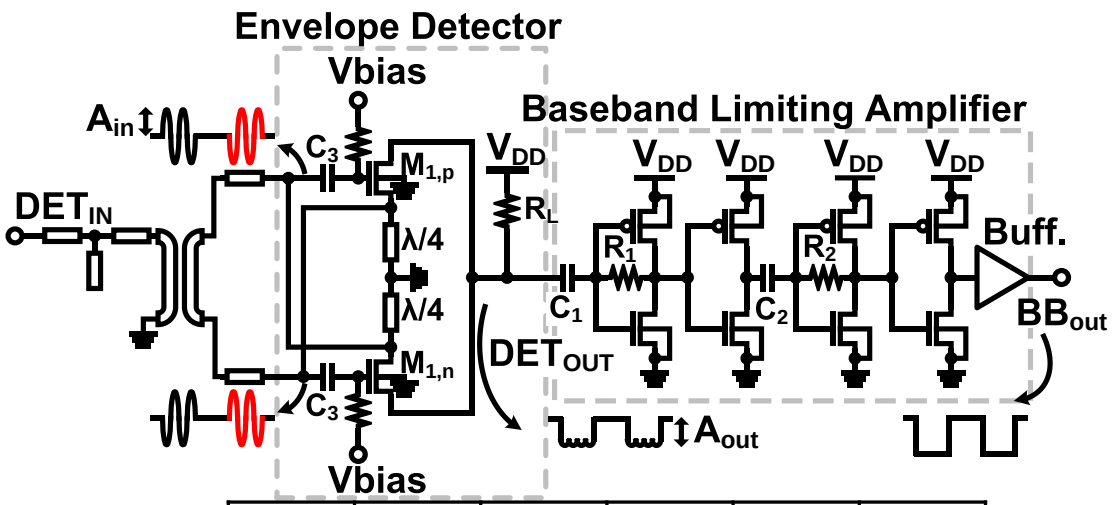


(a) (b)

stages	1	2	3	4	5
Cascaded NF (dB)	4.3	5.3	5.8	6.1	6.2
Cascaded Gain (dB)	4.1	7.2	13.4	19.6	26.5

(c)

Figure 5.16: Simulated LNA (a) source impedance, (b) NF, small signal gain, reflection coefficient (c) and cascaded NF.



$M_{1p,n}$	$C_{1,2}$	C_3	$R_{1,2}$	R_L	Vbias
16/0.065	600fF	200fF	1MΩ	2.5kΩ	0.32V

Figure 5.17: Schematic of the envelope detector and baseband limiting amplifier.

expressed as

$$CG = \frac{A_{out}}{A_{in}} \approx \frac{1}{2}\mu_n C_{ox} \cdot \left(\frac{W_1}{L_1}\right) \cdot (4A_{in}) \cdot |Z_L| \tag{5.26}$$

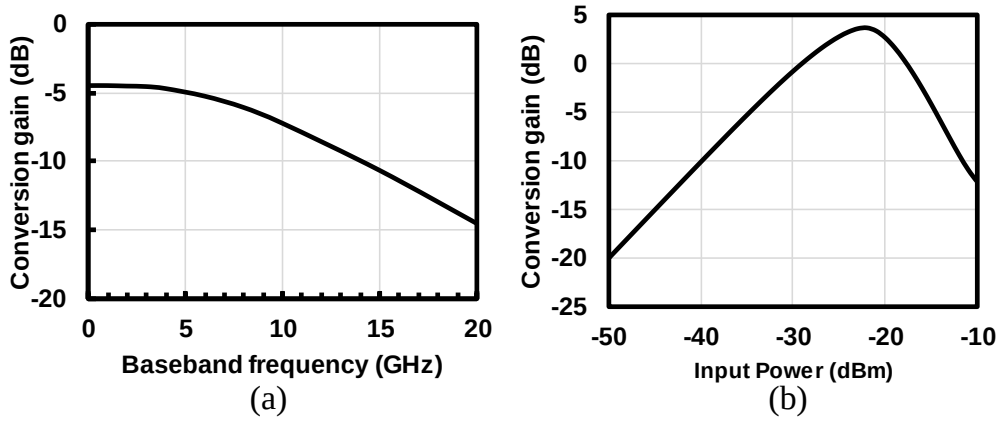


Figure 5.18: Simulated envelope detector conversion gain (a) at -35dBm input power, (b) at 5GHz baseband frequency.

Z_L is the detector load impedance given as where $r_{out} = (1/2)r_{o1} = 1.1k\Omega$ is the equivalent output resistance of transistor pair M_{1p} and M_{1n}. $C_{out} = 2C_{d1} = 7.7fF$ is the parallel drain capacitance of M_{1p} and M_{1n} seen at the output. $C_{1p} = 8.2fF$ is the parasitic capacitance of C_1. The calculated high cut-off frequency is 13.1 GHz. Fig. 5.18(a) shows the simulated conversion gain of the detector with high cut-off frequency at 10.2 GHz at -35dBm input. The conversion gain with a wide range of input power is also presented in Fig. 5.18(b). A low-power inverter-based baseband limiting amplifier is used to amplify the detected baseband signal to rail-to-rail, with a simulated lower cut-off frequency at 2.7 MHz. A 50Ω source follower is used at the output of limiting amplifier for high drive ability.

5.4 Measurement Results

The 60-GHz BPOOK transceiver chipset is designed and fabricated in the standard 65-nm CMOS technology. Fig. 5.19 shows the chipset die micrographs. The core area of the transmitter is 1.20 mm^2 and receiver is and 0.36 mm^2. The transmitter and the receiver consumes a power of 78 mW and 22 mW, respectively, both from 1-V supply.

The receiver measurement first took place for checking the receiver demodulation capability. As the BPOOK RF signal has the same envelope with OOK RF signal, an external OOK transmitter is implemented for measurement. Fig. 5.20 shows the on wafer measurement setup for receiver. The external OOK transmitter consists of a pulse pattern generator (Anritsu MP1775A) for baseband pseudo random binary sequence (PRBS) input, a mixer, and a 60-GHz signal generator (Agilent E8257D) for LO. The OOK signal is connected to the receiver input through a variable attenuator. The receiver demodulated

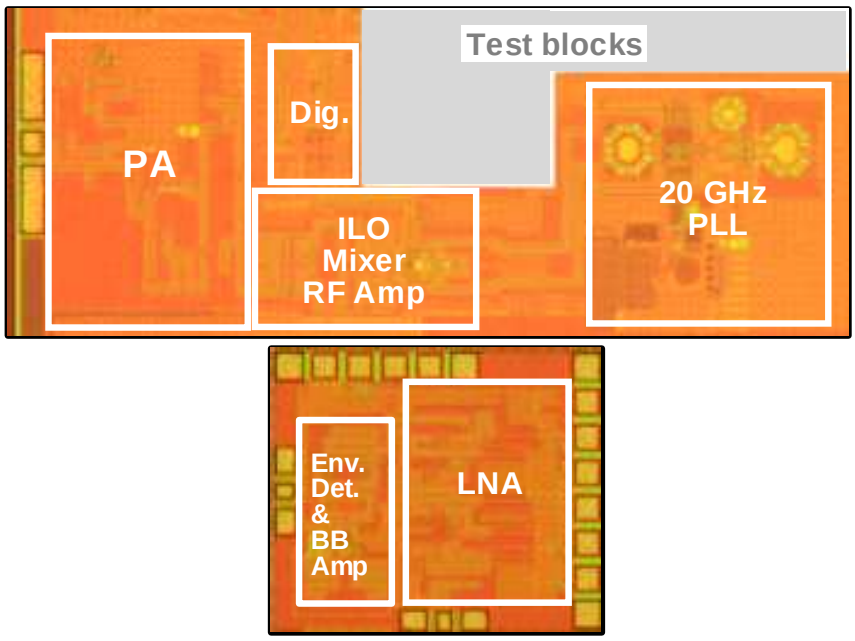


Figure 5.19: Die micrographs.

Table 5.2: Transceiver Area and Power Summary

		Area	Power
TX	Digital+LPF	0.01 mm^2	4.2 mW
	ILO+Mixer	0.14 mm^2	5.0 mW
	20-GHz PLL	0.40 mm^2	25.0 mW
	RF Amp.	0.14 mm^2	6.0 mW
	PA	0.51 mm^2	38.0 mW
	TX total	1.2 mm^2	78 mW
RX	LNA	0.23 mm^2	20.0 mW
	Envelope Detector	0.12 mm^2	0.1 mW
	Baseband Amplifier	0.01 mm^2	1.7 mW
	RX total	0.36 mm^2	22 mW

data is analyzed using an oscilloscope (Keysight DSO91304A). Fig. 5.21 shows the captured eye-diagram of receiver demodulated baseband at a data rate of 12.5 Gb/s, which is the up-limit data rate that Anritsu MP1775A can generate. The clean eye-diagram shows that the incoherent OOK demodulator is capable of at least 12.5 Gb/s data rate.

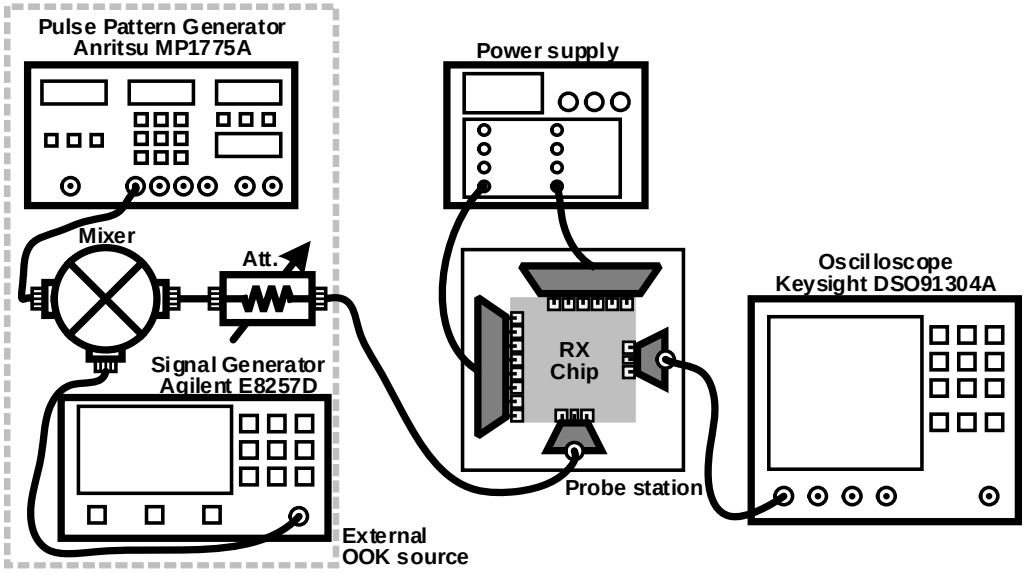


Figure 5.20: Measurement setup for receiver capability.

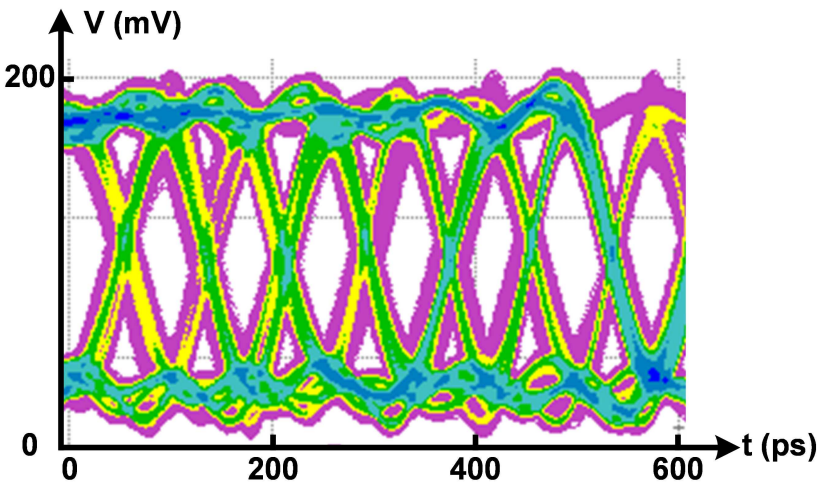


Figure 5.21: Receiver demodulated baseband eye-diagram at 12.5 Gb/s data rate.

Fig. 5.22 shows the measurement setup for transceiver. A PCB for transmitter is used. The baseband PRBS data is generated by pulse pattern generator (Anritsu MP1775A), and connected to transmitter PCB. There are two modulation modes: the BPOOK mode, and the conventional OOK mode for comparison. The transmitter RF signal is connected to a power splitter. One path is connected to receiver for demodulation. Another path is down-converted and connected to spectrum analyzer (Agilent E4448A).

The measured transmitter output power including wire bonding and PCB connection

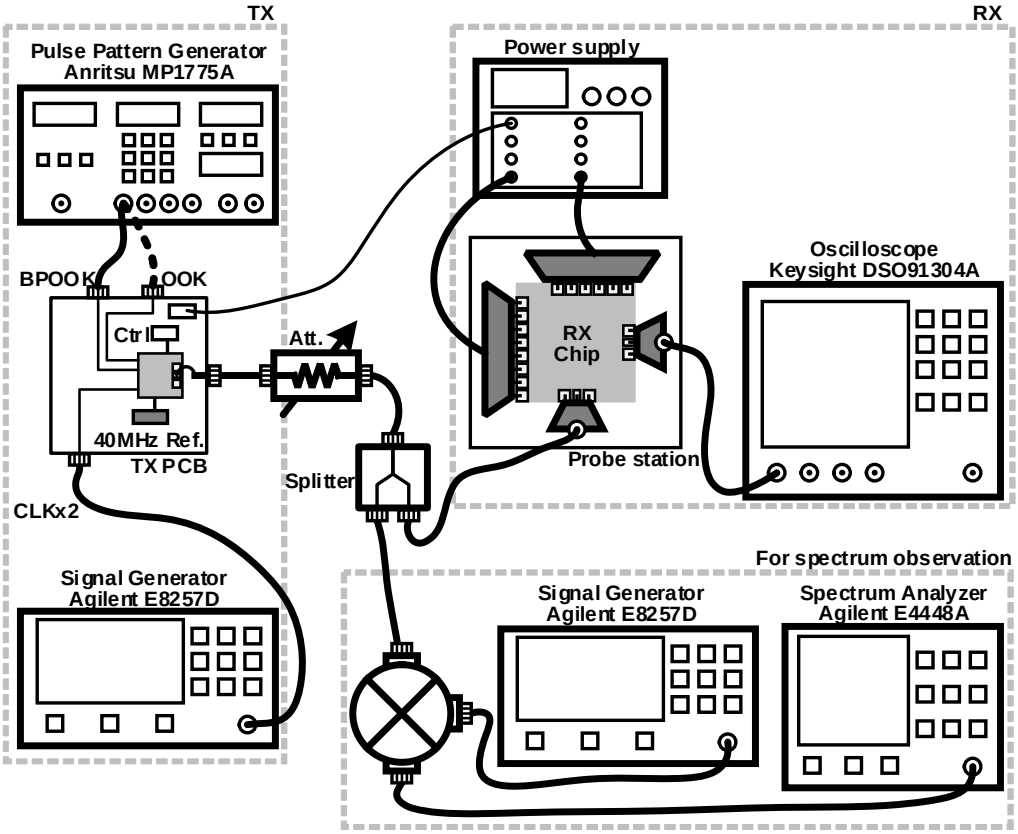


Figure 5.22: Measurement setup for transceiver.

loss is -8.7 dBm, -7.8 dBm, -8.0 dBm, and -9.8 dBm at 58.32 GHz, 60.48 GHz, 62.64 GHz and 64.80 GHz, respectively. By increasing mixer driving power and RF-amplifier gain, the transmitter maximum output power is achieved -3.0 dBm at 61.56 GHz. The transmitter linearity measurement cannot be done since the baseband and RF blocks are connected internally.

Fig. 5.23 shows the receiver demodulated baseband eye-diagram at 3.0 Gb/s data rate, with PRBS length of both $2^7 - 1$ and $2^{31} - 1$. The data-rate is mainly limited by transmitter digital circuits, including buffers and clock. The receiver sensitivity is measured by adjusting variable attenuator. Fig. 5.24 shows measured receiver sensitivity as a function of input power at the data rate of 3.0 Gb/s. The performance for $2^{31} - 1$ PRBS is degraded due to the $2^{31} - 1$ PRBS contains more low-frequency components, and the baseband limiting amplifier has a lower cut-off frequency of 2.7MHz. The communication distance is evaluated by assuming two 6-dBi antennas for transmitter and receiver packaging [82, 83]. The distance is calculated using Friis free space propagation equation

$$\frac{P_r}{P_t} = D_r D_t (\frac{\lambda}{4\pi d})^2 \tag{5.27}$$

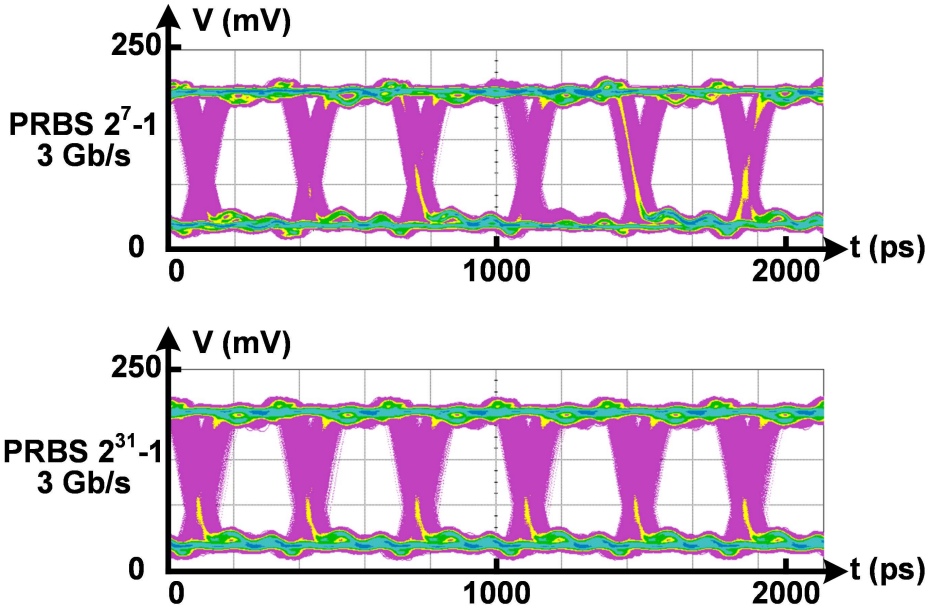


Figure 5.23: Receiver demodulated baseband eye-diagram at 3Gb/s data rate.

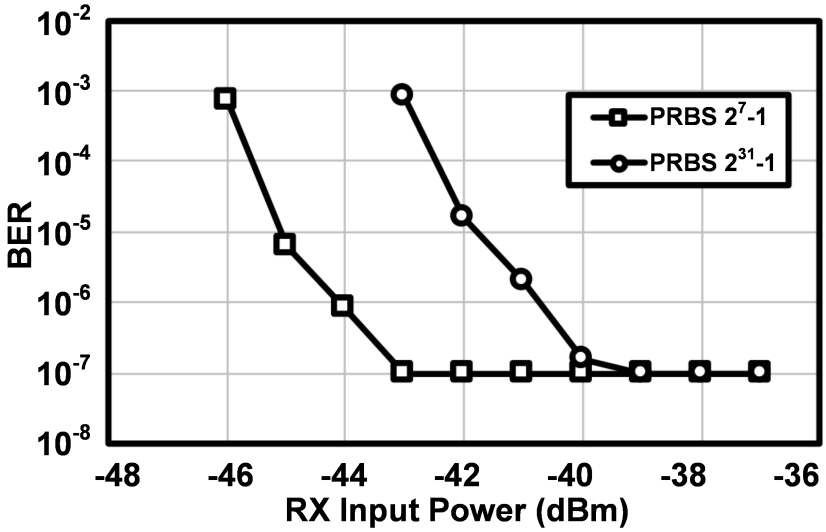
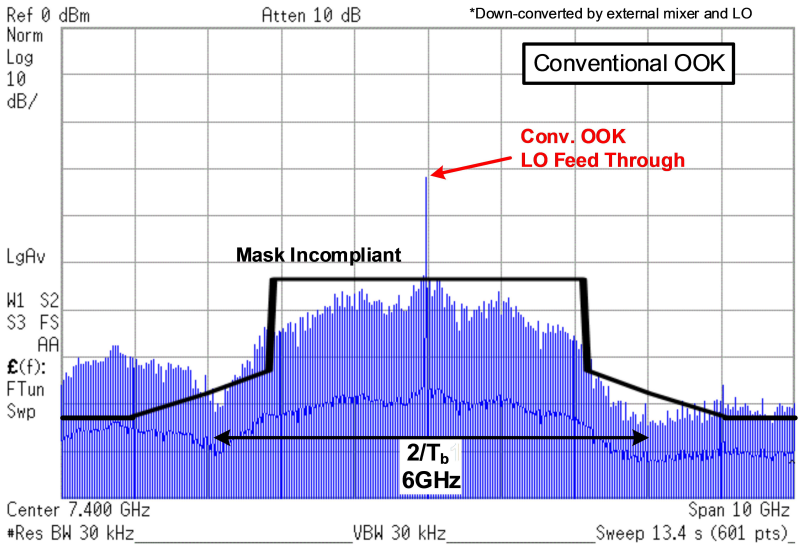
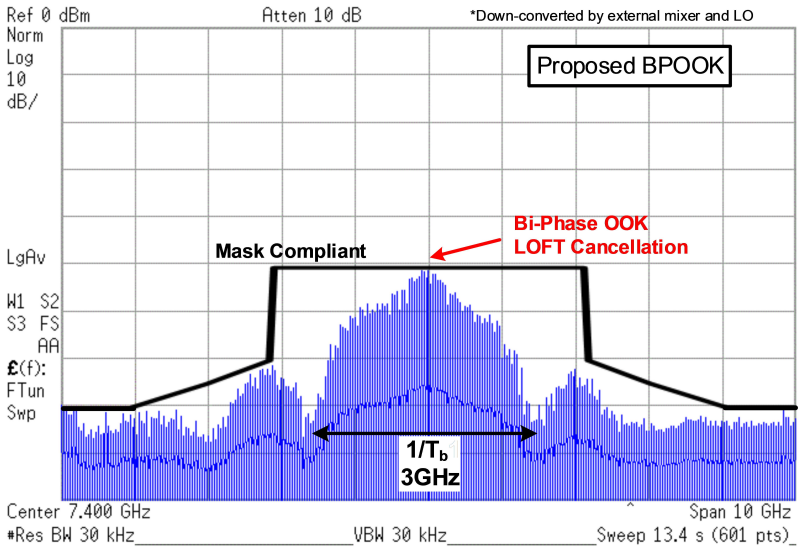


Figure 5.24: BER as a function of RX input power.

where P_r, D_r, and P_t, D_t denotes receiver input power, antenna directivity, and transmitter output power, antenna directivity. λ is the freespace wavelength at 60-GHz, and d is the distance between the antennas. For $P_r = -46dBm$ and $P_t = -3dBm$, the estimated communication distance at 3.0 Gb/s data rate is 0.14 m with a BER of $< 10^{-3}$. The communication distance can be further improved by employing antenna arrays [84], which benefit from small antenna size at millimeter wave frequency.



(a)



(b)

Figure 5.25: Measured 2-channel bonding spectrum of transmitter at 3.0 Gb/s data rate on (a) OOK mode, and (b) BPOOK mode.

Fig. 5.25 shows the measured transmission spectrum on OOK mode and BPOOK mode both at the 3.0 Gb/s data rate. The carrier frequency is 59.4 GHz for two-channel (ch.1 and ch.2) bonding. The measured output power in BPOOK mode is -9.1 dBm. The transmission spectrum is measured by using a down-conversion mixer and a signal generator as shown in Fig. 5.22. It can be observed that in conventional OOK mode, the mainlobe of the spectrum occupies a bandwidth of 6 GHz, and the LO feed through is high. In the proposed BPOOK mode, the mainlobe of the spectrum is 3 GHz, which is on-

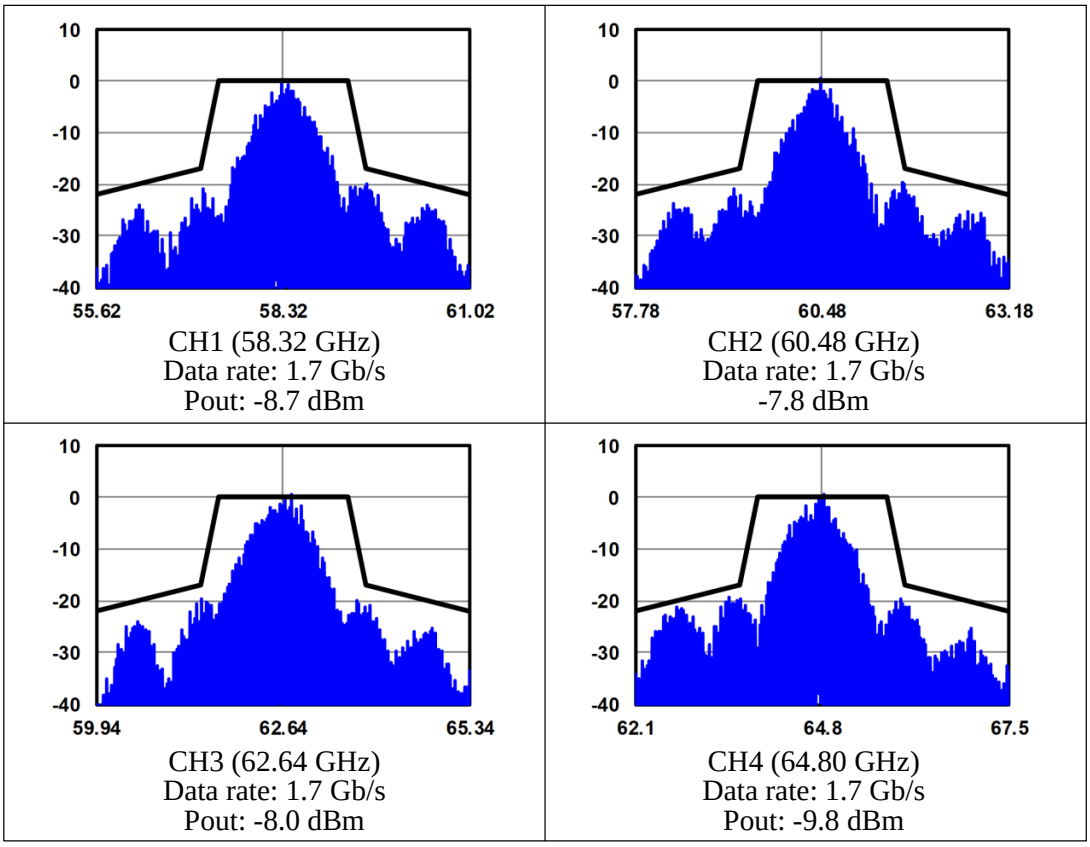


Figure 5.26: Measured spectrum of transmitter at 1.7 Gb/s data rate on BPOOK mode for all 802.11ad channels.

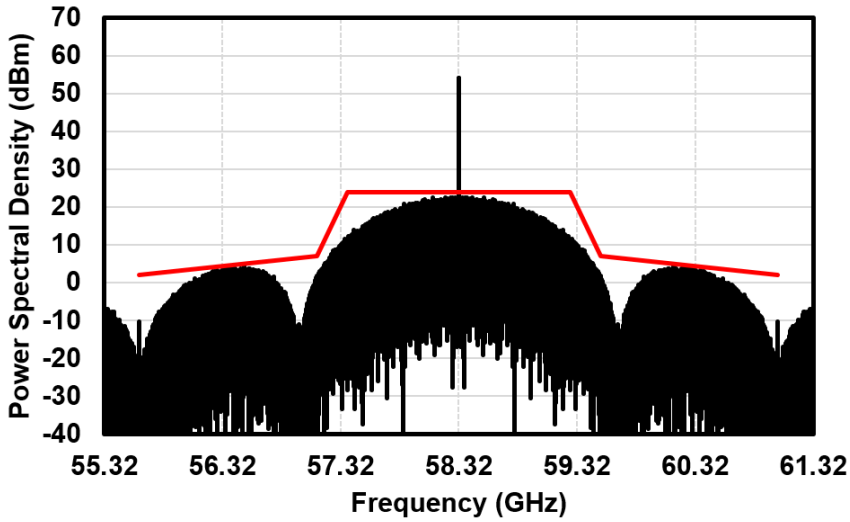


Figure 5.27: Simulated highest data rate on OOK mode with 1-channel bandwidth in IEEE 802.11ad standard.

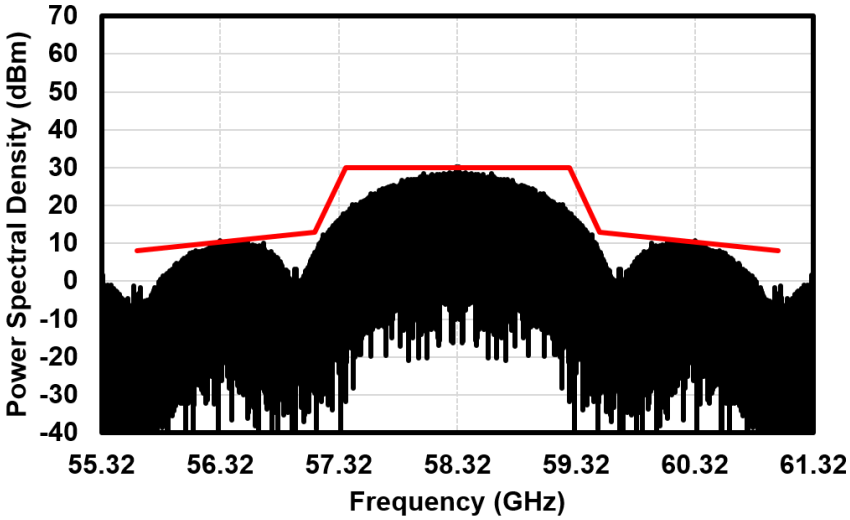


Figure 5.28: Simulated highest data rate on BPOOK mode with 1-channel bandwidth in IEEE 802.11ad standard.

ly half of that in OOK mode. Moreover, the BPOOK modulation cancels the LOFT issue. A spectrum mask for 60-GHz two-channel bonding is applied to both OOK and BPOOK spectrum. The BPOOK spectrum shows good compliance with the mask. Fig. 5.26 shows the measured transmission spectrum on BPOOK mode for all 802.11ad channels. It can be observed that the BPOOK transmission spectrum has a good compliance with the single-channel mask at a data rate of 1.7 Gb/s. The measured ACLR is 18.37dB at 60.48 GHz.

Applying the spectrum mask given in IEEE 802.11ad standard above to a BPOOK transmit signal and a OOK transmit signal, the BPOOK achieves a highest data rate of 2.7Gbps. The OOK achieves a highest data rate of 1.35Gbps under the spectrum mask with a large LOFT leakage. The spectrum efficiencies are 1.25b/s/Hz and 0.63b/s/Hz for BPOOK and OOK respectively. The simulated spectrums are shown in Fig. 5.27 and Fig. 5.28.

Table 5.3 shows a performance comparison of 60-GHz transceivers with digital input-output interface. Under the constraint of spectrum mask, the proposed BPOOK transceiver achieves 3.0 Gb/s data rate, while consuming a lowest power of 100 mW. The energy efficiency of the transceiver achieves 33.3 pJ/bit, which is a significant improvement compared with the state-of-the-art 60-GHz transceivers.

5.5 Conclusion

This chapter presents a 60-GHz low-power spectrum efficient LOFT-free BPOOK transceiver. This transceiver achieves 3.0 Gb/s data rate while occupies a bandwidth of 3 GHz. The

Table 5.3: Performance Comparison of 60-GHz Transceivers

	Process	Modulation	Integration	Spectrum mask compliance	Data-rate	Sensitivity	Power	Energy efficiency	Chip area
[20]	90nm CMOS	OOK	RF, LO (/wo PLL), Digital IO	NO	3.3 Gb/s	-28dBm†	TX 183 mW RX 103 mW	86.7 pJ/bit	1.11 mm^2
[71]	90nm CMOS	OOK	RF, LO (/wo PLL), Digital IO	NO	10.7 Gb/s‡	-32.5dBm	TX 31 mW RX 36 mW	6.3 pJ/bit	0.44 mm^2
[24]	RFIC/BBIC 65nm/40nm CMOS	16QAM	RF, LO, Analog BB, Digital BB (PHY)	YES	6.3 Gb/s	-55.4dBm†	TX 515 mW RX 650 mW	184.9 pJ/bit	7.7 mm^2
[67]	RFIC/BBIC 90nm/40nm CMOS	QPSK	RF, LO, Analog BB, Digital BB (PHY, MAC, USB 3.0)	YES	1.8 Gb/s*	-78dBm	TX 621 mW RX 1151 mW	984.4 pJ/bit	60.1 mm^2
[68]	65nm CMOS	QPSK	RF, LO, Analog BB, Digital BB (PHY, MAC), PMU	YES	2.6 Gb/s	-	TX 581 mW RX 687 mW	487.7 pJ/bit	16.9 mm^2
This work	65nm CMOS	BPOOK	RF, LO, Digital IO**	YES	3.0 Gb/s	-46dBm	TX 78 mW RX 22 mW	33.3 pJ/bit	1.56 mm^2

* mac data rate
** require external oversampling clock
† estimated from Pout, distance and antenna gain
‡ >21.4 GHz BW

proposed BPOOK modulation eliminates LOFT issue. The transceiver consumes a power of 100 mW with digital baseband interface, which is suitable for 60-GHz low-power short-range wireless.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this research, millimeter-wave transceivers implemented in CMOS technology are demonstrated. The wireless transceivers in millimeter-wave frequencies has the advantages of high bandwidth, high data-rate and small chip size. In the recent 5G New Radio network construction, millimeter-wave bands including 28 GHz and 39 GHz has raised great attention from both telecommunication carriers and the developers. The 5G NR in millimeter-wave bands will provide over ten times data-rate increase than our current 4G cellular network. In order to establish a far distance link between base station and user equipment in millimeter-wave bands, the RF transceivers are required with the characteristics of high output power, high linearity and low noise figure. The linearity in the transmitter is especially important since the transmitter will be driven to as high output power as possible to achieve longer distance and higher system energy efficiency. The main limitation of transmitter linearity is the power amplifier, which is the last stage of the transmitter. The power amplifier is required to be capable of high output power without introducing large waveform distortion. This research proposes power amplifier with current type power combining using high quality factor vertical transformer and modeled transmission line. The main concern on the high linearity power amplifier design lies with the power stage impedance matching. In order to achieve as high output power as possible without decreasing gain characteristic, the transistor size are carefully chosen. In order to achieve a low-loss highly-accurate impedance matching, the proposed power amplifier uses high quality factor vertical transformer and modeled transmission line. The vertical transformer has highest coupling efficiency among the on-chip transformers due to the metal layer can be designed with wide width. Thank to the simpler EM structure and measurement data based transmission line, the proposed power amplifier achieves high

linearity and output power. The standalone power amplifiers are implemented and evaluated by using non-constant high-order modulation signal. The proposed power amplifier achieves highest continuous wave P_{SAT} and highest modulated signal average output power in CMOS technology under low voltage supply.

The millimeter wave phased-array transceivers using proposed power amplifier are investigated and implemented. The antenna array can enhance the signal strength and by phase shifting each TX elements, the phased-array transceiver can steering the beam direction to establish a desired link. Although the antenna array are used, however, the system maximum achievable SNR are the same with one channel link by employing one TX and one RX. The one channel TX and RX are optimized based on the circuit architecture and other limitations, like the chip area, supply voltage, energy efficiency and the signal distribution path. The one transceiver one channel RF characteristics are evaluated by measurement, both TX and RX show good capability of high data rate.

Phased-array transceivers are implemented for 28 GHz and 39 GHz 5G NR bands. The proposed transceiver integrates built-in calibration blocks to enhance the large-array beamforming quality and eliminate the sliding IF architecture LOFT issue. The proposed method is to quantize the phase gain and LOFT signal at lower frequency by reusing a pair of sub-array TX and RX. The proposed method has a phase quantization RMS error of 0.08° and a gain quantization RMS error of 0.01dB. The calibrated phase gain map is written in the register and a highly accurate beam steering can be achieved. In order to satisfy the radiation regulations at undesired bands, the image and LOFT signal are suppressed -50 dBc and -70 dBm respectively. Evaluated by 5G NR modulated baseband signal, the proposed transceiver has a good capability of wideband and high data rate at 39 GHz with a compact packaging, which is a promising solution for 5G NR.

In addition to conventional QAM modulation, a spectrum efficient low power BPOOK modulation scheme is proposed, which has the same spectrum efficiency with QPSK modulation and has the same low power characteristic as OOK modulation. The proposed transceiver operates at 60 GHz with a data rate at 3.0 Gb/s. The proposed BPOOK transceiver solves the intrinsic issue in conventional OOK transceiver, which is a widely used modulation scheme in low power wireless application. First, the data rate is doubled in the same given bandwidth, which enables high speed short distance communication with consuming only 100 mW power. Second, the intrinsic LOFT is cancelled, and makes the spectrum easy to comply with the spectrum mask in wireless standards. Third, it has the same envelope with OOK, which means the proposed BPOOK modulation can be demodulated using the same low power envelope detector and guarantee the overall system energy efficiency. Finally, it requires no analog baseband circuitry such as ADC or DAC, the transceiver is compatible with digital interface, which makes its practical application

easy to implement.

6.2 Future Work

The proposed millimeter-wave transceiver has the advantage of short wave-length and small package size. In the product implementation, the mismatch due to the chip PVT factor or signal distribution path mismatch in package fabrication will degrade the beam-forming quality. The proposed 39 GHz phased-array transceiver with phase gain calibration is introduced in the thesis. The proposed transceiver achieves on-chip calibration phase RMS error of 0.08° and gain RMS error of 0.01 dB. There are several design points or implementation points can be updated to realize a smart auto-calibrated phased-array system.

First, the external calibration including antenna. In order to calibrate the entire phased-array system, two element external calibration method is used to find the phase relationship between transceivers and chips. The external calibration procedure is illustrated as follow shown in Figure 6.1. In order to find the phase relation between each chips, one TX phase and gain is fixed as reference, tune another TX phase at first to find minimum amplitude received in spectrum analyzer. The minimum amplitude between two sinusoid waves $f_1(t) = A \cdot \sin(\omega t)$ and $f_2(t) = B \cdot \sin(\omega t + \varphi)$ are derived as follow: The summed waveform is

$$f(t) = f_1(t) + f_2(t) \tag{6.1}$$

$$= A \cdot \sin(\omega t) + B \cdot \sin(\omega t + \varphi) \tag{6.2}$$

The signal power in one waveform period is:

$$P = \frac{1}{R} \int_0^{\frac{2\pi}{\omega}} f^2(t)\, dt \tag{6.3}$$

$$= \frac{1}{R} \int_0^{\frac{2\pi}{\omega}} (A \cdot \sin(\omega t) + B \cdot \sin(\omega t + \varphi))^2\, dt \tag{6.4}$$

$$= \frac{1}{R\omega} \left(A^2 \cdot \pi + B^2 \cdot \pi + 2AB \cdot \pi \cdot \cos(\varphi)\right) \tag{6.5}$$

The minimum power is at the phase φ that makes $P(\varphi)$ minimum is when the $\varphi = \pi$.

$$P_{min}(\varphi) = P(\varphi = \pi) \tag{6.6}$$

$$= \frac{\pi}{R\omega} (A - B)^2 \tag{6.7}$$

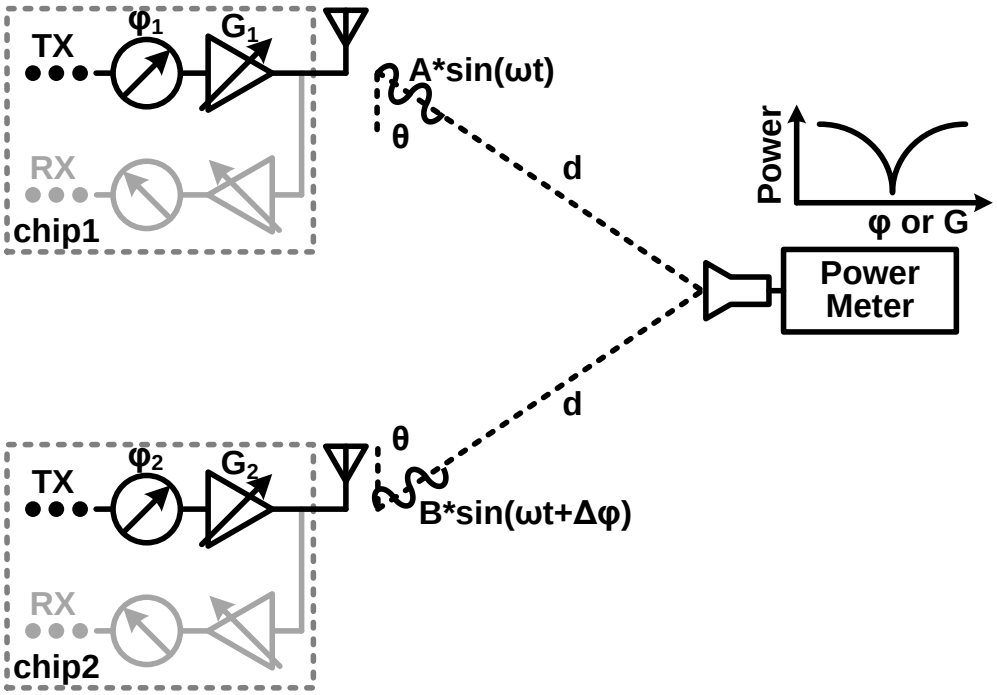


Figure 6.1: External phased gain calibration method.

Equation (6.5) indicates that, whatever two sinusoid wave amplitudes, the condition of two sinusoid wave power summation achieving minimum power and the maximum power are $P_{min} = P(\varphi = \pi)$ and $P_{max} = P(\varphi = 0)$. The derived results are clear and simple. The external calibration is following the two steps. First, set the horn antenna at the center of two transmitter and calibrate the gain to the same level by using the power meter. The second step is by tuning one of the RX phase value to find the minimum power summation, which represents the two wave are with 180° phase difference. By referring the phase map plotted in the register, the desired phase difference can be setup accurately. However, the above mentioned method takes time to setup an external power detector, and requires some human resource to calibrate the chips by order. a automatic global calibration algorithm is preferred during initializing the large array transceiver. The future work can focus on the a auto-calibration algorithm at low frequency instead of calibrating at RF frequency.

The proposed millimeter-wave phased-array transceiver with highly accurate beamforming can be a good candidate for satellite communication. Figure 6.2 shows the two types of current satellite communication. The Geosynchronous Equatorial Orbit (GEO) satellite is orbiting the earth geosynchronously with a constant distance of 36,000 km to the earth. Usually three or four satellites can cover the full area of the earth. However, due

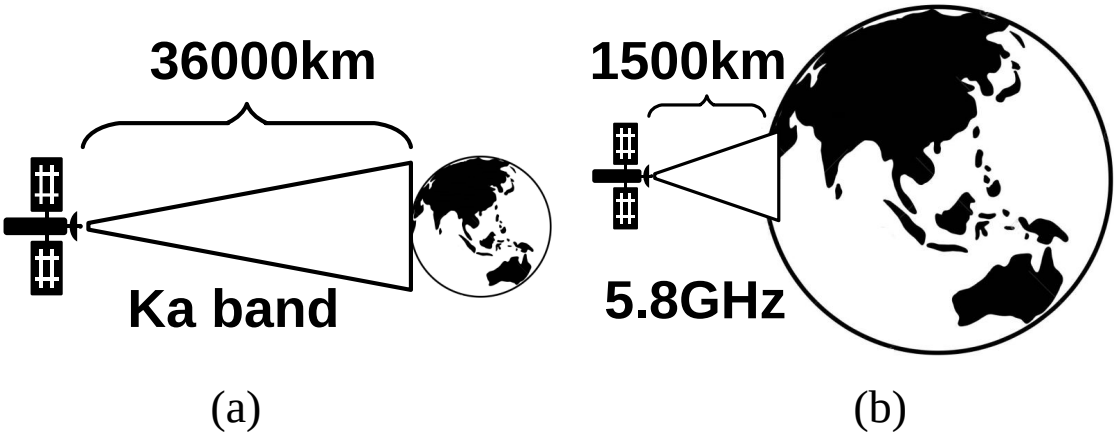


Figure 6.2: (a) Geosynchronous Equatorial Orbit (GEO) satellite, (b)Low Earth Orbit(LEO) satellite.

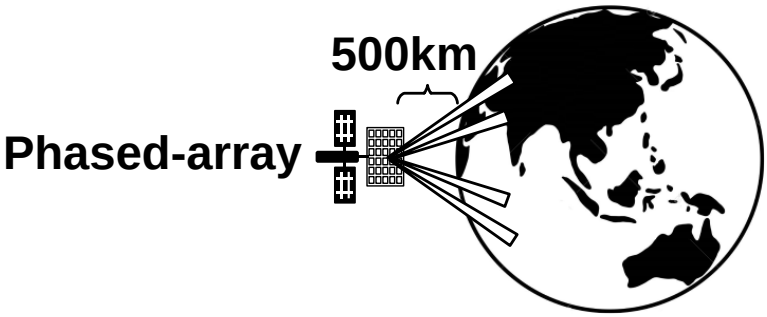


Figure 6.3: LEO satellite communication using phased-array transceiver at millimeter-wave frequency in CMOS technology.

to the very long distance between GEO satellites and the earth, the free space path loss is then very high. Therefore, the communication data rate and the total data capacity are low. Instead of orbiting the earth geosynchronously, the Low Earth Orbit(LEO) satellite has a much closer distance between the earth compared with the GEO satellites. Due to the close distance, the single satellite coverage area becomes smaller, and thousands of satellites can be deployed to cover the whole earth. The free space path loss is not as high as GEO satellites, moderate the data rate can be achieved.

The conventional LEO satellites are usually employing mechanical steering method to change the beam direction. However, the mechanical steering suffers from low flexibility and low accuracy. The proposed phased-array transceiver can be extended to satellite communication in LEO mode. Figure 6.3 shows the scenario of LEO satellite using phased-array transceiver. With further decreased distance, the LEO satellites has a dis-

tance of 500km to the earth, which makes the free space path loss even smaller and the system achievable data rate higher. By deploying tens of thousands of satellites in the low earth orbit, the network capacity is largely improved. Due to the phased-array architecture, the satellites can reach the desired area fast and accurately. The proposed phase gain calibration technique can further enhance the beamforming accuracy for large size array in CMOS technology.

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Appendix A

Publication List

A.1 Journal Papers

- **Yun Wang**, Bangan Liu, Rui Wu, Hanli Liu, Aravind Tharayil Narayanan, Jian Pang, Ning Li, Toru Yoshioka, Yuki Terashima, Haosheng Zhang, Dexian Tang, Makihiko Katsuragi, Daeyoung Lee, Sungtae Choi, Kenichi Okada, and Akira Matsuzawa, "A 60-GHz 3.0Gb/s spectrum efficient BPOOK transceiver for low-power short-range wireless in 65-nm CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, 2019.

- **Yun Wang**, Makihiko Katsuragi, Kenichi Okada, and Akira Matsuzawa, "A 20-GHz differential push-push VCO for 60-GHz frequency synthesizer toward 256QAM wireless transmission in 65-nm CMOS," *IEICE Transactions on Electronics*, Vol. E100-C, No. 6, pp. 568-575, June 2017.

A.2 International Conferences and Workshops

- **Yun Wang**, Rui Wu, Jian Pang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Xi Fu, Daiki Matsumoto, Takeshi Nakamura, Ryo Kubozoe, Masaru Kawabuchi, Bangan Liu, Haosheng Zhang, Junjun Qiu, Hanli Liu, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane and Kenichi Okada, "A 39GHz Phased-Array CMOS Transceiver with Built-in Calibration for Large-Array 5G NR," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, MA, Jun. 2019.

- **Yun Wang**, Rui Wu, Jian Pang, Atsushi Shirane, Kenichi Okada, *IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview*,

San Francisco, CA, Feb. 2019.

- **Yun Wang**, Rui Wu and Kenichi Okada, "A compact 39-GHz 17.2-dBm power amplifier for 5G communication in 65-nm CMOS," *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Melbourne, Australia, Aug. 2018.
- **Yun Wang**, Bangan Liu, Hanli Liu, Aravind Tharayil Narayanan, Jian Pang, Ning Li, Toru Yoshioka, Yuki Terashima, Haosheng Zhang, Dexian Tang, Makihiko Katsuragi, Daeyoung Lee, Sungtae Choi, Rui Wu, Kenichi Okada, and Akira Matsuzawa, "A 100mW 3.0Gb/s spectrum efficient 60GHz bi-phase OOK CMOS transceiver," *IEEE Symposium on VLSI Circuits (VLSI Circuits)*, Kyoto, pp. 298-299, June 2017.

A.3 Domestic Conferences and Workshops

- **Yun Wang**, Bangan Liu, Hiroshi Hamada, Makoto Yaita, Hideyuki Nosaka, Kenichi Okada and Akira Matsuzawa, "300 GHz CMOS-InP transceiver design for 16 QAM data transmission," *IEICE Society Conference*, Sapporo, Hokkaido, C-12-2, Sep. 22, 2016.

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A.4.1 Journal Papers

- Jian Pang, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul Fajri, Tohru Kaneko, Toru Yoshioka, Bangan Liu, **Yun Wang**, Rui Wu, Ning Li, Korkut Kaan Tokgoz, Masaya Miyahara, Atsushi Shirane, and Kenichi Okada, "A 50.1Gb/s 60-GHz CMOS transceiver for IEEE 802.11ay with calibration of LO feed-through and I/Q imbalance," *IEEE Journal of Solid-State Circuits (JSSC)*, 2019.
- Bangan Liu, **Yun Wang**, Jian Pang, Haosheng Zhang, Dongsheng Yang, Aravind Tharayil Narayanan, DaeYoung Lee, SungTae Choi, Rui Wu, Kenichi Okada, and Akira Matsuzawa, "A low-power pulse-shaped duobinary ASK modulator for IEEE 802.11ad compliant 60GHz transmitter in 65nm CMOS," *IEICE Transactions on Electronics*, Vol. E101-C, No. 2, pp.126-134, Feb. 2018.

- Rui Wu, Ryo Minami, Yuuki Tsukui, Seitaro Kawai, Yuuki Seo, Shinji Sato, Kento Kimura, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shotarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Korkut Kaan Tokgoz, Teerachot Siriburanon, Bangan Liu, **Yun Wang**, Jian Pang, Ning Li, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "64-QAM 60-GHz CMOS transceivers for IEEE 802.11ad/ay," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 52, No. 11, pp. 2871-2891, Nov. 2017.

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- Jian Pang, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul

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