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Author(English)	Jeonghoon HAN
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Study on Phase Locked Loop using Injection-Locked Ring Oscillator

Jeonghoon Han

A Dissertation in Partial Fulfillment
of the Requirements for the Degree of
Doctor of Philosophy

Department of International Development of Engineering
Graduate School of Science and Engineering
Tokyo Institute of Technology

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To My Loving Parents

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Abstract

This thesis presents a study on a phase-locked loop (PLL) with an injection-locked ring oscillator. The proposed injection-locked PLL separates the injection-locked ring oscillator from the phase-tracking loop of the PLL such that can provide stable lock-state maintenance and the tolerance to temperature and supply voltage variation. The ideal lock range is also derived under direct injection method in an injection-locked ring oscillator to clarify stable lock state. The measurement results show that the proposed injection-locked PLL has the tolerance to a voltage variation of 11.2% in supply voltage of 1.2 V. In-band noises of the proposed PLL at offset frequencies of 10kHz and 100kHz are -108.2dBc/Hz and -114.6dBc/Hz, respectively.

Moreover, the metastable range detection method is introduced to achieve a balance of frequency coverage of the PLL. Also, the compensation technique to voltage and temperature variation in PLLs with hybrid control is introduced to enhance the tolerance to the variations

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Chapter 1

Introduction

Semiconductor technology has greatly been progressed over the last few decades. It may not be exaggeration that semiconductor technology has also accelerated the development and improvement of other technology and improved many aspects of our lives. Semiconductors allow various electronic devices to be implemented in an integrated chip and to be operated with low power consumption and high speed. These days, the most popular semiconductors would be complementary metal-oxide-semiconductor (CMOS), which is widely used for various systems since it is cheap, small, stable, and less-power hungry.

CMOS is very suitable for digital processing owing to very low static power consumption and also used in analog circuits, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF baseband circuits. Moreover, mixed circuits with both analog and digital systems can be implemented by CMOS in the same wafer [1]. Development of CMOS technology has allowed high speed high resolution analog-to-digital converters (ADCs), high performance baseband circuits, high speed digital signal processors, and so on.

In CMOS integrated circuits, most of systems require periodic signals, called system clocks, generally to synchronize internal components or to sample data. The quality of the system clocks critically affects the performance of many systems. For example, noisy clock generators can increase bite error rate of communication systems and reduce signal-to-noise ratio (SNR) in ADCs [2].

The clock generators in most of integrated circuits are implemented by the frequency synthesizers, such as phase-locked loops employing a crystal oscillator

as a reference, for high performance and stability [3] [4]. With the development of the CMOS technology, the clock generators have also been required to reduce power consumption and cost while maintain the quality of their performances.

This chapter summarizes the process scaling, also called semiconductor scaling, guiding the CMOS technology development. And it reviews challenges in mixed signal circuits. The motivation of this thesis is also introduced.

1.1 Process Scaling

In 1965, Gordon Moore predicted that the number of components on the IC would be roughly double each year, based on the late 1950's and the early 1960's technologies [5]. He also insisted that the increase of the components results in a cost reduction for components. It was not for the long term but for the next 10 years. However, the trend of the increase of components has been continued for the last few decades [6] - [13]. The increase of components has been mainly achieved by the device scaling. In 1974, the scaling method of the circuit was proposed by Dennard as shown in Table 1.1 [17]. Even though the limit and the future of scaling have been discussed for long time [6]- [16], Iwai expected that the scaling would be continued until the gate length of around 5nm, which is supposed to be the physical limit [13].

Table 1.1: Scaling results for circuit performance

Device or circuit parameter	Scaling factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration Na	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Figure 1.1 shows load map for gate length and cut-off frequency, f_T, based on the scaling of CMOS processes in ITRS 2011 [21]. CMOS scaling provides

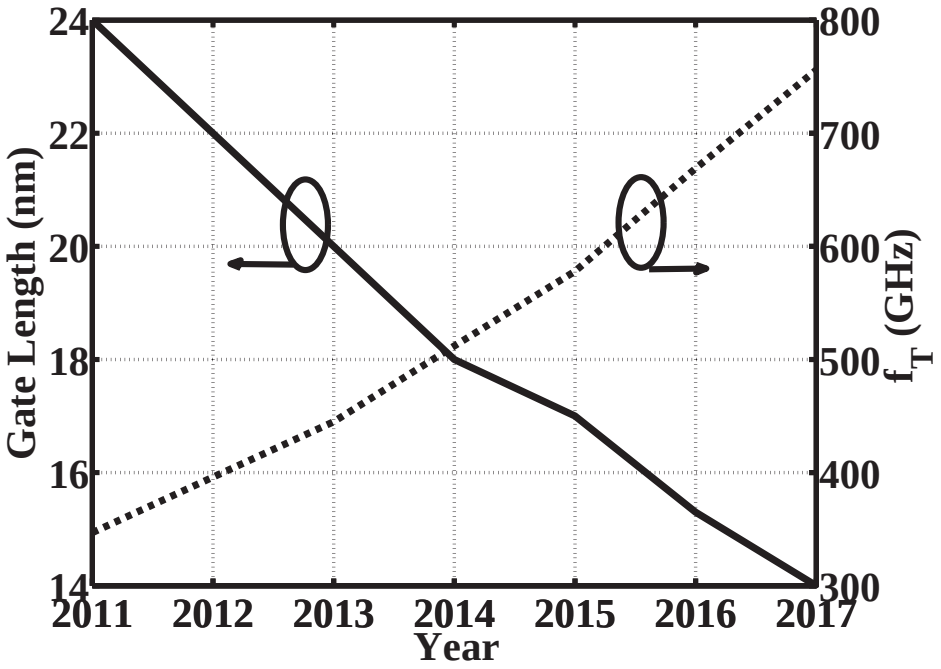


Figure 1.1: ITRS load map for gate length.

digital circuits with a few benefits [8] [18]. When gate length is reduced, gate capacitance, C_{GS}, is also reduced and its cut-off frequency is increased since it is inversely proportionally to gate capacitance [22].

$$f_T = \frac{gm}{2\pi C_{GS}} \tag{1.1}$$

It allows faster circuits. And chip area decreases such that the cost of the circuit can be reduced and power consumption too.

$$P_{digital} = CV_{DD}^2 f \tag{1.2}$$

Power consumption, $P_{digital}$, in digital circuits is also reduced since the power supply voltage, V_{DD}, has been reduced as well as the reduction of the gate length, even though the rate of the voltage supply reduction is not as large as the rate of the gate length reduction [6].

1.2 Analog and Digital Circuits

One of advantages of CMOS process can implement analog and digital circuits in one wafer. In these days, many kinds of communication systems have been implemented together with digital circuits in CMOS process.

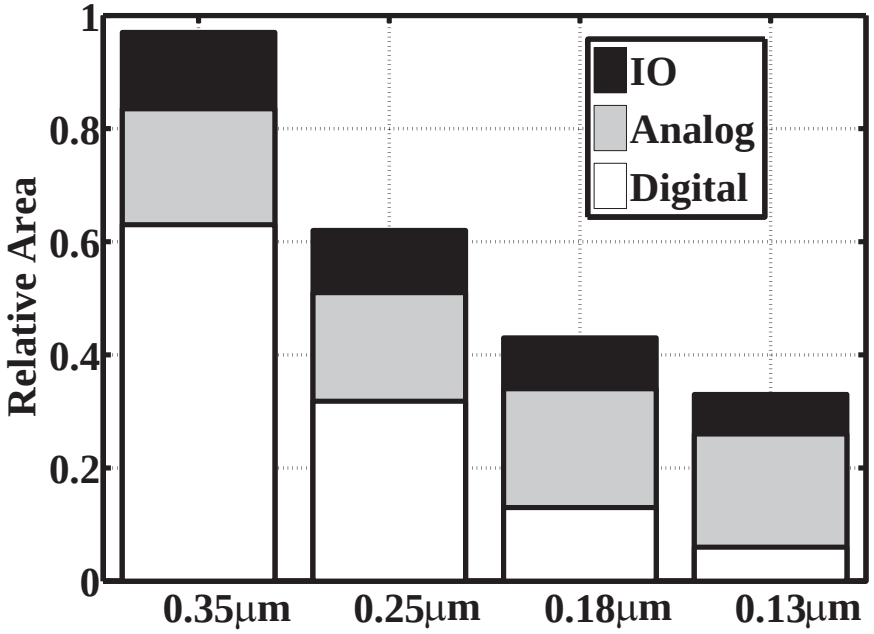


Figure 1.2: Chip area in a system-on-chip (SoC).

As well as digital circuits, the device scaling provides analog circuits with some benefits, such as the reduction of the minimum noise figure of a MOSFET and the improvements of the quality factor of MIM (Metal-Insulator-Metal) capacitor [18]. However, analog circuits do not have benefits from the process scaling as much as digital circuits. The intrinsic gain is reduced and the gap between pre- and post-layout simulation results is widen as the devices are scaled down [19] [20]. Area sharing ratio of analog circuits in a chip becomes larger. Figure 1.2 shows chip area when the mixed signal system-on-chip (SoC) is fabricated in the CMOS process [23]. As the process scaling proceeds, the whole area becomes small but the chip sharing ratio of analog circuits increases since the passive circuits, such

as inductors and capacitors, are hardly scaled down with the process scaling. Especially, inductors require large area.

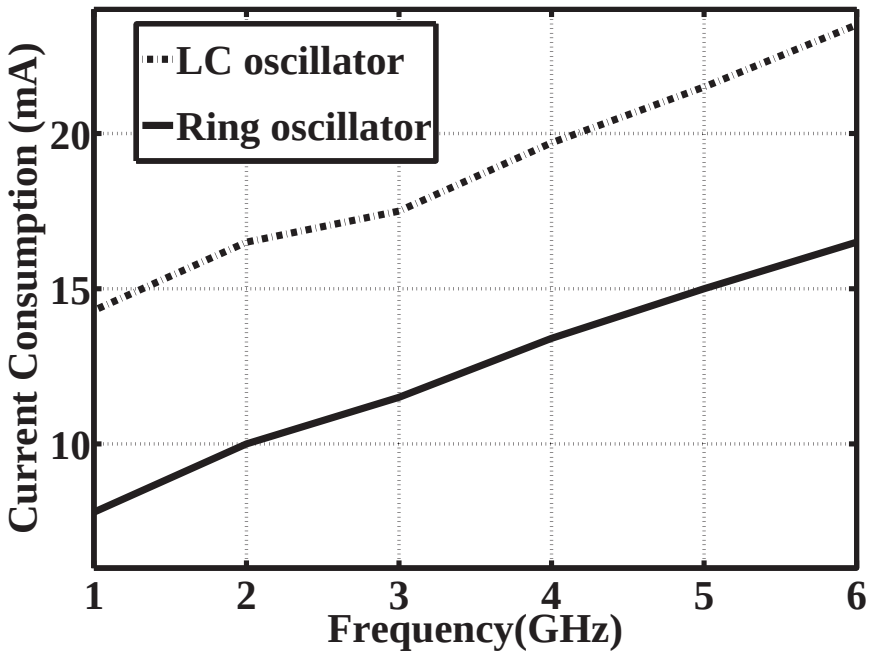


Figure 1.3: Comparison between current consumptions of LC and ring oscillators.

In the view of chip area, performance, and power consumption, there is very big difference between analog circuits with or without inductors. Let us give an example of design of a clock generator. When the clock generators are designed for the system, one of two major types of oscillators is generally selected. One is LC oscillators and the other is ring oscillators. LC oscillators are composed of LC resonant circuit and have low noise characteristic than other oscillators. Ring oscillators have poor noise characteristics such that they are seldom used for the systems requiring high purity oscillation frequency. However, ring oscillators have several advantages compared to LC oscillators. They have wide tuning range, low power consumption, and small occupied area. Figure 1.3 shows comparison of power consumption between the ring oscillator and the LC oscillator fabricated in 90nm CMOS process [24]. Both increase current consumption as the oscillation frequency increases. However, the LC oscillator consume the current about 2.5

times larger than that of the ring oscillator. Power consumption becomes more important in mobile systems using battery.

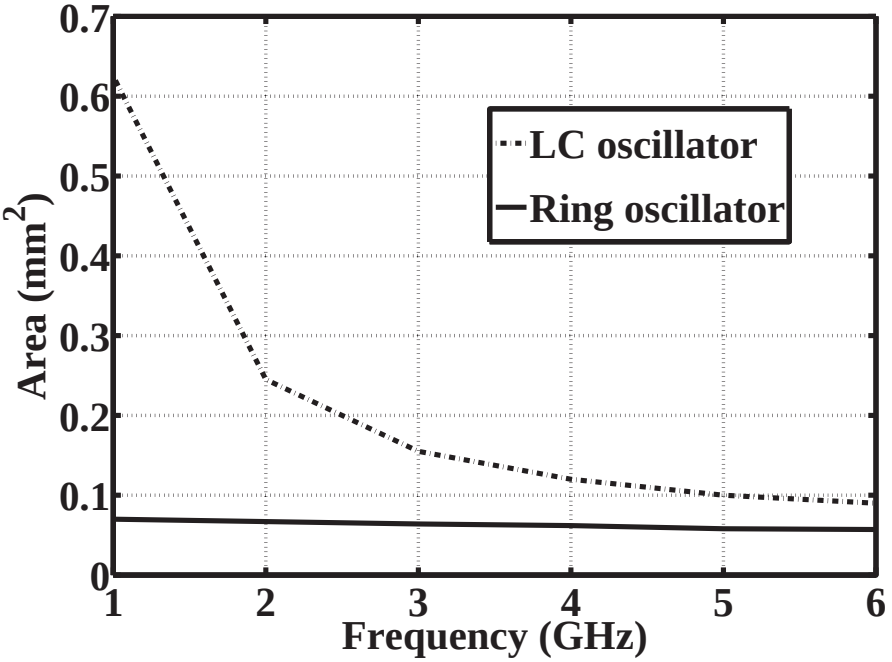


Figure 1.4: Comparison between occupied chip areas of LC and ring oscillators.

Figure 1.4 shows comparison of occupied area between the two oscillators. As the oscillation frequency increases, the occupied area of the LC oscillator decreases while the area of the ring oscillator looks almost same. Since the oscillation frequency of the LC oscillator is inversely proportional to the inductance, the area of the LC oscillator becomes small as the oscillation frequency increases. It is thus considered that LC oscillators will be preferred as high frequency clock generator in fine CMOS process without any restriction of power consumption. In the case of the relatively low oscillation frequency, for example, around 1GHz, it is not easy to select one between ring and LC oscillators. Considering the power consumption, chip area, and tuning range, the ring oscillator is suitable. But the phase noises of the ring oscillators is hard to reach the LC oscillators theoretically [25]. On the other hand, the LC oscillator has better phase noise characteristics but requires large area and has a limited tuning range.

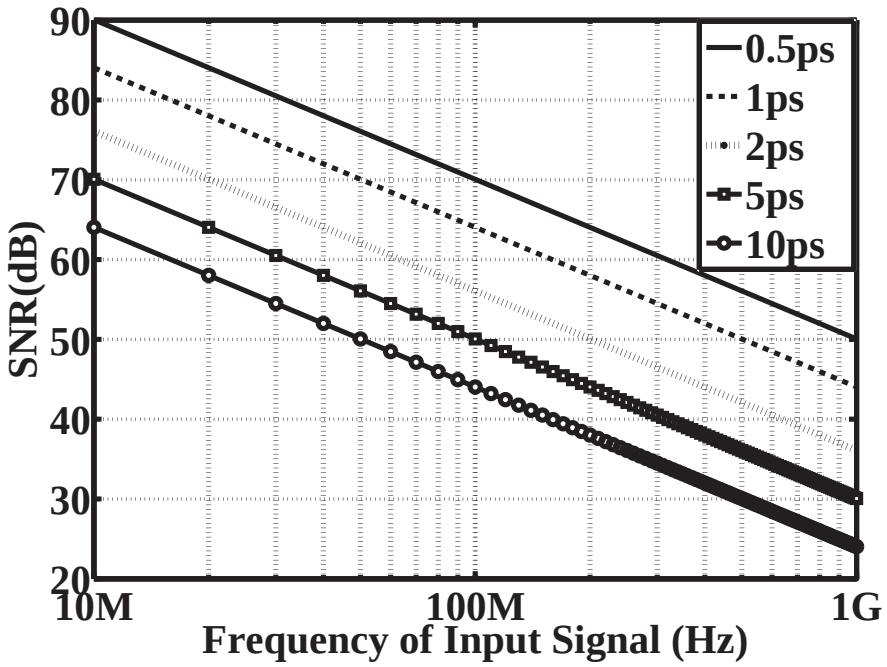


Figure 1.5: Signal-to-noise ratio (SNR) of an ADC due to the clock jitter.

Relatively low frequency clock generators with low phase noise is generally required for analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Figure 1.5 shows signal-to-noise ratio (SNR) of an ADC due to the clock jitter [26]. When the clock has any timing disturbance during sampling operation of an ADC, it generates error in the sampled data and directly effects performance of the ADC.

Figure 1.6 shows SNR due to the clock jitter in a 7-bit 1Gsps ADC [2]. When the frequency of the input signal is low, the clock jitter seldom affects performance of the ADC. However, when the frequency of the input signal goes higher, the SNR of the ADC goes down rapidly. For input signal with one-half the sampling frequency, the clock jitter should be below 2ps. Thus, the clock jitter is very important factor for the performance of the ADCs and DAC.

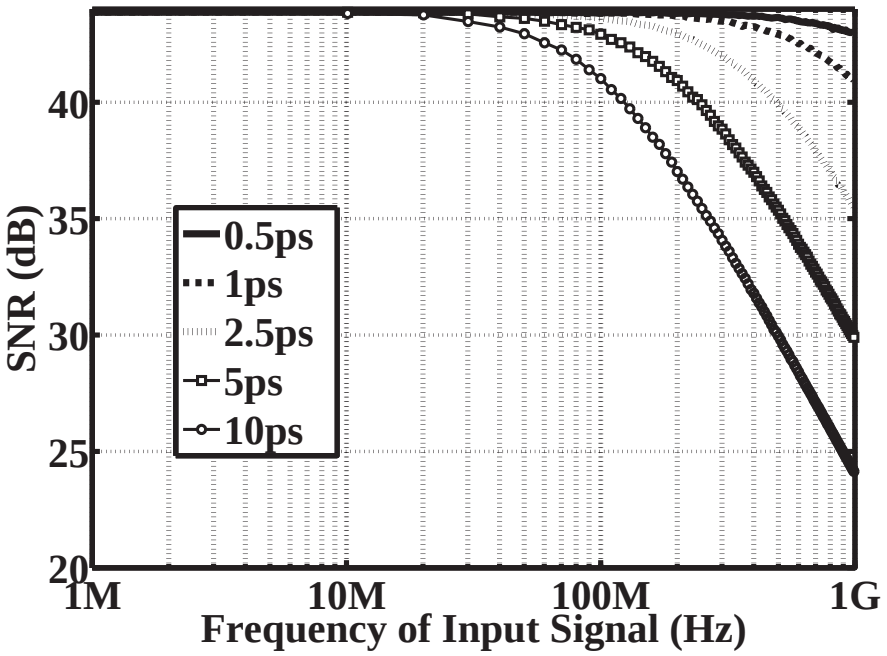


Figure 1.6: SNR due to the clock jitter in a 7-bit 1Gsps ADC.

1.3 Motivation and Thesis Organization

1.3.1 Motivation

The scaling of CMOS technology allows faster circuits, small chip areas, and low power consumption for many systems. However, not every system requires a high frequency clock as high as the frequencies required in RF circuits. When LC oscillators are implemented as a clock generator with a frequency around 1GHz in a fine CMOS process, very large area and power consumption are accompanied. On the other hand, ring oscillators can not provide good noise characteristics as low as the LC oscillator.

This thesis focuses on the relatively low frequency oscillators with low noise characteristic and small occupied area. Recently, injection-locked oscillators as frequency multipliers are rising again [27] - [32]. Injection-locked oscillators generally have been used to be not frequency multipliers but frequency dividers [33] - [36]. There are two kinds of injection-locked oscillators. One is based on ring

oscillators and the other is LC oscillators. The injection-locked LC oscillators require large area as same as LC oscillators but injection-locked ring oscillators do not. When they are locked, the phase noise of the injection-locked oscillators tend to follow the low phase noise of the reference. However, there are a few challenge in using the injection-locked ring oscillators as a frequency multiplier. First of all, it is difficult to achieve high multiplication ratio. The second is that the lock range is still ambiguous. The third is that it is very weak to the voltage-temperature variations.

Thus, this thesis discusses about a maximum lock range of an injection-locked ring oscillator and an injection-locked charge-pump phase-locked loop to maintain the stable lock state.

1.3.2 Thesis Organization

In chapter 2, fundamentals of oscillators and the phase locked loop are described and the trade-offs in selecting oscillators for the phase-locked loop is discussed. In chapter 3, an ideal lock range of an injection-locked oscillator used as a frequency multiplier is derived. In chapter 4, it is introduced that an injection-locked ring oscillator is embedded in the charge pump phase-locked loop. Chapter 5 describes lock detection technique in a lock controller and how to enhance the tolerance to voltage-temperature variations in the injection-locked phase-locked loop. In chapter 6, a summary of this thesis is presented with the future works.

Chapter 2

Phase-Locked Loops

In submicron processes, design of frequency synthesizer in relatively low frequency, for example around 1GHz, looks facile since much more higher frequency synthesizers can be implemented. However, considering some required specifications for the frequency synthesizers, such as power consumption, occupied chip area, and low phase noises, it is difficult and tricky for the designer to handle trade-offs among them. When it is implemented in more fine processes, it becomes more tricky. PLLs are widely used in many systems which requires clock generator since they can provide stable high frequency signal. This chapter describes the noise in the clock generators and clarifies the trade-offs in design of the PLLs after basic concepts of their components are presented.

2.1 Jitter and Phase Noise

All electric systems suffer undesired noises. An ideal clock generator outputs a certain signal waveform with a fixed period or frequency. However, real clock generators provide output signals of which periods or frequencies fluctuate around fixed ones as shown in Fig. 2.1. The clock generator can be an oscillator or a system including the oscillator, such as phase-locked loop. The clock generators with excessive noise will increase the bit error rate in communication systems or malfunction in digital systems. First of all, in order to avoid such undesired conditions, stability of the oscillators must be considered. Stability of the oscillators

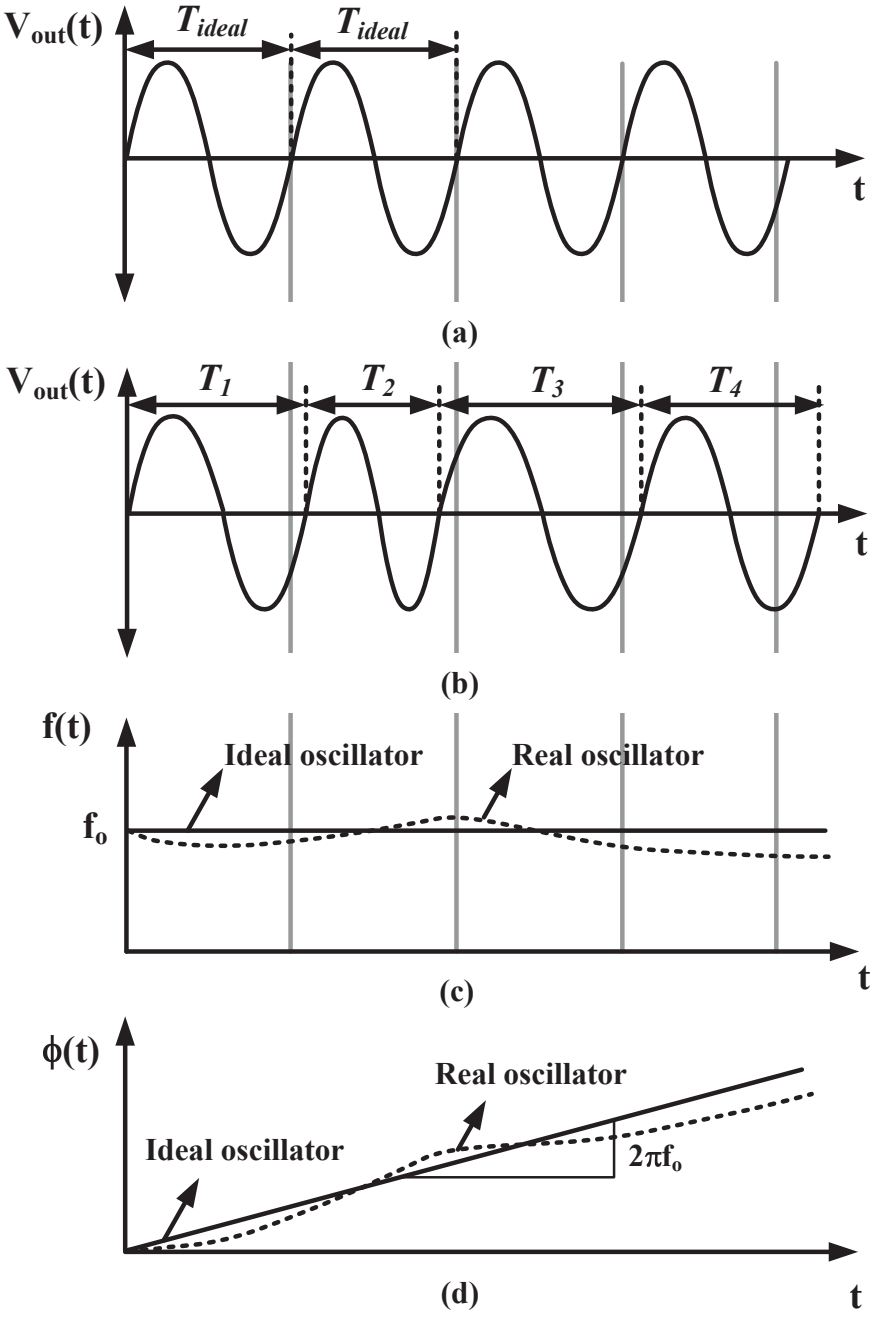


Figure 2.1: Free running outputs of (a) an ideal oscillator and (b) a real oscillator, and (c) the output frequencies and (d) phases of the oscillators.

for systems are generally quantified by two means. One is observed in the time domain and the other is in the frequency domain.

The instability of the clock in time domain is called timing jitter. Jitter is specified by statistical terms since it has a random characteristic. Two kinds of timing jitters are widely used. One is a period-jitter and the other is a cycle-to-cycle jitter. A period jitter, ΔT_p, as shown in Eq. 2.1 is a change of the period from an ideal period and generally used to calculate timing margin in digital systems [37].

$$\Delta T_p = T_k - T_{ideal} \tag{2.1}$$

Its RMS (root-mean-square), σ_p, is expressed as following:

$$\sigma_p^2 = \lim_{N\to\infty} \frac{1}{N} \sum_{k=1}^{N} (\Delta T_p)^2 \tag{2.2}$$

Cycle-to-cycle jitter, ΔT_{c2c}, is a deviation in the period between two adjacent periods as shown in Eq. 2.3 [38].

$$\Delta T_{c2c} = T_{k+1} - T_k \tag{2.3}$$

The RMS of the cycle-to-cycle error, σ_{c2c}, is

$$\sigma_{c2c}^2 = \lim_{N\to\infty} \frac{1}{N} \sum_{k=1}^{N} (\Delta T_{c2c})^2 \tag{2.4}$$

Figure 2.1 shows the characteristics of a noiseless and a noisy oscillators with sinusoidal waveforms. The ideal oscillator outputs $Asin(2\pi f_o t)$ but a noisy oscillator does $Asin(2\pi f_o t + \phi_n)$. ϕ_n is a noise component called jitter. The change of the transition of the oscillators in the time domain results in fluctuation of the oscillation frequency in the frequency domain as shown in Fig. 2.1(c). Thus, its spectrum looks skirt around the ideal oscillation frequency as shown in Fig. 2.2. ϕ_n is also a noise component to modulate the phase of the oscillator in the frequency domain. Thus, phase noise is used to evaluate the stability of the oscillator in the frequency domain. Phase noise, $L(\Delta f)$, is defined as the ratio of the noise power in a 1 Hz bandwidth at a certain frequency offset, Δf, to the signal

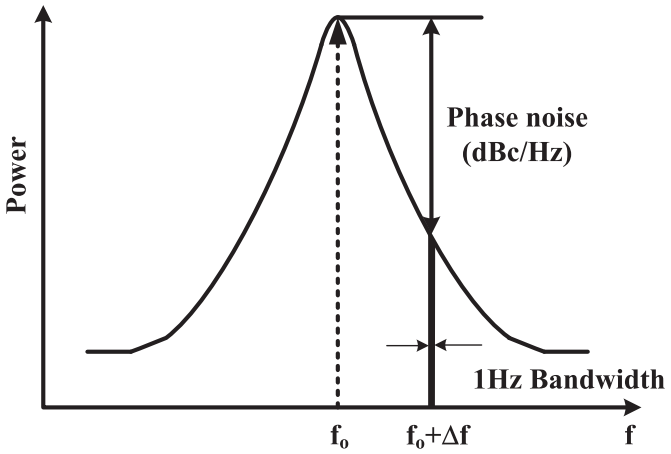


Figure 2.2: Definition of phase noise.

power at a carrier frequency, f_o.

$$L(\Delta f) = 10log\{\frac{\text{noise power in a 1 Hz bandwidth at frequency offset}}{\text{power at a carrier frequency}}\}[\text{dBc/Hz}] \tag{2.5}$$

Phase noise is a very important factor to evaluate the purity of the oscillators or frequency synthesizers since phase locked loop is generally designed in the frequency domain. Figure 2.3 shows the characteristic of the phase noise in the oscillators. In the low offset frequency, the phase noise is inversely proportional to the frequency. Especially, the phase noise with a 30dB/decade slope is associated with the flicker noise which is the dominant noise source at low frequencies in silicon MOSFETs. The flicker noise is expressed by the fluctuation of the channel free carriers due to the random capture emission or the fluctuations in the surface potential. It is mainly dominated in NMOS by carrier-density fluctuation and in PMOS by mobility fluctuation [53]. Thus, it can be roughly modeled as two dominant approaches [52]. The first approach provides a power spectral density $S_{nf}(f)$, of the equivalent input noise voltage appearing in series with the gate.

$$S_{nf}(f) = \frac{K}{C'^2_{ox} W L} \frac{1}{f} \tag{2.6}$$

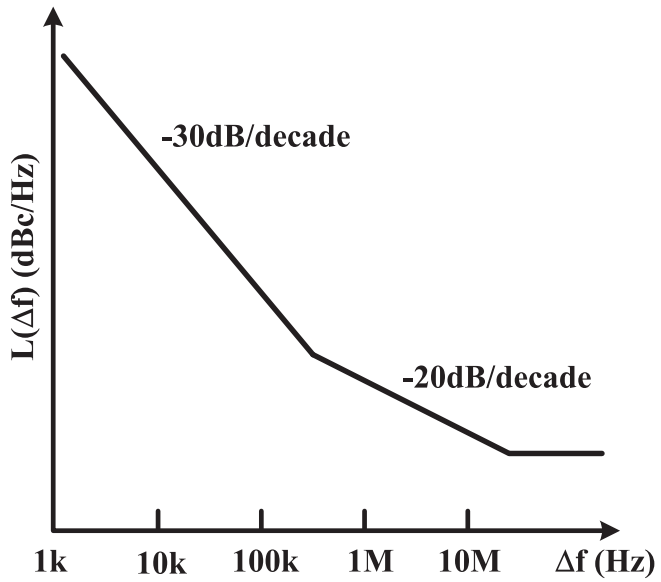


Figure 2.3: Phase noise of an oscillator.

where K is process-dependent coefficient, C'_{ox} oxide capacitance per unit area, and W and L the channel width and length. This equation is suitable for NMOSs since flicker noise of the n-channel devices have independence on the gate bias voltage. Another approach is for PMOSs providing a power spectral density for the equivalent input noise voltage, which depends on the gate bias voltage.

$$S_{nf}(f) = \frac{K(V_{GS})}{C'_{ox}WL}\frac{1}{f} \tag{2.7}$$

where K is bias-dependent coefficient. In oscillators, the flicker noise is up-converted to the oscillation frequency and is dominant in $1/f^3$, region of phase noise [54].

2.2 Oscillators

In electronic systems, two kinds of oscillators are widely used. One is LC oscillators and the other is ring oscillators. In this section, their characteristics are investigated. Furthermore, injection-locked oscillators are also described. The

injection-locked oscillators are generally used as frequency dividers. A few papers presented that the injection-locked oscillators are used as frequency multipliers.

2.2.1 LC Oscillators

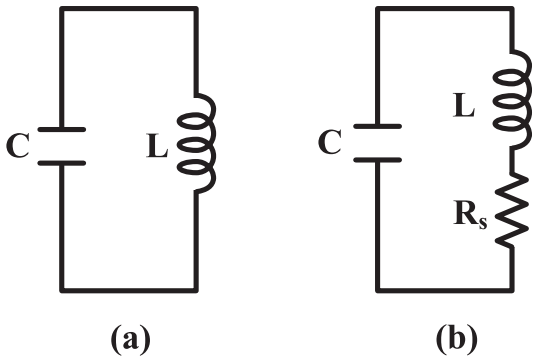


Figure 2.4: (a) Ideal LC resonant tank (b) resonant tank with parasitic resistance.

LC oscillators are a type of the most widely used oscillators in CMOS technology since they have low phase noise characteristic than other oscillators. The LC oscillator is composed of resonant component of inductor and capacitor as shown in Fig. 2.4 [39]. Its resonant frequency depends on inductance and capacitance. Resonant tank has an infinite impedance at the resonant frequency such that the oscillator outputs a periodic signal. The resonant frequency is obtained as following:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.8}$$

Since a real inductor has series parasitic resistance as shown in Fig. 2.4 (b), the real resonant tank composed of only an inductor and a capacitor outputs not a periodic signal but a decaying signal. The series parasitic resistance can be replaced with the parallel parasitic resistance as shown in Fig. 2.5 (a) [40]. The parallel parasitic resistance, R_p, can be expressed by the series parasitic resistance, R_s, and the quality factor, Q, of the inductor.

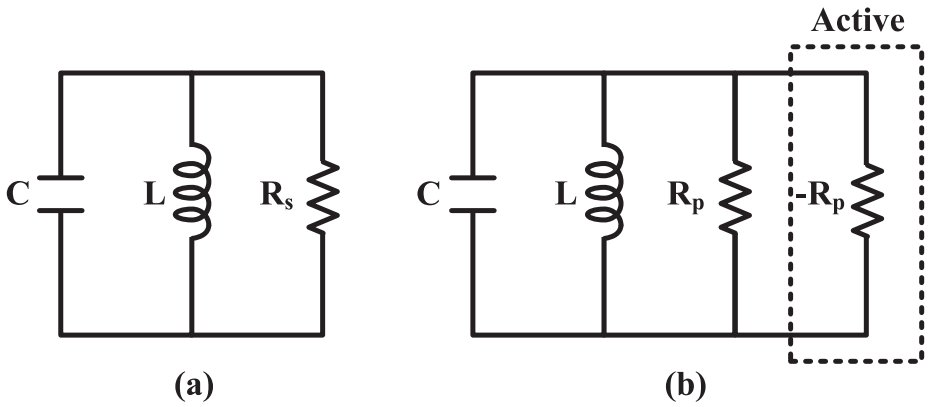


Figure 2.5: (a) Resonant tank with a parallel parasitic resistance (b) resonant tank with a negative resistance.

$$R_p = (Q^2 + 1)R_s \qquad \text{where } Q = \frac{R_p}{X_p} \tag{2.9}$$

where X_p is a shunt reactance. When negative resistance is connected to the resonant tank in parallel as shown in Fig. 2.5 (b), the resonant tank will recover infinite impedance at the resonant frequency. The negative resistance can be implemented by cross coupled transistors and its value is determined by the transconductance.

Widely used LC oscillator has cross coupled negative resistance as shown in Fig. 2.6 [41]. It is possible to be implemented only with NMOS or PMOS cross coupled negative resistance. The phase noise spectrum, $L(\Delta\omega)$, of the LC oscillator can be expressed as following [42]:

$$L(\Delta\omega) = 10log[\frac{2FkT}{P_{sig}}\{1 + (\frac{\omega_o}{2Q\Delta\omega})^2\}(1 + \frac{\omega_{1/f^3}}{|\Delta\omega|})] \tag{2.10}$$

where F is fitting factor to account for excess noise in all regions. The phase noise of the LC oscillators mainly depends on the quality factor, Q, of the LC tank and the signal power, P_{sig}.

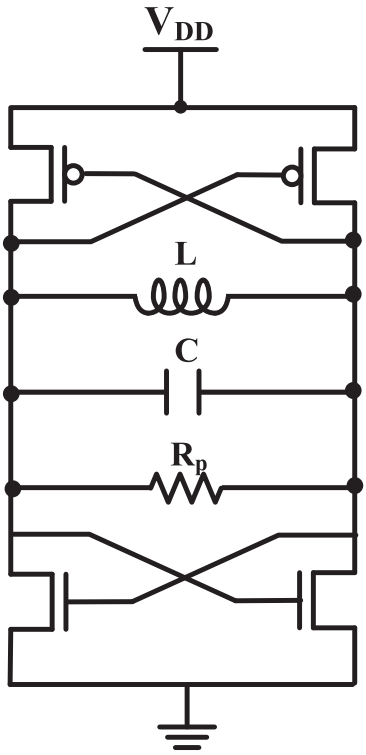


Figure 2.6: Complementary LC oscillator.

2.2.2 Ring Oscillators

A different type of most widely used oscillators is a ring oscillator since it has less occupied area, wide tuning range, and low power consumption. Figure 2.7 shows a 3-stage inverter-based ring oscillator. Its oscillation frequencies are generally controlled by the current sources, which can be only one between top or bottom ones. Inverter-based ring oscillators are composed of odd-stage inverters. An inverter basically outputs the reversed voltage of its input voltage. As shown in Fig. 2.7, the input of the first stage is high but the output of the third stage is low. When the input of the first stage is connected to the output of third stage, the inverter chain becomes unstable and then oscillates. That is, an unstable state results in a stable oscillation.

The ring oscillator has a very simple structure. However, it is not easy to achieve an accurate oscillation frequency estimation since it has not any resonant

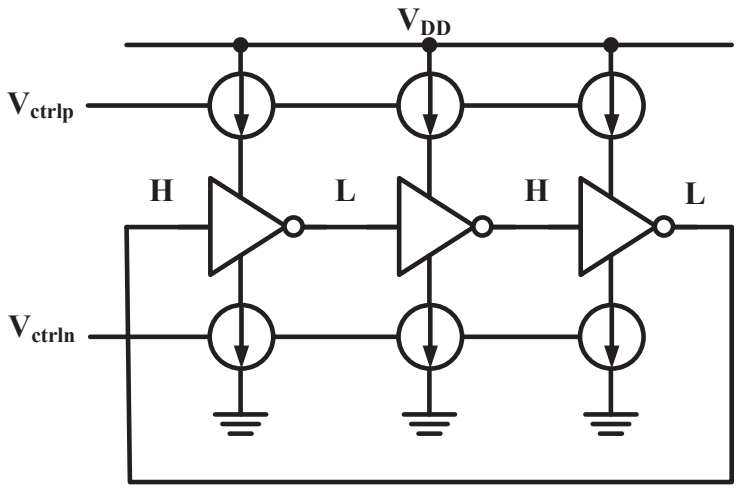


Figure 2.7: Inverter-based ring oscillator.

components unlike LC oscillators. Oscillation of ring oscillators is substantially based on amplification of MOSFETs and RC delays. Since MOSFETs are inherently nonlinear active devices, analyses of them are not facile. However, they can be linearly analyzed under the restricted condition called small signal analysis, which the gate bias is fixed and the input and output signals are very small enough to be linearized. However, ring oscillators have large input and output signals, generally from ground to the supply voltage, called full swing. The small signal analysis is not useful for analysis of the ring oscillator. Moreover, they change in time. In other words, ring oscillators are a nonlinear and time variant system. Thus, accurate analysis of them is quite tricky.

The oscillation frequency estimation of the ring oscillator is mainly performed by two approaches. The first approach is to use charging and discharging mechanism of a capacitor. A simple circuit model of the inverter is shown in Fig. 2.8 [43]. The load capacitor, C_L, is parasitic capacitor at the output of the inverter stage. An additional capacitance can be also loaded at the output node. The current, I_{ctrl}, is controlled by the control voltages, V_{ctrlp} and V_{ctrln}, which are gate bias voltages of the NMOS or PMOS used to be current sources. When the capacitor is charged as shown in Fig. 2.8 (b), the current, I_{ctrlp}, is as following:

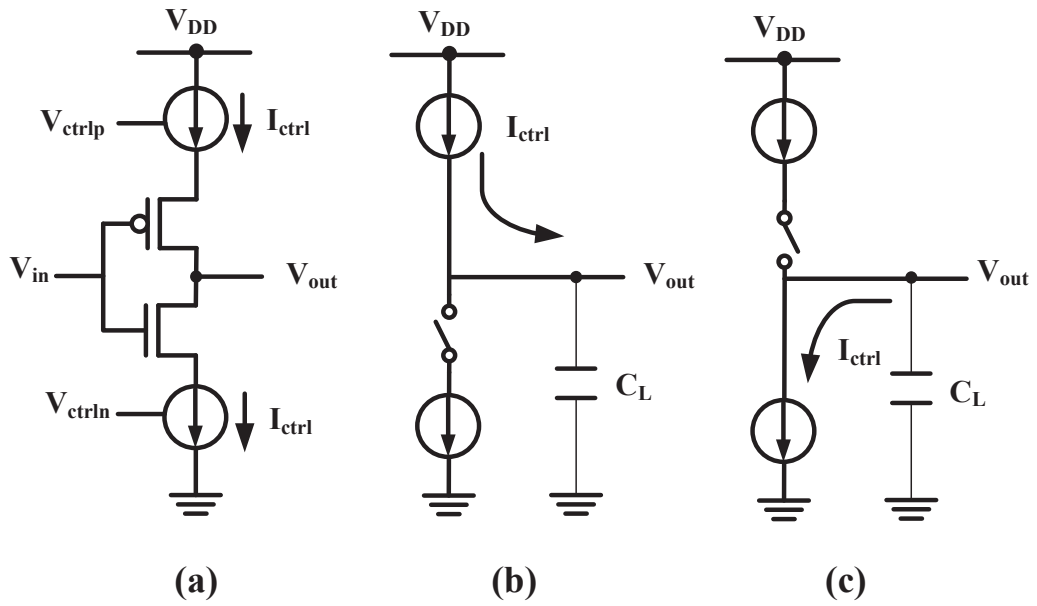


Figure 2.8: (a) Delay stage of the inverter-based ring oscillator, and a simple circuit model to estimate (b) rising and (c) falling delays.

$$I_{ctrlp} = \frac{\mu_p C_{oxp}}{2} \frac{W_p}{L_p} (V_{ctrlp} - V_{thp})^2 \tag{2.11}$$

where V_{thp} is a threshold voltage of the PMOS, μ_p is a mobility of a carrier, C_{oxp} is an oxide capacitance, and W_p and L_p are the channel width and length, respectively. Thus, the rising time, t_r, is $C_L V_{DD}/I_{ctrlp}$ and can be rewritten as following:

$$t_r = C_L V_{DD} \frac{2L_p}{W_p \mu_p C_{oxp}} \frac{1}{(V_{DD} - V_{thp})^2} \tag{2.12}$$

When the capacitor is discharged as shown in Fig. 2.8(c), the falling time, t_f, can be also obtained by the same method. Thus, the oscillation frequency. f_{OSC}, of a N-stage ring oscillator can be estimated as following:

$$f_{OSC} = \frac{1}{N(t_r + t_f)} \tag{2.13}$$

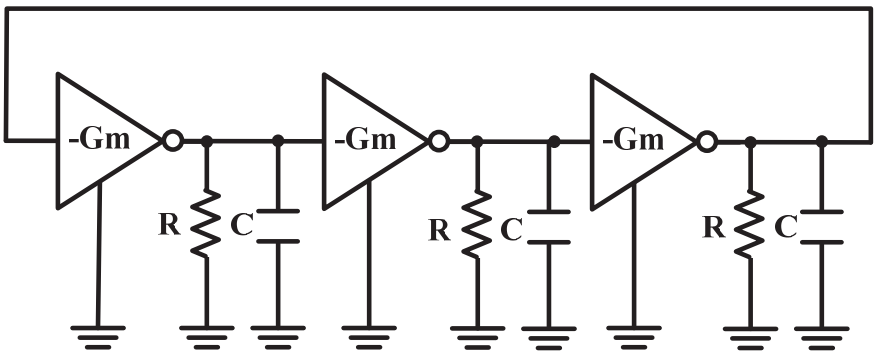


Figure 2.9: Linear model of the ring oscillator.

The other approach for the oscillation frequency estimation is to linearize a delay cell with Gm cell and RC load in the case of a 3-stage differential ring oscillator [44]. Figure 2.9 shows a linear model of the ring oscillator. The oscillation frequency of a 3-stage ring oscillator is as following:

$$f_{OSC} = \frac{\sqrt{3}}{2\pi RC} \tag{2.14}$$

The oscillation frequency can be also estimated by considering currents in the delay stage and time-varying characteristics of parasitics and the gate resistance [45], or by analyzing a ring oscillator as a nonlinear feedback system [46].

Phase noises of the inverter-based ring oscillator were introduced in [25]. They were modeled by producing a voltage ramp at its output in response to a correctly positioned step input. The phase noises, $L_{ring,1/f}(f)$ and $L_{ring,white}(f)$, due to flicker and white noises, are respectively

$$L_{ring,1/f}(f) = \frac{C'_{ox}}{8MI}\left(\frac{\mu_N K_{fN}}{L_N^2} + \frac{\mu_P K_{fP}}{L_P^2}\right)\frac{f_o^2}{f^3} \tag{2.15}$$

$$L_{ring,white}(f) = \frac{2\mathrm{kT}}{I}\left(\frac{1}{V_{DD} - V_t}(\gamma_N + \gamma_P) + \frac{1}{V_{DD}}\right)\left(\frac{f_{OSC}}{f}\right)^2 \tag{2.16}$$

where I is a pull-up current charging an inverter's load C to V_{DD}, μ_N and μ_N are carrier mobilities of NMOS and PMOS respectively, K_{fN} is the empirical coefficient, K_{fP} is a bias-dependent quality, f_o is oscillation frequency, V_t is the

threshold voltage, and γ_N and γ_P are noise factors of NMOS and PMOS, respectively. These equations show that the low phase noise can be obtained by the longest channel length and the larger current consumption.

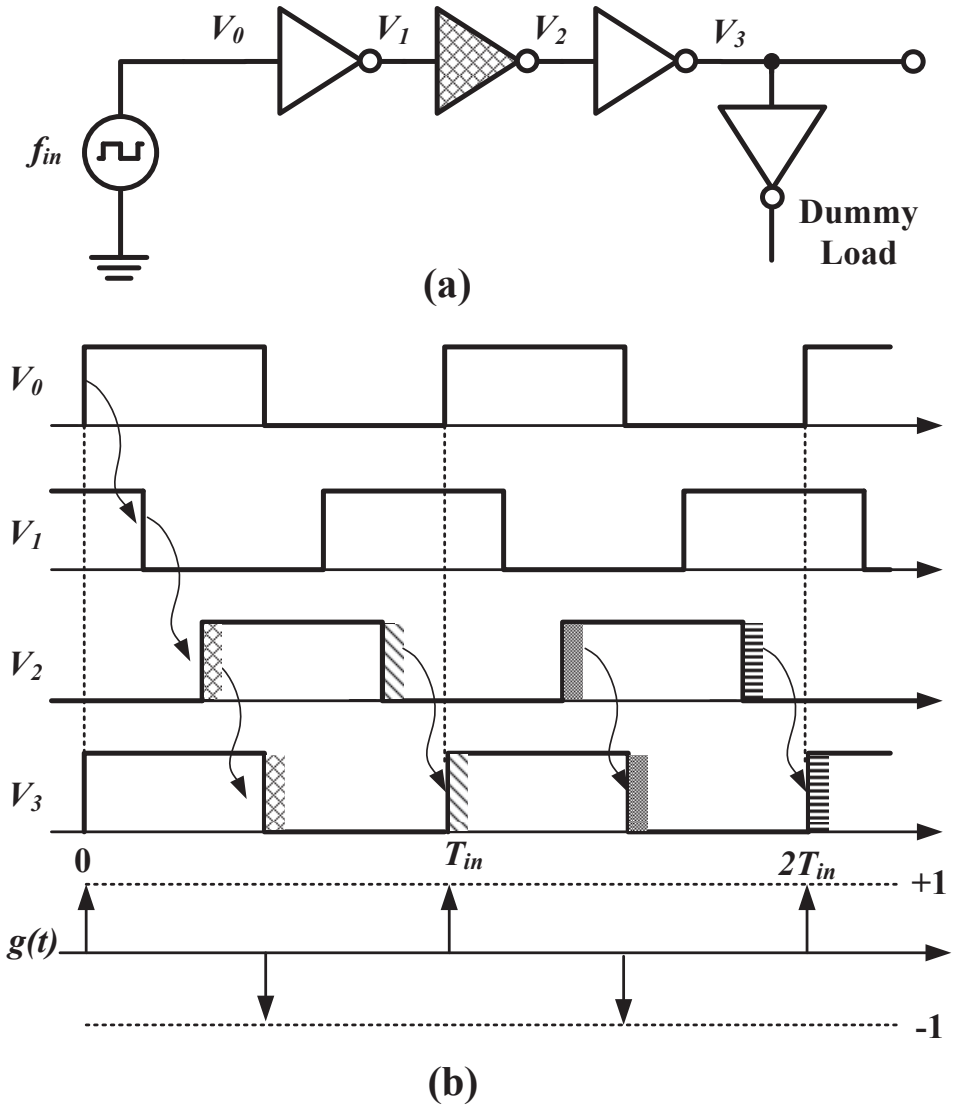


Figure 2.10: (a) Delay line with only one noisy stage and (b) waveforms of the delay line.

Another phase noise model can be derived from phase noise of a delay line multiplying a shaping function [47]. Figure 2.10 shows three-stage delay line with

only one noisy inverter and node voltages at each output. Under a certain input frequency, the output voltage of the latter stage has more large noise since it suffers all uncorrelated noises of the previous stages. Homayoun obtained the two-sided phase noise, $S_{\Phi,DL}$, of the delay line from uncorrelated jitters on the rising and falling edges and derived the phase noise. Homayoun's approach is to obtain the phase noise of the delay line with only one noisy stage and the overall phase noise of the delay line by multiplying the phase noise of the one noisy stage with the number of delay stages. The two-sided phase noise, $S_{\Phi,white,DL}$, due to white noise and the two-sided phase noise, $S_{\Phi,1/f,DL}$, due to 1/f noise in N-delay line are respectively

$$\begin{aligned} S_{\Phi,white,DL} &= \frac{\pi^2}{2I_D^2}\left[S_I(f)|_{NMOS} + S_I(f)|_{PMOS}\right] \\ &\quad + \frac{2kT\pi^2}{I_D V_{DD}} \qquad (2.17) \\ S_{\Phi,1/f,DL} &= \frac{\pi^2}{4NI_D^2}\left[S_{1/f}(f)|_{NMOS} + S_{1/f}(f)|_{PMOS}\right] \qquad (2.18) \end{aligned}$$

where $S_I(f)$ is the thermal noise current, $S_{1/f}(f)$ is the flicker noise current, k is the Boltzmann constant, T is the absolute temperature, I_D is the drain current of the on-transistor, and V_{DD} is the supply voltage.

Homayoun's model for the phase noise of the ring oscillator also assumed that the only second stage inverter has noise. And it investigated the effect on the output of the stage as shown in Fig. 2.11. Contrary to the delay stage, the ring oscillator accumulates the previous jitters as shown in Fig. 2.11 (b). The output waveform was thus obtained by convoluting the noise sources with g(t) and adding it to an ideal wave. The phase noise, $S_{\Phi,ring}$, of the ring oscillator shown in Fig. 2.11 (a) was obtained by multiplying the phase noise of the delay line with the shaping function, $G(f)$.

$$\begin{aligned} S_{\Phi,ring}(\Delta f) &= S_{\Phi,DL}(\Delta f)|G(f)|^2 \qquad (2.19) \\ &= \left(S_{\Phi,white,DL} + S_{\Phi,1/f,DL}\right)\left(\frac{f_{osc}}{\pi\Delta f}\right)^2 \qquad (2.20) \end{aligned}$$

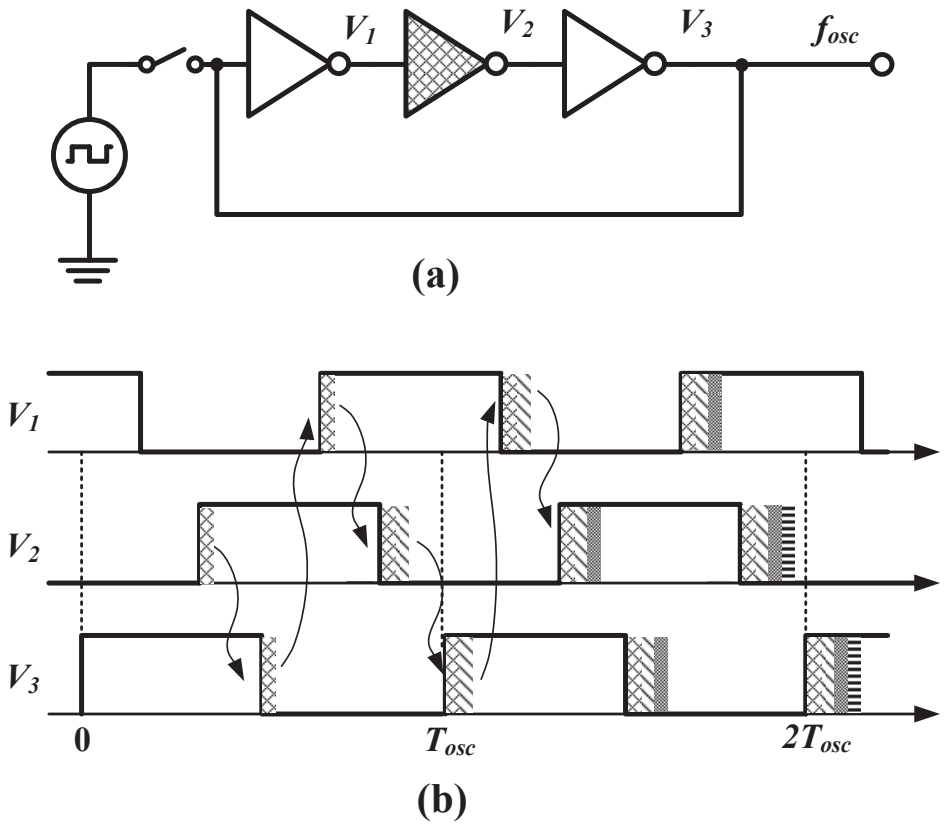


Figure 2.11: (a) Ring oscillator with only one noisy stage and (b) waveforms of the ring oscillator.

This equation can be rewritten as follows

$$S_{\Phi,ring}(\Delta f) = \frac{f_{osc}^2}{\Delta f^2}\{\frac{1}{2I_D^2}[S_I(\Delta f)|_{NMOS} + S_I(\Delta f)|_{PMOS}] + \frac{2kT}{I_D V_{DD}}\} + \frac{f_{osc}^2}{4NI_D^2\Delta f^2}\frac{1}{2I_D^2}[S_{1/f}(\Delta f)|_{NMOS} + S_{1/f}(\Delta f)|_{PMOS}] \quad (2.21)$$

Equation 2.21 shows that the phase noise due to white noise in the ring oscillator is inversely proportional to the drain current of the on-transistor and the supply voltage. And the phase noise due to flicker noise is inversely proportional to the number of the delay stages and the drain current of the on-transistor. The

number of the delay stages is inversely proportional to the oscillation frequency. When the oscillation frequency is predetermined and the current consumption is fixed, the phase noise due to flicker noise mainly depends on the flicker noise current, which relies on area of the MOSs and the process characteristics. Thus, Homayoun's model also shows that the phase noise of the ring oscillator mainly depends on the current consumption under the same supply voltage and oscillation frequency. It gives the same design insight as Abidi's model.

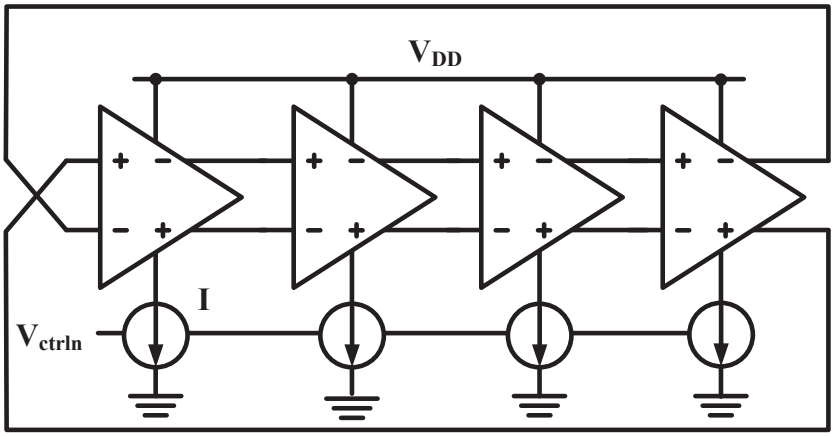


Figure 2.12: 4-stage differential ring oscillator.

Another popular topology in ring oscillators is a differential type as shown in Figure 2.12. While the inverter-based ring oscillators must have odd stages, the differential ring oscillators can have odd or even stages. The oscillation frequency in differential ring oscillators can be also estimated by the above methods.

Ring oscillators can be implemented with small chip area and low power consumption, but they have generally poor phase noise since they do not have any resonant components unlike LC oscillators. The phase noises, $L_{1/f}(f)$ and $L_{white}(f)$, due to flicker and white noises in a differential ring oscillator were introduced in [25].

$$L_{1/f}(f) = A\frac{K_f}{WLC'_{ox}f}(\frac{1}{V^2_{efft}})\frac{f_o^2}{f^3} \tag{2.22}$$

$$L_{white}(f) = \frac{2kT}{Iln2}\{\gamma(\frac{3/4}{V_{effd}} + \frac{1}{V_{efft}}) + \frac{1}{V_{op}}\}(\frac{f_{OSC}}{f})^2 \tag{2.23}$$

where K_f is the empirical coefficient, I is the tail current, V_{effd} is the effective gate voltage on the differential pair, V_{efft} is the effective gate voltage in the tail current source, and V_{op} is a differential peak output voltage swing, Comparison between the phase noises of the ring and LC oscillator in [25] shows that the ring oscillator takes takes 450 times large current compared with that of the LC oscillator in order to achieve the same phase noise. That is why LC oscillators are mostly used in applications requiring low phase noise.

2.2.3 Injection-Locked Oscillators

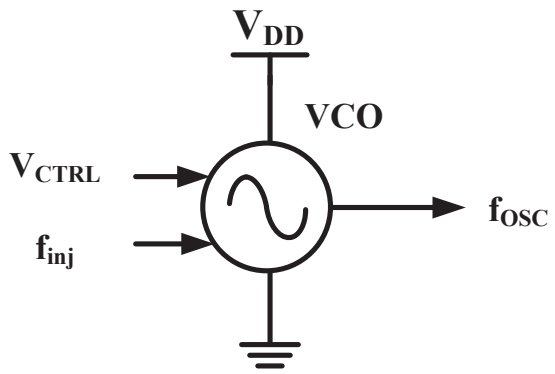


Figure 2.13: Concept of an injection-locked oscillator.

Basic concept of an injection-locked ring oscillator is shown in Fig. 2.13. The injection-locked oscillator is composed of a voltage-controlled oscillator and an external signal source. Let's consider that the oscillator outputs a signal with a frequency, f_{OSC}, which is controlled by a voltage, V_{CTRL}. Then, when the external signal with a frequency, f_{inj} is inputted to the oscillator and the oscillator is locked by the external signal, the output of the oscillator is realigned every period of the injection signal. The injection signal can be sinusoidal or pulse shaped signals.

Figure 2.14 shows waveforms in an injection-locked oscillator when the injection signal and the oscillator have the same frequency. In noisy oscillator, the

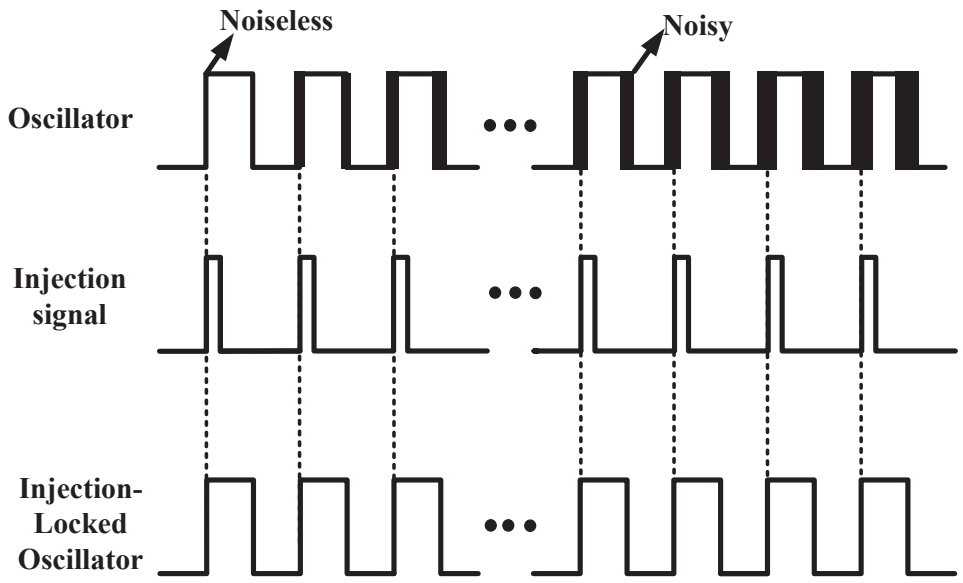


Figure 2.14: Waveforms in an injection-locked oscillator.

output waveform fluctuates from an ideal waveform. When time goes by, the deviation from the ideal waveform may increase due to noises. However, if the injection signal has lower phase noise than the oscillator, the waveform of the oscillator will realign at the injection signal every injection period and the phase noise of the oscillator approaches the one of the injection signal. The injection oscillators are generally used as a frequency divider, called the injection-locked frequency divider, and especially preferred for high frequencies, which the digital dividers can not cover [48]- [50].

The phase noise of the injection-locked frequency divider is mainly determined by the phase noise of the injection signal.

$$L_{ILFD} \approx L_{inj} - 20log(N) \tag{2.24}$$

where L_{ILFD} is the phase noise of the injection-locked frequency divider, L_{inj} is the phase noise of the injection signal, and N is the division ratio. The injection-locked frequency dividers can be based on LC or ring oscillators. LC-based injection-locked oscillators have better noise performance the ring-based

but suffer narrower locking range and unwanted harmonics.

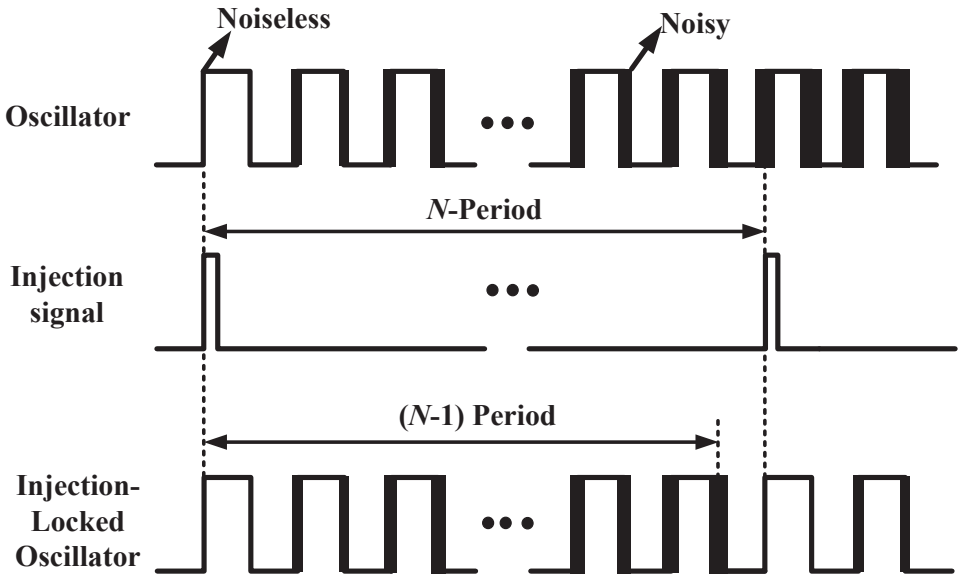


Figure 2.15: Waveforms in an injection-locked oscillator.

The injection-locked oscillators can be also used as frequency multipliers. Figure 2.15 shows waveforms in an injection-locked oscillator when the frequency of the injection signal is higher than the oscillator. When the ratio between two frequencies is small, the phase noise of the oscillator is closer to the phase noise of the injection signal and the lock state is more stable. However, when the ratio becomes larger, it is getting hard for the oscillator to be locked by the injection signal since the deviation from the ideal waveform may increased due to the noises generated by the oscillator itself during non-injected periods.

When the oscillator is locked by the injection signal, the phase noise of the oscillator tends to follow the phase noise of the injection signal. When the frequency of the injection signal is N-times higher than the oscillator, the phase noise, L_{OSC} of the oscillator as following:

$$L_{OSC} \approx L_{inj} + 20log(N) + \alpha \tag{2.25}$$

where α is noise of the oscillator during $(N-1)$ periods. When the frequency

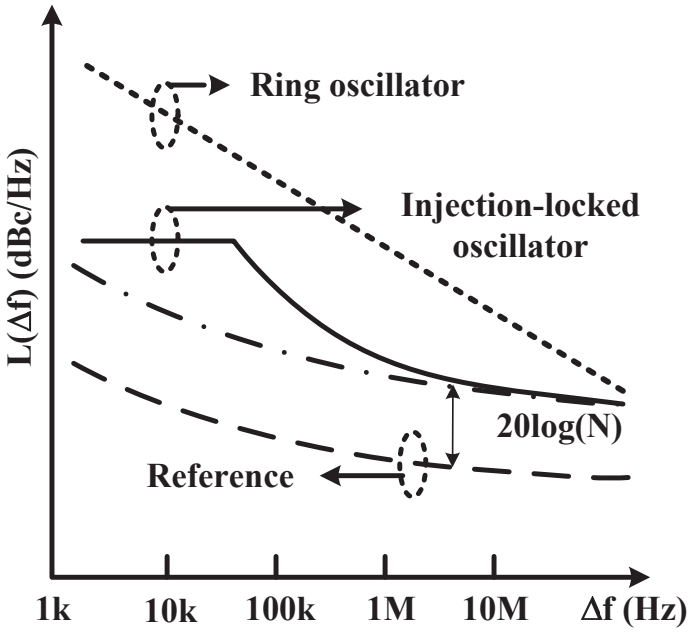


Figure 2.16: Phase noise in the injection-locked ring oscillators as a frequency multiplier.

of the injection signal is N-times lower than the oscillator, the phase noise, L_{OSC} of the oscillator becomes as shown in Fig. 2.16. At the low offset frequency, the phase noise of the oscillator is a little bit higher than $L_{inj} + 20log(N)$ and at the high offset frequency, the phase noise of the oscillator becomes $L_{inj} + 20log(N)$. In CMOS technology, it is substantially difficult to secure the stable lock state due to quite narrow lock range, process variations, and poor modeling [51].

2.3 Phase-Locked Loops

In many CMOS VLSI systems, the clock generators do not consist of only oscillators since the generated signal can have quite poor and unstable performance. Thus, the clock generators are generally composed of a system including the oscillators, such as PLLs. Simple block diagram of charge-pump PLLs is shown in Fig. 2.17. Charge pump PLLs are most widely used for clock generators since they have good stability and reasonable phase noise characteristics.

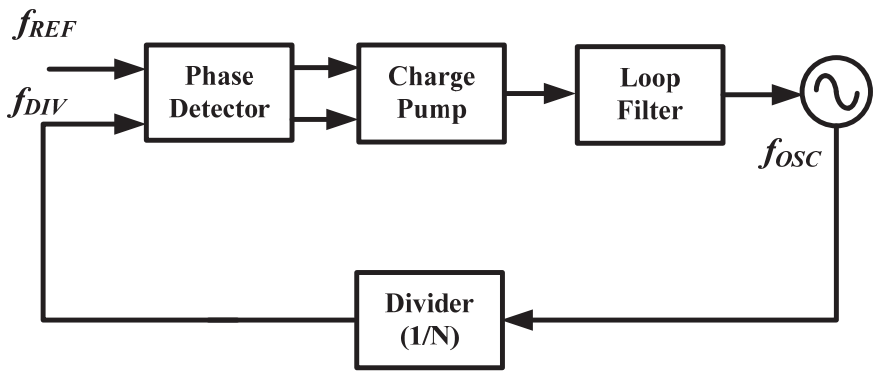


Figure 2.17: Block diagram of a charge-pump PLL.

The charge-pump PLLs are composed of a voltage-controlled oscillator, a frequency divider, phase-frequency detector, a charge-pump, and a loop filter. The voltage-controlled oscillator is controlled by a voltage, which is proportional to the frequency of its output signal. The frequency divider divides the frequency of its input signal to output the frequency-divided signal. Then the output of the divider has the same frequency to the reference. The crystal oscillators are frequently used as the reference since they have low phase noise and high stability. The phase-frequency detector detects the frequency or phase difference between two input signals, the reference signal and the output of divider, and outputs the indicating signal whether the phase of the output of the divider leads or lags the phase of the reference. The charge-pump converts the pulse width of its input signals to current. This current is a high frequency signal and then is filtered in the loop filter. The loop filter is actually a low pass filter and is a very important component to secure the stability of the feedback loop. The output of the loop filter is inputted to the oscillator and the frequency of the oscillator is thus controlled by the phase difference with the reference.

2.3.1 Phase Detector

A simple phase detector can be implemented by an exclusive-OR gate as shown in Fig. 2.18. It outputs high when the two inputs are different with each other.

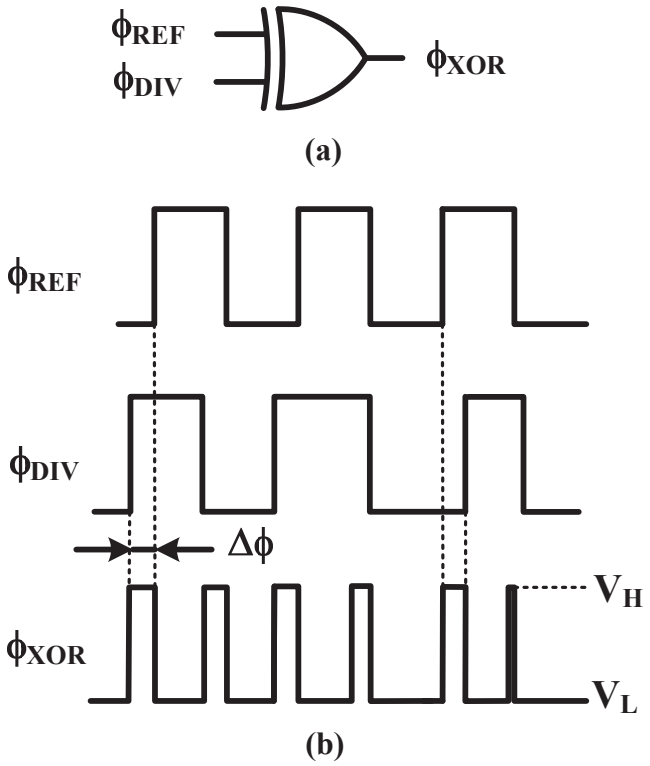


Figure 2.18: (a) Exclusive-OR phase detector (b) input an output signals of the exclusive-OR gate.

Thus, its average output has the same value when the phase difference. The transfer function of the phase detector is called the gain of the phase detector and defined as following:

$$K_{PD} = \frac{V_{mean}}{\Delta\Phi}[V/rad] \tag{2.26}$$

where V_{mean} is the mean of the output voltage and $\Delta\Phi$ is the phase difference. The phase detector of the exclusive-OR has the following phase gain:

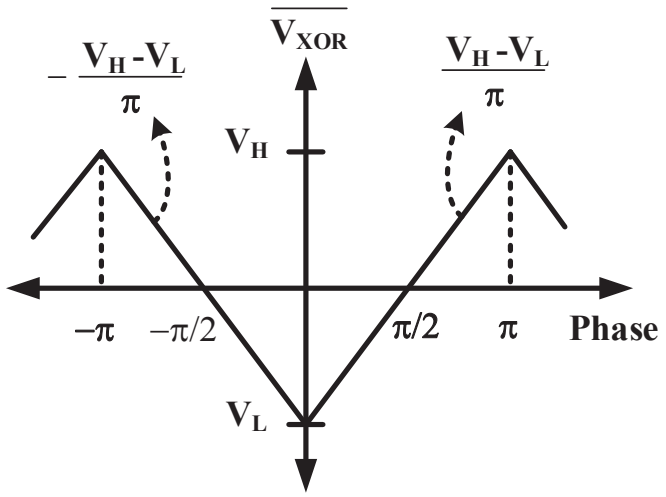


Figure 2.19: The gain of the exclusive-OR gate.

$$K_{PD} = \frac{V_H - V_L}{\pi} \text{ for } -\pi < \Delta\phi < 0 \quad (2.27)$$

$$= -\frac{V_H - V_L}{\pi} \text{ for } 0 < \Delta\phi < \pi \quad (2.28)$$

The stable lock happens at the phase difference of -$\pi/2$ or $\pi/2$. Thus, only the range of π is usable. The gain with the same sign in positive and negative phase differences may lose the lock.

These kinds of problem can be solved by a tristate phase-frequency detector. It is composed of two D-flipflop and an AND gate as shown in Fig. 2.20. It outputs two kinds of signals, UP and DOWN. When the reference leads the output of the divider, the phase frequency detector outputs UP first and then when the output of the divider is high, the down signal is outputted and the phase-frequency detector is reset. The phase-frequency detector has three states, that is, up, down, and zero. Zero state is not substantially zero. As shown in Fig. 2.21, the phase-frequency detector outputs up and down at the same time when the two inputs are the same phase. The pulse width, PW_{min}, in this case

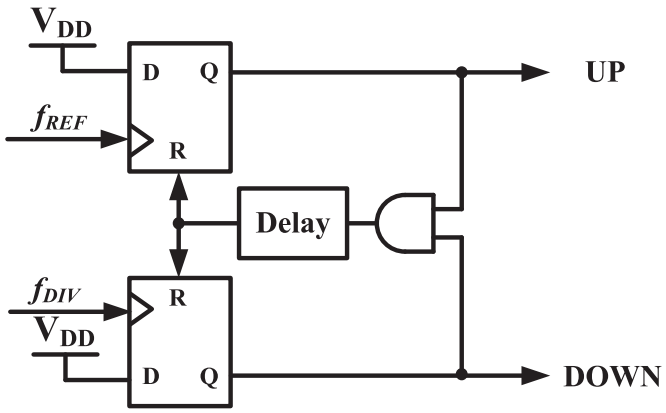


Figure 2.20: Tristate phase-frequency detector.

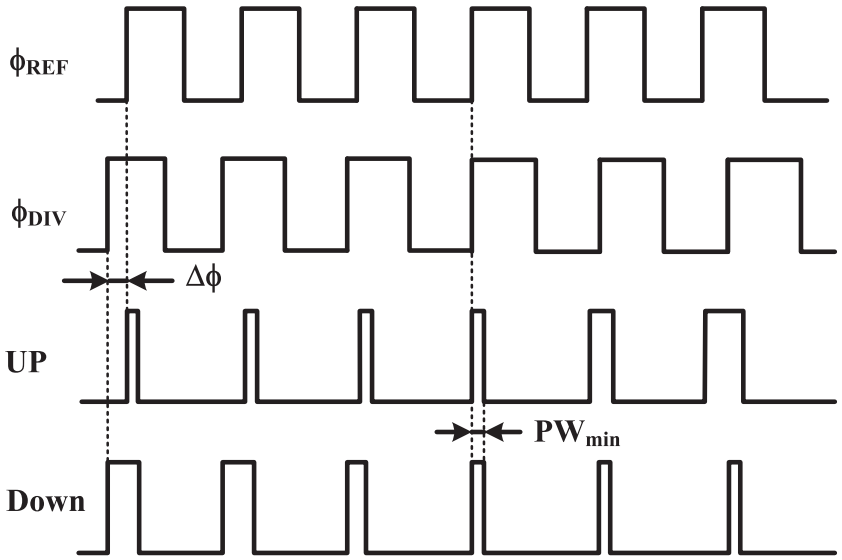


Figure 2.21: Input an output signals of the tristate phase-frequency detector.

is determined by delay of the AND gate, D-flipflop, and delay block. Without the delay stage, the phase-frequency detector outputs a very narrow pulse when two inputs has almost zero phase difference. it can not properly operate the next stage of the charge pump and results in dead zone. The deadzone will increase

phase noise. The problem can be solved by inserting the delay stage. The delay stage increases minimum pulse width to properly operate the next stage.

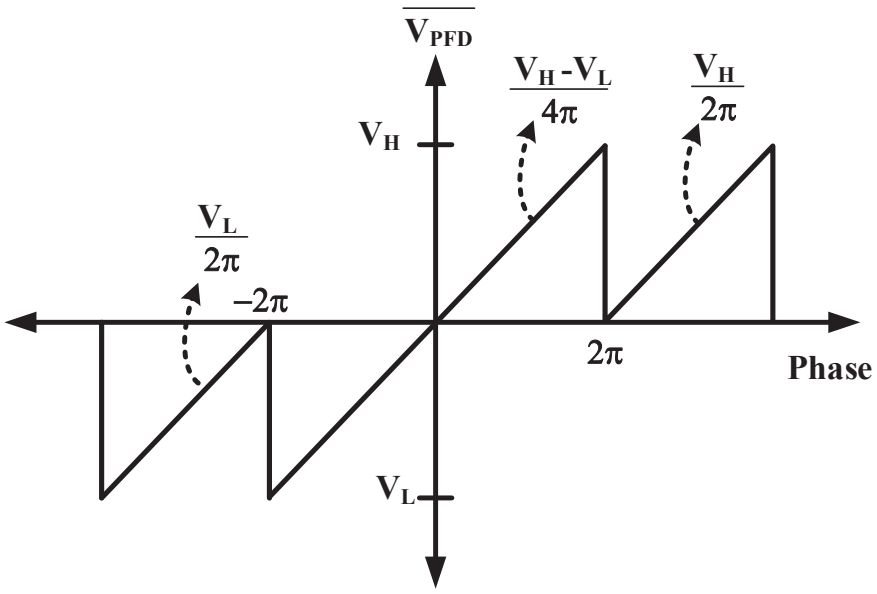


Figure 2.22: Gain of the tristate phase-frequency detector.

The transfer function of the phase-frequency detector is shown in Fig. 2.22. Its linear phase detection range is 4π, which is four times wider than that of the exclusive-OR.

$$K_{PFD} = \frac{V_H - V_L}{4\pi} \text{ for } -2\pi < \Delta\phi < 2\pi \tag{2.29}$$

$$= \frac{1}{2\pi} \text{ when } V_H = 1 \text{ and } V_L = -1 \tag{2.30}$$

The gains with different signs in positive and negative phase differences allow frequency detection and stable lock happens zero phase difference.

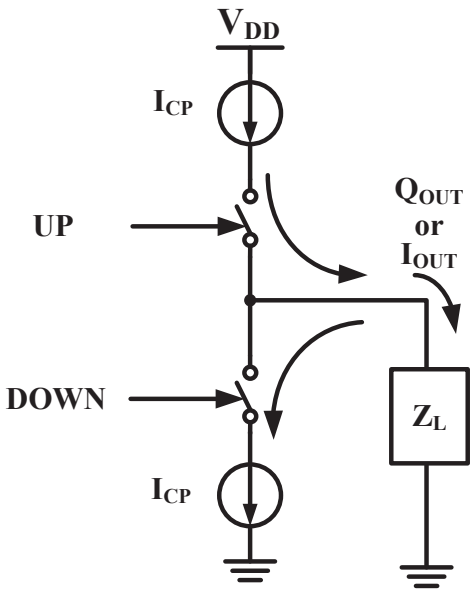


Figure 2.23: Charge pump.

2.3.2 Charge Pump

The charge pump is a kind of a converter converting digital error pulse to analog current. Figure 2.23 shows a simple block diagram of the charge pump. The UP and DOWN signals switch on or off the current source, respectively. When UP is high, the current, I_{CP} flows in the load and when DOWN is high, the current flow out of the load. Thus, the transfer function of the charge pump is I_{CP}[A/V]. This simple concept does not provide relation between the phase error and the output of the charge pump. When both the phase-frequency detector and the charge pump is considered at the same time, the relation between them can be provided and the combine gain of them also obtained.

The charge pump convert the output of the phase-frequency detector to charge, which is proportional to the pulse width of the output. When the current source outputs constant current, I_{CP}, the UP and DOWN switch on or off the current source for the pulse width, PW_{UP} and PW_{DOWN}. Thus, charge, Q_{CP}, flows in or out of the load, Z_L. Figure 2.24 shows the input and output signals

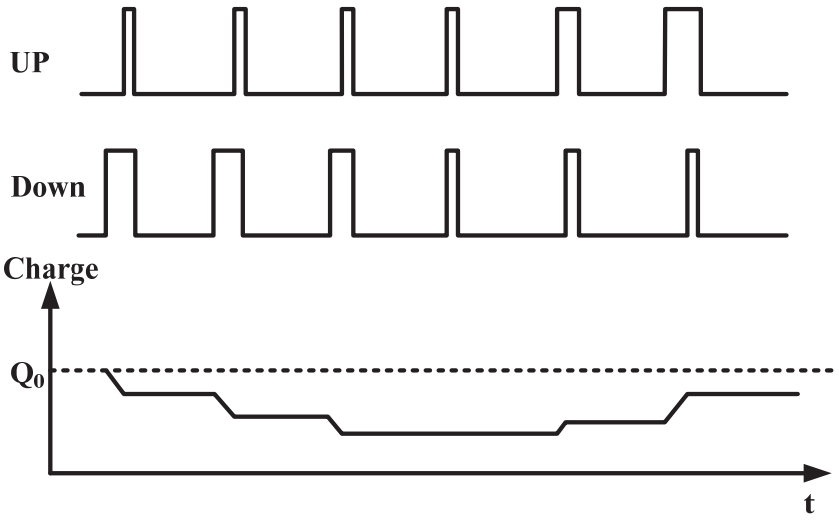


Figure 2.24: Input and output signals of the charge pump.

of the charge pump. Q_0 is an initial charge in the capacitor. Thus, the output charge, Q_{OUT}, due to the phase difference, $\Delta\phi$, is as following:

$$Q_{OUT} = \frac{I_{CP}\Delta\phi}{2\pi f_{REF}}[C] \tag{2.31}$$

The output charge can be average by the period and converted to the average output current, $I_{OUTmean}$.

$$\frac{Q_{OUT}}{T_{REF}} = \frac{I_{CP}\Delta\phi}{2\pi f_{REF}} \cdot T_{REF}\left[\frac{C}{s}\right] \tag{2.32}$$

This equation can be written as following:

$$I_{OUTmean} = \frac{I_{CP}\Delta\phi}{2\pi}[A] \tag{2.33}$$

Thus, the combine gain, $K_{PDF\cdot CP}$ with the phase-frequency detector in Eq. 2.30 and the charge pump is obtained as following [55]:

$$K_{PDF\cdot CP} = \frac{I_{OUTmean}}{\Delta\phi} = \frac{I_{CP}}{2\pi}\left[\frac{A}{rad}\right] \tag{2.34}$$

2.3.3 Loop Filter

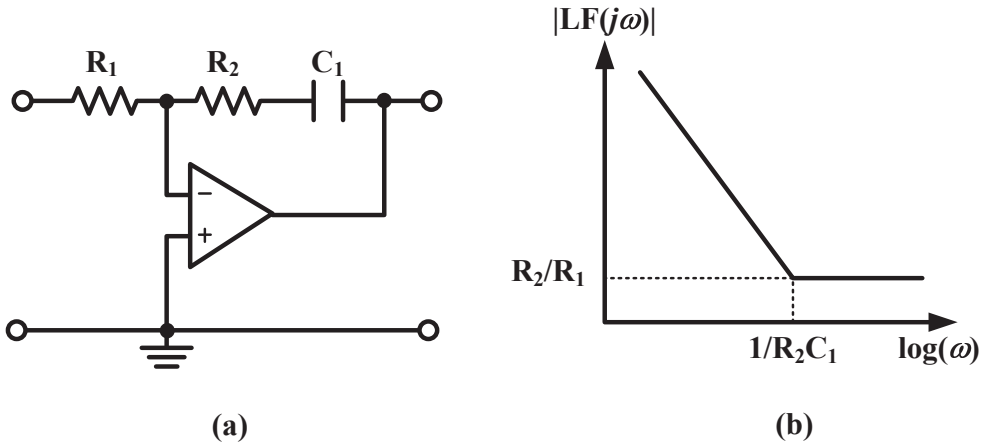


Figure 2.25: Active proportional-integral loop filter.

The loop filter integrates the output current of the charge pump and outputs the averaged voltage. The main purpose of the loop filter is to establish the dynamics of the feedback loop and to secure a suitable control of the oscillator [56]. The loop filter can be implemented by active or passive elements, which are called active loop filters and passive filter, respectively. Figure 2.25 shows an active proportional-Integral (PI) loop filter. Its transfer function is as following:

$$|LF_{PI}(s)| = \frac{sC_1R_2 + 1}{sC_1R_1} \tag{2.35}$$

The active PI loop filter has a pole at 0 Hz and a zero at $1/(C_1R_2)$Hz. Thus, it has a large open loop gain at low frequency. While higher order active filters can filter out of the noise, they has still a few of drawback. The linearity and open loop gain of the active filter limits the frequency gain of the loop. And the noise of the active filter can increase the phase noise of the PLL.

The most simple passive loop filter is shown in Fig. 2.26. Its transfer function is as following:

$$|LF_{P1st}(s)| = R + \frac{1}{sC} \tag{2.36}$$

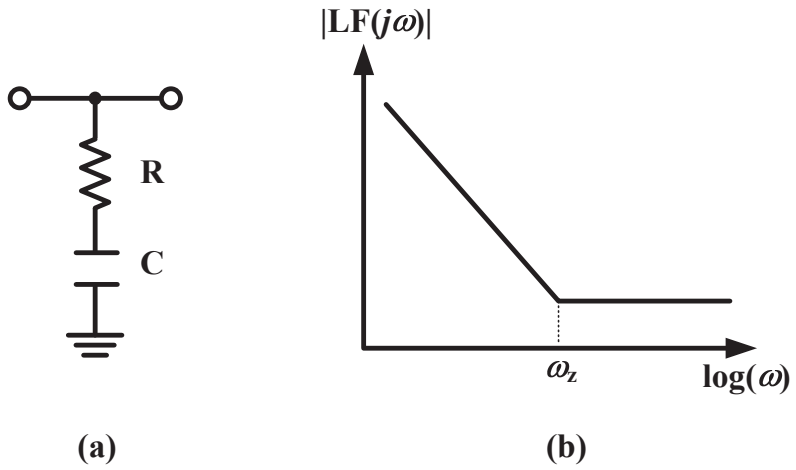


Figure 2.26: Passive 1st order loop filter.

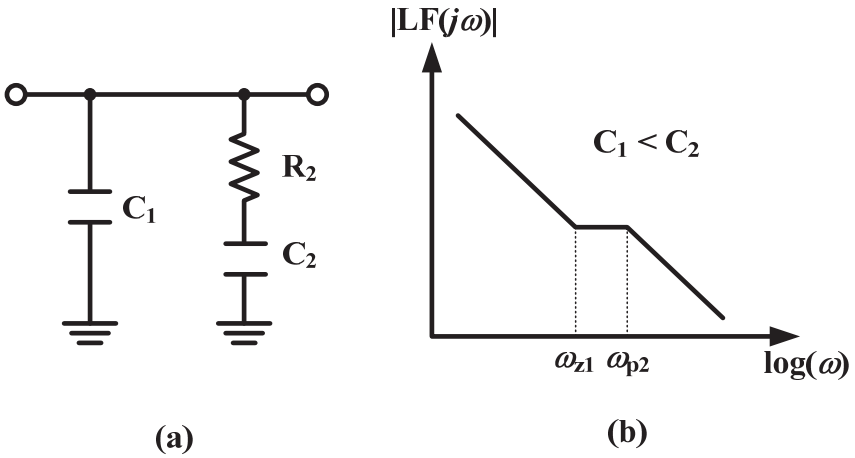


Figure 2.27: Passive 2nd order loop filter.

The passive 1st-order loop filter can track the signal more quickly than higher-order loop filter. But this has critical drawback which the control voltage experiences discrete steps due to abrupt changes in the charge pump current. This ripple can be mitigated by adding an additive capacitor to the 1-st-order loop filter. Then, the loop filter becomes 2nd-order shown in Fig 2.27. It has the

following transfer function:

$$|LF_{P2nd}(s)| = \frac{sC_2R_2 + 1}{s^2C_1C_2R_2 + s(C_1 + C_2)} \tag{2.37}$$

If k is larger than unity and C_2 is k times larger than C_1, then the transfer function can be rewritten as following:

$$|LF_{P2nd}(s)| = \frac{skC_1R_2 + 1}{s(k+1)C_1\{skC_1R_2/(k+1) + 1\}} \tag{2.38}$$

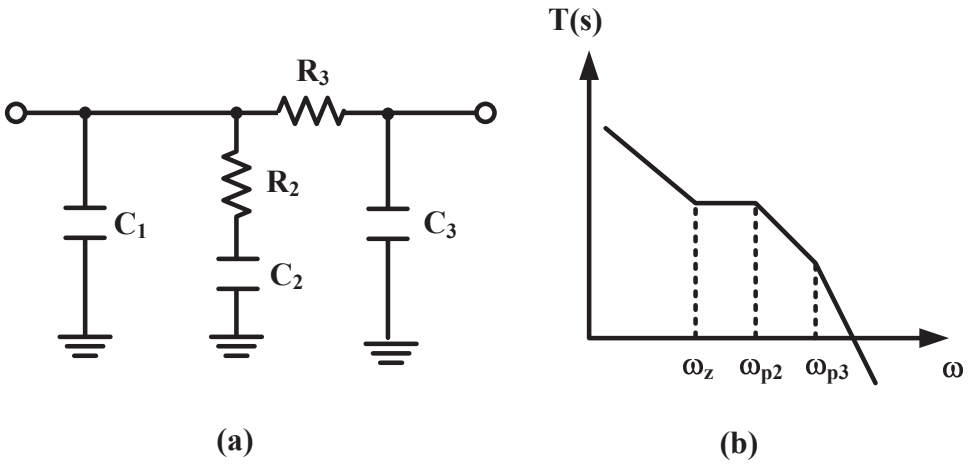


Figure 2.28: Passive 3rd order loop filter.

In order to further suppress reference spurs and high frequency noise, another pole can be added in the loop filter as shown in Fig. 2.28. Higher-order loop filters can be also implemented. However, they are seldom used in practice since it is hard to obtain the phase margin for stability. The 2nd and 3rd order loop filters are mostly preferred.

2.3.4 Voltage Controlled Oscillator

The output of a voltage controlled oscillator such as LC and ring oscillators has an inherent frequency sensitivity over control voltage. It is called an oscillator gain, K_{VCO}, defined as following:

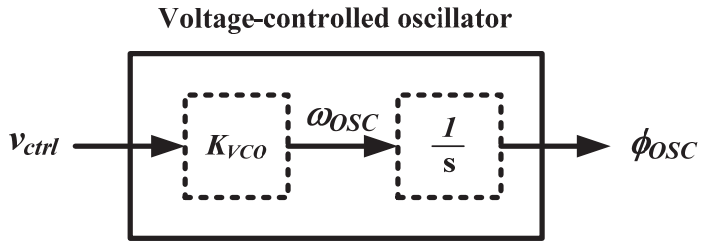


Figure 2.29: Transfer function of the voltage-controlled oscillator.

$$K_{VCO} = \frac{\omega_2 - \omega_1}{v_{ctrl2} - v_{ctrl1}} \left[\frac{radHz}{V}\right] \tag{2.39}$$

Thus, the angular frequency, $\omega_{OSC}(t)$, is

$$\omega_{OSC}(t) = K_{VCO} v_{ctrl}(t) \tag{2.40}$$

Thus output phase of the oscillator, $\phi_{OSC}(t)$, is

$$\phi_{OSC}(t) = K_{VCO} \int v_{ctrl}(t) dt \tag{2.41}$$

In the phase-locked loop, the transfer function of the oscillator is obtained by taking the Laplace transform to the phase of the oscillator output.

$$\frac{\Phi_{OSC}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \tag{2.42}$$

Thus, an ideal voltage-controlled oscillator is an integrator.

2.3.5 Loop Transfer Functions

The linear model of the phase-locked loop can be expressed as shown in Fig. 2.30. The loop characteristics of the phase-locked loop can be considered by the linear model. The forward-loop transfer function, $T(s)$, is as following:

$$T(s) = \frac{\phi_{OSC}}{\phi_{REF}} = \frac{K_{PDF \cdot CP} \cdot LF(s) \cdot K_{VCO}}{s} \tag{2.43}$$

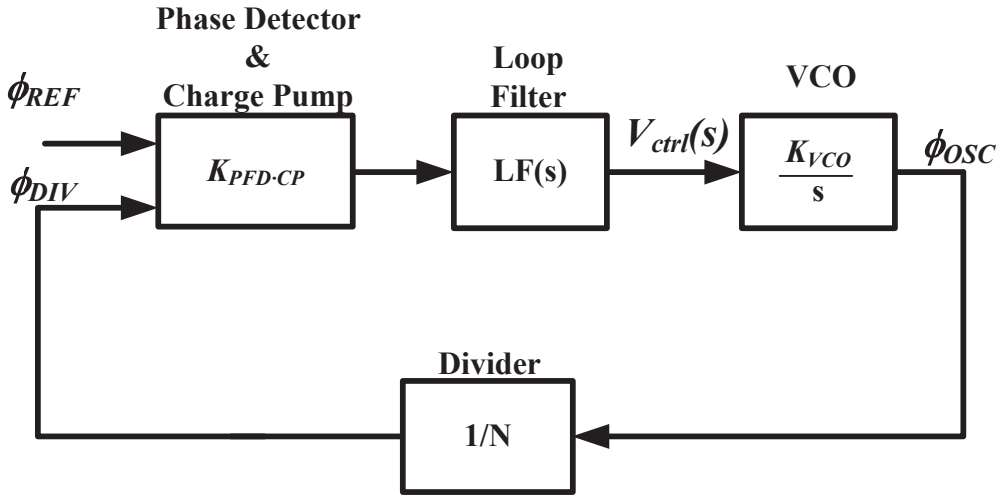


Figure 2.30: Linear model of the phase-locked loop.

The order of the phase locked loop is defined by the number of poles in the open loop transfer function. When the passive 1st order loop filter is adapted, the phase-locked loop is the 2nd order. Its forward transfer function becomes as following:

$$T(s) = \frac{I_{CP}}{2\pi} \cdot \frac{K_{VCO}}{s} \frac{(sCR+1)}{sC} \tag{2.44}$$

The open-loop transfer function has two poles at 0 rad/sec and one zero at $\omega_{z1} = 1/(CR)$. The crossover frequency, ω_c, of the forward loop transfer function is obtained by the following equation.

$$|T(j\omega)| = \frac{I_{CP}}{2\pi} \cdot \frac{K_{VCO}\sqrt{\omega_c^2 C^2 R^2 + 1}}{\omega_c^2 C^2} = 1 \tag{2.45}$$

Assume that $\omega_c^2 C^2 R^2 >> 1$, then the crossover frequency, ω_c, is

$$\omega_c = \frac{I_{CP} K_{VCO} R}{2\pi C} \tag{2.46}$$

Figure 2.31 shows the open-loop response of the 2nd order phase locked loop. Its closed-loop transfer function, is expressed as following:

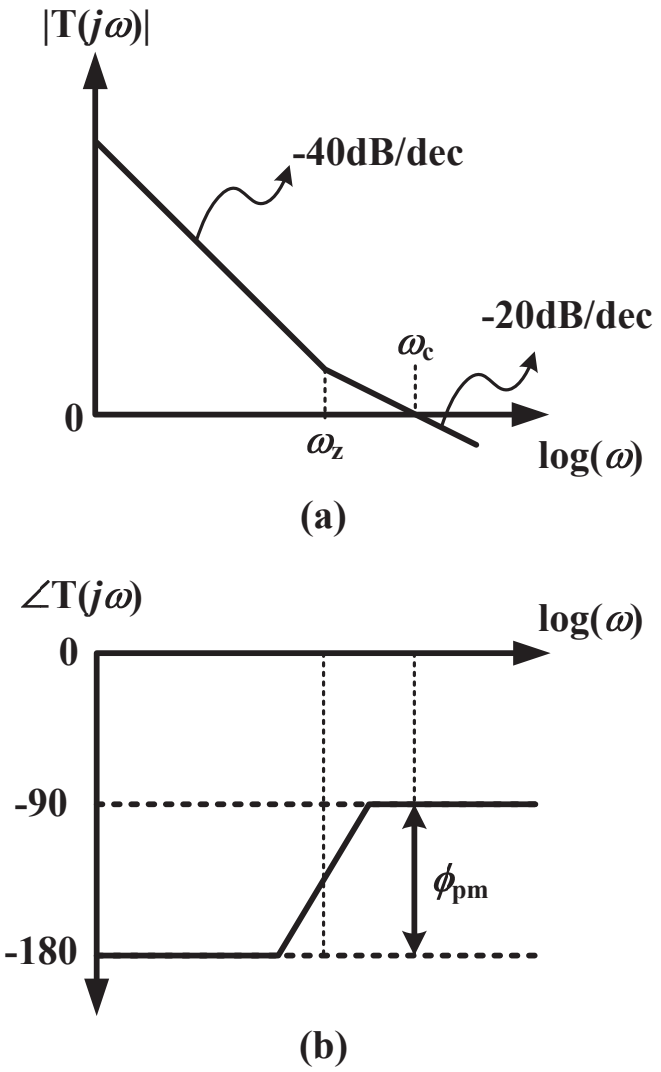


Figure 2.31: (a) Forward-loop response and (b) its phase of the 2nd order phase locked loop.

$$\begin{aligned} H(s) &= \frac{\phi_{OSC}}{\phi_{REF}} = \frac{K_{PDF\cdot CP} \cdot LF(s) \cdot K_{VCO}/s}{1 + K_{PDF\cdot CP} \cdot LF(s) \cdot K_{VCO}/(N \cdot s)} \\ &= \frac{N(sCR+1)}{2\pi CNs^2/(I_{CP}K_{VCO}) + sCR + 1} \end{aligned} \tag{2.47}$$

And its denominator can be expressed by the 2nd-order equation.

$$2\pi CNs^2/(I_{CP}K_{VCO}) + sCR + 1 = K(s^2 + 2\xi\omega_n s + \omega_n^2) \tag{2.48}$$

Thus, the natural frequency, ω_n, the damping factor, ξ, and the constant, K, are extracted from the denominator.

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi CN}} \tag{2.49}$$

$$\xi = \frac{R}{2}\sqrt{\frac{I_{CP}K_{VCO}C}{2\pi N}} \tag{2.50}$$

$$K = \omega_n^2 \tag{2.51}$$

Thus, the crossover frequency of the forward loop transfer function can be rewritten in terms with the natural frequency.

$$\omega_c = \frac{N}{R}\omega_n^2 \tag{2.52}$$

When the zero of the closed loop transfer function is $\omega_z = 1/RC = \omega_z/(2\xi)$, the closed loop transfer function can be expressed as following:

$$H(s) = \frac{N(s2\xi/\omega_n + 1)}{\omega_n^2(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{2.53}$$

The closed loop gain of the 2nd order PLL is shown in Fig. 2.32. The overshoot in the frequency response results in the overshoot in the step response in the time domain. Thus, the damping factor is generally selected to be $1/\sqrt{2}$. The most important function of the PLL is noise filtering. The open-loop transfer function, $G(s)$, is

$$G(s) = NT(s) = \omega_n^2\frac{(s2\xi/\omega_n + 1)}{s^2} \tag{2.54}$$

Figure 2.33 shows the linear noise model of the PLL. Transfer function from each noise source to output phase can be obtained by the open loop transfer function. For example, transfer function, $N_{OSC}(s)$, of the noise source from the

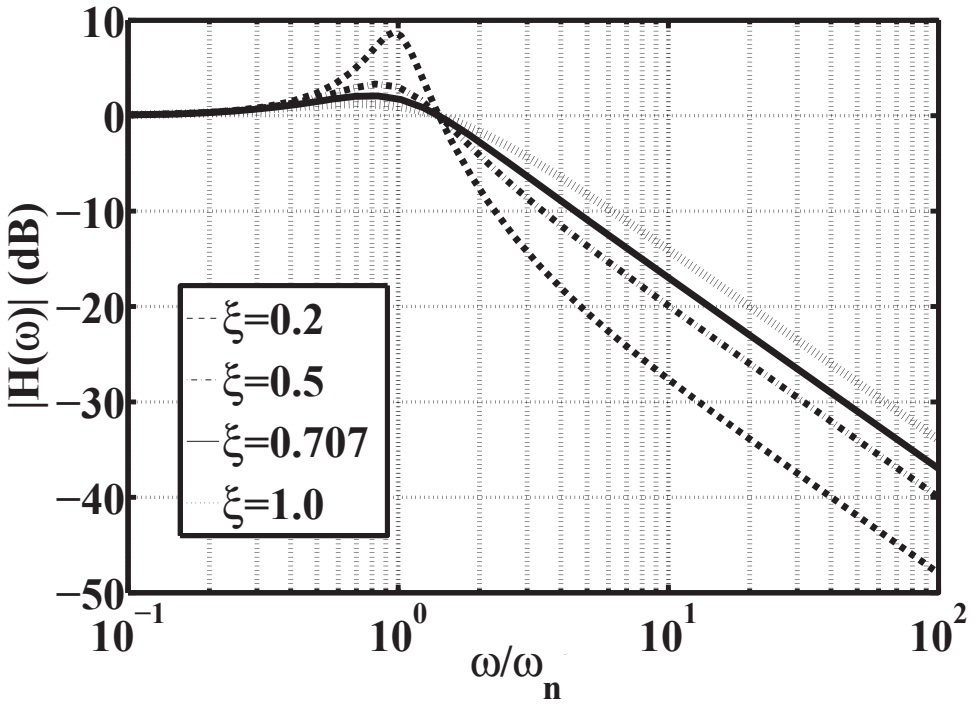


Figure 2.32: Closed loop gain of the 2nd order PLL.

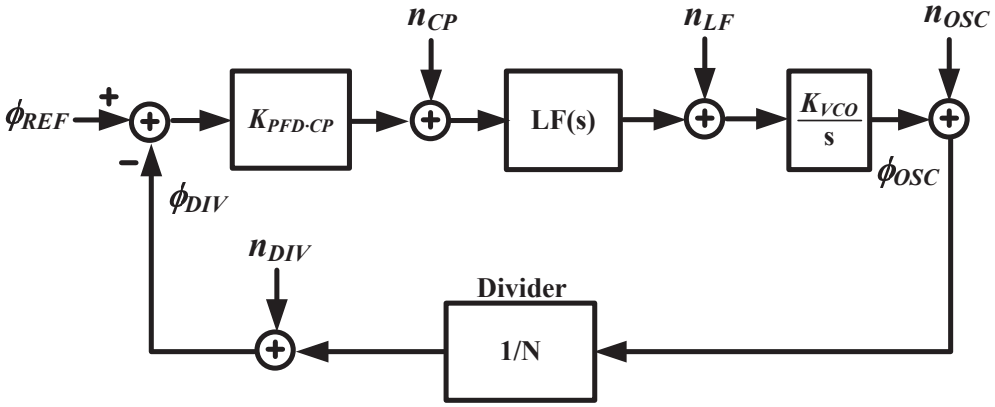


Figure 2.33: Linear noise model of the PLL.

oscillator is $1/(1 + G(s))$. Thus, the noise transfer functions from each noise source are as following:

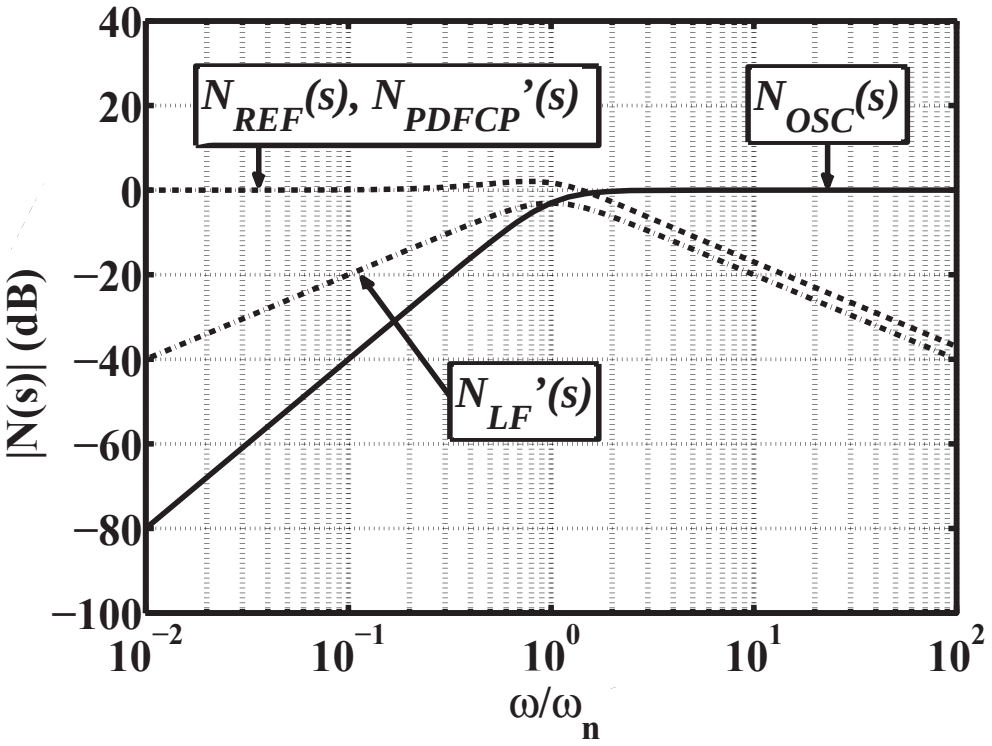


Figure 2.34: Noise transfer functions of the 2nd order PLL.

$$N_{OSC}(s) = \frac{\Phi_{OSC}(s)}{n_{OSC}(s)} = \frac{s^2}{s^2 + 2\xi\omega_n s + 1} \tag{2.55}$$

$$N_{DIV}(s) = \frac{\Phi_{OSC}(s)}{n_{DIV}(s)} = \frac{-N(s2\xi/\omega_n + 1)}{\omega_n^2(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{2.56}$$

$$N_{LF}(s) = \frac{\Phi_{OSC}(s)}{n_{LF}(S)} = \frac{sK_{VCO}}{s^2 + 2\xi\omega_n s + 1} \tag{2.57}$$

$$N_{PDFCP}(s) = \frac{\Phi_{OSC}(s)}{n_{PDFCP}(s)} = \frac{N(s2\xi/\omega_n + 1)}{K_{PDFCP}\omega_n^2(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{2.58}$$

The noise transfer functions of the 2nd order PLL are shown in Fig. 2.34. $N'_{LF}(s)$ and $N'_{PDFCP}(s)$ are transfer functions normalized by gains of $N_{LF}(s)$ and $N_{PDFCP}(s)$, respectively. The noise transfer functions of the noises generated at

the reference, the phase frequency detector and charge pump have characteristic of a low pass filter. And the noise transfer function of the noises generated at the loop filter has characteristic of a bandpass filter. Especially, noise transfer function of the noise generated at the oscillator has high pass filter and then noises with high power around the oscillation frequency can be filtered out. Thus, large loop bandwidth can block much larger noises from the oscillator but increases inband noise from the reference, the phase frequency detector, and the charge pump. The loop bandwidth, f_{LB}, is generally selected by balancing the noises such that the output noise can be minimized.

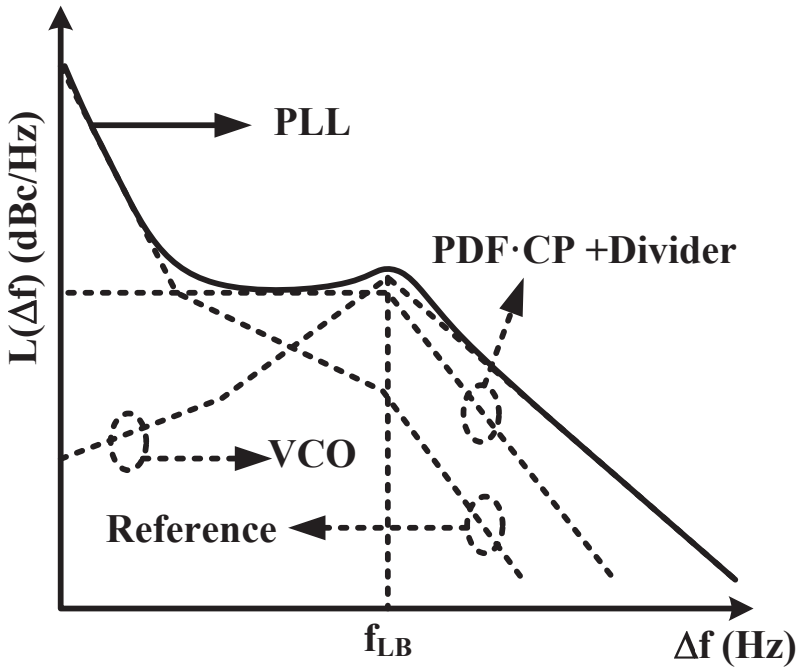


Figure 2.35: Total phase noise of the PLL.

Figure 2.35 shows the total phase noise of the PLL. The output noise mainly depends on the noises of the oscillator and the reference. For lower phase noise, LC oscillators are preferred but are accompanied with large power consumption and chip area, and narrow tuning range. For wide tuning range and low power consumption, ring oscillators are preferred but also accompanied with poor phase

noise and large chip area for loop filter due to high frequency sensitivity of the ring oscillator. For the PLL around 1GHz, the PLL with the ring oscillator has smaller area since area of the LC oscillator itself requires large area about $500 \times 500\mu m^2$ [58], but the phase noise is inferior than the PLL with a LC oscillator.

2.4 Summary

In this chapter, basic concept of the phase locked loop was discussed and its components described. LC oscillator-based phase-locked loops (PLLs) can provide relatively lower-jitter and lower-phase noise performance than ring oscillator-based PLLs [59]- [61]. However, LC oscillator-based PLLs are more suitable for higher frequency clock than required clock frequency of ADCs since high-Q inductors for low frequency oscillator occupy relatively large chip area in modern nano-CMOS technologies process. When ring oscillator is adopted for PLLs, area of a ring oscillator itself is small but the PLLs have generally poor phase noise. Furthermore, high voltage sensitivity of the ring oscillator increases area of the loop filter.

Another approach for achieving low phase noise acquisition utilizes the benefits of CMOS scaling such as All-Digital PLLs [89] [92]. They are suitable to be implemented in fine digital CMOS technology but still require high power consumption and large area to obtain low phase noise.

Chapter 3

Injection-Locked Ring Oscillator as a Frequency Multiplier

This chapter derives a simple lock range model for injection-locked ring oscillators as a frequency multiplier to provide insight and guideline for designers. The model is based on variations in the output signal of the injection-locked ring oscillator when the injection signal is inputted. Moreover, it is discussed about asymmetry of the lock range.

3.1 Conventional Lock Range of Injection-locked Oscillator

Conventional models on injection locking in oscillators are mainly based on phase shifts by external signals in resonance oscillation. Their lock ranges are represented in terms of quality factor of LC tank and powers of oscillation and injection signals. Injection lock oscillators have been mainly used as a high frequency divider called an injection lock frequency divider (ILFD). Thus, the analyses of the injection-locked oscillators are mostly concerned with frequency dividers [51] [62]-[65]

As shown in Fig. 3.1, conventional models on injection locking in oscillators are mainly based on phase shifts by external signals in resonance oscillation [51] [62]. When the radian frequency of the oscillator is ω_o and Q is the quality factor

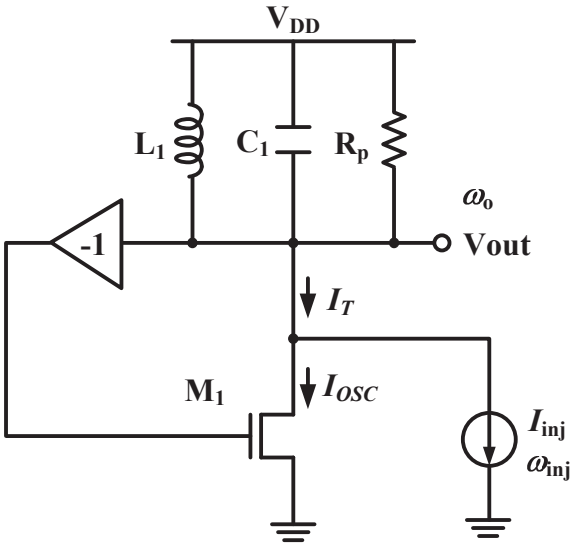


Figure 3.1: Conventional injection-locked oscillator model.

of LC tank, the lock range, ω_L, is

$$\omega_L \approx \frac{\omega_o}{2Q}\frac{I_{inj}}{I_{osc}} \tag{3.1}$$

They provide insight to analyze injection-locked oscillators based on a resonant-based oscillator. However, it is somewhat tricky to apply their concepts for injection-locked ring oscillators because ring oscillators are not composed of LC resonant circuit.

3.2 Ideal Lock Range

It is discussed about an ideal lock range model for injection-locked ring oscillators as a frequency multiplier. It is considered that an injection-locked oscillator is composed of N_d delay stages and a direct inject signal is inputted to one stage of the outputs as shown in Fig. 3.2. The direct injection-locked ring oscillator is simply achieved by injecting a very narrow signal into an input or an output of the ring oscillator. Then the input or output becomes the same amplitude.

It is assumed that a free running frequency, f_{osc}, of the ring oscillator is around

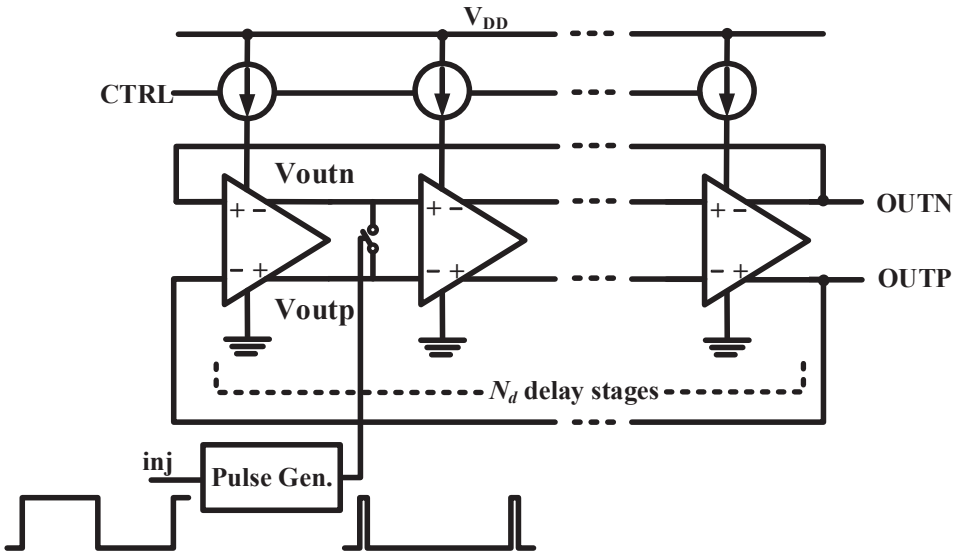


Figure 3.2: injection-locked ring oscillator with N_d delay stages.

N times to a frequency, f_{inj}, of an injection pulse signal, where N is a positive integer. The periodic pulse signal is generally the same frequency of the reference clock but has narrower pulse width. For simplicity, it is also assumed that the reference clock has no jitter and the injection signal is narrow but strong enough to pull the phase of the free running to the phase of the injection pulse at once. When the ring oscillator oscillates at $f_{osc} = 1/T_{osc}$ and the input at a delay stage does not reach the maximum amplitude, that is $|\phi_{osc}| < \pi/2$, it is assumed that the input voltage is not large enough to switch the output of the delay stage from high to low and vice versa.

Figure 3.3 shows a desirable relation between the free running and the injection pulse. ϕ_{osc} is a phase of the oscillator shifted from the origin of NT_{osc}, where N is a positive integer. That is, zero phase degree, $\phi_{osc} = 0$, of the free running means the phase of the $N - th$ period of the free running oscillator. Thus, the period of noiseless oscillator, T_{osc_ideal} , is exactly equal to the period of the injection signal over N. However, the free running frequency is actually noisy and its phase varies around zero phase.

Consider that the injection signal is inputted when the phase of the ring

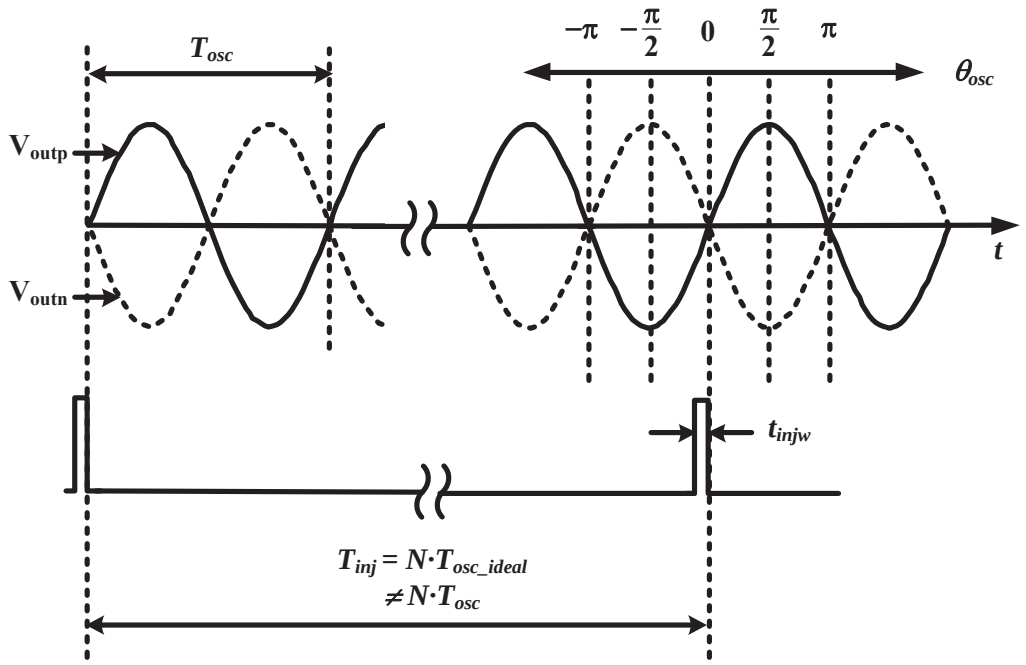


Figure 3.3: Relation between the free running and the injection pulse.

oscillator varies between $-\pi/2$ and $\pi/2$ as shown in Fig. 3.4. Figure 3.4(b) shows pulse injection at $-\pi/2 < \phi_{osc} < 0$ of the oscillator output which means that the free-running frequency is a little bit lower than Nf_{inj}. When the pulse with very narrow pulse width, t_{injw}, is injected to the oscillator, the differential outputs of the oscillator become short and then have the same voltage. Consequently, the phase of the oscillator is pulled to zero phase and the next output starts again at 0 of the phase degree as shown in Fig. 3.4(b). After the input of the injection pulse, the oscillator becomes thus advanced by ΔT.

Let us consider that the free-running frequency is a little bit higher than Nf_{inj}. Figure 3.4(c) shows pulse injection at $0 < \phi_{osc} < \pi/2$ of the oscillator output. In this case, the oscillator is delayed by ΔT. In the both cases, the last period results in not T_{osc} but $T_{osc} \pm \Delta T$ and the oscillation frequency becomes Nf_{inj}. Thus, the oscillator is locked at Nf_{inj} when the injection pulse is inputted at the $-\pi/2 < \phi_{osc} < \pi/2$. The phase expression of $-\pi/2 < \phi_{osc} < \pi/2$ is somewhat ambiguous because the oscillator is noisy and then fluctuated around

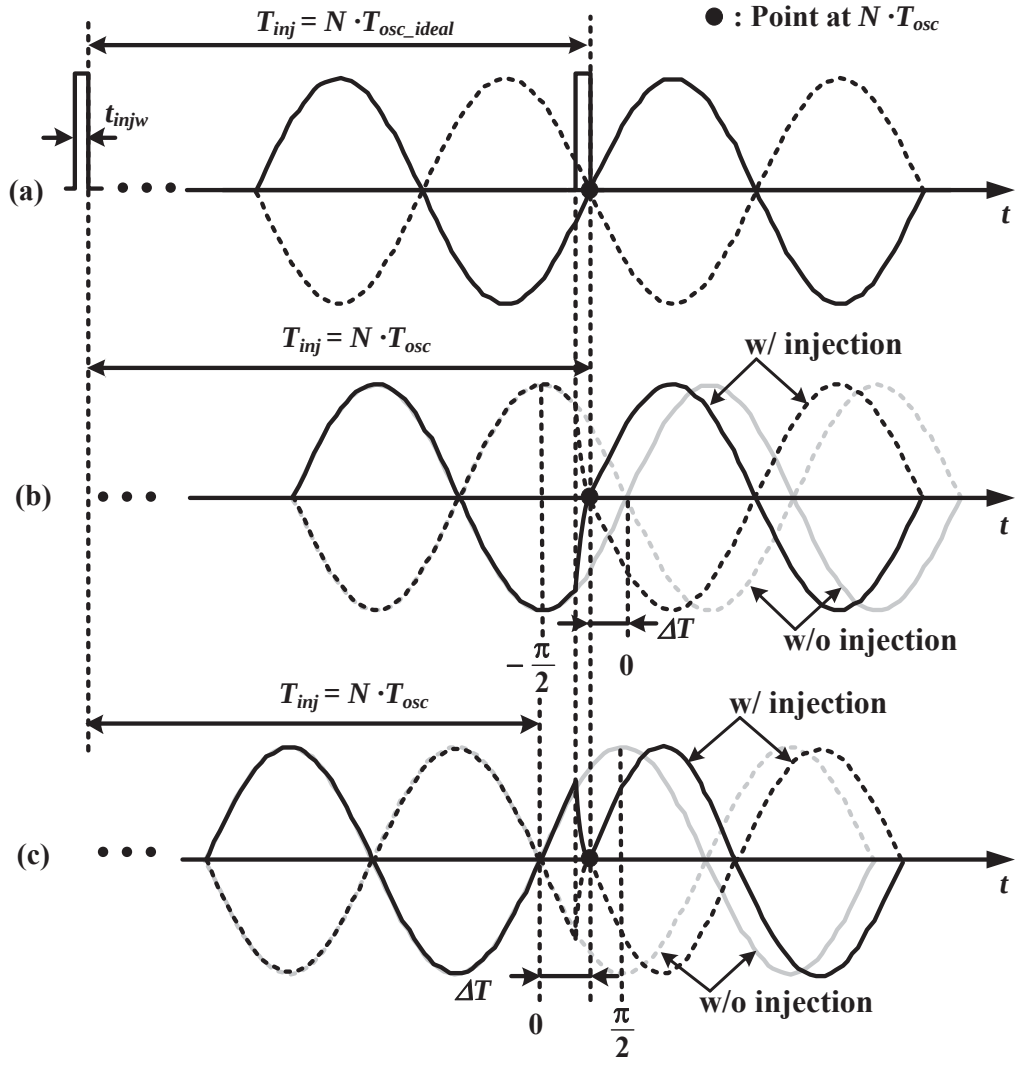


Figure 3.4: (a) Noiseless oscillator output and injection pulse (b) differential outputs of the oscillator before and after injection when the pulse signal is injected at $-\pi/2 < \phi_{osc} < 0$ of the phase of the oscillator (c) differential outputs of the oscillator before and after injection when the pulse signal is injected at $0 < \phi_{osc} < \pi/2$ of the phase of the oscillator.

the ideal frequency of the noiseless oscillator. For the clear explanation, the phase expression of $-\pi/2 < \phi_{osc} < \pi/2$ can be exchanged into the frequency of the reference clock, which is more accurate and less noise than the oscillator. The lower boundary of the phase is $T_{inj} = (N - 1/4)T_{osc}$, since the $\pi/2$ of the period

corresponds a quarter period. This can be expressed as $f_{osc} = (N - 1/4)f_{inj}$. Thus, the upper boundary is $f_{osc} = (N + 1/4)f_{inj}$. In other words, the oscillator is locked at Nf_{inj} when the oscillator has the frequency between $(N - 1/4)f_{inj}$ and $(N + 1/4)f_{inj}$

Let us consider that the oscillator is more noisier than the previous one, as shown in Fig. 3.5. Figure 3.5(b) show the injection pulse is inputted at $-\pi < \phi_{osc} < -\pi/2$. The oscillator has $(N - 1/2)T_{osc}$ within T_{inj}. That is, the oscillator is locked at $(N - 1/2)T_{osc}$, not NT_{osc}. This means that the oscillator locks at $(N-1/2)f_{inj}$. From the same view, the oscillator in Fig. 3.5(c) is locked at $(N + 1/2)T_{osc}$, that is, the frequency of $(N + 1/2)f_{inj}$.

Consequently, in order to lock the ring oscillator at Nf_{inj}, the phase variation of the oscillator should be in $-\pi/2 < \phi_{osc} < \pi/2$ and the maximum lock range is the half of the period of the oscillator and the frequency variation of the oscillator should be in as follows:

$$(N - \frac{1}{4})f_{inj} < f_{osc} < (N + \frac{1}{4})f_{inj} \tag{3.2}$$

Thus, frequency difference between the oscillator and its replica should be within $|f_{inj}|/2$ in order to lock at Nf_{inj}. Note that the injection-locked oscillator can be locked at not only Nf_{inj} but also $(N + 1/2)f_{inj}$ as described in Fig. 3.5. Therefore, the maximum achievable lock range of Eq. 3.2 can be generalized as follow:

$$(N - \frac{1}{2})\frac{f_{inj}}{2} < f_{osc} < (N + \frac{1}{2})\frac{f_{inj}}{2} \tag{3.3}$$

where N is a positive integer and f_{osc} is locked at $Nf_{inj}/2$. The ideal lock range is symmetric to the desired frequency of the oscillator. Note that the injection-locked oscillator operates not as a frequency multiplier but as a frequency divider when N is 1. the However, a substantial injection-locked oscillator may not have a symmetric lock range and be as wide as the ideal lock range mainly due to non-zero on-resistance of switches and the pulse width of the injection signal.

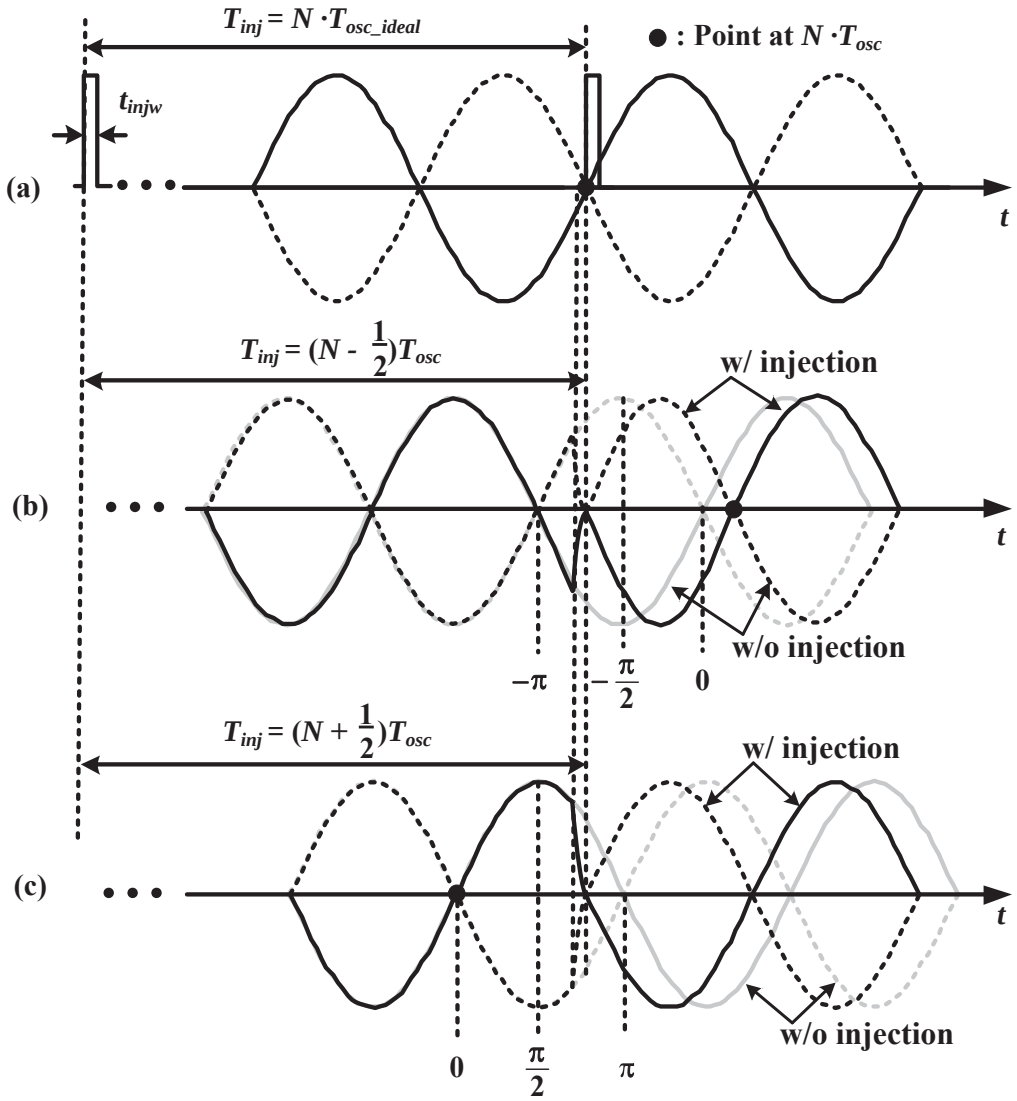


Figure 3.5: (a) Noiseless oscillator output and injection pulse (b) differential outputs of the oscillator before and after injection when the pulse signal is injected at $-\pi < \phi_{osc} < -\pi/2$ of the phase of the oscillator (c) differential outputs of the oscillator before and after injection when the pulse signal is injected at $\pi/2 < \phi_{osc} < \pi$ of the phase of the oscillator.

3.3 Asymmetric Lock Range of an Injection-Locked Ring Oscillator

The lock range of the injection-locked oscillator is symmetric with respect to the oscillation frequency under the ideal condition, which the injection signal has very

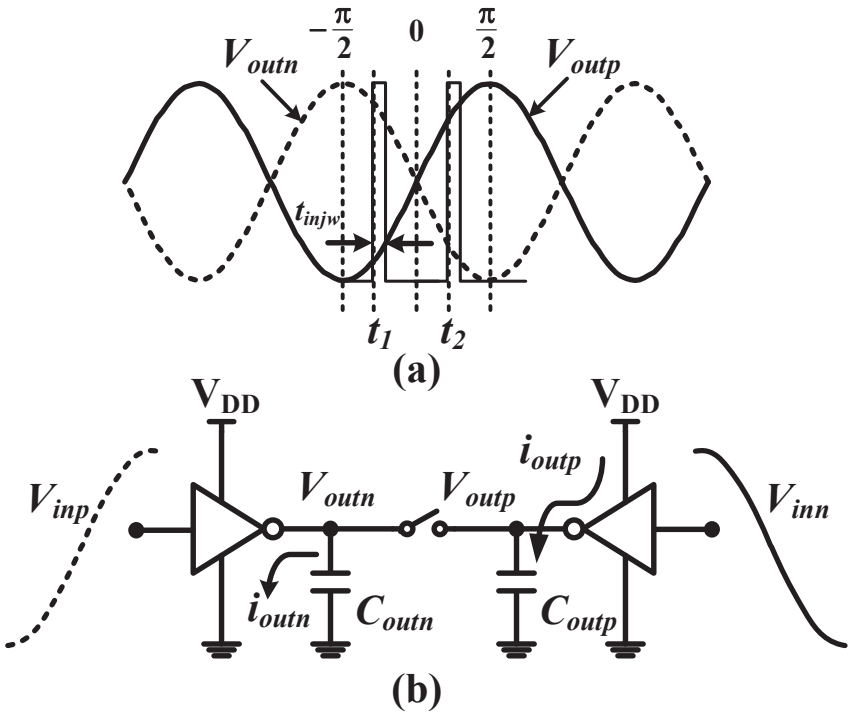


Figure 3.6: General current flow in a ring oscillator.

narrow pulse width but is strong enough to lock the oscillator. That is, the ideal condition means that the injection signal is an impulse signal and on-resistance of the switch for injection is zero. However, the injection signal substantially has a certain pulse width and the on-resistance of the switch is not zero. Though the on-resistance of the switch is desired to be as low as possible, the low on-resistance induces large parasitic capacitance in the output stage of the oscillator since it can be obtained by the large size of the switch. The large parasitic capacitance in the output stage causes more power consumption to obtain a certain oscillation frequency. For low power consumption, the use of high on-resistance requires the wide pulse width to lock the oscillator. However, the wide pulse width may disturb the oscillator when the oscillator have a desired oscillation frequency. Thus, the size of the switch and the pulse width should be carefully selected considering the power consumption so as not to disturb the oscillator when the oscillator have a desired oscillation frequency. Non-zero on-resistance also makes

the injection lock range asymmetric with respect to the oscillation frequency, which the upper lock range becomes narrower than the lower lock range. The asymmetric lock range can be explained by the current flows in the oscillator. Figure 3.6 shows an operation of the injection-locked oscillator without injection when $-\pi/2 < \phi_{osc} < \pi/2$. For $-\pi/2 < \phi_{osc} < \pi/2$, the oscillator discharges C_{outn} and charges C_{outp} and their current flows, i_{outn} and i_{outp} are shown in Fig. 3.6 (b). Let us take a look at the change of the output voltages V_{outn} and V_{outp} from t_1 to $t_1 + t_{injw}$ as shown in Fig. 3.6 (a). When the output voltages are $V_{outn\_t_1}$ and $V_{outp\_t_1}$ at t_1, the output voltages at $t_1 + t_{injw}$ can be expressed as follows:

$$V_{outn} = V_{outn\_t_1} + \frac{1}{C_{outn}} \int_{t_1}^{t_1+t_{injw}} i_{outn}\, dt \tag{3.4}$$

$$= V_{outn\_t_1} + \frac{1}{C_{outn}} \int_{t_1}^{t_1+t_{injw}} -|i_{outn}|\, dt \tag{3.5}$$

$$V_{outp} = V_{outp\_t_1} + \frac{1}{C_{outp}} \int_{t_1}^{t_1+t_{injw}} i_{outp}\, dt \tag{3.6}$$

$$= V_{outp\_t_1} + \frac{1}{C_{outp}} \int_{t_1}^{t_1+t_{injw}} |i_{outp}|\, dt \tag{3.7}$$

In Eq. 3.5 the negative sign of the integral means that the load capacitor, C_{outn}, is discharged and then its output voltage, V_{outn}, becomes low. On the contrary, C_{outp} is charged and V_{outp} becomes high in Eq. 3.7. The change of the output voltages V_{outn} and V_{outp} from t_2 to $t_2 + t_{injw}$ can be also obtained by replacing the subscript, t_1, with t_2 in Eq. 3.5 and 3.7, respectively. That is, it is the natural operation of the oscillator without injection that C_{outn} is discharged and C_{outp} is charged for $-\pi/2 < \phi_{osc} < \pi/2$.

Let us consider the oscillator under the injection. When an injection pulse with the pulse width, t_{injw}, is inputted at t_1, the switch connecting the both outputs is short and the current flows through the switch as shown in Fig. 3.7. Since V_{outn} is higher than V_{outp}, the current, i_{inj}, due to the injection flows from C_{outn} to C_{outp} and the changes of the output voltages can be expressed as follows:

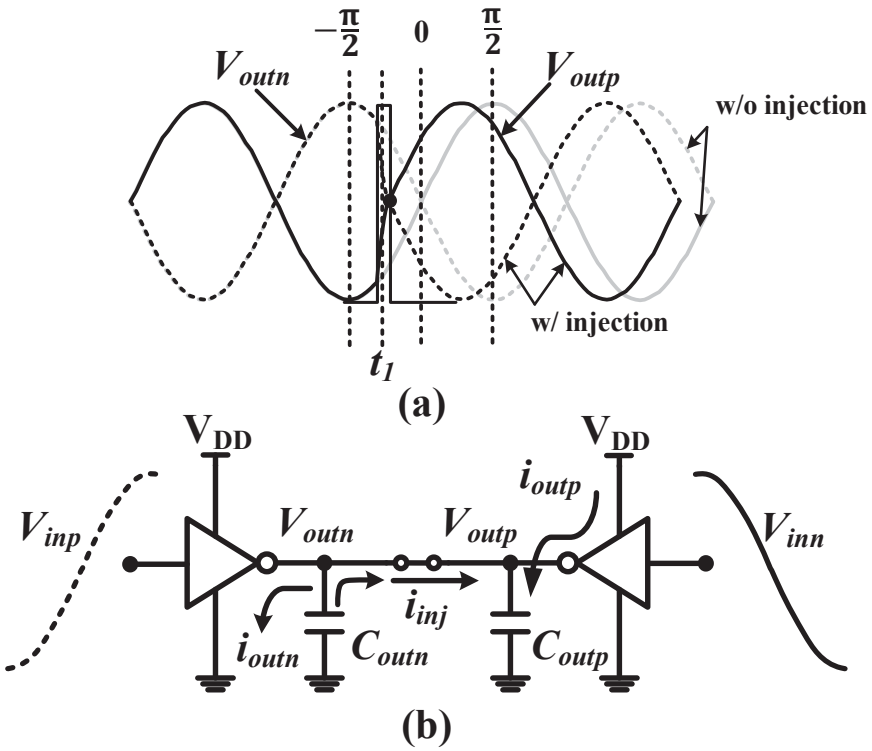


Figure 3.7: Current flow when an injection signal is inputted at $-\pi/2 < \phi_{osc} < 0$.

$$V_{outn} = V_{outn\_t_1} + \frac{1}{C_{outn}} \int_{t_1}^{t_1+t_{injw}} \{-|i_{outn}| - |i_{inj}|\}\, dt \tag{3.8}$$

$$V_{outp} = V_{outp\_t_1} + \frac{1}{C_{outp}} \int_{t_1}^{t_1+t_{injw}} \{|i_{outp}| + |i_{inj}|\}\, dt \tag{3.9}$$

In Eq. 3.8 and 3.9, the sign of the current, i_{inj}, originated by the injection pulse is the same of the current flows without the injection and then helps the natural changes of the output voltages to speed up, such that the oscillator can be easily locked.

Meanwhile, the injection for $0 < \phi_{osc} < \pi/2$ as shown in Fig. 3.8 works obviously different with the injection at t_1. When an injection pulse is inputted at t_2, that is, within $0 < \phi_{osc} < \pi/2$, V_{outp} is higher than V_{outn} and then the current, i_{inj}, due to the injection flows from C_{outp} to C_{outn} and this direction is

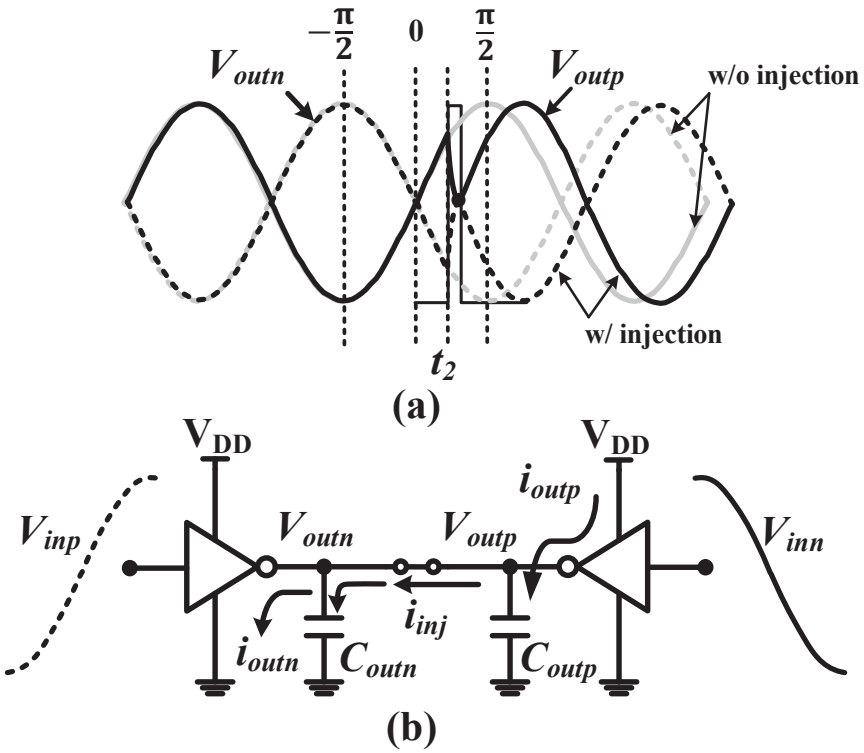


Figure 3.8: Current flow when an injection signal is inputted at $0 < \phi_{osc} < \pi/2$.

opposite to the direction of the currents, i_{outn} and i_{outp}, of the oscillator. The output voltages are expressed as follows:

$$V_{outn} = V_{outn\_t_2} + \frac{1}{C_{outn}} \int_{t_2}^{t_2+t_{injw}} \{-|i_{outn}| + |i_{inj}|\}\, dt \tag{3.10}$$

$$V_{outp} = V_{outp\_t_2} + \frac{1}{C_{outp}} \int_{t_2}^{t_2+t_{injw}} \{|i_{outp}| - |i_{inj}|\}\, dt \tag{3.11}$$

As mentioned above, it is natural that the output, V_{outn}, goes down and the output, V_{outp}, goes up when $0 < \phi_{osc} < \pi/2$ without the injection. However, the injection within $0 < \phi_{osc} < \pi/2$ disturbs the natural movement of the oscillator, that is, the injection pulse forces the outputs to move to the opposite such that the outputs can be the same. If the on-resistance is low enough, the current, i_{inj}, is larger enough than i_{outn} and i_{outp} and then the oscillator will be locked

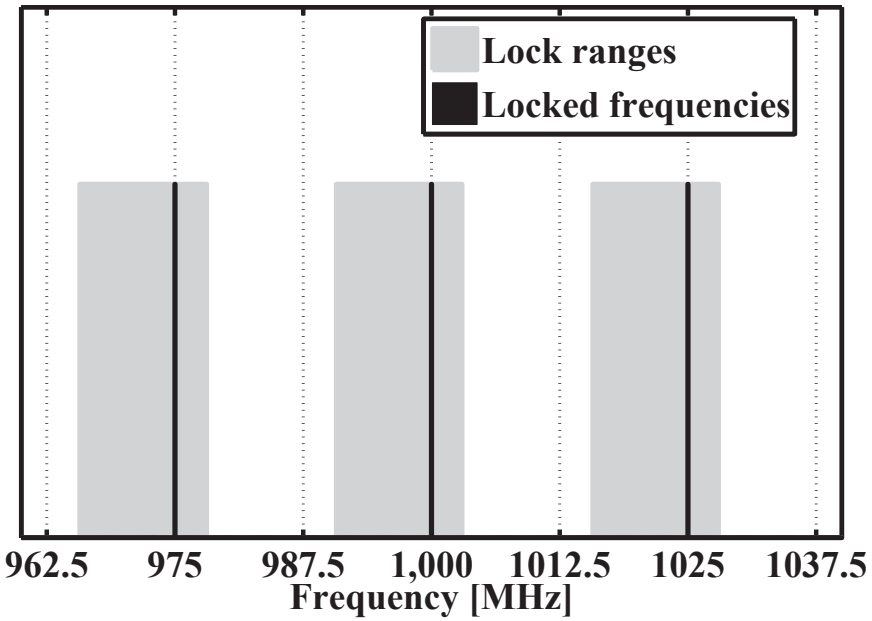


Figure 3.9: Simulation results on asymmetric lock ranges and locked frequencies.

within t_{injw}. Once the size of the switch for the injection is chosen, the size can not be changed depending on the oscillator's condition, which the oscillator has a little lower or higher frequency with respect to the desired frequency. Under a certain size of the switch and a fixed pulse width, it is clear that the injection at $-\pi/2 < \phi_{osc} < 0$ makes the oscillator locked easier than the injection at $0 < \phi_{osc} < \pi/2$ does. In other words, the lock range under $-\pi/2 < \phi_{osc} < 0$ would be substantially wider than the one under $0 < \phi_{osc} < \pi/2$ under the same pulse width and on-resistance. Thus, the lower lock range is asymmetric to the upper lock range.

Figure 3.9 shows simulation results of a 3-stage injection-locked ring oscillator, which is shown in Fig. 3.2. The black lines indicate the locked frequencies and the gray lines are the frequencies which the oscillator can be locked, that is, the lock ranges. The frequency of the injection signal is 50MHz. The oscillation frequencies are examined between 962.5 MHz and 1037.5MHz. Figure 3.9 shows that the oscillator has three locked frequencies and its respective lock ranges within the simulated frequency range. Their multiplication ratios are 19.5, 20,

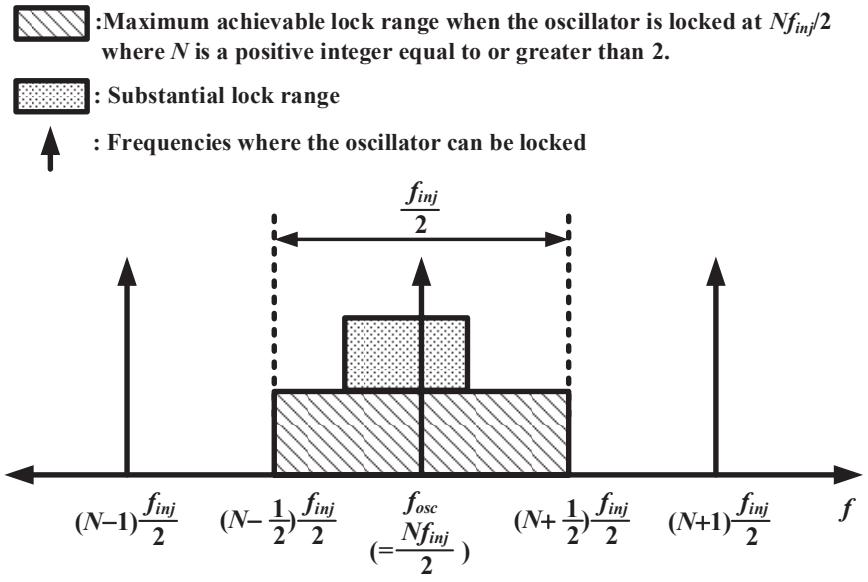


Figure 3.10: Ideal lock range of the injection-locked ring oscillator.

and 20.5, respectively. In each lock range, the lower lock range are wider than the upper lock range. For example, in the case of 1000MHz the lower lock range is 9.7MHz but the upper lock range 2.9MHz. The simulation results also give very good agreement with the results derived in Sec. 3.2.

3.4 Summary

In this chapter, the maximum achievable lock range in the injection-locked ring oscillator was derived. The lock range is shown in Fig. 3.10. The lock range is inversely proportional to the multiplication ratio of the injection signal to the oscillation frequency. The lock range is derived under the ideal condition, which the power of the injection signal is strong enough to lock the ring oscillator in a short pulse width. Substantially, the injection signal is inputted to the ring oscillator through the switch. When the injection power is not transferred enough to the injected stage due to the on-resistance of the switch, the ring oscillator may not be locked. As the switch size becomes large, the lock range would become wider but the oscillation frequency under the same current would be lowered due

to the increase of the parasitic capacitance of the switch.

The lock range is asymmetric to the oscillation frequency since the injection operation is opposite to the natural movement of the oscillator for $0 < \phi_{\mathrm{osc}} < \pi/2$ and the lock range would become narrower than the ideal lock range. Moreover, since the ring oscillator generally has poor noise characteristic, it would be quite difficult to achieve the high multiplication ratio.

Chapter 4

Injection-Locked Charge Pump Phase-Locked Loop with a Replica Ring Oscillator

This chapter reviews the conventional phase-locked loops and introduces the proposed injection-locked charge pump phase-locked loop with a replica ring oscillator. The proposed injection-locked loop is introduced and verified by a large number of simulations to secure tolerance to process, temperature, and power supply variations. Moreover, it was fabricated in a standard 90nm CMOS process and its measurement result is compared with the conventional phase-locked loops.

4.1 Conventional Phase Locked Loop

For a few decades, the charge-pump phase-locked loops (CPPLLs) were the main current of frequency synthesizer and clock generator. They are still most commonly used since they provide high stability and reasonable phase-noise characteristics. Many of them use an integer-N divider. The output frequency step of Integer-N PLLs is restricted to the reference frequency. In order to provide narrower output frequency step, the lower reference frequency is required such that the division ration increases and then results in increase of phase noise. To

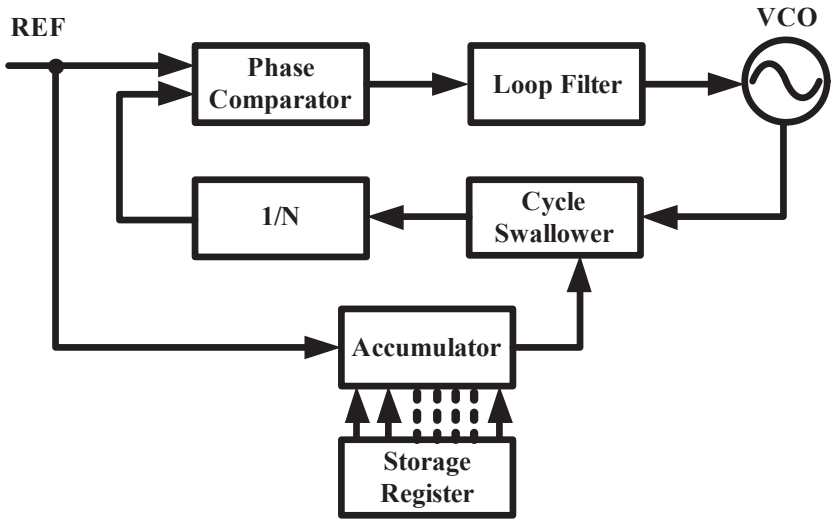


Figure 4.1: Fractional-N phase-locked loop.

avoid these drawbacks, a PLL with a fraction-N divider was disclosed as shown in Fig. 4.1 [69]. Fractional-N PLLs switch the division ratio between N and N+1 to obtain the fractional division ratio and are widely used as a frequency synthesizer. But these periodic switching produces the sideband noise called fractional spur. This problem was alleviated by applying a $\Delta\Sigma$ modulation concept [70] to a fractional-N PLL [71]. Fractional-N and $\Delta\Sigma$ Fractional-N PLLs utilize filters such as FIR Filters to further alleviate noises [72]- [76]. They generally consume large power above 10mW for about $1 \sim 2$GHz outputs. Fractional-N PLLs with relatively low power consumption and small occupied area were also introduced but do not provide good phase noise characteristics [77] [78].

With the development of the CMOS technology, the merit of digital technology in fine process increases and has then led many analog circuits to be implemented by digital circuits. Some or all components of the phase-locked loops have also been tried to be replaced by digital circuits as shown in Fig. 4.2. The oscillators are replaced to digitally-controlled oscillators, which compose of a digital-to-analog converter and a voltage-oscillator or has a digitally-controlled capacitor-bank, a varactor, or current sources [79]- [84]. Analog phase-frequency detectors can be also replaced to a digital phase-frequency detector, and a counter

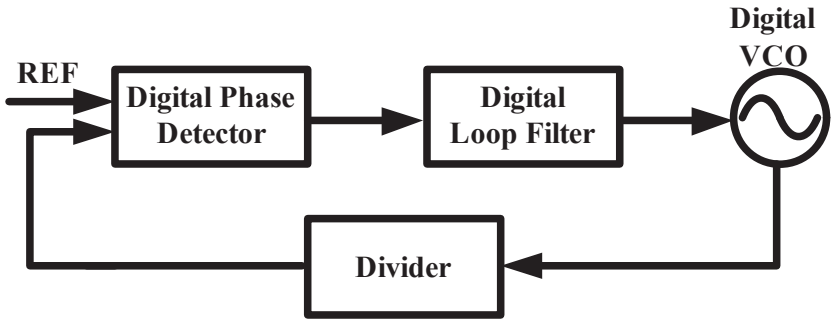


Figure 4.2: All digital phase-locked loop.

or a time-to-digital converter [85]- [88]. Digital PLLs utilize the benefits of CMOS scaling and then became one of dominant methods used in the wireless communication industry. They are suitable to be implemented in fine CMOS technology. However, digital and all digital phase locked loops also require high power consumption and large area to obtain low phase noise [89]- [93]. Hong presented a digital PLL with low power consumption and small occupied area but it shows poor phase noise characteristics [94].

The realignment by injection locking the oscillator to the reference was published to reduce the phase noise introduced by the oscillator [95]. As mentioned in Chapter 2, the phase noise of the injection-locked oscillator approaches the phase noise of the injection signal. Most of injection-locked oscillators are used not as frequency multipliers [27] [31] [96] [97] but as frequency dividers [33]- [36] [98]- [102] replacing the current mode logic(CML) frequency dividers, which consume large power especially at high frequencies [103]. Though the injection-locked oscillators may have better noise performance than injection-less oscillators, it is proper to be carefully used in a phase-locked loop to provide better performance, stability, and reliability. When an injection-locked oscillator is incorporated with conventional PLLs not as a divider but as a main oscillator, the PLLs may have critical problems in stability and reliability.

When an injection-locked oscillator is used as a main oscillator in conventional PLLs, the PLLs may suffer from the confliction between phase realignments by a phase-locked loop and a pulse injection. The phase confliction is caused by phase realignments at two different points, since the PLL tries to realign the phase of a

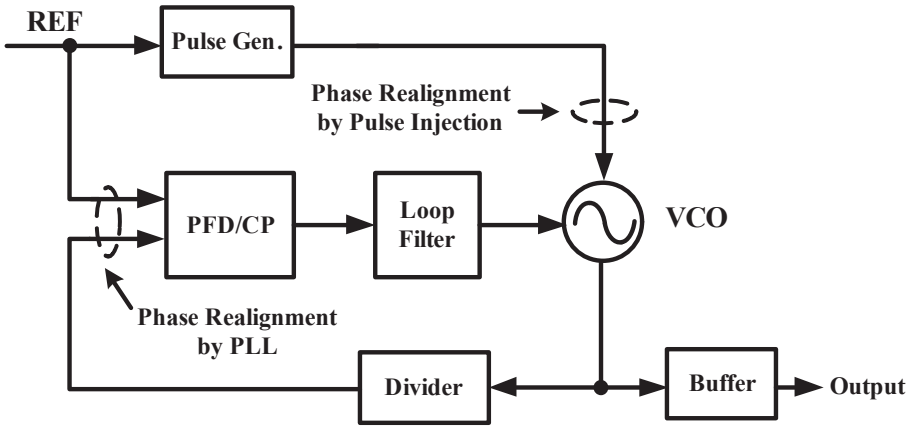


Figure 4.3: Phase confliction due to pulse injection in a conventional PLL.

divider output at the input of phase-frequency detector while the pulse injection tries to realign phase of oscillator output at the injected stage, as shown in Fig. 4.3. This confliction may cause the PLL to fail to maintain lock state. Thus, any supplemental phase controller is required to prevent such confliction [29] [31].

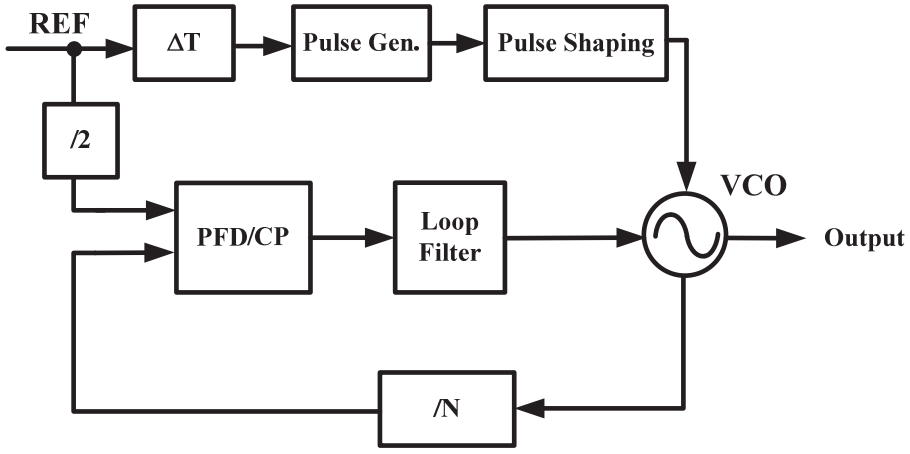


Figure 4.4: Injection-locked PLL with a pulse timing control.

The first method to avoid the phase confliction is to directly control the injection timing (ΔT) as shown in Fig. 4.4 [31]. However, it is not facile to exactly control the injection timing and to compensate temperature and voltage varia-

tions due to various noises under operation.

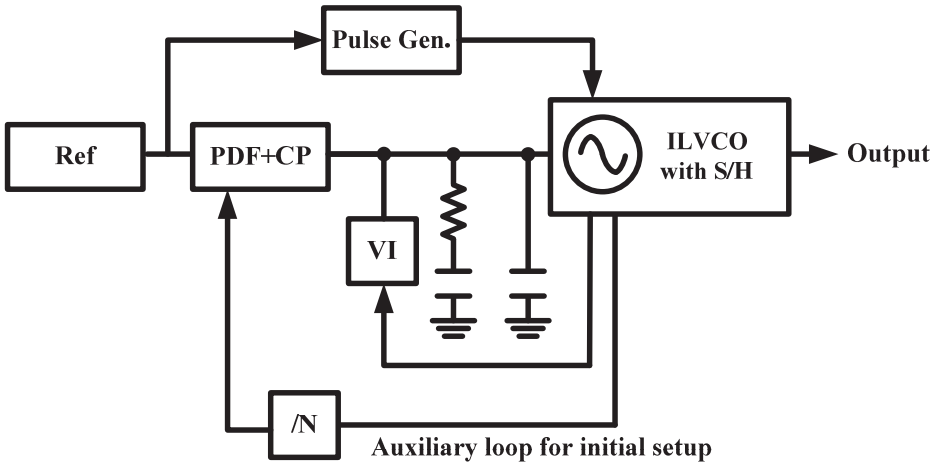


Figure 4.5: Injection-locked PLL with self-aligned injection window.

Liang introduced an injection-locked PLL with self-aligned injection window as shown in Fig. 4.5 [29]. The injection-locked PLL is composed of an injection-locked oscillator with a sample-and-hold (S/H) circuit and a conventional loop with PDF, CP, and a divider for initial setup. The S/H provides voltage-to-current converter (VI) with the phase information of the injection-locked oscillator when the injection signal is inputted. The VI converts the voltage phase error signal to the current signal such that the phase of the oscillator is realigned. However, the PLL has a narrow loop bandwidth for stability. Once the oscillator is locked at undesired frequency due to high frequency noises, the PLL may not return the desired frequency.

As shown in Fig. 4.6, the other method to avoid the phase confliction has been introduced in [104]. It adopts a replica of the oscillator to distinguish the injection-locked oscillator with the loop of the PLL. And it includes the calibration phases to compensate the frequency difference between two oscillators. However, when the supply and temperature variation changes excess the calibration after calibration or the reference clock is changed, the PLL should be re-calibrated. Especially, even small increment of the supply voltage increases the 1LSB of DAC and *kvco* of the oscillator, such that it may cause the ILPLL to lose lock.

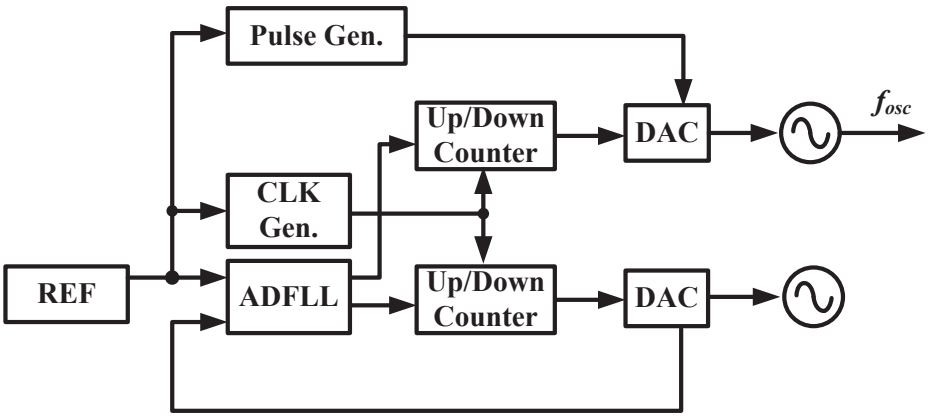


Figure 4.6: Phase realignment in a conventional PLL.

Moreover, when the frequency multiplication ratio is increased, the time required to control the oscillator becomes longer while the lock range becomes narrower. Thus, this configuration is not suitable for high frequency multiplication ratio.

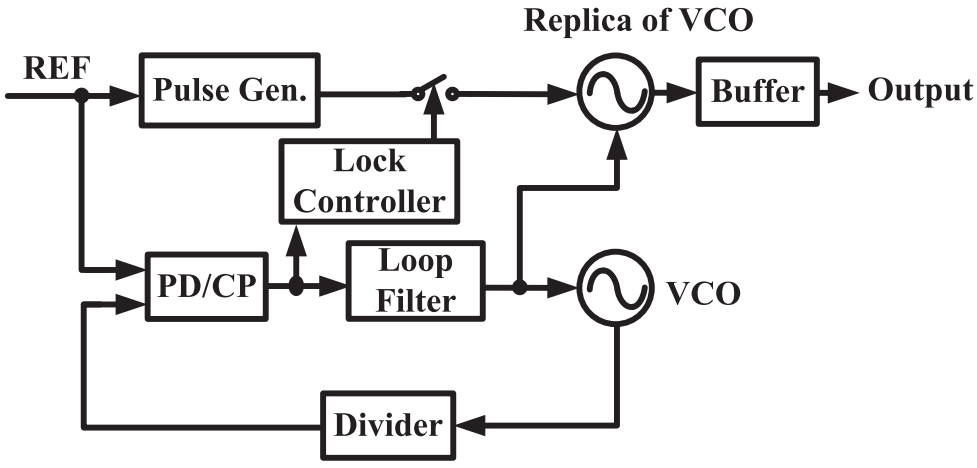


Figure 4.7: Proposed injection-locked CPPLL with a replica of the ring oscillator.

This thesis presents an injection-locked PLL without any calibration phases, which has two loops separated into a conventional charge-pump phase-locked loop (CPPLL) and an injection loop as shown in Fig. 4.7 so as to avoid the phase confliction and to be tolerable to process-voltage-temperature (PVT) vari-

ations. Well-designed two ring oscillators themselves can be considerably tolerant to process variation to maintain lock state while they occupy large area. Continuous phase tracking by a conventional CPPLL can provide robustness to supply voltage and temperature variations.

4.2 Design of Injection-Locked Oscillator

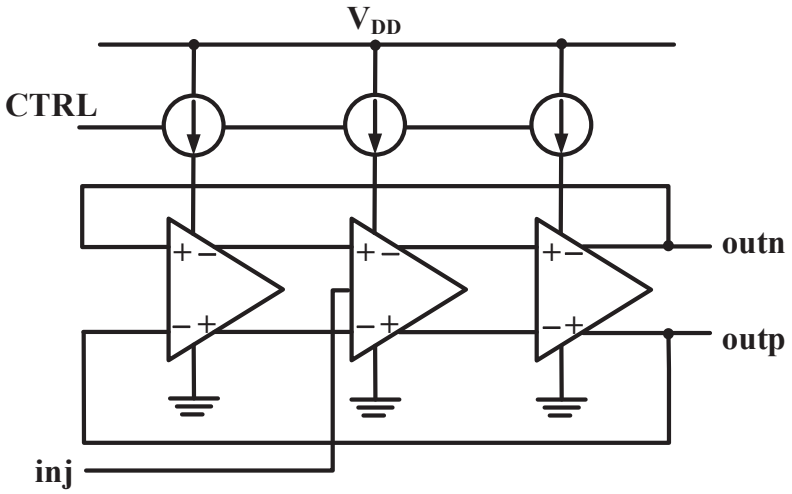


Figure 4.8: Block diagram of 3-stage injection-locked ring oscillator.

An injection-locked ring oscillator is a 3-stage differential ring oscillator as shown in Fig. 4.8. A periodic pulse is injected to the output of its middle stage. The target frequency is 1GHz and the division ratio in the PLL is 20. In the case of the 4-stage differential ring oscillator, it is possible to input the injection signal into two stages at the same time such that the substantial lock range will become wider than the 3-stage oscillator. However, the pulse injection is a kind of disturbance in the view of the ring oscillator itself. The even-stage oscillator may latch up or down due to unexpected external disturbance. Thus, in order to secure stable oscillation, the 3-stage ring oscillator is chosen.

Figure 4.9 shows the one delay stage of the ring oscillator with one current source. The oscillation frequency is controlled by one current source. As described

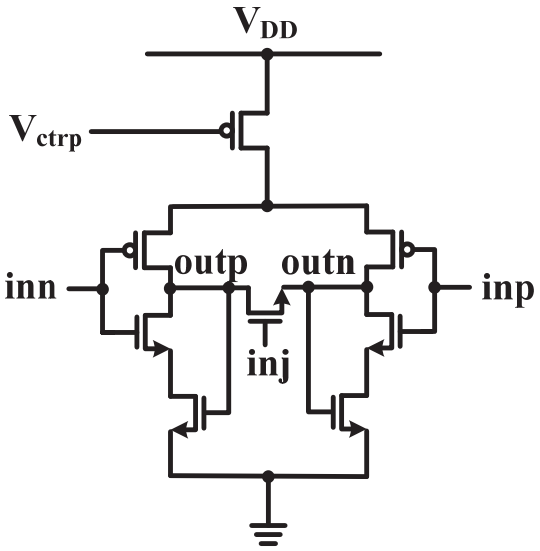


Figure 4.9: Delay stage of the injection-locked ring oscillator with one current source.

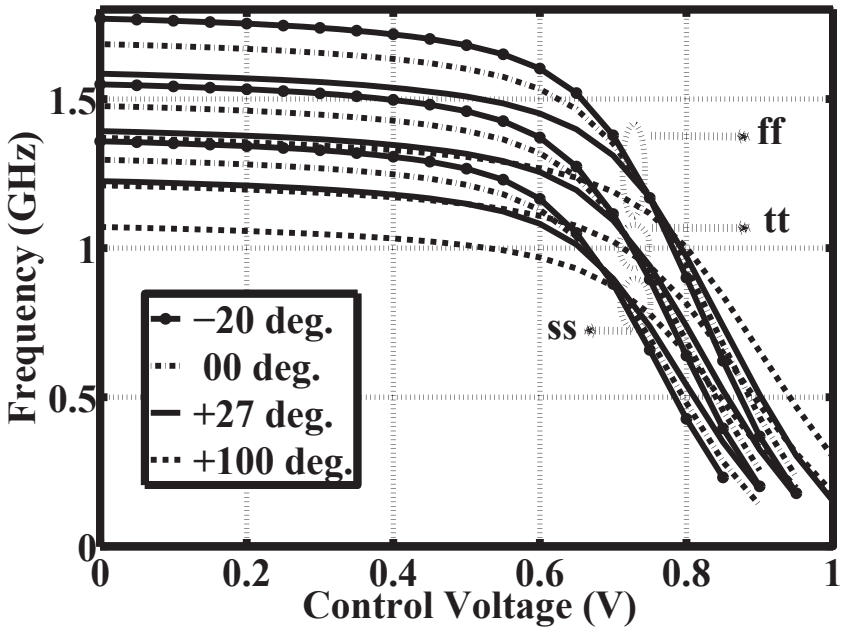


Figure 4.10: Tuning ranges of the 3-stage injection-locked ring oscillator.

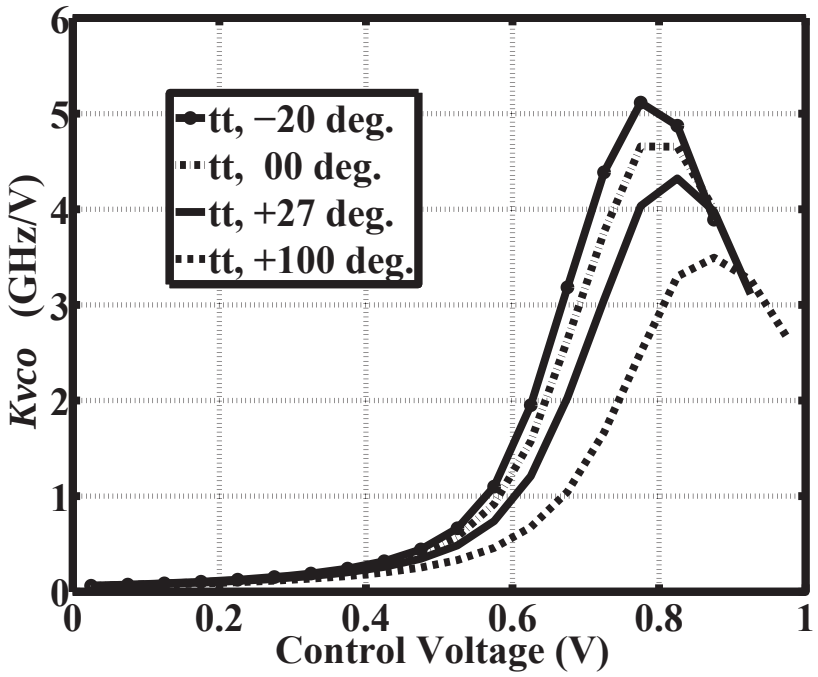


Figure 4.11: Oscillator gain, K_{VCO}, of the 3-stage injection-locked ring oscillator.

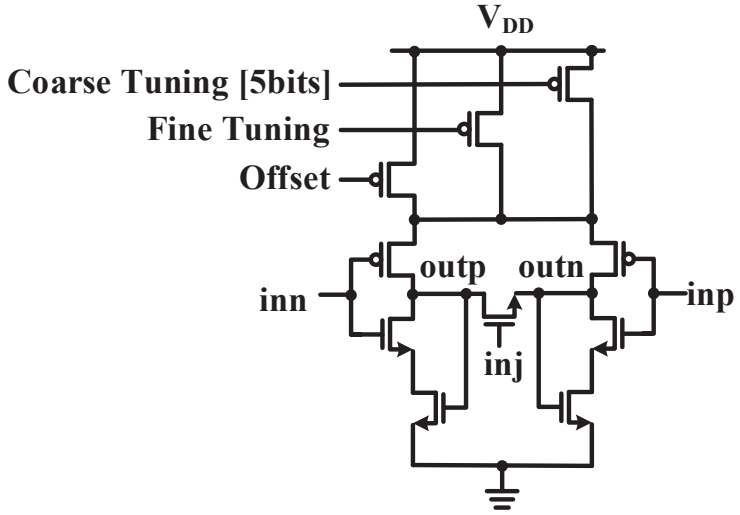


Figure 4.12: Delay stage of the injection-locked ring oscillator with multiple current sources.

in Chapter 2, the ring oscillators have generally large voltage gain, K_{VCO}, and are highly sensitive to PVT variations. Thus, in design of the ring oscillator, the corner analysis for process variation are desirable to be performed considering temperature variation. Figure 4.10 shows tuning ranges of the 3-stage injection-locked ring oscillator in corner analyses depending on temperature variation. In the typical-typical (typical NMOS-typical PMOS, tt) corner, the target oscillation frequency is designed to be almost fixed at a control voltage (focus control voltage) - in this case, 0.72V - though the temperature changes. The focus becomes higher in the fast-fast (ff) corner and lower in the slow-slow (ss) corner. In the all critical corners and temperature variation from -20 to 100 degrees, the oscillator can secure the target frequency. However, as shown in Fig. 4.11, the oscillator gain has a few GHz/V. This is general in the ring oscillator since the oscillator gain is around $2 \sim 4$ times as high as that of the maximum oscillator frequency. The large oscillator gain requires the large capacitance of the loop filter.

In order to reduce the oscillator gain, the current source of the oscillator is divided into 3-kinds of current sources as shown in Fig. 4.12. The first current source for an offset frequency provides the lower limit of the output frequency. This also allows settling time of the coarse tuning to be shortened. The second current source for coarse tuning is controlled by 5 bits. The third current source for fine tuning is connected to the output of the loop filter.

Figure 4.13 shows oscillating frequencies over each coarse tuning step. The frequency ranges of each coarse tuning step are the coverage of fine tuning current source. During the coarse tuning, the oscillator is designed to lock at the 4th or 5th coarse step. Figure 4.14 shows the oscillation frequency and the oscillation gain over the fine tuning voltage at the 5th coarse step. The oscillation gain became below 400MHz/V from a few GHz/V. Through these configurations, K_{vco} of the oscillator can be lowered such that it results in the small area of the loop filter. When the oscillator controlled by one current source, the total required capacitance for third order loop filter is about 2.85μF but the oscillator with 3 kinds of current sources requires about 0.5μF.

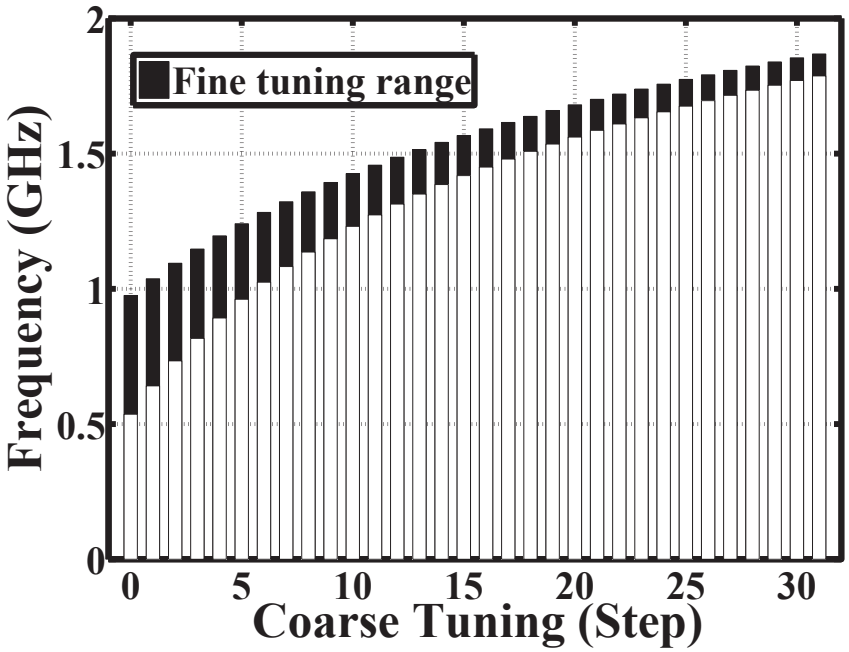


Figure 4.13: Coarse tuning and fine tuning ranges of the injection-locked ring oscillator.

4.2.1 Process Variation

First of all, to design the ring oscillator, the frequency variations due to the process variation is considered . In order to investigate the frequency difference between the oscillators, it is considered about the effects due to sizes of delay stages and current source, respectively. Figure 4.15 shows the frequency variations and current consumptions with respect to the delay sizes of the oscillator. The sizes are expressed by considering only the channel lengths and widths. Note that only delay stages are affected by process variation. As the sizes increases, the frequency variation decreases but the current consumption increases. Thus, the size of the delay stages should be determined by considering not only area but also current consumption.

Figure 4.16 shows the frequency variation with respect to sizes of the current sources and all components of the oscillator. Though large sizes results in small frequency variation, it will lead to larger occupied area and current consumption.

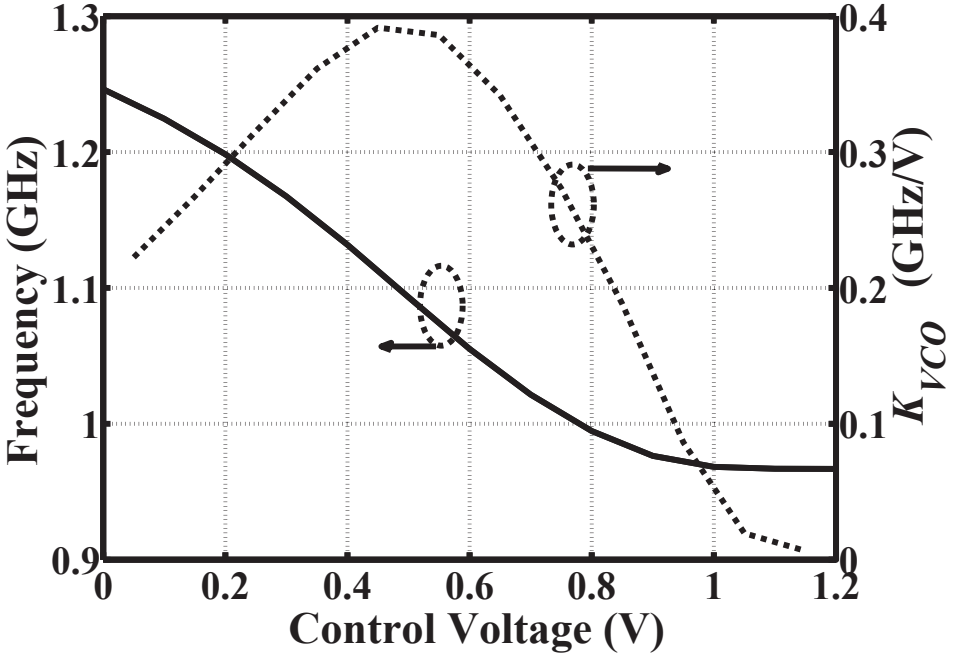


Figure 4.14: Oscillation frequency and oscillator gain over the fine tuning voltage.

It is now considered the relationship between lock range and the size of the switch for the injection. The referential size is 100nm of the channel length and 1um of the width. Figure 4.17 shows the relationship between lock ranges of the injection-locked oscillator and sizes of switches. As expected in Chapter 3, the lock ranges are asymmetric. As the fingers of the switch increase, the lock range increases. However, they are saturated at certain size of the switch. It is considered why the injection current is saturated under a specific oscillation frequency even though the on-resistance still decreases, since the output voltages and the pulse width of the injection are finite. The larger sizes result in wider lock range and also incur the increase of the current consumption due to the increase of the parasitic capacitance of the switch. The lock range of the injection-locked oscillator in this paper is designed to be 991.5∼1006.2MHz.

According to the above results, the ring oscillator is designed to be tolerable to process variation. However, every system suffers voltage and temperature variations. Thus, the oscillators should be checked about voltage and temper-

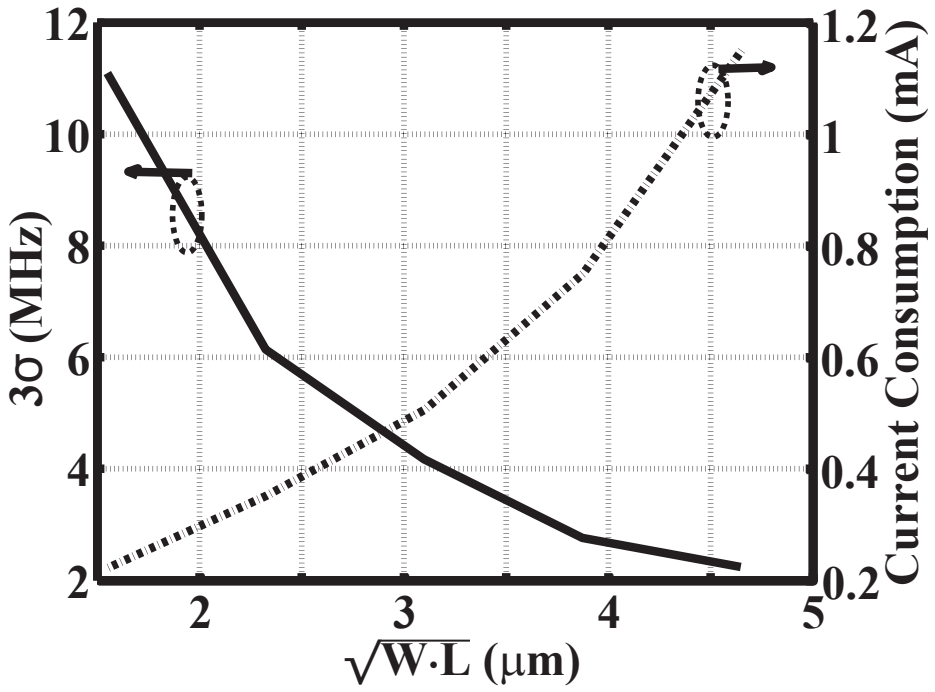


Figure 4.15: Monte Carlo simulation results on the frequency variations and current consumptions with respect to the delay sizes of the oscillator.

ature variations under the local process variation. Monte Carlo simulations on two oscillators are required to show whether the difference of the both oscillation frequencies is within the lock range. Tolerances to supply voltage and temperature variations are investigated respectively. Furthermore, since two oscillators suffer from the process variation, there is a frequency offset between the oscillators. Thus, the temperature dependency of the two oscillators under the process variation is also investigated by Monte Carlo simulation.

Ring oscillators are generally sensitive to PVT variations. In the proposed injection-locked CPPLL, voltage-temperature variations are less problematic than process variation since two oscillators will suffer the same variations and the proposed injection-locked CPPLL can be tolerable to variations within fine-tuning coverage. However, the local process variation may be critical because the offset frequency between two oscillators is not eliminated without any compensation and the injection pulse may fail to lock the replica when there is too large fre-

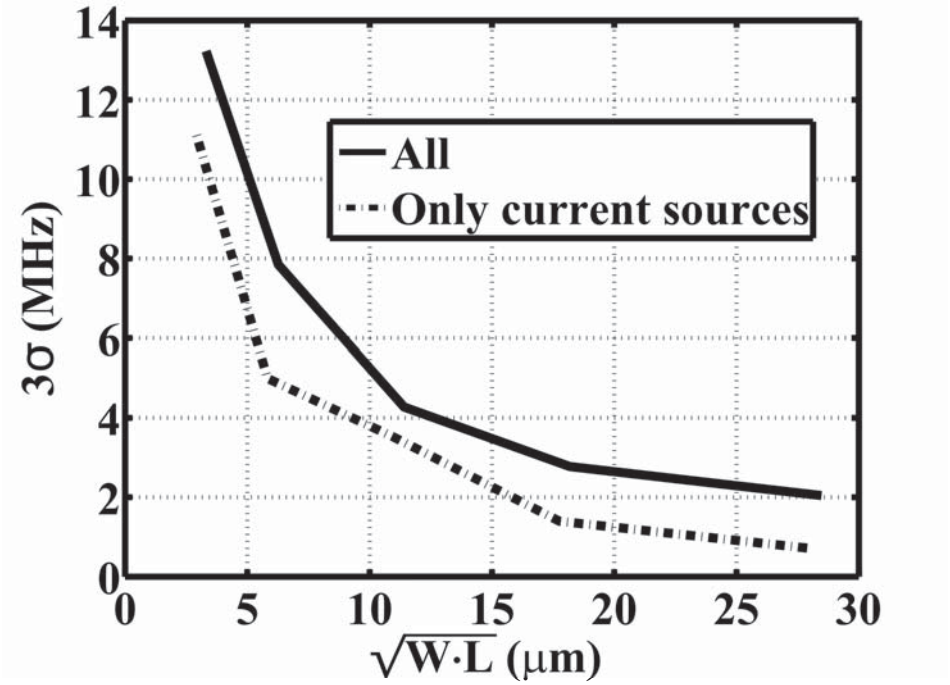


Figure 4.16: Monte Carlo simulation results on the frequency variation with respect to sizes of the current sources and all components of the oscillator.

quency difference between the ring oscillator and its replica. It may be also possible to calibrate the frequency difference even though it is hard to compensate frequency difference in the oscillators to be small enough to achieve stable lock state. However, it brings out another problem whether it can guarantee that the compensation circuit is able to maintain the frequency difference small enough when the oscillators further suffers voltage-temperature variations. Thus, it is desirable to design the oscillators tolerable to process variation such that the frequency difference between them due to the process variation is within the lock range to ensure the stable injection lock state.

Monte Carlo simulation is performed to investigate the frequency difference between the oscillator and its replica due to process variation. Figure 4.18 shows the Monte Carlo simulation results when the oscillation frequency is 1GHz. The mean, μ, and the standard deviation, σ, of the difference between the oscillation frequencies of two oscillators are 1.74MHz and 1.32MHz, respectively. The simu-

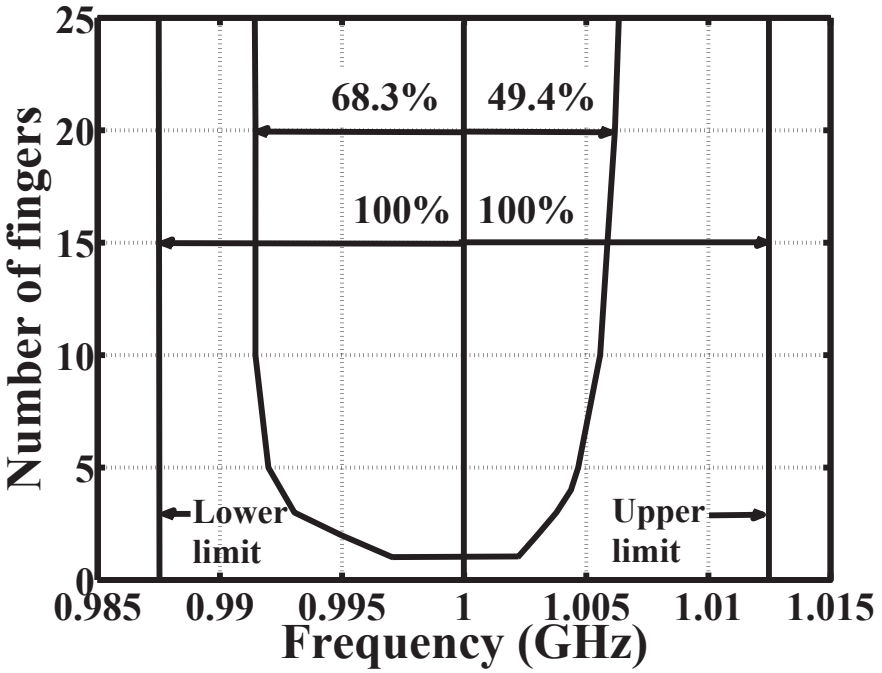


Figure 4.17: Lock ranges of the injection-locked oscillator with respect to sizes of switches.

lation results show that the frequency differences between the two oscillators are within 5.70MHz with a 99.7% (3 σ limit) probability. This corresponds 45.6% with respect to the maximum lock range, 12.5MHz, respectively. The frequency difference between the two oscillators is thus considered to have small enough to achieve stable lock state.

4.2.2 Power Supply Voltage Variation

In general, the oscillation frequencies of the ring oscillators are highly dependent on variation of the supply voltage. Tolerance to supply voltage variation in the ring oscillators is thus investigated. Figure 4.19 and 4.20 show free-running frequencies of the ring oscillator with respect to supply voltage (V_{DD}) variation of $\pm$10%. In spite of the supply voltage variation of $\pm$10%, the oscillator is able to cover the target frequency as shown in Fig. 4.19 and its oscillation frequencies seem to be linearly proportional to the supply voltage. For more detail, the

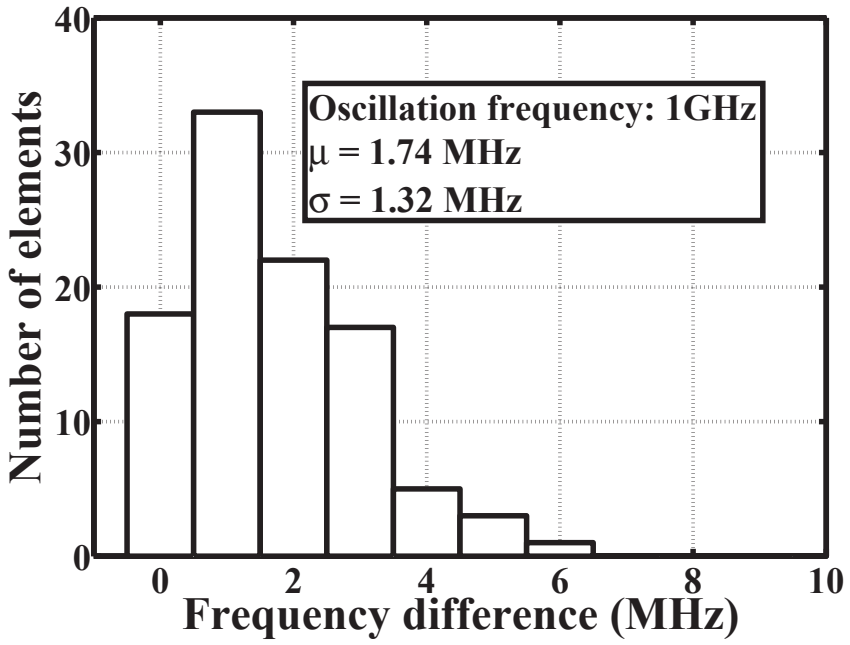


Figure 4.18: Monte Carlo simulation results on the frequency difference between the oscillator and its replica due to process variation.

changes of the oscillation frequencies with respect to the supply voltage variations are shown in Fig. 4.20, which provides the changes depending on fine tuning voltages. On the basis of fine tuning voltages, the oscillation frequencies are very linearly proportional to the supply voltages. It is thus considered that coverage against the supply voltage variation can be obtained by interpolation and extrapolation on the basis of fine tuning voltages. Its coverage results in 1.03V $\sim$ 1.24V. It occupies 17.5% of the regular supply voltage, 1.2V. An average of the frequency-to-supply voltage ratio is 1.32GHz/V, which can be used to estimate the tolerance range to temperature variation as described in the next section.

4.2.3 Temperature Variation

It seldom finds exact coverage over temperature variation in a PLL through simulations because temperature variation in a PLL leads the control voltage change

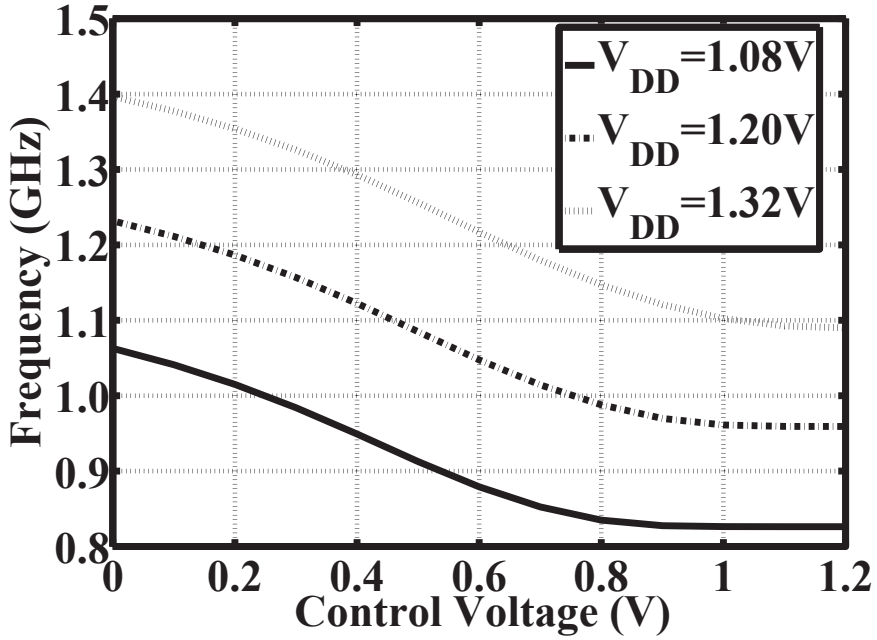


Figure 4.19: Free-running frequencies with respect to supply voltage (V_{DD}) variation.

of the oscillator to compensate the frequency change. When a PLL is locked at a desired frequency and after then temperature changes, the frequency of the oscillator will deviate from a desired the frequency and the control voltage will move to compensate frequency variation due to the temperature change. These trajectory of the frequency change due to temperature change appears a curve on the 3-dimension, which is composed of control voltage, temperature, and frequency. When this work is applied to find frequency difference between two oscillators thorough Monte Carlo simulation, the number of simulations will be enormously increased. Thus, this thesis verifies tolerance to temperature variation with the averages of frequency-to-voltage ratio and frequency-to-temperature ratio, which can reduce the number of the simulations and provide reasonable approximation.

First of all, temperature characteristic of the ring oscillator is investigated as shown in Fig. 4.21. It shows a quite linear variation over temperature. An average of the frequency-to-temperature ratio is 1.78MHz/°C. From frequency-to-temperature ratio and frequency-to-supply voltage ratio as obtained the previous

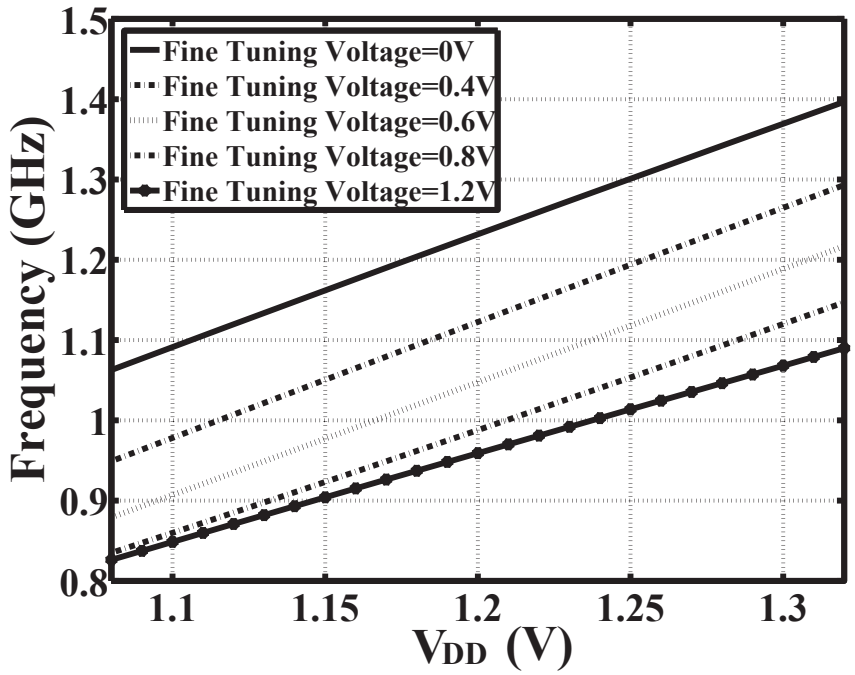


Figure 4.20: Free-running frequencies with respect to supply voltage (V_{DD}) variation.

section, the following relation can be derived:

$$\left(\frac{\Delta f}{\Delta V_{DD}}\right) / \left(\frac{\Delta f}{\Delta Temp}\right) = \frac{\Delta Temp}{\Delta V_{DD}} \tag{4.1}$$

The temperature-to-supply voltage ratio is 741.6°C/V. When the oscillator is tolerable to supply voltage of 0.21V, temperature tolerance of the oscillator is 155.7°C. The following investigation shows that this approach is quite reasonable.

Temperature characteristic between two oscillators thorough Monte Carlo simulation is investigated. Figure 4.22 shows frequency-to-temperature ratios of two oscillators in Monte Carlo simulation. The frequency-to-temperature ratios of two oscillators look identical over the whole fine tuning range. This means that the two oscillators would move on the almost same trajectory responding to temperature variation while they have frequency difference due to process variation.

Difference of average frequency-to-temperature ratios in two ring oscillators

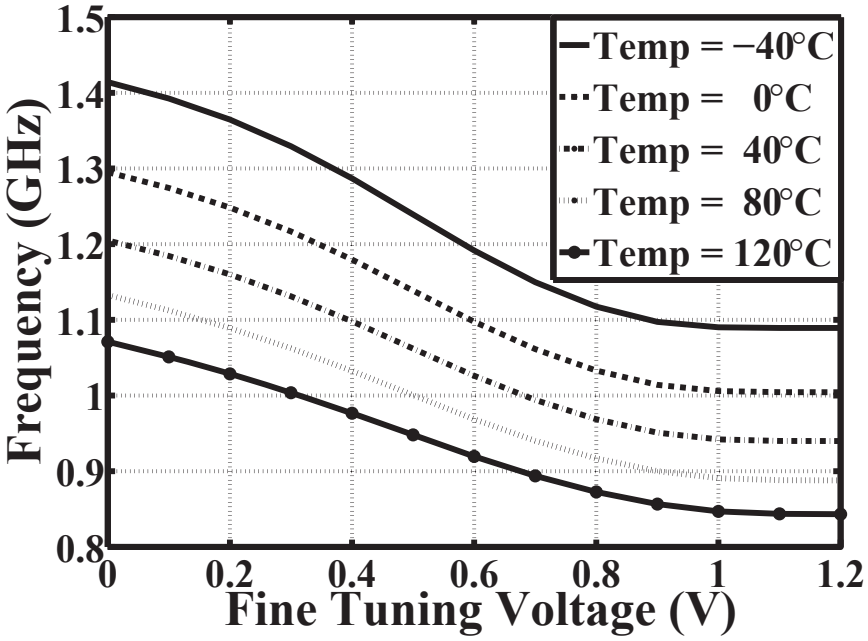


Figure 4.21: Oscillation frequency over temperature variation.

is shown in Fig. 4.23. The data was obtained by 2,500 simulations composed of 100 iterations in Monte Carlo simulation, which have 5 fine tuning voltages and 5 temperature variation. Monte Carlo simulation shows that frequency difference due to temperature dependence of the two oscillators is below 1.5MHz when temperature changes 150°C. The average of the difference is 2.08kHz/°C. Especially, the difference is proportional to the frequency difference due to process variation. Thus, the small offset frequency due to process variation will move on the almost same trajectory responding to temperature variation.

4.3 Implementation of the Proposed Injection-Locked CPPLL

Figure 4.24 shows the proposed injection-locked PLL which has a replica of the oscillator and separates the injection-locked oscillator from the phase-tracking loop of the PLL. The proposed injection-locked oscillator has three kinds of the

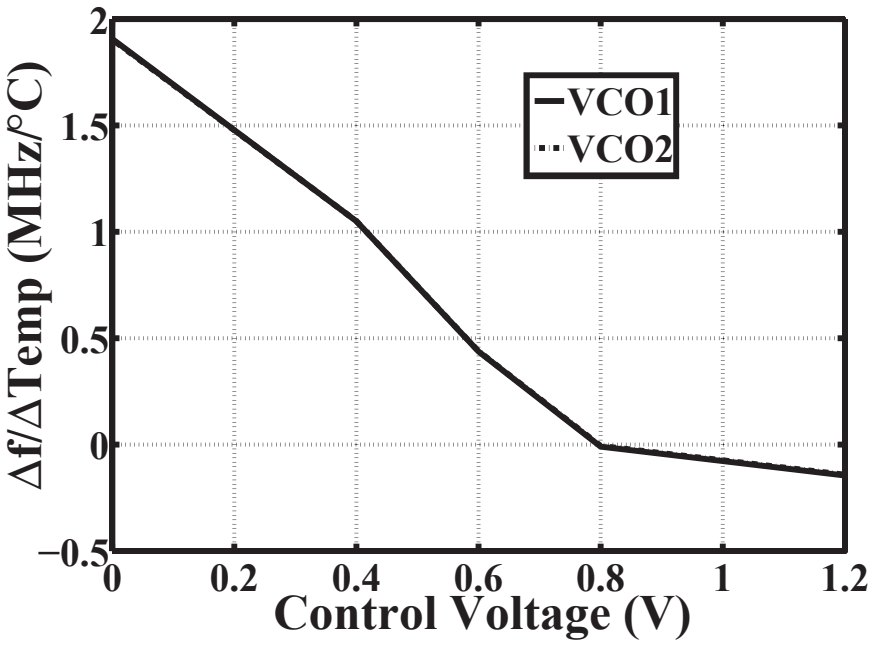


Figure 4.22: Frequency-to-temperature ratio of two oscillators in Monte Carlo simulation.

current sources. And two kinds of current sources except the offset current source should be controlled properly. In this section, the lock controller is introduced and then configuration and operation of the proposed injection-locked CPPLL are described.

4.3.1 Design of Lock Controller

The proposed injection-locked CPPLL is a combinational system of a conventional CPPLL and an injection-locked oscillator and takes advantage of their respective merits. The conventional CPPLL is stable but can not overcome conventional phase noise performance. The injection-locked oscillator is prone to be unstable, especially before the oscillator is locked, but once it is locked at a certain frequency, it has excellent phase noise performance. When the injection signal is inputted to the injection-locked oscillator in oscillating beyond the desired lock range or within undesired lock ranges, the injection-locked oscillator may get to

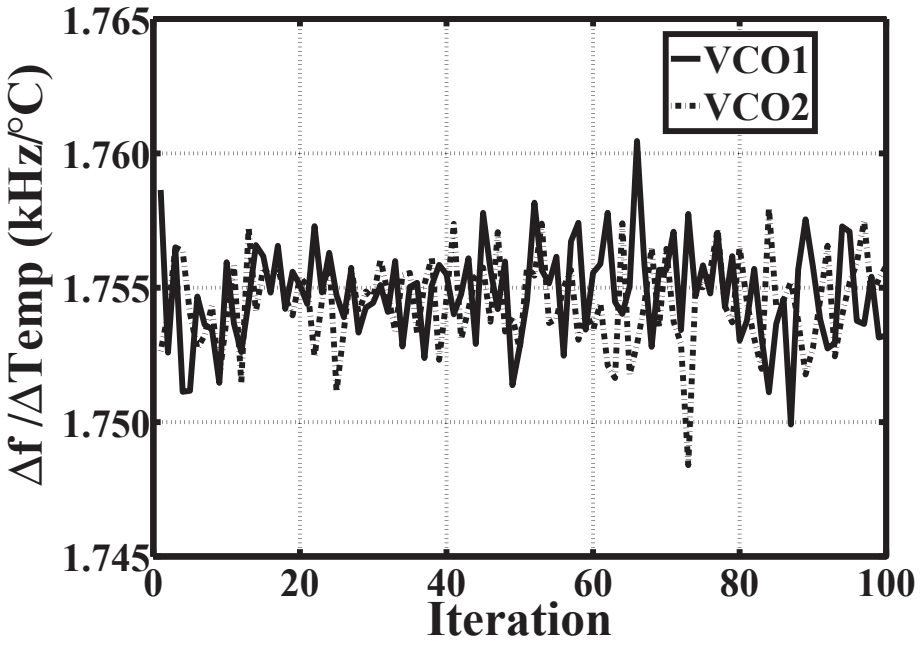


Figure 4.23: Difference between average frequency-to-temperature ratio in two ring oscillators (Monte Carlo simulations).

be unstable or be locked at undesired frequencies. These problems can be solved by adapting a lock controller, which controls the stable lock for the conventional CPPLL and the injection timing for stable lock at the desired frequency. Then, the injection-locked CPPLL can have stable lock state and excellent phase noise performance.

A basic concept of the lock controller is to compare the two input signals to determine which one has higher or lower frequency using k-bit counters and to decide whether the oscillator is locked. In the proposed injection-locked PLL, there are three essential points on the lock controller. The first is to lock the coarse tuning. The second is to lock the fine tuning. And the last is to determine when the injection signal is inputted to the oscillator. They are described in order.

First of all, it is described to lock the coarse tuning. Figure 4.25 shows a block diagram of a lock controller for coarse tuning. Unlike the conventional CPPLL, the loop filter of the ILPLL is initially connected to an initial voltage

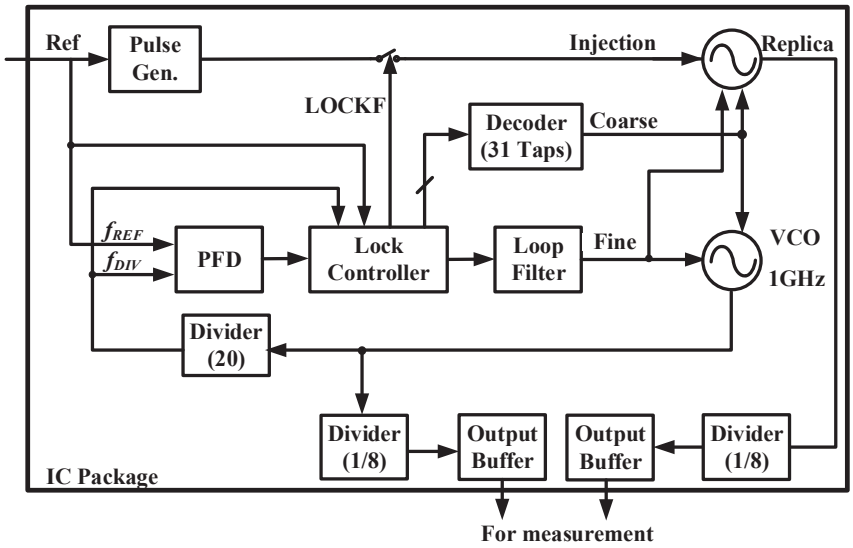


Figure 4.24: Proposed injection-locked CPPLL with a replica of the ring oscillator.

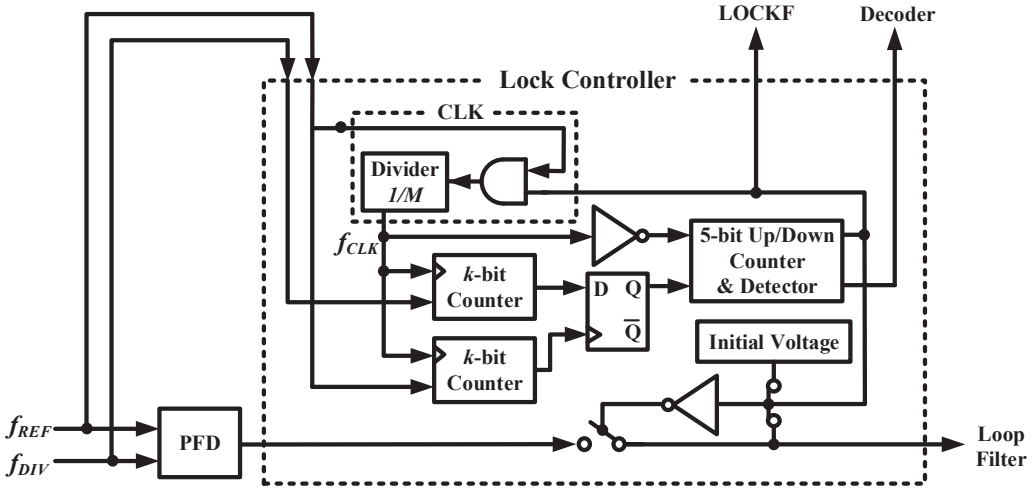


Figure 4.25: Block diagram of a lock controller for the coarse tuning.

for the coarse tuning. Thus, the oscillator can have the middle frequency of the each fine tuning range during the coarse tuning as shown in Fig. 4.13. The reference and the output of the divider are inputted to each k-bit counter. The

k-counters are activated during the half period of the clock, f_{CLK}. The other half clock is used for the up/down counter. The each k-counter starts to count the number of the rising edges of its input at rising edge of the clock and then outputs high when it becomes MSB. When the frequency of the reference is higher than the frequency of the divider output, the D-filp flop outputs low and then the up/down counter counts down to increase the frequency of the oscillator. The output of the up/down counter is converted from binary code to thermometer code in the decoder. Note that the oscillator has PMOS current sources and the low state thus turns on the current source to increase the frequency of the oscillator. When the frequency of the reference is lower than the frequency of the divider output, the D-filp flop outputs high and the up/down counter counts up to decrease the frequency of the oscillator. The output of the up/down counter is decoded to binary code in the decoder, which turns on or off the current sources for the coarse tuning of the oscillator. When the frequency of the divider output is most close to the frequency of the reference, the up/down counter repeats up and down in series and the detector outputs the lock alarm, LOCKC, when it detects a certain times of iteration. Then the coarse tuning process ends and the PFD and the loop filter are connected to start the fine tuning process. A clock of k-bit counters is obtained by dividing the reference clock without an external clock and its frequency, f_{CLK}, is $f_{REF}/(k+2)$ to complete k-bit counting for its half period. The number of bits of k-bit counters is a key factor to determine the clock frequency and the resolution of the frequency comparison. Thus, it should be selected very carefully.

In order to determine the number of bits, it is required to consider on delay effects, that is, the time differences from the rising edge of the clock to the first rising edges of the reference and the divider outputs, since it is not guaranteed that they have the same delay times and the different delay times may lead to different results under the same condition. In other words, there is a metastable range that may not make a proper decision based on the difference between the delay times of the input signals.

Figure 4.26 shows that the divider and the reference have the same frequency but the different delay times. Since the k-counters count the rising edges of the inputs during the high state of the clock, the delay times are defined as the time

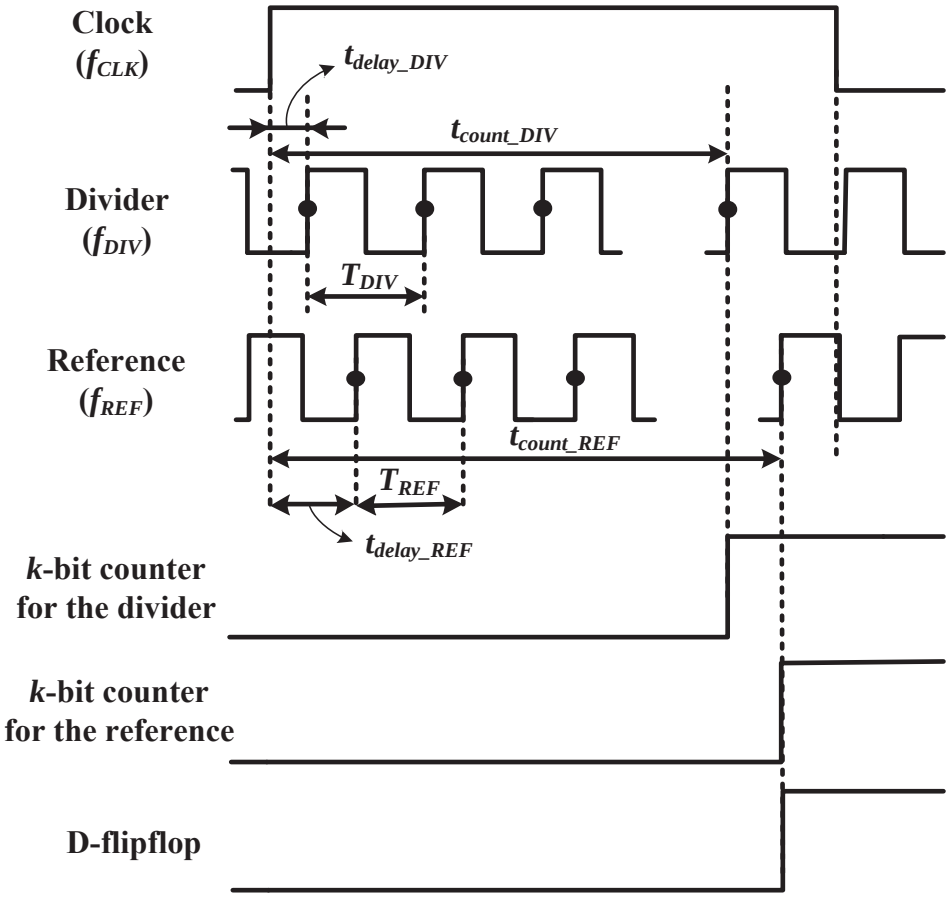


Figure 4.26: Timing chart of the signals for coarse tuning.

differences from the rising edge of the clock to the first rising edges of the reference and the divider outputs. t_{delay_REF} is the delay time of the reference with respect to the rising edge of the clock and t_{delay_DIV} is the delay time of the divider. In Fig. 4.26, they have the same frequency but the delay time of the divider is shorter than the reference. Thus, the k-counter for the divider reaches MSB and outputs high before the k-counter for the reference outputs high. Consequently, the D flip-flop outputs high and the up/down counter counts up to decrease the frequency of the oscillator. When the delay time of the reference is shorter than the divider, the up/down counter counts down and then the frequency of oscillator would be increased. Although they have the same frequency, the results become

different based on the their delay times.

The delay effects of the two input signals are considered in more detail. The two input signals, f_{REF} and f_{DIV}, in the lock controller can be expressed as T_{REF} and T_{DIV} obtained by taking their reciprocals, respectively. That is, T_{REF} and T_{DIV} are the periods of the reference and the divider output, respectively. t_{delay_REF} has a value between 0 and T_{REF} and t_{delay_DIV} has a value between 0 and T_{DIV}. And t_{count_REF} and t_{count_DIV} are the times that it takes for each counter of the reference and the divider to reach MSB, respectively. Thus, the times, t_{count_REF} and t_{count_DIV}, are as following:

$$t_{count\_REF} = T_{REF}(2^k - 1) + t_{delay\_REF} \tag{4.2}$$

$$t_{count\_DIV} = T_{DIV}(2^k - 1) + t_{delay\_DIV} \tag{4.3}$$

It should be noted that the up/down counter compares not T_{REF} with T_{DIV} but t_{count_REF} with t_{count_DIV}. The accuracy of frequency comparison in the up/down counter should be thus evaluated by considering the two input signals and their delay times at the same time. First of all, two cases are considered: the k-bit counter for the output of the divider outputs high first before the k-bit counter for the reference outputs high, and vice versa. The accuracy of frequency comparison is verified by applying the boundary conditions of t_{delay_REF} and t_{delay_DIV} to the two cases.

When the k-bit counter for the output of the divider outputs high first before the k-bit counter for the reference outputs high, the 5-bit up/down counter subtracts one from the output itself since the output of the divider is considered to have higher frequency than the reference. For proper decision, the following conditions should be thus satisfied in the first case at the same time.

$$t_{count\_REF} > t_{count\_DIV} \tag{4.4}$$

$$T_{REF} > T_{DIV} \tag{4.5}$$

For Eq. 4.4, it should be further considered that t_{delay_REF} or t_{delay_DIV} approaches zero, or T_{REF} or T_{DIV}, respectively. For ease of understanding, the

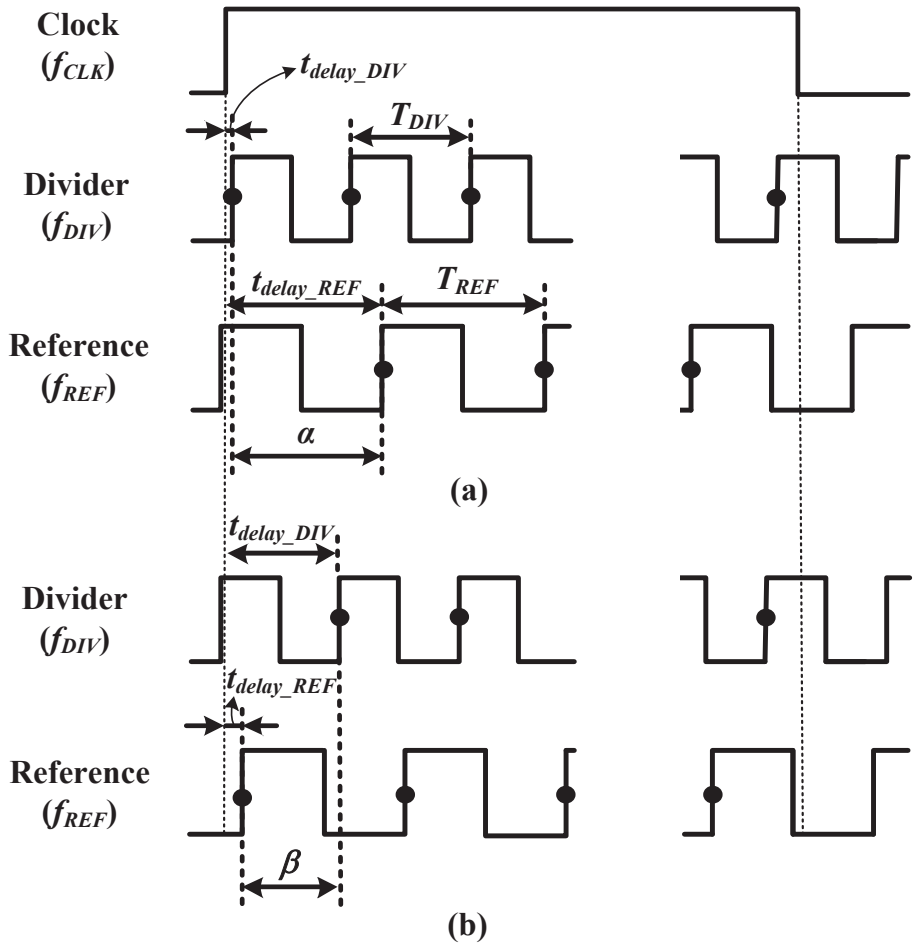


Figure 4.27: Delay differences (a) when $t_{delay\_REF} \geq t_{delay\_DIV}$ and (b) $t_{delay\_REF} \leq t_{delay\_DIV}$.

differences between the two delay times, α and β, are defined as shown in Fig 4.27. Figure 4.27 (a) shows that t_{delay_REF} is equal to or larger than t_{delay_DIV} and Figure 4.27 (b) shows that t_{delay_REF} is equal to or less than t_{delay_DIV}. Thus, α and β are defined respectively as follow:

$$\alpha = t_{delay\_REF} - t_{delay\_DIV} \tag{4.6}$$

$$\beta = t_{delay\_DIV} - t_{delay\_REF} \tag{4.7}$$

Since the periods of the two signal are not the same, their boundary conditions are not the same and have respectively as follow: .

$$0 \leqq \alpha < T_{REF} \tag{4.8}$$

$$0 \leqq \beta < T_{DIV} \tag{4.9}$$

Thus, Eq. 4.4 can be rewritten as follow:

$$T_{REF} + \frac{\alpha}{2^k - 1} > T_{DIV} \text{ where } t_{delay\_REF} \geqq t_{delay\_DIV} \tag{4.10}$$

$$T_{REF} > T_{DIV} + \frac{\beta}{2^k - 1} \text{ where } t_{delay\_REF} \leqq t_{delay\_DIV} \tag{4.11}$$

When there is no difference between the delay times, Eq. 4.10 and 4.11 become the same to Eq.4.5. Meanwhile, when the difference between the delay times becomes lager than zero, the decision boundary begins to deviate from the proper one.

Let's consider that the difference between the delay times reach to the maximums. In this case, t_{delay_REF} and t_{delay_DIV} approach T_{REF} and zero, respectively, when $t_{delay\_REF} \geq t_{delay\_DIV}$. And t_{delay_REF} and t_{delay_DIV} approach zero and T_{DIV}, respectively, when $t_{delay\_REF} \leq t_{delay\_DIV}$. That is, when the difference between the delay times reach to the maximums, α and β become as follow:

$$\alpha \approx T_{REF} \tag{4.12}$$

$$\beta \approx T_{DIV} \tag{4.13}$$

When α approaches T_{REF}, Eq. 4.10 becomes as follow:

$$T_{REF} + \frac{T_{REF}}{2^k - 1} > T_{DIV} \text{ from Eq. 4.10} \tag{4.14}$$

$$(1 + \frac{1}{2^k - 1})T_{REF} > T_{DIV} \tag{4.15}$$

When β approaches T_{DIV}, Eq. 4.11 becomes as follow:

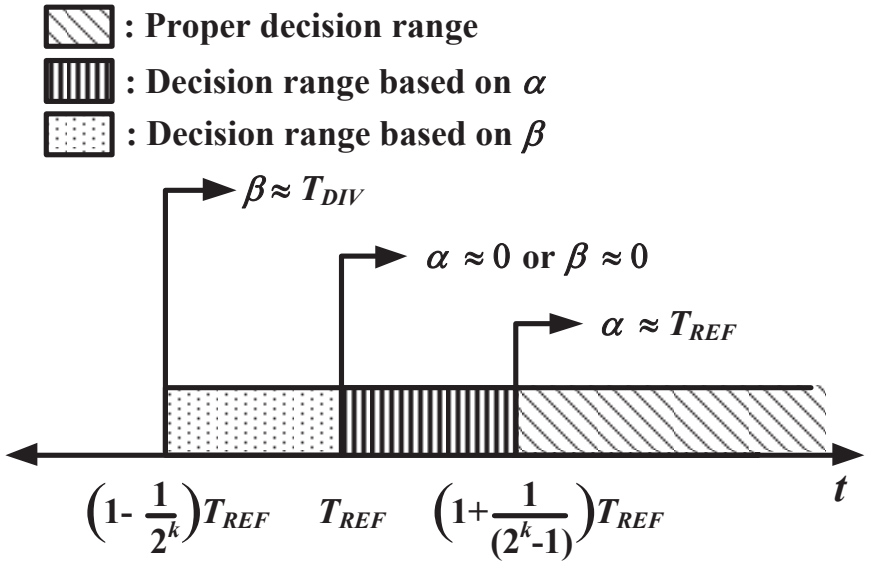


Figure 4.28: Decision range in which the period of the reference is decided to be larger than one of the divider.

$$T_{REF} > T_{DIV} + \frac{T_{DIV}}{2^k - 1} \text{ from Eq. 4.11} \tag{4.16}$$

$$T_{REF} > \frac{2^k}{2^k - 1} T_{DIV} \tag{4.17}$$

$$(1 - \frac{1}{2^k}) T_{REF} > T_{DIV} \tag{4.18}$$

Figure 4.28 shows the decision range in which the period of the reference is decided to be larger than one of the divider. This indicates that the decision of the up/down counter is always correct only if $(1 + \frac{1}{2^k - 1}) T_{REF} > T_{DIV}$. Although the period of the reference is less than the one of the divider, the up/down counter makes a decision that the reference is larger than the one of the divider in the range based on β. In the range based on α, the up/down counter may make a decision that the reference is less than or larger than the one of the divider, depending on the delay differences and the periods of the two input signals.

It is now considered that the up/down counter decides that the period of the reference is less than one of the divider, that is, the k-bit counter for the output

of the divider outputs high first before the k-bit counter for the reference outputs high. If the decision is valid, the following conditions should be satisfied:

$$t_{count\_REF} < t_{count\_DIV} \tag{4.19}$$

$$T_{REF} < T_{DIV} \tag{4.20}$$

And the their delay differences are defined as the same to Eq. 4.6 and 4.7, respectively. Their boundary conditions thus are the same to Eq. 4.8 and 4.9, respectively. When the time delay of the reference is equal to or larger than one of the divider, Eq. 4.19 can be rewritten as follow:

$$T_{REF} + \frac{\alpha}{2^k - 1} < T_{DIV} \text{ where } t_{delay\_REF} \geqq t_{delay\_DIV} \tag{4.21}$$

When α approaches zero, Eq. 4.21 becomes the same to Eq. 4.20. However, when α approaches T_{REF}, then Eq. 4.21 is as following:

$$(1 + \frac{1}{2^k - 1})T_{REF} < T_{DIV} \tag{4.22}$$

This means that the up/down counter makes wrong decision when $T_{REF} < T_{DIV} < (1 + \frac{1}{2^k - 1})T_{REF}$.

When the time delay of the reference is equal or less than one of the divider, Eq. 4.19 can be rewritten as follow:

$$T_{REF} < T_{DIV} + \frac{\beta}{2^k - 1} \text{ where } t_{delay\_REF} \leqq t_{delay\_DIV} \tag{4.23}$$

When β approaches zero, the above equation becomes as follow:

$$T_{REF} < T_{DIV} \text{ where } \beta \text{ approaches zero} \tag{4.24}$$

When β approaches T_{DIV}, Eq.4.23 becomes as follow:

$$T_{REF} < T_{DIV} + \frac{T_{DIV}}{2^k - 1} \tag{4.25}$$

$$T_{REF} < \frac{2^k}{2^k - 1} T_{DIV} \tag{4.26}$$

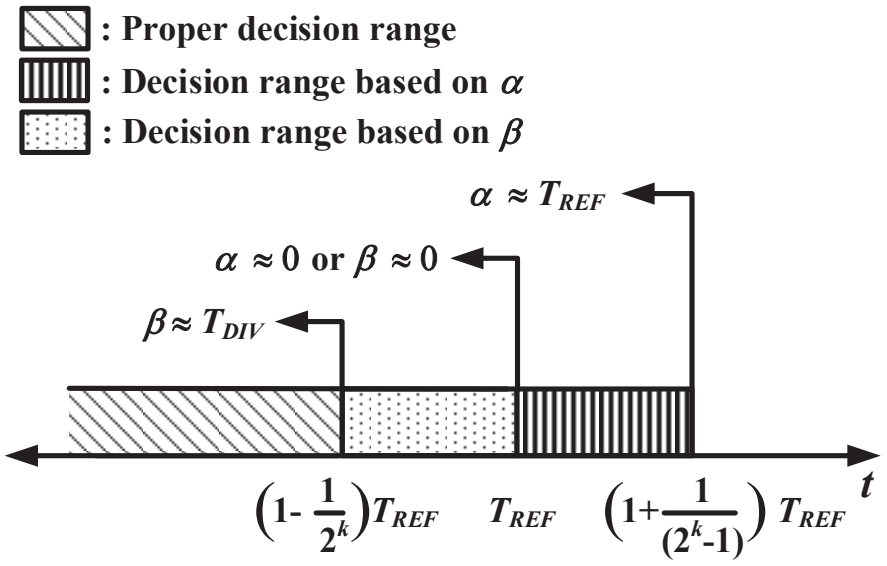


Figure 4.29: Decision range in which the period of the reference is decided to be less than one of the divider.

$$(1 - \frac{1}{2^k})T_{REF} < T_{DIV} \text{ where } \beta \text{ approaches } T_{DIV} \tag{4.27}$$

Figure 4.29 shows the decision range in which the period of the reference is decided to be less than one of the divider by the up/down counter. In this case, the up/down counter may also make wrong or right decisions in the decision range based on β. And the decision of the up/down counter is always correct only if $(1 - \frac{1}{2^k})T_{REF} < T_{DIV}$ without the delay times of its input signals.

In summary, the decision of the up/down counter may be wrong or right based on the delay differences between their inputs in the following range, defined as metastable range:

$$(1 - \frac{1}{2^k})T_{REF} < T_{DIV} < (1 + \frac{1}{2^k - 1})T_{REF} \tag{4.28}$$

This equation can be expressed in terms of the frequency of the reference, by taking its reciprocal.

$$\frac{1}{(1 + \frac{1}{2^k - 1})} f_{REF} < f_{DIV} < \frac{1}{(1 - \frac{1}{2^k})} f_{REF} \tag{4.29}$$

And this can be rewritten in the simplest form as follow:

$$(1 - \frac{1}{2^k}) f_{REF} < f_{DIV} < (1 + \frac{1}{2^k - 1}) f_{REF} \tag{4.30}$$

Multiplying the all sides by N, then it is

$$(1 - \frac{1}{2^k}) N f_{REF} < N f_{DIV} < (1 + \frac{1}{2^k - 1}) N f_{REF} \tag{4.31}$$

Since $N f_{DIV}$ is equal to the frequency of the oscillator, f_{OSC}, Eq. 4.31 can be rewritten as follow:

$$(1 - \frac{1}{2^k}) N f_{REF} < f_{OSC} < (1 + \frac{1}{2^k - 1}) N f_{REF} \tag{4.32}$$

This is the metastable range of the lock controller based on the k-bit counters and the up/down counter.

Table 4.1: Metastable range based on the number, k, of bits of the counters.

k (bits)	Lower limit (GHz)	Upper limit (GHz)	Metastable range (MHz)
1	0.5000	2.0000	1500.0
2	0.7500	1.3334	583.4
3	0.8750	1.1429	267.9
4	0.9375	1.0667	129.2
5	0.9687	1.0323	63.6
6	0.9843	1.0159	31.6
7	0.9921	1.0079	15.8
8	0.9660	1.0040	8.0
9	0.9980	1.0020	4.0
10	0.9990	1.0010	2.0
11	0.9995	1.0005	1.0
12	0.9997	1.0003	0.6

When the detection frequency of the oscillator is 1GHz and the reference has the frequency of 50MHz, the both limits of metastable range are shown in Table. 4.1. Thus, 7-bit counters and 10-bit counters are used for coarse tuning and fine tuning lock control, respectively.

In summary, the lock controller is composed of two 7/10-bit counters, a 5-bit up/down counter and detector, a D flip-flop, an initial voltage, and an internal

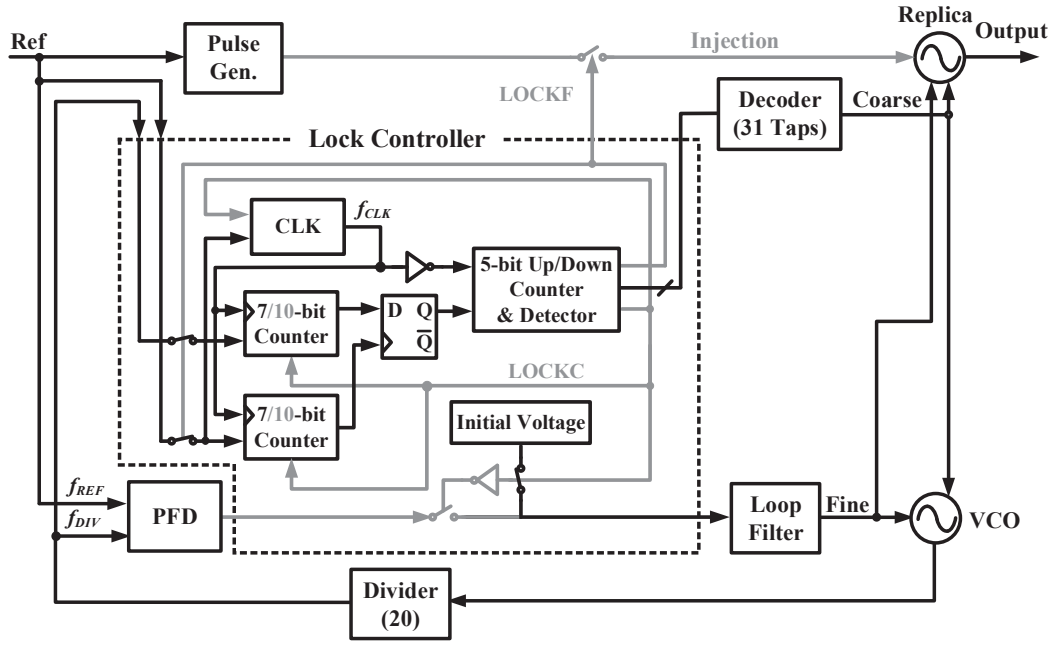


Figure 4.30: Operation of the proposed injection-locked CPPLL for coarse tuning.

clock generator (CLK). The 5-bit up/down counter and detector outputs three kinds of signals; 5-bit code for coarse tuning of the VCO, LOCKC indicating that coarse tuning is locked, and LOCKF indicating that fine tuning is locked. The CLK block outputs a clock signal for counters by dividing the Ref by 2^9 during the coarse tuning or 2^{12} during the fine tuning. The detail operation of the lock controller will be described in the next subsection.

4.3.2 Configuration and Operation of the Proposed Injection-Locked CPPLL

The operation of the proposed injection-locked CPPLL has basically three stages which are coarse tuning stage, fine tuning stage, and normal operation stage. At first, the proposed injection-locked CPPLL tries to lock the coarse tuning at the coarse tuning stage. As soon as the coarse tuning is locked, the fine tuning stage starts to determine whether the oscillator operates at the desired frequency. After the fine tuning is locked, the injection signal is inputted to

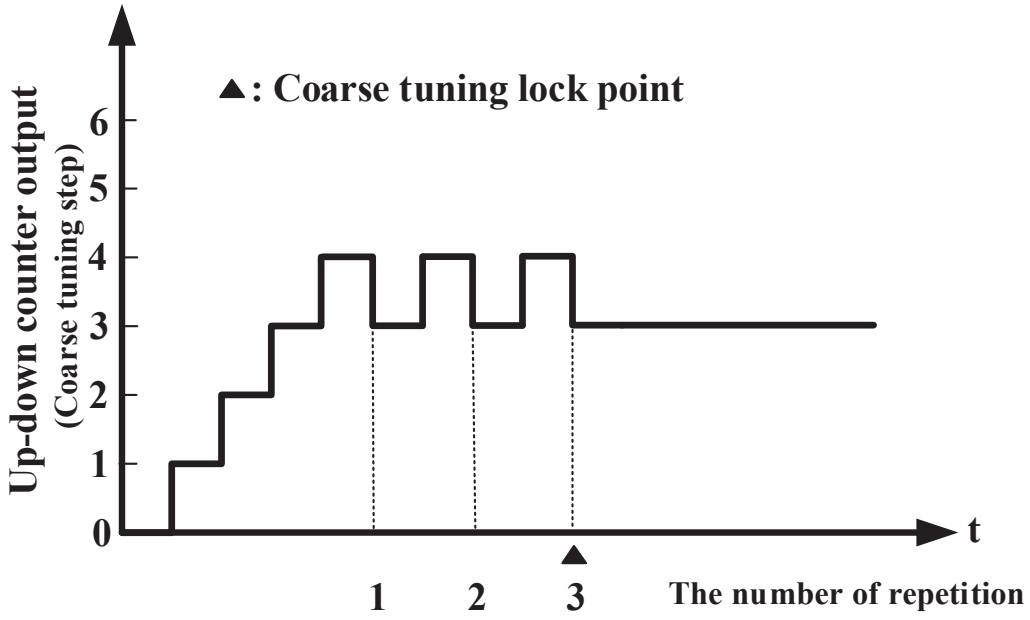


Figure 4.31: The output of the up-down counter for coarse tuning.

the injection-locked oscillator and then the proposed injection-locked CPPLL operates at normal operation stage.

Figure 4.30 shows the operation of the proposed injection-locked CPPLL for coarse tuning. The black lines and the gray lines show active devices and inactive devices, respectively. At the coarse tuning, the lock controller fixes the fine tuning voltage at a specified value and compares between frequencies of the reference clock and the divider. For coarse tuning, 7/10-bit counters operate as 7-bit counters. As shown in Fig. 4.13, the lowest step of the coarse tuning code is closer to the target frequency than the highest step of the coarse tuning code. Thus, the initial value of the decoder is set to the lowest step. When the frequency of the divider comes up to the frequency of the reference, the 5-bit up/down counter repeats up and down and the decoder also outputs repeatedly two adjacent codes at which the oscillator has the frequency most close to the target frequency, as shown in Fig. 4.31. Note that the output of the up-down counter is a binary code but is described with corresponding coarse tuning step, that is, a decimal number, in Fig. 4.31. Then the detector detects the repeat of up and down of

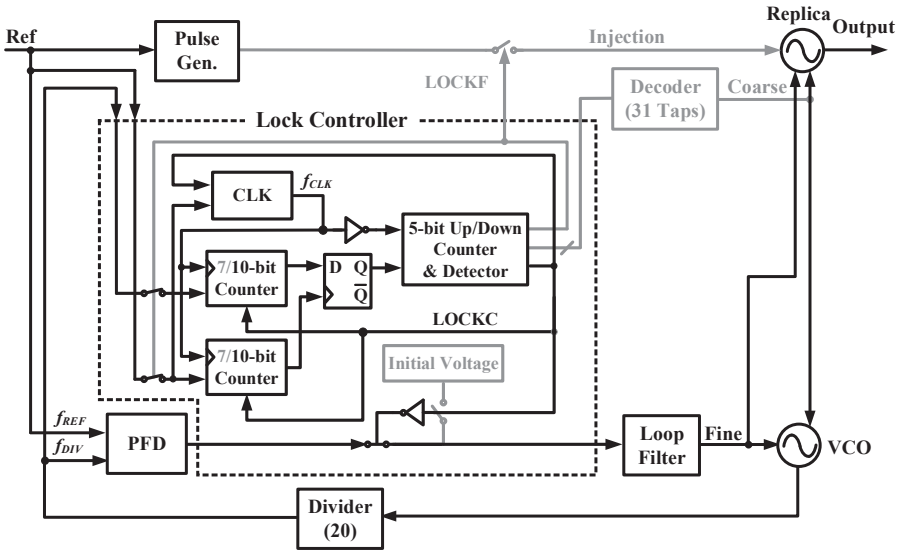


Figure 4.32: Operation of the proposed injection-locked CPPLL for fine tuning.

the 5-bit up/down counter, that is, it counts up when the current output of the 5-bit up/down counter is low and the previous one is high. When the repetition of up and down reaches to the predetermined number, the detector outputs an alarm of LOCKC, which indicates the lock of coarse tuning. For obtaining stable lock, the number of repetition is set to 3 times. Then the coarse tuning finishes and the fine tuning stage begins.

When LOCKC is alarmed, the proposed injection-locked CPPLL proceeds to the operation of for fine tuning as shown in Fig. 4.32. The decoder is locked and the loop filter is connected to PD/CP output. And the 7/10-bit counters are switched to 10-bit counters for fine tuning by LOCKC. As described in Section 4.3.1, this configuration provides a frequency error below ±1 MHz in which the injection-locked oscillator can be locked. When the frequency of the oscillator is less than the difference of ± 1 MHz compared to the target frequency, the 5-bit up/down counter repeats between up and down with similarly to the coarse tuning. When the repetition continues a several times, the detector alarms LOCKF. The fine tuning stage comes to close.

Figure 4.33 shows the normal operation of the proposed injection-locked CPPLL. When LOCKF is alarmed, the injection signal is inputted to a replica of

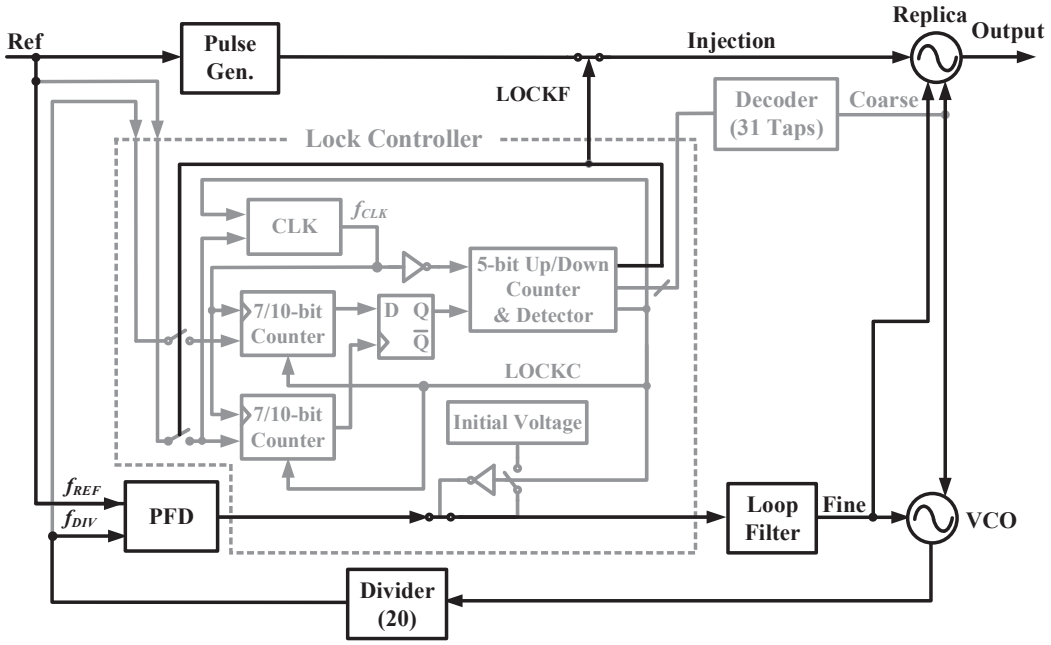


Figure 4.33: Normal operation of the proposed injection-locked CPPLL.

the oscillator. The proposed injection-locked CPPLL proceeds to normal operation. Though the coarse tuning code is locked for the normal operation, the proposed injection-locked CPPLL can provide the tolerance to temperature and supply voltages since the fine tuning range is enough wide as shown in Fig. 4.13. When the coarse tuning is locked in the 4th code, the coarse tuning lock time is $92.2\mu s$. For fine tuning, about $251.8\mu s$ is required. Thus, the total lock time is about $344\mu s$.

This can provide stable lock-state maintenance and tolerance to temperature and supply voltage variation if effect on the loop of the CPPLL by injection is so weak that the loop stability can maintain. The effect on the loop by injection is through the output of the loop filter because two oscillators share it. When a pulse signal is injected to the replica of the oscillator and the replica is locked by the injection pulse, its frequency is pulled from free running frequency, f_{OSC}, to N times of injection frequency, f_{inj}. In the case of the difference of Δf in the oscillation frequency of the oscillator, output of the loop filter is affected by substantially less than $\Delta f / k_{vco} V$. Δf in the injection-locked oscillator is

desirably less than $f_{inj}/4$ which is so small to hardly affect the loop stability. Periodic injection is also filtered out by the loop of the PLL because the injection frequency is out of the loop bandwidth. Thus, the proposed injection-locked CPPLL can avoid the phase confliction and be tolerable to voltage-temperature (VT) variations to maintain the stability.

4.4 Performance Comparison

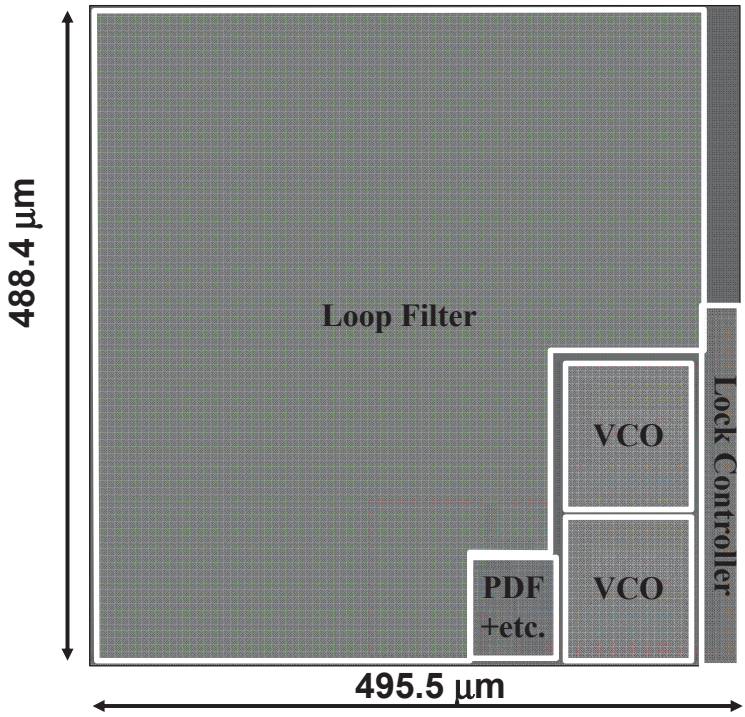


Figure 4.34: Layout of the proposed injection-locked CPPLL.

Figure 4.34 shows the layout of the proposed PLL. The proposed PLL is fabricated in a 90nm CMOS process and occupies an area of $495.5 \times 488.4 \mu m^2$. It is also packaged in a chip due to chip-sharing and measurement environment. Thus, the outputs for the measurement are divided by 8 to avoid noise at high frequency due to wires bonding and so on. The measurement was performed on the supply voltage of 1.2V.

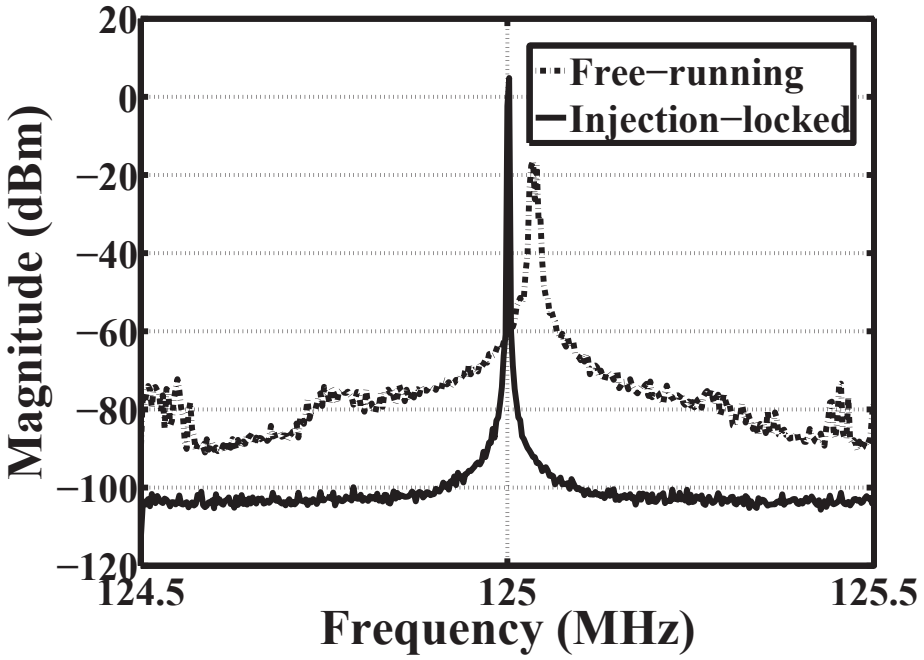


Figure 4.35: Measured spectra of the free-running and injection-locked oscillators with (a) resolution bandwidth of 1kHz (b) resolution bandwidth of 10Hz.

Figure 4.35 shows the measured spectra of the free-running and injection-locked oscillators and Figure 4.36 show measured phase noises. All data except the reference were converted to the phase noise seen at 1GHz, that is, the data are added by 20·log(8). While in-band noises of the free-running oscillator at 10kHz and 100kHz are −43.5dBc/Hz and −79.0dBc/Hz, respectively, in-band noises of the injection-locked oscillator are −108.2dBc/Hz and −114.6dBc/Hz. The power consumption was 2.8mW. In the case that the supply voltage changed around 1.2V since the injection-locked oscillator is locked, we confirmed that the oscillator maintained stable locked state from 1.13V∼1.26V. This tolerance to supply voltage corresponds to tolerance to temperature of 96.4°C from Eq. 4.1.

A comparison with other PLLs is demonstrated in Table 4.2. The proposed injection-locked CPPLL shows high injection ratio, wide tolerance to supply voltage variation, and low in-band phase noise. Compared with other injection-locked PLLs [31] [104], the proposed PLL consumes more area but can guarantee stable lock state under PVT variations. Especially, the tolerance of the supply volt-

Table 4.2: Performance comparison.

	This work	[31]	[104]	[73]	[78]	[76]	[93]	[75]
Output Frequency	1GHz	2GHz	1.2GHz	1GHz	1GHz	0.93GHz	3.1GHz	1GHz
N	20	25	4	32	37.156	–	–	–
Inband Phase Noise (dBc/Hz) at 10kHz offset	−108.2	–	−102 ∼ −105	−90	−85	−109	−87	−80
Inband Phase Noise (dBc/Hz) at 100Hz offset	−114.4	−103	−100	−106	N.A.	−111	−101	−95
Supply Voltage (V)	1.2	1.2	1.0	1.2	N.A.	1.8	1.2	N.A.
Tolerance Range (V) to Supply Voltage Variation	1.13 ∼ 1.26	–	–	–	–	–	–	–
Core Power (mW)	2.8	22	0.97	16.8	6.1	36	27.5	2.2
Core Area (mm^2)	0.242	0.083	0.022	0.31	0.5	0.8	0.336	0.026
VCO Type	Ring	Ring	Ring	Ring	Ring	LC	Ring	Ring
PLL Type	Injection	Injection	Injection	ΣΔ frac.N	ΣΔ frac.N	frac. N	Digital	Digital
Technology (CMOS)	90nm	90nm	65nm	130 nm	180nm	180nm	65nm	28nm

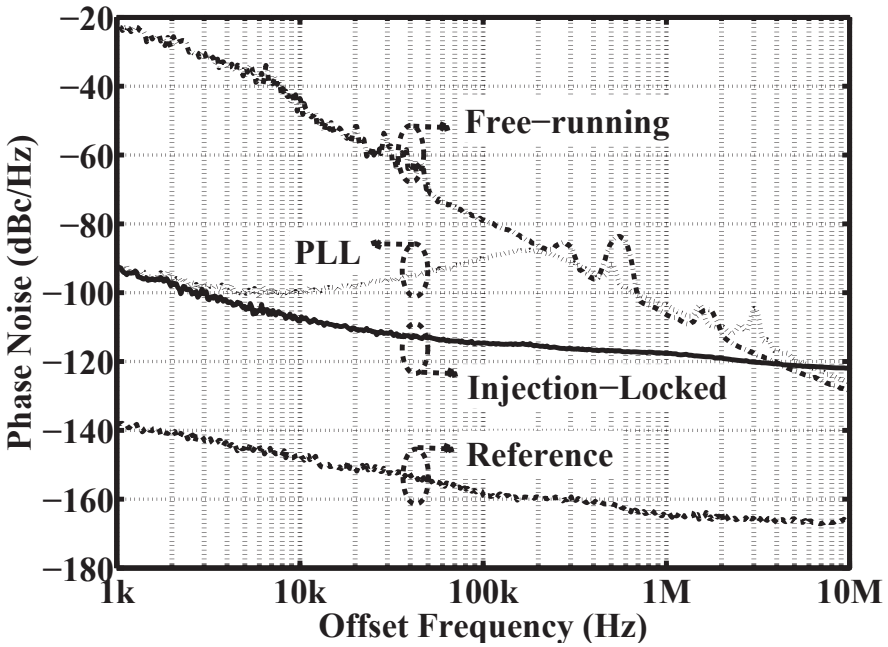


Figure 4.36: Measurement phase noises (note that all data except the reference was converted to the phase noise seen at 1GHz).

age is very important for the injection-locked PLLs since they are vulnerable to the supply voltage variation. The conventional fractional and $\Sigma\Delta$ fractional-N PLLs consume large power to obtain low phase noise [73] [78]. The fractional N PLL with a LC oscillator uses an output divider to obtain lower output frequencies than the output of the oscillator [76]. It reduces the chip area avoiding large inductor but results in the increase of the power consumption. Digital PLLs has relatively small area compared to LC-based PLLs [93] and can be also implemented with very small area [75]. However, Digital PLL with very small area can hardly obtain good phase noise characteristics [75]. Consequently, the proposed injection-locked CPPLL has reasonable chip area, power consumption, good phase noise characteristics, and also wide tolerance to very high stability for PVT variations.

4.5 Summary

This chapter presented an injection-locked charge-pump phase-locked loop with a replica of a ring oscillator. Its simulation and measurement results show the proposed injection-locked CPPLL is widely tolerable to PVT variations.

The proposed injection-locked CPPLL has the high injection ratio of 20 and is tolerable to $-5.8\% \sim 5.0\%$ variation of the supply voltage, which corresponds to tolerance to temperature of 96.4°C. In-band noises of the injection-locked oscillator at offset frequencies of 10kHz and 100kHz are -108.2dBc/Hz and -114.6dBc/Hz, respectively. The chip area occupies 0.242mm^2. The power consumption is 2.8mW.

Chapter 5

Enhancement of Tolerance to Voltage-Temperature Variation

This chapter discusses two issues, detection of the meta-stable range in the lock controller and enhancement of tolerance to voltage and temperature variations. The lock controller including a frequency comparator was presented in the previous chapter. The frequency comparator based on the two D flip-flops has a simple configuration and stable performance. However, it has a meta-stable range which can not provide a proper decision as described in Section 4.3.1. Since the meta-stable range is inversely proportional to the bit number of the counters, the narrow meta-stable range for the precise decision leads to the increases of not only the bit number but also the lock time. From a different view, if the meta-stable range can be detected, the lock controller may more efficiently control the ILPLL and the number of bits of the counter can be reduced.

Another issue in the proposed injection-locked CPPLL is that the ring oscillator with multiple current sources has narrower fine tuning range than the ring oscillators with single current source. As previously mentioned in Chapter 4 about the trade-off between ring oscillators with single current source and with multiple current sources, the relatively narrow fine tuning range is an alternative to reduce the area of the loop filter but reduces the tolerance to voltage and temperature variations. Thus, this chapter introduces a method to enhance fine tuning range paying relatively small area and low current consumption.

5.1 Meta-Stable Detection

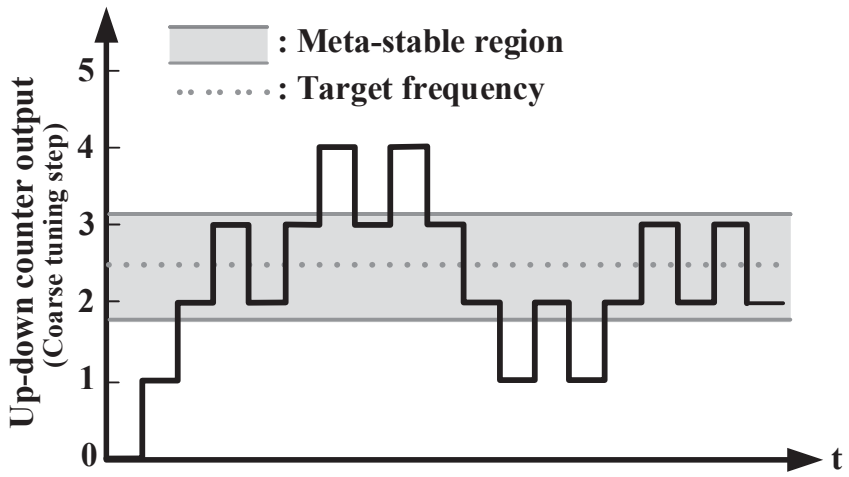


Figure 5.1: Wide meta-stable region.

The meta-stable range already described in Chapter 4.3.1 is a systematic limit of the lock controller which makes a comparison between frequencies of two signals with a simple frequency comparator. It is possible to reduce this systematic limit, that is, the meta-stable range, by increasing the number of bits in the counters. Although it increases the lock time, the narrower meta-stable range can provide better decision accuracy in frequency comparison, which is conducted for coarse tuning and fine tuning in the proposed ILPLL. However, the narrow meta-stable range may make the coarse tuning locked at acceptable but non-optimal coarse tuning step. Before discussing how to lock the coarse tuning at the optimal step, it needs to examine the effects relating to the size of the meta-stable range in detail.

Figure 5.1 shows possible lock codes of the lock controller with wide meta-stable region. Since the meta-stable region is wider than the coverage of the one coarse tuning step, possible lock codes of the coarse tuning would be from 1 to 3. Thus, the narrow meta-stable region is preferred to be able to compare the two frequencies at the high resolution. However, there is a question whether the large numbers of bits provide always benefit to detect the proper code.

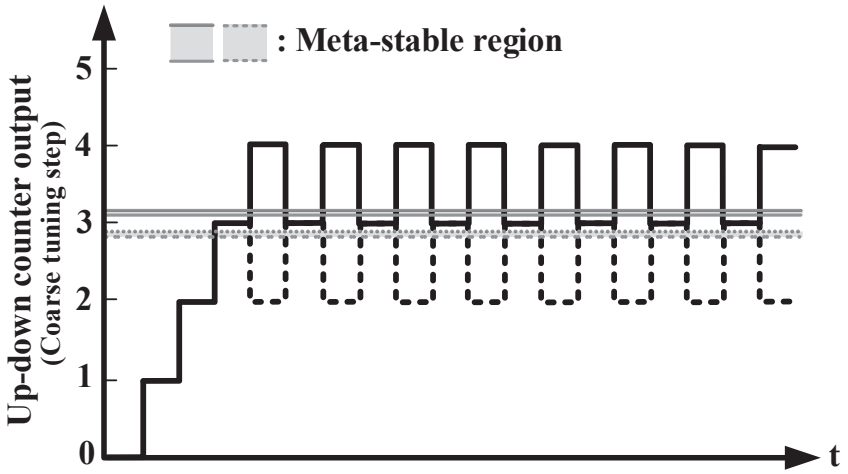


Figure 5.2: Narrow meta-stable region.

Figure 5.2 shows possible lock codes of the lock controller with very narrow meta-stable region. Assume that the target oscillation frequency is a little bit higher -indicated with the solid line - or lower - indicated with the dotted line - than the 3rd coarse tuning step. In this case, it is desired to lock at the 3rd coarse tuning step. As previously mentioned in Section 4.3.2, the coarse tuning is locked when consecutive up and down is repeated 3 times. Thus, when the target oscillation frequency is a little bit higher than 3rd coarse tuning step, the coarse tuning is locked at the 3rd coarse tuning step. however, when the target oscillation frequency is a little bit lower than 3rd coarse tuning step, the coarse tuning is locked at the 2nd coarse tuning step, which is acceptable but non-optimal. In this case, frequency coverage almost by one step of the coarse tuning should be recovered by the fine tuning, such that it results in reducing tolerance of the fine tuning to voltage-temperature variations.

When the meta-stable region is proper, the lock controller will normally lock the coarse tuning at the optimal step, as shown in Fig. 4.31. In Fig. 4.31, there is the meta-stable range between the 3rd and 4th coarse tuning steps. However, it would happen that the meta-stable range would include the 3rd coarse tuning step due to process variation, as shown in Fig. 5.3. In this case, the coarse tuning code moves among the 2nd, 3rd, and 4th. The coarse tuning would be locked

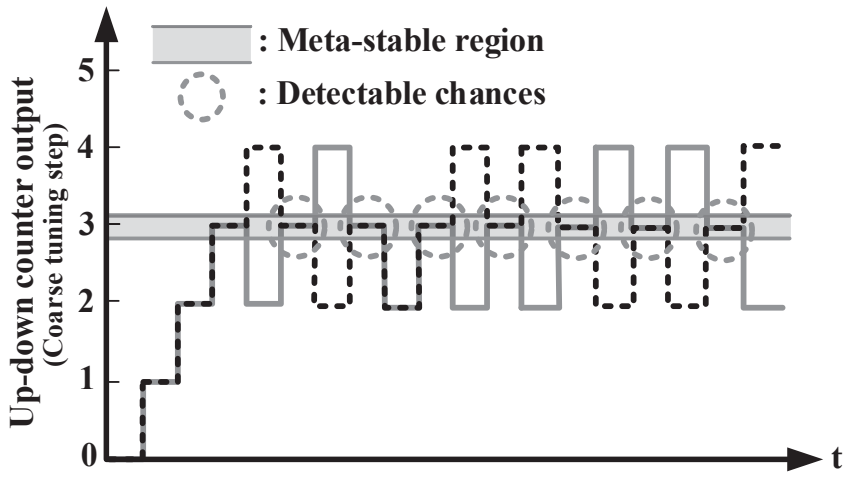


Figure 5.3: Medium meta-stable region.

at one of the 2nd or 3rd coarse tuning step. As described above, the 2nd coarse tuning step is acceptable but non-optimal. Although the proper meta-stable range may sometimes cause the lock at the non-optimal coarse tuning step, the proper meta-stable range would still be the best option among them since the wide meta-stable range may also cause the similar problem and furthermore leads to more long lock time.

If the coarse tuning step within the meta-stable range can be detected, the coarse tuning can be locked at the optimal step even when the meta-stable range includes the target frequency. That is, when the lock controller has the comparison function between them and detects the middle code in Fig. 5.3, the most desired coarse tuning range can be selected. This comparison function can be easily implemented by VHDL or Verilog-HDL. Dotted circles in Fig. 5.3 show chances to detect a coarse tuning step within the meta-stable range, called detectable chances. Three coarse tuning steps including the step within the meta-stable range are required for the meta-stable detection. Thus, the first detectable chance is given when the lock comparator compares frequencies since the up-down counter counts down in first. In other words, the detectable chances are provided in every meta-stable range except the first. And probability of the meta-stable detection is 50% in a chance. Assume that the oscillation frequency is within

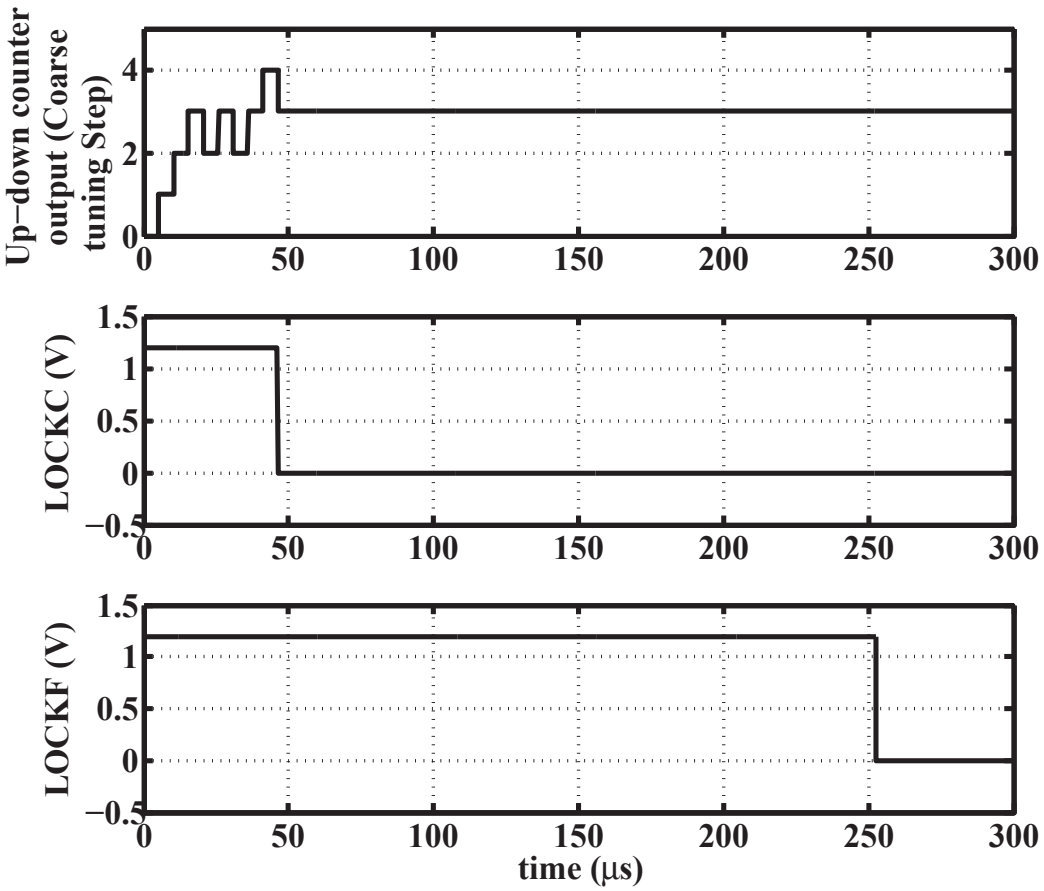


Figure 5.4: Simulation results of the meta-stable detection.

the meta-stable range and D is defined as the number of the detectable chances. And $P(D)$ is defined as the probability to detect a coarse tuning step within the meta-stable range. Then, the probability to detect a coarse tuning step within the meta-stable range is as follow:

$$P(D) = 1 - \frac{1}{2^D} \tag{5.1}$$

When D is 5, the lock controller can detect the meta-stable region with the probability of 96.9%.

Fig. 5.4 shows the simulation results of the meta-stable detection. The output of the up-down counter indicates that the coarse tuning of the oscillator is set to

the 4-th coarse tuning step - corresponding to 3 coarse tuning step -, which is included in the meta-stable range. LOCKC is a lock alarm indicating that the coarse tuning is locked and LOCKF is a lock alarm indicating that the fine tuning is locked, as shown in Fig. 4.30 and 4.32. In the previous chapter, the counters for coarse tuning were 7 bit, which results in the meta-stable range of 15.8MHz as shown in Table 4.1. Using the detection of the meta-stable range, the 6 bit counters with the meta-stable range of 31.6MHz is enough to detect the optimal coarse tuning step. Thus, the 6 bit counters are used for the coarse tuning in the simulation. Simulation results show that the coarse tuning is locked at the optimal coarse tuning step and fine tuning is also locked without any problem. Thus, the fine tuning current can have better potential tolerance to the voltage and temperature variations.

5.2 Enhancement of Fine Tuning Range

In the chapter 4, the injection-locked ring oscillator is controlled by 3 kinds of the current sources, such that the oscillator gain is reduced and the chip area of the loop filter can be reduced. However, after the coarse tuning in the PLL is locked, the frequency coverage of the PLL over the power supply voltage and temperature variations almost depends on the coverage of the fine tuning range. For large frequency coverage, the large fine tuning range is required. If the channel width of the fine tuning current source is increased to extend the coverage, it will lead to larger oscillator gain and then require the larger chip area of the loop filter in order to maintain the same loop bandwidth.

An alternative method is to control the coarse tuning current sources again in order to compensate the power supply voltage and temperature variations after the PLL is locked. However, it will cause that the PLL should suffer the lock procedure for the coarse and fine tuning again. Furthermore, the system needs to pause till the PLL is locked.

This section introduces a proposed method to enhance the tuning range of the oscillator in the PLLs without the re-lock procedure and the pause of the system.

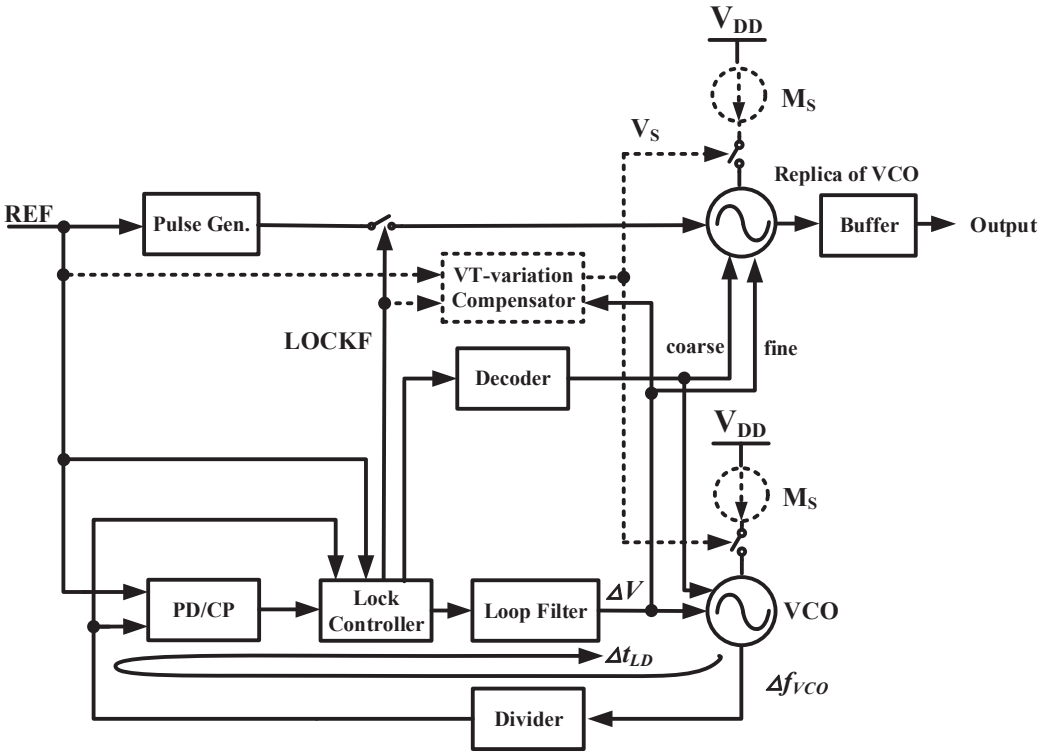


Figure 5.5: Injection-locked PLL with a VT variation compensator.

5.2.1 Basic Concept of Enhancement of Fine Tuning Range

The basic concept of extension of the tolerance to the VT variations is to turn on or off a supplementary current source without interruption of the lock state in the PLL. For ease of understanding, this thesis describes the case that the supplementary current source is turned on. The same method can be easily applied to the case that the supplementary current source is turned off.

Figure 5.5 shows an injection-locked PLL with a supplementary current source, M_S, and a VT variation compensator. When the supply voltage decreases or temperature increases, the oscillation frequency of the VCO decreases. When the oscillation frequency changes by Δf_{VCO}, the PLL changes a control voltage by ΔV to compensate the deviation of the frequency after the loop delay time, Δt_{LD}. Meanwhile, when the gate voltage of the fine tuning current source has already reached to the acceptable limit voltage and cannot accept the additive control

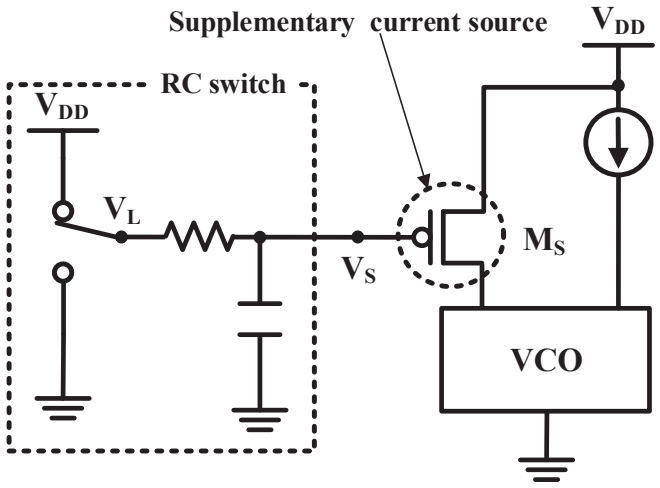


Figure 5.6: Basic concept to turn on or off a current source slowly.

voltage ΔV, the PLL and the injection-locked oscillator will lose lock. In such a case, if a compensator detects it and turns on or off a supplementary current source slowly enough in order not to interrupt the lock state in the PLL, the PLL and the injection-locked oscillator can maintain the stable lock state. The question is how to turn on or off a supplementary current source slowly enough in order not to interrupt the lock state in the PLL. This can be solved by a simple low pass filter, called a RC switch.

Figure 5.6 shows a basic concept to turn on or off the supplementary current source slowly. As described above, the general turn-on of a coarse tuning current source causes the frequency of the oscillator to change very sharply. This leads to an unstable condition of the whole ILPLL. Meanwhile, if the supplementary current source is turned on through a RC lowpass filter, its gate voltage, V_S, is slowly changed like the transient response of the RC circuit. And then the oscillator changes its frequency slowly. The next subsection discusses about how large R and C are required to maintain the stable lock state and how large frequency is changed in the oscillator by the RC switch and the supplementary current source.

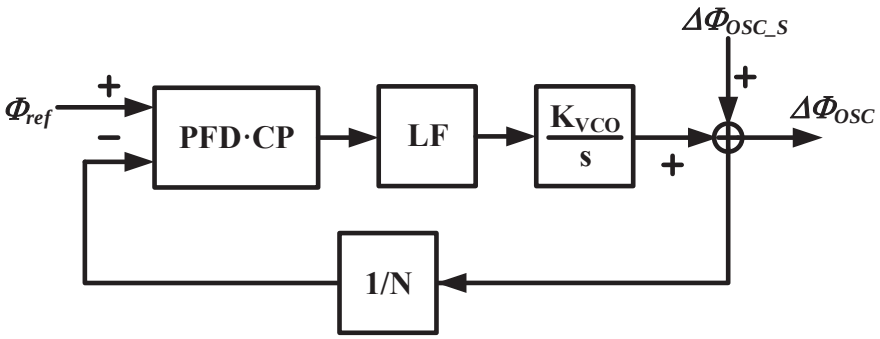


Figure 5.7: Liner noise model of the PLL with the noise in the oscillator.

5.2.2 Analysis of Tolerance Enhancement

The linear noise model of the PLL as shown in Fig. 5.7 is used to examine how large frequency is changed in the oscillator by the RC switch and the supplementary current source. That is, the frequency variation, Δf_{OSC_S}, in the oscillator alone due to the supplementary current source is considered to be a noise in the oscillator. And the frequency variation, Δf_{OSC}, of the oscillator in the ILPLL can be obtained through its noise transfer function. Since the noise model is the phase noise model, Δf_{OSC_S} and Δf_{OSC} are corresponded to $\Delta\Phi_{OSC\_S}$ and $\Delta\Phi_{OSC}$ in terms of phase, respectively.

First of all, the phase variation, $\Delta\Phi_{OSC_S}$, caused by the supplementary current source is to be obtained. When the supply voltage decreases and it is detected that the gate voltage of the fine tuning current source is out of the predetermined voltage, V_L is switched from V_{DD} to ground and $\mathrm{M_S}$ is slowly turned on by its gate voltage, V_S, which is the output of the RC switch. V_S changes with the time constant, τ, of the RC switch and can be expressed as follow:

$$V_S(t) = \mathrm{V_{DD}} \cdot e^{-t/\tau} \tag{5.2}$$

where $\mathrm{V_{DD}}$ is the supply voltage. When $\mathrm{M_S}$ is turned on, the frequency of the oscillator is increased by the $\Delta f_{OSC\_S}(t)$. Note that the frequency of the oscillator is a time dependent variable since its control voltage, V_S, is a time dependent variable. When the oscillation gain, K_{VCO_S}, of $\mathrm{M_S}$ is modeled to have

a positive value, the frequency variation in the oscillator, $\Delta f_{OSC\_S}(t)$, caused by M_S is

$$\Delta f_{OSC\_S}(t) = K_{VCO\_S} \cdot (V_{DD} - V_S(t)) \tag{5.3}$$

In Eq. 5.3, the oscillator gain, K_{VCO_S}, is constant. However, In many cases, the oscillator gain is assumed as a constant in the narrow range but is substantially dependent on the control voltage, that is, the gate voltage of the current source, as shown in Fig. 4.11. Thus, K_{VCO_S} also depends on the gate voltage, V_S. It is reminded that V_S is time dependent. And then, K_{VCO_S} is a time dependent variable, too. Consequently, $K_{VCO\_S}(t)$ should be defined as follow:

$$K_{VCO\_S}(t) = K_{VCO\_S\prime} \cdot (V_{DD} - V_S(t)) \tag{5.4}$$

where $K_{VCO\_S\prime}$ is a constant. Then, the incremented oscillation frequency, Δf_{OSC_S}, by M_S, is

$$\Delta f_{OSC\_S}(t) = K_{VCO\_S\prime} V_{DD}^2 (1 - e^{-t/\tau})^2 \tag{5.5}$$

This is a quite rough approximation since the oscillator gain, $K_{VCO\_S\prime}$, is assumed as a constant in Eq. 5.4 even though the control voltage, $V_S(t)$, is widely changed from V_{DD} to ground. However, this is useful to find the maximum frequency variation in the ILPLL caused by the supplementary current source and to verify the stability of the ILPLL, if and only if $K_{VCO\_S\prime} V_{DD}^2$ is defined as the maximum incremented frequency, $\Delta f_{OSC\_S\_MAX}$, caused by the supplementary current source, M_S. Thus, the incremented oscillation frequency is defined again as follow:

$$\Delta f_{OSC\_S}(t) \approx \Delta f_{OSC\_S\_MAX} (1 - e^{-t/\tau})^2 \tag{5.6}$$

where $\Delta f_{OSC\_S\_MAX}$ is the maximum incremented frequency caused by the supplementary current source, M_S. This is expressed in terms of the frequency and should be converted to a phase variation in order to be applied to the noise transfer function. Equation 5.6 can be rewritten as follow:

$$\Delta\Phi_{OSC\_S}(t) \approx \Delta\Phi_{OSC\_S\_MAX}(1 - e^{-t/\tau})^2 \tag{5.7}$$

where $\Delta\Phi_{OSC\_S\_MAX}$ is the maximum phase variation with respect to the phase of the oscillation frequency.

As described in Sec. 2.3.5, the transfer function of the noise source from the oscillator, N_{osc}, is

$$N_{osc} = \frac{1}{1 + G(s)} \tag{5.8}$$

where $G(s)$ is the open-loop transfer function. Since the frequency variation, Δf_{OSC_S}, in the oscillator alone due to the supplementary current source is considered to be a noise source in the oscillator, this equation can be expressed as follow:

$$N_{osc} = \frac{\Delta\Phi_{OSC}(s)}{\Delta\Phi_{OSC\_S}(s)} \tag{5.9}$$

It is reminded again that $\Delta\Phi_{OSC}$ and $\Delta\Phi_{OSC\_S}(s)$ are phase expressions of Δf_{OSC} and Δf_{OSC_S}, respectively. And the open loop transfer function, G(s), becomes as follow:

$$G(s) = \frac{K_{PDF\cdot CP} K_{VCO} LF(s)}{N \cdot s} \tag{5.10}$$

where $K_{PDF\cdot CP}$ is the combine gain of the phase-frequency detector and the charge pump, K_{VCO} is the oscillator gain, N is the division ratio, and $LF(s)$ is the transfer function of the loop filter. The 3rd-order loop filter, $LF(s)$, in the PLL as shown in Fig. 2.28 is modeled as follow:

$$LF(s) = \frac{1}{s(C_1 + C_2 + C_3)} \left(\frac{sC_2R_2 + 1}{s^2 \frac{C_1C_2C_3R_2R_3}{C_1+C_2+C_3} + s\frac{(C_1+C_3)C_2R_2+(C_1+C_2)C_3R_3}{C_1+C_2+C_3} + 1} \right) \tag{5.11}$$

When $C_2 >> C_1, C_3$ and $R_2 > R_3$, the equation 5.11 can be approximated as follow:

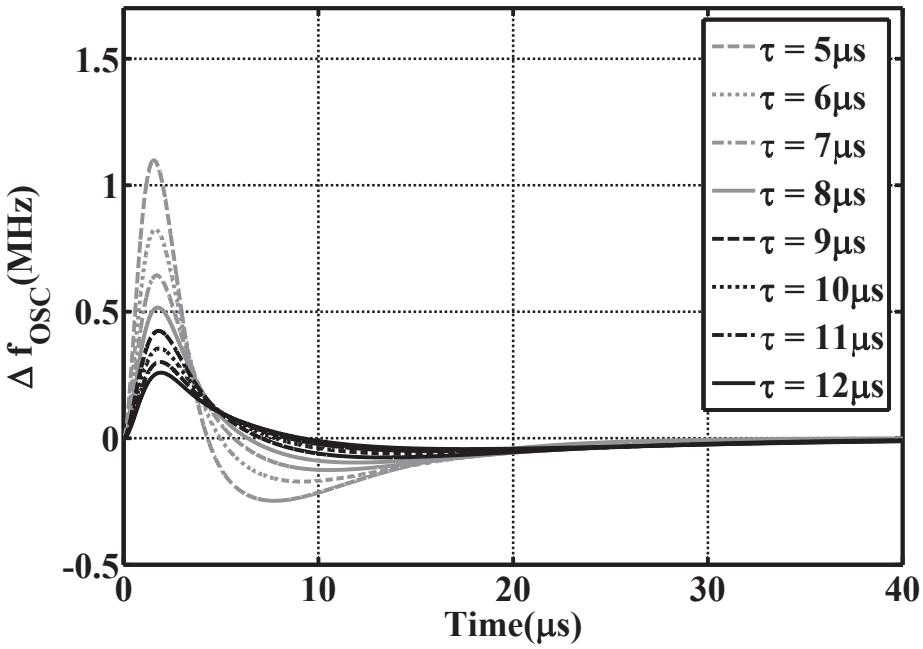


Figure 5.8: Calculation results of Δf_{OSC}.

$$LF(s) \approx \frac{1}{s(C_1+C_2+C_3)}\left(\frac{sC_2R_2+1}{s^2C_1C_3R_2R_3+s(C_1+C_3)R_2+1}\right) \tag{5.12}$$

From Eq. 5.8, 5.9, and 5.10, and 5.12, the phase variation in the oscillator, $\Delta\Phi_{OSC}$, can be obtained as follows:

$$\Delta\Phi_{OSC}(s) \approx \frac{s^2k_1+sk_0}{s^2k_1+s(k_0+K\cdot k_2)+K}\Delta\Phi_{OSC\_S}(s) \tag{5.13}$$

where K is $I_{CP}K_{VCO}/N$, I_{CP} is the current of the charge pump, K_{VCO} is the oscillator gain, N is the division ratio, k_0 is $(C_1+C_2+C_3)$, k_1 is $(C_1+C_2+C_3)(C_1+C_3)R_2$, and k_2 is C_2R_2.

Figure 5.8 shows calculation result of Δf_{OSC} when the oscillation frequency is 1GHz. The calculation results show that the maximum deviation of the output frequency can be suppressed below the loop bandwidth of the ILPLL, 470kHz, when the RC time constant is above 8.5 μs.

5.2.3 Circuit Configuration and Operation

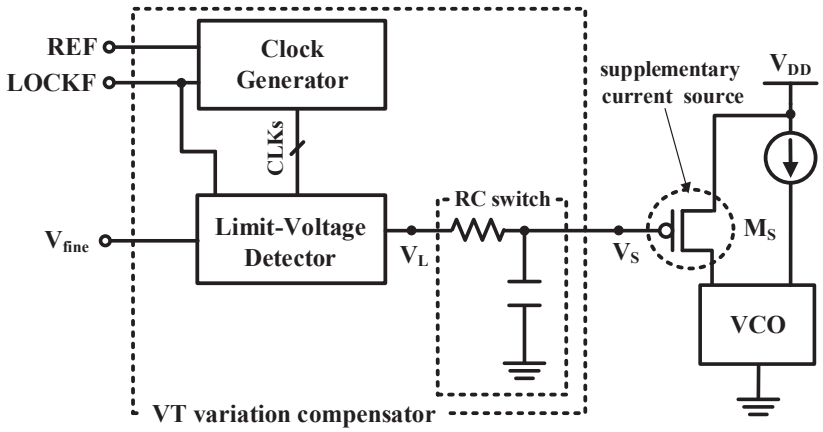


Figure 5.9: Block diagram of a VT variation compensator.

The block diagram of a VT variation compensator is shown in Fig. 5.9. The VT variation compensator is composed of three components, a limit-voltage detector which detects that the fine tuning voltage is out of the predetermined range, a clock generator whose output clocks are used to control the limit-voltage detector, and a RC switch which turns on or off the supplementary current source enough slowly in order not to disturb the lock state. That is, its main function is to detect that the fine tuning voltage is out of the predetermined range and to turn on a supplementary current source without interruption of the lock state in the PLL. Each block of the VT variation compensator is described in detail.

Figure 5.10 shows a circuit diagram of the RC switch and a modified delay stage of the ring oscillator in Chapter 4. In Fig. 5.10 (b), a supplementary current source, M_S, is to compensate a drop of the oscillation frequency due to the power supply voltage and temperature variations. Thus, initial state of the current source, V_S, is the supply voltage since it is a PMOS current source. When the fine tuning voltage is out of the predetermined range and the oscillator cannot increase the oscillation frequency, the supplementary current source is turned on. In order to obtain the RC time constant of 8.4 μs, the large resistance and capacitance is required. The proposed RC switch is similar to a low pass filter. It utilizes the large dynamic resistance of MOSFET and then requires relatively

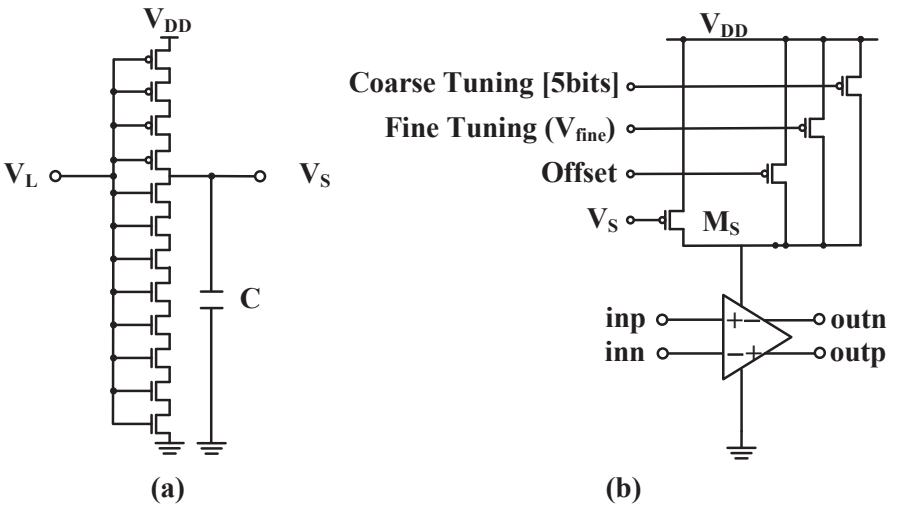


Figure 5.10: (a) RC switch and (b) Modified delay stage of the ring oscillator.

small capacitor. When all MOS sizes are the channel length of 300µm and width of 300nm, its equivalent resistance is $0.66 \sim 0.9M\Omega$.

The clock generator and its waveforms are shown in Fig. 5.11. When LOCKF alarms, the clock generator starts to operate. The clock generator outputs 3 kinds of waveforms, CLKA, CLKB, and CLKC. CLKA is for the sampling of the fine tuning voltage and has high for one period of the input, CLKIN. CLKB is for the reference voltages and has the pulse width of one period of the input. The half period of the input is inserted between the CLKA and CLKB. And CLKC is for comparison between the fine tuning voltage and the reference voltage. CLKC has the half period of the input and. Every clock has the period which is 3 times of the input. CLKA is not overlapped with CLKB and CLKC as shown in Fig. 5.11 (b). When LOCKF has been alarmed and CLKA is high, the sampling of V_{fine} starts. In this case, a lower-limit voltage, V_{LL}, of the initial state is high. When the power supply voltage is decreased, the oscillation frequency of the ring oscillator falls down and then the PLL tries to decrease the fine tuning voltage to maintain the desired frequency. When the fine tuning voltage is lower than the predetermined voltage, then the current source of M_S will be turned on.

Figure 5.12 shows the limit-voltage detector, which detects whether the gate voltage of the fine tuning current source is out of the predetermined voltages,

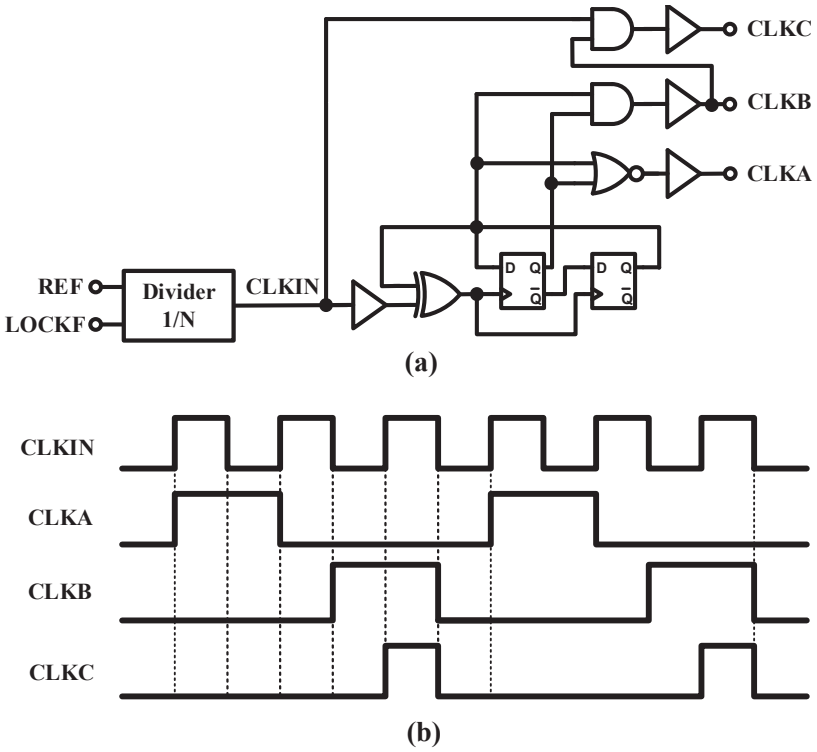


Figure 5.11: Clock generator and its waveforms for the limit-voltage detector.

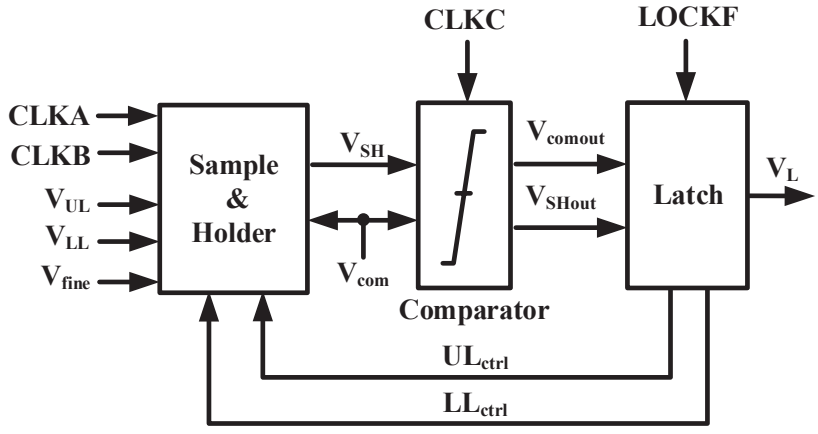
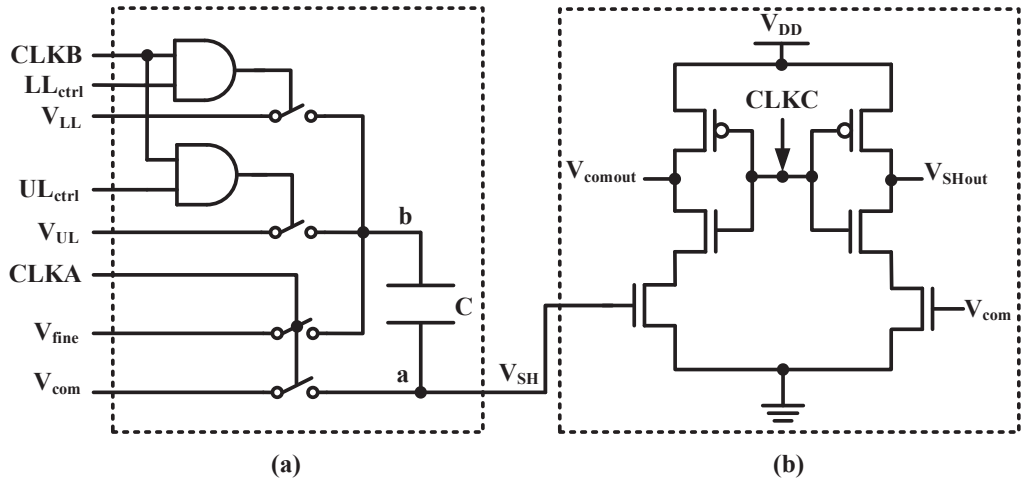


Figure 5.12: Limit-voltage detector.

V_{LL} and V_{UL}. V_{LL} and V_{UL} are the lower- and upper-limit voltages compared to



the gate voltage of the fine tuning current source

Figure 5.13: (a) Sample-and-holder and (b) comparator.

the gate voltage of the fine tuning current source, respectively. The limit-voltage detector is composed of a sample-and-holder, a comparator, and a latch. The sample-and-holder and comparator compare between V_{fine} and the predetermined limit voltages and its result is hold by the latch. The latch is composed of a double tail latch presented in [104] and a SR latch. The latch is reset by LOCKF and outputs three signals, that is, two control signals and V_L. V_L is used to turn on or off the RC switch. Two control signals are UL_{ctrl} and LL_{ctrl}. They are used to control the sample-and-holder to select one of two limit voltages, which is compared to the gate voltage of the fine tuning current source.

It is described about comparison between the limit voltages and the gate voltage of the fine tuning current source. Figure 5.13 shows the sample-and-holder and the comparator in the limit-voltage comparator. Assume that the frequency of the oscillator decreases due to VT variations and then the gate voltage of the fine tuning current source approaches the lower-limit voltage. Thus, the initial state is that LL_{ctrl} is high and UL_{ctrl} is low. When CLKA is high, the capacitor is connected to V_{fine} and V_{com}, which is the reference of the comparator. The charge at node a is

$$Q_a = C(V_{com} - V_{fine}) \tag{5.14}$$

And then CLKB is high and node b is connected to V_{LL}. Since the node a is floating now, the charge, Q_a is not changed. The voltage, V_{SH}, at node a becomes

$$V_{SH} = V_{com} - V_{fine} + V_{LL} \tag{5.15}$$

When CLKC is high, the comparator starts to compare V_{SH} with V_{com}. Assume that V_{SH} is larger than V_{com} .

$$V_{com} - V_{fine} + V_{LL} > V_{com} \tag{5.16}$$

$$V_{LL} > V_{fine} \tag{5.17}$$

It leads to the result that the fine tuning voltage is lower than predetermined lower-limit voltage, V_{LL}. Thus, the current source, M_S, is required to be turned on. Equation 5.17 shows that the comparison is performed between V_{fine} and V_{LL}, not between V_{fine} and the reference, V_{com}, of the comparator. When V_{SH} is larger than V_{com}, V_{SHout} becomes larger than V_{comout}. The latch following the comparator holds the state and changes V_L from low to high. Then the gate voltage, V_S, of the supplementary current source, M_S, changes from the supply voltage to ground very slowly through the RC switch. At the same time, LL_{ctrl} becomes low and LH_{ctrl} does high. This reversion of the control signals is for preparation when the power supply voltage is recovered to the initial voltage. When the power supply voltage is recovered to the initial voltage, the current source, M_S, will be turned off very slowly by the same method.

5.2.4 Simulation Results

Figure 5.14 shows the calculation and simulation results of Δf_{OSC} when the proposed VT variation compensator is used. The relative error is obtained by comparing Δf_{OSC} with the oscillation frequency. The trajectory of the calculation results is similar to simulation results but there is a large difference between them. This difference is considered to be mainly due to the limitation of the linear noise

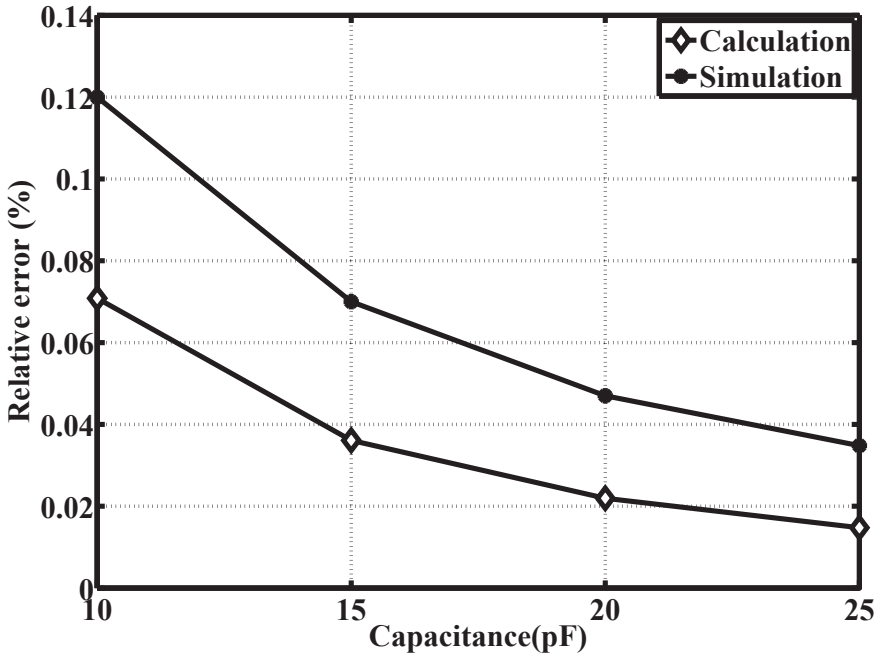


Figure 5.14: Comparison between the calculation and the simulation results of Δf_{OSC} when the proposed VT variation compensator is used.

model and the relatively low accuracy caused by tolerances in the simulation. It is hardly to simulate the PLL for long time with high accuracy. The simulation results show the maximum deviation of the output frequency is below 480kHz when C=20pF. Thus, the injection-locked PLL can maintain the lock state during the compensation.

Figure 5.15 shows the simulation results when the supplementary current source is turned on without the RC switch. The PLL suffers the re-lock procedure for fine tuning. For the re-lock procedure, the injection-lock oscillator may loose the lock-state.

Figure 5.16 shows the simulation results when the supplementary current source is turned on through the RC switch. The capacitance of the RC switch is 20pF and all MOS sizes are the channel length of $300\mu m$ and width of $300nm$ as shown in Fig. 5.10 (a). Its equivalent resistance is $0.66 \sim 0.9M\Omega$ and the loop bandwidth of the PLL is 480kHz when the supply voltage is about 1.08V and V_{fine}

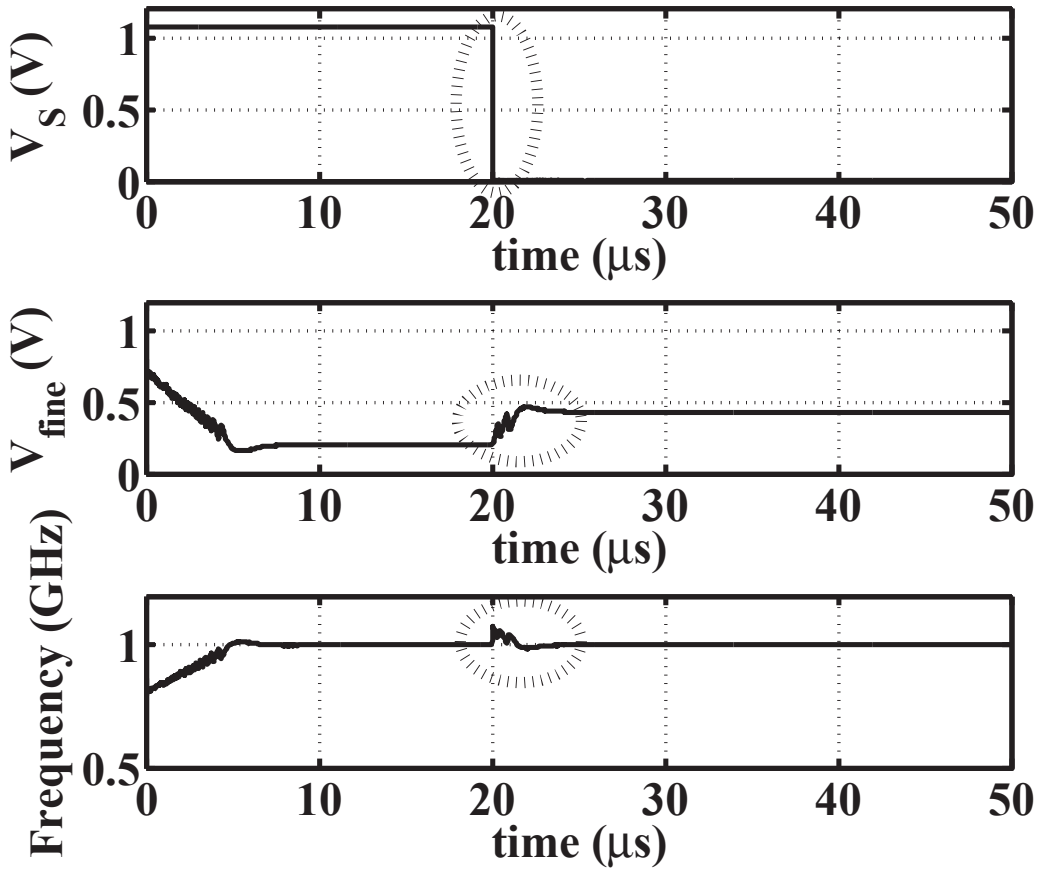


Figure 5.15: Simulation results in the case of without the RC switch.

is 0.2V. The channel width of M_S is a half of the fine tuning current source. When the clock for monitoring is 1MHz, the total current consumption is $102.4\mu A$. Since the supply voltage does not drop in a short time, the monitoring period can be selected to be more lower frequency. Without the RC switch as shown in Fig. 5.15, the control voltage for the supplementary current source abruptly changes from V_{DD} to ground and then the PLL suffers re-lock procedure. However, the PLL with the RC switch maintains the normal lock state. The tolerance to the supply voltage variation is $0.987 \sim 1.26$V. It occupies 22.8% of the regular supply voltage, 1.2V.

It is also possible to obtain the same effect through the increase of sizes of the fine tuning range. It results in the increase of the oscillation gain and the additive

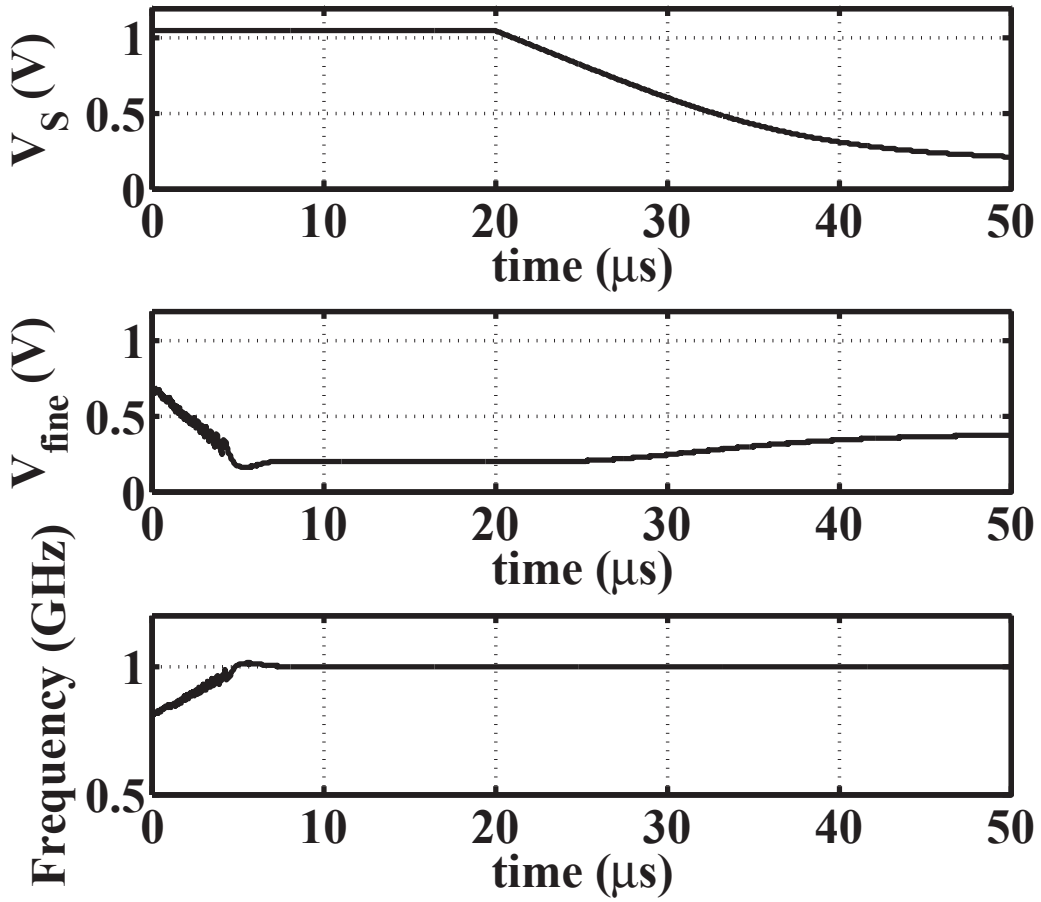


Figure 5.16: Simulation results in the case of with the RC switch.

capacitance about 100pF is required for the loop filter. Thus, this method can achieve the extension of the tolerance to voltage and temperature variations with relatively small area and low current consumption.

5.3 Summary

This chapter introduced the meta-stable detection and enhancement of tolerance to voltage and temperature variations. Meta-stable region is generally avoided but can be used to balance the coverage of the fine tuning range and extend potential tolerance to the voltage and temperature variations.

This chapter also presented the method which can achieve the extension of the tolerance to voltage and temperature variations with relatively small area and small current consumption. The proposed method can enhance the tuning range of the oscillator in the PLLs without the re-lock procedure or the pause of the system.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis has raised challenges in the design of the phase locked loops in nanometer CMOS processes. As the CMOS processes are scaled down, the systems embedded in CMOS processes are suitable for high frequency operations. However, the phase locked loops generating relatively low operation frequency has faced challenges, since the passive components like inductors are hardly scaled down. Thus, this thesis has discussed about an injection-locked charge-pump phase-locked loop (PLL) with a replica of a ring oscillator as an alternative proposal. Though the injection-locked oscillator has introduced long time ago, it has seldom used as a frequency multiplier since it is substantially difficult to secure the stable lock state due to quite narrow range, poor modeling, and so on.

This thesis has proposed a model of the direct injection-locked ring oscillator based on its output waveforms and derived the maximum achievable lock range, which is expressed only with the frequencies of the injection signal and the oscillation. It can provide insight and design guideline for designers. Though the careful investigations about process, supply voltage, and temperature variations, the proposed injection-locked PLL has the tolerance to a voltage variation of $-5.8\% \sim 5.0\%$ in supply voltage of 1.2 V. In-band noises of the injection-locked oscillator at offset frequencies of 10kHz and 100kHz are -108.2dBc/Hz and -114.6dBc/Hz, respectively. Moreover, the metastable range detection method is

introduced to achieve a balance of frequency coverage of the PLL and to extend potential tolerance to the voltage and temperature variations. Also, the compensation technique to voltage and temperature variation in the injection-locked PLL has been introduced to enhance the tolerance to the variations with relatively small area and small current consumption. When the PLL is required to have more wide tolerance to supply voltage and temperature variation after its design is already finished, it can be easily achieved by adding the compensator without the overall modification of the PLL.

6.2 Future Work

There remain two major problems in the proposed injection-locked PLL. They are power consumptions and occupied chip area. The proposed injection-locked charge pump PLL has two oscillators to avoid the confliction between phase realignments by the PLL loop and the injection. In order to have sufficient tolerance to process variation, chip area of the oscillators should be large enough and the power consumption for the oscillators becomes twice to the conventional PLLs with one oscillator.

If it is possible for the injection-locked oscillator to be included in the loop of the PLL, there is no necessary for two oscillators. Moreover, if analog filter is replaced with digital filter, the chip area can be considerably reduced. However, they lead the designer again to the same problems in the conventional injection-locked PLL, which are presented in the chapter 4.

Nevertheless, they may be possible. The phase confliction is due to high performance of the PFD, which realigns the phases of the reference and the output of the divider to be same. If the PFD has somewhat margin based on the multiplication ratio to track the phase of the divider without interrupting the injection, the injection-locked oscillator can be inserted in the loop of the PLL.

Furthermore, it is desired to optimize trade-offs among the overall phase noise, the phase noises of the reference and oscillator, and the frequency multiplication ratio. For the optimization, the noise analysis on the direct injection-locked oscillator should be researched beforehand.

Bibliography

[1] L. Counts, "Analog and Mixed-Signal Innovation: The Process-Circuit-Application Interaction,"*ISSCC Dig. Tech. Paper*, pp. 26-29, 2007.

[2] C. Azeredo-Leme, "Clock Jitter Effects on Sampling: A Tutorial," *IEEE Circuits and Systems Magazine*, vol.11, pp. 26-37, Oct. 2011.

[3] A. Aktas and M. Ismail, *CMOS PLLs and VCOs for 4G Wireless*, USA: Kluwer Academic Publishers, 2004.

[4] R. Sobot, *Wireless Communication Electronics: Introduction to RF Circuits and Design Techniques*, NY: Springer, 2012.

[5] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, vol. 38, no. 8, pp. 33-35, Apr. 1965.

[6] H. Iwai, "CMOS scaling towards its limits," *Solid-State and Int. Circuit Technology, 5th Intl. Conf. on*, pp. 31-34, Oct. 1998.

[7] Y. Taur, "CMOS design near the limit of scaling," *IBM Journal of Research and Development* , vol. 46, no. 2/3, pp. 213-222, Mar. 2002.

[8] E. J. Nowak, "Maintaining the benefits of CMOS scaling of CMOS scaling when scaling bogs down," *IBM J. RES. DEV.*, vol. 46, no. 2, Mar. 2002.

[9] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," *IEDM Technical Digest*, pp. 7-15, 2005

[10] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong, and F. Boeuf, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16-26, Jan. 2005.

[11] R.D. Isaac, "The future of CMOS technology," *IBM Journal of Research and Development* , vol. 44, no. 3, pp. 369-378, May 2000.

[12] N. Z. Haron and S. Hamdioui, "Why is CMOS scaling coming to an END?" *in Proceedings of International Design and Test Workshop*, pp. 98-103, 2008.

[13] H. Iwai, "Roadmap for 22nm and beyond," *Microelctron. Eng.*, vol. 86, no. 7-9, pp. 1520-1529, 2009.

[14] F. Ellinger, M. Claus, M. Schröter and C. Carta, "Review of Advanced and Beyond CMOS FET Technologies for Radio Frequency Circuit Design," *Proc. IMOC 2011*, pp. 347-351, 2011

[15] K. Zhang, "Challenges and opportunities for circuit design in nano-scale CMOS technologies," *ESSCIRC 2012*, pp. 28-29, 2012.

[16] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Trans. on Electron Devices*, vol. 59, no. 7, pp. 1813-1828, Jul. 2012.

[17] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits*, vol. sc-9, no. 5, pp. 256-268, Oct. 1974.

[18] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park, and B.-I. Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. on Electron Devices*, vol. 52, no. 7, pp. 1415-1422, Jul. 2005.

[19] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog Circuit Design in Nanoscale CMOS Technologies," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1687-1714, Oct. 2009.

[20] L. L. Lewyn, "Is a New Paradigm for nanoscale Analog CMOS Design Needed?" *Proceedings of the IEEE*, vol. 99, no. 1, pp. 3-6, Jan. 2011.

[21] ITRS, "ITRS Reports," Available for download at http://www.itrs.net/reports.htm.

[22] J. N. Burghartz, et.at, "RF Potential of a 0.18-μm CMOS Logic Device Technology," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 864-870, Apr. 2000.

[23] A. Matsuzawa, "RF-SoC Expectations and Required Conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 245-253, Jan. 2002. 2000.

[24] M.-T. Hsieh and G. E. Sobelman, "Comparison of LC and Ring VCOs for PLLs in a 90 nm Digital CMOS Process," *Proceedings, International SoC Design Conference*, pp. 19-22, 2006.

[25] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," *IEEE Journal of Solid-Stage Circuits*, vol. 41, no. 8, pp. 1803-1816, Aug. 2006.

[26] B. Brannon and A. Barlow, "Aperture Uncertainty and ADC System Performance," *Application Note AN-501*, Analog Devices, Inc., Jan. 1998.

[27] Y. Kobayashi, S. Amakawa, N. Ishihara, and K. Masu, "A Low-Phase-Noise Injection-Locked Differential Ring-VCO with Half-Integral Subharmonic Locking in 0.18um CMOS," *European Solid-State Circuits Conference (ESSCIRC)*, pp. 440-443, Sep. 2009.

[28] S. Lim and M. Fujishima, "24GHz 1.89mW 12x CMOS Frequency Multiplier Using Pulse-Injected Oscillator," *Proceedings, European Microwave Integrated Circuits Conference*, pp. 180-183, 2009.

[29] C.-F. Liang, K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," *ISSCC Dig. Tech. Papers*, pp. 90-92, Feb. 2011.

[30] Y.-C. Huang and S.-I. Liu, "A 2.4GHz Sub-Harmonically Injection-Locked PLL With Self Calibrated Injection Timing," *ISSCC Dig. Tech. Papers*, pp. 338-340, Feb. 2012.

[31] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara, and K. Masu, "An Indcutorless Injection-Locked PLL with 1/2 and 1/4- Integral Subharmonic Locking in 90nm CMOS," *2012 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 189-192, Jun. 2012.

[32] J. Han, M. Miyahara, and A. Matsuzawa, "An Injection-locked Ring Oscillator for an ADC and a DAC embedded in a 38GHz-band FWA System,"

International Workshop on Millimeter Wave Wireless Technology and Applications, pp. 126-127, Dec. 2010.

[33] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers", *IEEE J. Solid-State Circuits*, vol. 34, pp.813 -821, 1999

[34] A. Mirzaei, M. E. Heidari, R. Bagheri and A. A. Abidi, "Multi-Phase Injection Widens Lock Range of Ring-Oscillator-Based Frequency Dividers", *IEEE J. Solid-State Circuits*, vol. 45, pp. 656 - 671, Mar. 2008.

[35] S. Hara, K. Okada, and A. Matsuzawa, "10MHz to 7GHz Quadrature Signal Generation Using a Divide-by-4/3, -3/2, -5/3, -2, -5/2, -3, -4, and -5 Injection-Locked Frequency Divider," *VLSI 2010*, pp. 51-52, Jun. 2010.

[36] M. A. Awan, M. S. Asghar and M. P. Kennedy, "A "divide-by-odd number" direct injection CMOS LC injection-locked frequency divider", *ICECS 2010*, pp. 488 - 491, 2012.

[37] M. P. Li, *Jitter, Noise, a Signal Integrity at High-Speed*, USA: Springer, 2007.

[38] F. Herzel and B. Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate," *IEEE Transactions on Circuits and Systems*, vol. 46, pp. 56-62, Jan. 1999.

[39] B. Razavi, *Design of Analog Integrated Circuit.*, USA: McGraw-Hill, 2001.

[40] C. Bowick, J. Blyler, and C. Aljuni, *RF CIRCUIT design.*, UK: Newnes, 2008.

[41] M. Hershenson, A. Hajimiri, S. S. Mohan, S. P. Boyd, and T. H. Lee, "Design and optimization of LC oscillator," *Proc. IEEE/ACM Int. Conf. Computer Aided Design*, pp. 65 -69, 1999.

[42] A. Hajimiri, S. Liimotyakis, and T. H. Lee, "Jitter and Phase Noise in Ring Oscillators," *IEEE J. Solid-state Circuits*, vol. 34, no. 6, pp. 790-804, Jun. 1999.

[43] J. S. and C. F. Hawkins, *CMOS ELECTRONICS.*, New Jersey: John Wiley & Sons, Inc., 2004.

[44] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE Journal of Solid-Stage Circuits*, vol. 31, no. 3, pp. 331-343, Mar. 1996.

[45] S. Docking and M. Sachdev, "An Analytical Equation for the Oscillation Frequency of High-Frequency Ring Oscillators," *IEEE Journal of Solid-Stage Circuits*, vol. 39, no. 3, pp. 533-537, Mar. 2004.

[46] C. Chung, S.-Y. Chao and M. F. Lu, "Nonlinear Feedback System for an Inverter-Based Ring Oscillator," *WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS*, issue 7, vol. 8, pp. 538-547, Jun. 2009.

[47] A. Homayoun and B. Razavi, "Relation Between Delay Line Phase Noise and Ring Oscillator Phase Noise," *IEEE Journal of Solid-Stage Circuits*, issue 2, vol. 49, pp. 384-391, Feb. 2014.

[48] T.-N. Luo and Y.-J.E. Chen, "A 0.8-mW 55-GHz Dual-Injection-Locked CMOS Frequency Divider," *IEEE Trans. on Microwave Theory and Techniques*, vol. 56, pp. 620 - 625, Mar. 2008.

[49] B. Y. Lin, K. H. Tsai, and S. I. Liu, "A 128.24-to-137.00 GHz injection-locked frequency divider in 65 nm CMOS," *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, pp. 282-283, Feb. 2009.

[50] L. Wu and H.C. Luong, "Analysis and Design of a 0.6 V 2.2 mW 58.5-to-72.9 GHz Divide-by-4 Injection-Locked Frequency Divider With Harmonic Boosting", IEEE Trans. on Circuits and Systems, vol. 60, pp. 2001 - 2008, Aug. 2013.

[51] B. Razavi, "A Study of Injection Locking and Pulling in Oscillators," *IEEE Journal of Solid-Stage Circuits*, vol. 39, no. 9, pp. 1415-1424, Sep. 2004.

[52] Y. Tsividis, *Operation and Modeling of the MOS Transistor.*, Second Ed., Boston: McGraw-Hill, 1999.

[53] J. Chang, A. A. Abidi, and C.R. Viswanathan, "Flicker noise in CMOS Transistors from Subthreshold to Strong Inversion at Various Temperatures," *IEEE Trans. On Electron Devices*, vol. 41, no. 11, pp. 1965-1971, Nov. 1994.

[54] A. Hajimiri, and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE J. Solid-state Circuits*, vol. 33, no. 2, pp. 179-194, Feb. 1998.

[55] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Trans. on Comm*, vol. COM-28, no. 11, pp. 1849-1980, Nov. 1980.

[56] F. M. Garder, *Phaselock Techniques.*, USA: Wiley-Interscience, 2005.

[57] K. Shu, and E. Sánchez-Sinencio, it CMOS PLL Synthesizers: Analysis and Design, USA: Springer, 2005.

[58] M. Tiebout, "A CMOS Fully Integrated 1GHz and 2GHz Dual Band VCO with a Voltage Controlled Inductor," *ESSCIRC 2002*, pp. 799-802, Sep. 2002.

[59] X. Gao, E.A.M. Klumperink, M. Bohsali, and B. Nauta, "A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and 0.15psrms jitter in 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 392-393,393a, Feb. 2009.

[60] B. M. Helal, C. Hsu, K. Jonson, and M. H. Perrott, "A Low Jitter Programming Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop," *IEEE Journal of Solid-Stage Circuits*, vol. 44, no. 5, pp 1391-1400, 2009.

[61] J. Lee and H. Wang, "Study of Subharmonically Injection-Locked PLLs," *IEEE Journal of Solid-Stage Circuits*, vol. 44, no. 5, pp. 1539-1553, May 2009.

[62] R. Adler, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 61, pp. 1380-1385, Oct. 1973.

[63] S. Verma, H. R. Rategh, and T. H. Lee, "A Unified Model for Injection-Locked Frequency Dividers," *IEEE Journal of Solid-Stage Circuits*, vol. 38, no. 6, pp. 1015-1027, Jun. 2003.

[64] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked LC dividers for quadrature generation," *IEEE J. Solid-StateCircuits*, vol. 39, no. 9, pp. 1425-433, Sep. 2004.

[65] F.-H. Huang and Y.-J. Chan, "A V-Band CMOS Injection-Locked Oscillator Using Fundamental Harmonic Injection," *IEEE Microwave and Wireless Components Letters*, vol. 17, pp 882-884, 2007

[66] K. Takano, M. Motoyoshi, and M. Fujishima, "4.8GHz CMOS Frequency Multiplier with Subharmonic Pulse-Injection Locking," *IEEE Asian Solid-State Circuits Conference*, pp. 336-339, Nov. 2007.

[67] N. Kanameru, S. Ikeda, S. Lee, S. Tanoi, H. Ito, N. Ishihara, and K. Masu, "A Ring-VCO-Based Injection-Locked Frequency Multiplier Using a New Pulse Generation Technique, *International SoC Design Conference 2011 (ISOCC)*, pp. 32-35, Nov. 2011.

[68] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A Compact, Low-Power and Low-Jitter Dual-Loop Injection-Locked PLL Using All-Digital PVT Calibration," *IEEE Journal of Solid-Stage Circuits*, vol. 49, no. 1, pp. 50-60, Jan. 2014.

[69] C. A. Kingsford-Smith, "Device for Synthesizering Frequencies Which Are Rational Multiples of a Fundamental Frequency," U.S. Patent No. 3,928,813, field Sept. 26, 1974, issued Dec. 23, 1975.

[70] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *Proceedings of the IEEE*, vo. 51, no. 11, pp.1524-1535, Nov. 1963.

[71] T. Jackson, "Fractional-N Synthesizer," U.S. Patent No. 4,758,802, PCT field Feb. 21, 1986, issued Jan. 19. 1988.

[72] M. Kondou, A. Matsuda, H. Yamazaki, and O. Kobayashi, "A 0.3mm^2 90-to-770MHz Fractional-N Synthesizer for a Digital TV Tuner," *ISSCC Dig. Tech. Papers*, pp. 248-250, Feb. 2010.

[73] D.-W. Jee, Y. Suh, H.-J. Park, and J.-Y. Sim, "A 0.1-f_{ref} BW 1GHz Fractional-N PLL with FIR Embedded Phase-Interpolator-Based Noise Filtering," *ISSCC Dig. Tech. Papers*, pp. 94-96, Feb. 2011.

[74] M.-H. Hsieh, L.-H. Chen, S.-I. Liu, C. C.-P. Chen, "A 6.7MHz-to-1.24GHz 0.0318mm^2 Fast-Locking All-Digital DLL in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 244-246, Feb. 2012.

[75] T.-K. Jang, X. Nan, F. Liu, and J. Shin, "A 0.026mm2 5.3mW 32-to-2000MHz Digital Fractional-N Phase Locked-Loop Using a Phase-Interpolating Phase-to-Digital Converter," *ISSCC Dig. Tech. Papers*, pp. 254-256, Feb. 2013.

[76] Z. Tang, X. Wan, M. Wang, and J. Liu, "A 50-to-930MHz Quadrature-Output Fractional-N Frequency Synthesizer with 770-to-1860MHz Single-Inductor LC-VCO and Without Noise Folding Effect for Multistandard DTV Tuners," *ISSCC Dig. Tech. Papers*, pp. 358-360, Feb. 2013.

[77] S.-A. Yu and P. Kinget, "A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 302-303, 604, Feb. 2007.

[78] X.i Yu, Y. Sun, L. Zhang, W. Rhee, and Z. Wang, "A 1GHz Fractional-N PLL Clock Generator with Low-OSR $\Sigma\Delta$ Modulation and FIR-Embedded Noise Filtering," *ISSCC Dig. Tech. Papers*, pp. 346-347, 618, Feb. 2008.

[79] R. B. Staszewski, D. Leipold and P. T. Balsara, "A first multigigahertz digitally controlled oscillator for wireless applications," *IEEE Transactions on Microwave theory and techniques*, vol. 51, no. 11, pp. 2154- 2164. Nov. 2003.

[80] P.-L. Chen, C.-C. Chung, and C.-Y. Lee, "A portable digitally controlled oscillator using novel varactors," *IEEE Transactions on Circuits and Systems II*, vol. 52, no. 5, pp. 233-237, 2005.

[81] S. M. Rezaul Hasan, "A novel 16-bit CMOS digital controlled Oscillator," *IEEE international symposium on circuit and system*, pp. 680- 684, Aug. 6-9, 2006.

[82] Y.-M. Chung and C.-L. Wei, "An all-digital phase-locked loop for digital power management integratged chips," *IEEE international symposium on circuit and system*, pp. 2413-2416, May 2009.

[83] K.-H. Choi, J.-B. Shin, J.-Y. Sim and H.-J. Park, "An interpolating digital controlled oscillator for wide range all digital PLL," *IEEE transaction on circuits and systems-I*, vol. 56, no. 9pp. 2055-2063, Sep. 2009.

[84] L. Fanori, A. Liscidini, and R. Castello, "3.3GHz DCO with a Frequency Resolution of 150Hz for All-Digital PLL," *ISSCC Dig. Tech. Papers*, pp. 48-51, Feb. 2010.

[85] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line," *IEEE Journal of Solid-State Circuits*, vol. 35, No. 2, pp. 240-246, Feb. 2000.

[86] J. Kim and S. Cho, "A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage-Controlled Oscillator," *IEEE international symposium on circuit and system, 2009 (ISCAS 2006)*, pp. 3934-3937, 21-24 May 2006.

[87] J. Tangudu, S. Gunturi, S. Jalan, J. Janardhanan, R. Ganesan, D. Sahu, K. Waheed, J. Wallberg, and R. B. Staszewski, "Quantization Noise Improvement of Time to Digital Converter (TDC) for ADPLL," *IEEE international symposium on circuit and system, 2009 (ISCAS 2009)*, pp. 1020-1023, 24-27 May 2009.

[88] J. Yu, F. F. Dai, and R.C. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13μm CMOS Technology," *IEEE VLSI Symp. Dig. Tech. Papers*, pp. 232-233, Jun. 2009.

[89] R.B. Staszewski, et.at., "All-Digital PLL and Transmitter for Mobile Phones," *IEEE Journal of Solid-Stage Circuits*, vol. 40, no 12, pp. 2469-2482, Dec. 2005.

[90] D. Shin, J. Song, H. Chae, K.-W. Kim, Y. J. Choi, and C. Kim, "A 7ps-Jitter 0.053mm^2 Fast-Lock ADDLL with Wide-Range and High-Resolution All-Digital DCC," *ISSCC Dig. Tech. Papers*, pp. 184-185, 595, Feb. 2007.

[91] T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, and M. Fukaishi, "A 2.1-to-2.8GHz All-Digital Frequency Synthesizer with a Time-Windowed TDC," *ISSCC Dig. Tech. Papers*, pp. 470-472, Feb. 2010.

[92] A. Sai, et.at., "A 570fsrms Integrated-Jitter Ring-VCO-Based 1.21GHz PLL with Hybrid Loop," *ISSCC Dig. Tech. Papers*, pp. 98-100, Feb. 2011.

[93] A. Sai, Y. Kobayashi, S. Saigusa, O. Watanabe, and T. Itakura, "A Digitally Stabilized Type-III PLL Using Ring VCO with 1.01psrms Integrated Jitter in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 248-250, Feb. 2012.

[94] J.-P. Hong, S.-J. Kim, J. Liu, N. Xing, T.-K. Jang, J. Park, J. Kim, T. Kim, and H. Park, "A 0.004mm^2 250μW $\Delta\Sigma$ TDC with Time-Difference Accumulator and a 0.012mm^2 2.5mW Bang-Bang Digital PLL Using PRNG for Low-Power SoC Applications," *ISSCC Dig. Tech. Papers*, pp. 240-242, Feb. 2012.

[95] S. Ye, L. Jansson, and I. Galton, "A Multiple-Crystal interface PLL with VCO realignment to reduce phase noise," *IEEE Journal of Solid-Stage Circuits*, vol. 37, no. 12, pp. 1795- 1803, Dec. 2002.

[96] K. Takano, M. Motoyoshi, and M. Fujishima, "4.8GHz CMOS Frequency Multiplier with Subharmonic Pulse-Injeciton Locking," *IEEE Asian Solid-State Circuits Conference*, pp. 336-339, 12-14 Nov. 2007.

[97] W. L. Chan, J. R. Long, and J. J Pekarik, "A 56-to-65GHz Injection-Locked Frequency Tripler with Quadrature Outputs in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 480-481, 629, Feb. 2008.

[98] L.-H. Lu, and J.-C. Chien, "A Wide-Band CMOS Injeciton-Locked Ring Oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 15, No. 10, pp. 676-678, 2005.

[99] Y.-H. Chuang, S.-H. Lee, S.-L. Jang, J.-J Chao, and M.-H Juang, "A Ring-Oscillator-Based Wide Locking Range Frequency Divider," *IEEE Microwave and Wireless Components Letters*, vol. 16, No. 8, pp. 470-472, Aug. 2006.

[100] J.-C. Chien and L.-H. Lu, "40GHz Wide-Locking-Range Regenerative Frequency Divider and Low-Phase-Noise Balanced VCO in 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 544-545, 621, Feb. 2007.

[101] S.-L. Jang Y.-H. Chuang, S.-H. Lee, and J.-J. Chao, "Circuit Techniques for CMOS Divide-by-Four Frequency Divider," *IEEE Microwave and Wireless Components Letters*, vol. 17, No. 3, pp. 217-219, Mar. 2007.

[102] F. Brandonisio and M. P. Kennedy, "Comparison of Ring and LC Oscillator -based ILFDs in Terms of Phase Noise, Locking Range, Power Consumption and Quality Factor," *Research in Microelectronics and Electronics 2009*, pp. 292-295, 12-19 Jul. 2009.

[103] Y. Mo, E. Skafidas, R. Evans, and I. Mareels, "A 40GHz Power Efficient Static CML Frequency Divider in 0.13μm CMOS Technology for High Speed Milimeter-Wave Wireless Systems," *Circuits and Systems for Communications 2008 (ICCSC 2008)*, pp. 812-8115, 26-28 May 2008.

[104] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.022mm^2 970μW Dual-Loop Injection-Locked PLL with -243dB FOM Using Synthesizable All-Digital PVT Calibration Circuits," *ISSCC Dig. Tech. Papers*, pp. 248-249, Feb. 2013.

[105] M. Miyahara, Y. Asada, D. Paik and Akira Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," *in Proc. A-SSCC*, pp 269-272, Nov. 2008.

Appendix A

List of Published Papers

A.1 Journal Papers

Jeonghoon Han, Masaya Miyahara, and Akira Matsuzawa, "Injection Locked Charge-Pump PLL with a Replica of the Ring Oscillator," *IEICE Trans. Electronics*, vol. E97-C, no. 4, pp. 316-324 April 2014.

Jeonghoon Han, Masaya Miyahara, and Akira Matsuzawa, "Extension method of tolerance to voltage and temperature variations in an injection-locked PLL," *IEICE Electronic Express*, vol. 11, no. 9, pp. 20140127, 2014.

A.2 International Conferences and Workshops without review

Jeonghoon Han, Masaya Miyahara, and Akira Matsuzawa, "An Injection-locked Ring Oscillator for an ADC and a DAC embedded in a 38GHz-band FWA System," *International Workshop on Millimeter Wave Wireless Technology and Applications*, pp.126-127, Tokyo, Japan, Dec. 2010.

A.3 Domestic Conferences and Workshops

Jeonghoon Han, Kenich Okada, and Akira Matsuzawa, "A Low Noise Current Source for Ring Oscillators," *IEICE Society Conference*, C-12-37, Sep. 2009.

A.4 Co-Authors

A.4.1 International Conferences and Workshops

Ahmed Musa, Jeonghoon Han, Kenich Okada, Akira Matsuzawa, "Injection Locked 1.17GHz 7.2mW Dual Ring VCOs with Synthesizable All Digital PVT Calibration Circuitry," *IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview*, Feb. 2012.