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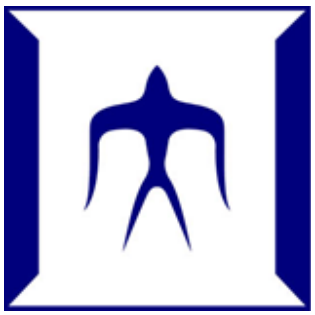

Study of Digital-Intensive Ultra-Low-Power Wireless Transceiver

by

Bangan Liu

A Ph.D. dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Department of Physical Electronics

in the

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of

Tokyo Institute of Technology

Supervised by

Professor Kenichi Okada

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To my family

Acknowledgment

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Abstract

Battery-powered communication devices require power efficient wireless transceivers. Compared to conventional analog-intensive counterparts, the digital-intensive transceivers are more versatile and flexible, and more compatible to advanced CMOS technologies. With proposed digital intensive differential duobinary modulation, an IEEE 802.11ad spectrum mask compliant transmitter modulator was realized with 24.3mW at 1.7Gbps date rate. It achieved a 50% reduction in power consumption compared to the state-of-the-art modulator implementations at similar data rate. Besides, digital-intensive transceivers enabled extensive digital calibration, and accelerated design speed. A sub-GHz transceiver with a ring oscillator based local oscillator, a fully-synthesizable digital transmitter and a digital-intensive receiver was implemented with 3.3/4.6mW power consumption in receiver and transmitter mode respectively. The transceiver achieved 21.7% system efficiency at 0dBm output power, which is 10 times higher than current products, thanks to the digital-intensive architecture and the extensive digital calibrations.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Since its inception in 1958, integrated circuits has revolutionized the human society from many different aspects. Today, after six decades's progress, the integration density have reached unprecedented level. A single CPU die would have billions of transistors. With it, numerous inconceivable applications have become reality. Today people communicate through cell phones, work on the computers, exercise with smart watches and bracelets, and commute with cars which equipped with various sensors and radars. What is more, a number of new applications are at the brink of large scale commercialization.

Among the various applications, the internet of things (IoT) will be one of the most exciting one. As shown in Fig. 1.1, there are many possible IoT applications. In the health care, the IoT enabled medical devices would monitor the physiological parameters in a 24-7 style, and give doctors a complete view of the patients. With the IoT, the vehicles could communicate with each other, and the infrastructure. And together will more powerful artificial intelligent (AI) chips and enhanced wireless links with ultra-reliable low latency communication (URLLC), autonomous driving cars would free people from the daily chores of commuting. And human-less factories and smart home appliances would be reality, with massive deployment of IoT devices.

Actually, due to its wide application, it has been predicated that the number of IoT devices will soon surpass all the other kinds of wireless devices combined, as shown in Fig. 1.2. And form the market share perspective, the IoT applications will enjoy a hefty Compound Annual Growth Rate (CAGR) of 39%, much higher than any other segmentation of the IT industry.

However, to fulfill of the potential IoT application, several obstacles need to be addressed. One of the limiting factor of current IoT devices is their poor power efficiency. As most IoT devices are operating on batteries, the battery capacity limits the operation time. Unfortunately, due to the physical limitation of battery technology, the progress of

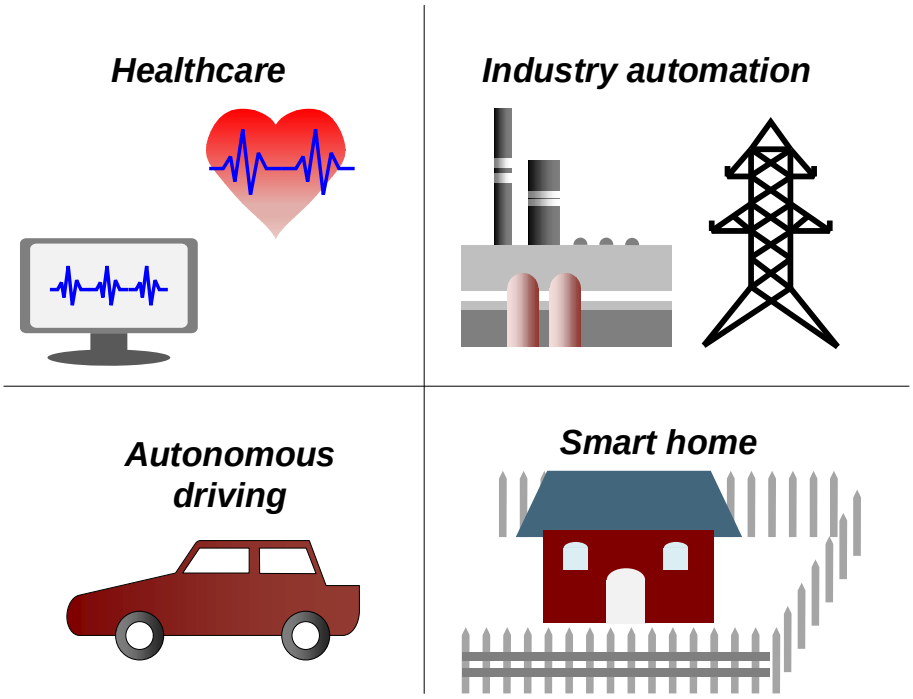


Figure 1.1: Applications of Internet of Things (IoT).

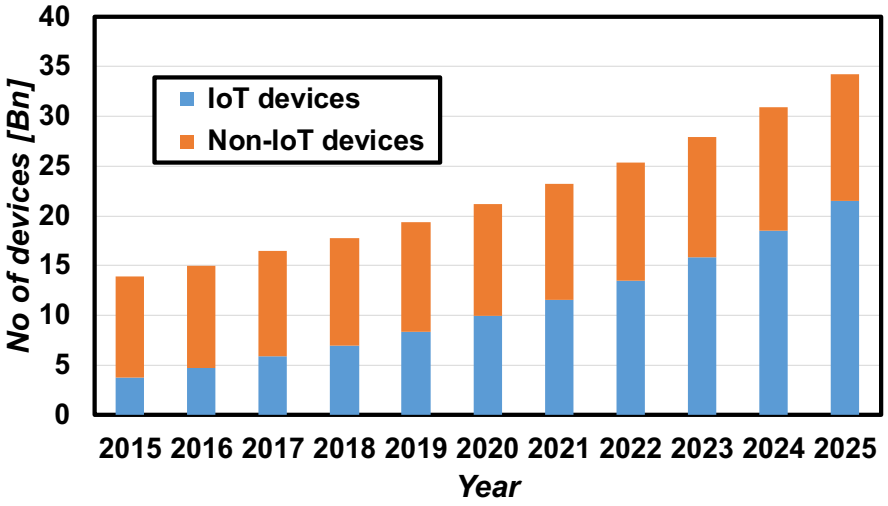


Figure 1.2: Predication of IoT device number [1].

power density (defined as W·h/kg) of batteries has lagged behind for a long time. Therefore IoT devices with higher power efficiency is required. Based on predication in Fig. 1.3, the power efficiency need an x100 improvement in the next decade, which necessities a rethink of low power design methodology for wireless transceivers.

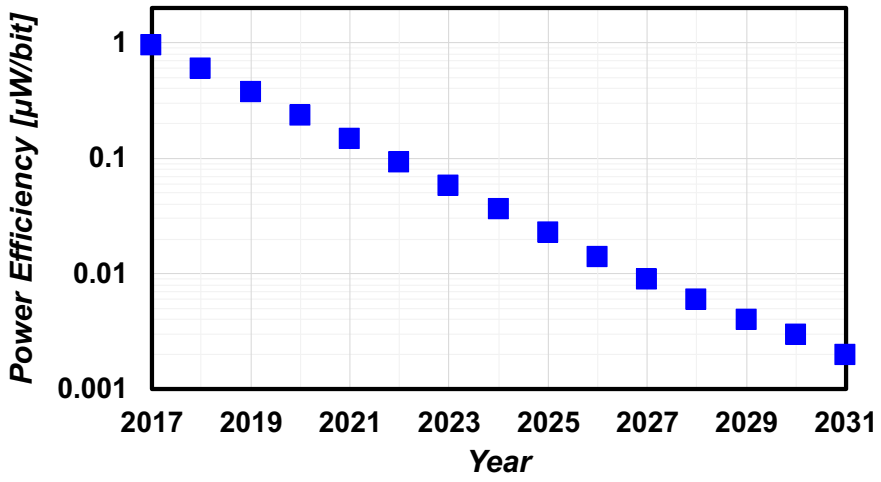


Figure 1.3: Predicated power efficiency improvement of IoT devices [2].

1.1 Implication of process scaling

Together with the evolution of wireless communication systems, the CMOS process also progress. With the process scaling, various challenges emerges, which have profound impact on the circuit design. In this section, the implications of CMOS process scaling for circuit design will be discussed.

1.1.1 Device speed and supply voltage

The first trend of process scaling is the improvement of device speed. As shown in Fig. 1.4, the transit frequency (f_t) of CMOS transistors has improved by more than 8 times from to 180 nm to 7 nm process. With this kind of speed improvement, both analog circuit and digital circuit benefit dramatically. And numerous new applications have been possible with CMOS process, such as mm-wave phased arrays, THz transceivers and image sensors. However, the process scaling is not always beneficial. One adverse result of process scaling is the reduction of supply voltage VDD. In the latest 7 nm CMOS process, the core supply voltage have reduced to around 0.6 V. Together with these two trends, the signal transition of transistors have become faster and sharper, as shown in Fig. 1.5.

This might not be a problem for digital circuits. Actually for digital logic, only the switch mode matters. And the lower propagation delay helps to achieve higher operation speed. On the other hand, the analog circuits rely on the intermediate voltage range for linear operation. As the signal slope increases and supply reduces, the voltage headroom for linear operation has reduced significantly. The analog circuits has become more like

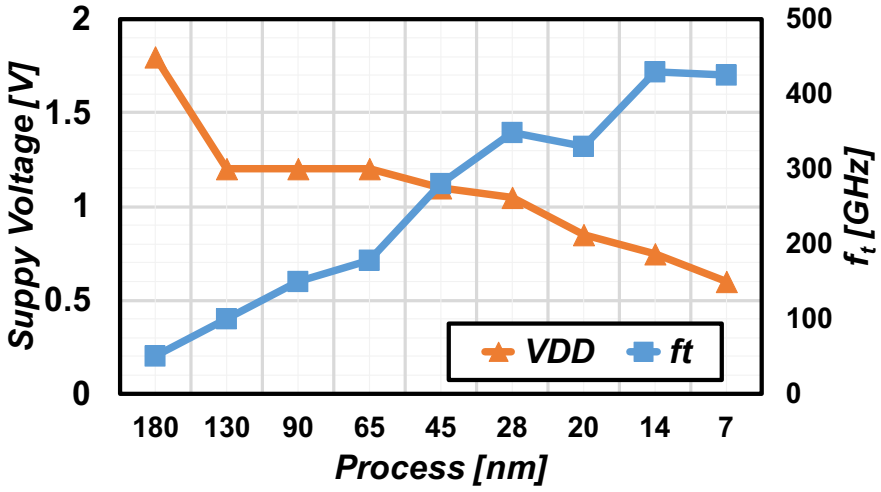


Figure 1.4: Transit frequency (f_t) and supply voltage (VDD) of representative processes [2, 3].

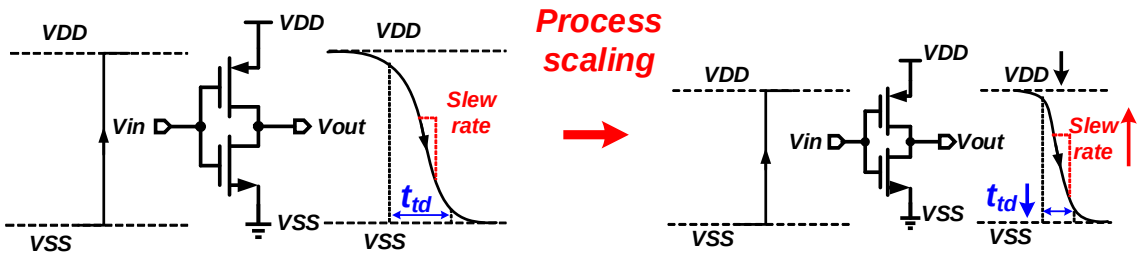


Figure 1.5: Process scaling on time domain behavior.

switch devices than conventional linear circuits. Due to this reason, various analog circuits have been re-designed, which exhibit switch mode operation

1.1.2 Area scaling

Another benefit of process scaling in the area reduction of transistors, as shown in Fig. 1.6. Actually, with the saturation of device speed improvement, the area reduction has been the most dominant driving force behind the process scaling.

However, the process scaling mainly benefit the design of digital circuits, whereas the analog circuit benefit to a lesser extent, as shown in Fig. 1.7. For digital circuits designed with digital standard cells, only transistors are used. Therefore the circuit area scales with transistor size. On the other hand, in analog circuits the area is mainly consumed by passive devices such as resistors, capacitors and inductors, and the transistors only occupy

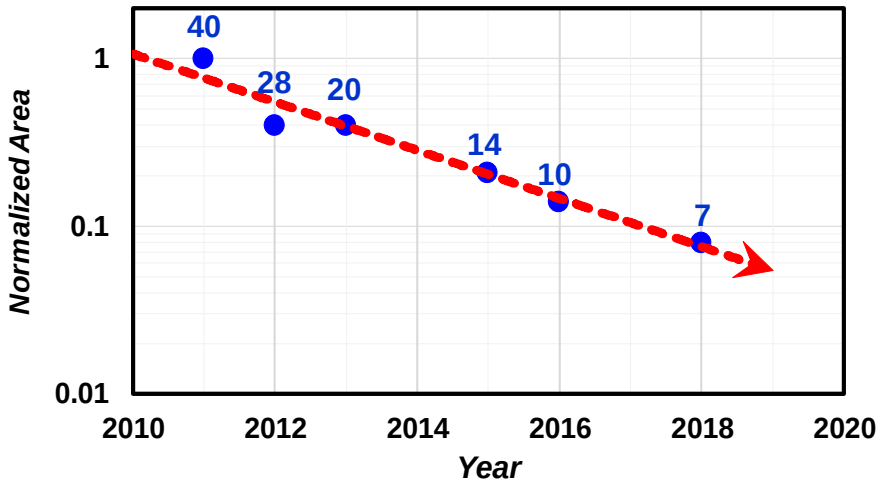


Figure 1.6: Relative area of standard cell size across processes [4].

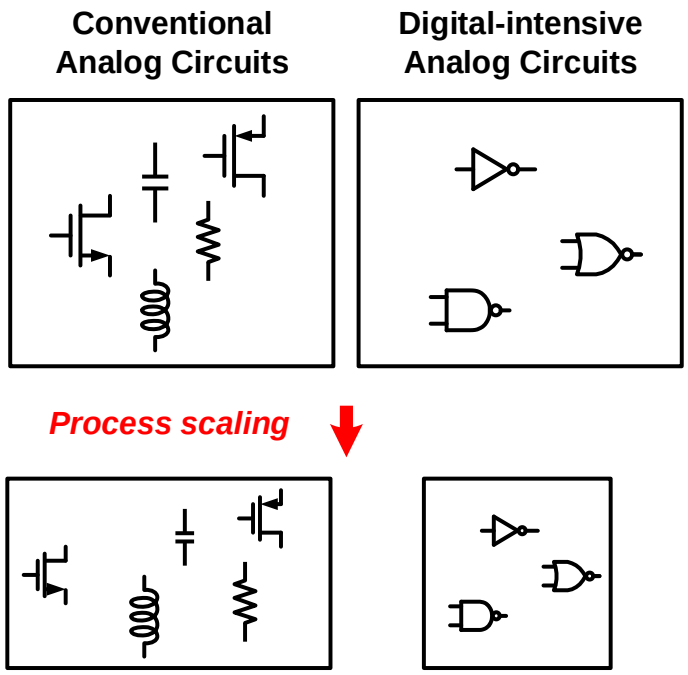
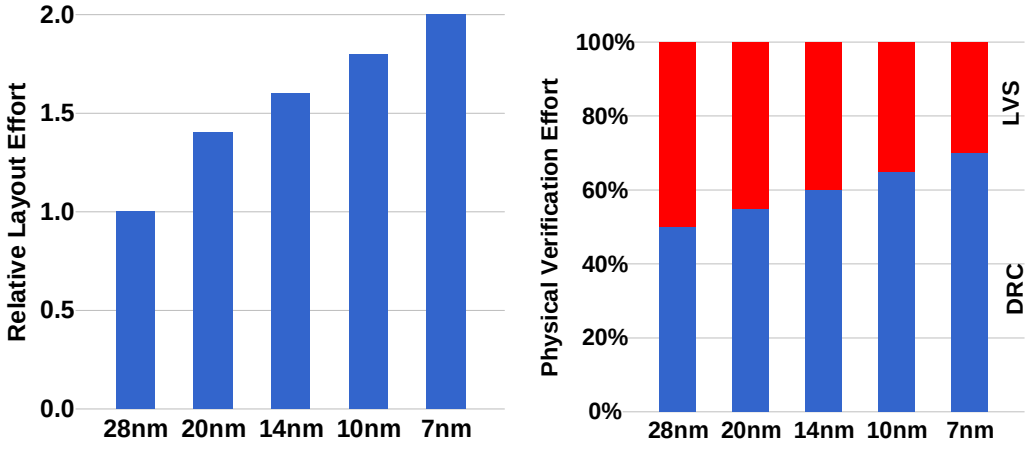


Figure 1.7: Area scaling of analog intensive design and digital intensive designs.

a small portion of the total area.

Among the commonly used passive devices, only metal-oxide-metal (MOM) capacitors could benefit from process scaling due to the increased capacitance density provided by scaled metal pitch. Whereas for the metal-insulator-metal (MIM) capacitors, whose capacitance density is determined by the relatively constant vertical insulator thickness,



(a) (b)

Figure 1.8: Relative layout effort (a) and physical verification effort (b) for different processes [4, 5].

the process scaling does not reduce the area. On the other hand, for ploy-silicon resistors, the sheet resistance barely change across different processes. And the inductor could degrade due to reduced quality factor given more metal fills required by stringent design rules. Therefore, the analog circuit occupies an increasing larger portion of the total chip if the same circuits are used in more advanced processes.

1.1.3 Design cost

Another implication of process scaling is the increasingly more complex design rules, especially the most advanced FinFET processes. On one hand, it is well known that the number of design rules are much larger, and exotic rules are emerged to ensure the circuit performance. Therefore the time needed for the physical design is much longer. As shown in Fig 1.8(a), across different processes, the layout design effort is doubled from 28 nm to 7 nm process. Besides, the circuit electrical characteristics are more sensitive to layout design. Various layout dependent effects (LDE) are emerged, such as stress LDE, gate cut LDE and source drain contact resistance. Therefore, much more time is need to for physical verification. And as the design rule check (DRC) rules become more stringent, more effort is needed to achieve DRC closure, as shown in Fig. 1.8(b), which means more design iterations are inevitable.

However, the increased time delay is not only happened in the physical design stage. The functional design stage also need more time. Circuit designs need device models, and in essence device models are developed by correlating current-voltage combinations.

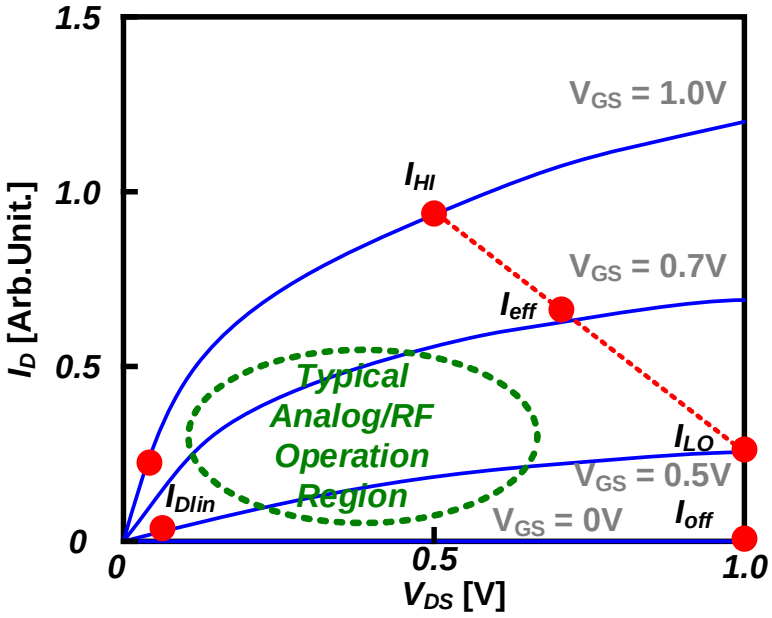


Figure 1.9: Device modeling for digital circuits and analog circuits [4].

While in digital circuits, only a few points around logic low and high are important, the analog circuits need much more information around the transition region, as shown in Fig. 1.9. Unfortunately, the initial device models provided by foundries are usually developed for digital applications, therefore the analog circuit models only have limited accuracy. In older technologies, the analog designer has to have some design iterations to gain more knowledge about the process and have a working design. However, in the most advanced processes, many more masks are needed in the scaled processes, therefore the turnaround time of tape-out is much longer. Inevitably, the time-to-market would be delayed, which will be another huge cost.

1.2 The need for digital-intensive design

Therefore, the digital intensive design has become more and more attractive. First of all, with the digital intensive design, more digital calibrations can be employed to improve the circuit performance. As shown in Fig. 1.10, the analog signal processing is more power efficient in the low-to-medium signal-to-noise ratio (SNR) region, whereas the digital signal process is more attractive in high SNR range. With process scaling, the digital circuits gain more than analog circuits. Therefore, more digital signal processing is an effective way to reduce the overall power consumption.

Besides, by having more signal processing in the digital domain, the digital intensive

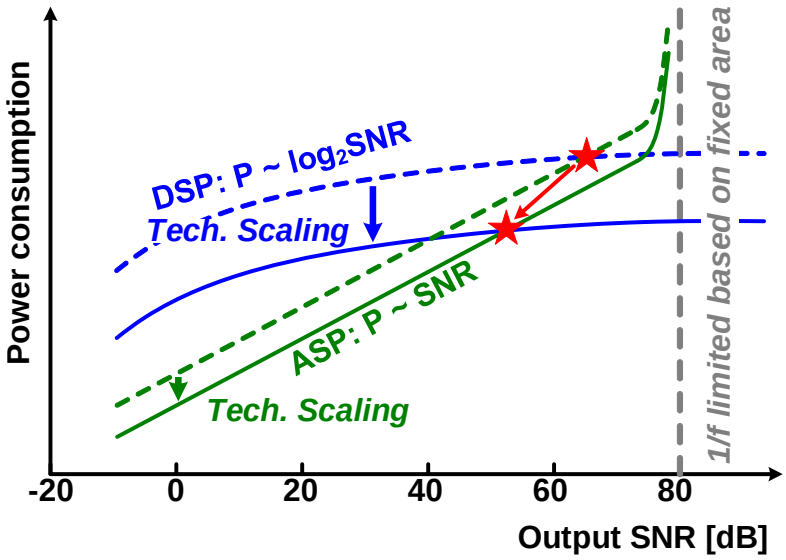


Figure 1.10: Power scaling of analog circuits and digital circuits with process scaling [6].

design can have smaller chip area. As discussed in previous section, the analog circuit area is mainly dominated by passive devices, which barely scales down with process scaling. By minimizing the portion of analog designs, the overall system would scales more like digital circuits.

Last but not the least, by having a digital intensive design, much shorter design time is needed. Both functional design and physical design need more time and effort in the more advanced processes. Worse still, design rules such as DRC rules might need to update to address yield concerns, therefore frequent re-design with updated rules is necessary. To address these issues, there has been a number of proposed layout generators, which can be used to accelerate the physical design [11, 12]. However, such layout generator is not process portable, and dedicated customizations are needed for each specific processes. Besides, the layout generator cannot accelerate the design in the functional design stage.

On the contrary, the digital intensive design try to realize analog function using digital standard cells. By nature, the circuits operate in large signal region, which circumvent the need for accurate analog models. Thus accelerated functional design can be achieved. Besides, by piggybacking the standard digital design flow, the physical design of analog circuits can be much faster. As one additional bonus, the layout of analog circuits have the same density of the synthesized digital logic, therefore tight integration can be achieved, saving significant chip area for density transition.

However, challenges exist in the digital intensive design. In conventional synthesized analog circuits, the analog functions are imitated by digital standard cells, and no ar-

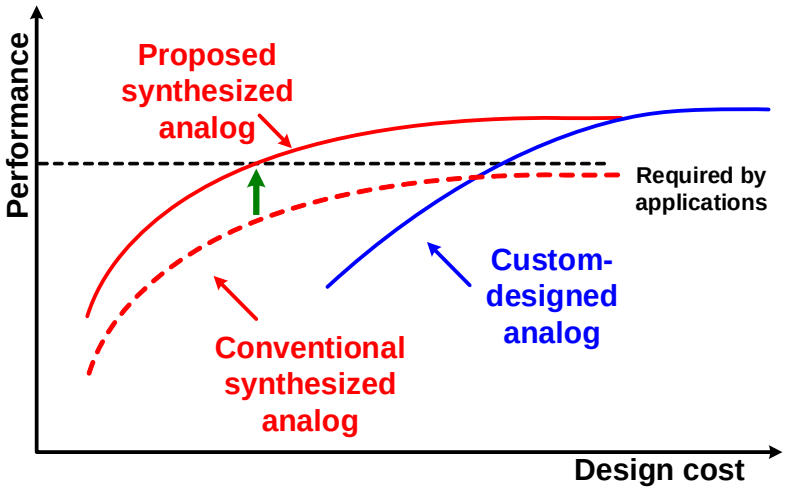


Figure 1.11: Conceptual design cost and performance in analog circuit design.

chitectural or design methodology modifications is applied. With the automated layout synthesis, the P&R randomness will inevitably degrade the performance, rendering it inadequate for analog applications, as shown in Fig. 1.11. Therefore, conventionally the analog circuits are designed with fully customized layout. However, not all the circuit architectures have the same sensitivity to layout randomness. With new circuit architecture that are less sensitive to layout randomness, and the improved design methodology, the performance of synthesized digital-intensive analog designs can be significantly improved. Therefore, the proposed synthesized analog circuit can be applied.

Besides, with increased circuit size and more advanced scaling, the custom-designed analog need much higher design cost to meet certain performance requirements. On the contrary, the impact on the design cost of synthesized analog circuits is much relaxed. Therefore, the advantage in terms of design cost is even higher for synthesized analog circuits.

Moreover, above figure only considered the power consumption of signal processing circuits. Another important design factor of digital-intensive transceiver is the analog-to-digital converters (ADC), which could be the dominant factor in the overall power consumption. Fig. 1.12 shows the power consumption of each conversion step in published ADCs. High sampling rate ADC is extremely power in-efficient, even though great flexibility can be achieved. Therefore, careful system planing and partition is needed to realize a power efficient highly robust digital-intensive design.

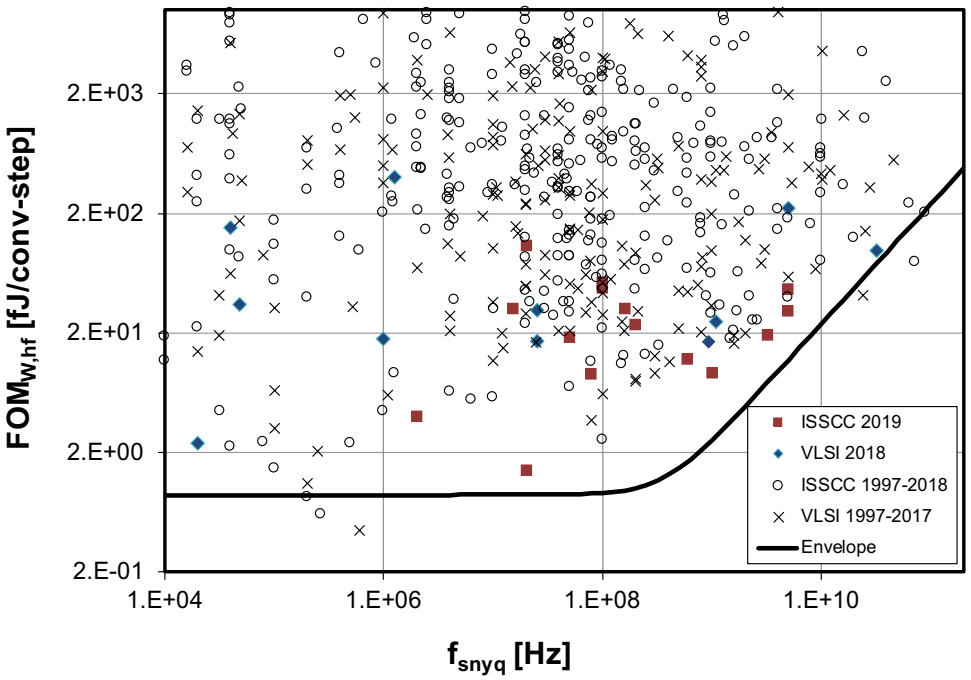


Figure 1.12: Power consumption of ADCs [7].

1.3 Thesis organization

This thesis focus on the realization of low-power wireless transceiver (TRX) with digital intensive architecture. By taking advantage of the improved efficiency of digital circuits, digital intensive designs can achieve higher power efficiency than conventional analog intensive designs. Besides, the area could be smaller, especially considering the process scaling.

The thesis organization is shown in Fig. 1.13. The second chapter reviews the basics of wireless transceiver design, and presents the background of digital intensive TRX.

Chapter 3 presents the design digital intensive frequency synthesizers for wireless transceiver. Fully synthesizable injection-locked phase-locked loops (PLLs) with novel design methodology, circuit topology and system architecture are proposed to meet the stringent requirements of wireless communication. Chapter 4 presents the design a digital intensive TRX for sub-GHz IoT application. Power efficient design achieved with all-digital PLL-based transmitter and digital-intensive receiver. Design considerations are presented, with proposed low power techniques presented to achieve an low power high performance design. Chapter 5 presents a digital intensive transmitter design. Differential duobinary modulator is proposed to realize spectrum mask compliant signal transmission. The modulator realizes a power efficient signal conditioning with co-designed analog/dig-

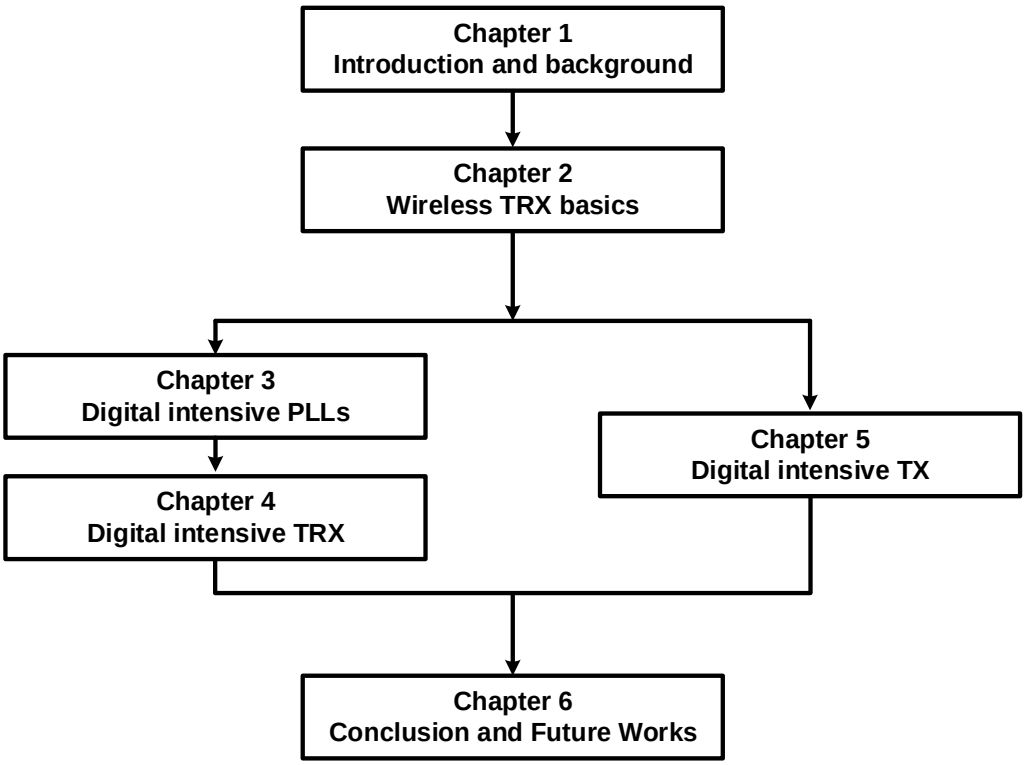


Figure 1.13: Organization of thesis.

ital signal processing, enabling power efficient transceiver design. Chapter 6 concludes the thesis and give a discussion of future works.

Chapter 2

Basics of Low-Power Wireless Transceivers

The transceiver design entails a multitude of aspects, from modulation scheme, transceiver architecture, to circuit implementation. In this chapter, only the concepts pertaining to this thesis will be briefly discussed to give the necessary background information for following chapters.

2.1 Wireless transceiver system architecture

2.1.1 Building blocks

A generic transceiver system diagram is shown in Fig. 2.1. Usually the transceiver is divided into analog/RF frontend, data converters and the digital backend. While the data converters and digital backend also have great impact on the transceiver system, in this section, our discussion will mainly focus to the analog/RF frontend part of the system.

Transmitter

A generic transmitter (TX) is shown in the lower part of Fig. 2.1, which includes digital baseband (DBB), digital-to-analog converter (DAC), analog baseband (ABB), up conversion mixer, and power amplifier (PA). The TX DBB is responsible for signal processing in the digital domain, including modulation, pulse shaping, and filtering. The digital signal is converted to analog signal through DAC, and the TX ABB is used to perform the filtering and gain control to the DAC output. The up conversion mixer translates the signal from direct current (DC) to carrier frequency, and the PA amplifies the signal and interface with matching networks and antenna.

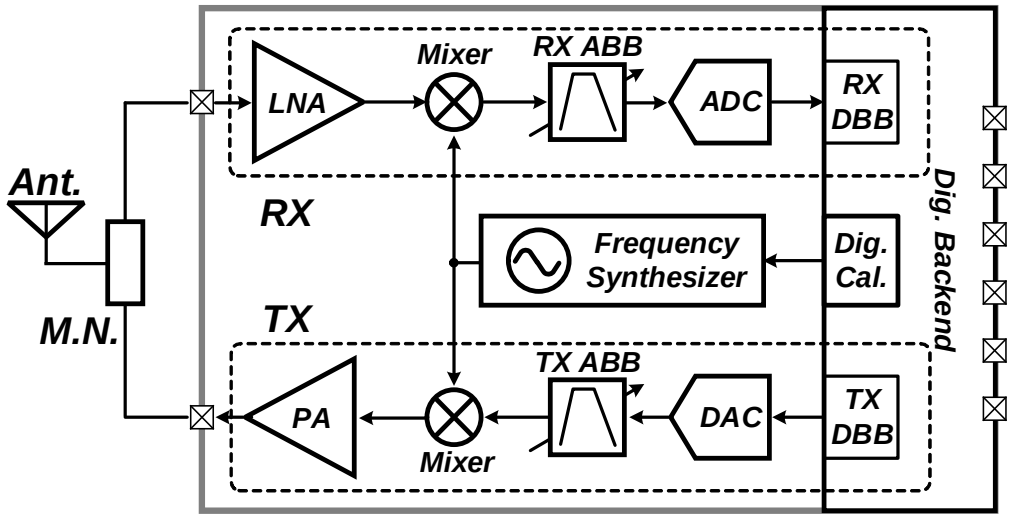


Figure 2.1: System diagram of a generic wireless transceiver.

Receiver

The receiver (RX) system diagram is shown in the upper part of the Fig. 2.1. The function is a reverse of that of TX. Low noise amplifier (LNA) amplifies the received signal from antenna, which is translated to around DC using the down conversion mixer. The analog baseband performs the gain control and filtering, and send to analog-to-digital converter,(ADC). Further filtering, decimation and demodulation is performed in the RX DBB.

Frequency synthesizer

The frequency synthesizer is used to provide an accurate timing information to the system. Multiple frequency synthesizers are employed in a typical wireless transceiver. On the analog/RF side, the frequency synthesizer provides the local oscillation signal to up conversion mixer and down conversion mixer, and defines the carrier frequency. Besides, additional frequency synthesizers are used to provide clock signal to data converters and digital baseband.

2.1.2 System specification

To quantitatively characterize the performance of a wireless transceiver, several system specifications are defined and widely used among circuit designer community. Typically these specifications are stipulated in wireless standards, and all the standard certified designs need to meet those specifications. In the following section, the definition is explained, together with procedures of how it can be measured and calculated.

Sensitivity

Sensitivity quantize the receiver's ability to receive weak signals. The sensitivity is defined as the minimum signal level at which certain bit error rate (BER) or packet error rate (PER) can be achieved. In the measurements, the sensitivity is tested by recording various input signal levels and the corresponding BER. By finding the intercept of the BER curve and the BER requirement, the sensitivity can be found. In a typical wireless transceiver, the baseband modem requires certain signal-to-noise ratio (SNR_{DBB}) to meet the BER requirements. And the sensitivity can be derived with the following equation.

$$Sensitivity = -174 + 10 \cdot \log10(BW) + NF + SNR_{\mathrm{DBB}} \tag{2.1}$$

where the BW is the receiver noise bandwidth in Hz, NF is the RX overall noise figure in dB. The -174 is the thermal noise floor at room temperature, and the unit is dBm/Hz.

Adjacent channel rejection (ACR)

Adjacent channel rejection quantize the receiver's ability to reject strong interference when receiving the weak desired signal. It is defined as the maximum signal power ratio between interference and the desired signal when the RX can still correctly receive the desired signal. In the standards, the ACR is stipulated with a desired signal level defined with respect to the reference sensitivity, frequency offset between interference, and BER condition. In the measurement, an approach similar to the sensitivity measurement is undertaken. With pre-defined desired signal level and frequency offset, the interference signal power is increased until the BER requirement is violated. The ACR is affect by a multitude of factors, including RX frontend linearity, frequency phase noise and blocker type and frequency.

Adjacent channel power ratio (ACPR)

The ACPR quantizes how clean the transmitter output. It is defined as the power ratio between adjacent channel and the transmitting signal. The larger the value, the power spillover to adjacent channel is smaller, and more clean of the transmitter output. In the measurements, ACPR is measured with spectrum analyzer, with the TX modulation and output power set to the conditions defined in the standards. The ACPR is mainly affected by TX nonlinearity and frequency phase noise.

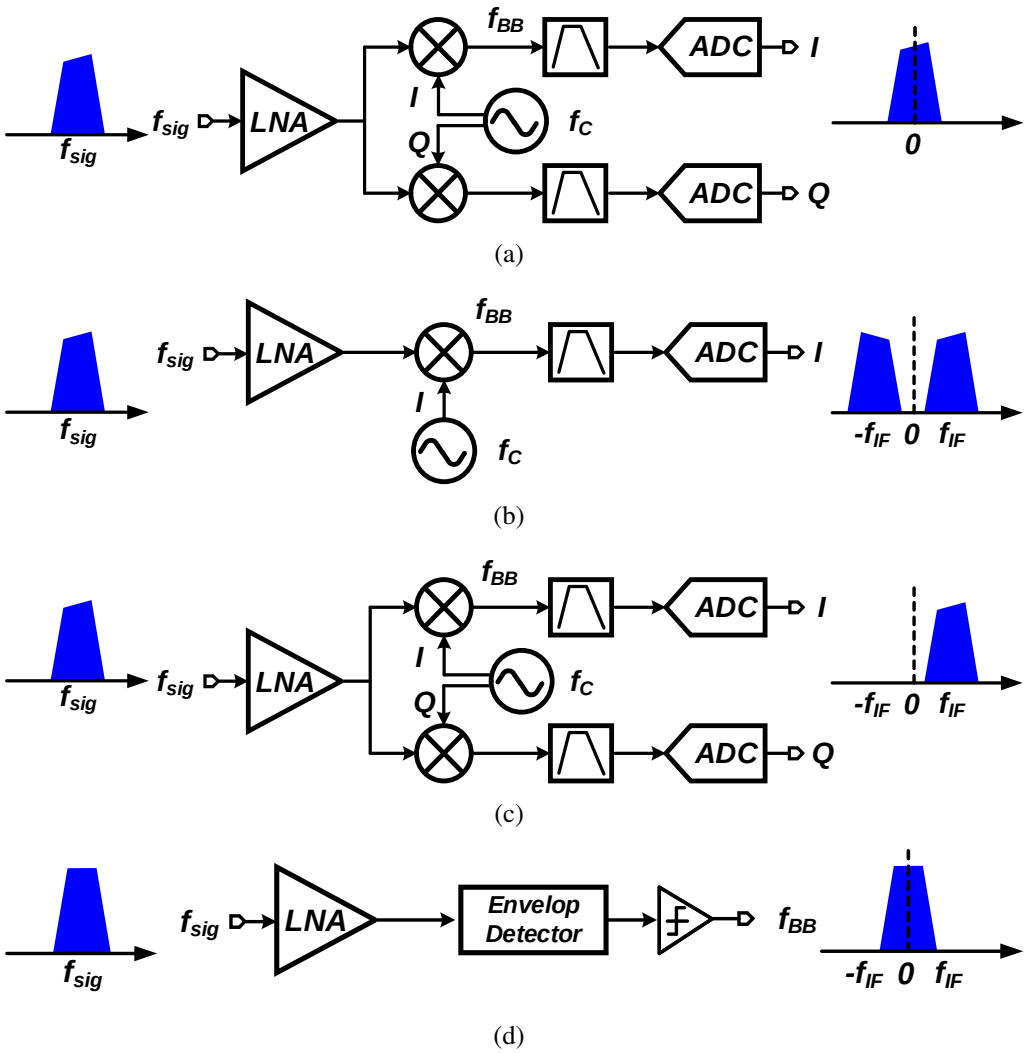


Figure 2.2: Common receiver architectures (a) direct conversion (b) super-heterodyne, (c) low-IF and (d) envelope detector based non-coherent receiver.

2.2 Transceiver architectures

The TRX architecture has a huge impact on the system performance, and thus greatly affect the performance and overall power consumption. In this section, the commonly used receiver and transmitter architectures will be briefly introduced.

2.2.1 Receiver architectures

The RX architectures can be loosely classified into two categories, the coherent receivers and non-coherent receivers. The difference lies in that the coherent receivers require a

precise local oscillation (LO) signal with accurate frequency and phase information.

Direct conversion receiver

The direct conversion receiver is shown in Fig. 2.2(a). In direct conversion receivers, quadrature LO is required, and the LO frequency f_C is equal to the signal frequency f_{sig}. The output is a complex signal, with asymmetrical spectrum. Here the image signal is the desired signal itself, and with quadrature LO, image rejection can be realized in digital domain. Besides, the direct conversion receiver does not require intermediate frequency (IF) filters, which make is suitable for monolithic integration. The direct conversion architecture is the most widely used architecture in current CMOS wireless transceivers, especially for wide-band high data rate systems, such as WiFi and LTE. However, the direct conversion receivers requires two paths of analog baseband filters and ADCs. Also extensive calibrations such as LO IQ phase calibration and DC offset calibration (DCOC) are needed. Besides, because the baseband signal located at DC, it suffers from the flicker noise degradation. Thus it is seldom used in narrow band communication systems, such as GSM and Bluetooth.

Super heterodyne receiver

The super heterodyne receiver architecture is shown in Fig. 2.2(b). The LO carrier frequency f_C is not equal to the signal frequency f_{sig}, and the baseband is located at a non-zero intermediate frequency f_{IF}. In the receiver, only a single phase LO is required, and only one path of analog baseband and ADC are required. The baseband signal spectrum is symmetrical with respect to the DC. However, the super heterodyne suffers from the image, and there is a tradeoff between image rejection and IF frequency. Besides, to coherently detect the signal, a quadrature down conversion is required after the ADC.

Low IF receiver

As a tradeoff between direct conversion architecture and super heterodyne architecture, low-IF receiver is proposed. As shown in Fig. 2.2(c), the low IF RX has the same hardware as of direct conversion architecture, and the output is a complex signal with asymmetrical spectrum with respect to DC. However, a non-zero baseband frequency is used to avoid the flicker noise degradation. Besides, the DCOC is not required as AC coupling can be employed. On the other hand, the low-IF RX has a tradeoff between image rejection and flicker noise contamination. The higher the IF frequency, the flicker noise degradation is lesser, but the higher image rejection ratio is required [13].

Non-coherent RX with envelope detector

Previously receiver architectures are mainly used for coherent receivers. For amplitude modulated signals, such as on-off keying (OOK), a non-coherent envelope detector based receiver can be used, as shown in Fig. 2.2(d). With this architecture, very high power efficiency can be achieved. However, such design suffers from poor blocker rejection, as the RX has little frequency rejection.

2.2.2 Transmitter architectures

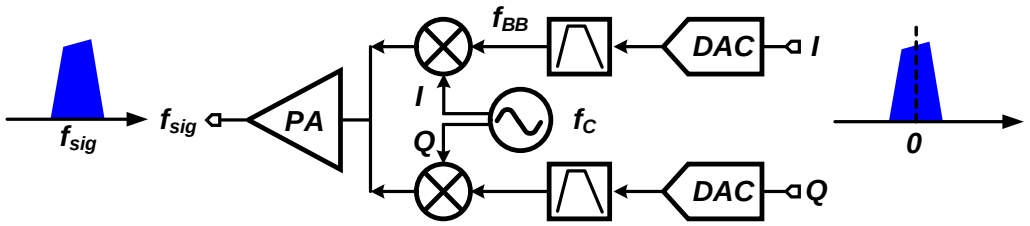
The commonly used transmitter architectures are explained in this section, and the pros and cons of each architectures are briefly discussed.

Cartesian transmitter

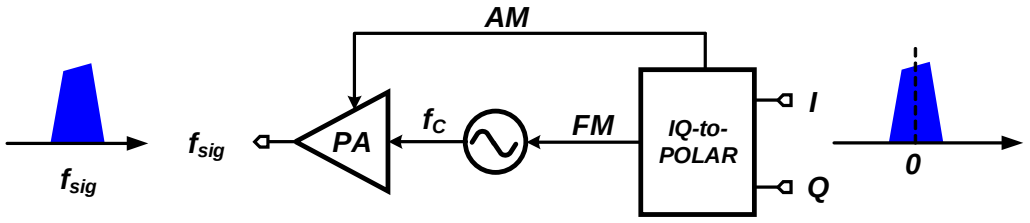
The block diagram of Cartesian transmitter is shown in Fig. 2.3(a). As the most commonly used TX architecture, it can be viewed as the reverse of direct conversion receivers. The TX takes in complex baseband, the output spectrum is asymmetrical with respect to carrier frequency. The Cartesian TX can support wideband communication. However, the transmitter requires DACs and analog reconstruction filters, which makes it analog intensive. The Cartesian transmitter requires relatively large area and has relatively low power efficiency. Besides, it suffers from various non-idealities such as local oscillation feedthrough (LOFT) and PA pulling to the frequency synthesizers.

Polar transmitter

The polar transmitter architecture is shown in Fig. 2.3(b). Here the input IQ signal is converted to magnitude-phase signal in the digital domain. The phase domain signal is differentiated into frequency domain signal, which is used to control a frequency modulator. On the other hand, the magnitude signal is realized by amplitude modulating a power amplifier. Compared to Cartesian architecture, the polar transmitter's output frequency is exactly the same as the PLL output, therefore this polar implementation does not have the PA pulling. Besides, the polar transmitter does not require DACs or analog reconstruction filers, and is friendly to digital implementation. However, the conversion from IQ to polar would significantly expand the signal bandwidth, thus wide bandwidth frequency /phase modulator and amplitude modulator are required [14]. Therefore, the polar TX is mainly used for narrow band communication systems such as GSM and Bluetooth, and very good power efficiency can be achieved with digital intensive implementations.



(a)



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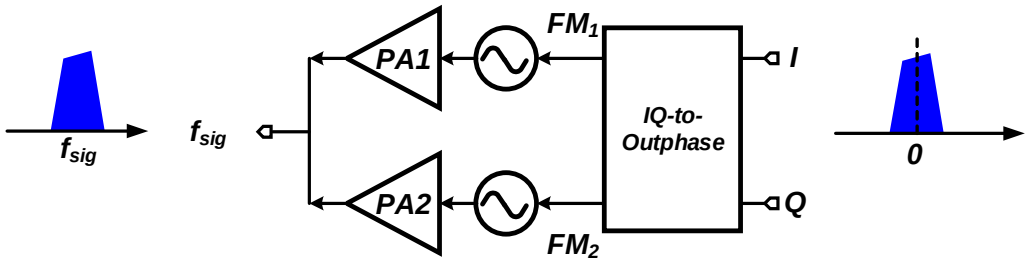
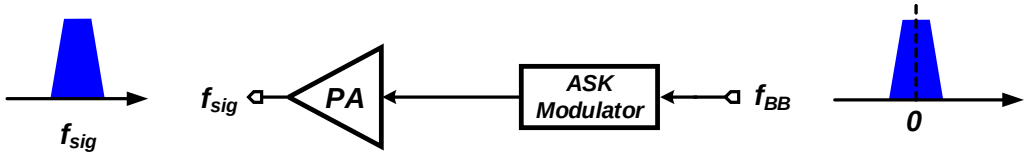


(c)



(d)

Figure 2.3: Common transceivers architectures (a) Cartesian (b) polar, (c) outphasing and (d) amplitude shift keying (ASK) transmitters.

Outphasing transmitter

The outphasing transmitter is shown in Fig. 2.3(c). A digital modulator converts the IQ signal to two constant envelope angular modulated signals. With these two constant envelope signals, variable envelope signals amplification can be realized with nonlinear power amplifiers, thus potentially high power efficiency can be achieved [15]. However, the conversion from IQ to outphasing signals also expands the signal bandwidth, thus high bandwidth is required for frequency modulators.

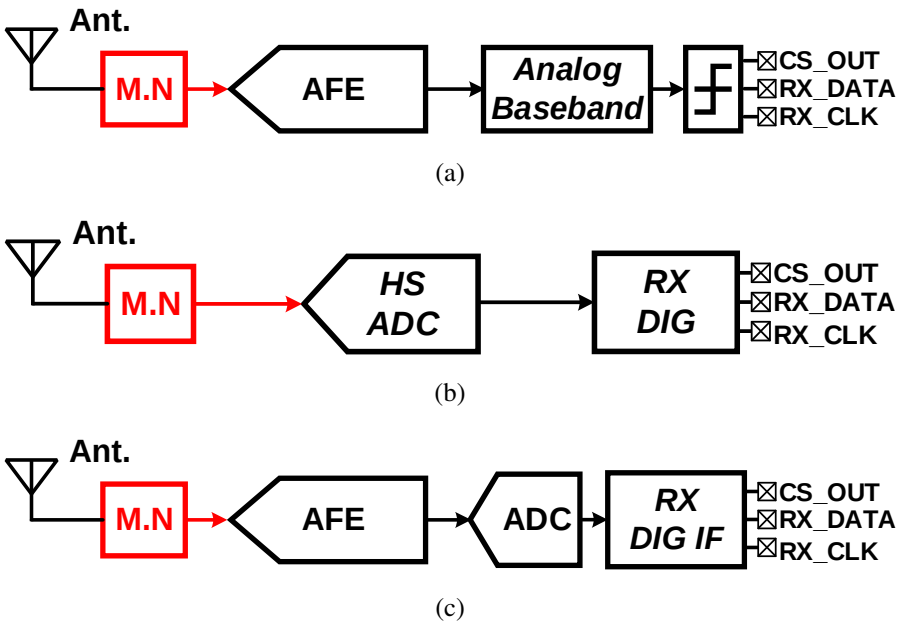


Figure 2.4: Three receiver implementations, (a) analog-intensive receiver, (b) ADC-based digital receiver and (c) digital-intensive receiver.

Amplitude Shift Keying (ASK) transmitter

All the previous transmitters are used for complex modulations with IQ digital input. For simple amplitude modulations, a simple amplitude shift keying TX can be used, as shown in Fig. 2.3(d). Similar to the envelope detector based non-coherent RX, the TX can achieve excellent power efficiency. However, the ASK TX has poor spectrum efficiency, which limit its usage.

2.2.3 Power consumption with different transceiver architectures

The power consumption and design complexity of wireless transceiver highly depend on its implementation, especially how the signal processing is performed. Fig. 2.4 shows the three different receiver architectures, with different partition of analog signal processing and digital signal processing. Fig. 2.4(a) shows the conventional analog-intensive architecture, in which most of the signal processing is in analog domain. On the other hand, the receiver could also have an all-digital architecture, as shown in Fig. 2.4(b), where a high speed ADC is placed after antenna, and all the signal processing is performed in digital domain.

Both the analog-intensive receivers and the all-digital receivers have pros and cons. For analog-intensive receivers, the circuit design requires dedicated optimization for

specific process. And a significant standby power consumption is required to provide the bias current. Therefore, for applications with low data rate, the power efficiency of analog-intensive receiver is relatively poor, as evident from [9]. Besides, the configurability of analog-intensive receiver is limited. Different transceivers are needed for different applications, incurring large design overhead for multi-mode multi-standard wireless transceivers.

On the other hand, the ADC-based all-digital receiver could offer higher flexibility. Theoretically different applications can be supported by re-configure the digital logic. And high power efficiency could be achieved by dynamically re-configure the operation voltage and frequency. However, for low-data rate band-pass wireless applications, the sampling rate required by carrier frequency is much higher than the data rate, which is often in the range of GHz. And to accommodate the strong interferences, high dynamic range is required. Therefore, the ADC would dominate the transceiver power consumption [16], and limit the overall power efficacy.

Therefore, the most power-efficient transceiver implementation is a hybrid of continuous-time analog signal processing and discrete-time digital signal processing, especially on the receiver side, as shown in Fig. 2.4(c). The analog frontend is used to perform signal amplification and down-conversion. After the down-conversion, the signal carrier frequency is significantly reduced, and the data conversion can be performed with much lower power consumption. Most of the signal processing is performance in the digital IF stage, which does not have standby power consumption and promises higher power efficiency than analog baseband. Therefore, the digital-intensive transceiver could be realize a high-flexible design with low power consumption.

2.3 Power analysis of wireless transceivers

The power consumption is a strong function of the used modulation. Transceivers with constant envelope modulation tend to have better power efficiency as high efficiency nonlinear power amplifiers can be used. Besides, transceiver architecture also plays a significant role in the overall power consumption. Conventional wisdom assumes the power amplifier and the receiver chain would be the limiting factor of system power consumption. However, this might not be the case in the low-power IoT applications. In this section, we will present a quantitative analysis of the power consumption of a sub-GHz IoT transceiver. With the analysis, it will direct the power optimization in the next step.

The wireless transceiver under analysis is the SPIRIT1 from STMicroelectronics [9]. On the transmitter side, a PLL-based polar architecture is employed, with amplitude modulation path being a constant. The receiver is implemented as a low-IF architecture. It can

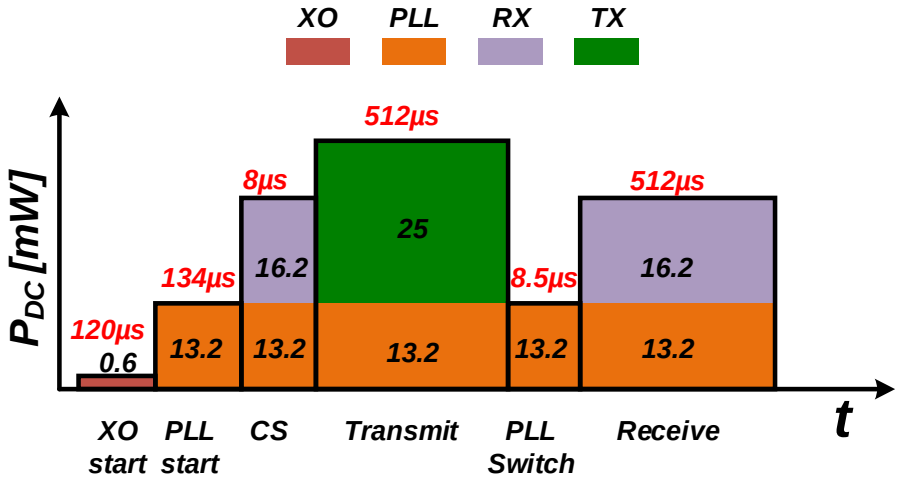


Figure 2.5: Duration and power consumption of each operation mode (not to scale).

support multiple work modes with different modulations and data rates. In this analysis, the modulation is GMSK modulation, and data rate is 500 kbps. The data packet length is 256 bit, and the output power is assumed at 0 dBm. Note in the receive mode, the power consumption is the sum of PLL and receiver circuits, which includes LNA, mixer, analog baseband, ADC and digital baseband. Similarly, the power in the transmit mode is the sum of PLL and transmitter, and in the analysis, we assume the majority of transmitter power consumption is from power amplifier. According to the data sheet 2.1, in the transmit mode with 11 dBm output power, the PLL and transmitter together consume 60 mW. Thus the power amplifier consumes 46.8 mW, and the drain efficiency is around 26.9%. Assume Class-B PA power back off characteristic, the PA drain efficiency at 0 dBm is less than 4%. In this analysis, a PA power consumption of 25 mW is assumed at 0 dBm output power. Therefore, the power consumption and duration of each working mode is summarized in Table 2.1.

The operation time and power consumption of each circuit block is shown in Fig. 2.5. The total power consumption of each operation mode is shown in Fig. 2.6, and the power breakdown of each circuit block is shown in Fig. 2.7. As shown in the figure, while the most power consuming operation modes are transmit and receive, the PLL is the most power consuming circuit block of the system. Therefore, in order to reduce to overall power consumption of the transceiver, not only the PA and receiver chain need to be low power, but also a low power frequency synthesizer is needed.

Table 2.1: Duration and power consumption of each operation mode.

Mode	Duration [μs]	Pdc [mW]
XO start	120	0.6*
PLL start	134	13.2
Carrier sense (CS)	8	29.4
Transmit	512	38.2†
PLL switch	8.5	13.2
Receive	512	29.4

* Average power consumption estimated assuming total XO startup energy of 70 nJ.

† Assume the power consumption in transmit mode is only from PLL and PA, power efficiency at 0 dBm P_{OUT} is estimated from peak power efficiency at 11 dBm and Class-B power back off.

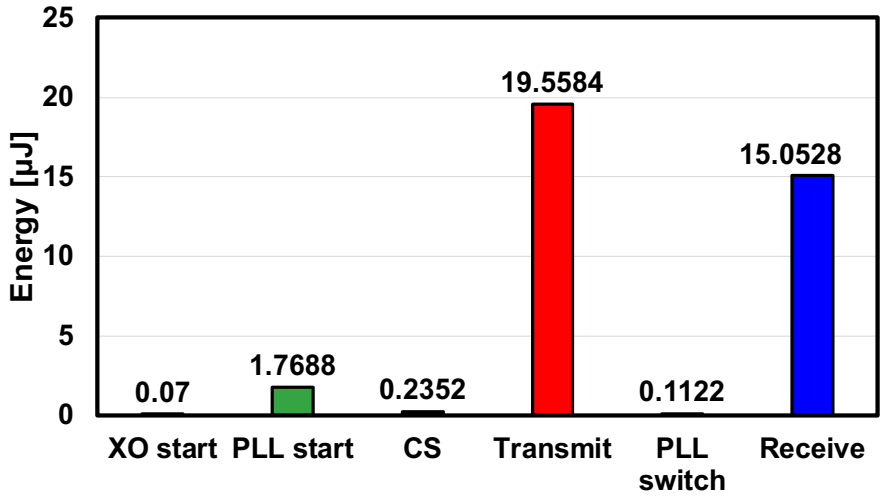


Figure 2.6: Energy dissipated in each operation mode.

2.4 Basic frequency synthesizer

As explained in the previous sections, the frequency synthesizers is an important circuit block in terms of power optimization of the whole wireless transceiver. Besides, frequency synthesizer can be used as frequency modulators, which is an essential block in the

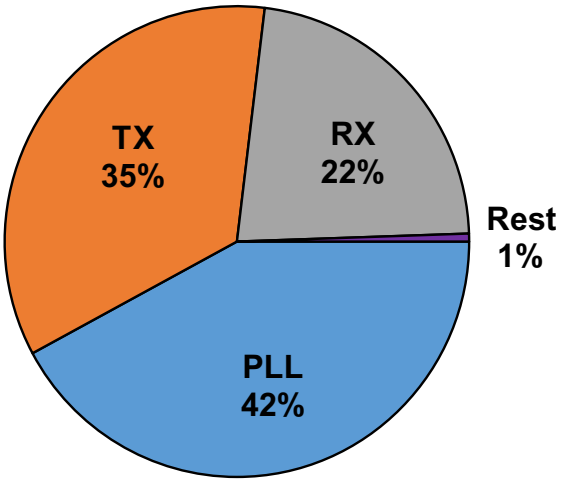


Figure 2.7: Power consumption of each circuit block.

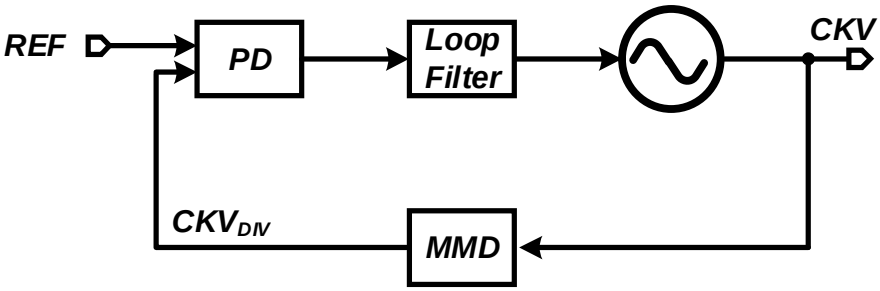


Figure 2.8: System diagram of a generic phase-locked loop.

design of a low power polar transmitter. Therefore the frequency synthesizer basics are covered in this section.

The frequency synthesizer have many different implementations, such as direct digital frequency synthesis (DDFS), direct analog frequency synthesis (DAFS). However, the majority of today's CMOS monolithic frequency synthesizer is based on PLLs. Therefore we will devote this section to the implementation of PLLs.

2.4.1 PLL system diagram

The system diagram of PLL is shown in Fig. 2.8. The input reference signal is compared against the divided feedback signal from multi-modulus divider (MMD) in the phase detector. The phase detector extracts the phase error, and provides a proportional output.

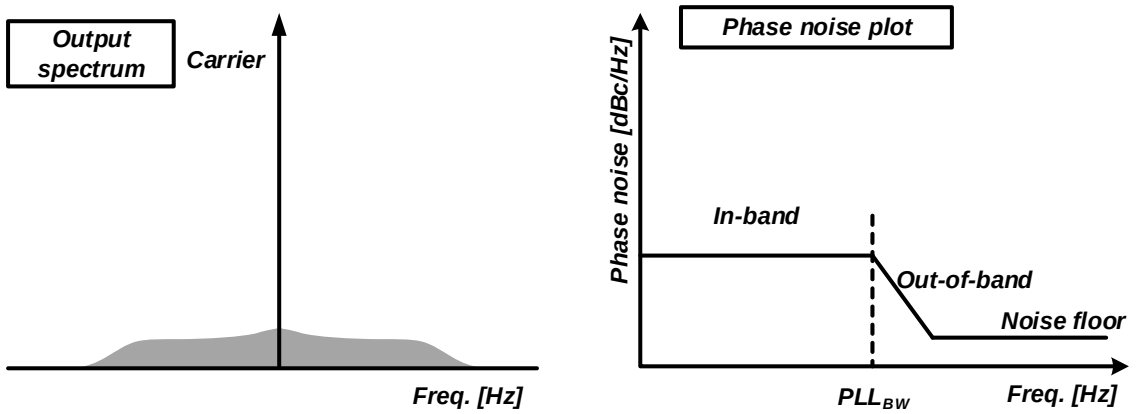


Figure 2.9: PLL output spectrum and phase noise plot.

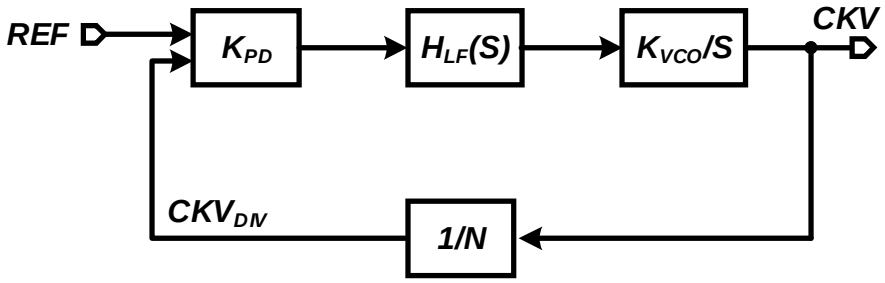


Figure 2.10: PLL noise model.

The loop filter filters the phase detector output, and used to control the oscillator. Both the phase detector and loop filter can be implemented in either analog or digital form. In the analog PLL, the phase detector is implemented with phase frequency detector (PFD) and charge-pump (CP), and the loop filter is implemented with analog passive low-pass filters. On the other hand, the digital PLL utilizes time-to-digital converter (TDC) and quantizes the phase error into digital code, and a digital low-pass filter is used as the loop filter.

A typical PLL output is shown in Fig. 2.9. The output spectrum contains the carrier frequency and noise "skirt" surrounding it. The phase noise plot is shown at the right. The phase noise can be divided into three regions: the flat in-band region, the output-of-band region with a phase noise roll-off, and the noise floor.

The phase noise model of an integer-N PLL is shown in Fig. 3.4(b), and the noise contribution from various sources is shown in Fig. 2.11. The integer-N PLL operates with 50 MHz reference frequency, and the output frequency is 1 GHz. The modelled oscillator noise is -100 dBc/Hz at 1 MHz frequency offset, and the phase detector noise

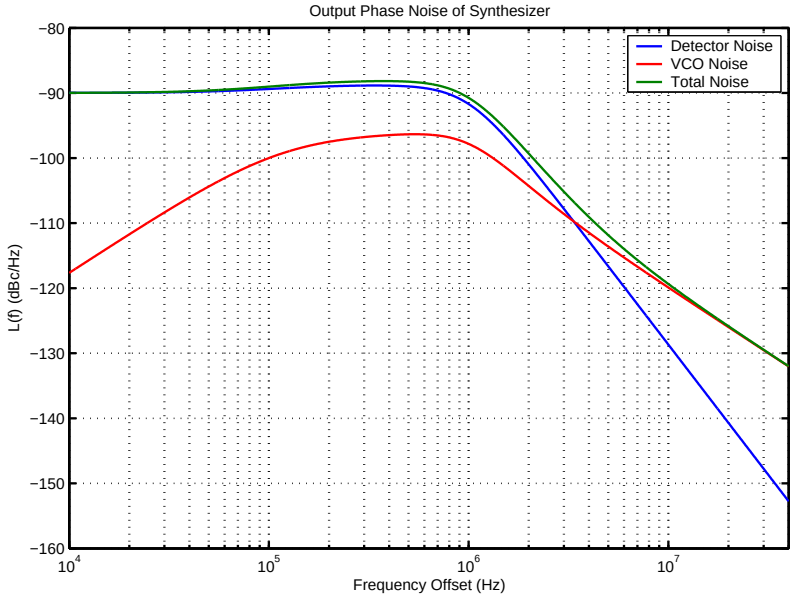


Figure 2.11: Noise contribution of an integer-N PLL.

is -90 dBc/Hz. As evident from the plot, for a well-designed type-II PLL with 1 MHz bandwidth, the in-band noise is dominated by the phase detector, and the output phase noise is dominated by the oscillator. Therefore, both the oscillator and phase detector need to be designed with low noise.

2.4.2 Oscillators

As evident from previous analysis, the oscillators determines the PLL out-of-band phase noise, and directs the design of PLL bandwidth. Besides, the oscillators operates at the highest frequency of the PLL, and often are the most power hungry circuit block in a PLL. Therefore, significant efforts have been made to its design and optimization. Generally speaking, the oscillator can be separated into two categories: the LC oscillator which is realized with inductor capacitor (LC) resonator bank, and the ring oscillators which has no magnetic components, as shown in Fig. 2.12.

Because of the frequency selectivity of LC resonators, the LC oscillators has better phase noise, and consumes less power for the same phase noise performance. However, the inductors occupy large chip area, and the size barely shrinks with process scaling. Therefore, the LC oscillators are unattractive in advanced technologies, and are reserved for applications where extremely low phase noise is needed. On the other hand, the ring oscillators can be implemented with transistors, resistors and capacitors, thus much smaller area is needed. However, they suffer from poor phase noise, and overall power-noise

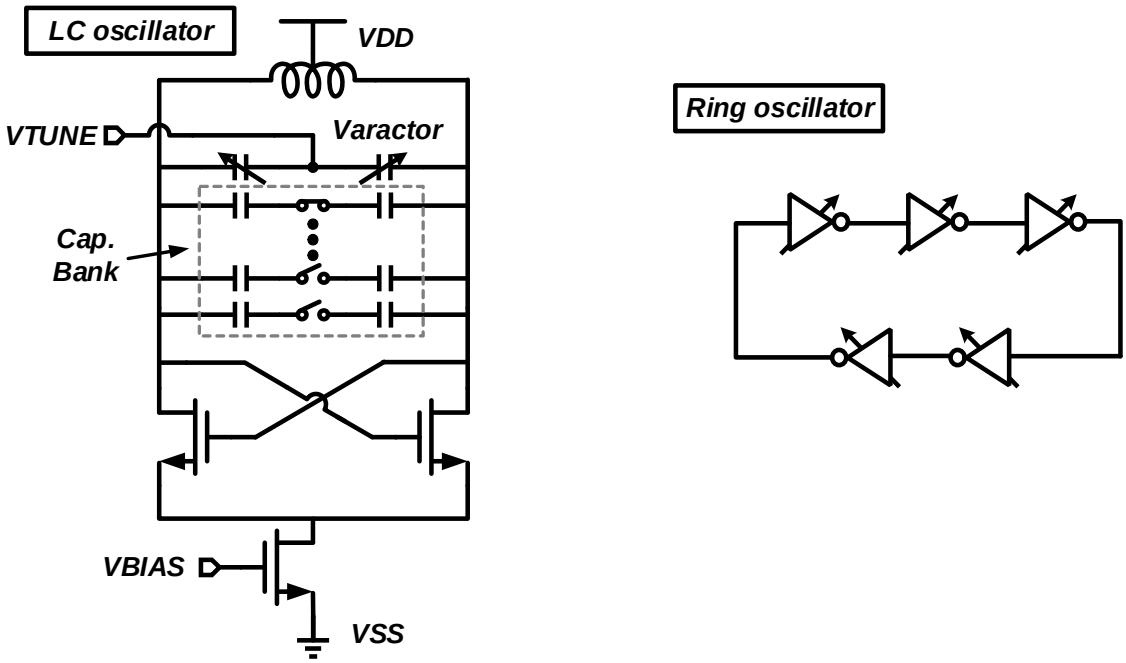


Figure 2.12: Circuit implementations of LC oscillator and ring oscillator.

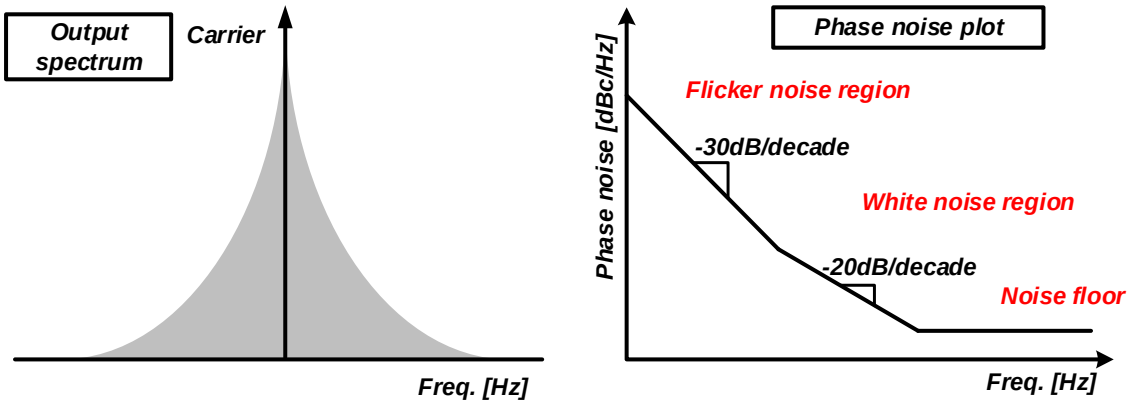


Figure 2.13: Output spectrum and phase noise plot of oscillator.

FoM is lower compared to LC oscillators [17].

The typical output spectrum and phase noise of oscillators are shown in Fig. 2.13. In the phase noise plot, there are three regions: the flicker noise region caused by up-converted flicker noise, which has a -30 dB/decade roll-off; the thermal noise region caused by up-converted white noise, which has a -20 dB/decade roll-off; and the noise floor which is caused by white noise. Both LC oscillators and ring oscillators have similar phase noise profile, and the difference lies in the exact numbers.

Aside from the noise performance, the tuning characteristic of oscillator also merit-

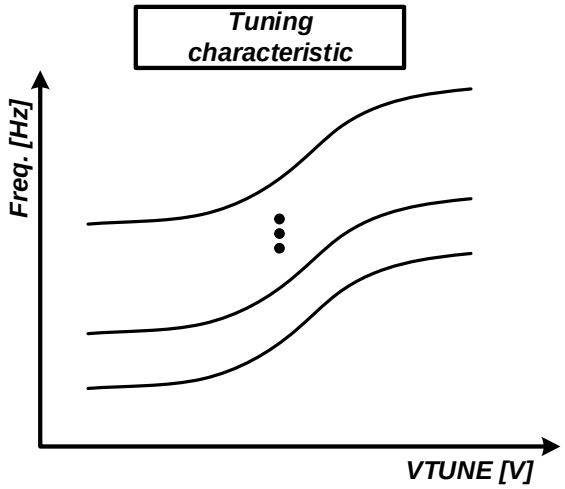


Figure 2.14: Tuning characteristics of oscillator.

s examination, as has an impact on PLL design. Depending on how the tuning signal is applied, the oscillator can be either tuning in analog way or digital way. The analog tuned oscillator can be a voltage controlled oscillator (VCO), or a current controlled oscillator (CCO), while the digital tuned oscillator generally referred as digital controlled oscillator (DCO). To reduce the noise sensitivity, the oscillator tuning sensitivity Kvco is limited, and a segmented bank is used, as shown in Fig. 2.14. The tuning characteristic affect the dynamic behaviors of the PLL, such as the frequency settling speed and cycle slip, thus sufficient overlap between tuning curves is needed.

2.4.3 Phase detector

The phase detector noise affect the PLL in-band phase noise, thus a low noise design is essential for a high performance PLL.

In the analog PLLs, the phase detector is realized with a PFD /CP cascade, as shown in Fig. 2.15. The PFD input is the input reference and feedback divided PLL output, and the output is a train of pulse width modulated signal whose pulse width is proportional to phase difference. The charge pump takes in the PFD output, and output the current with proportional duration, i.e. charge. On the other hand, TDC is used in digital PLLs, and the output is digital code that is proportional to the input phase difference. Due to the analog pulse-width modulation nature, the analog PFD /CP can provide excellent resolution with large dynamic range. However, the analog implementation makes it susceptible to analog non-idealities, and unfriendly to process scaling. Besides, the analog output provide little configurability.

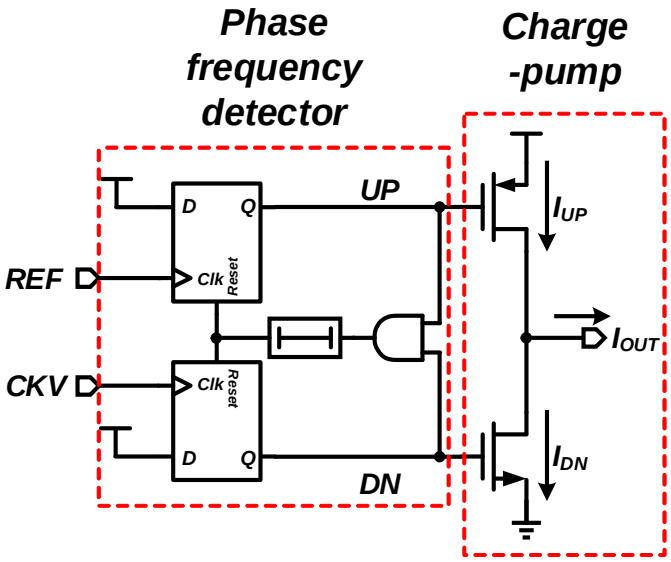


Figure 2.15: Circuit implementation of PFD/CP.

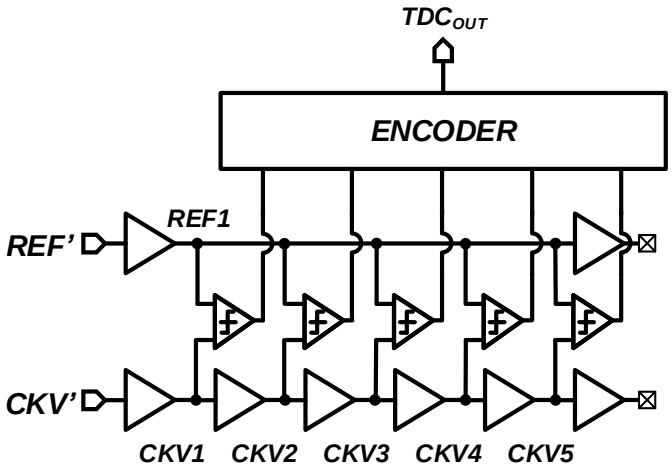


Figure 2.16: Circuit implementation of a flash TDC.

On the other hand, TDC can be implemented with simple digital gates, as shown in Fig. 2.16, which makes it popular in scaled processes, especially those where there is no accurate analog models. Besides, the digital output makes the digital loop filter possible, and high configurability can be achieved in digital domain.

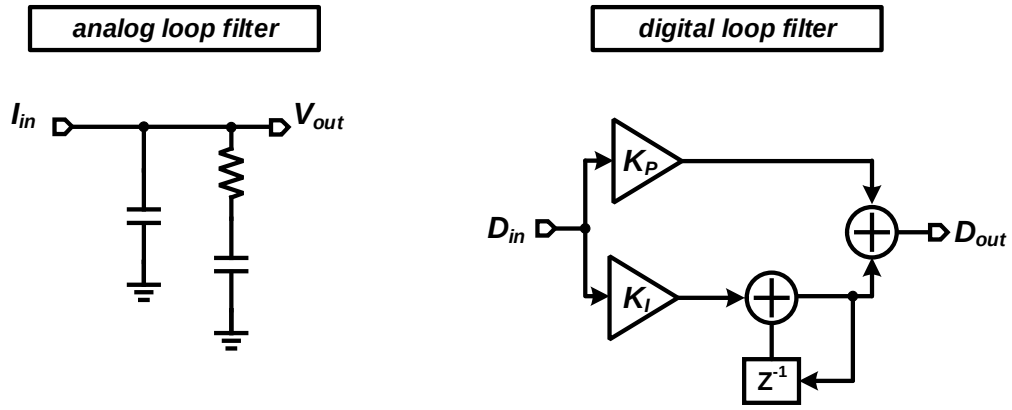


Figure 2.17: Circuit implementation of analog loop filter and digital loop filter.

2.4.4 Loop filter

The loop filters are basically low pass filters which only output low frequency components of the input and attenuates the rest. Depending on the output of phase detector, either analog loop filter (ALF) or digital loop filter (DLF) is possible, as shown in Fig. 2.17. The analog loop filters are usually implemented with passive devices such as ploy resistors and capacitors. Due to the low cutoff frequency required, large capacitors might needed, resulting in large chip area. On the other hand, the digital loop filters can be very compact with synthesized digital logic, and can be easily re-configured to meet different bandwidth and attenuation requirements. One possible disadvantage is that the digital logic introduce extra latencies to the loop, which could potentially degrade the PLL stability.

2.4.5 PLL specifications

The PLL affects the transceiver performance in a number of ways. In this section, the PLL effect will be studied quantitatively, and the required performance of PLL will be derived.

On the receiver side, the phase noise affect the blocker rejection performance. The blocker signal can be mixed with the phase noise and down converted to the baseband. To quantize this effect, the blocker noise figure (BNF) can be used, with all the other components assumed to be ideal.

$$BNF = P_{\mathrm{BLK}} + PN - (-174) \tag{2.2}$$

where the P_{BLK} is the blocker power, PN is the phase noise at the blocker frequency offset. For example, with -48 dBm blocker signal power, and -100 dBc/Hz phase noise, the BNF is 26 dB, which means the reciprocal mixing alone would raise the noise floor by 26 dB.

Therefore, the frequency synthesizer phase noise need to minimize to reduce the impact of blocker signals.

On the TX sides, the phase noise of frequency synthesizer degrades the ACRP performance. For phase/frequency modulated signals such as Gaussian Minimum Shift Keying (GMSK), the phase noise for a certain ACPR can be calculated with the following equation,

$$PN = ACPR - 10 \cdot \log10(BW) \tag{2.3}$$

where the BW is the signal bandwidth. For example, with -40 dBc ACPR, and 1 MHz BW, the required PN need to be less than -100 dBc/Hz.

Besides, the integrated in-band phase noise affects signal error vector magnitude (EVM), which has a significant effect for high performance wireless communication systems such as 5G. From the required EVM, and PN can be estimated by

$$PN = EVM - 10 \cdot \log10(BW) - 3 \tag{2.4}$$

where the 3 dB accounts the phase noise of both TX and RX. For example, if the required EVM is less than -40 dBc, and BW is 100 MHz, the required in-band phase noise is lower than -123 dBc/Hz.

2.5 Design of advanced fractional-N PLLs

As discussed in the previous section, PLL greatly affects the system performance of wireless transceivers, thus significant design efforts are required. Besides, in many wireless standards, fine frequency resolution is required to realize small channel spacing or frequency modulation. Therefore, fractional-N PLL is a must, and will be investigated in this section.

2.5.1 Analog charge-pump fractional-N PLL

Fig. 2.18 shows the system diagram of an analog implementation of fractional-N PLLs. The fractional-N operation is realized with the delta-sigma modulator (DSM) controlled MMD. The DSM provides a digital sequence whose average value is equal to the input, while the quantization error is shaped to high frequency. Therefore, the MMD output's average frequency is equal to the reference signal, while the instantaneous phase error at phase detector input is proportional to the DSM quantization noise. This high-pass

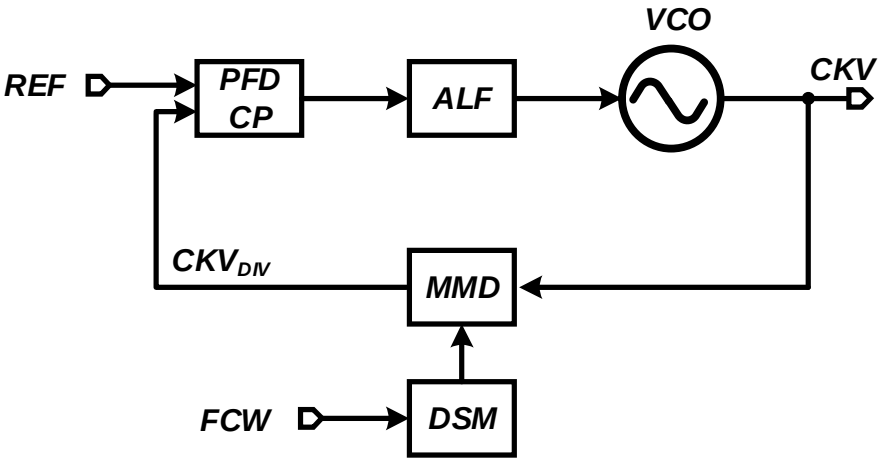


Figure 2.18: Circuit implementation of analog fractional-N PLL.

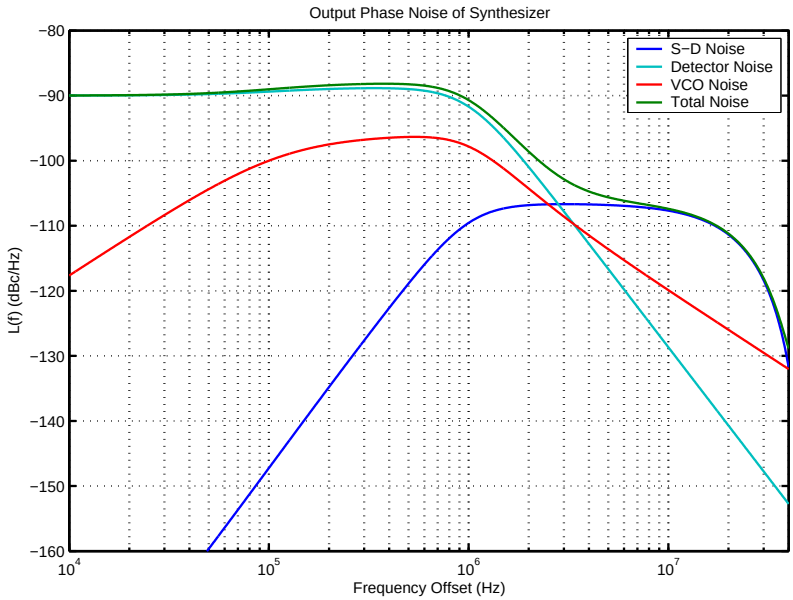


Figure 2.19: Noise contribution of digital fractional-N PLL.

DSM quantization noise is filtered by the loop filter, whereas only the average phase error remained.

The phase noise plot of a fractional-N analog charge-pump PLL is shown in Fig. 2.19. The reference frequency is 50 MHz, output frequency is 1 GHz, and the PLL bandwidth is 1 MHz. The modelled oscillator has -100 dBc/Hz phase noise at 1 MHz, and the phase detector's noise is -90 dBc/Hz. As evident form the noise plot, the in-band phase noise is dominated by phase detector, which is same as integer-N PLL. However, the out-of-band noise is dominated by the DSM quantization noise. Thus in conventional analog CP

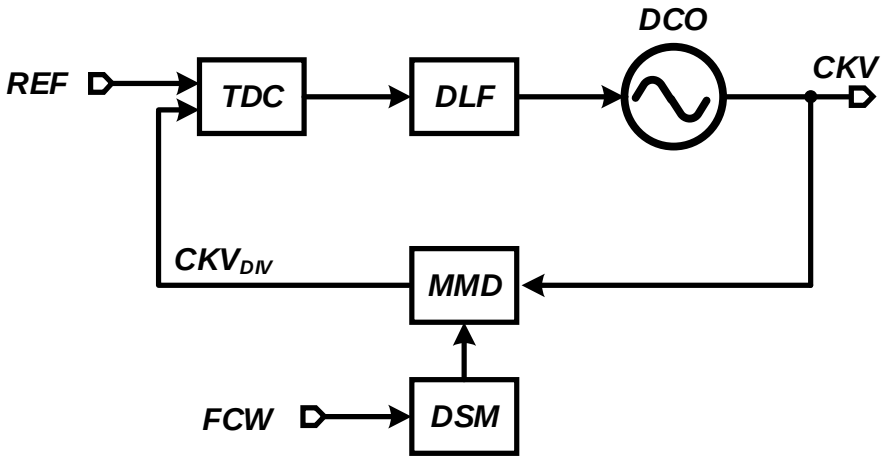


Figure 2.20: Circuit implementation of digial fractional-N PLL.

fractional-N PLLs, narrow PLL bandwidth is used to sufficiently suppress the quantization noise. However, the narrow PLL bandwidth limits the suppression of oscillator phase noise. Therefore, a design tradeoff between different noise sources is needed.

Besides, the charge-pump noise is proportional to the turn on time. With DSM, the phase detector noise will be proportional to the DSM quantization noise, which is decided by the DSM order. For example, the quantization noise range is one oscillator period for 1st DSM, 3 oscillator periods for 2nd DSM, and 7 oscillator periods for 3rd DSM. Therefore, the higher order DSM will cause larger phase detector noise. Besides, high order DSM is desired to reduce the in-band fractional spurs caused by control sequence periodicity. On the other hand, the DSM quantization noise will fold to in-band if the PFD /CP have nonlinearity, which will create fractional spurs in the PLL output. Thus, the DSM quantization noise poses a big challenge to the low jitter high performance PLL design.

2.5.2 Digital fractional-N PLL

A digital implementation of the fractional-N PLL is also possible, with the phase detector realized with TDC, and loop filter realized as digital filters, as shown in Fig. 2.20. However, the same argument about the DSM and phase detector holds in digital PLLs as well. On one hand, the TDC in this design need to cover a significant wider range to cover the integrated deterministic phase errors. On the other hand, fine resolution is required to ensure the in-band phase noise is sufficiently low, and high linearity is required to ensure minimal noise folding and in-band fractional-N spur. Thus a high performance TDC is required, which could incur significant power and area consumption.

2.5.3 Noise cancelling fractional-N PLL

To reduce the extra design difficulties caused by DSM quantization, several techniques has been proposed. The fundamental cause of the DSM quantization noise is the limited resolution of the MMD on the feedback path. In conventional MMDs, the resolution is limited by one oscillator period, which caused large quantization noise at MMD output. Therefore, if finer delay resolution can be achieved, the quantization noise will be smaller, and the noise and bandwidth can be improved. Under ideal conditions, if a delay line with infinite resolution can be achieved, the phase detector would only see the thermal noise.

Notice that the frequency control word is already available in the digital domain, and the MMD control code is also a know value, thus the required delay to cancel the DSM quantization can be easily calculated. In Fig. 2.21(a), the quantization noise can be accumulated and use as the control code to a digital-to-time converter (DTC) to cancel out the DSM quantization noise [8]. The accumulation is used because the MMD works in phase domain, and the FCW and the quantization error are frequency domain variables. To match the DTC gain and MMD, a least mean square (LMS)-based gain calibration can be employed. The LMS calibration logic takes in the TDC output and DTC control code, and accumulate the correlation results of the two variable and use as the gain value. After the gain calibration settle, the correlation of TDC output and DTC control code is of zero mean, indicating the DTC gain error does not contribute to the phase error detected by the TDC. Therefore the DTC gain can be assumed to be correct.

Equivalently, the DTC can also placed on the reference path, albeit with an opposite polarity. By introducing a time varying delay to the reference signal, the REF' will align to the MMD output. Compared to the feedback path cancellation, the noise contribution is the same. However, this arrangement is more suitable to fractional-N injection-locked PLLs [18] [19] or sub-sampling PLLs [20], where a perfect alignment of reference signal edge and oscillator edge is required.

Previous noise cancellation schemes deal with quantization noise at phase detector input. Noise cancellation at phase detector output is also possible, as shown in Fig. 2.21(c). The cancellation block directly cancels the component caused by quantization noise. All the calibration happens in digital domain [21], while an analog implementation is also possible [22]. However, in this arrangement a highly linear large dynamic range TDC is required, which is much more complex and power consuming than DTCs. Therefore, this arrangement is not as attractive from the perspective of power consumption.

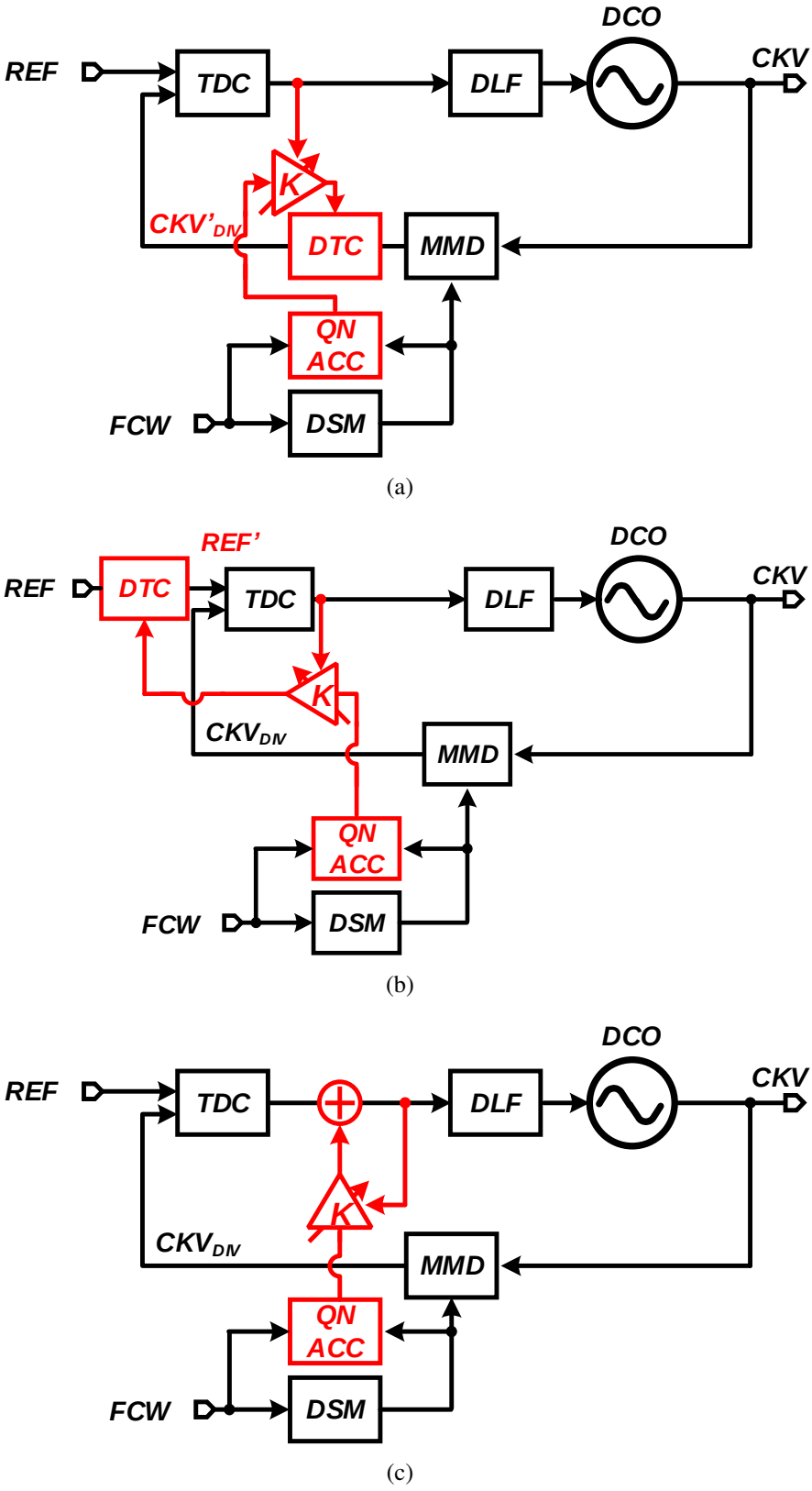


Figure 2.21: Implementations of noise cancelling fractional-N PLL, with cancellation at (a) feedback path, (b) reference path and (c) TDC output.

Chapter 3

Fully-Synthesizable Digital-Intensive Frequency Synthesizer

As one the most important building blocks of a wireless transceiver, the frequency synthesizer has significant impact on the transceiver performance and power consumption, as discussed in the previous chapter. Therefore, the frequency synthesizers, specifically PLLs have been a heated topic, and numerous papers have been devoted to this area. Among those published PLLs, the digital intensive PLLs, or all-digital PLLs have attracted a lot of attentions since its introduction [23]. Compared to conventional analog PLLs, the digital-intensive PLLs promises higher re-configurability, smaller area, and is more amenable to to process scaling. While taking advantage of digital circuits in scaled CMOS technology, digital-intensive or all-digital PLL designs still cannot be implemented with standard digital design flow.

This chapter investigates the design of digital intensive synthesizable PLLs. In the synthesizable PLLs, all circuit building blocks are implemented in all-digital architecture and expressed in a hardware description language, which can then be synthesized from commercial standard-cell libraries and is compatible to standard digital design flow. Compared to conventional pure analog or digital-intensive analog implementations, the digital-intensive synthesizable PPLs can significantly shorten the design time and cost. Besides, the fully synthesizable PLLs can be better integrated with digital systems. Functions such as calibration logic, built-in-self-test (BIST), and boundary scan can be readily integrated in order to monitor the internal circuit state, which is very helpful in circuit design and de-bugging.

While a number of fully synthesizable PLLs have been reported recently [24–27] there is still considerable room for improvement in terms of power consumption and chip area. Moreover, a considerable amount of custom-designed cells are required in previous syn-

thesizable PLLs, which introduce additional design and place-and-route (P&R) procedures [25, 26, 28]. These additional design procedures lead to a performance degradation in terms of portability, integration, and scalability.

In order to address the aforementioned issues, this chapter presents two fully synthesizable PLLs, which do not use any custom design, but are purely designed using a foundry-provided standard-cell library by a standard digital design flow. In order to mitigate the mismatches and variations of fully synthesizable designs, a holistic optimization of system design, circuit topology, and implementation flow is adopted.

The remainder of this chapter is organized as follows. Section 3.1 explains the digital compatible design process of synthesizable PLLs with illustrative design examples. Section 3.2 describes the overall architecture of the PLL and relevant considerations. Section 3.3 presents a synthesizable injection-locked PLL (IL-PLL) with self-clocked nonoverlap update and a slope-balanced sub-sampling bang-bang phase detector (SS-BBPB). Section 3.4 presents a fully synthesizable fractional-N IL-PLL with synthesizable DTC and extensive digital backgrounds. Finally, the chapter is summarized in Section 3.5.

3.1 Design process

3.1.1 Digital-compatible design flow

Fig. 3.1 shows the design flow of a fully synthesizable PLL. Analog building blocks, such as DCOs and phase detectors are designed with standard cells and are described in gate-level hardware description language (HDL). The digital control logic, such as loop filters and calibration blocks, are described in register-transfer level (RTL) HDL and are mapped to a gate-level netlist using digital synthesis tools. The netlists from the two parts are combined and converted to layout using automated layout synthesis. When migration to a new process is needed, only the analog circuits need to be redesigned by replacing standard cells with appropriate timing characteristics, whereas the digital logics can be readily re-synthesized. Thus, the design migration is significantly accelerated. In order to mitigate the mismatches and variations caused by automatic synthesis, techniques such as relative placement can be used. With such design constraints, reasonably good performance can be expected. Moreover, these design constraints are process independent and can be readily used across different processes.

One interesting specification that merits examination is the total time used for this design. Here, the design time of both a conventional analog PLL and the proposed synthesizable PLL are summarized in Table 3.1. Compared to a conventional analog PLL, the synthesizable PLL enables faster circuit design for a new process, since only re-sizing

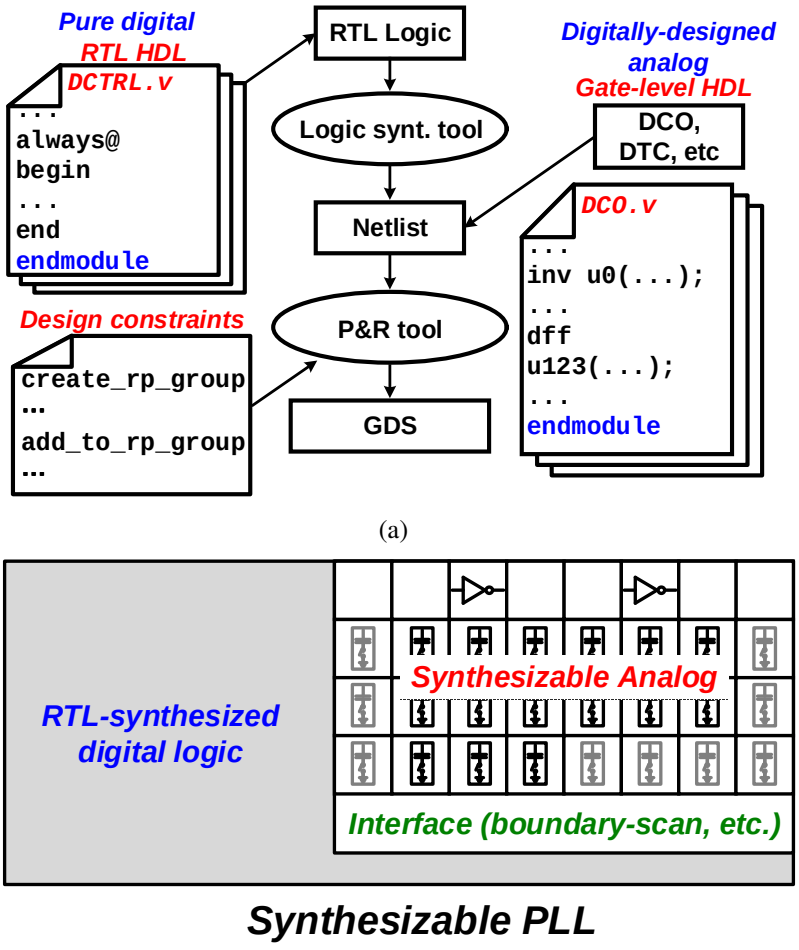


Figure 3.1: Design of a fully-synthesizable PLL, (a) digital compatible design process, (b) layout with constraint-directed auto P&R.

standard cells is required. In addition, the layout design is greatly accelerated, as automatic P&R can be used to eliminate the burden of re-learning complex DRC rules, especially for advanced technologies. Although the two PLL have different architectures, comparable performance was designed to guarantee a fair comparison. And the significantly shorter design time validated the advantages of proposed synthesizable design approach.

3.1.2 HDL-based circuit design

As a demonstration, the implementation of a bang-bang phase detector (BBPD)-based PLL is designed, and example codes of the loop filter and DCO are shown. Code listing 3.1 shows a DLF for a PLL with a BBPD. The DLF accepts the binary output from

Table 3.1: Design Times of the Synthesizable Phase-locked Loop and the Conventional Analog Phase-locked Loop.

	Analog PLL	Synthesizable PLL
System level design	~hours	~hours
Block design*	~months	~weeks
Layout design*	~months	~hours

* for a new process.

the BBPD, and the output is used to control the DCO. Due to the digital implementation, the DLF has a compact area and can be easily re-configured to realize different transfer functions. The DLF used in this design has two paths: the proportional path and the integral path. The outputs of the two paths are combined in a digital domain. The RTL Verilog code implementation of the DLF is shown in Code listing 3.1.

Listing 3.1: Verilog code of digital loopfilter

```
//DLF.V
module DLF (CLK, PD, Dout, RSTB);
    parameter   beta = 6;
    parameter   alpha = 4;
    input                       CLK, PD, RSTB;
    output      [4:0]           Dout;
    reg         signed [30:0]   integ;
    wire        signed [30:0]   Dout_temp, i_path, p_path;
//
    assign      i_path = integ <<< alpha;
    assign      p_path = {{10{PD}}} <<< beta;
    assign      Dout_temp = i_path + p_path+31?00100000;
    assign      Dout = Dout_temp[20:16];
//
    always @( posedge CLK ) begin
        if (!RSTB) begin
            integ <= 0;
        end
        else begin
            if (DIN == 0) begin
                integ <= integ - {{20{1'b0}}, {10?3FF}};
```

```
            end
            else begin
                    integ <= integ + {{20{1'b0}}, {10?3FF}};
            end
        end
    end
endmodule
```

As one of the most important blocks of a PLL, the DCO determines the out-of-band phase noise, and directs the PLL design. Code listing 3.2 shows a multi-stage inverter-based ring oscillator with NAND2-based digital varactors. Due to this standard-cell-only implementation, the design can be easily ported to other processes. The DCO is described in gate-level Verilog, and the netlist is shown in Code listing 3.2. In order to reduce the mismatches and variations of automatic P&R, design constraints such as relative placement can be applied, as shown in Code listing 3.3. Note that such design constraints are independent of technology niceties, and can be readily re-used across different processes.

Listing 3.2: Verilog code of the digitally controlled oscillator

```
//DCO_BBPLL.V
module DCO_BBPLL (DCO_out, Din_dec);
    input       [30:0]  Din_dec;
    output              DCO_out;
//
    NAND2X6BA10TR I47 (  .VDD(VDD), .VSS(VSS),
        .B(Din_dec[18]), .Y(net596), .A(FINE3));
    NAND2X6BA10TR I46 (  .VDD(VDD), .VSS(VSS),
        .B(Din_dec[19]), .Y(net597), .A(FINE4));

    ...

    INVX3BA10TR I1 (  .VDD(VDD), .VSS(VSS), .Y(FINE2),
        .A(FINE1));
    INVX3BA10TR I0 (  .VDD(VDD), .VSS(VSS), .Y(FINE1),
        .A(DCO_IN));

endmodule
```

Listing 3.3: Digitally controlled oscillator relative placement commands

```
create_rp_group DCO_RP -column M -row N

add_to_rp_group DCO_BBPLL::DCO_RP -column C1 -row R1
                 -leaf DCO_BBPLL/I0
add_to_rp_group DCO_BBPLL::DCO_RP -column C2 -row R2
                 -leaf DCO_BBPLL/I1

    ...

add_to_rp_group DCO_BBPLL::DCO_RP -column C3 -row R3
                 -leaf DCO_BBPLL/I46
add_to_rp_group DCO_BBPLL::DCO_RP -column C4 -row R4
                 -leaf DCO_BBPLL/I47
```

3.2 IL-PLL architecture and analysis

Most of the all-digital PLLs today adopt the TDC-based architecture, as shown in Fig. 3.2. The TDC is either placed on the feedback path [23] or the feed-forward path [29]. And its noise and non-linearity will directly affect the PLL output. Therefore, while most parts of the all-digital PLLs can be synthesized from HDL [30] , most of TDCs are still designed with fully customized layout. This significantly reduced the design efficiency, and making the TDC the bottleneck of all-digital PLL. To improve the design efficiency, some custom cells can be employed [26], which is at the expense of reduced design portability.

Besides, the TDC-based all-digital PLLs suffer from the same trade-offs as the conventional analog PLLs. For a conventional analog type-II PLL, the PLL suppresses the phase noise of a free-running oscillator only within its loop bandwidth. Due to stability concerns, the PLL loop bandwidth is typically less than 0.1 times f_{fref}. However, the narrow loop bandwidth results in a limited suppression of oscillator phase noise. The same tradeoff applies to TDC-based all-digital PLLs as well, which further burdens the TDC design.

On the other hand, IL-PLLs feature a feed-forward reference injection path to correct the oscillator error, as shown in Fig. 3.3. Thus, problems with TDC, such as linearity and power-resolution trade-off, can be avoided. Moreover, the periodic phase alignment by injecting a clean reference into the oscillator makes use of the stable reference clock over a much wider bandwidth, thereby improving the suppression of free-running oscillator phase noise to obtain low in-band phase noise.

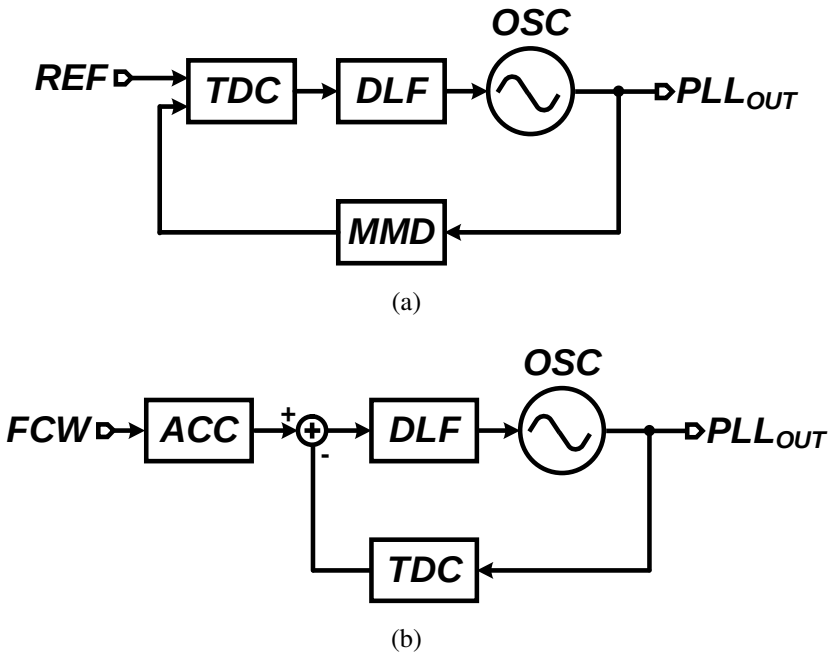


Figure 3.2: TDC-based PLL with TDC on (a) feed-forward path and (b) feedback path.

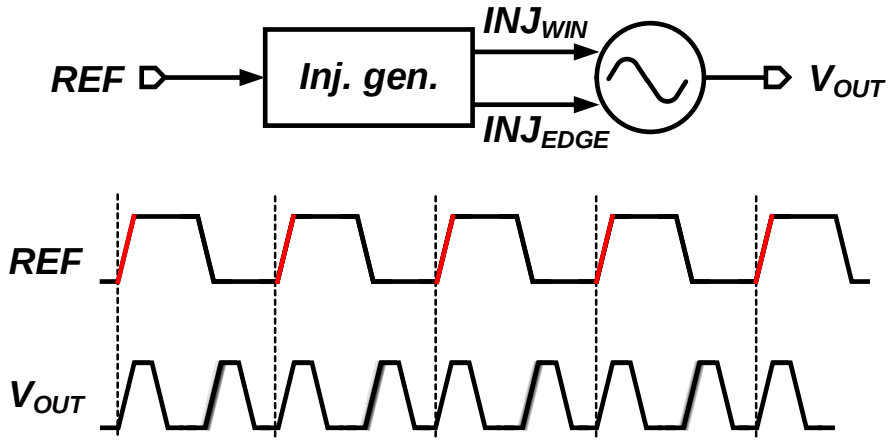


Figure 3.3: Conceptual operation of a generic injection-locked PLL (IL-PLL).

A number of published papers have devoted to the phase noise analysis of injection-locked PLL. Both continuous-time domain analysis [31, 32] and discrete-time domain analysis [33] have been performed. Note that the single side band (SSB) phase noise power spectrum density (PSD) $\mathcal{L}(f)_{\text{free-running}}$ of a free-running oscillator at frequency offset f is expressed as $\sigma_p^2 N f_{\text{ref}}/(8\pi^2 f^2)$. The SSB phase noise PSD $\mathcal{L}(f)_{\text{injection}}$ of an

edge injection-locked oscillator is given as:

$$\mathcal{L}(f)_{\text{injection}} = \mathcal{L}(f)_{\text{free-running}} \cdot \frac{2\pi^2(N-1)(2N-1)}{3f_{\text{ref}}^2N^2} \cdot \frac{f^2}{1+(f/f_{\text{inj}})^2} \tag{3.1}$$

and the injection-locking bandwidth $\mathcal{L}(f)_{\text{inj}}$ is:

$$f_{\text{inj}} = f_{\text{ref}} \cdot \frac{1}{\pi} \cdot \sqrt{\frac{3N}{2(N-1)}} \tag{3.2}$$

where f_{ref} is the injection reference, N is the multiplication factor, and σ_p^2 is the variance of Gaussian random variables of phase errors.

At high frequency offset, Eq. 3.1 can be approximated as

$$\mathcal{L}(f)_{\text{injection}} = \mathcal{L}(f)_{\text{free-running}} \cdot \frac{2N-1}{N} \approx \mathcal{L}(f)_{\text{free-running}} \cdot 2 \tag{3.3}$$

Equations (3.2) and (3.3) reveal several things. First, at a high value of N, f_{inj} is close to 0.4 times f_{ref}, which is much wider than PLL bandwidth. In addition, the phase noise of an edge injection-locked oscillator is approximately 3 dB higher than that of a free-running oscillator at high offset frequency.

3.3 Integer-N IL-PLL with non-overlap self-clocked update

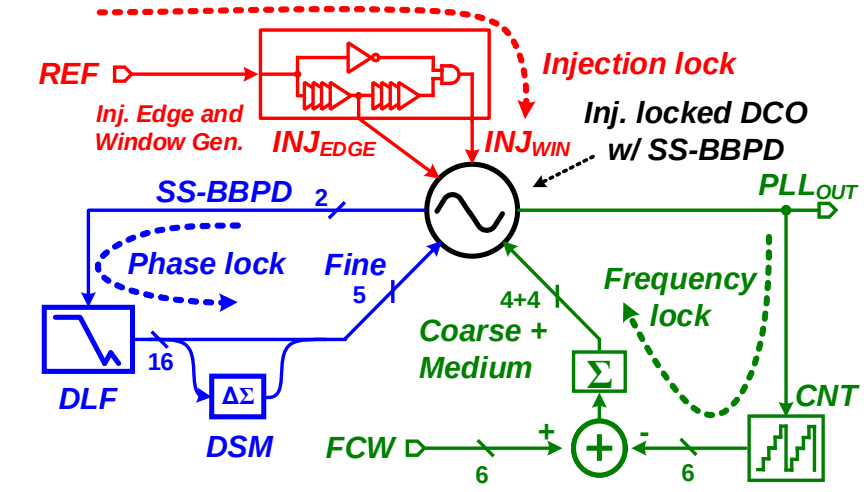
In spite of the high performance of injection-locked PLL, the phase noise performance is sensitive to frequency mismatch between the desired output frequency and oscillator free-run frequency. The synthesizable PLL in [34] used a replica oscillator to track the frequency mismatch. However, the replica oscillator incurs additional power consumption. In addition, the main oscillator and the replica oscillator inevitably have mismatches due to both device statistical variations and automatic P&R. Moreover, the different working conditions of the two oscillators also introduces a frequency mismatch, as explained in [34]. Even with interpolative DCO, a non-zero frequency mismatch persists in the oscillators. Also, the phase relationship between the injection signal edge and the DCO edge is un-synchronized with only the frequency-locked loop.

Therefore, in this design, a frequency/phase-synchronized IL-PLL is proposed. A novel DCO architecture is proposed to realized low-power operation. By using a fully symmetrical multiplexer (MUX) and an SS-BBPD, the proposed DCO can realize simultaneous injection and phase comparison without using an additional replica oscillator, thus significantly reducing power consumption. In order to minimize the reference spur, a self-clocked non-overlap update scheme is proposed in order to reduce the reference spur caused by digital logic clocking. In addition, a slope equalization technique is proposed for the SS-BBPD, which minimizes the slope-induced delay offset.

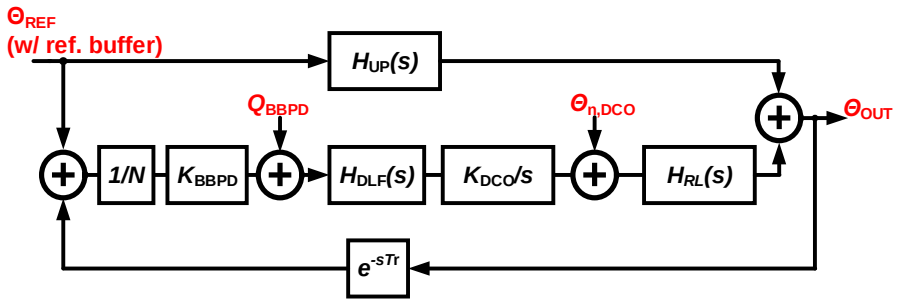
3.3.1 Phase-locked loop architecture and noise analysis

The architecture of the proposed fully synthesizable PLL is shown in Fig. 3.4(a). Three paths exist in the PLLs, the injection-lock path, the frequency-lock path, and phase-lock path. The injection-lock path has wide bandwidth and could effectively suppress the high phase noise of ring oscillators. However, ILPLL is sensitive to frequency and phase offset, and thus proper frequency and phase lock is required to mitigate process, voltage, and temperature (PVT) variations [35–37]. In this PLL design, both the frequency-lock path and phase-lock path are implemented in a digital domain, making them area-compact and synthesizable. The counter-based frequency-lock path controls the DCO coarse and medium stages. In addition, the phase-lock path uses an SS-BBPD and a digital loop filter to control the DCO fine stage. In order to further enhance the effective resolution, a DSM, which is clocked by a divided DCO output, is used to quantize the fractional bits.

Unlike the FLL-based frequency calibrated IL-PLL described in [34], the SS-BBPD phase-lock path and the injection path work simultaneously. However, the total output



(a)



(b)

Figure 3.4: (a) System architecture and (b) linearized noise model of the proposed fully synthesizable ILPLL.

phase noise is jointly determined by the injection path and the phase-lock path in order to quantize the noise contribution of each noise source. The linearized noise model of proposed PLL is shown in Fig. 3.4(b). The input reference is 100 MHz, and the frequency multiplication ratio (FMR) N is 10. The input reference phase is denoted as $\Theta_{\mathrm{n,REF}}$. For the reference injection path, a model similar to that in [31] is adopted with the phase realignment factor β set to 1. This model is described by

$$H_{\mathrm{UP}}(s) = N * e^{-sT_{\mathrm{r}}/2} * \mathrm{sinc}(\omega T_{\mathrm{r}}/2) \tag{3.4}$$

$$H_{\mathrm{RL}}(s) = 1 - e^{-sT_{\mathrm{r}}/2} * \mathrm{sinc}(\omega T_{\mathrm{r}}/2) \tag{3.5}$$

where H_{UP} represents the up-conversion of the reference noise to the PLL output, and H_{RL} is the effect of phase resetting by injection. The symmetrical SS-BBPD and MUX operation is modeled by the time delay $e^{-sT_{\mathrm{r}}}$. The SS-BBPD is modeled as a linear gain

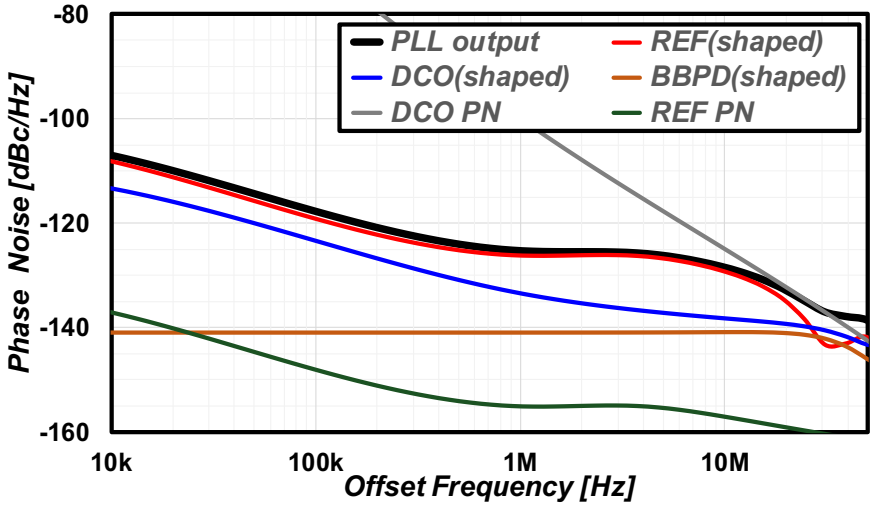


Figure 3.5: Total output noise and noise contribution from each noise source of the proposed IL-PLL based on the linear noise model.

plus output quantization noise [38, 39], as

$$K_{\mathrm{BBPD}} = \sqrt{\tfrac{2}{\pi}} \times \tfrac{1}{2\pi f_{\mathrm{ref}} \sigma_{\mathrm{t}}} \tag{3.6}$$

$$Q_{\mathrm{BBPD}}(f) = \left(1 - \tfrac{2}{\pi}\right) \tfrac{2}{f_{\mathrm{ref}}} \times \left(\mathrm{sinc}(\tfrac{f}{f_{\mathrm{ref}}})\right)^2 \tag{3.7}$$

where σ_{t} is the time domain root-mean-square (RMS) jitter at SS-BBPD input. In this noise model, σ_{t} is approximated by PLL output jitter. The digital loop filter (DLF) with 1-MHz bandwidth is modeled as its continuous-time equivalent $H_{DLF}(s) = K_P + K_I/s$, and the DCO is modeled as a continuous-time integrator K_{DCO}/s. The open-loop gain $T(s)$ and noise transfer functions (NTFs) are as follows:

$$T(s) = e^{-sT_{\mathrm{r}}} * \tfrac{K_{\mathrm{BBPD}} K_{\mathrm{DCO}}}{Ns} H_{\mathrm{DLF}}(s) H_{\mathrm{RL}}(s) \tag{3.8}$$

$$\mathrm{NTF}_{\mathrm{REF}}(s) = H_{\mathrm{UP}}(s) + \tfrac{T(s) \times e^{sT_{\mathrm{r}}}}{1+T(s)} \tag{3.9}$$

$$\mathrm{NTF}_{\mathrm{BBPD}}(s) = \tfrac{H_{\mathrm{DLF}}(s) H_{\mathrm{RL}}(s) K_{\mathrm{DCO}}/s}{1+T(s)} \tag{3.10}$$

$$\mathrm{NTF}_{\mathrm{DCO}}(s) = \tfrac{H_{\mathrm{RL}}(s)}{1+T(s)}$$

Fig. 3.5 shows the total output noise of the PLL and the noise contributions. Both DCO and reference phase noise are related to the measurement results. The modeled DCO phase noise is -100 dBc/Hz at a frequency offset of 1 MHz, with a flicker noise corner of 3 MHz. The integrated reference jitter from 10 kHz to 10 MHz is 0.25 ps, including the jitter of the reference buffers.

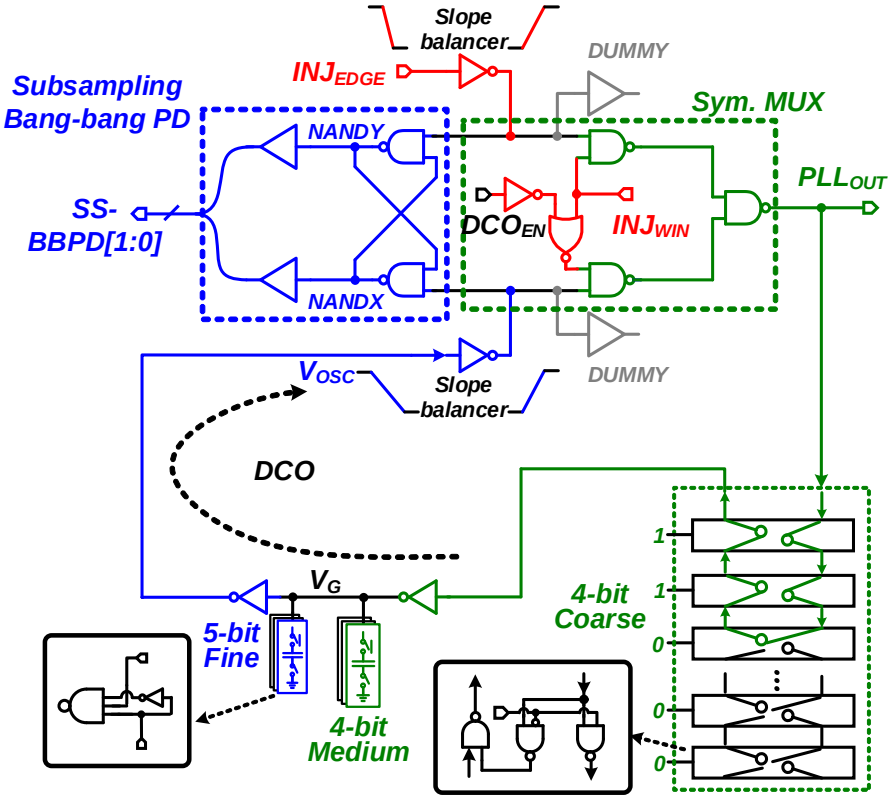


Figure 3.6: Implementation of the proposed injection-locked DCO with a sub-sampling bang-bang phase detector (SS-BBPD).

3.3.2 Highly-linear digitally controlled oscillator with self-clocked non-overlap update

In order to satisfy the power, phase noise, and tuning range requirements, a multi-stage ring DCO is proposed, as shown in Fig. 3.6. The DCO coarse stage features a delay cell based on path selection, whereas the medium and fine stages use NAND3-based digital varactors to tune the delay. The proposed varactor applies two complementary control signals to control the lowest and highest NMOSs in the NAND3 cell.

In order to reduce the digital clocking induced spur, a novel self-clocked non-overlap update scheme is proposed, as shown in Fig. 3.7. The capacitance of a digital varactor is a function of both load voltage and the digital control code. Thus, the control code update time has a significant effect on capacitance discontinuity. In Fig. 3.8, two fine-stage varactors have the same NAND3 implementation and control code, but with different update timings. In the conventional update, the control code is synchronized to a global signal, such as $\mathrm{PLL_{OUT}}$. Since the delay between $\mathrm{PLL_{OUT}}$ and V_G depends on the DCO coarse stage delay and PVT conditions, there is a possibility that the control code updates

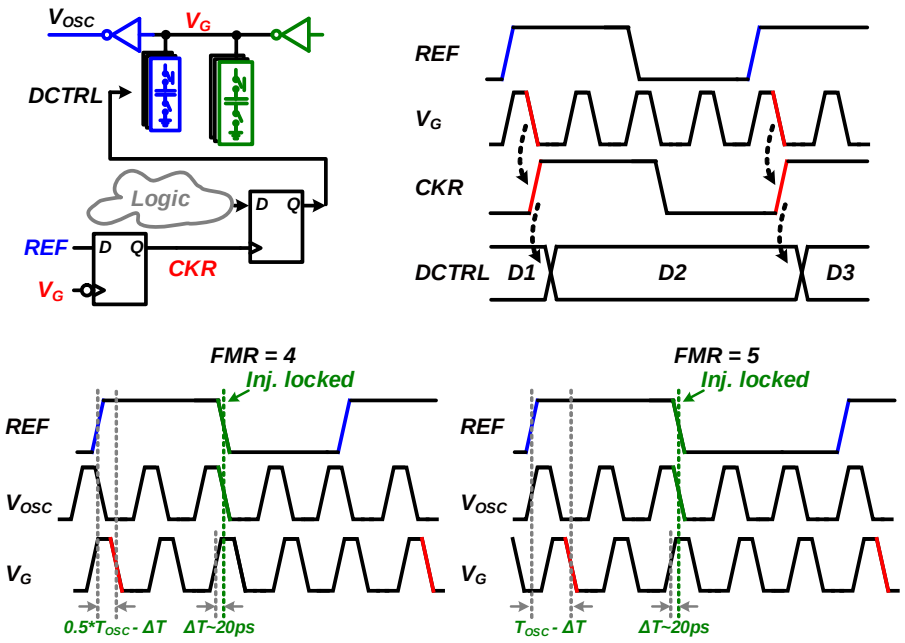


Figure 3.7: Circuit implementation of the proposed self-clocked non-overlap update scheme.

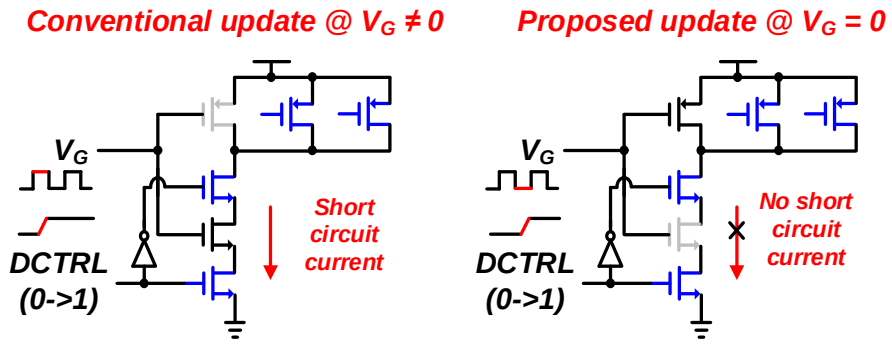


Figure 3.8: Time-domain operation of the proposed self-clocked non-overlap update scheme.

at non-zero V_G. This will induce a capacitance discontinuity and degrade the reference spur, as shown in Fig. 3.9. In contrast, in the proposed self-clocked non-overlap update scheme, the fine-stage control code is locally synchronized to its output V_G. Thus, the control code is guaranteed to update when V_G is zero. In this way, capacitance discontinuity is eliminated, as shown in Fig. 3.9. As an additional bonus, the proposed update scheme eliminates short circuit currents in the NAND3 varactor, which enables a power reduction of 30% as compared to the conventional NAND2 varactor while having the same resolution.

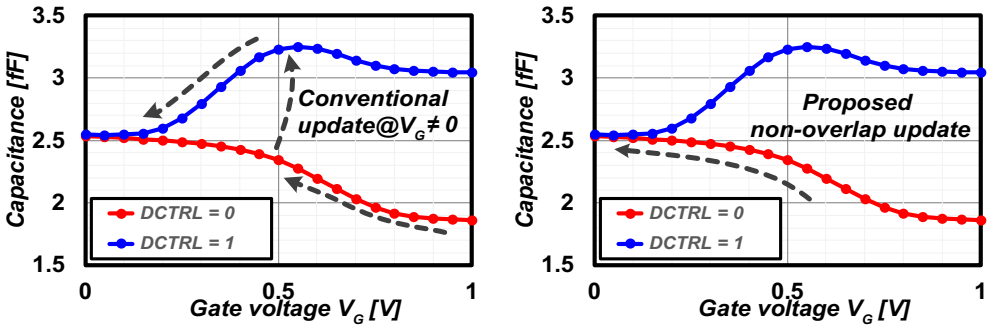


Figure 3.9: Varactor capacitance characteristic of the proposed self-clocked non-overlap update scheme.

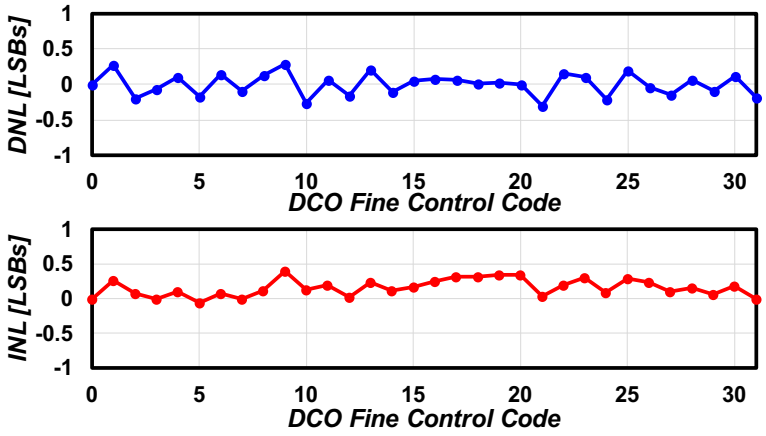


Figure 3.10: Digitally controlled oscillator fine-stage nonlinearity obtained from post-layout simulation.

The timing relationship among REF, V_{OSC}, and V_G is shown in Fig. 3.7. With falling edge injection, the falling edges of REF and V_{OSC} are aligned, and the rising edge of V_G is $\Delta\tau$ ahead, where $\Delta\tau$ is one inverter delay (approximately 20 ps). The timing margin is $0.5 \cdot T_{OSC} - \Delta\tau$ and $T_{OSC} - \Delta\tau$ for even and odd FMRs, respectively, where T_{OSC} is the DCO period. The worst-case additional delay is less than one DCO period, which has a negligible effect on stability. Moreover, in order to mitigate layout-induced mismatches and variations, relative placement design constraints are applied to standard digital P&R, and a reasonably good linearity was achieved, as shown in Fig. 3.10. The DNL represents the differential nonlinearity, whereas the INL represents the integral nonlinearity.

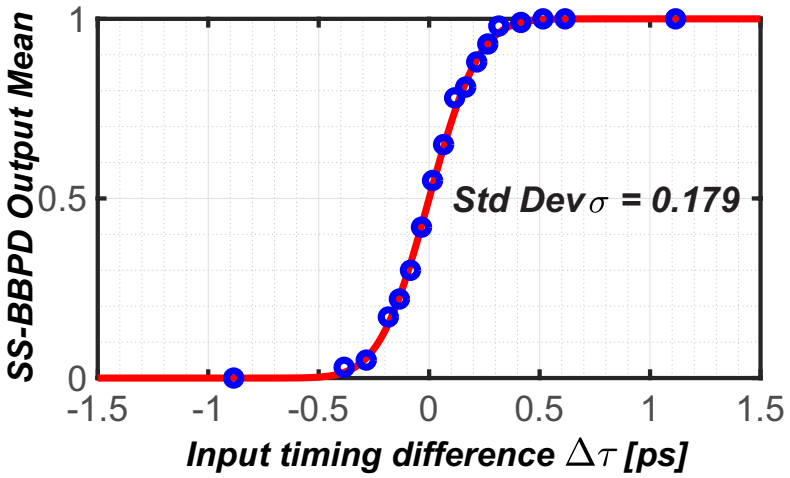


Figure 3.11: Sub-sampling bang-bang phase detector input offset obtained from Monte-Carlo post-layout simulation.

3.3.3 Fully symmetrical low-offset multiplexer and sub-sampling bang-bang phase detector design

Since the IL-PLL is sensitive to delay mismatch between the injection path and the phase detection path [37,40], single-ended fully symmetrical MUX and SS-BBPD are integrated into the DCO in order to simplify routing and reduce the mismatch. In order to minimize path mismatch between the MUX and the SSPD, the two parts are designed jointly and are optimized for low delay offset. As shown in Fig. 3.6, both the SS-BBPD and the MUX are implemented with NAND2 standard cells so as to ensure symmetry. In order to minimize the slope induced delay offset in the SS-BBPD, a pair of slope balancers are placed on the V_{OSC} and the INJ_{EDGE} path. In addition, two dummy loads are added in order to reduce the percent of capacitance variation with different INJ_{WIN} conditions. The layout mismatches and variations are minimized with compact area and constraint-directed layout synthesis. In order to further reduce slew-rate mismatch, background calibration can be implemented [41].

The intrinsic delay of the proposed MUX is only three inverter delays, which is beneficial in order to achieve a high oscillation frequency of 1.8 GHz in this design. The delay offset of the proposed SS-BBPD in the presence of device mismatch is obtained through Monte-Carlo simulation. Two inputs V_{OSC} and INJ_{EDGE} with different timing differences between were swept, and the occurrence of output 10/01 was recorded in order to obtain the mean value. Figure 3.11 shows the output mean value under each timing setting. A RMS phase offset of 0.18 ps was obtained by fitting the result to a Gaussian error function (erf), which translates to an offset-induced reference spur of < -74 dBc.

Table 3.2: Summary of reference spur simulation.

	Before Cal. [dB]	After Cal. [dB]
$Spur_{\text{BBPD}}$	-47.5	-74.9
$Spur_{\text{Varactor}}$	-50.1	-78.7
$Spur_{\text{tot}}$	-42.7	-70.5

The effectiveness of the proposed reference spur calibration can be estimated with the following equation.

$$Spur_{\text{tot}} = 20 \cdot log10(10^{\frac{Spur_{\text{BBPD}}}{20}} + 10^{\frac{Spur_{\text{Varactor}}}{20}}) \tag{3.11}$$

where the $Spur_{\text{tot}}$ is the total reference spur, $Spur_{\text{BBPD}}$ is the BBPD offset-induced reference spur, $Spur_{\text{Varactor}}$ is the reference spur caused by non-ideal clock update timing. All the reference spurs are expressed in dB. Since the reference spurs are caused by deterministic imperfects, the worst cause reference can be estimated by adding the magnitude of various imperfects.

To quantize the effectiveness of each calibration, a set of behavioral simulations were carried out. Only one imperfect was considered in one simulation, with all the other factors being ideal. The simulation results are summarized in Table 3.2. As clear from the table, before the calibration, the total reference spur is jointly determined by both BBPD delay offset and varactor non-ideal clock update timing. And the BBPD delay offset contributed more to the overall reference spur. And to realize < -70 dBc reference spur, both imperfects need to be minimized.

3.3.4 Measurement results

The entire PLL is synthesized using commercial digital design tools with a non-modified standard cell library. The core area of the PLL is 0.035 mm^2, which is fabricated in a 65 nm CMOS process. Figure 3.12 shows the die photograph. The phase noise is measured by a signal source analyzer (Keysight E5052B), and the spectrum is measured by a spectrum analyzer (Anritsu MS2830A). Figures 3.13 and 3.14 show the measured phase noise and spectrum in integer-N mode with a 100 MHz reference clock. The integrated jitter is 0.4 ps jitter from 10 kHz to 10 MHz. The DCO achieves -98 dBc/Hz at a frequency offset of 1 MHz and a power consumption of 1.0 mW. Note that the spurs around 10 kHz, 100 kHz, and 10 MHz are caused by non-ideal grounding of measurement equip-

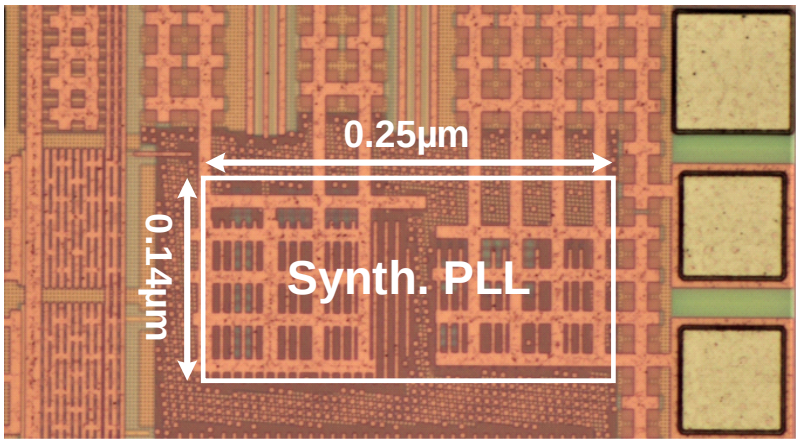


Figure 3.12: Die micrograph of the fully synthesizable ILPLL.

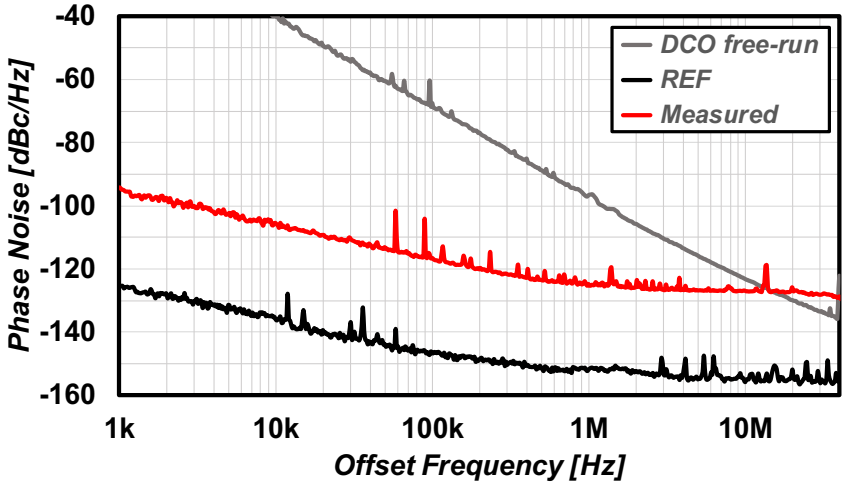


Figure 3.13: Measured PLL output phase noise at an output frequency of 1.0 GHz with an input reference of 100 MHz.

ment. The reference spur at a frequency offset of 100 MHz is around -52 dBc, which is 7 dB better than that in a previous study [19]. In order to investigate the higher than expected reference spur, the DCO supply was changed by ±50mV. The reference spur was barely changed, indicating that the phase offset between the MUX and the SS-BBPD is not the limiting factor. On the other hand, the reference spur could be improved by 2 dB by reducing the input reference power from 12 dBm to 7 dBm, albeit with much degraded phase noise. Thus, the limiting factor could be parasitic coupling through input pads, probe pins, or supply.

The PLL performance is summarized and compared in Table 5.3. The -52 dBc refer-

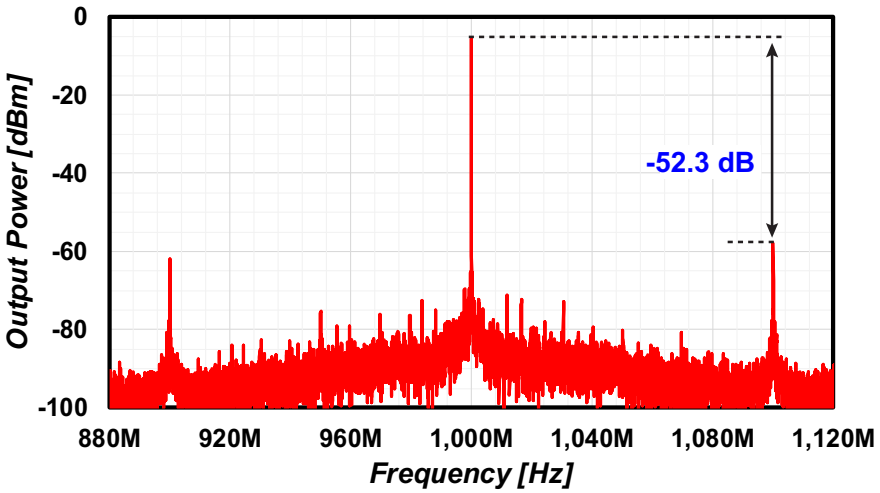


Figure 3.14: Measured PLL output spectrum at an output frequency of 1 GHz with an input reference of 100 MHz.

ence spur is the best among the synthesizable PLLs, but is worse than that reported in a previous study [41]. In addition, the proposed PLL achieves the highest jitter-power FOM among the synthesizable PLLs, even without using a reference doubler.

Table 3.3: Performance summary and comparison.

	This Work	**[19]**	**[28]**	**[40]**	**[41]**
Arch.	IL-PLL	IL-PLL	TDC PLL	MDLL	ILCM
Synth. ?	**Yes**	Yes	Yes	No	No
Marco ?	**No**	No	Yes	-	-
Type	Int-N	Frac-N	Int-N	Int-N	Int-N
Tech. [nm]	65	65	14	28	65
Area [mm^2]	0.035	0.012	0.009	0.0056	0.055
Power [mW]	1.2	2.2*	9.7	1.45	11.0
Ref. [MHz]	100	100	50	200	100
FMR	10	10	100	15	24
Int. Jitter [ps]	0.4	0.3*	4.71	0.292	0.14
Int. BW [MHz]	0.01-10	0.01-10	-	0.01-40	0.01-30
Ref. Spur [dBc]	**-52**	-45	-40	-44	-72
FOM† [dB]	-247.2	-246.7*	-216.8	-249.1	-246.7
Design Time	Days		Months		

* Integer-N mode w/ reference doubler

† $\text{FOM} = 10 \cdot \log[(\sigma_t/1s)^2(P_{DC}/1\text{mW})]$

3.4 DTC-based fractional-N injection-locked PLL

The IL-PLL presented in previous section, as well as a variety of other IL-PLLs and multiplying delay-locked loops (MDLLs) [34, 35, 40, 42–54], achieved impressive jitter performance, due to the high bandwidth offered by the IL-PLLs/MDLLs. However, conventional IL-PLLs/MDLLs are limited to integer-N operation, whereas in wireless transceivers, fractional-N operation is desired. To extend injection locking to fractional-N operation, either a delay-modulated reference [18, 43] or multi-phase injection [44] can be employed. In this section, a DTC-based IL-PLL will be presented [19]. The DTC introduces a time-varying delay to the injection signal, thereby enabling the realization of fractional-N injection locking.

3.4.1 System diagram

The system diagram of the proposed IL-PLL is shown in Fig. 3.15. The upper part contains the synthesizable timing generation blocks, which consists of a reference doubler (REFD), a DTC and an injection-locked oscillator (ILO). The low part includes the RTL-synthesized calibration logics for each of the timing generation blocks. All of the calibration blocks utilize the same bang-bang phase detector (BBPD) output, and each calibration block extracts the corresponding error information from the statistical distribution of the BBPD output. This arrangement makes the calibration result consistent and free of mismatch.

Due to the vastly different range of each non-idealities, dedicated optimization is required, as shown in Table 3.4. The duty cycle error inside the reference doubler and the frequency error within the injection-locked oscillator are on the order of tens of ps, which is relatively narrow. For the DTC, on the other hand, a large dynamic range is needed to cover more than one DCO period, which is approximately 1 ns. Furthermore, the DTC resolution must be fine enough to minimize the effect of DTC quantization noise, and is set to approximately 0.3 ps. Therefore, the DTC must have an effective number of bits (ENOB) of more than 12. Thus calibration of nonlinearity is necessary. Besides, the DTC must also have the correct gain, which is defined as the ratio of the timing domain delay to the digital control code. Thus, the DTC design and calibration prove to be crucial in proposed design, and will be the main focus of this study.

3.4.2 Multi-stage synthesizable DTC

There are many different DTC implementations, such as constant-slope (CS) [55–57], variable-slope (VS) [8, 58–60], path-selection (PS) based topologies [19, 35, 54, 61]. Sev-

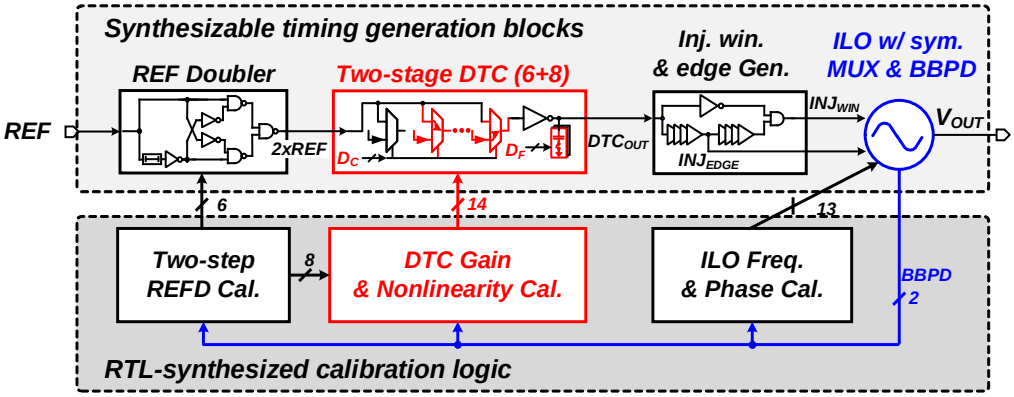


Figure 3.15: System diagram of proposed fully-synthesizable DTC-based fractional-N MDLL.

Table 3.4: Errors and calibrations of the proposed MDLL.

	REF. Doubler	Coarse DTC		Fine DTC	ILO
Range	Narrow (10 ps)	Wide (1000 ps)		Narrow (10 ps)	Narrow (10 ps)
Error Type	Duty Cycle Error	Gain Error	**Nonlinearity***	Gain Error	Freq./Phase Error
Compensated by	Fine DTC	Coarse DTC	**Fine DTC**	Fine DTC	ILO

* Proposed in this paper.

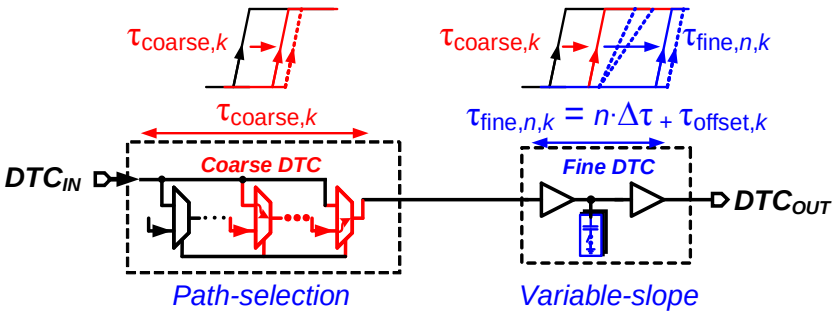


Figure 3.16: Two-stage synthesizable DTC with path-selection DTC as coarse stage, and variable-slope DTC as fine stage.

eral design considerations guide the design of DTCs, among which the most important are delay range, resolution, noise and nonlinearity. Considering the feasibility for standard cell implementation, VS and PS DTCs are preferred, as shown in Fig. 3.16. The PS DTCs have a resolution of about two inverter delays, which is around 30 ps in a 65 nm CMOS process, whereas the VS DTCs could have sub-ps resolution. However, besides the achievable resolution, these two kinds of DTCs have very different noise and nonlinearity

characteristics, which merit close examination and careful design optimization.

Noise analysis: white noise and flicker noise

Since the DTC noise will directly translate to the IL-PLL output, low noise design is of great importance. The noise of a VS DTC is proportional to the total delay $\tau_{\text{delay,tot}}$, as described by [58, 62].

$$\mathcal{L}_{\text{white}} \propto 10\log\Big(f_{\text{out}}\frac{kTC_{\text{L}}}{I_{\text{dis}}^2}\Big) \propto 10\log\Big(f_{\text{out}}\frac{kT\tau_{\text{delay,tot}}}{I_{\text{dis}}}\Big) \tag{3.12}$$

$$\mathcal{L}_{\text{flicker}} \propto 10\log\Big(f_{\text{out}}^2\frac{C_{\text{L}}^2}{I_{\text{dis}}^2}\frac{2K}{WLf}\Big) \propto 10\log\Big(f_{\text{out}}^2\tau_{\text{delay,tot}}^2\frac{2K}{WLf}\Big) \tag{3.13}$$

$$\tau_{\text{delay,tot}} = \tau_{\text{variable}} + \tau_{\text{overhead}} \approx 3\cdot\tau_{\text{variable}} \tag{3.14}$$

where $\mathcal{L}_{\text{white}}$ is the phase noise caused by thermal noise, and $\mathcal{L}_{\text{flicker}}$ the phase noise caused by flicker noise. τ_{variable} is the maximum variable delay, and τ_{overhead} is the delay overhead. Because the synthesizable digital varactors have limited ON/OFF capacitance ratio of approximately 3/2, therefore large delay overhead is resulted for a given variable delay range, making the total delay three times the usable variable delay range.

On the other hand, assuming the noise of each delay cell are uncorrelated, the noise of a N-stage PS DTC can be expressed as

$$\mathcal{L}_{\text{white}} = 10\log(N) + \mathcal{L}_{\text{white,0}} \propto 10\log\Big(N\cdot f_{\text{out}}\frac{kT\tau_{\text{delay,0}}}{I_{\text{dis}}}\Big) \tag{3.15}$$

$$\mathcal{L}_{\text{flicker}} = 10\log(N) + \mathcal{L}_{\text{flicker,0}} \propto 10\log\Big(N\cdot f_{\text{out}}^2\tau_{\text{delay,0}}^2\frac{2K}{WLf}\Big) \tag{3.16}$$

$$\tau_{\text{delay,tot}} = \tau_{\text{overhead}} + \tau_{\text{variable}} \approx N\cdot\tau_{\text{delay,0}} \tag{3.17}$$

where $\tau_{\text{delay,0}}$ is the delay of unit delay cells, $\mathcal{L}_{\text{white,0}}$ is the single stage white noise induced phase noise, $\mathcal{L}_{\text{flicker,0}}$ is the single stage flicker noise induced phase noise. The $\mathcal{L}_{\text{white,0}}$ and $\mathcal{L}_{\text{flicker,0}}$ can be calculated with Eqs.(3.12-3.13). Above equations can be re-written as

$$\mathcal{L}_{\text{white}} \propto 10\log\Big(f_{\text{out}}\frac{kT\tau_{\text{delay,tot}}}{I_{\text{dis}}}\Big) \tag{3.18}$$

$$\mathcal{L}_{\text{flicker}} \propto 10\log\Big(f_{\text{out}}^2\frac{\tau_{\text{delay,tot}}^2}{N}\frac{2K}{WLf}\Big) \tag{3.19}$$

Because PS DTCs have negligible delay offset, the total delay is approximately equal to the usable variable delay range. Therefore, PS DTCs are more power efficient than VS DTCs for a given noise requirement. For a given variable delay range τ_{variable}, the PS DTCs have $10\log(3) \approx 4.8$ dB lower phase noise in white noise region, and $10*\log(9N)$ dB lower phase noise in flicker noise region. On the other hand, for a given total delay $\tau_{\text{delay,tot}}$, the PS DTC has $10 * \log(N)$ dB lower the flicker noise, which agrees well with the phase

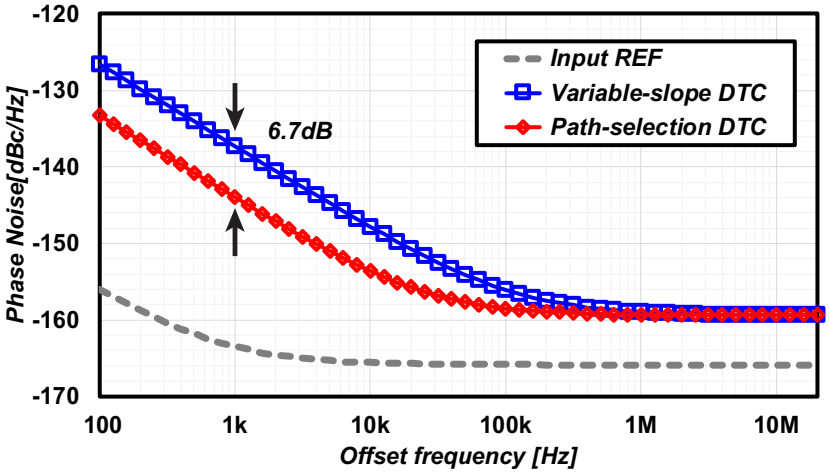
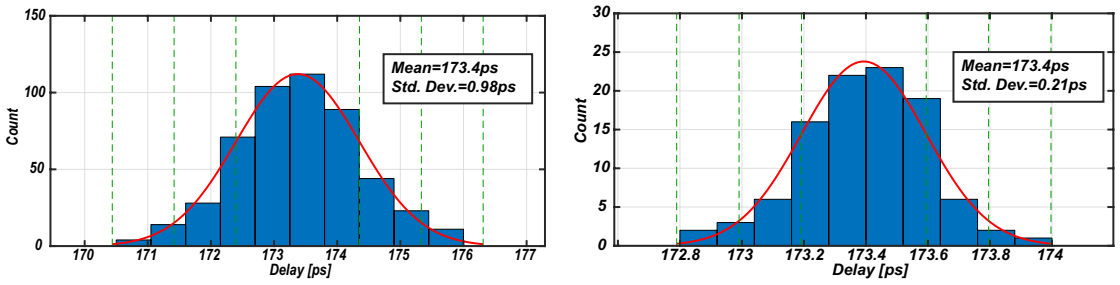


Figure 3.17: Simulated phase noise of a variable-slope DTC and 6-stage path-selection DTC. The two DTCs are designed with the same power consumption and delay.

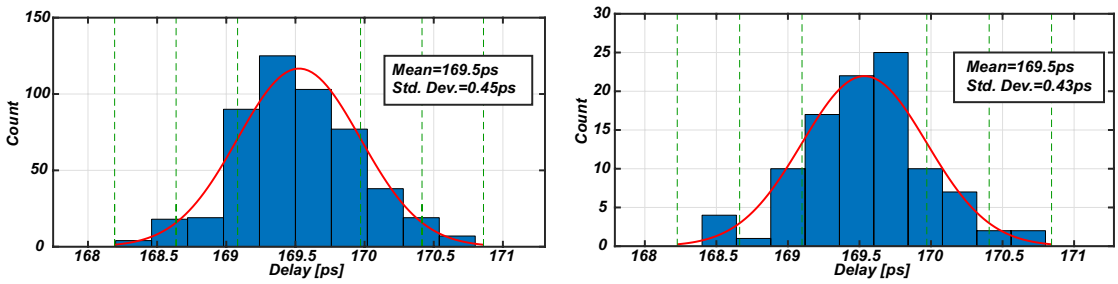


(a) (b)

Figure 3.18: Statics of variable-slope based DTC delays with (a) 500x Monte Carlo simulations and (b) 100 samples from 10 trails of automatic P&R.

analysis in ring oscillators [17].

As an example, the phase noise of a VS DTC and a 6-stage PS DTC are simulated, and the simulated phase noise plots are shown in Fig. 3.17. The two DTCs are designed to have the same total delay $\tau_{\text{delay,tot}}$ and power consumption. In the white noise region, the phase noise of the two DTCs are about the same, which is as expected. In the flicker noise region, the PS DTC has 6.7 dB lower phase noise than the VS DTC. This difference is a little lower than expected value of $10 * \log(6) \approx 7.8$ dB, which could attribute to the different noise models caused by different device sizes. Nonetheless, the simulation results validated above noise analysis and comparison of PS DTCs and VS DTCs.



(a) (b)

Figure 3.19: Statics of path-selection based DTC delays with (a) 500x Monte Carlo simulations and (b) 100 samples from 10 trails of automatic P&R.

Nonlinearity analysis: statistical device mismatch and P&R mismatches

Nonlinearity in DTC causes spurs and noise, and interferes the DTC gain calibration. Therefore, highly-linear DTCs are desired. The nonlinearity is not only affected by circuit topology, but also affected by device statistical mismatch and how the layout is implemented. The device statistical mismatch is generally modeled as a zero-mean normal distribution, whereas nonlinearity from circuit effects such as slope dependent prorogation delay [8, 59, 60, 63] is a deterministic value which can be predicted through circuit simulations. On the other hand, The P&R mismatch is deterministic in custom designs with manual layout, but proved to follow a zero-mean normal distribution in a automatic P&R design [64]. Therefore, for synthesizable DTCs, the mismatch induced DNL of DTC can be estimated from the distribution of each mismatch sources.

$$\sigma_{\mathrm{DNL,tot}} = \sqrt{\sigma^2_{\mathrm{DNL,stat.}} + \sigma^2_{\mathrm{DNL,P\&R}}} \tag{3.20}$$

where $\sigma_{\mathrm{DNL,tot}}$ is the total standard deviation of DTC DNL, and $\sigma_{\mathrm{DNL,stat.}}$ and $\sigma_{\mathrm{DNL,P\&R.}}$ are standard deviation of DNL from device statistical mismatch and automatic P&R respectively.

For DNL caused by device statistical mismatch, the transfer function is similar to the one from device flicker noise to output noise. Thus

$$\sigma_{\mathrm{DNL,stat}} \propto \begin{cases} \tau^2_{\mathrm{delay,tot}} & \text{variable-slope DTC} \\ \tau^2_{\mathrm{delay,tot}}/N & \text{path-selection DTC} \end{cases} \tag{3.21}$$

where N represents the number of activated PS DTC stages. On the other hand, the DNL caused by automatic P&R depends not only device parameters, but also layout constraints such as standard cell size, routing line width, and overall circuit size. Therefore, post-

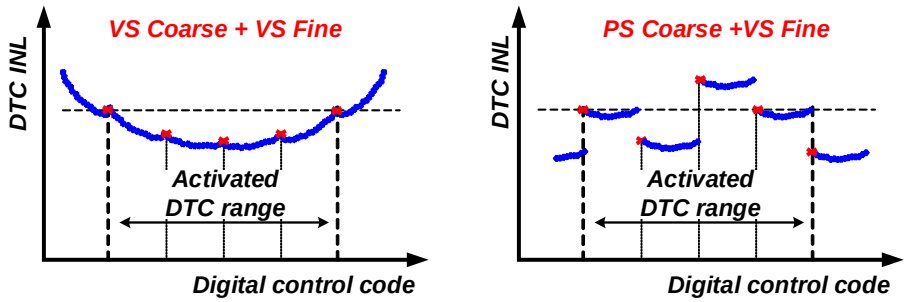


Figure 3.20: Nonlinearity characteristics of a two-stage variable-slope DTCs [8], and proposed two-stage DTC with path-selection coarse stage and variable-slope fine stage.

layout simulations of multiple automatic P&R trials are needed to obtain the mean and standard deviation of P&R mismatch. The DNLs of the VS DTC and PS DTC for previous phase noise comparison are shown in Fig. 3.18 and Fig. 3.19 respectively. The DNLs from device mismatch are obtained from schematic level Monte-Carlo simulations. The ratio of standard deviations of the two DTCs follows the result predicted by Eq.(3.21). The DNLs from automatic P&R are obtained from 100 layout samples. As evident from the results, the standard deviation of PS DTC is larger than VS one, which could attribute to the different layout sizes and line routing.

Based on noise and resolution analysis, it is evident that a multi-stage segmented DTC implementation with PS as coarse stage and VS as fine stage is preferred. However, the PS coarse stage nonlinearity is dominated by device mismatches and automatic P&R, whereas the VS fine stage nonlinearity is dominated by system INL caused by slope prorogation delay. Such difference proves critical in nonlinearity calibration, with which new calibration scheme is required.

3.4.3 TANC nonlinearity calibration for DTC

To sufficiently suppress the noise and nonlinearity, large devices and high power consumption are typically employed in custom designed VS DTCs [58, 60]. However, for synthesizable PS DTCs, larger devices will cause longer routing lines, increasing congestion and variation, thus degrade linearity. Therefore, the over-sizing is not a viable option, and nonlinearity calibration is a must.

Proposed nonlinearity calibration

For VS DTCs with custom layout [8, 20, 59], the DNL is much smaller than the systemic INL. To calibrate the systemic INL, piece-wise linear interpolation (PWLI) based calibra-

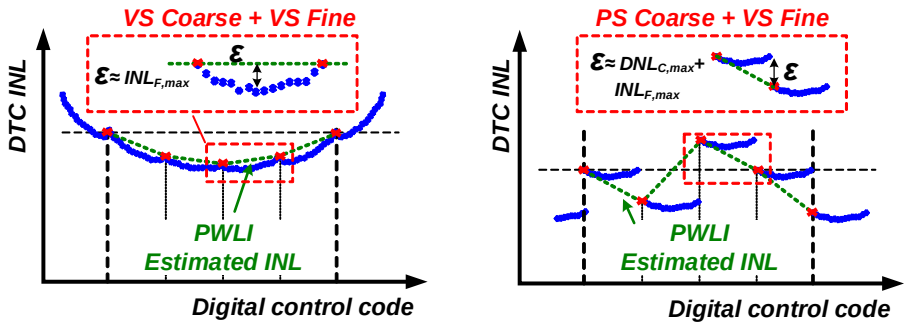


Figure 3.21: Concept of conventional PWLI-based calibration for custom-designed VS DTC, and synthesizable PS-VS DTC.

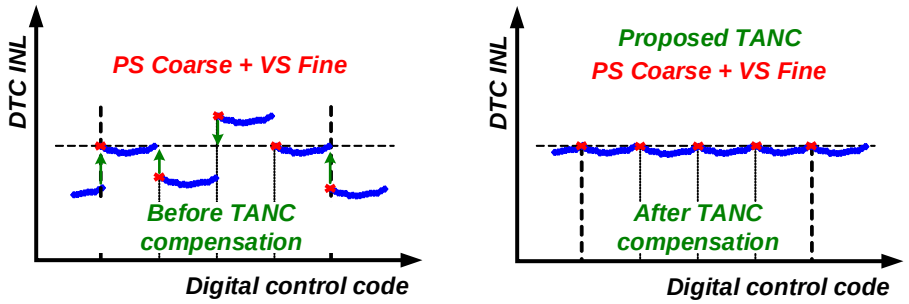


Figure 3.22: Concept of proposed TANC nonlinearity calibration for synthesizable PS-VS DTC.

Table 3.5: Implementation of DTCs and associated nonlinearity calibration

	DTC design	Synth.?	Cal.
JSSC'14 [8]	coarse stage VS + fine stage VS	No	PWLI
JSSC'15 [35]	coarse stage PS + fine stage VS	No	PWLI
JSSC'16 [65]	single-stage VS	No	PWLI
This work	coarse stage PS + fine stage VS	**Yes**	**TANC**

tion have been proposed in [8], [20,65], as shown in Fig. 3.20. Assume the DTC transfer function can be approximated by a nonlinear function $f(x)$. An inverse function

$$\hat{c}(x) = f^{-1}(\xi x + \delta) \tag{3.22}$$

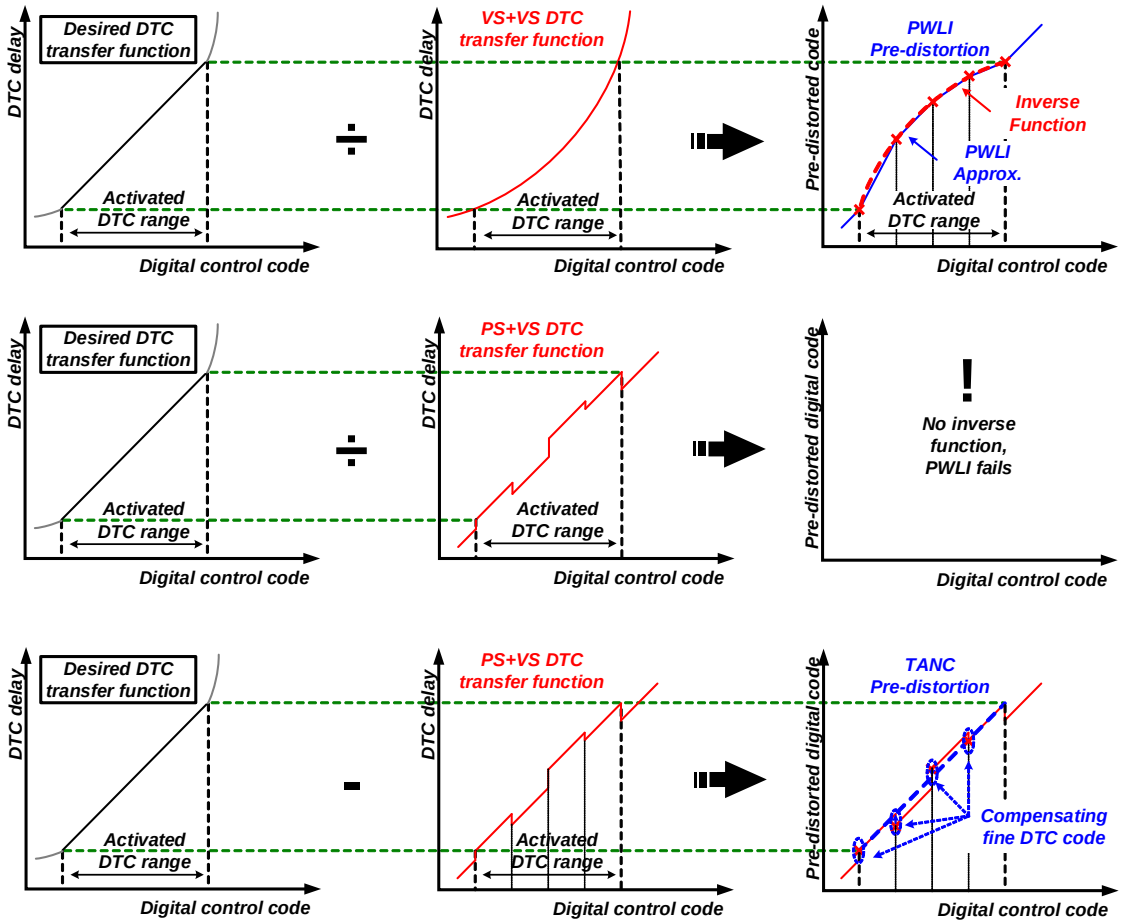


Figure 3.23: Comparison of conventional PWLI and proposed TANC nonlinearity calibration for systemic INL dominated VS DTCs and local DNL dominated synthesizable PS-VS DTCs.

can be found to linearize the composite function $f[\hat{c}(x)]$. And the PLWI approximate the $\hat{c}(x)$ with a look-up table (LUT). However, as correctly identified by the authors in [8, 65], the PWLI calibration can only correct “global" INL, while leave the localized DNL uncorrected. In [8], the mismatch of coarse DTC capacitors were assumed to be much smaller than the systemic INL caused by slope dependent prorogation delay, which is about 1.2% of the DTC full range, i.e. 3.6 ps. Whereas in [65], the DTC capacitor array were sized to ensure the mismatch-induced DNL is negligible.

Such arrangement has been proved sufficient for custom-designed VS DTCs. However, for synthesizable DTCs with PS-VS segmented design, the DNL is comparable to systemic INL, as evident by simulation results in Fig. 3.19. The maximum PWLI estima-

tion error $\epsilon_{\max}$ can be estimated by

$$\epsilon_{\max} \approx DNL_{\mathrm{C,max}} + INL_{\mathrm{F,max}} \tag{3.23}$$

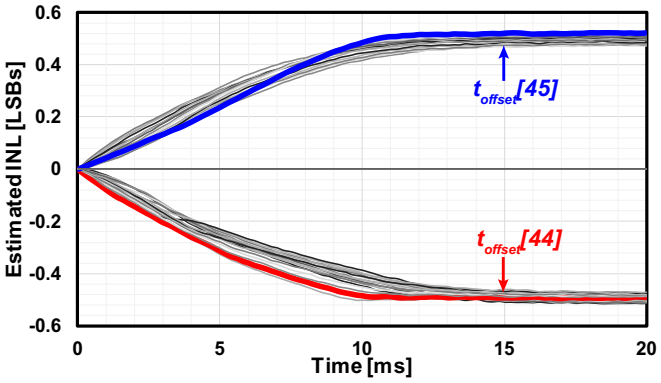
where $DNL_{\mathrm{C,max}}$ is the maximum DNL of the coarse stage, and $INL_{\mathrm{F,max}}$ is the systemic nonlinearity of the the fine stage. For synthesizable DTC designs with automatic P&R, the $DNL_{\mathrm{C,max}}$ is much larger than $INL_{\mathrm{F,max}}$, as shown in Fig. 3.21. Such a large error prevents the DTC gain calibration and PWLI-based nonlinearity calibration from correct convergence. Therefore, to more efficiently calibrate nonlinearity, a new calibration scheme is proposed for the synthesizable DTC. As shown in Fig. 3.20, the overall INL exhibits a "staircase" shape. Therefore, the calibration points are designed to match the coarse stage segmentation. The LUT coefficients are designed to match the coarse DTC code, and the compensation coefficients are directly added to the fine stage, realizing a “zero-order" estimation and compensation, as shown in Fig. 3.22. Besides, the proposed TANC eliminates the power consumption of linear interpolation computations [66]. Therefore, it is more power and area efficient for the synthesizable DTC implementation.

More fundamentally, the difference between the proposed TANC and conventional PWLI lies in the underlying assumption of nonlinearity. As shown in Fig. 3.23, the PWLI assumes an inverse function of the real DTC transfer function exists, and that inverse function can be curve fitted by with a set of piece-wise linear functions. However, for DTCs that do not meet such requirements, such as the PS-VS segmented DTCs, no inverse function can be found to approximate the whole delay range. Thus the PWLI would fail. On the other hand, the TANC does not try to find a global inverse function. It just find the cause of each transfer function discontinuity, and apply compensating value to the respective point. Thus it is more robust and universal.

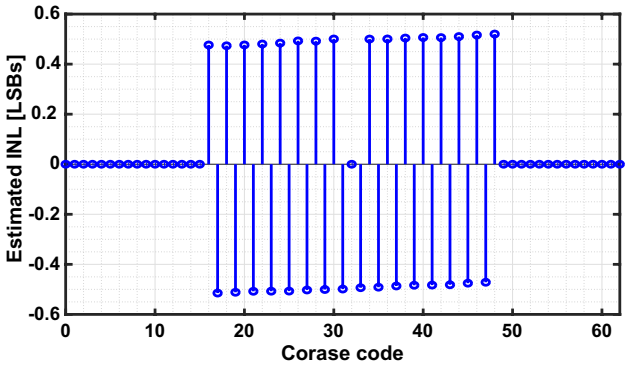
Table 3.5 summarizes the DTC and associated digital nonlinearity calibration in the proposed IL-PLL and related DTC-based PLLs/MDLLs. All the previous designs employed PWLI-based DTC calibration, regardless of the DTC implementations. On the other hand, this design recognizes the difference between path-selection DTCs and variable-slope DTCs. And a novel calibration scheme TANC is proposed to more efficiently compensate the segmented DTC nonlinearity.

Simulation results

To validate the effectiveness of the proposed TANC method, behavioral simulations were performed. Both the digital calibration and the synthesizable analog circuits, such as the DCO and DTC, are modeled with time-domain Verilog models. Thus the model is truly event-driven in time domain, and can be simulated at fast speed. To best demonstrate the



(a)



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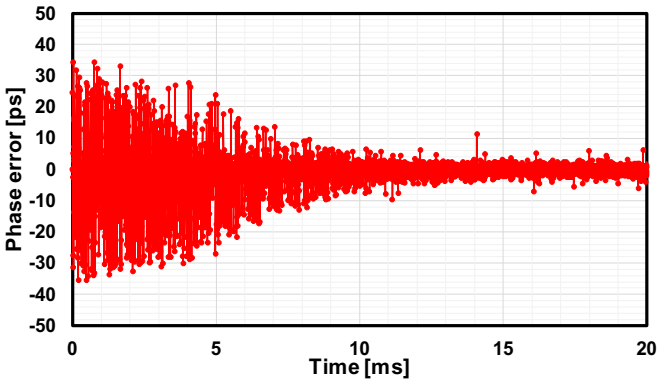
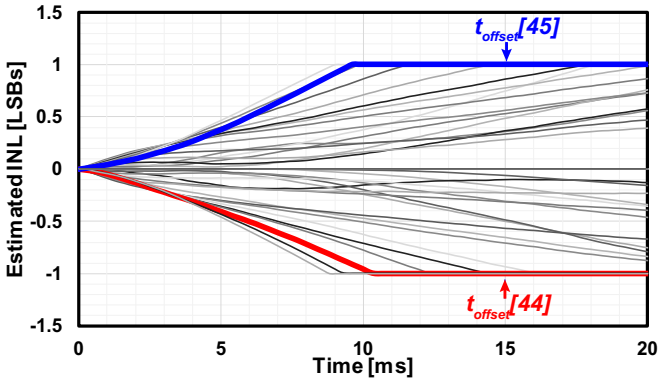


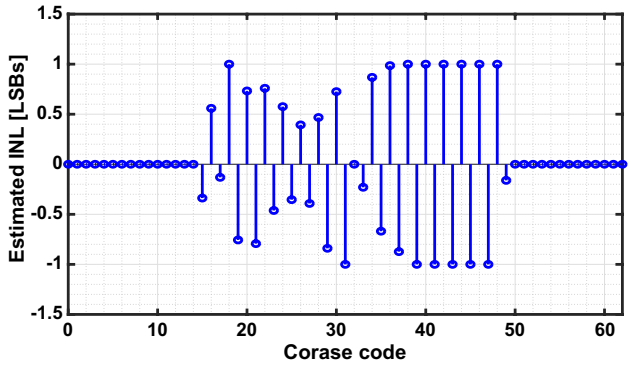
(c)

Figure 3.24: Behaviorial simulation of the proposed TANC for a DTC with ±30 ps DNL, when FCW = $N + \alpha$, where N=10, $\alpha = 2^{-6} + 2^{-12}$ and f_{ref}=50 MHz. (a) Time-domain convergence plot (b) Final settled INL estimate(c) Time-domain phase error present at the BBPD input.

advantages of proposed calibration, the DTC was modeled with large DNL jumps as large as 30 ps, i.e. 1 LSB, albeit practically DNL is smaller. The calibration results with the proposed TANC method are shown in Fig. 3.24. The calibration converged to the correct



(a)



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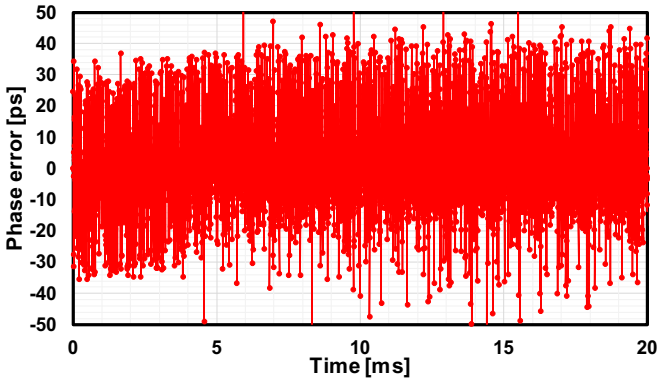


(c)

Figure 3.25: Behaviorial simulation of conventional PWLI calibration for a DTC with ±30 ps DNL, when FCW = $N + \alpha$, where N=10, $\alpha = 2^{-6} + 2^{-12}$ and f_{ref}=50 MHz. (a) Time-domain convergence plot (b) Final settled INL estimate(c) Time-domain phase error present at the BBPD input.

value after 10 ms. Additionally, the phase error was significantly reduced with TANC enabled, as shown in Fig.3.24(c). For comparison, the calibration of the same nonlinearity with conventional PWLI calibration is also shown in Fig.3.25. With the same number of

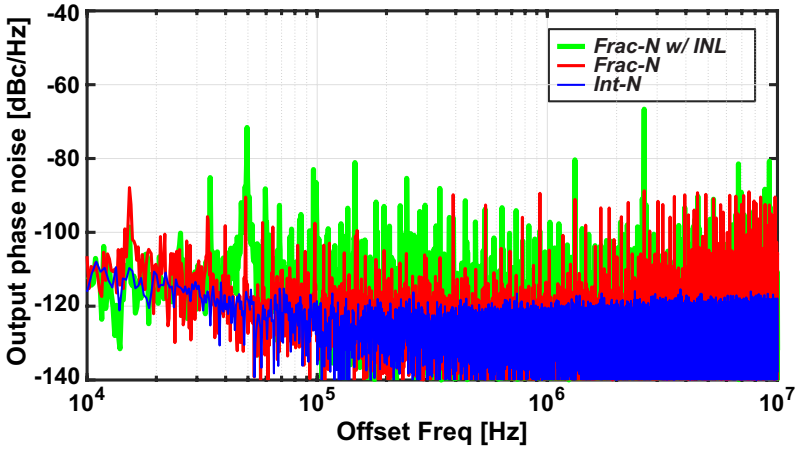


Figure 3.26: Simulated phase noise of IL-PLL with 100 MHz reference frequency and reference doubler, in 1) integer-N mode, 2) fractional-N mode w/ INL calibration and 3) fractional-N mode w/o INL calibration. The integer-N mode output frequency is 1 GHz, and the fractional-N output frequency is 971.24 MHz.

Table 3.6: Implementation of proposed two-stage synthesizable DTC

	Control bits	Range [ps]	Resolution [ps]
Coarse	6-bit	1801.7 (119.4-1921.1)	28.6
Fine	8-bit	60.6 (113.8-174.4)	0.24

calibration points, the PWLI calibration cannot converge and saturates to the calibration limit. This demonstrates that the success of proposed TANC is due to the underlying calibration algorithm, rather than implementation details. Additional simulations showed that the proposed TANC can works with nonlinearities of conventional VS DTCs as well, indicating its usage is not limited to this particular DTC implementation.

The phase noise of IL-PLL output with 100 MHz input reference frequency is shown in Fig.3.26. The integer-N mode phase noise is shown along with fractional-N mode with both calibration ON and OFF. The DTC coarse stage nonlinearity is modelled with ±0.5 LSB INL, and the fine stage is modeled with +3 LSB INL. With the calibration, the nonlinearity induced spur and noise folding are greatly reduced, validating the effectiveness of proposed calibration.

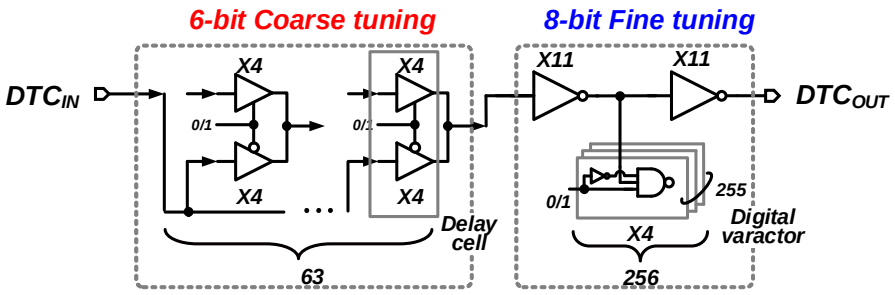


Figure 3.27: Implementation details of proposed two-stage PS-VS DTC.

3.4.4 Circuit implementation

The proposed fractional-N IL-PLL extended the integer-N design [67] by adopting a DTC on the reference path. Thus in this section only the proposed synthesizable two-stage PS-VS DTC and the true arbitrary nonlinearity calibration logic will be explained.

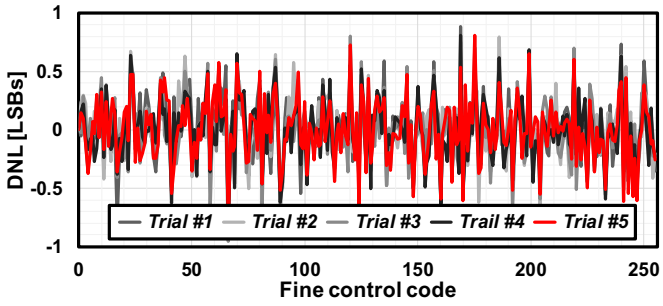
DTC implementation

In the present work, a two-stage DTC implementation was adopted, as shown in Fig. 3.27, and the details about delay and segmentation are summarized in Table 3.6. The coarse stage is a 6-bit PS design, and the fine stage is an 8-bit VS design. The coarse stage delay cells are implemented with tristate buffers, and the fine stage delay cell is implemented with NAND3 based varactors. The delay resolutions are approximately 28.6 ps and 0.24 ps for coarse and fine stages respectively. The 6-bit coarse stage could cover a range of approximately 1.8 ns to ensure a enough sufficient margin under PVT variations, while the 8-bit fine stage ensure sufficient overlap between coarse codes. Depending on phase noise and device mismatch requirements, the coarse stage and fine stage can be scaled up or down to achieve the best system performance.

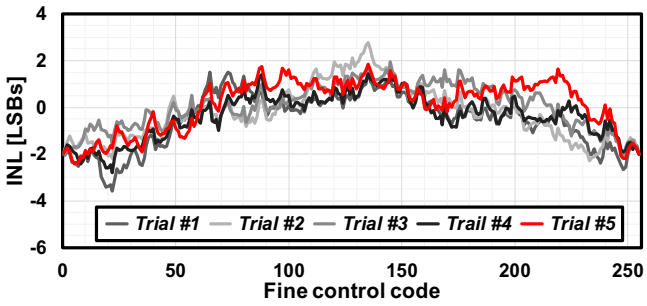
The DNL and INL of both coarse and fine stage DTCs are obtained from post-layout simulations, with 5 different P&R trials, and are shown in Fig. 3.28. Note that the coarse stage LSB is about 100 times that of fine stage. As evident from the plots, the nonlinearity of coarse stage PS DTC is dominated by DNL from device mismatch and automatic P&R. On the other hand, the fine stage VS DTC is rather smooth, and the systemic INL is similar to those custom-designed VS DTCs [8, 58].

DTC TANC implementation

The implementation of the DTC calibration logic is shown in Fig. 3.29. Both gain calibration and TANC were implemented. During the calibration, the gain calibration and



(a)



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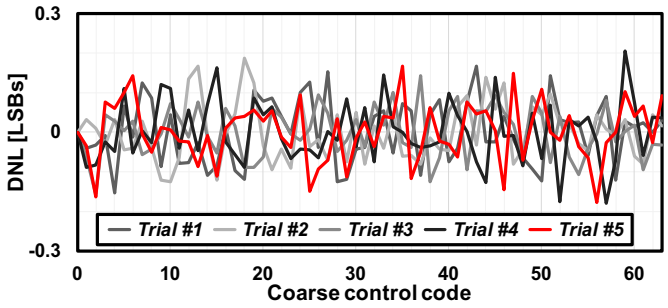
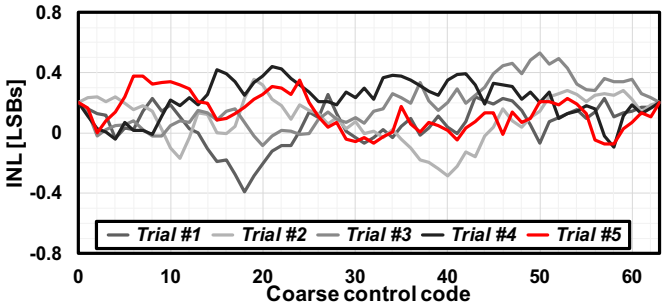
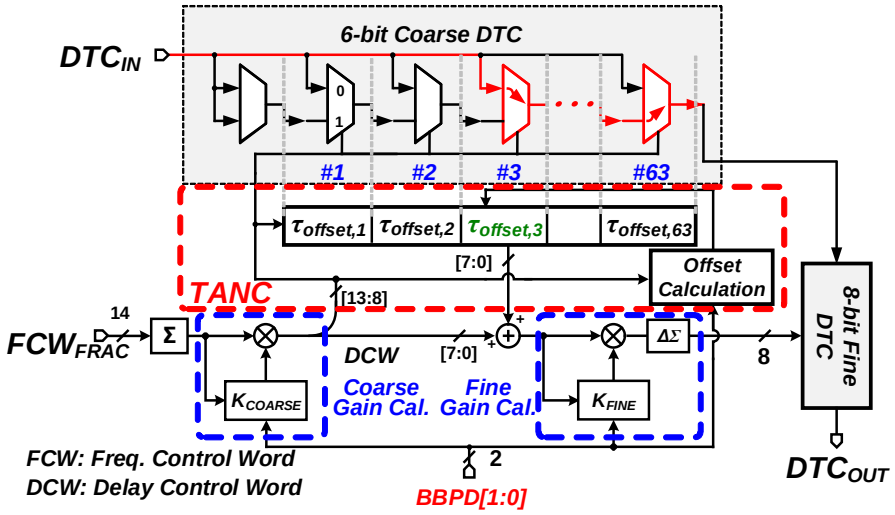


(c)

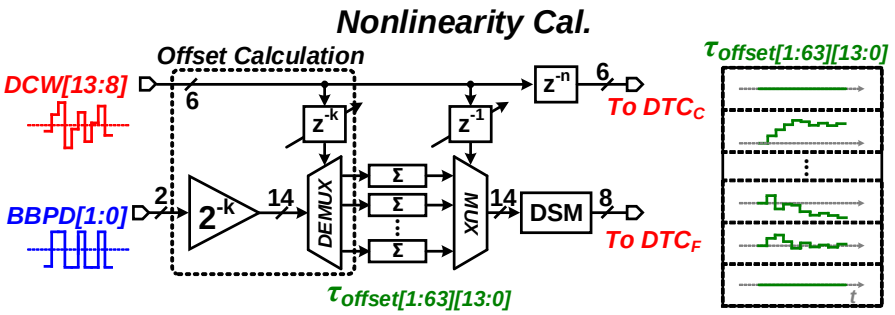


(d)

Figure 3.28: Two-stage synthesizable DTC nonlinearity characteristics under typical corner with 5 different automatic P&R trials, (a) DNL of fine stage and (b) INL of fine stage, (c) DNL of coarse stage and (d) INL of coarse stage. The DNL and INL are normalized to LSB of respective stages.



(a)



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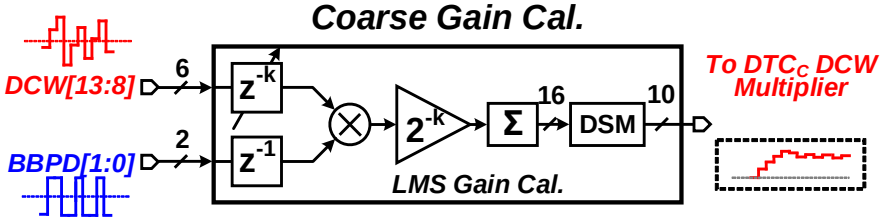


(c)

Figure 3.29: Implementation of DTC gain and nonlinearity calibrations, (a) system architecture, (b) TANC implementation and (c) gain calibration.

the TANC operate in parallel with different gain settings. The gain calibration would converge first, then the TANC would correct the INL while the DTC gain change incrementally. The input fractional FCW is first accumulated and then gain normalized by the least mean square (LMS) calibration block to get the DTC control word (DCW). The 6-bit most significant bits (MSBs) of DCW is applied to both coarse DTC and TANC, whereas the 8-bit least significant bits (LSBs) are added with the 8-bit TANC calibration code. The

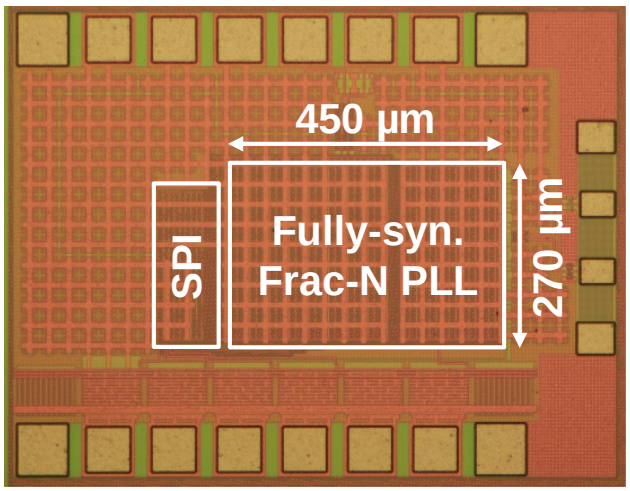


Figure 3.30: Die micro-graph of the fully-synthesizable fractional-N IL-PLL.

sum are further normalized by fine stage gain calibration, and applied to fine DTC.

To illustrate the time-domain operation, the LMS gain calibration of coarse stage are shown in Fig. 3.29(c). After proper delay alignment, the coarse DCW is multiplied by the BBPD output error to get the correlation, then the product is scaled, filtered and accumulated. When calibration converges, the result converges to a constant value, which is the optimal gain value. The scaling factor controls the convergence speed of the calibration loop, and to save implementation cost, shift shift operation is employed to realize the multiplication. The LMS gain calibration of fine stage has the same architecture, albeit with a different input DCW bit width.

On the other hand, the nonlinearity calibration need to supply a calibration value for each coarse code, therefore a look-up table (LUT)-based implementation is employed. For the input, the coarse DCWs are firstly delayed to align with BBPD output. Then the DCWs de-multiplexes the BBPD output to one of the LUT entries. Inside the LUT entries, the BBPD output are accumulated to obtain the calibration value. For the output, the coarse DCWs select the corresponding LUT entry, and the value is used as calibration value. Unlike gain calibration, the nonlinearity calibration logic provides each activated coarse stage control code a calibration value. To ensure proper data alignment, delays are inserted to compensate the loop latency and digital logic delays.

3.4.5 Measurement results

The entire IL-PLL is synthesized using commercial digital design tools with a non-modified standard cell library. The core area of the IL-PLL is 0.12 mm^2, which is fabricated in a 65 nm CMOS process. Fig. 5.8 shows the die photo. The phase noise is measured by a

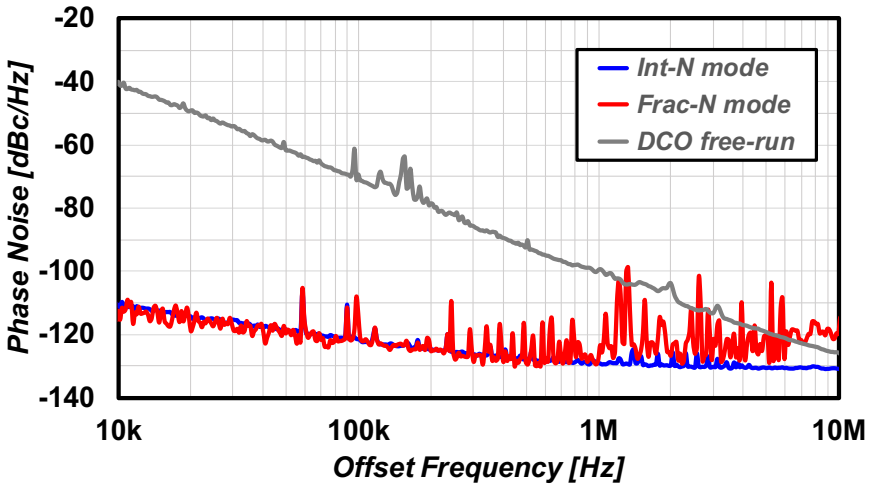
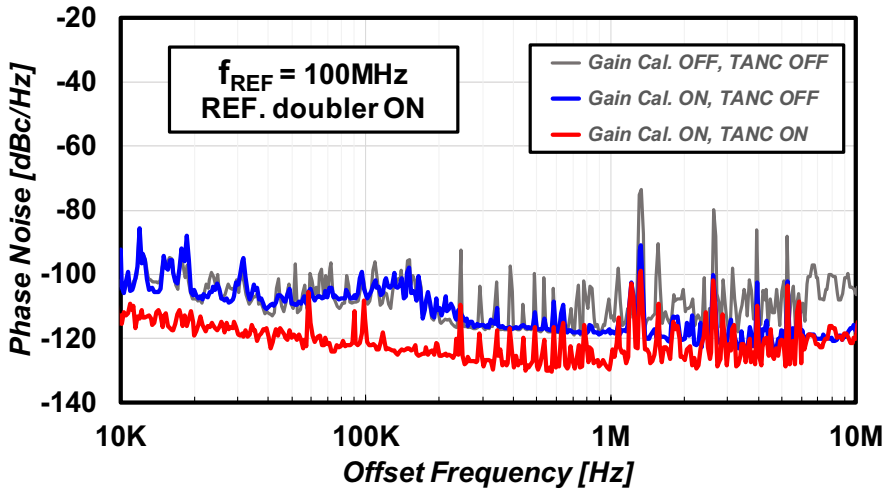


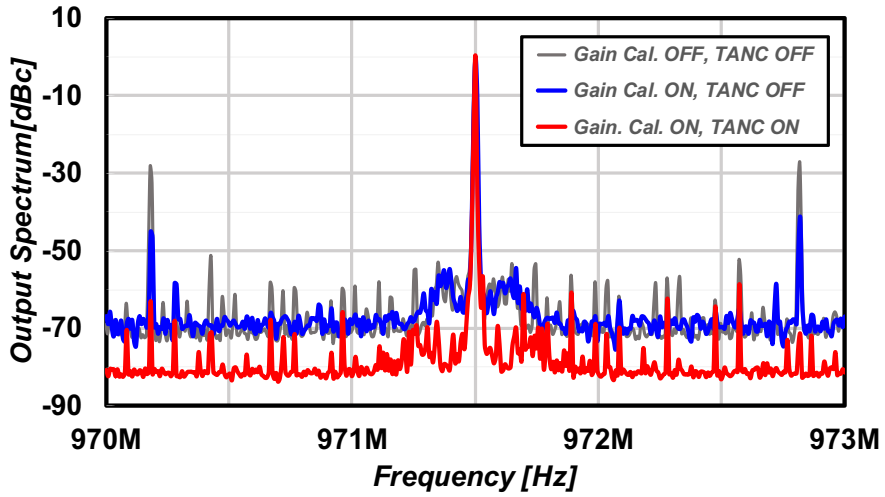
Figure 3.31: Measured phase noise in (a) DCO free-run mode (b) integer-N injection-locked mode and (c) fractional-N injection-locked mode.

signal source analyzer (Keysight E5052B), and the spectrum is measured by a spectrum analyzer (Keysight E4407B). Fig. 3.31 shows the measured phase noise with a 100 MHz reference clock. The IL-PLL achieves 0.3 ps jitter at 1 GHz output in integer-N mode, and 1.2 ps jitter at 971.24 MHz output in fractional-N mode, which is integrated from 10 kHz to 10 MHz. The power consumptions for these two modes are 2.2 mW and 2.5 mW, respectively.

The effectiveness of the proposed DTC gain calibration and TANC for INL calibration is demonstrated in Fig. 3.32. When both the gain calibration and TANC are off, the output has large fractional-N spur and high in-band phase noise. The integrated jitter is 12.9 ps, and the in-band fractional-N spur is higher than −30 dBc. When only DTC gain calibration is ON, the fractional-N spur is reduced to around −45 dBc, whereas the in-band phase noise is still high. Turning on the TANC in addition to the DTC gain calibration reduces the in-band phase noise and fractional-N spur. The measured fractional spur is −58.5 dBc at 1.0725 MHz offset, and the integrated jitter is approximately 1.2 ps. The effectiveness of proposed calibration is also evident from in-band fractional-N level in the corresponding spectrum, as shown in Fig. 3.32(b). Fig. 3.33 shows the fractional spur level with and without TANC. The worst case fractional-N spur after calibration is around −40 dBc. On average, the fractional-N spur improvement by TANC is approximately 10 dB, but it is frequency dependent. For a frequency offset approximately 1 MHz, the improvement is approximately 5 dB, and a 23 dB improvement is observed at approximately 6 MHz. The reference spur at 100 MHz frequency offset is about −45dBc. The larger than expected spurs could due to larger than expected DTC nonlinearity. Besides, the systemic INL



(a)



(b)

Figure 3.32: Measured fractional-N mode (a) phase noise and (b) spectrum with under three conditions: with (1) both DTC gain calibration and TANC off, (2) DTC gain calibration on, TANC off, and (3) both DTC gain calibration and TANC on.

of the fine DTC stages could increase the spur and noise level at high offset frequency. Therefore, additional nonlinearity calibration for fine stage would improve the IL-PLL performance. Nonetheless, current jitter and spur performance suffice applications such as digital clocking.

Table 3.7 and Table 3.8 summarize the measured performance of the proposed IL-PLL in integer-N and fractional-N modes respectively, along with the state-of-the-art PLL-s/MDLLs. The proposed IL-PLL achieves an FOM of -246.7 dB in integer-N mode,

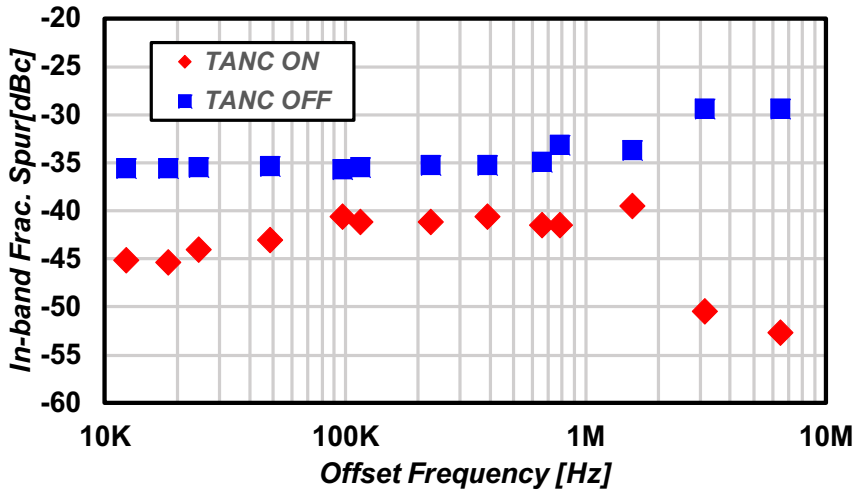


Figure 3.33: Measured in-band fractional-N spur versus frequency offset.

which is 5 dB better than the state-of-the-art [46]. The IL-PLL also achieves an FOM of −234.4 dB in fractional-N mode, which is 10 dB better than [44]. The measured worst case fractional spur is −40 dBc after the proposed TANC calibration. The proposed IL-PLL achieved the best results among the fully-synthesizable PLLs/MDLLs, and the results are comparable to those of custom-designed digital PLLs/MDLLs.

3.4.6 Conclusion

A fully-synthesizable fully calibrated fractional-N IL-PLL is presented in this paper. Based on noise and linearity analysis of different DTC architectures, a low-power, high performance synthesizable DTC is proposed and implemented, along with the proposed digital calibration optimized for the synthesizable design. The IL-PLL achieves 1.2 ps RMS jitter with 2.5 mW power consumption in the fractional-N mode, corresponding to FOM of -234.4 dB, which is 10 dB better than previous fully-synthesizable fractional-N PLLs/MDLLs.

3.5 Summary

In this chapter, the design of fully-synthesizable digital-intensive PLL is presented. With the proposed fully-synthesizable design methodology, high performance PLLs can be design with short time and small area. By employing injection-locking technique and the integrated digital background calibrations, low power high performance can be realized with area compact ring oscillators. The PLLs achieved excellent jitter-power FOM, and

Table 3.7: Performance summary and comparison with ring oscillator based integer-N IL-PLLs/MDLLs.

	JSSC'15 [35]	JSSC'19 [68]	JSSC'19 [69]	ISSCC'19 [41]	ISSCC'17 [46]	SSCL'18 [28]	**This Work**
	Custom-design				Fully-synthesizable		
Architecture	IL-PLL	ILCM	IL-PLL	ILCM	IL-PLL	TDC-PLL	IL-PLL
Freq. [GHz]	1.6~1.9	2.6~5.2	1.55~3.35	2.2~2.5	0.52~1.15	1.0~5.5	0.6~1.7
Ref. [MHz]	50	54	200	100	150	50	100
Integ Jitter. [ps]	0.47	0.366	0.292	0.14	0.42	4.71	**0.3**
Pdc [mW]/Freq. [GHz]	2.4@1.6	6.5@4.752	1.45@3.0	11.0@2.4	3.8@0.9	9.7@5.0	**2.2@1.0**
FOM* [dB]	-242.7	-239.4	-249.1	-246.7	-241.7	-216.8	**-246.7**
CMOS Tech.	65 nm	65 nm	28 nm	65 nm	65 nm	14 nm	65 nm
Area [mm^2]	0.09	0.16	0.0056	0.055	0.028	0.009	0.12
Ref. Spur [dBc]	-55.4	-53	-44	-72	–	-40	-45

* $\text{FOM} = 10 \cdot \log[(\sigma_t/1s)^2(P_{DC}/1\text{mW})]$

Table 3.8: Performance summary and comparison with DTC-based and synthesizable fractional-N PLLs/MDLLs.

	JSSC'14 [8]	JSSC'15 [35]	JSSC'16 [65]	JSSC'18 [36]	CICC'19 [54]	ISSCC'15 [44]	JSSC'19 [64]	**This Work**
	Custom-design					Fully-synthesizable		
Architecture	DTC + BBPD DPLL	DTC + IL-PLL	DTC + SSPLL	DTC + ILCM	DTC + IL-PLL	Soft-inj. IL-PLL	DI-TDC PLL	**DTC + IL-PLL**
Freq. [GHz]	3~4	1.6~1.9	10.1~12.4	6.75~8.25	1.6~3.0	0.8~1.7	0.1~2.01	0.6~1.7
Ref. [MHz]	40	50	40	115	100	380	80	**100**
Integ Jitter. [ps]	0.7	1.4	0.197	0.11	0.397	3.6	2.13	**1.2**
Pdc [mW]/Freq. [GHz]	4.2@3.6	3.0@1.7	5.6@11.72	3.25@7.36	2.5	3.0@1.5	6.95@2.056	**2.5@0.97**
FOM [dB]	-247.0	-232.3	-246.6	-254	-244	-224.6	-225.0	**-234.4**
CMOS Tech.	65 nm	65 nm	28 nm	65 nm	65 nm	65 nm	28 nm	65 nm
Area [mm^2]	0.2	0.09	0.25	0.27	0.0275	0.05	0.0043	0.12
Frac. Spur [dBc]	-51.7	-47	-56.6	-42.4	-51.5	–	-24	-40
Ref. Spur [dBc]	–	-55.4	-69	-52	-50	–	-52	-45
DTC Cal.	Gain +INL	Gain +INL	Gain +INL	Gain	Gain +INL	–	–	Gain +INL

very low fractional spur and reference spur performance, making them ideal for the use of low-power wireless transceivers.

Chapter 4

Fully-Synthesizable Digital-Intensive Sub-GHz IoT Transceiver

In this chapter a fully-synthesizable transceiver will be presented. With the digital-intensive design, the transceiver achieved record low power consumption with state-of-the-art sensitivity and EVM. Besides, the ring oscillator based design enables a very compact chip implementation, and could be much smaller with process scaling. With all the features, the proposed transceiver is ideal for low-cost IoT applications.

4.1 Introduction

Following the PLLs, the design of low-power digital intensive transmitter and receiver will be presented in this chapter. The low-power digital intensive transceiver is target for sub-GHz IoT applications. With AI-enabled edge computing, billions of intelligent IoT devices can be deployed, which promises revolution in various areas, such as health care, autonomous driving and industry automation. To enable such vision, a power, performance and area (PPA) optimized IoT transceiver is highly desired to have long operation time, low hardware cost with good performance. Besides, to leverage the increased computing power offered by the advanced technologies, digital intensive IoT transceiver that can be easily integrated into the SoC is highly valued.

Unfortunately, current sub-GHz IoT transceivers are highly inefficient in terms of P-PA, especially power consumption. Excellent performance are achieved at the expense of high power consumption, as shown in [9, 70, 71]. To reduce the power consumption, low power transceivers are proposed in [72–74]. However, large chip area are consumed due to the extensive use of inductors in oscillator and matching networks. On the other hand, small area and low power consumption are obtained with inductor-less transceiver

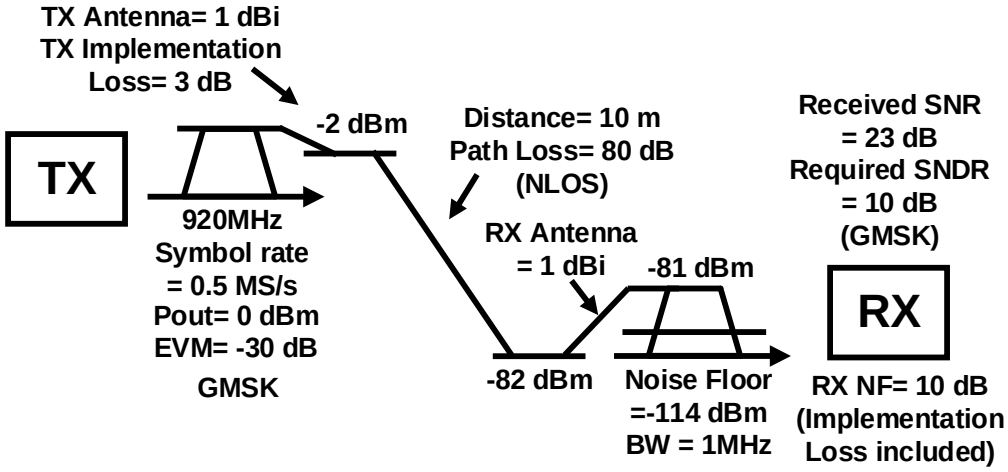


Figure 4.1: Link budget for proposed sub-GHz IoT network.

design, such as the transmitter in [75]. Yet the relatively poor PLL performance prevented its usage in the receiver side.

In this chapter, a low-power area-compact high-performance sub-GHz IoT transceiver is presented. The transceiver achieved excellent performance with low-power consumption with a small chip area. Besides, the transceiver features a digital intensive architecture in which the majority of the transceiver is described in HDL and can be synthesized with digital standard cells. This greatly eased the SoC system integration, and improved the design configurability.

To reduce the power consumption, a co-optimization of system architecture and circuit implementation is adopted. Besides, the transceiver mode switch time is minimized by novel frequency synthesizer and transceiver architecture. The transceiver achieved state-of-the-art performance in terms of EVM and sensitivity with digitally calibrated synthesizable analog designs. Besides, ultra-fast settling speed of frequency switch and transceiver mode switch was achieved. As for system power efficiency, an order higher system power efficiency at 0 dBm output power was achieved, making the transceiver ideal for short-range sub-GHz IoT applications.

4.2 System requirements and design considerations

To optimize for the best power, performance and area combination the required system specifications for each building blocks will be derived based on the target application. For a typical IEEE 802.15.4g standard compliant transceiver, the required system specifications are listed in Table 4.1. Because the standard employed GMSK modulation,

Table 4.1: Summary of the proposed IEEE 802.15.4g TRX specifications

Channel BW [kHz]	1000
Date rate [kbps]	500
Modulation	GMSK
RX Sensitivity [dBm]	≤ -81
RX ACR [dB]	≥30
TX EVM [dB]	≤-30
TX ACPR [dB]	≤30

which is a special kind of frequency shift keying (FSK), and is relatively insensitive to the amplitude errors. Thus the frequency synthesizer plays an important role in the system performance.

To quantitatively analyze the system requirements, Fig.4.1 shows a link budget for a transceiver for densely populated short-range indoor IoT networks. Both the transmitter and receiver implementation loss are 3 dB, and the antennas are omnidirectional designs with a 1 dBi gain. On the TX side, an EVM of -30 dB is assumed at the power amplifier output. The path loss is assumed to be 90 dB, accounting for the the complex transmission scenario in an indoor environment [76]. On the RX side, the RX bandwidth is assumed to be 1 MHz, and the NF is 7 dB. Therefore, the received signal has an SNR of 13 dB. On the other hand, to have an bit error rate (BER) less than 10^{-4}, the GMSK signal must have an Eb/No 13 dB. The required SNR can be calculated with

$$\frac{S}{N} = \frac{E_b}{N_0}\frac{R}{B_\mathrm{n}} \tag{4.1}$$

where B_n is the noise bandwidth of RX, R is the data rate. Thus, the required SNR is equal to 10 dB, and the proposed TRX has a 3 dB margin to guarantee the sensitivity.

4.2.1 Requirements for frequency synthesizer based transmitter

In this design, a PLL-based direct frequency modulation is used for transmitter. The PLL is configured to perform frequency modulation in the transmit mode, and re-configured to synthesize a single-tone carrier in the receive mode. Therefore, the PLL not only affect the transmitter performance, but also affect the RX performance. In the transmit

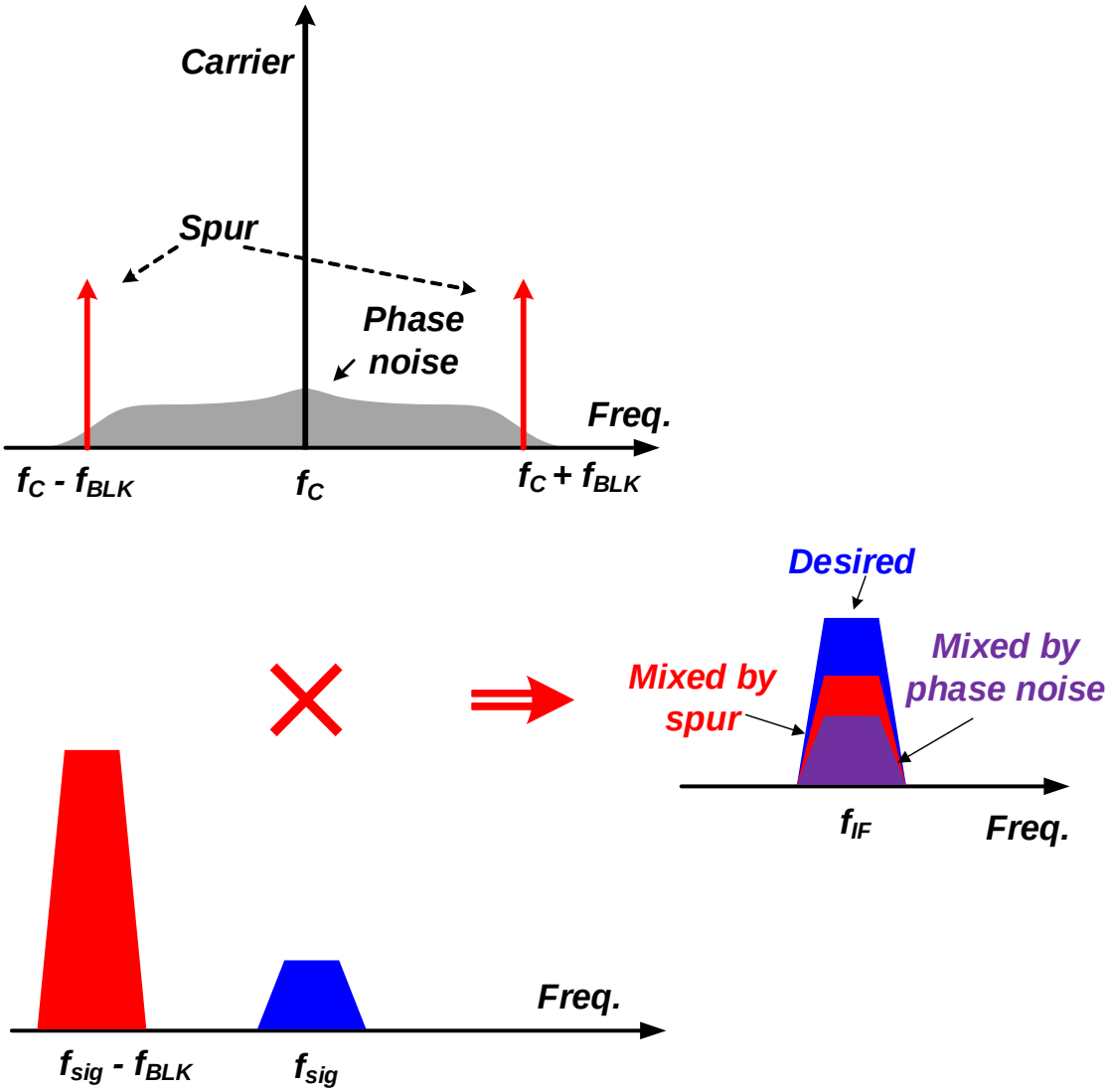


Figure 4.2: Concept of reciprocal mixing.

mode, specifications such as EVM, TX ACPR is considered. While sensitivity and ACR is considered in the receive mode. Among the various the specifications, the TX EVM and ACPR determines the frequency synthesizer on the TX side. While the reciprocal mixing and noise figure determines the requirement on the RX side.

For TX EVM, the required in-band EVM can be roughly estimated with the following equation.

$$EVM = 2\int_0^{f_{\mathrm{BW}}/2} \mathcal{L}(f)df \tag{4.2}$$

$$\approx \mathcal{L}_{\mathrm{inband}} \cdot f_{\mathrm{BW}} \tag{4.3}$$

where the f_{BW} is the EVM evaluation bandwidth, $\mathcal{L}(f)$ is the PLL phase noise. Assume the in-band phase noise is flat, the f_{BW} is lower than the PLL bandwidth, Eq. (4.2) can be simplified to Eq. (4.3). Plugging into the required EVM of -30 dBc, and f_{BW} of 1 MHz, the required in-band phase noise $\mathcal{L}_{\mathrm{inband}}$ should be lower than -90dBc/Hz.

On the other hand, the TX ACPR places requirements on out-of-band phase noise requirement. Assume the output-of-band emission is mainly contributed by phase noise, the required out-of-band phase noise $\mathcal{L}_{\mathrm{out-of-band}}$ can be estimated by

$$\mathcal{L}_{\mathrm{out-of-band}} = ACPR - 10\log10(f_{\mathrm{CH}}) \tag{4.4}$$

where the f_{CH} is the channel bandwidth. With the -35 dBc ACPR requirement, the out-of-band phase noise should be less than -95 dBc for frequency offset larger than 1 MHz.

On the RX side, the phase noise affect the sensitivity through reciprocal mixing, as shown in Fig. 4.2. Assuming the frequency synthesizer has the same phase noise performance in both TX and RX mode, the integrated in-band phase noise is less than -30 dBc, which is negligible compared to thermal noise. On the other hand, the ACR places significant requirements on the out-of-band phase noise requirement.

$$\mathcal{L}_{\mathrm{out-of-band}} = S_{\mathrm{desired}} - S_{\mathrm{blocker}} - SNR_{\mathrm{required}} - 10\log10(f_{\mathrm{CH}}) \tag{4.5}$$

where the S_{desired} is the desired signal power, S_{blocker} is the blocker signal power, $SNR_{required}$ is the required SNR for demodulation. With 30 dB ACR requirement at >3 MHz frequency offset, and 10 dB SNR_{required}, the $\mathcal{L}_{\mathrm{out-of-band}}$ needs to be lower than -100 dBc/Hz for >3 MHz frequency offset. Besides, the spur could also mixing down the blocker signal in a similar way, thus the required spur level can be calculated as:

$$Spur_{\mathrm{ACR}} = S_{\mathrm{desired}} - S_{\mathrm{blocker}} - SNR_{\mathrm{required}} \tag{4.6}$$

Therefore, the spur level need to be lower than -40 dBc.

Summarize up the requirements of both TX and RX, the PLL output phase need to be less than -90 dBc/Hz for frequency offset less than 1 MHz, and -100 dBc/Hz for frequency offset larger than 3 MHz. Meanwhile, the spur level need to be less than -40 dBc.

For this reason, the previous ring oscillator based frequency synthesizers are only applied to transmitters with relatively relaxed specifications [77]. All the previous ring oscillator based frequency synthesizers cannot meet the stringent phase noise requirement of receiver side. And the commercially products usually employed area consuming LC oscillator based designs to meet the phase noise requirements.

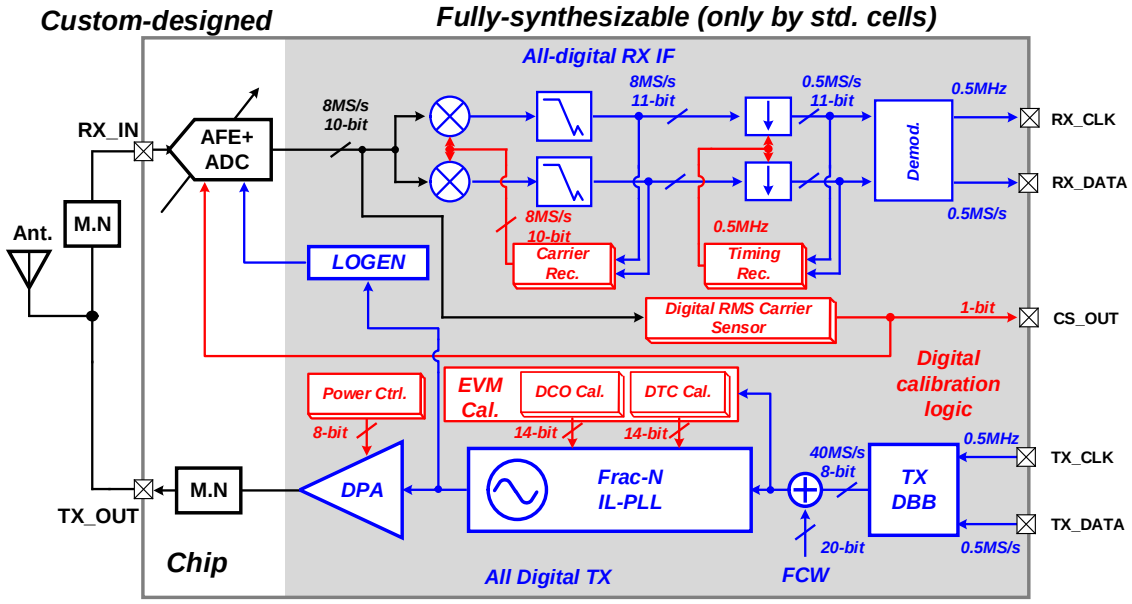


Figure 4.3: System diagram of proposed sub-GHz IoT transceiver.

4.2.2 Requirements for receiver

Aside from the frequency synthesizer, the transmitter and receiver need careful design to meet system specification. In this design, the transmitter only need to handle a low output power of less than 3 dBm, while greatly relaxed the transmitter design. On the other hand, the receiver need to have a high sensitivity and high linearity, thus a high performance RX is required. However, high performance is realized at expense at high power consumption and large area in conventional receivers. Conventional sub-GHz IoT receivers employ low-IF architecture, as a trade-off between flicker noise and image rejection. However, the low IF RX requires quadrature LO, complex filters and two ADCs, which are extremely area consuming considering the narrow bandwidth required. Besides, to reduce the effect of flicker noise, large devices with large power consumption are needed, incurring further power consumption.

In this this design, a heterodyne RX with all digital quadrature down-conversion and demodulation is employed. With the heterodyne architecture, only single-phase LO is required, relax the power consumption and routing complexity. Besides, both analog baseband filters and ADCs can be halved, saving significant area and power consumption. On the other, with the heterodyne architecture, the image rejection is introduced, which can solved by careful frequency planning and medium access control (MAC) protocol design.

An IF of 1 MHz is selected as a tradeoff between the flicker noise corner, blocker

rejection, power consumption and area. With 1 MHz IF, the band-pass filter has a 500 kHz low-pass cutoff frequency, and 1500 kHz high-pass cutoff frequency. Thus the corruption from flicker noise is minimized, and large capacitors can be saved. On the other hand, with 1 MHz IF frequency, and 1 MHz bandwidth, the image signal is located at 2 MHz lower than the desired signal. To avoid the image issue, channel carrier sensing is conducted before the real communication to assess the channel occupation, and the medium access control logic directs the such channel to be skipped.

Besides, the linearity requirement of the RX is derived. The overall required RX 3-rd input referred intercept point (IIP3) before ADC can be calculated as

$$IIP3 = \frac{3 \cdot P_{\mathrm{BLK}} - Sensitivity + SNR_{\mathrm{required}}}{2} \tag{4.7}$$

where the $Sensitivity$ is the reference sensitivity defined in the standards. In this design, with -48 dBm P_{BLK}, -81 dBm $Sensitivity$, and 10 dB SNR_{required}, the required IIP3 is -26.5 dBm. Therefore the overall receiver need to achieve -26.5 dBm in-band IIP3.

4.2.3 System architecture

Based on the system specifications, the system diagram of the proposed transceiver is shown in Fig. 4.3. The upper part shows the receiver, and the lower shows the transmitter. To reduce the power consumption and increase the design configurability, extensive digital calibrations are integrated. The majority of the transceiver is fully synthesizable design, which can be implemented with standard digital library. To facilitate the test, the transmitter output matching networks are integrated on-chip, and is power matched to antenna. Besides, the receiver matching network is realized as a combination of on-chip and off-chip components. Both of the TX and RX matching networks can replaced with off-chip implementation to further reduce the area consumption.

The all-digital transmitter is consist of digital baseband, PLL-based frequency modulator and the Class-D digital power amplifier. The receiver part is consist of an analog frontend, a successive-approximation-register (SAR) ADC, and all digital IF stage, which includes quadrature down conversion, sampling rate converter and demodulation. To simplify the LO signal routing, the LO signal is distributed from PLL to the receiver through a singled-end signal, and is recovered to differential signal locally at the mixer.

In this design, a ring oscillator based injection-locked fractional-N frequency synthesizer is employed. Due to the wide bandwidth offered by the injection locking, the phase noise of ring oscillator can be highly suppressed. Therefore, a high performance frequency synthesizer can be implemented with small area and low power consumption, while

Table 4.2: Comparison of Multi-stage and Single-stage TX DBB.

	Area [μm^2]	Power [mW]	SNR [dB]
Single-stage	53225	0.651	48.6
Multi-stage	22123	0.102	46.9

satisfying the stringent requirement for the receiver.

4.3 Circuit implementation

4.3.1 All-digital direct frequency modulation transmitter

The detailed transmitter implementation is shown in Fig.4.4(a). The TX DBB preforms GMSK modulation, and the output is added to the digital FCW to the frequency synthesizer, which act as a direct frequency modulator in the TX mode. Based on the analysis in Section 4.2, the frequency synthesizer need to have low phase noise to meet the EVM and ACPR specifications. Therefore, a low-power ring oscillator based fractional-N injection locked PLL is employed in this design. The fractional-N IL-PLL implementation is shown in Fig. 4.4(b), which is similar to the one presented in [19]. The fractional-N operation is realized with a DTC, and extensive digital calibration of DTC gain error, nonlinearity and oscillator frequency and phase error are integrated. Besides, with the integrated digital calibration, the modulation EVM can be calibrated in background, enabling realtime optimziation of modulation quality. And in order to reduce the out-of-band emissions, the non-overlapped self-clocked update scheme in Chapter 3 is employed to reduce the reference spur.

4.3.2 Power and area efficient TX DBB

The TX DBB implementation is shown in Fig. 4.5, which includes a modulator, a Gaussian pulse shaping filter, and interpolation filters. The interpolation filters are used to up-sample the modulation signal to reference clock frequency, and suppress the effect of image replicas. To save the power and area, a multi-stage multi-rate design is adopted. The modulator operates at 0.5 MHz, the Gaussian pulse shaping filter filter operates at 5 MHz, and the interpolation filter runs at 40 MHz. As shown in Table 4.2, compared to a single stage implementation, the proposed multi-stage multi-rate implementation save

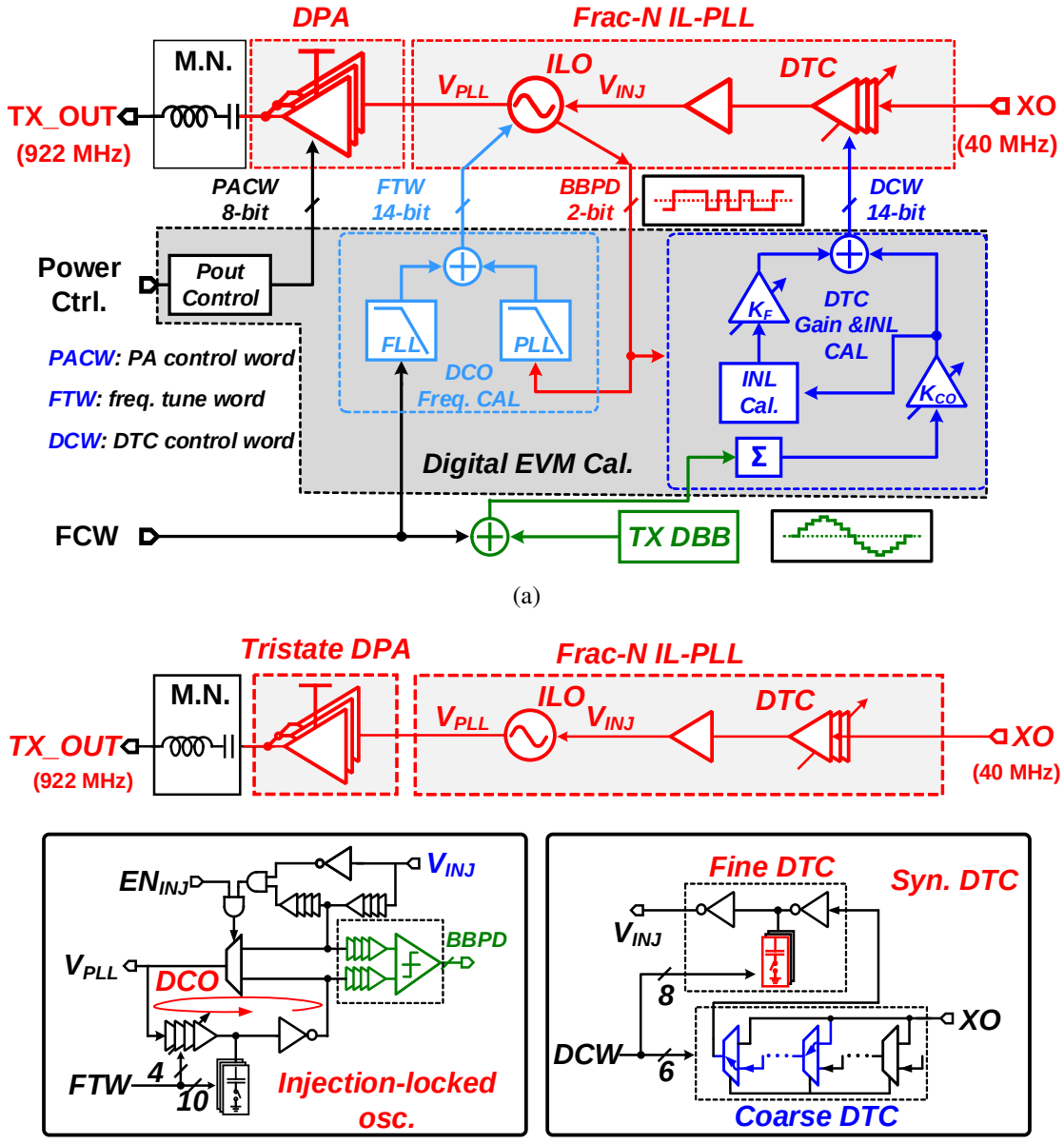


Figure 4.4: Proposed fully-synthesizable sub-GHz IoT transceiver (a) system diagram (b) circuit implementations.

more than 60% area and 80% power power consumption, while the SNR degradation is less than 2 dB. The GMSK output with the the proposed TX DBB is shown in Fig. 4.6. The multi-stage implementation only negligibly degraded the spectrum at around 2 MHz frequency offset, and still maintain excellent SNR across the band.

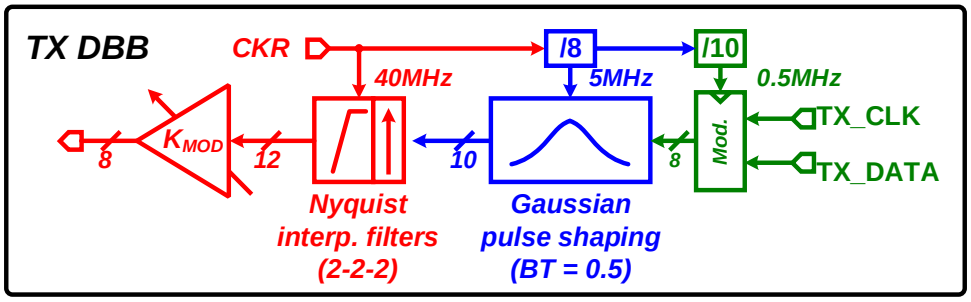


Figure 4.5: Proposed multi-rate multi-stage implementation of TX digital baseband .

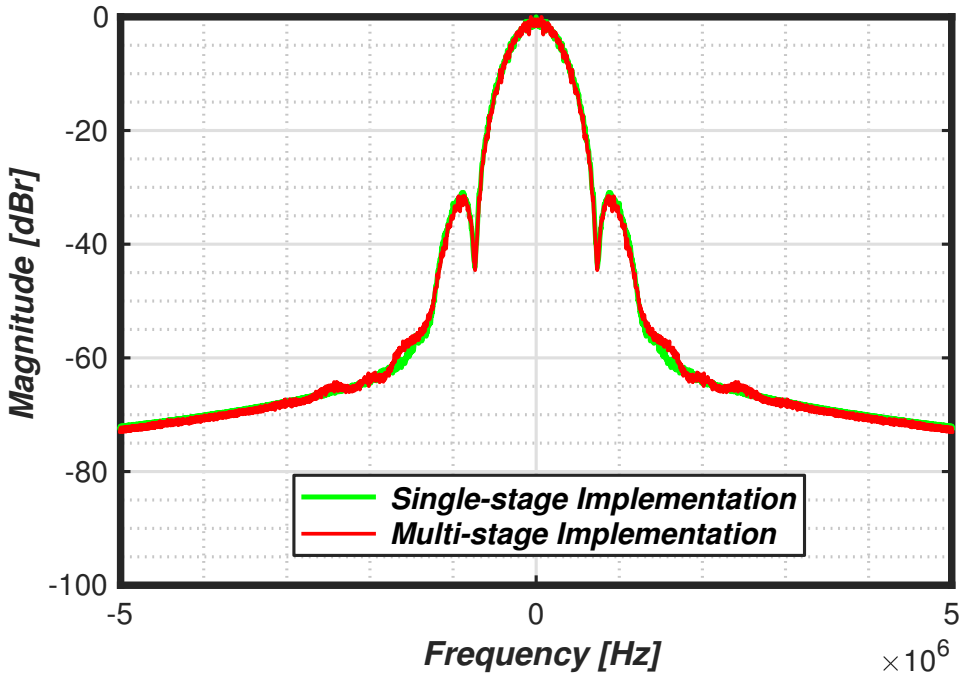


Figure 4.6: Comparison of proposed multi-stage pulse-shaping filter and single stage implementation.

4.3.3 PVT-robust digital intensive receiver

The block diagram of RX is shown in Fig. 4.7. The analog frontend includes low noise trans-conductance amplifier (LNTA), passive mixer, bandpass filter (BPF) and variable gain amplifier (VGA). The LNTA is a source degenerated design, and the matching network is realized with both on-chip and off-chip components. Both the BPF and VGA are implemented with flipped voltage followers, which are especially suitable for low supply design due to its high linearity [78]. The output of analog frontend is quantized by a 10-bit SAR ADC running at 8 MS/s, and further processed by the RX IF stage in the digital

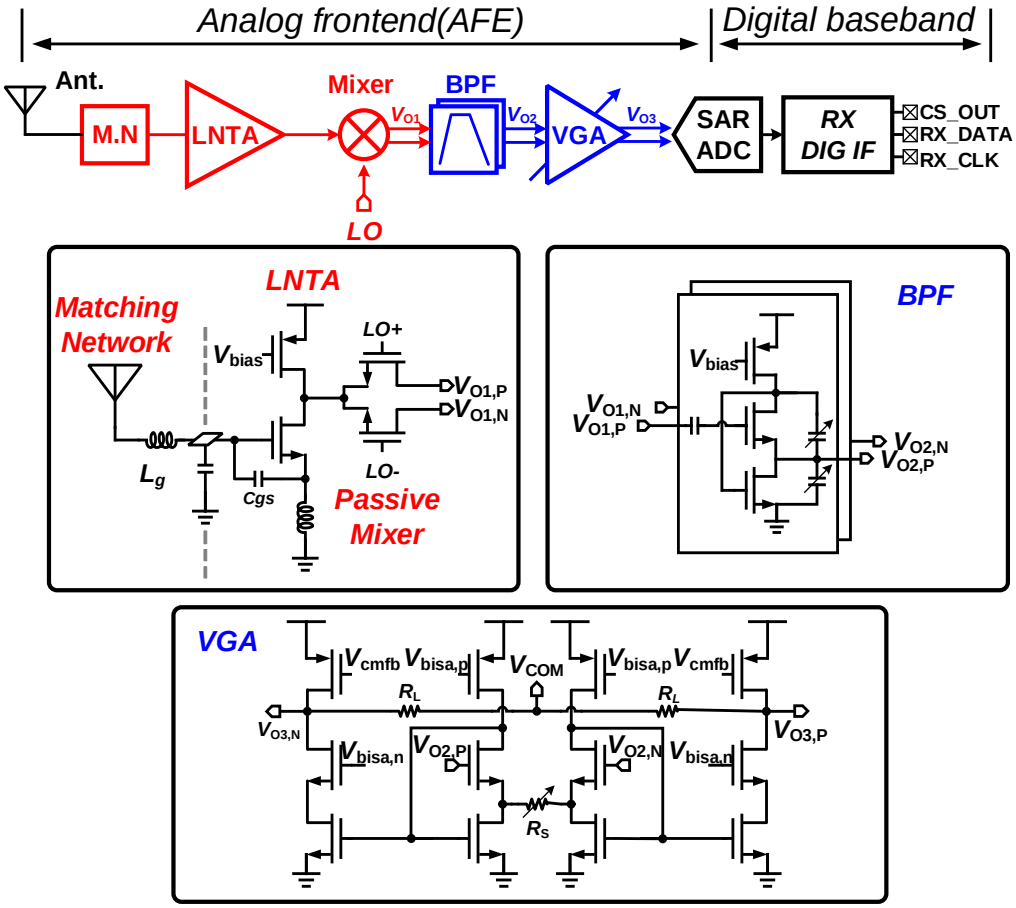


Figure 4.7: System diagram and circuit implementations of proposed digital receiver frontend.

domain.

Among the RX building blocks, the RX signal conditioning a lot of power and chip area, which performs narrow-band channel selection filtering. Both high signal rejection and low distortion is required. Conventional sub-GHz IoT transceivers employ continuous-time analog filters in the design. However, such analog filters are power and area hungry, and are difficult to implement in advanced technologies [79]. On the other hand, discrete time filters with have been proposed in [80, 81]. High configurability can be realized, and the implementation only requires switches and capacitors, making them friendly to process scaling. Yet large capacitor array are required, and the multi-phase clock generation consumed large power consumption. By combining of continuo-time and discrete-time operation, low sampling frequency can be used. Therefore, high power efficiency and configurability can be achieved [82]. However, the large area capacitor array is still needed.

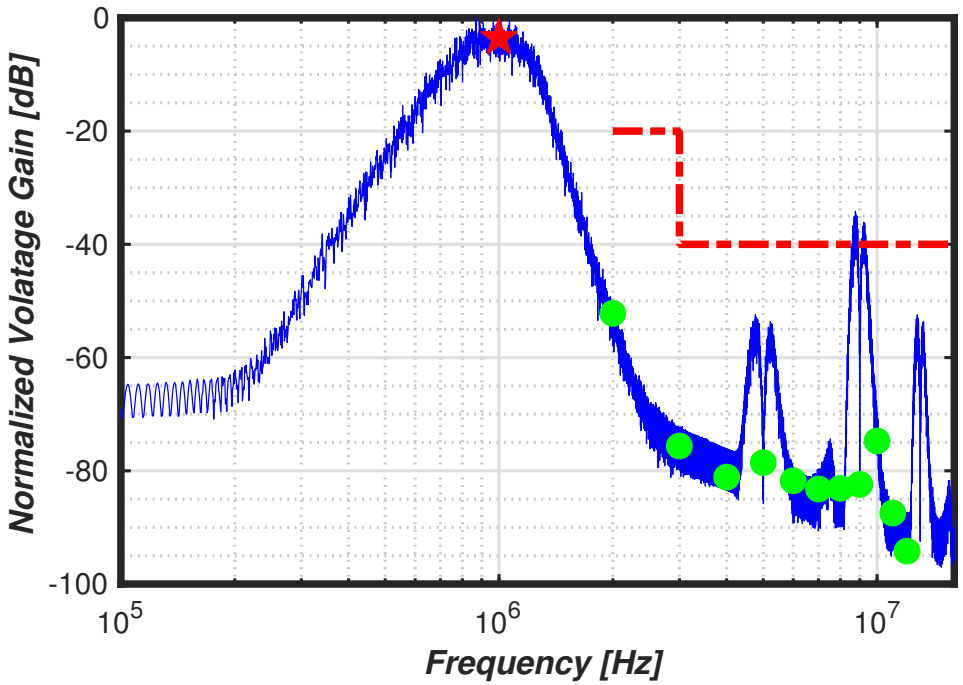


Figure 4.8: Frequency response of composite analog baseband and digital baseband.

In this design, the channel selection filtering is performed by a combination of analog and digital filters. In the analog domain, only simple 4th-order Butterworth filter was used to reduce the complexity. The rest of the signal filtering was performed in the digital domain, which is more flexible and area compact than analog filtering. In this design, the required channel filters need to have -20 dBr rejection at 1 MHz frequency offset, and -40 dBr rejection at $\geqslant$2 MHz frequency offset to meet the ACR specifications. Assuming the cut-off frequency is 0.5 MHz to avoid excessive signal loss, a 4th order low-pass is required. Such an analog filter would be extremely power and area hungry due to to narrow bandwidth, especially considering the PVT variations. To realize a low power signal conditioning, a hybrid of analog and digital filters were employed. In the analog domain, a bandpass filter with 4th-order high frequency roll-off and 2nd-order low frequency roll-off was employed. Following the analog BPF, the signal is digitized by a 10-bit SAR ADC and further processed by the digital filters.

The digital filters contains a high-pass infinite impulse response (IIR) filter which removes the DC offset and low frequency noise, and a two stage low-pass IIR filters with tunable bandwidth. The first stage low-pass IIR filters is designed with low latency to ensure the carrier recovery loop stability, whereas the second IIR was designed with high attenuation at blocker frequencies. The composite frequency response is shown in Fig. 4.8. For all the blocker frequencies, sufficient rejection is achieved to ensure the blocker is

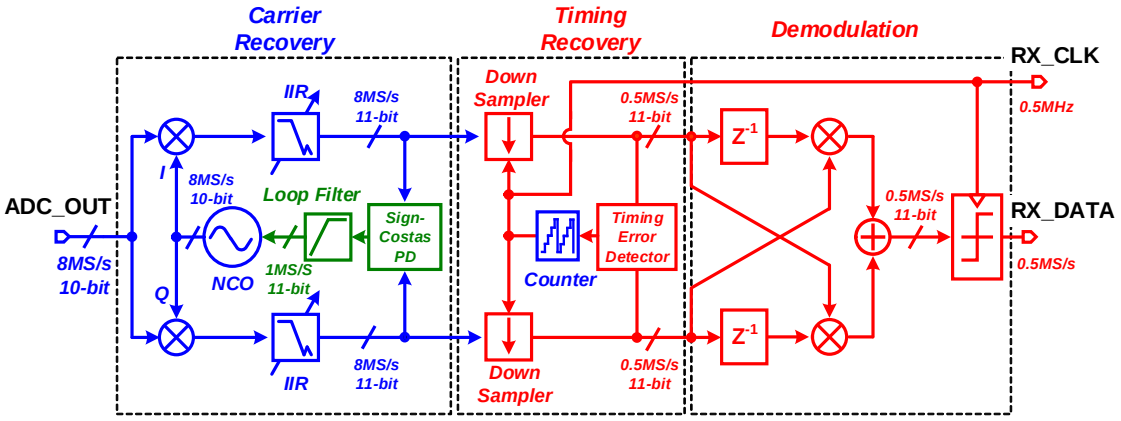


Figure 4.9: Implementations of RX digital IF stage.

at least 50 dB lower than the desired signal. To ensure robust operation, the analog BPF high frequency roll-off is realized with two flipped-voltage-follower (FVF)-based filters, and low frequency roll-off is realized by two 1st order passive RC filter. Thus the implementation consumes 0.15 mW powerm and is stable with ±10% supply variation, i.e. 1.08 – 1.32V.

4.3.4 All-digital RX IF stage

The detailed implementation of the RX IF stage is shown in Fig. 4.9. The DBB consists of three parts: carrier recovery, timing recovery and demodulation. Since the input digital signal is centered at 1 MHz, a precise quadrature LO is required to performed the down conversion. The such LO signal is recovered from input signal using the carrier recovery loop. The carrier recover loop features a multi-rate loop to reduce the power consumption and ensure stability. The quadrature downconversion mixer and tunable IIR lowpass filter run at 8 MS/s. The phase error is extracted with a sign-Costas phase detector. An integration-and-dump filter is cascaded after the phase detector to perform the filtering and down conversion from 8 MS/s to 1 MS/s. The digital loop filter of the carrier recovery loop runs at the 1 Ms/s, relaxing the latency effect on loop stability.

The timing recovery loop is responsible for decimate the signal from 8 MS/s to 0.5 MS/s. The optimal downsampling phase is generated with a Mueller-Muller timing error detector. After the decimation, the signal is demodulated with a one-bit difference demodulator, and sent to the external digital logic for further processing.

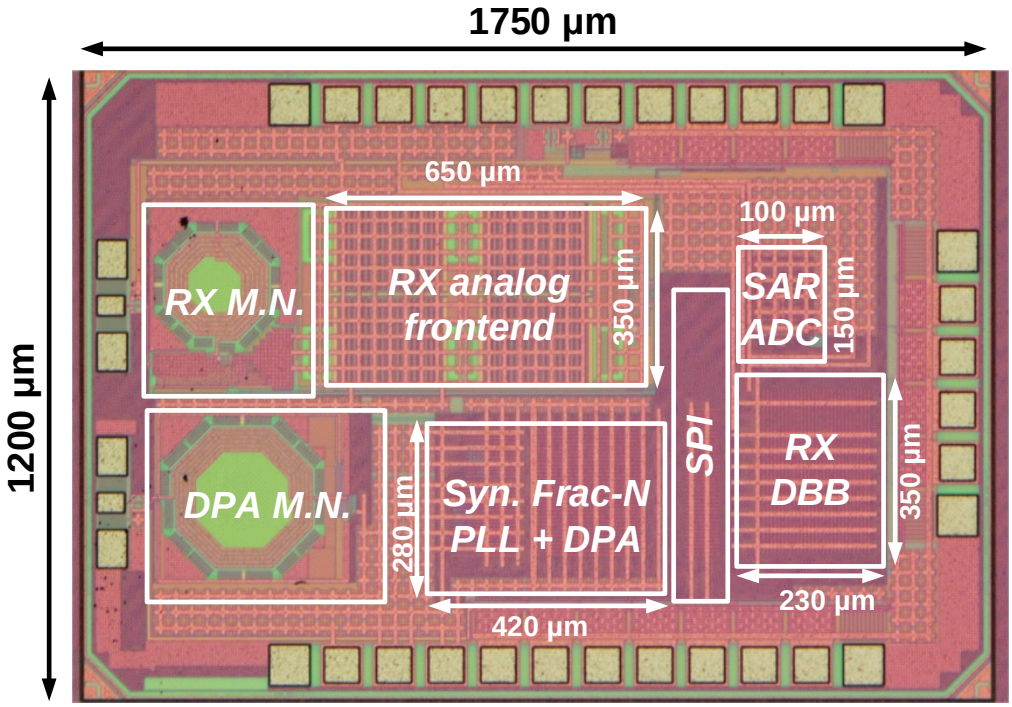


Figure 4.10: Chip Micrograph.

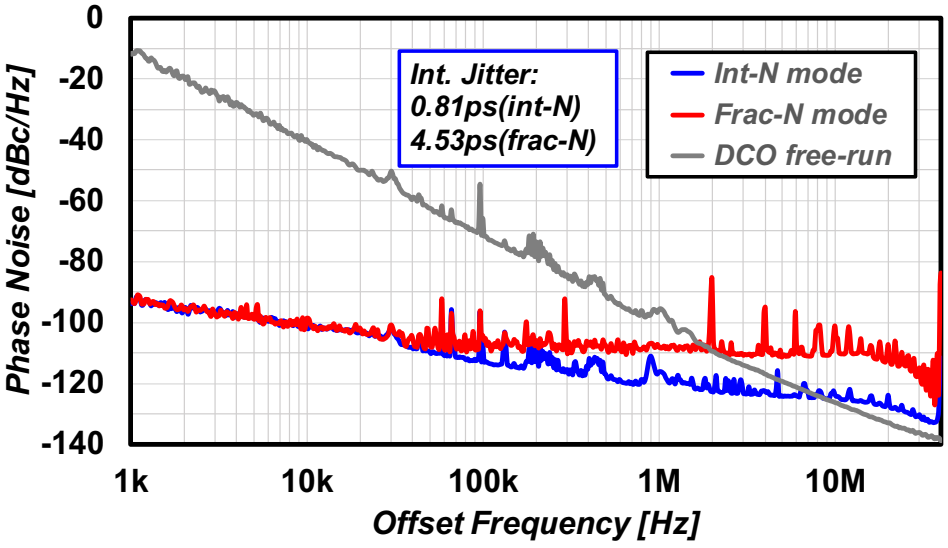


Figure 4.11: Measured phase noise of digital controlled ring oscillator and PLL.

Table 4.3: Area breakdown of proposed trasnceiver

Block	Area [mm^2]
TX (PLL+DBB+DPA)	0.42×0.28
RX frontend	0.65×0.35
ADC	0.15×0.1
RX DBB	0.35×0.23
TX M.N.	0.38×0.33
RX M.N.	0.37×0.28
Total	0.67
Total w/o M.N.	0.44

4.4 Measurement Results

The chip photo is shown in Fig.4.10. The design is implemented in a 65 nm CMOS process, with a total area of 2.1 mm^2. The area of each building blocks is summarized in Table 4.3, and the total active area excluding inductors is 0.44 mm^2. The PLL-based transmitter, RX IF stage and serial peripheral interface (SPI) control logic are combined together and fully synthesized with digital tools, with only foundry provided standard cells.

4.4.1 Transceiver measurement

PLL

The PLL phase noise is evaluated with the Keysight E5052B signal source analyzer. The measurement phase noise characteristic is shown in Fig.4.11. The spurs and noise bumps between 100 kHz and 1 MHz are caused by non-ideal grounding of the measurement equipment. The DCO consumes 1.0 mA under 1.2 V power supply, and the phase noise in the free-run mode is -98 dBc/Hz at 1 MHz frequency offset. With 40 MHz reference frequency, the PLL achieved -110 dBc/Hz phase noise at 1 MHz frequency offset in the fractional-N mode, which is lower than the -100 dBc/Hz phase noise requirement derived for ACR requirement. The integrated jitter from 10 kHz to 10 MHz is 0.8 ps and 4.53 ps for integer-N and fractional-N mode respectively, and the power consumption is 1.44 mW and 1.8 mW respectively. The in-band fractional-N spur is lower than -45 dBc across the whole operation band near 920 MHz, which ensures the LO spur is not the limiting factor

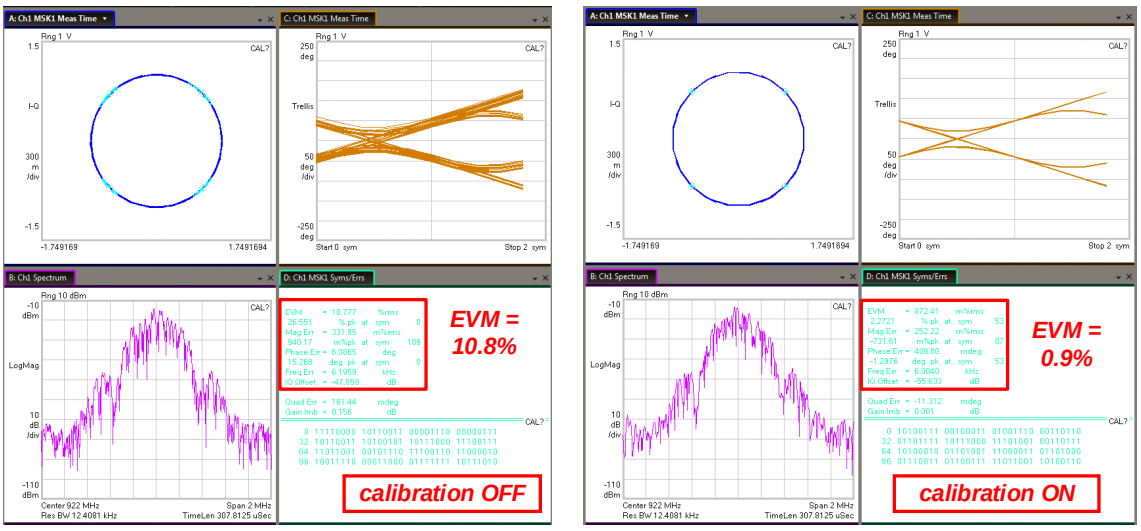


Figure 4.12: TX measurement results of EVM with calibration ON an OFF.

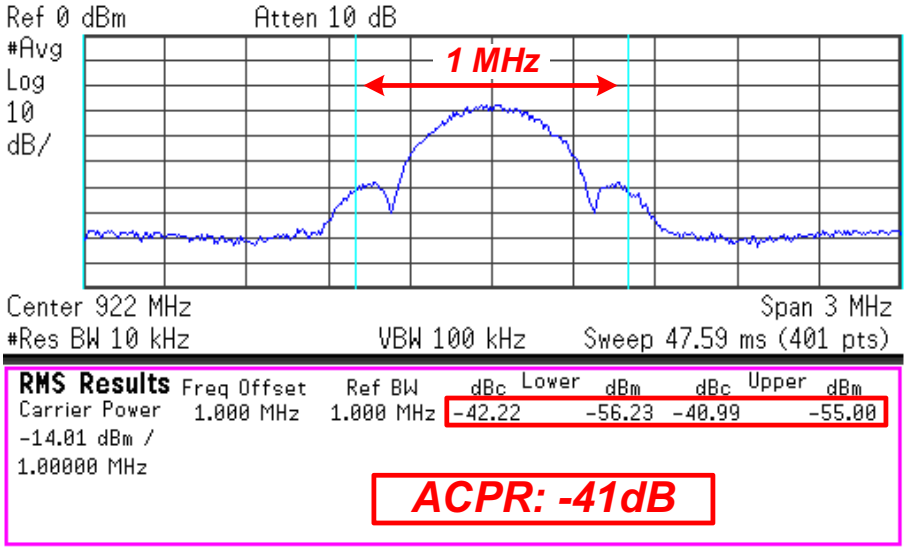


Figure 4.13: TX measurement results of ACPR.

for ACR. Note that in this design the PLL is over-designed to ensure sufficient margin for blocker rejection and sensitivity. Further power reduction is possible by reducing the phase noise performance of the ring oscillator.

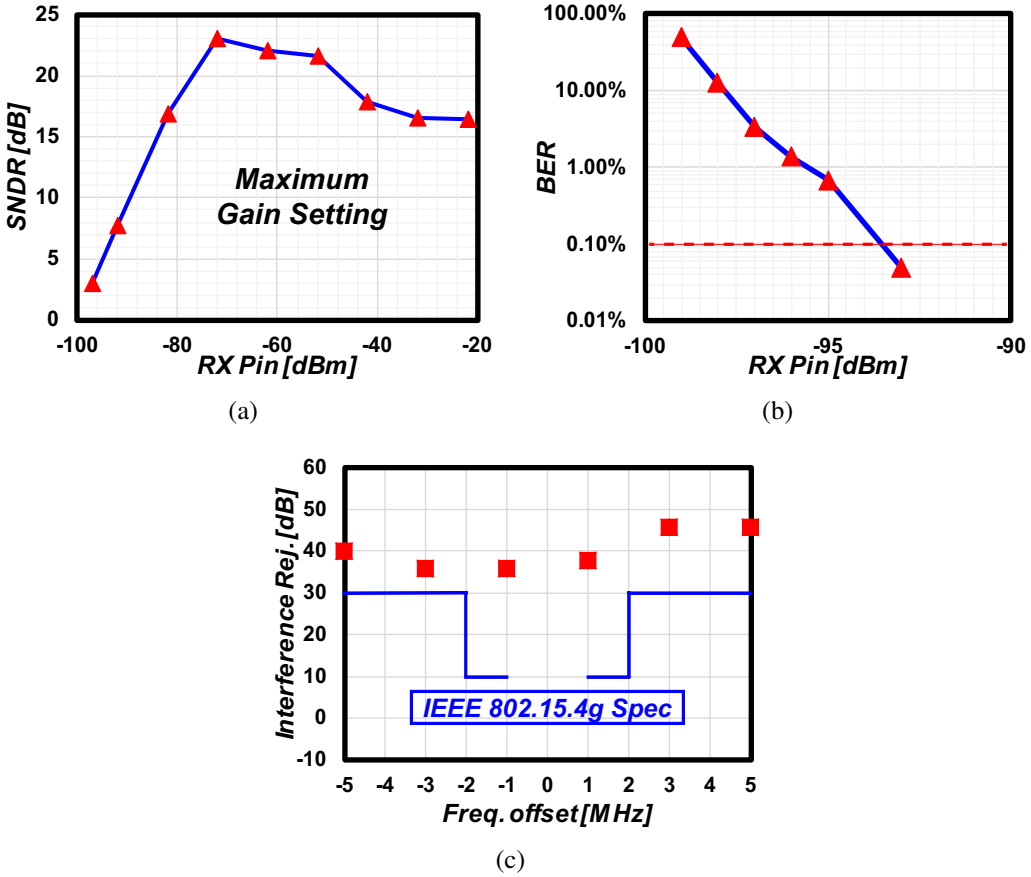


Figure 4.14: RX measurement results of (a)SNDR, (b)Sensitivity and (c)ACR.

Transmitter

The TX is tested with 500 kbps GMSK modulation, and the carrier frequency is 922 MHz. The EVM is measured with both digital calibration off and on the verify its effectiveness, as shown in Fig. 4.12. With the EVM calibration off, the EVM was about 10.8%. The EVM was reduced to about 0.9% after turn on the digital calibration. The ACPR measurement result is shown in Fig. 4.13. The measured ACPR is -41 dBc, which is 6 dB lower than the IEEE 802.15.4g specifications. The spectrum could also satisfy the ARIB STD-T108 spectrum mask, with more than 20 dB margin on both adjacent leakage emission and spurious emission requirements.

Receiver

The RX measurement results are shown in Fig. 4.14. The analog frontend SNDR was measured with a test signal before ADC. The test signal was captured by a Rhode&Schwartz

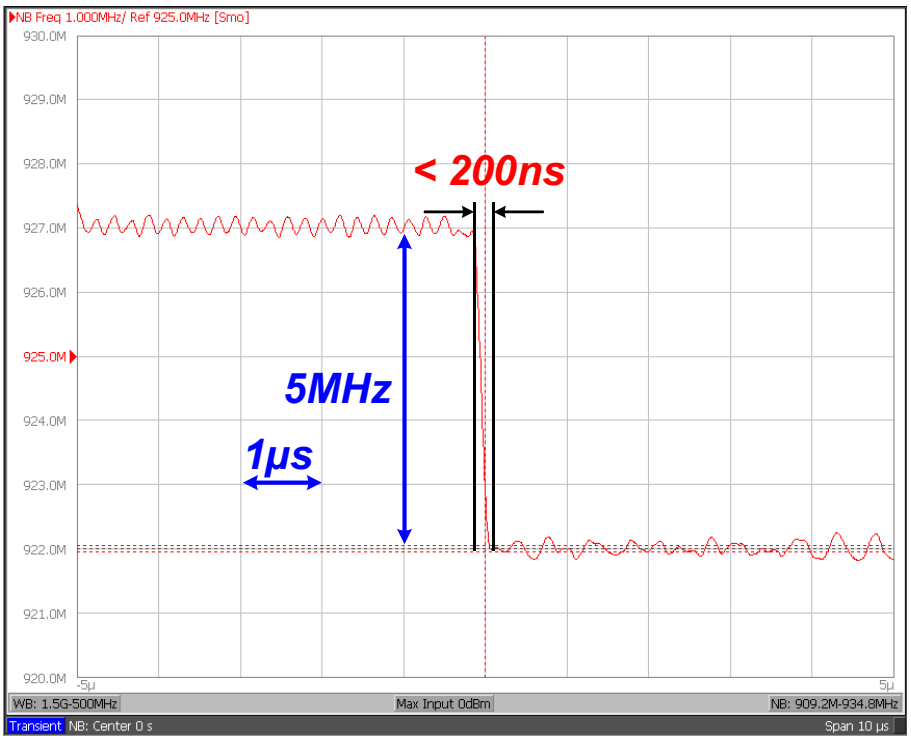


Figure 4.15: PLL settling behavior.

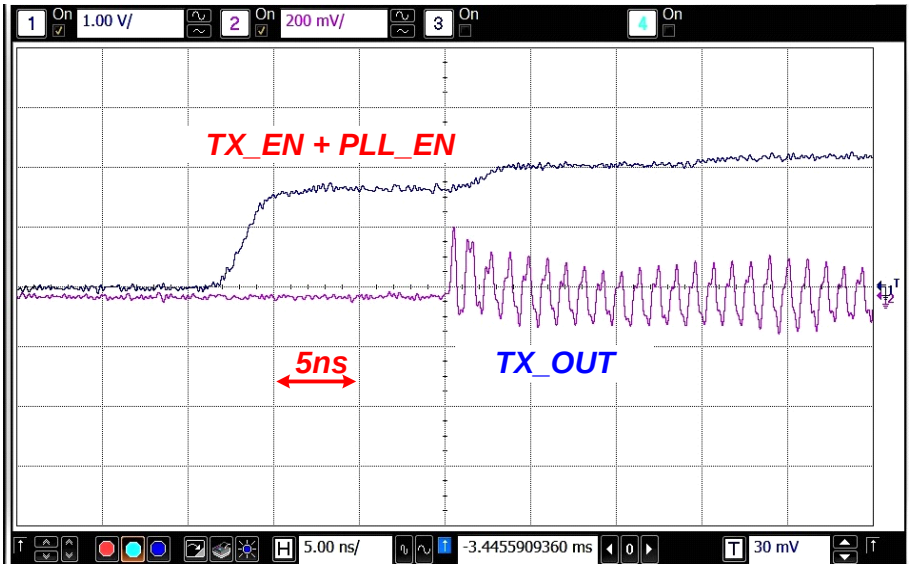


Figure 4.16: TX settling behavior.

RTO1004 oscilloscope with high impedance input, and the captured signal was post-processed in Matlab to calculate the SNDR. As shown in Fig. 4.14(a), the analog frontend SNDR linear increased with input power, and achieved a peak SNDR of 23 dB at -72 dBm

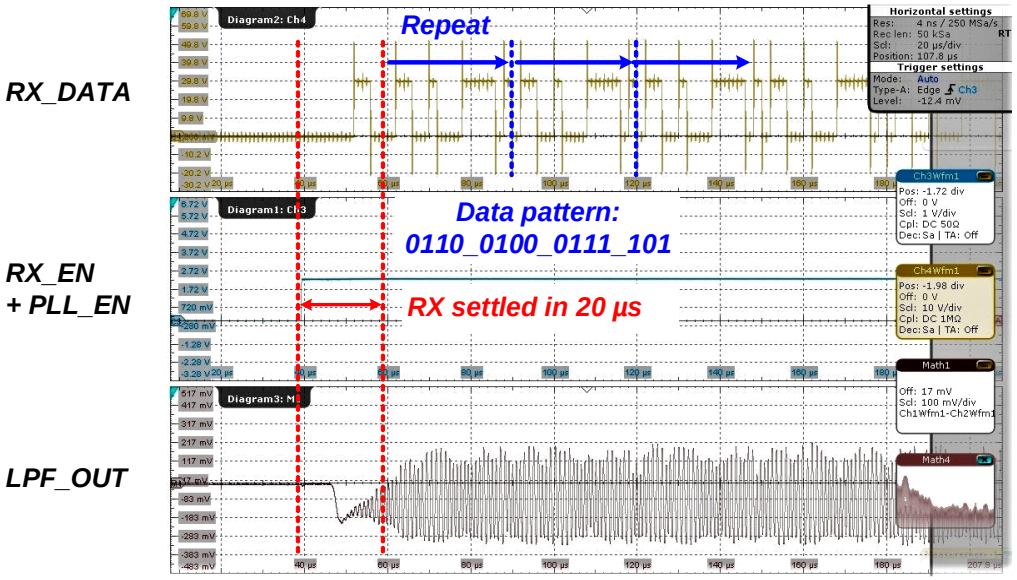


Figure 4.17: RX settling behavior.

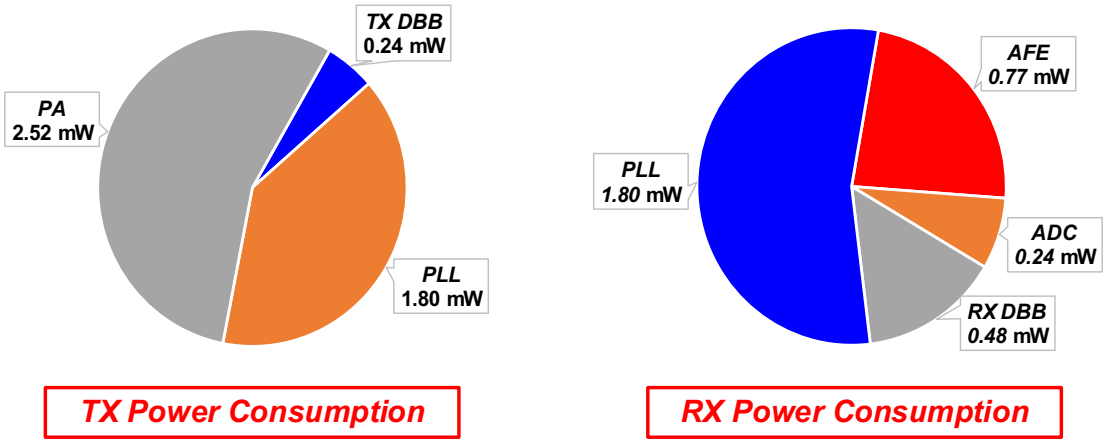


Figure 4.18: Power breakdown of sub-GHz IoT transceiver.

input power under the maximum gain setting. Further increase the input power caused reduced SNDR due to increased nonlinearity. Note that because the analog out buffer has a voltage gain lower than 1, the measured SNDR at the low power region is lower than the real value present to ADC. The sensitivity and ACR measurement results are shown in Fig. 4.14(b) and Fig. 4.14(c) respectively. Both RX sensitivity and blocker rejection are tested using modulated input under BER<0.1% without any forward error correction (FEC). The measured RX sensitivity is -94 dBm. The blocker rejection is 36 dB at 1MHz frequency offset, and satisfy the specifications of IEEE 802.15.4g standard.

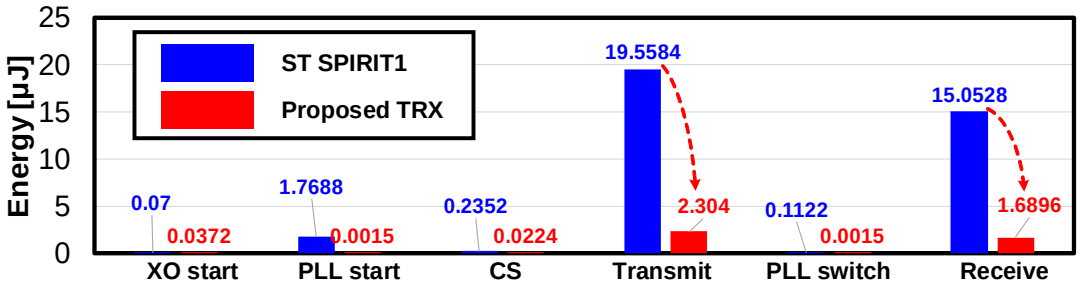


Figure 4.19: TRX power consumption of proposed TRX and a commercial product [9].

4.4.2 Transciver mode switch transient measurements

To check the transceiver transient performance, the setup time of each block is tested.

The PLL frequency settling behavior was tested with Keysight E5052B. Thanks to the wide bandwidth offered by the injection locking architecture, the PLL could settle within 200 ns for a 5 MHz frequency jump, as shown in Fig. 4.15. The TX startup behavior is shown in Fig. 4.16. The TX_EN signal and PLL_EN are controlled by the same external trigger signal, and the output waveform is captured by Keysight DSO91304A high speed oscilloscope. The TX output power settled in about 15 ns. The frequency settle behavior is measured by postprocess the captured data to a spectrogram. The measured frequency settle time was around 400 ns, which limited by the trade-off between FFT time-frequency resolution.

The RX settle behavior was measured by sending a signal of repeated pattern and observing the DBB output. As shown in Fig. 4.17, the total RX correctly settled in about 20 μs, in which the analog frontend startup in about 14 μs, and the digital IF stage takes 3 clock cycles to output the correct demodulated signal.

The power consumption of TRX is shown in Fig. 4.18. The TX total power consumption is 4.6 mW, and the RX total power consumption is 3.3 mW, both under nominal supply of 1.2V. The PA consumes 2.52 mW with 0 dBm POUT, achieving power efficiency of 40%. Thanks to the robustness offered by the digital intensive implementation, the TRX could operate normally with ±10% supply variation, i.e. from 1.08 V to 1.32 V. As shown in Fig. 4.19, compared to the commercial product [9], proposed TRX significantly reduced the active power consumption in transmit and receive mode, resulting a dramatic improvement in overall power efficiency.

The performance of the proposed sub-GHz IoT transceiver is summarized in Table 4.4, and compared against the state-of-the-art sub-GHz IoT transceivers in Table 5.3. The proposed transceiver is the first ring oscillator based synthesizable design. It achieves the

Table 4.4: Performance summary of proposed sub-GHz transceivers.

Architecture	PLL	Digital IL-PLL
	TX	Direct FM + Class-D DPA
	RX	Heterodyne + All-digital IQ IF
Modulation		GMSK/GFSK
Data rate		500 kbps
Standard Compliance		IEEE 802.15.4g/ARIB STD T-108
TX	EVM	0.9
	ACPR	-41 dBc (Ref. value: -35 dBc)
RX	RX BW	100 kHz
	Norm. Sens.	-94 dBm (Ref. value: -81 dBm)
	ACR	>36 dBc (Ref. value: 30 dB)

state-of-the-art TX and RX performance in terms of sensitivity and EVM, with 3.3/4.6 mW power consumption in RX and TX mode respectively. Besides, it achieves 21.7% system power efficiency at 0 dBm output power in TX mode, which is an order higher than previous designs.

4.5 Summary

This chapter presents a ring oscillator (RO) based sub-GHz IoT transceiver (TRX) in 65 nm CMOS. The TRX has a fully synthesizable fractional-N PLL, a digital FSK transmitter, and a heterodyne receiver with all-digital IF stage, and mostly can be described by HDL and designed by digital design tools. A ring oscillator based IL-PLL is employed as frequency synthesizer, and achieves 0.8/3.9 ps jitter in integer-N mode and fractional-N mode, all with 40 MHz reference frequency. The TRX achieves the state-of-the-art EVM of 0.9% and sensitivity of -94dBm, with 3.3/4.6 mW power consumption in RX/TX modes.

Table 4.5: Performance summary and comparison with state-of-the-art Sub-GHz Transceivers.

Ref		**This Work**	ADI ISSCC16 [71]	TI CC1310 [70]	ST SPIRIT1 [9]	CEA Leti ISSCC17 [83]
Process		65 nm	180 nm	-	-	65 nm
Area [mm^2]		2.1	12	-	-	3.8
Osc. Type		***Ring. Osc***	*LC*	*LC*	*LC*	*LC*
Synthesizable?		**Yes**	No	No	No	No
Modulation		GM/FSK	(G)M/FSK/OOK	(G)M/FSK/OOK	(G)M/FSK/OOK/ASK	DBPSK/GFSK
PLL	PN_{INBAND} [dBc/Hz]	-110@10kHz	-113@10kHz	-98@100kHz	-97@10kHz	-85@100kHz
	P_{DC} [mW]	1.1 (Int-N)/1.8 (Frac-N)	-	-	13.2	2.3(RX)/4.8(TX)
	Settle Time [μs]	**0.5**	-	-	60	-
TX	P_{OUT}(min/max) [dBm]	-30/2	-20/17	-/10	-30/11	-/14.7
	EVM	**0.9%**	0.8%	-	-	5%
	ACPR [dB]	-41	-84	-	-	-
RX	Data Rate [kbps]	500	2.4	500	500	0.1
	Norm. Sens. [dBm]	**-94**	-103	-98	-95	-96
	ACR [dB]	36	70	44	38	-
P_{DC}	RX [mW]	**3.3**	44	19.4	29.4	14.5
	TX [mW]	**4.6 (0 dBm)**	96.8 (13 dBm)	48.2 (10 dBm)	60 (11 dBm)	66 (10 dBm)
	TX w/o PA [mW]	**2.0**	-	-	13.2	10.3
	TX Sys. Eff.@0dBm	**21.7%**	2.5%*	2.9%*	2.4%*	1.9%*

* Assume PA peak power efficiency of 50%, and Class-B power back-off efficiency

Chapter 5

Digital-Intensive Differential Duobinary Modulator

With the advent of 5G cellular communication, mm-Wave frequency bands have attracted a lot of attentions. As a complement to the lower frequency band which has a larger coverage range, the license-free band around 60 GHz can be used for high-speed near-field-communication (NFC) [84]. The high data rate requirement, together with the limited battery power of mobile devices, necessitates a new design approach for power-efficient transceivers.

Based on whether or not pulse-shaping is employed, current 60 GHz transceivers can be divided into two categories. As shown in Fig. 5.1(a), conventionally the transceivers with pulse shaping were implemented as quadrature transceivers. The conventional quadrature transceivers, while being versatile in function, are power hungry due to the required wide-band signal conditioning [85], high-speed data conversion [86] and digital signal processing [87] at both transmitter and receiver side. Besides the RF frontends might require complex calibration to satisfy certain EVM limits dictated by modulation scheme [88–90], which incurs additional power penalty.

On the other hand, OOK transceivers with envelope detection can achieve very high power efficiency [91, 92] due to simplicity in architecture, yet the simple modulation not only limits the spectral efficiency, but also resulted in poor ACPR performance, which limits the usage of such transceivers.

In this paper, we propose a novel ultra-low-power modulator that enables an IEEE 802.11ad standard spectrum-mask-compliant ASK transceiver, as shown in Fig.5.1(c). Compared to conventional OOK transceivers, this design could achieve higher data rate with simple envelope detection while still meet the spectrum mask.

The transceiver system design is presented in Section 5.1. Circuit implementation

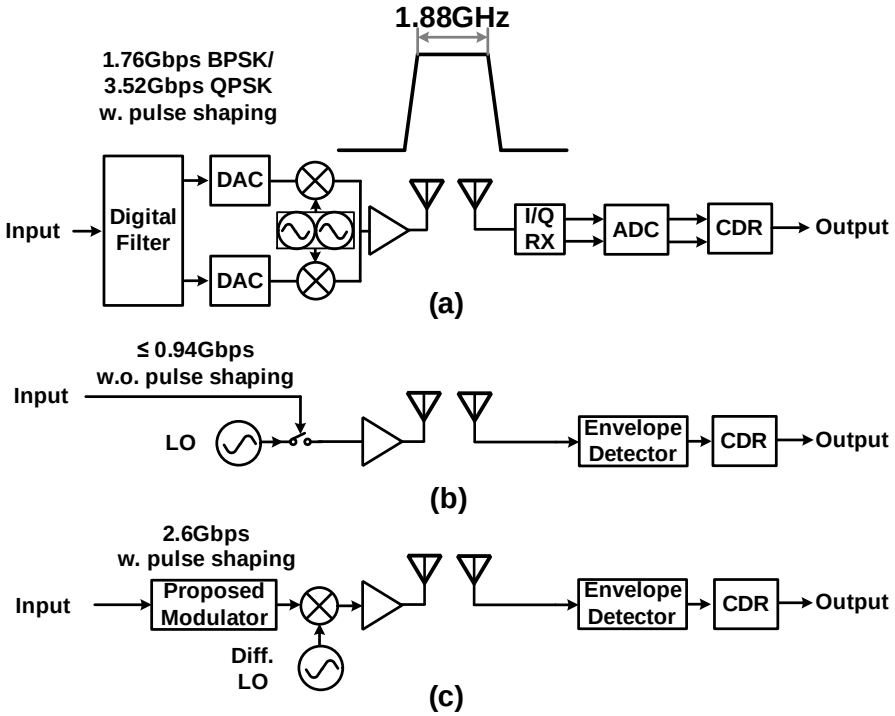


Figure 5.1: System block diagram and single-channel data rate of (a) conventional quadrature transceiver; (b) conventional OOK transceiver and (c) proposed pulse-shaped ASK transceiver.

of differential duobinary coder and semi-digital finite impulse response (FIR) filter are described in Section 5.2 and Section 5.3 respectively. Experimental results are explained in Section 5.4. Finally the paper is concluded in Section 5.5.

5.1 Modulator design for spectrum-mask-compliant ASK transceiver

It is commonly recognized that modulation format has a significant effect on transceiver's throughput and implementation complexity. While the throughput is mainly determined by modulation scheme and channel bandwidth, the power consumption is jointly determined by RF front-end, data converters and digital baseband.

Take a single IEEE 802.11ad channel as an example, which has a double-sided-bandwidth (DSB) of 1.88 GHz as specified by the standard [84]. On one hand quadrature transceiver can achieve 1.76 Gbps/3.52 Gbps data rate with pulse-shaped BPSK/QPSK modulation, and higher data rate with more complex modulation [86, 93, 94]. But the

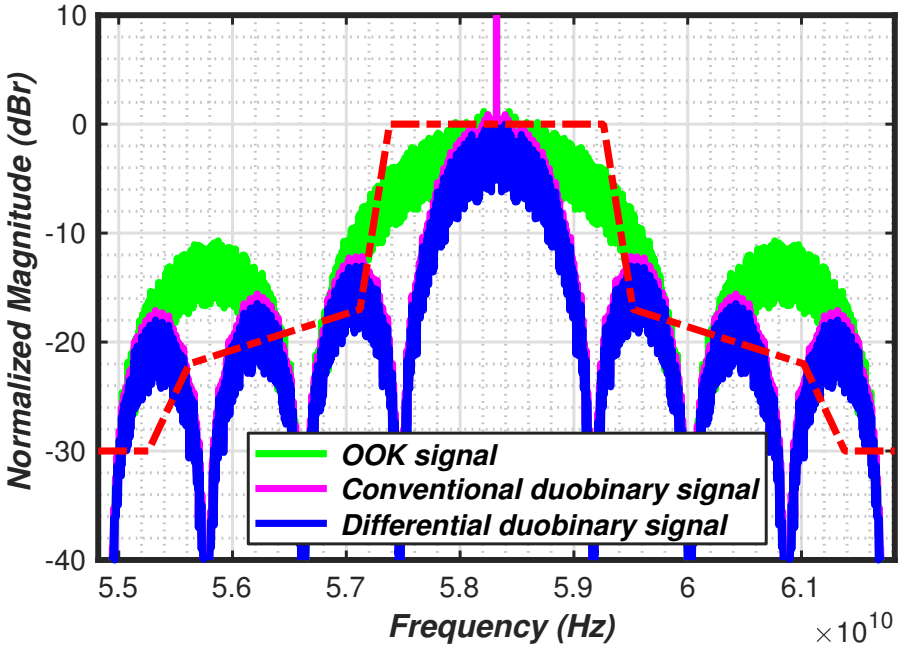


Figure 5.2: Normalized Power Spectral Density(PSD) of 1.7 Gbps OOK signal, conventional duobinary signal and differential duobinary signal.

high SNR requirement of complex modulation schemes necessitates carefully calibrated RF frontend, high speed and high resolution data converters and delicate synchronization and data recovery in the digital baseband [95], as shown in Fig.5.1(a). On the other hand, OOK modulation encode the symbol information by controlling the existence of signal. OOK transceivers can achieve very competitive power efficiency because of simplicity in architecture. Neither data converter nor modem is required in this architecture, as shown in Fig.5.1(b).

However OOK transceivers have their own problems. The green curve in Fig.5.2 is the output spectrum of an ideal OOK transmitter. The OOK data rate rate is 1.7 Gbps, and the carrier frequency is 58.32 GHz, the center frequency of the 1st channel of IEEE 802.11ad standard [84]. And the transmit mask IEEE 802.11ad standard is overlayed for comparison. From the graph two disadvantages of OOK modulation is evident. The first one is the poor ACPR performance. For OOK modulation, the spectral images are only attenuated by the $SINC$ response provided by zero-order-hold (ZOH) operation. But this is insufficient to meet the -30 dBr ACPR requirement of IEEE 802.11ad standard [84]. The second one lies in that OOK baseband signal has a non-zero DC component, which will introduce a LOFT in transmitter output. For the first problem, we can sacrifice data rate for better ACPR. For example, if we define the bandwidth of a non-return-to-zero (NRZ) pseudo-random bit sequence (PRBS) signal by the first PSD notch, the maximum achiev-

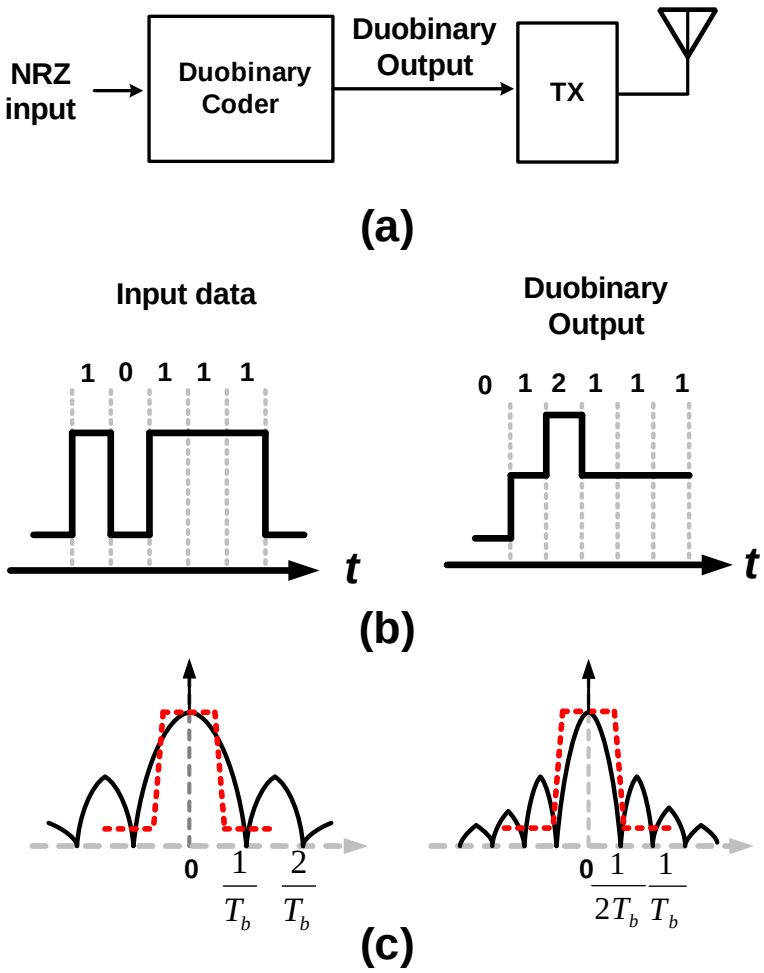


Figure 5.3: Illustration of conventional 3-level duobinary modulator (a) system block diagram; (b) time-domain waveforms; (c) frequency spectrum.

able data rate is 0.94 Gbps, while the actual value could be even lower if spectrum mask compliance is strictly required.

In [96] a duobinary modulator was proposed. The duobinary coding could theoretically halve the occupied bandwidth. Fig. 5.2 shows the conceptual spectrum of duobinary modulation with an ideal up-converter. The carrier frequency is set to 58.32 GHz, which is the one of channel center frequency specified by the IEEE 802.11ad standard. However the LOFT problem still exists, as shown in Fig. 5.3. Besides, the signal has 3 levels, thus simple envelope detector and comparator are not enough, resulting in more complexity in receiver. Also the side-band still could violate the spectrum mask if no additional filtering is applied.

To summarize, one ideal ultra-low-power (ULP) transceiver should have pulse-shaped

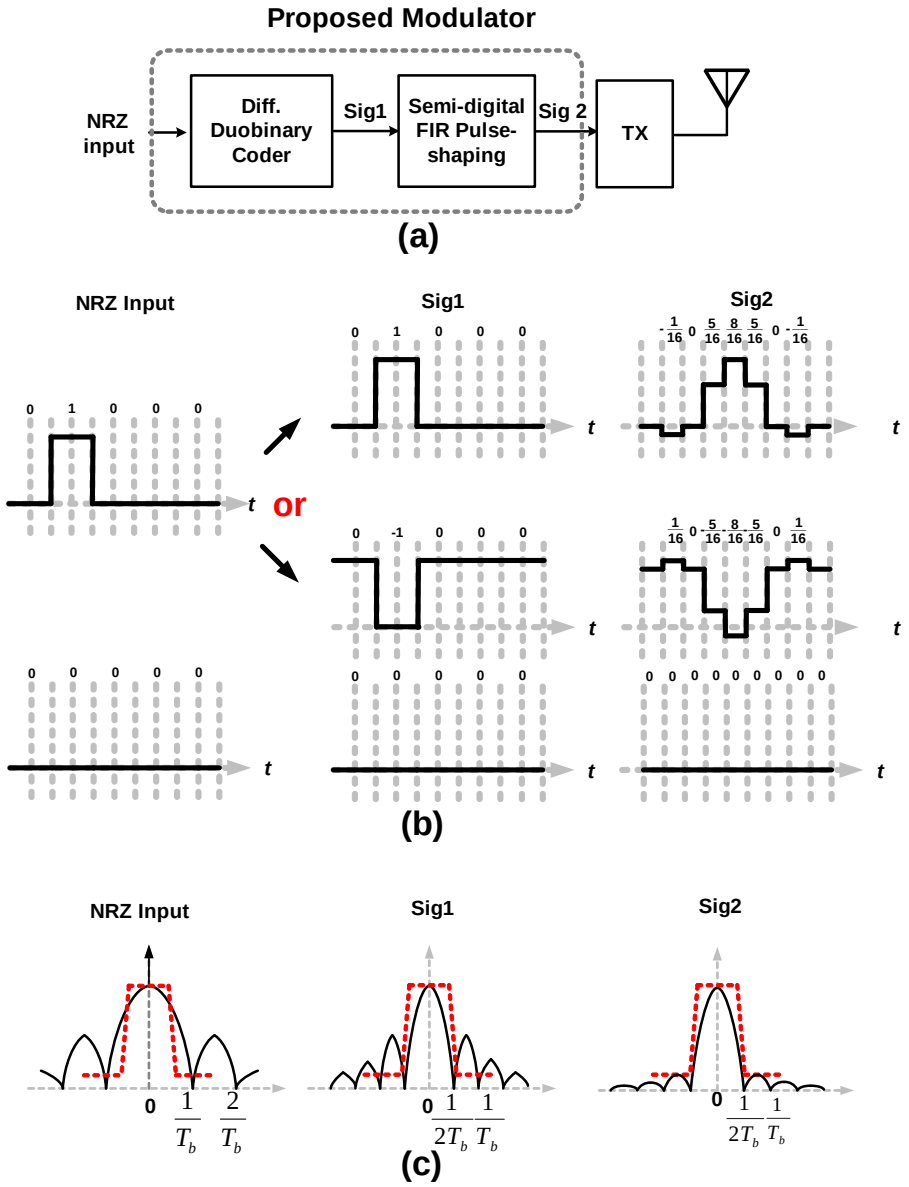


Figure 5.4: Proposed pulse-shaped differential duobinary modulator (a) system block diagram; (b) time-domain waveforms; (c) frequency spectrum.

output signal without any LOFT, so that spectrum mask can be satisfied. On the other hand, the transmitted signal should be demodulated incoherently, so that simple receiver can be employed to reduce power consumption. So the total power consumption can be minimized.

Fig. 5.4 shows our proposed modulator. The transmitter consists of differential duobinary coder and semi-digital FIR pulse-shaping filter. As shown in the figure, the input symbol 0 is converted to symbol 0 at output, while the input symbol 1 is converted to

either symbol +1 or symbol −1 depending on the preceding symbols [97]. Because the DC component is zero, the LOFT is eliminated, as shown in Fig. 5.2. On the other hand, this coding process only changes the phase of input symbol 1, but the amplitude is remain unchanged, so this duobinary signal can still be received by a simple envelope detector. To provide additional filtering and reduce inter-symbol-interference (ISI), a pulse-shaping filter is cascaded after the differential duobinary coder. Conventionally this pulse-shaping filter is implemented as an digital FIR filter. In our design, we observe that the inputs are two binary data streams which only have level 0 and level 1. Therefore semi-digital FIR filter is employed to reduce power consumption.

5.2 Differential duobinary coder: theory and implementation

The differential duobinary coder implementation is shown in Fig. 5.5. It consists of duobinary precoder and encoder, of which the transfer functions are listed below.

$$H_{\text{precoder}}(z) = \frac{1}{1 + z^{-1}} \tag{5.1}$$

$$H_{\text{encoder}}(z) = 1 + z^{-1} \tag{5.2}$$

From transfer function, the precoder has a feedback, which poses a stringent timing requirement when data rate is high. As shown in Fig. 5.6(a), the precoder is implemented by performing an XOR operation of input data and delayed output. This implementation requires the sum of the D flip-flop delay and XOR delay to be equal to the bit period, i.e.

$$T_{\text{b}} = T_{\text{D->Q}} + T_{\text{XOR}} \tag{5.3}$$

where T_{b} is the bit period, $T_{\text{D->Q}}$ is the D flip-flop delay and T_{XOR} is the XOR gate delay. Fig. 5.6(b) illustrates another precoder implementation, which is used in [98]. The precoder is consisted of an AND gate followed by a modulus-2 counter. The AND gate is used to generate edge transition during each data period. Its correct operation requires the falling edge of data trails the falling edge of clock, so the phase margin is about half

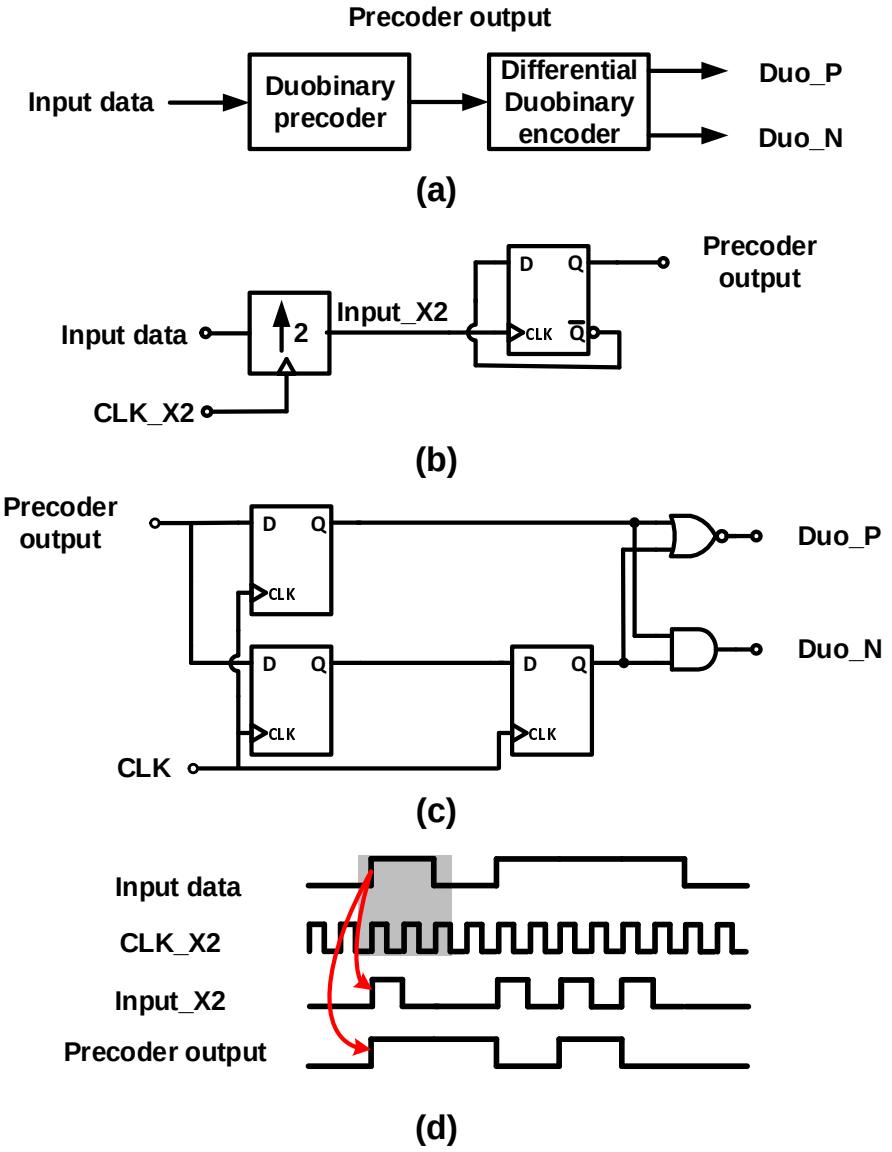


Figure 5.5: Differential duobinary coder (a) system block diagram; (b) schematic of duobinary precoder; (c) schematic of differential duobinary encoder; (d) timing analysis of precoder.

data period, i.e. 180°. Additional clock-data-recovery (CDR) circuit is needed to align the data and clock.

In our design, an over-sampling implementation of precoder is employed, as shown in Fig. 5.5(b). The proposed precoder consists of a ×2 up-sampler and a modulus-2 counter. Because the clock frequency is twice of data rate, edge transition can be reliably generated during each data period. And the ×2 up-sampler does not require data-clock alignment as long as metastablilty is avoided. Besides, unlike the precoder proposed in Fig. 5.6(b),

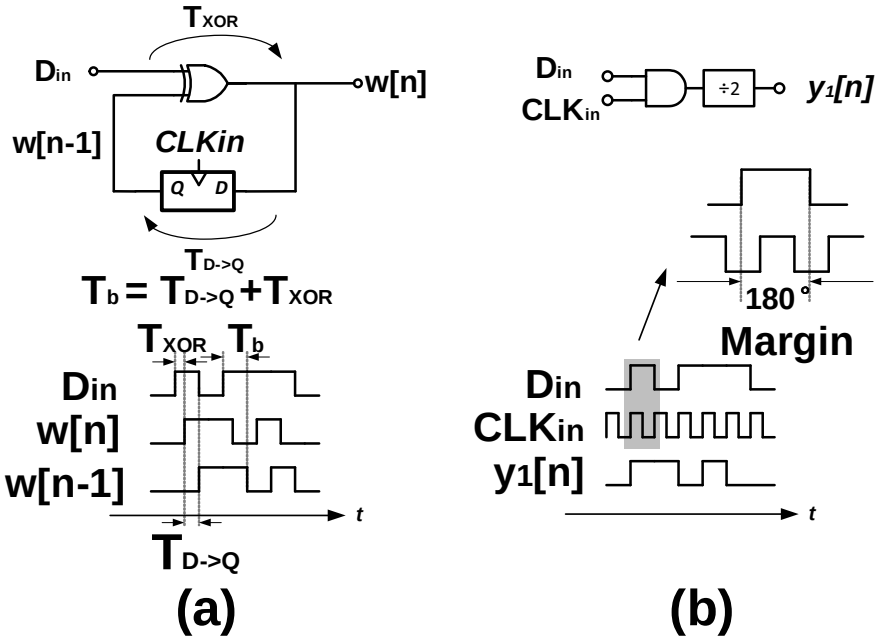


Figure 5.6: Conventional duobinary precoder (a) feedback based implementation; (b) counter based implementation.

which operates on signal level, the proposed precoder is edge trigged, thus is more robust to external noise. Notice that the oversampling clock is re-used from semi-digital FIR filter, therefore this arrangement does not require any extra clock.

The differential encoder implementation is shown in Fig. 5.5(c), which consists of only digital standard cells. The two outputs Duo_P and Duo_N are binary signals which only has level 0 and 1. And the difference of the two signals, Duo_P − Duo_N, is a signal with 3 levels. The mapping relationship between Duo_P − Duo_N and input NRZ signal is shown in Table 5.1, and this relationship ensures signal envelope does not change after duobinary coding process.

Both precoder and differential encoder are implemented with standard cells, and are optimized across different PVT conditions to ensure robust operation. The pure digital implementation also means this design has good scalability, and can achieve higher performance with more advanced technologies.

5.3 Semi-digital FIR filter design

To further suppress the side band of differential duobinary output, a raised-cosine(RC) pulse-shaping filter is introduced after differential duobinary coding. Compared to other

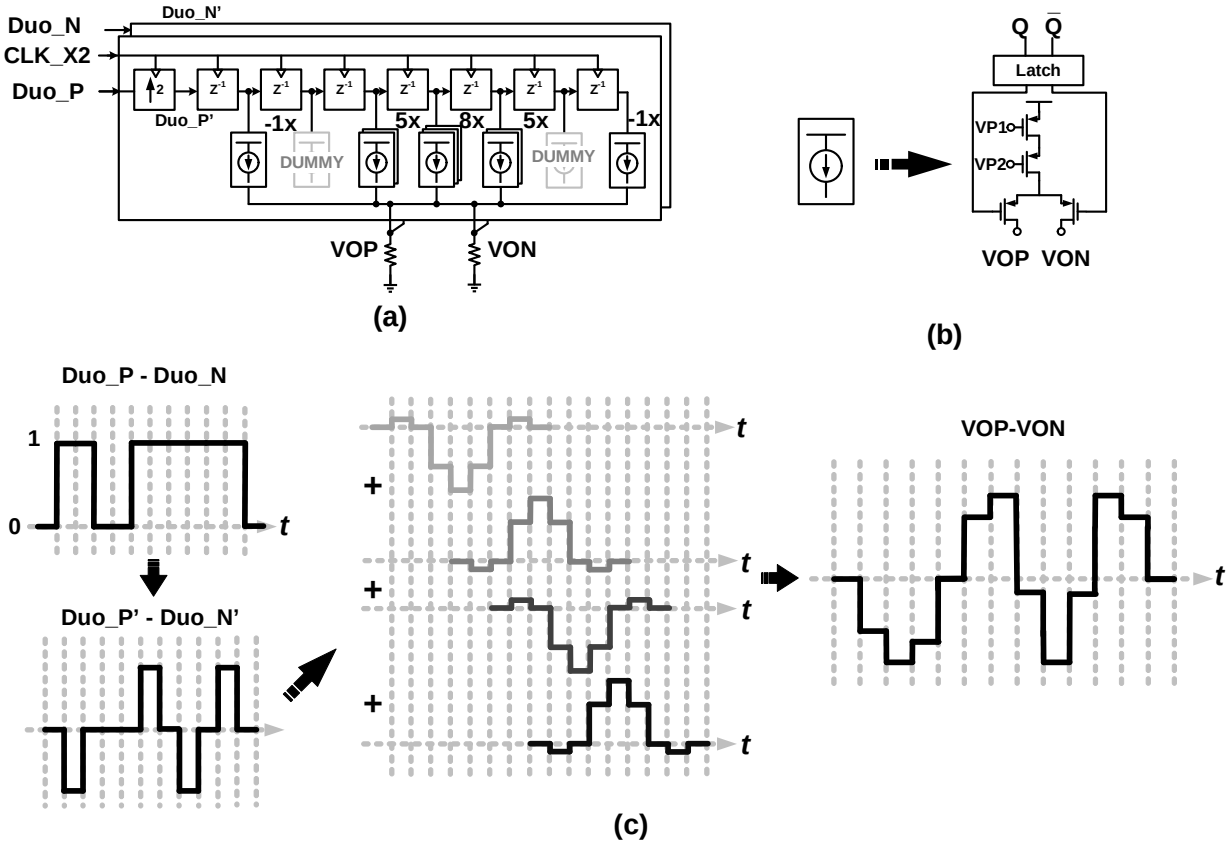


Figure 5.7: Illustration of semi-digital FIR pulse-shaping filter (a) system diagram; (b) current source implementation; (c)time-domain waveforms.

Table 5.1: Duobinary coder output vs. NRZ inpput

NRZ input	Duobinary output	Output amplitude
1	± 1	1
0	0	0

low-pass filters, the raised-cosine pulse-shaping filter could minimize the inter-symbol-interference(ISI) introduced by low-pass filtering. Finite-impulse-response(FIR) architecture is chosen as implementation form, since FIR has linear phase response and constant group delay, which is important in wireless communication system. The filter parameters are listed in Table 5.2.

The β determines the bandwidth(BW) of filter output according to following equation.

Table 5.2: Raised-cosine Pulse-shaping FIR Parameter

roll-off factor β	0.25
over-sampling ratio (OSR)	2
filter order	6
coefficient width	5-bit

$$BW = \frac{(1+\beta) \times DR}{2} \tag{5.4}$$

where DR is the data rate. Smaller β gives narrower signal bandwidth, but the data recovery will be more sensitive to timing jitter. As a tradeoff, the value of 0.25 specified in the IEEE 802.11ad standard is adopted in this design. The OSR affects the spectral image's position and level. The higher OSR, the lower spectral images, and farther away the spectral images from signal. However, given the target Gbps data rate and technology limit of 65 nm CMOS process, higher OSR larger than 2 will pose an extremely stringent timing requirement. Therefore the OSR of 2 is used in this design. The filter order and coefficient width jointly determined the filter shape and its achievable SNR, thus need careful design. To reduce implementation and power cost, extensive system analysis and circuit simulations are performed to optimize these two parameters. In this implementation, the filter order is set to 6, and coefficient width is 5 bit.

Traditionally FIR filters is implemented in digital domain, and requires multi-bit multiplication and accumulation. But such operation is very power hungry when data rate is high [87] . In this design, we recognize that each of Duo_P and Duo_N only has level 0 and 1, so the multiplication can be realized by switching of current sizes of different size, while the accumulation can be realized by current summation. In this way, the high speed digital FIR filter can be eliminated, reducing the power consumption. Notice that previous semi-digital FIR filter can only support constant envelope BPSK/QPSK signals [99], in our implementation, two differential semi-digital FIR filters are used to support ASK signals.

The detailed implementation of semi-digital FIR pulse-shaping filter is shown in Fig. 5.7. Current-steering architecture is adopted for its superior linearity. Cascoded PMOS current sources are used to improve isolation and linearity, and are thermometer-segmented to ensure good linearity. Dummy current sources are added to balance load and minimize clock skew. For the clock buffers, both jitter performance and spectral images are consid-

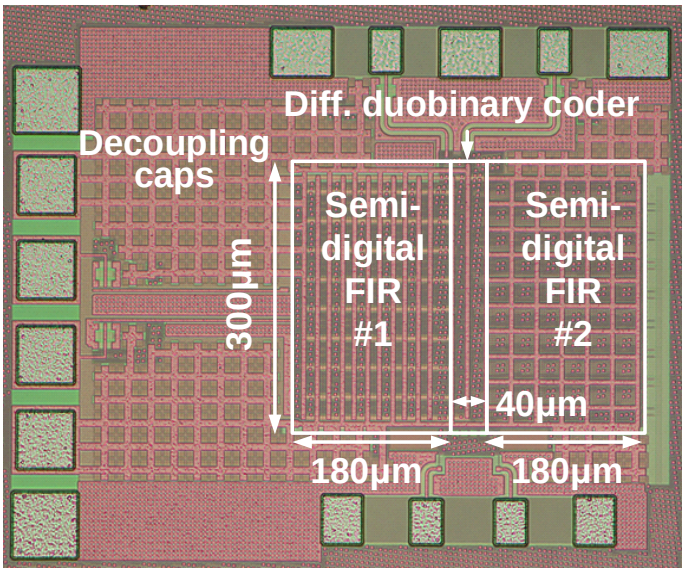


Figure 5.8: Chip micro-graph of proposed modulator. Modulator core area: 0.12 mm^2.

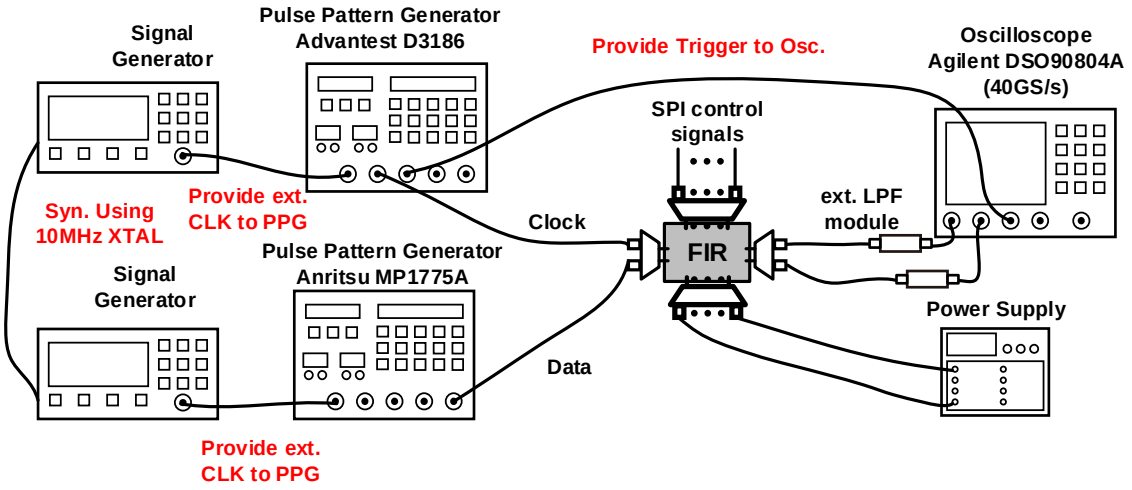


Figure 5.9: The illustration of on-wafer measurement setup for proposed duobinary pulse-shaped ASK modulator.

ered [100], and simulation are used to optimize their sizes.

5.4 Measurement results

To verify the design, the proposed pulse-shaped duobinary ASK modulator is fabricated in a 65 nm CMOS technology. The chip micro-graph is shown in Fig. 5.8. The design occupies a chip area of 0.48 mm^2, in which the core area is 0.12 mm^2. Among the core

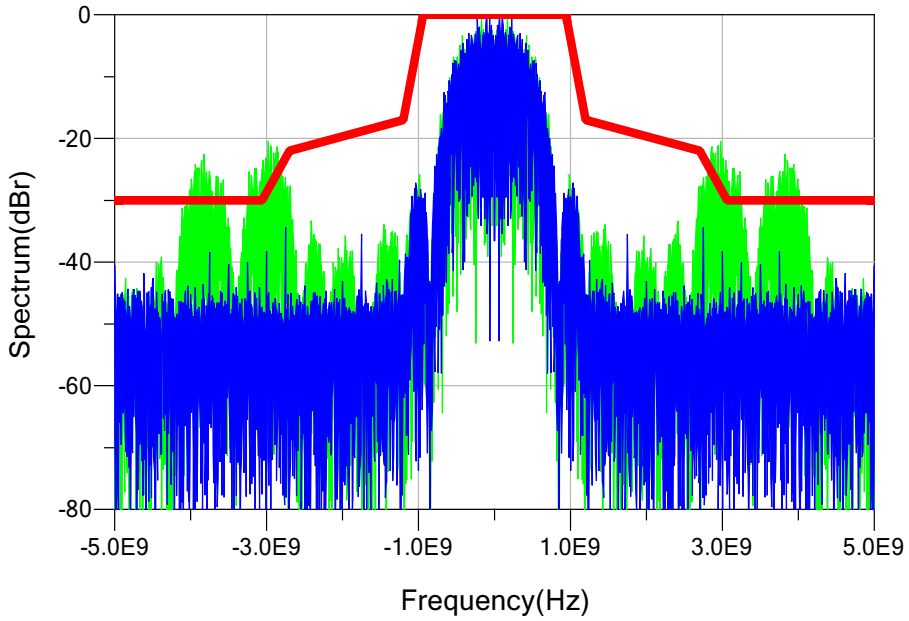


Figure 5.10: Measured output spectrum with external LPF(blue) and without(green) at 1.7Gbps data rate. The IEEE 802.11ad signal channel spectrum mask(red) is overlaid for comparison.

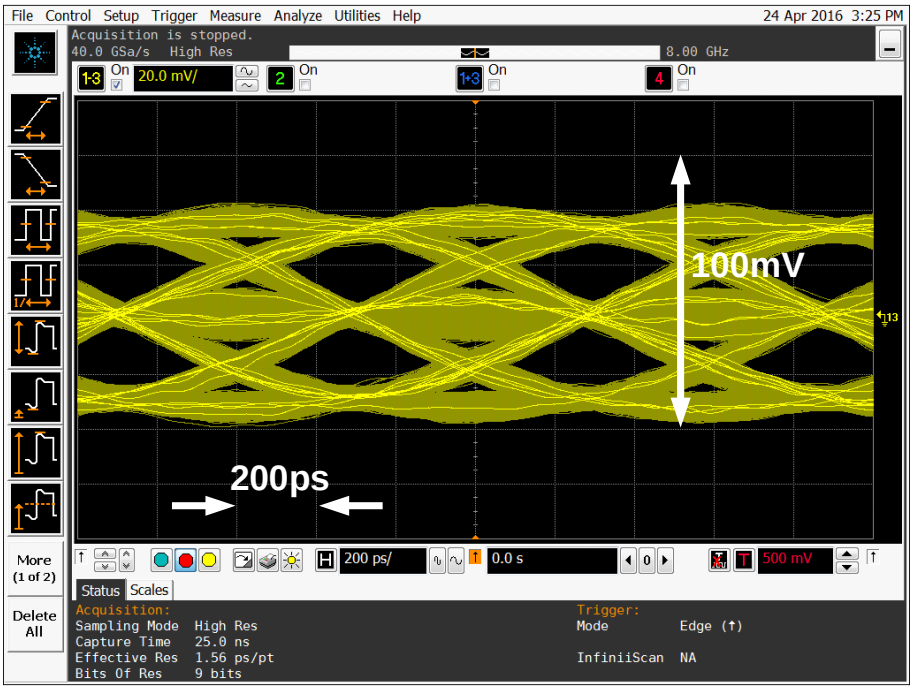


Figure 5.11: Measured eye diagram at 1.7Gbps data rate.

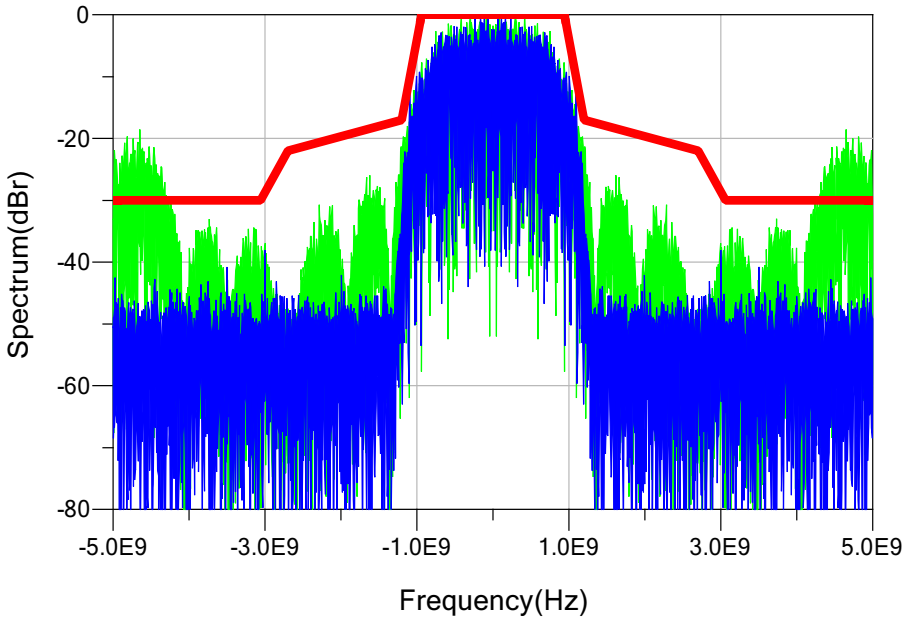


Figure 5.12: Measured output spectrum with external LPF(blue) and without(green) at 2.6Gbps data rate. The IEEE 802.11ad signal channel spectrum mask(red) is overlaid for comparison.

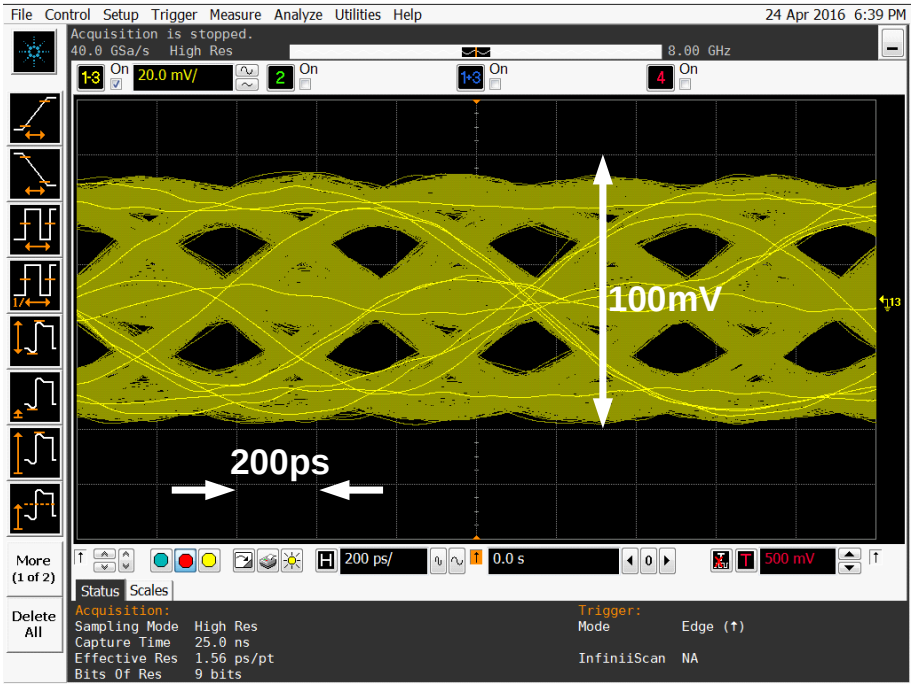


Figure 5.13: Measured eye diagram at 2.6Gbps data rate.

Supply voltage(V)

Data rate(Gbps)

	0.9	1	1.1	1.2
2.7				
2.6				42.8
2.5				42.08
2.4				39.14
2.3				38.42
2.2			33.2	37.8
2.1			31.35	36.5
2			30.69	35.88
1.9			29.81	34.58
1.8		24.8	29.36	33.84
1.7		24.3	28.16	32.54
1.6		23.9	27.6	31.44
1.5		23	26.4	40.22
1.4	19.22	22.2	25.62	29.04

Figure 5.14: Total power consumption for different combinations of data rate and supply voltage.

area, the semi-digital filter occupies an area of 0.108 mm^2, and the differential duobinary coder's area is 0.012 mm^2. The rest of chip area is occupied by the decoupling capacitors.

The measurement setup is shown in Fig. 5.9. During the measurement, a 2^{31} -1 PRBS signal is generated by pulse pattern generator (PPG) and feed to the chip as NRZ input. Another PPG is used to generate the ×2 oversampling clock signal. To ensure the correct frequency relationship of two PPGs, the PPGs are clocked by two signal generators which are synchronized by XTAL. The differential output is captured by a high-speed oscilloscope to observe the time domain waveform and stored for spectrum analysis. The PPG which generates data signal also provides a synchronize signal to oscilloscope so the eye diagram can be directly observed.

According to IEEE 802.11ad standard, the analog reconstruction filter should have a cut off frequency of around 1 GHz to suppress the spectral images. Due to mistakes in circuit design, the designed cutoff frequency of on-chip filter was too high, therefore external low-pass filters (LPFs) are used in measurements. But from simulations a second order LPF with 1 GHz cutoff frequency is suffice to satisfy the spectrum mask.

In the design, the digital part and the analog part have separated supplies. So the both the digital and analog supplies are varied to check the performance. From measurement, the modulator's operation speed is limited by the digital parts. The digital supply voltage DVDD is varied from 1.0 V to 1.2 V, while the analog supply voltage AVDD is fixed to 1 V. For reliability concerns higher DVDD is not used in measurement. Different data

Table 5.3: Performance Comparison of baseband modulators for spectrum mask compliant 60GHz transmitters.

Ref.	Architecture	Technology	Area (mm^2)	Throughout (GS/s)	Pdc/path (mW)
JSSC'13 [86]	Digital FIR+DAC	40nm CMOS	0.18	1.728	48
JSSC'12 [87]	Digital FIR	65nm CMOS	0.1	2.5	400*
CICC'09 [101]	Digital FIR+DAC	110nm CMOS	0.265	1.728	142
ESSCIRC'10 [99]	Semi-digital FIR	0.25μm SiGe HBT	1.6	1.7	990
This work	Differential Duobinary +Semi-digital FIR	65nm CMOS	0.12	**1.7**	**24.3**†
				2.6	**42.8**§

* Only digital FIR † DVDD=1V § DVDD=1.2V

rate are measured while eye diagrams are observed to ensure good signal quality. During the measurements, the eye diagram is displayed by oscilloscope in realtime. If the eye diagram does not show any erroneous trace, then we assume the modulator could work at this data rate. Otherwise we assume the the modulator cannot work at that data rate. In this way, we can get the data rates under which the modulator could has an error-free operation.

Based on above criteria, a maximum data rate of 2.6 Gbps is achieved at 1.2 V DVDD. The measured analog and digital supply currents are 6.8 mA and 30 mA respectively, resulting in a power consumption of 42.8 mW. To have a fair comparison with other designs with similar data rate, the power consumption under data rate of 1.7 Gbps is also measured. When data rate is 1.7 Gbps the DVDD can be lowered to 1 V. The measured analog and digital supply currents are 6.8 mA and 17.5 mA respectively, with total power consumption of 24.3 mW.

The measured output spectra of 1.7 Gbps data rate are shown in Fig. 5.10. The blue line shows the output spectrum with external LPF, and the green one shows when external LPF is not used. The IEEE 802.11ad single-channel spectrum mask is overlaid for comparison. The spectrum shows that the output meet the spectrum mask. The measured eye diagram is shown in Fig. 5.11. The eye diagram shows a three-level output, which is the evidence of the proposed differential duobinary operation. Excellent signal quality is also validated by the large eye opening.

The output spectra of 2.6 Gbps measurement are shown in Fig. 5.12. The blue line shows the output spectrum with external LPF, and the green one shows when external LPF is not used. The measured eye diagram is shown in Fig. 5.13. Though the eye diagram is degraded slightly compared to the 1.7 Gbps data rate case, the large eye opening indicates a reasonable good signal quality under this data rate.

Fig. 5.14 presents the Shmoo diagram. 2.6 Gbps data rate is the maximum data rate that could be reached with DVDD of 1.2 V. Based on LPE simulations, the speed limitation comes from the clock network. The clock speed can be higher by raising the digital supply voltage DVDD. Nevertheless the clock signal quality limits the global performance of the proposed modulator.

This work is compared with other state-of-the-art works, as summarized in Table 5.3. From this table, this work achieves lowest power consumption while satisfying the spectrum mask.

5.5 Summary

This chapters presents an power-efficient modulator for spectrum mask compliant ULP 60GHz ASK transceiver. With the proposed pulse shaped differential duobinary coding, this modulator successfully met the spectrum mask requirement of IEEE 802.11ad standard, while allowing power-efficient ASK modulation used for transceiver. The proposed differential duobinary coder adopts an over-sampling precoder, which relaxes the timing requirement and saves power. Besides, the pulse shaping is implemented by semi-digital FIR filter. No power consuming high speed digital multipliers and accumulators are required. Filter parameters such as OSR, filter order and coefficient width are carefully optimized for power consumption. The modulator supports a throughout of 1.7 Gbps/2.6 Gbps, with a power consumption of 24.3 mW/42.8 mW respectively. This represents one of the best power efficiency among spectrum mask compliant 60 GHz transceivers.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis presents a study of digital-intensive transceivers for low-power wireless communication applications. With the advent of numerous new applications, such as augmented reality (AR)/virtual reality (VR) and massive IoT, power efficiency has become one of the most pressing design concerns in wireless transceivers. While low power wireless transceivers have been proposed to address this issue, such implementations either have large chip area or poor system performance, limiting their potential usage.

Besides, the process scaling has brought both benefits and challenges to the wireless transceiver design. On one hand, process scaling has offered faster device with lower noise and higher cut-off frequency, which has greatly improved the performance of CMOS RFICs. On the other hand, it has also decreased the supply voltage and degraded the circuit linearity. What is more, the newer processes introduce more stringent design rules, significantly degrade the design productivity, and increase the required design man-month. Given the continuous pursuit of higher system integration level, more and more analog/RF circuits will be inevitably moved to the digital process, to have a more efficient system design.

In this study, a holistic approach is taken to fulfill the requirements of next generation wireless transceivers. Innovations from design methodologies, circuit implementations and system architectures are introduced. To provide high purity clock to the wireless transceiver, digital-intensive fully-synthesizable PLLs were presented. Excellent jitter performance is achieved with area compact ring oscillator, with the use of injection-locking technique. Low-power DTC design is realized with the proposed two-stage synthesizable implementation, enabling power efficient fractional-N operation. To avoid the degradation caused by reference spurs and fractional spurs, new circuit implementation

and robust nonlinearity calibrations are proposed. The integer-N IL-PLL realizes 0.4 ps jitter, -52 dBc reference spur and -247.2 dB FOM, with 0.035 mm^2 chip area in a 65 nm CMOS process. The fractional-N IL-PLL achieves 1.2 ps jitter in the fractional-N mode, -40 dBc in-band fractional-N spur, and -234.4 dB FOM, with 0.12 mm^2 chip area in a 65 nm CMOS process. All the building blocks are designed with digital standard cells, and the implementation is compatible to standard digital design flow, which greatly reduced the implementation time and maximized the portability.

Besides, a digital intensive transceiver is realized with the majority of circuit described in HDL and implemented with standard digital design flow. The TRX achieves the state-of-the-art EVM of 0.9% and sensitivity of -94 dBm, with 3.3/4.6 mW power consumption in RX/TX modes. The total transceiver excluding the matching network occupies an area of 0.44 mm^2 in a 65 nm CMOS process, making it ideal to be used in low-cost IoT devices.

At the same time, to reduce the power consumption of transmitter and receiver, digital transmitter with novel modulation scheme is proposed. With the proposed differential duobinary modulation, power efficient transmitter and receiver can be realized with high data rate. Besides, the digital domain filtering of duobinary coding and semi-digital FIR filter greatly suppress the image replicas, enabling IEEE 802.11ad spectrum mask compliant operation. The modulator occupies 0.12 mm^2 in a 65 nm CMOS process, and consumes 24.3/42.8 mW with 1.7/2.6 Gbps data rate, both satisfying the single-channel spectrum mask of IEEE 802.11ad standard. Compared to previous implementations, this design doubles the power efficiency with smaller chip area.

Besides, with the proposed digital-intensive design approach, robust operation with low supply voltage can be achieved. And the chip area benefits more from process scaling than conventional analog-intensive designs. Moreover, with proposed new circuit architecture, the performance sensitivity to layout randomness is reduced. Thus, faster design speed can be achieved with automatic layout synthesis.

6.2 Future work

The history of electronic engineering profession could dates back to the late 19th century. Initially electronic engineering is mainly about telegraph, and later included radio and telephone [102]. However, it is until the innovation of transistors in 1947 and integrated circuits in 1958 did the electronic engineering experience explosive development. Today, after 54 years after Gordon Moore first came up the the famous "Moore's law", the semiconductor industry is still trying to push the limits of process scaling.

Yet the progress of manufacturing technology is only part of the process scaling story. During the same time frame, the design methodology have also experienced great change,

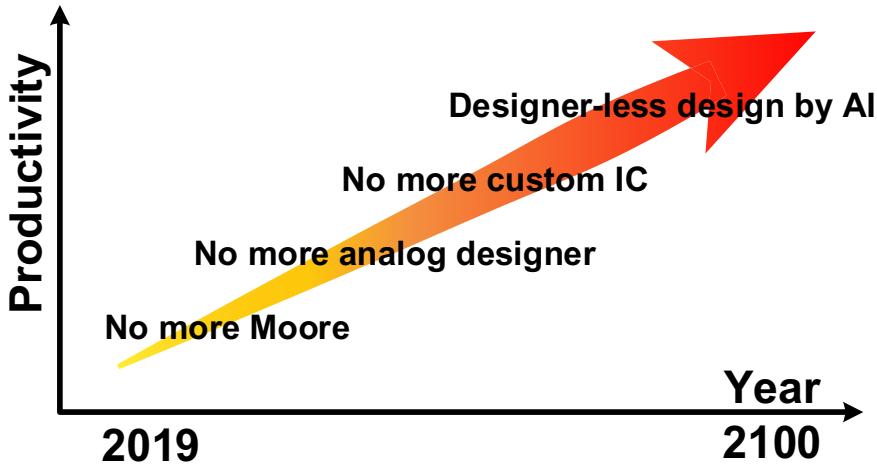


Figure 6.1: Circuit design with AI [10].

with exponential improvement in design productivity. However, the design productivity improvement mainly benefited the digital circuit designers. For analog circuit designers, the circuit design process is still quite primitive.

Both the analog circuit designer and digital circuit designers resort to customized layout to achieve the best performance. However, such customized layout requires significant design efforts, and might not be possible given the limited time and human resources for a certain project. Therefore, design automation was adopted to improve the design productivity. Today, the digital circuit designer community is migrating from RTL to high-level synthesis (HLS), which directly deals architectural-level design [103]. And with the development of AI, AI are making inroads to the electronic design automation (EDA) software which promises further productivity boost [104]. On the other hand, the analog circuit designers are still resorting to SPICE simulators for circuit design, and custom manual layout for physical implementation. Since we are still living in an analog world, analog circuits are still needed to interface the digital circuits with other systems. Therefore, such a gap between analog circuits and digital circuits will eventually bite on the overall system performance.

To closing the gap, digital-intensive fully-synthesizable designs are explored in this thesis, which promising results demonstrated. But the analog circuit design is notoriously complex, with numerous factors to consider and delicate tradeoffs to make in the design. With this in mind, it is imperative to have a rethink about analog circuit design, from design methodology, circuit topology, to architecture and algorithm.

6.2.1 Design methodology improvements

As mentioned in previous section, current analog circuits are designed with SPICE simulators. A lot the human interviews are required, as the majority of information is embedded in the analog waveforms, and experienced designers are required for eye examination. Besides, simulation setting are manually created by designers, and only a limited combinations can be examined.

To improve the design productivity, the analog design and verification should be automated. The circuit should be defined with a set of parameters, and test vectors can be automatically generated. To check the simulation results, assertion-based verification should be used. Besides, assertion should be automatic generated and checked, with minimal human innervation.

Furthermore, current physical design of analog circuits still requires layout engineers to understand the designers' intention. With future development, automatic physical design programs should be able understand the designer's intention. Automatic layout constraints generation should be available, and different optimization priorities can be automatically determined.

6.2.2 New circuit topologies

Another possible improvement comes from circuit level innovations. Different circuit topologies have different sensitivity to layout uncertainties, which until now has not been investigated yet. And the size of circuits also affect how the digital tools handle P&R in a limited chip area. Therefore, new circuit architectures that are area compact and insensitive to layout mismatches are highly desired.

Besides, current high performance synthesizable analog designs are limited to frequency synthesizers and transmitter, which by nature are large-signal circuits. For low noise small signal circuits, such as low noise amplifiers, the high performance synthesizable design that is comparable to custom design is not available yet. Such a design would be of great value, and a truly synthesizable design would be possible.

Moreover, current circuit designs are mainly based on CMOS technology. However, with the CMOS process scaling saturates, it is likely new devices will be emerge, such as carbon nanotube [105] and single-molecule devices [106]. Analog circuits with new process and new materials are needed.

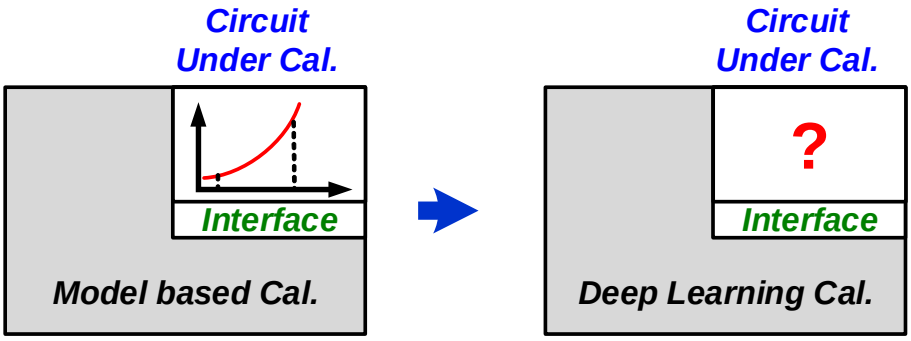


Figure 6.2: Digital calibration without model.

6.2.3 Improved architecture and algorithm

As shown in the frequency synthesizer design, current digital background calibrations, especially the DTC nonlinearity calibration, have very slow convergence speed. This might limit the applicability of the calibrations, as in SoC some voltage drop can be very fast. A high speed digital calibration is needed.

Therefore, on one hand, the interactions of the various calibration loops need to be analyzed carefully. Various calibration introduced a multitude of feedback loops inside the circuit. And the operation of some loops is more important than others. Therefore, proper bandwidth setting is needed to ensure the working of the interwind calibration loops. On the other hand, new digital calibrations is needed. A combination of background calibration and foreground calibration might be needed to accelerate the calibration speed and enhance the calibration stability.

More fundamentally, all the current calibrations or algorithms require some models contrived by human beings. For example, all the digital calibrations insides PLL are designed to address the known non-idealities. However, if the non-ideality is not recognized, current digital calibrations cannot correct it. However, AIs such as AlphaGo [107] have proved that machines might could have a better understanding than human beings. Therefore, concepts and techniques from deep learning might can be applied to circuit design as well. With sample designs provided to the AI, the algorithm could help the circuit designers to discover the unrecognized on-idealities, and correct it using the computing power of digital logic, as shown in Fig. 6.2. Better still, it is possible the AI could discover and solve the problem, even without being noticed by the human designers.

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Appendix A

Publication List

A.1 Journal Papers

- **Bangan Liu**, Huy Cu Ngo, Kengo Nakata, Wei Deng, Yuncheng Zhang, Junjun Qiu, Toru Yoshioka, Jun Emmei, Jian Pang, Aravind Tharayil Narayanan, Haosheng Zhang, Dongsheng Yang, Hanli Liu, Teruki Someya, Atsushi Shirane, Kenichi Okada, "A 0.4-ps-Jitter -52-dBc-Spur Synthesizable Injection-Locked PLL With Self-Clocked Nonoverlap Update and Slope-Balanced Subsampling BBPD," *IEEE Solid-State Circuits Letters*, Vol.2, No. 1, pp. 5-8, Jan. 2019.

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- Jian Pang, Shotaro Maki, Seitarou Kawai, Noriaki Nagashima, Yuuki Seo, Masato Dome, Hisashi Kato, Makihiko Katsuragi, Kento Kimura, Satoshi Kondo, Yuki Terashima, Hanli Liu, Teerachot Siriburanon, Aravind Tharayil Narayanan, Nurul Fajri, Tohru Kaneko, Toru Yoshioka, **Bangan Liu**, Yun Wang, Rui Wu, Ning Li, Korkut Kaan Tokgoz, Masaya Miyahara, Atsushi Shirane, and Kenichi Okada, "A 50.1Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay With Calibration of LO Feed-through and I/Q Imbalance," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 54, No. 5, pp. 1375-1390, May 2019.

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Appendix B

List of Abbreviations

ABB: analog baseband

ACPR: adjacent channel power ratio

ACR: adjacent channel rejection

ADC: analog-to-digital converter

AI: artificial intelligent

ALF: analog loop filter

AR: augmented reality

ASK: amplitude Shift Keying

BER: bit error rate

BIST: built-in-self-test

BNF: blocker noise figure

BPF: bandpass filter

BPSK: binary phase shift keying

BW: bandwidth

CAGR: compound annual growth rate

CCO: current controlled oscillator

CP: charge-pump

CS (DTC): constant-slope (DTC)

CS: carrier sense

DAC: digital-to-analog converter

DAFS: direct analog frequency synthesis

DBB: digital baseband

DCO: digital controlled oscillator

DCOC: DC offset calibration

DCW: DTC control word

DDFS: direct digital frequency synthesis

DLF: digital loop filter

DNL: differential nonlinearity

DRC: design rule check

DSB: double-sided-bandwidth

DSM: delta-sigma modulator

DTC: digital-to-time converter

EDA: electronic design automation

ENOB: effective number of bits

EVM: error vector magnitude

FCW: frequency control word

FEC: forward error correction

FIR: finite impulse response

FMR: frequency multiplication ratio

FOM: figure-of-merit

FSK: frequency shift keying

FVF: flipped-voltage-follower

GMSK: Gaussian Minimum Shift Keying

HDL: hardware description language

HLS: high-level synthesis

IF: intermediate frequency

IIR: infinite impulse response

IL-PLL: injection-locked PLL

ILO: injection-locked oscillator

INL: integral nonlinearity

ISI: inter-symbol-interference

IoT: Internet of things

LC: inductor capacitor

LDE: layout dependent effect

LMS: least mean square

LNA: low noise amplifier

LNTA: low noise trans-conductance amplifier

LO: local oscillation

LOFT: local oscillation feedthrough

LPE: layout parasitic extraction

LPF: low-pass filter

LSB: least significant bit

LUT: look-up table

MAC: medium access control

MDLL: multiplying delay-locked loop

MIM: metal-insulator-metal

MMD: multi-modulus divider

MOM: metal-oxide-metal

MSB: most significant bit

MUX: multiplexer

NF: noise figure

NFC: near-field-communication

NRZ: non-return-to-zero

OOK: on-off keying

OSR: over-sampling ratio

PA: power amplifier

PER: packet error rate

PFD: phase frequency detector

PLL: phase-locked loops

PPA: power, performance, area

PPG: pulse pattern generator

P&R: place-and-route

PRBS: pseudo random bit sequence

PS: path-selection

PSD: power spectrum density

PVT: process, voltage, temperature

PWLI: piece-wise linear interpolation

QPSK: quadrature phase-shift keying

REFD: reference doubler

RFIC: radio frequency integrated circuit

RMS: root-mean-square

RTL: register-transfer level

RX: receiver

SAR: successive-approximation-register

SNDR: signal-to-noise-and-distortion ratio

SNR: signal-to-noise ratio

SPI: serial peripheral interface

SS-BBPD: sub-sampling bang-bang phase detector

SSB: single side band

SoC: system-on-a-chip

TANC: true arbitrary nonlinearity calibration

TDC: time-to-digital converter

TRX: transceiver

TX: transmitter

ULP: ultra low power

URLLC: ultra-reliable low latency communication

VCO: voltage controlled oscillator

VGA: variable gain amplifier

VR: virtual reality

VS: variable-slope

XO: crystal oscillator

ZOH: zero-order-hold