論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Study of Digital-Intensive Ultra-Low-Power Wireless Transceiver
著者(和文)	Bangan Liu
Author(English)	Bangan Liu
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第11314号, 授与年月日:2019年9月20日, 学位の種別:課程博士, 審査員:岡田 健一,髙木 茂孝,本村 真人,德田 崇,伊藤 浩之,飯塚 哲也
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第11314号, Conferred date:2019/9/20, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	審査の要旨
Type(English)	Exam Summary

（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

専攻： Department of	電子物理工学 専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of (Philosophy)
学生氏名： Student's Name	Liu Bangan	指導教員（主）： Academic Supervisor(main)	岡田　健一
		指導教員（副）： Academic Supervisor(sub)	

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis presents a study of digital-intensive transceivers for low-power wireless communication applications. With the advent of numerous new applications, such as augmented reality (AR)/virtual reality (VR) and massive IoT, power efficiency has become one of the most pressing design concerns in wireless transceivers. While low power wireless transceivers have been proposed to address this issue, such implementations either have large chip area or poor system performance, limiting their potential usage.

Besides, the process scaling has brought both benefits and challenges to the wireless transceiver design. On one hand, process scaling has offered faster device with lower noise and higher cut-off frequency, which has greatly improved the performance of CMOS RFICs. On the other hand, it has also decreased the supply voltage and degraded the circuit linearity. What is more, the newer processes introduce more stringent design rules, significantly degrade the design productivity, and increase the required design man-month. Given the continuous pursuit of higher system integration level, more and more analog/RF circuits will be inevitably moved to the digital process, to have a more efficient system design.

In this study, a holistic approach is taken to fulfill the requirements of next generation wireless transceivers. Innovations from design methodologies, circuit implementations and system architectures are introduced. To provide high purity clock to the wireless transceiver, digital-intensive fully-synthesizable PLLs were presented. Excellent jitter performance is achieved with area compact ring oscillator, with the use of injection-locking technique. Low-power DTC design is realized with the proposed two-stage synthesizable implementation, enabling power efficient fractional-N operation. To avoid the degradation caused by reference spurs and fractional spurs, new circuit implementation and robust nonlinearity calibrations are proposed. The integer-N IL-PLL realizes 0.4 ps jitter, -52 dBc reference spur and -247.2 dB FOM, with 0.035 mm^2 chip area in a 65nm CMOS process. The fractional-N IL-PLL achieves 1.2 ps jitter in the fractional-N mode, -40 dBc in-band fractional-N spur, and -234.4 dB FOM, with 0.12 mm^2 chip area in a 65nm CMOS process. All the building blocks are designed with digital standard cells, and the implementation is compatible to standard digital design flow, which greatly reduced the implementation time and maximized the portability.

Besides, a digital intensive transceiver is realized with the majority of circuit described in HDL and implemented with standard digital design flow. The TRX achieves the state-of- the-art EVM of 0.9% and sensitivity of -94 dBm, with 3.3/4.6 mW power consumption in RX/TX modes. The total transceiver excluding the matching network occupies an area of 0.44 mm^2 in a 65nm CMOS process, making it ideal to be used in low-cost IoT devices.

At the same time, to reduce the power consumption of transmitter and receiver, digital transmitter with novel modulation scheme is proposed. With the proposed differential duobinary modulation, power efficient transmitter and receiver can be realized with high data rate. Besides, the digital domain filtering of duobinary coding and semi-digital FIR filter greatly suppress the image replicas, enabling IEEE 802.11ad spectrum mask compliant operation. The modulator occupies 0.12 mm^2 in a 65 nm CMOS process, and consumes 24.3/42.8mW with 1.7/2.6Gbps data rate, both satisfying the single-channel spectrum mask of IEEE 802.11ad standard. Compared to previous implementations, this design doubles the power efficiency with smaller chip area.

Besides, with the proposed digital-intensive design approach, robust operation with low supply voltage can be achieved. And the chip area benefits more from process scaling than conventional analog-intensive designs. Moreover, with proposed new circuit architecture, the performance sensitivity to layout randomness is reduced. Thus, faster design speed can be achieved with automatic layout synthesis.