

論文 / 著書情報
Article / Book Information

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Type(English)	Summary

論文要旨

THESIS SUMMARY

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Department of Graduate major in 電気電子コース
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申請学位(専攻分野)：博士 (工学)
Academic Degree Requested Doctor of
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要旨 (英文 800 語程度)

Thesis Summary (approx.800 English Words)

Ferroelectric memory is required for high-speed and low-voltage nonvolatile memory applications. Among the several types of ferroelectric memories, a ferroelectric gate field-effect transistor (MFSFET) is promising for high integration. Although it has been investigated with using ferroelectric materials such as $\text{Pb}(\text{Zr,Ti})\text{O}_3$ and $\text{SrBa}_2\text{Ti}_2\text{O}_9$ for decades, it has not been realized because of their Si-incompatibility and lack of scalability. In 2011, it was found that the orthorhombic phases of HfO_2 show ferroelectric properties. However, it is hard to be stabilized because it is metastable phase. The most widely used method to stabilize ferroelectric phase is doping. The doping requires high temperature annealing for the crystallization which leads to thick interfacial SiO_2 formation between HfO_2 and Si substrates. It induces the depolarization field and leads to degradation of the retention characteristics. Furthermore, the V_{TH} controllability is hard to be obtained with doped HfO_2 . Therefore, direct deposition with low temperature process is necessary to be investigated. The ferroelectric phase formation is also affected by top electrodes. Post metallization annealing (PMA) process with gate electrodes would be effective for the crystallization of ferroelectric HfO_2 . Furthermore, it is possible to reduce the crystallization temperature. In this dissertation, ferroelectric nondoped HfO_2 formation for MFSFET applications was investigated utilizing reactive sputtering with Hf target. The sputtering parameters such as gas flow ratio and sputtering power were precisely controlled to form the ferroelectric nondoped HfO_2 . Then, thin film formation below 10 nm was investigated utilizing PMA process. After investigation of the fabrication process of MFSFETs, electrical characteristics of MFSFETs with ferroelectric nondoped HfO_2 were investigated.

First, the reactive sputtering process for ferroelectric nondoped HfO_2 formation on Si(100) was investigated. In case of 24 nm thick HfO_2 directly deposited on Si(100) substrates after post deposition annealing (PDA) process at 600 °C, the orthorhombic phase fraction was increased as the oxygen flow rate during reactive sputtering was decreased from Ar/ O_2 of 2.0/1.0 to 2.0/0.2 sccm. At the same time, the memory window (MW) was increased from 0.4 to 0.8 V as the oxygen flow rate was decreased. It is assumed that the high oxygen flow rate forms a stable phase, while the energy gap for the phase transition to metastable orthorhombic is reduced with low oxygen flow rate during reactive sputtering. However, the sputtering power of 100 W shows the severe stretch in its C-V characteristics, which indicates the degradation of interface properties. By reducing sputtering power from 100 to 60 W for 20 nm thick HfO_2 utilizing PDA

process at 600 °C, the density of interface state (D_{it}) was decreased from 3.7×10^{10} to $2.5 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$. Furthermore, the leakage current was decreased from 1×10^{-8} to $3 \times 10^{-9} \text{ A/cm}^2$ at -3 V. Kr/ O_2 plasma sputtering with same gas flow rate of 2.0/0.2 sccm was also effective for further reduction of the leakage current to $1 \times 10^{-9} \text{ A/cm}^2$ at -3 V. The deposition with low damage was realized by Kr/ O_2 plasma sputtering because heavy inert gas reduced the damage to the film.

Next, thin film formation was investigated utilizing PMA process for low voltage operation. For 10 nm thick HfO_2 deposited by Ar/ O_2 plasma sputtering utilizing PDA process at 600 °C, the charge injection type hysteresis was observed in C-V characteristics, and paraelectric properties were shown in P-V characteristics. On the other hand, PMA process realized the ferroelectric properties in C-V and P-V characteristics. Even with low temperature process at 500 °C, the intrinsic P_r was on the order of $0.1 \mu\text{C/cm}^2$ and MW was around 0.3 V with sweep range from -3 to 3 V. The P_r corresponds to the sheet carrier density of $10^{12}/\text{cm}^2$ or higher, which is enough for inducing the inversion carriers in Si. It is because of the stress induced by Pt electrodes. For 5 nm thick HfO_2 , it was important to reduce the damage for ferroelectric HfO_2 formation. In case of Kr/ O_2 plasma sputtering, it showed MW of 0.2 V while Ar/ O_2 plasma sputtering showed the charge injection hysteresis. Therefore, low damage sputtering is promising for thin film formation.

Next, MFSFETs were fabricated with ferroelectric nondoped HfO_2 utilizing Pt gate electrodes. For gate last-process, dry etching with Ar/ Cl_2 plasma for Pt and HfO_2 has issues of plasma damage during gate patterning process. It directly damaged the HfO_2 on the channel region. Therefore, wet etching process was investigated for contact hole patterning and contact electrodes formation. Aqua regia and DHF successfully etched the Pt electrodes and as-deposited HfO_2 . The MFSFETs were fabricated by utilizing wet etching process based on this etching property. In case of Ar/ O_2 plasma sputtering, the fabricated MFSFETs with 10 nm thick HfO_2 gate insulator for gate length/width (L/W) of 3/15 μm utilizing PMA process at 500 °C realized the ferroelectric hysteresis in I_D - V_G characteristics. It showed MW of 0.9 V with sweep range from -3 to 3 V. The retention time of 10^3 s was obtained. The MW was increased by utilizing Kr/ O_2 plasma sputtering. It showed the MW of 1.3 V with sweep range from -2.5 to 2.5 V. Also, the current drivability was increased. The retention time of $8 \times 10^3 \text{ s}$ was observed. The improved characteristics were realized by reduction of sputtering damage.

In conclusion, the ferroelectric nondoped HfO_2 formation and MFSFETs were realized utilizing reactive sputtering. The low annealing temperature of 500 °C was utilized with nondoped HfO_2 by PMA process with Pt gate electrodes. The annealing temperature is lower than reported FET with doped HfO_2 . It is promising for future MFSFET applications.

備考：論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。

Note：Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).

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