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Doctoral Thesis

Chip Level Integration for High Performance Sputtered-MoS_2 *n*MISFETs

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Date: February 14th, 2020

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Certified by _____

Hitoshi Wakabayashi, Professor, Thesis Supervisor

Abstract of Doctoral Thesis February 14th, 2020

Chip Level Integration for High Performance Sputtered-MoS_2 *n*MISFETs

Supervisor: Professor Hitoshi Wakabayashi

Department of Electrical and Electronic Engineering

Kentaro Matsuura

In this thesis, normally-off sputtered molybdenum disulfide (MoS_2) *n*MISFETs with a top gate configuration are demonstrated with chip level integration process. A MoS_2 film, one of the transition-metal di-chalcogenide (TMDC), exhibits high mobility of approximately 200 cm^2/V-s in an extremely small thickness of 0.65 nm. The MoS_2 film has flexibility and transparency, and it is expected to be applied for Internet of Things (IoT) and wearable electronics. The MoS_2 thin films have largely relied on the mechanical exfoliation method, chemical vapor deposition (CVD) and Metal Organic CVD methods. However, the contamination of alkali metal or carbon is concerned. Therefore, radiofrequency-magnetron sputtering is selected for MoS_2 thin and large film. A passivation film for MoS_2 film as the sidewall realizes a test elementary group of MISFETs on a chip whose area is 2.5 x 2.5 cm^2. However, high contact resistance and normally-on operation are a challenge. Hence, a $MoSi_2$ contact is introduced and reduces the contact resistance down to 2.6 x 10^{-2} Ohm-cm^2. The causes of normally-on operation are 1) high carrier density of sputtered MoS_2 film due to sulfur vacancies, 2) residual photo resist and 3) high

interface trap density (Q_{it}) between MoS_2 and aluminum oxide (Al_2O_3) films and positive fixed charge (Q_f) of Al_2O_3 film. Sulfur powder annealing (SPA) compensates for sulfur vacancies and reduces the carrier density down to 1.8×10^{16} cm^{-3}. Piranha cleaning removes the photo resist. A forming gas (F.G.) annealing further reduces Q_{it} and Q_f, simultaneously. As a result, normally-off sputtered MoS_2 *n*MISFETs is achieved. Although F.G. annealing decreases transconductance due to the increase in the effective channel length and on current is needed to be increased by controlling the number of nucleation site during sputtering, the low off current of 10^{-6}~10^{-7} μA/μm is successfully observed and compatible with previous reports. This is the first report showing the normally-off operation with top-gate, which would realize the integrated circuits having low energy consumption using TMDC in the future.

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My research activity at Tokyo Institute of Technology is supported by many people. I would like to tell them gratitude for borrowing this place.

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Of course, I couldn't complete this thesis by myself. If there were not those encouragements, this thesis would not be materialized. In this environment, I could experience various and precious things.

Thank you.

February 14th, 2020

Kentaro Matsuura

Contents

Chapter1 Introduction

1.1 Internet of Things (IoT)

In 1999, K. Ashton started to use the phrase, “Internet of Things (IoT)”, meaning that all of the things and humans connect each other via internet and share the captured data [1.1]. Until today, this phase became familiar all over the world. He mentioned the background which he started to use this phrase as follows,

> *Today computers—and, therefore, the Internet—are almost wholly dependent on human beings for information. Nearly all of the roughly 50 petabytes (a petabyte is 1,024 terabytes) of data available on the Internet were first captured and created by human beings—by typing, pressing a record button, taking a digital picture or scanning a bar code. Conventional diagrams of the Internet include servers and routers and so on, but they leave out the most numerous and important routers of all*

The definition of “things” is not general-purpose devices, such as smartphones and PCs, but dedicated-function objects, such as vending machines, jet engines, connected cars and a myriad of other examples [1.2]. By 2020, more than 20 billion things are expected to be connected and security and privacy are concerning and discussing. However, “IoT” devices will give us a lot of benefits such as a reduction in expenses, optimization of assets, improvement of security.

1.2 Transparent display

As a type of IoT device, the transparent display has been researched and developed all over the world for application for Augmented Reality (AR) region or Virtual Reality (VR). The transparent display is expected to be used in many IoT devices such as electrical mobility, smartphone and head mount display. Table 1.1 shows the benchmark for the main light emitter for transparent display [1.3-1.5]. The pixel has room for improvement and 4k display is still difficult to develop. Transparent LCD and Inorganic EL has a strong point that is high transmittance. On the other hand, organic EL has the flexibility and low energy consumption.

Table 1.1 Performance comparison of transparent display [1.3-1.5].

	Transparent LCD	Organic EL	Inorganic EL
Photo			
Pixel	1920 x 1080 (Full HD)	Full HD	640 x 480
Size [inch]	27	55	10.4
Resolution [ppi]	~ 80	~ 40	~ 77
Frame rate [Hz]	---	120	---
Transmittance [%]	80	45	80

For all light emitters, the signal control by the transistor is necessary. Table 1.2 is the performance comparison of transistor channel materials for display. Crystalline silicon (c-Si), poly-Si and amorphous silicon are most widely used for conventional display such as CRT display. However, oxide semiconductors such as IGZO or organic semiconductors such as pentacene have been used for flexible and transparent display because these materials have relatively high mobility at thin film regions and flexibility and transparency. However, it is still difficult for these

materials to show more than 20 cm^2/V-s for realizing the 4k display.

Table 1.2 Performance comparison of transistor channel material for display.

	c-Si	poly-Si	a-Si	Oxide Semi. (Ex : IGZO)	Organic Semi. (Ex : Pentacene)
Band gap [eV]	1.12	1.12	~1.8	3	~ 3
Mobility [cm^2/V-s]	~500	>100	0.5	~10	~ 10
Flexibility	×	×	×	△	○○
Transparency	×	×	×	○	○

In this chapter, the concept of IoT and HMD as one example of IoT are described as the introduction. Figure 1.2 shows the structure of this thesis.

In chapter 2, the research background and motivation are shown.

In chapter 3, the first report of sputtered MoS_2-*n*MISFETs is shown. The process flow, the performance and the analysis for improvement are discussing.

In chapter 4, sulfur powder annealing (SPA) for sulfur compensation of sputtered MoS_2 film is described. The pressure and temperature characteristics of this annealing process are explored to discover the condition which can sulfurize sputtered MoS_2 film most.

In chapter 5, $MoSi_2$ contact for sputtered MoS_2 film to realize a low contact resistance is demonstrated.,

In chapter 6, normally-off sputtered MoS_2-*n*MISFETs with a top gate is achieved by improving the structure of chapter 3 and utilizing the technologies in chapters 4 and 5.

In chapter 7, the author's conclusion is stated.

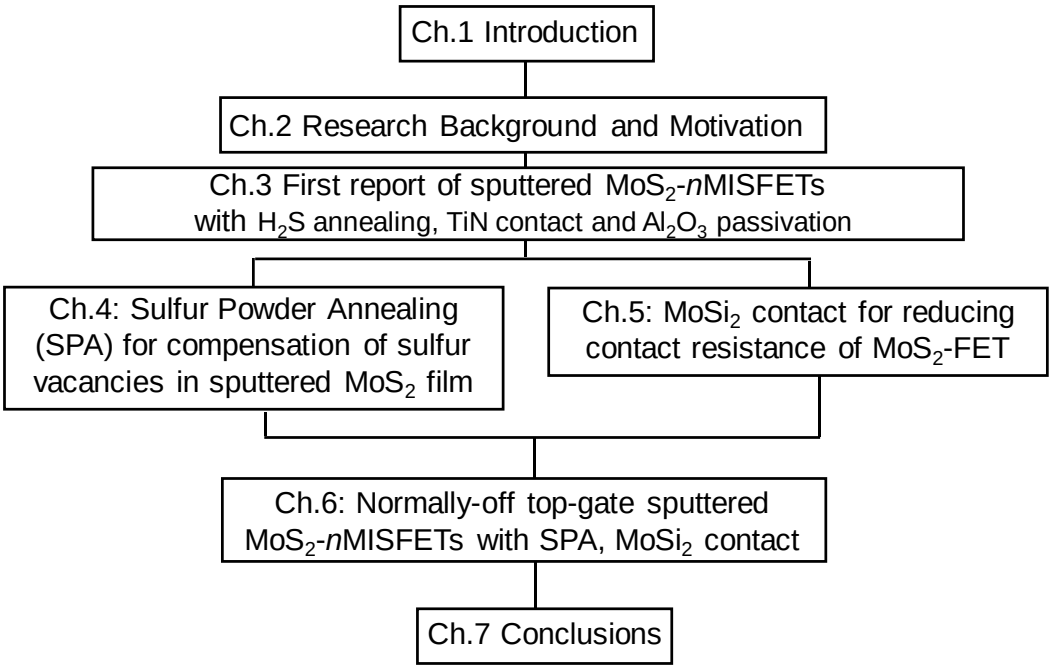

Figure 1.2 Structure of this thesis.

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[1.1] K. Ashton, “That “Internet of Things” Thing,” RFID Journal, (2019).

[1.2] Leading the IoT, <https://www.gartner.com/imagesrv/books/iot/iotEbook_digital.pdf>, Gartner.

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[1.5] Inorganic EL, <http://www.teidec.co.jp/InorganicEL/tasel.html>, TEIDEC.

Chapter 2 Research Background and motivation

2.1 Device miniaturization and scaling rule

Large Scale Integration (LSI) technology has been developing and contributing to today's IT society. In 1965, Gordon. E Moore who is one of the founders of Intel declared the very important trend about the integrated circuit in his paper. He said that the improvement of integrated circuit develops electronics and gives birth to the new science. He also states the practice trend that the number of transistors on integrated circuits doubles approximately every eighteen or twenty-four months [2.1]. This trend is said "Moore's law" Actually, the device miniaturization has been realized along with Moore's law. In 2003, 0.1 billion transistors per chip were achieved. Furthermore, 5 billion transistors per chip in 2010 and it is expected to reach 15 billion (more than that of our brain's neurons!) by 2015 in his paper. In fact, this expectation matches with real data roughly as shown in Figure 2.1 [2.1,2.2].

The reason why the miniaturizing device is important is that to make them even smaller devices leads to improve the property of switching movement of it. Figure 2.2 is schematic illustration of device miniaturization [2.1]. The basic principle of device miniaturization is that the length of the channel, the way carriers go through, shorten as the size of the device becomes small, therefore it enables the device to operate faster. The quantitative rule about this miniaturization was advocated by R. H. Dennard *et al* first [2.3]. Table 2.1 shows the scaling results of MOSFET device and circuit parameters. For example, if the size of the transistor is turned half times in the height direction, longitudinal direction, and lateral direction respectively and the voltage is halved, the power dissipation becomes one-fourth times and the delay time also becomes one-twice time. In other words, the device miniaturization leads to rapid response and high efficiency. That's why to make devices smaller is significant.

In order to realize the device miniaturization, it is said that the development of lithographic technology [2.3] is important. Today, lithographic technology for forming semiconductor integrated circuit improve day by day. However, it is nevertheless that the development of device design and structure to utilize the technology.

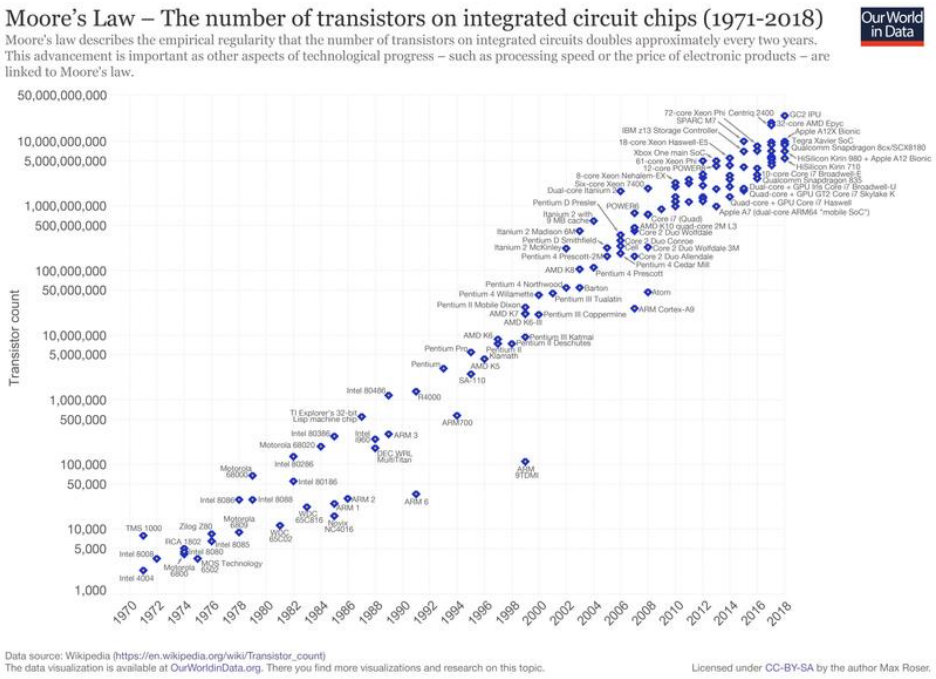


Figure 2.1 Transistor count [2.1,2.2].

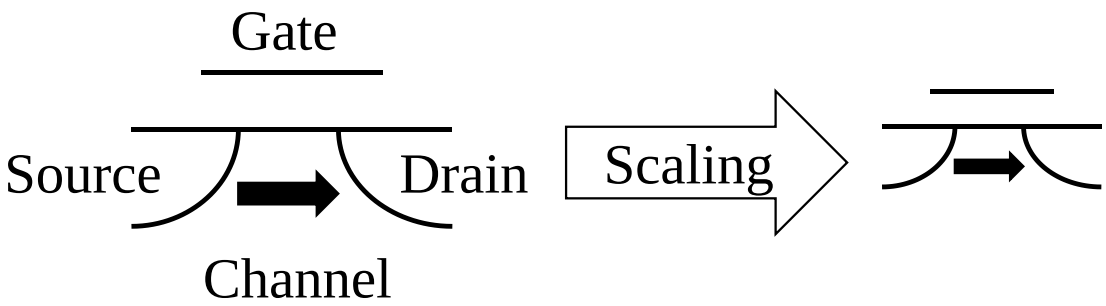


Figure 2.2 Schematic illustration of device miniaturization [2.1].

Table 2.1 Scaling results of MOSFET device and circuit parameters [2.3].

Device or circuit parameter	Scaling factor
Device dimensions (t_{ox}, L, W)	1/k
Doping concentration (N_a, N_d)	k
Voltage (V)	1/k
Current (I)	1/k
Capacitance ($C=\varepsilon A/t$)	1/k
Delay time per circuit ($\tau=CV/I$)	1/k
Power dissipation per circuit ($P=VI$)	$1/k^2$
Power density (VI/A)	1

2.2 Scaling limit of device miniaturization

It is said that the device miniaturization improves the property of device movement in the previous section and the scaling technology has been developed as shown in Figure 2.2. However, it is predicted that the speed of this improvement will not be able to catch up with Moore's law. There are some reasons why scaling technology has a limit. The first reason is leakage current due to short channel effect. The second reason is about the deterioration of mobility in terms of silicon (Si), the most prevalent material for advanced LSIs.

First, in order to make the device size smaller, it is necessary that the length of the lateral direction will also become small. At that time, the influence of short channel effect becomes bigger. Short channel effect leads to several deteriorations of device property. For example, the drain current becomes big and it leads to depletion of switching property and threshold voltage. Moreover, as miniaturization progresses, the oxide film becomes thinner and thinner. This phenomenon makes the leakage current bigger.

Second, it is important to have the device size smaller in height direction to prevent short channel effects from becoming bigger. However, it is reported that if the device becomes thinner, the mobility will decrease as shown in Figure 2.3 [2.4]. Figure 2.3 shows that the mobility change of Si used for advanced LSIs widely. In this Figure, first, the mobility also decreases until the thickness becomes around 5nm, however it increases when it is between 5 nm and 3 nm. Finally, the mobility decreases again when it is less than 3 nm.

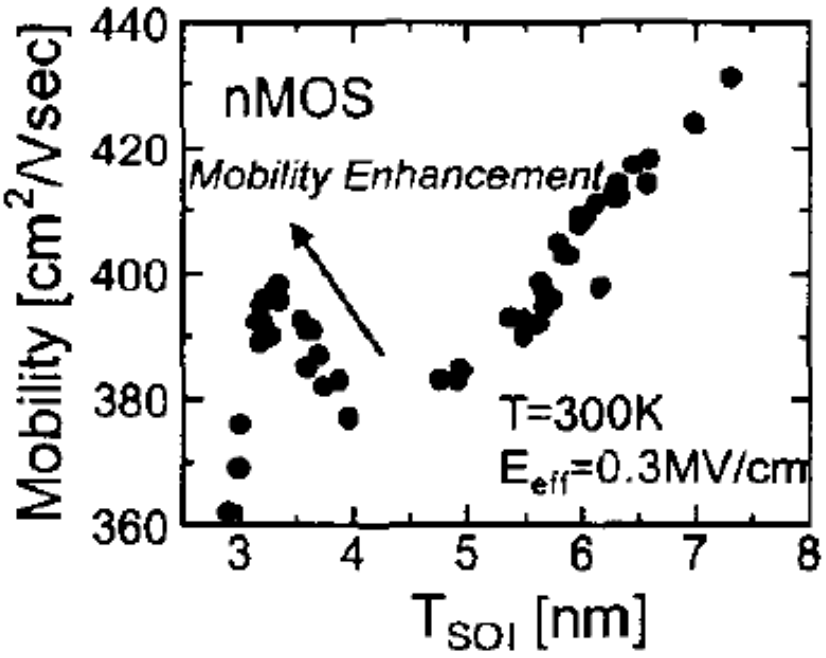


Figure 2.3 Si mobility versus TSOI [2.4].

This property can be explained in Figure 2.4 [2.5]. Figure 2.4 shows the schematic illustration of the conduction band of SOI-MOSFET with different SiO_2 film thickness. When the T_{SOI} is thicker than 20 nm, this SOI-MOSFET is regarded as bulk-MOSFET, so the mobility is also the same. As the thickness becomes smaller than 20 nm, the wave function of electron can't extend, especially in the four-fold valleys due to the decrease in physical thickness. That's why mobility also deteriorates. When the thickness becomes thinner than 5 nm, the energy of four-fold valleys is lifted up and the two-fold valleys start to dominate. Therefore, total mobility becomes high. Moreover, an increase in E_0 prevents two-band valleys from moving to four-fold valleys. That's why the occupancy of two-fold valleys become bigger further. However, when the thickness becomes thinner than 3 nm, two-fold valleys are also affected by the physical thickness and the mobility decrease again.

As a result, it is indispensable to decrease the size of the device because the performance characteristics improve, but the miniaturization technology has a limit in which the several

deteriorations will happen.

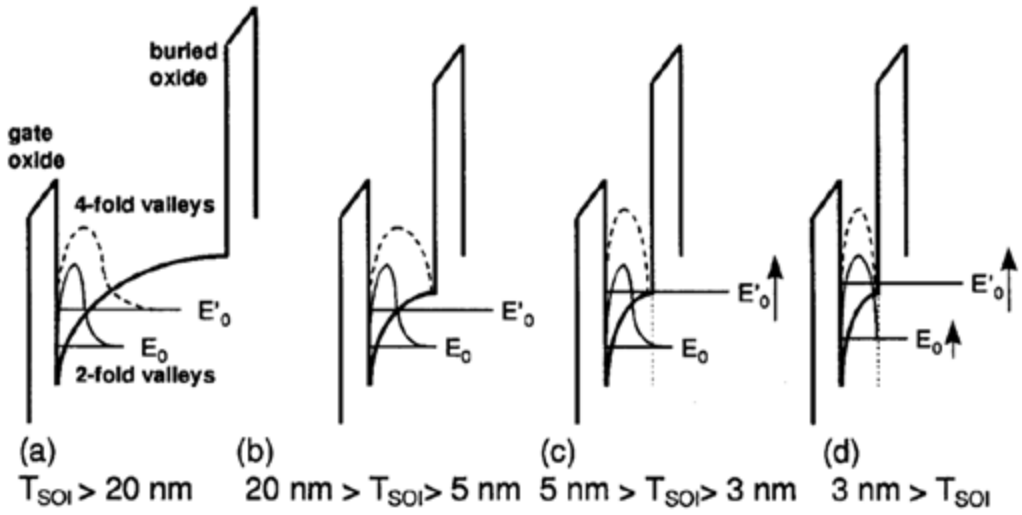


Figure 2.4 Conduction band of SOI MOSFETs with different TSOI [2.5].

2.3 Two-dimensional material, MoS_2

In order to break the scaling limit like that said in section 2.2, many presentations have been done, especially in recent year, transition metal dichalcogenides (TMDs) have been attracted attention because they have a good electronics, optical, mechanical, and thermal properties [2.6-2.9]. The first TMDs material which has been attracted is Graphene. It was found by Novoselov, *et al*. in 2004 and this was a concept of novel award. One of the most remarkable properties is very high mobility. It was found that Graphene has extremely more than 100 times higher carrier mobility (>10^5 cm^2/V-s) than Si at room temperature on SiO_2 substrate. Although Graphene doesn't have any Bandgap and it is a very significant challenge for application toward the electrical devices, it has been researching all over the world because it has not only high mobility but also mechanical properties such as flexibility and permeability.

On the other hand, molybdenum disulfide (MoS_2) is also a family of TMDs and has been used as a solid lubricant and it also has been attracted because of its good properties.

First, MoS_2 can keep high mobility even if it becomes a thin film as in Figure 2.5 [2.4,2.6, 2.10]. In this graph, the mobility of Si decreases dramatically when the thickness becomes smaller than 3 nm. On the other hand, the mobility of MoS_2 keeps around 700 cm^2/Vs in even atomically thin regions. That's why MoS_2 has a possibility which breakthrough the scaling limit as described in section 2.2.

Second, the mechanical properties of MoS_2 are also good. The structure of MoS_2 is layered as shown in Figure 2.6 [2.10]. Between layers, the van der Waals force only militates, so MoS_2 is suited to make a thinner film. Moreover, MoS_2 is thin substances by nature because the distance of layers is 0.65 nm and this number is relatedly small [2.10].

Third, MoS_2 has an energy bandgap that enables us to apply it for semiconductor device and graphene doesn't have as shown in Figure 2.7. The conduction band of MoS_2 is made by the

orbital-4d of Mo and the valence band of MoS_2 is derived from orbital-3p of S and orbital-4d of Mo. It is reported that the bandgap of Bulk and a few layer MoS_2 is 1.2 eV and that of monolayer MoS_2 is 1.9 eV [2.11]. These numbers are calculated by the first principle calculation. As shown in Figure 2.8, furthermore, the type of transition changes by the number of layers. Monolayer MoS_2 has a direct bandgap, but Bulk and a few layers MoS_2 has indirect bandgap [2.11].

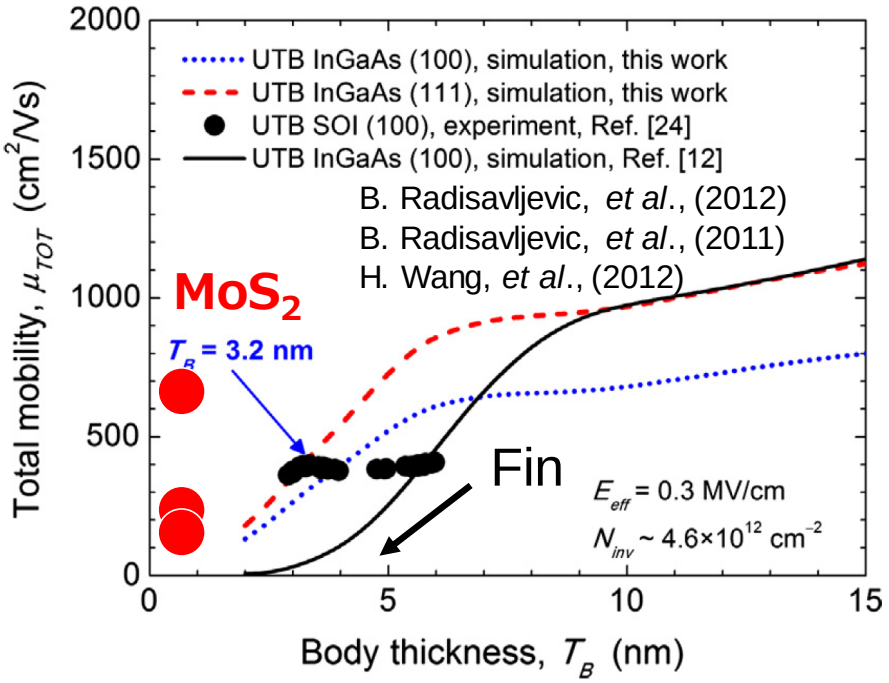


Figure 2.5 Mobility of Si, InGaAs and MoS_2 v.s. thickness [2.4,2.6,2.10].

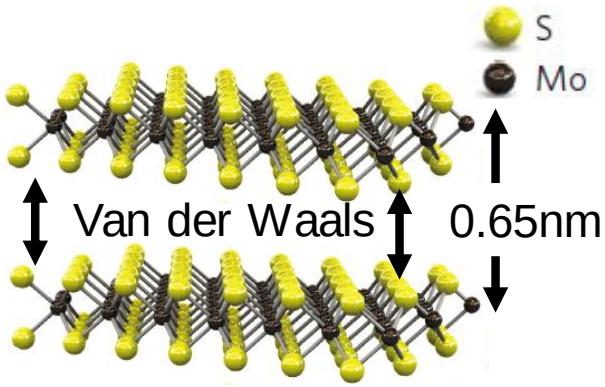


Figure 2.6 The schematic illustration of MoS_2 [2.10].

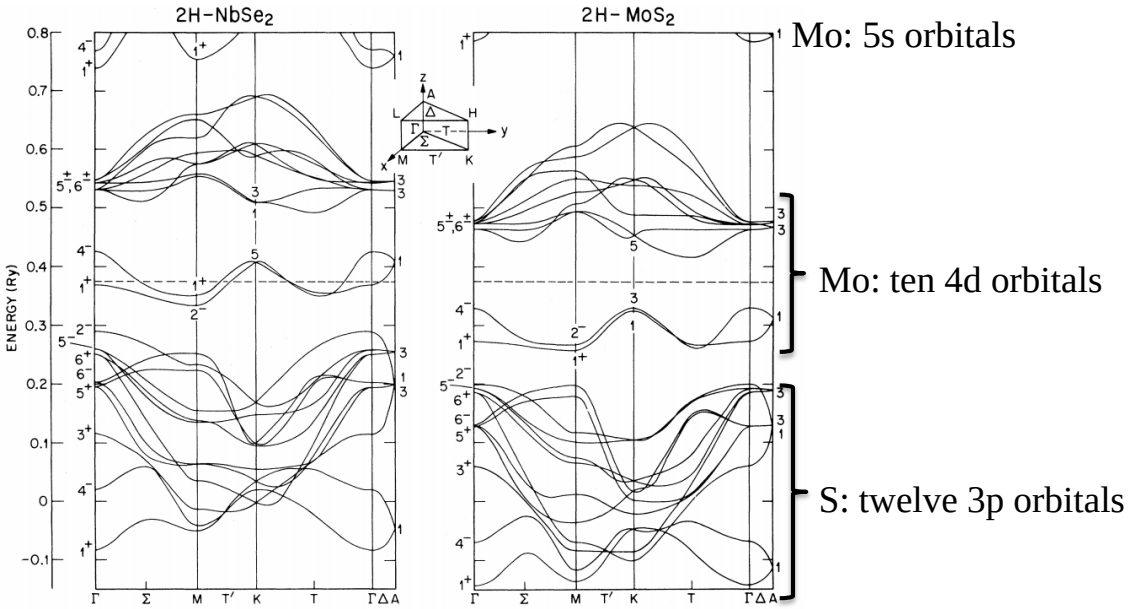


Figure 2.7 Band structure of MoS_2 [2.9].

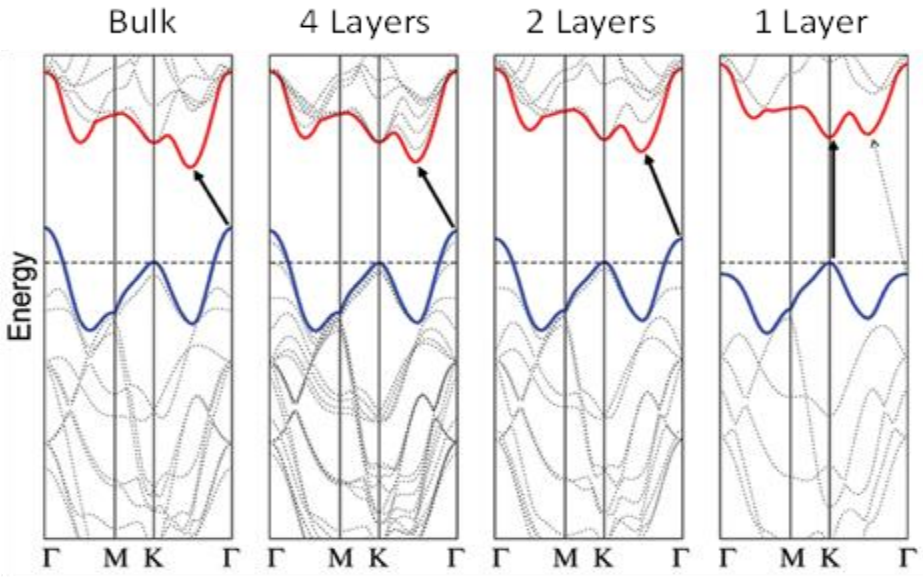
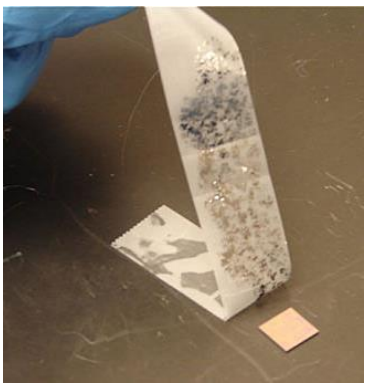


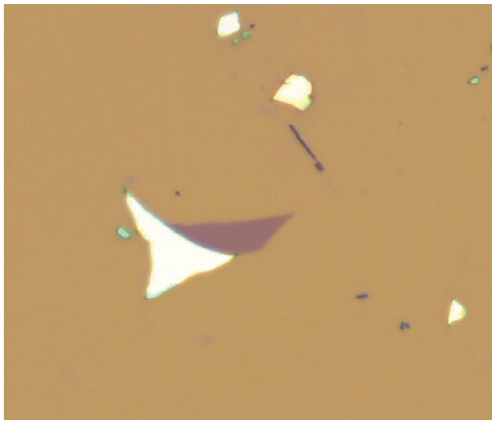
Figure 2.8 Calculated band structure of each layer MoS_2 [2.11].

2.4 Previous reports of MoS_2 FET by several synthesis methods

From the above, it is obvious that MoS_2 has good characteristics, but there are some problems with the application for channel materials. The problems are that the method which makes a large and uniform MoS_2 film without contamination is not established. Conventional synthesis methods for MoS_2 film are exfoliation, CVD and MOCVD. Figure 2.9 shows the MoS_2 film by exfoliated method [2.10]. Exfoliated method enables us to make good quality films but it is not possible to make a large film. The size of an MoS_2 thin film transferred by the exfoliation method is approximately the order of few micrometers. Moreover, it's carrier density becomes automatically high (up to 10^{20} cm^{-3}) [2.10] because of contamination by alkali metal as shown in Figure 2.10 [2.12]. In this graph, it is shown that there is pinning close to E_c by Sodium near from interface between MoS_2 and SiO_2. In CVD process, generally, Mo or MoO_3 and sulfur powder are used as the precursors, and a MoS_2 film is synthesized. Recently, the synthesis of a large-monolayer MoS_2 film has become possible by the CVD process as shown in Figure 2.11 [2.6,13,14]. However, perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) which decreases the surface energy of the substrate is necessary to synthesize the uniform MoS_2 film as shown in Figure 2.12 (a) [2.6]. MoS_2 is affected by the pinning effect when there are alkali metals between MoS_2 film and the substrate [2.15,16]. Figure 2.12 (b) shows the current-voltage characteristics of the CVD-MoS_2 FET. The contamination causes an increase in the carrier density of MoS_2 film automatically and inducing the normally-on operation. In addition, Metal Organic-CVD (MOCVD) synthesizes a large-monolayer MoS_2 film on the 4-inch wafer directly and it shows the high coverage [2.17]. However, the organic precursors in the case of MOCVD lead to contamination by carbon and some of them are toxic [2.18].



(a)



(b)

Figure 2.9 (a) Transfer the MoS_2 film to a substrate by scotch tape and (b) MoS_2 flake made by Exfoliation methods [2. 10].

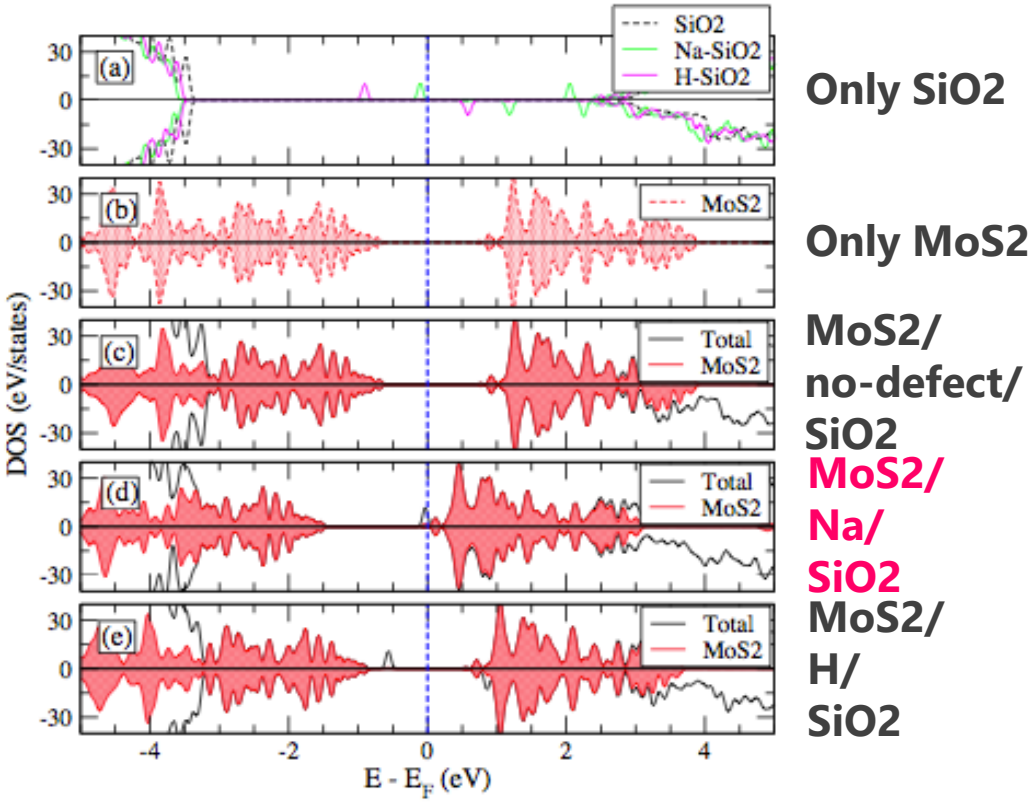


Figure 2.10 DOS by first principal calculation when it is contaminated by various materials [2.12].

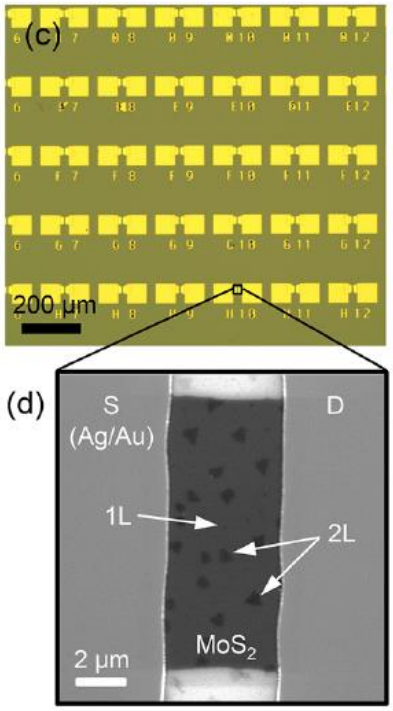
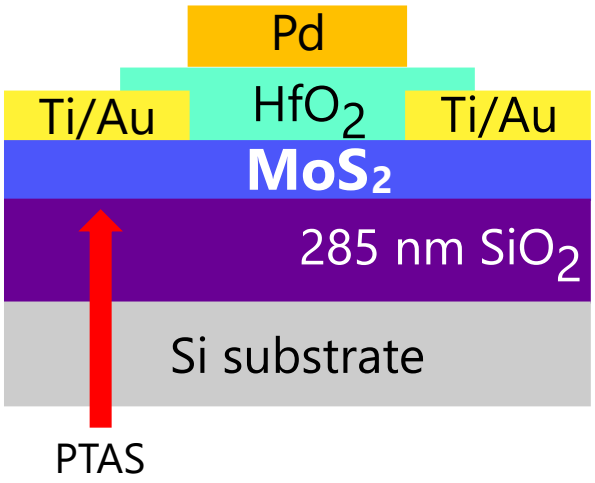
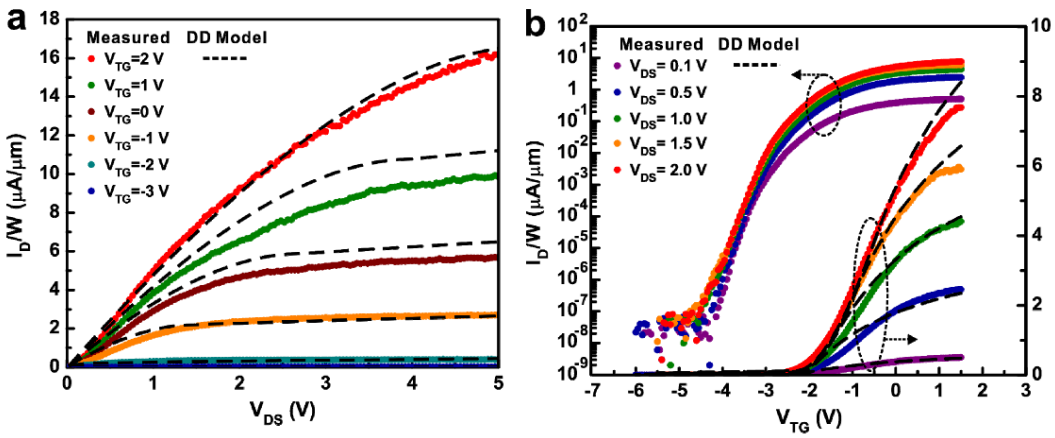


Figure 2.11 Large scale MoS_2 FET synthesized by CVD with back gate [2.14].



(a)



(b)

Figure 2.12 (a) Structure of CVD monolayer-MoS_2 FET with PTAS and (b) I-V characteristics [2.6].

2.5 Ultra High Vacuum (UHV) radio frequency (RF)-magnetron high-temperature sputtering

To resolve the challenges as denoted in previous sections, we selected radiofrequency (RF)-magnetron sputtering as the deposition method for MoS_2 thin and large film in clean ambient. Figure 2.13 shows schematic drawing of RF-magnetron sputtering. In this method, The MoS_2 film is deposited on SiO_2/Si substrate using UHV RF-magnetron sputtering with 80-mmϕ MoS_2 target. In this method, the atoms of target emerge because of the bombardment of Ar ions which are produced and accelerated by high applied voltage and the atoms accumulate and grow on the substrate because of electric potential difference between the target and substrate. As a result, the atoms which can arrive at the substrate synthesize each other, we can deposit a thin and large film. In this paper, we adjusted the several parameters of sputtering, for example, purity of the target, RF power, distance between the MoS_2 target and the substrate, Ar partial pressure. It is known that when the substrate temperature is high during sputtering, the amount of Mo-S bonding increases and the crystallinity improves [2.19]. Figure 2.14 shows the Raman peak intensity depending on the substrate temperature of deposition normalized by the Si intensity of the substrate. In this Figure, the increase in the amount of Mo-S bonding can be seen. Figure 2.15 (a) and (b) show the decrease in full-width at half maximum (FWHM) with an increase in substrate temperature which means the crystallinity improves. This is because the migration works successfully during sputtering by increasing substrate temperature.

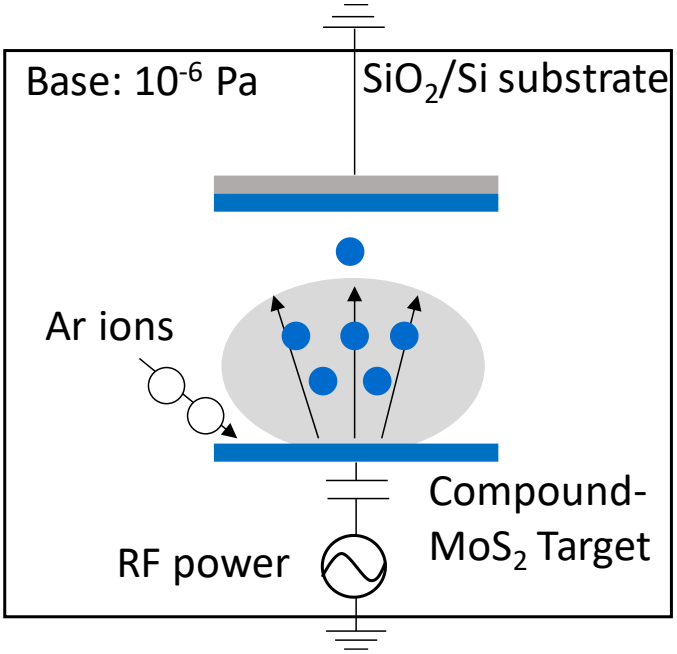


Figure 2. 13 Schematic drawing of RF-magnetron sputtering.

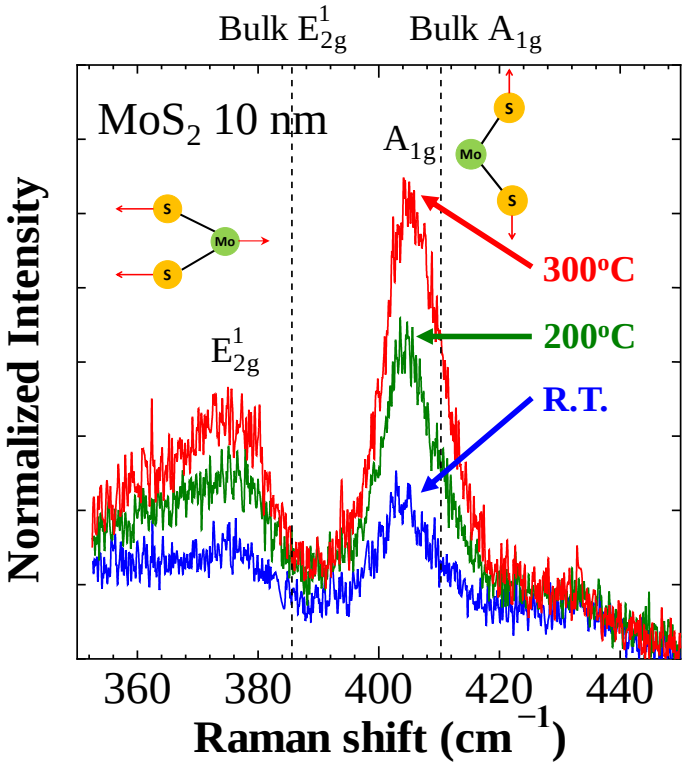


Figure 2.14 Raman spectra of MoS_2 film (10 nm thick) deposited at various substrate temperatures [2.19].

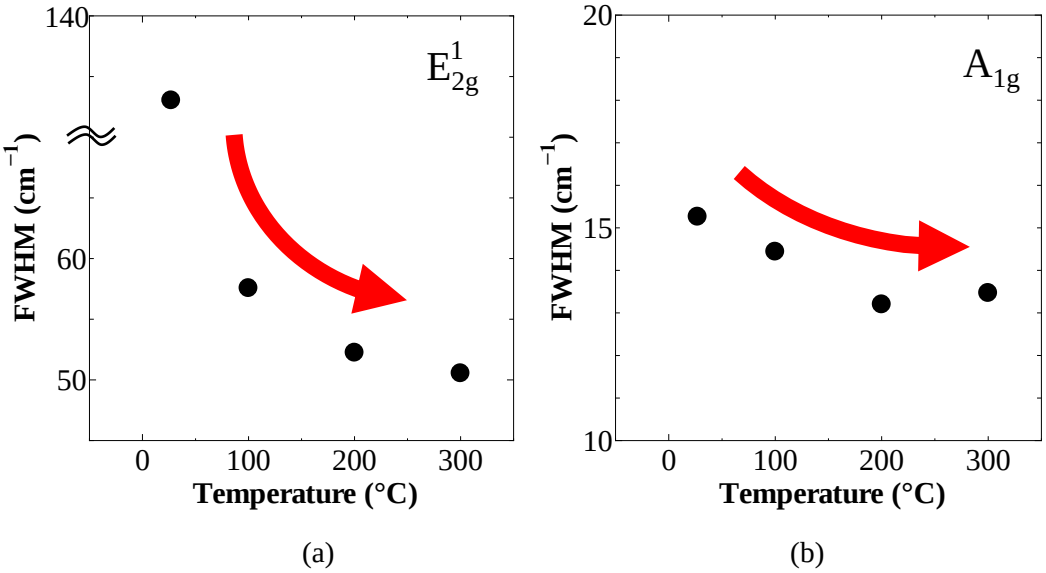


Figure 2.15 Full width at half maximum (FWHM) value of (a) E^1_{2g} and (b) A_{1g} [2.19].

However, there is still a significant challenge in sputtered MoS_2 film. When the quality of

as-sputtered MoS_2 film by XPS, the S/Mo composition ratio was 1.76. This result means that there are sulfur vacancies in sputtered MoS_2 film. In addition, previous work shows the sulfur vacancies play as a dopant because sulfur vacancies generate states with an energy level of 0.3 eV near the conduction band edge in monolayer MoS_2 film as shown in Figure 2.16 [2.20,2.21]. This leads to high carrier density. It was known that high career density results in depletion mode in accumulation transistor by simulation. Figure 2.17 shows the structure of the simulated device and the change of threshold voltage versus gate voltage when the impurity density of channel decrease is shown in Figure 2.18. In this Figure, the threshold voltage becomes plus when the impurity density becomes one-thousandth times as small as that of the reported device. $N_{ch}=1.5\times10^{20}$ cm^{-3} is the channel carrier density. Moreover, the suppression of short channel effect made by decreasing impurity density is shown. According to this Figure, enhancement- mode is possible until the gate length becomes shorter than 60 nm.

As a result, in order to realize the enhancement-mode MoS_2-MOSFET, it is important to make the carrier density decrease in the channel.

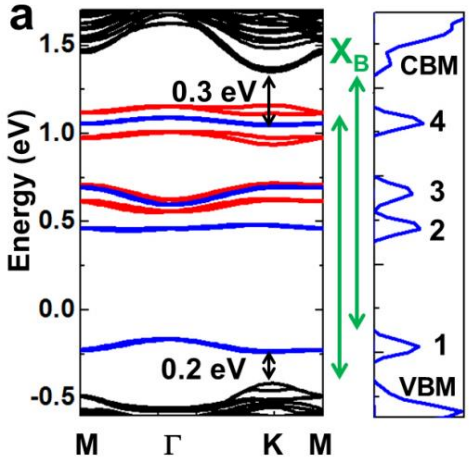


Figure 2.16 Calculated band structure of mono layer MoS_2 and energy level of sulfur vacancy [2.20,2.21].

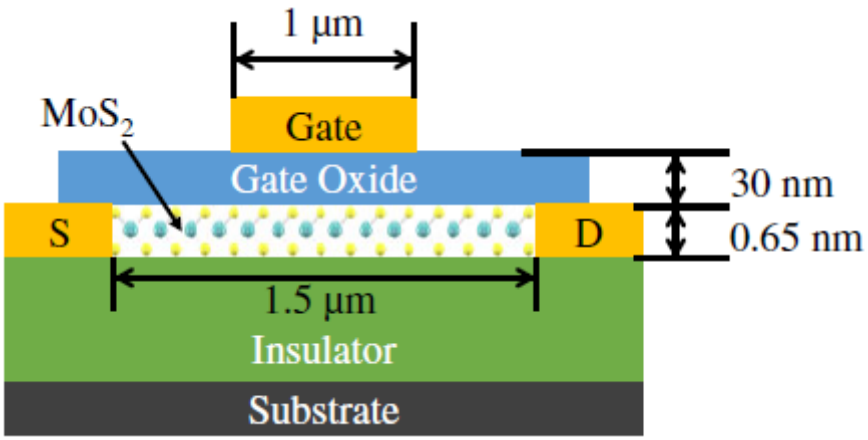


Figure 2.17 The structure of the device for the simulation [2.19].

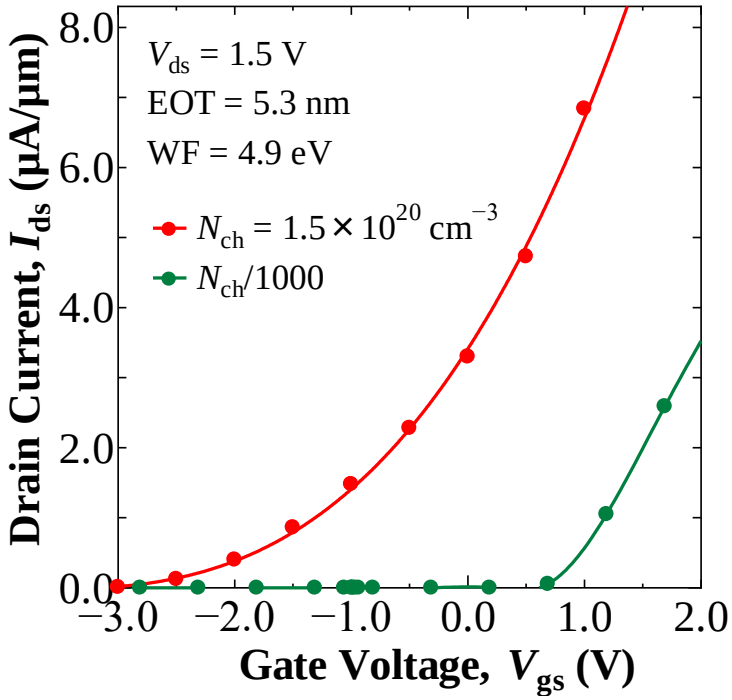


Figure 2.18 Threshold voltage shift by decreasing impurity density [2.19].

In addition to the sulfur vacancies, sputtered MoS_2 film has another challenging, small grain size. The grain size of the sputtered MoS_2 film was extracted as 10 nm at most [2.19]. This value is smaller than that of exfoliation and CVD methods (μm order at least). This is because the

number of nucleation which can arrive from the substrate to the substrate is significantly high. Before the first nucleation grows, the second nucleation is deposited on it and the conflict between them happens frequently. As a result, the grain size becomes small. The optimization of the sputtering condition is necessary to control the nucleation.

2.6 Methodology to design 2-D FET in this thesis

Figure 2.19 shows the methodology to design 2-D FET in this thesis, which includes to design the V_{off} and I_{off} according to boundary conditions of V_{dd}. On the other hand, further design from V_{th} is future work due to the difficulty to precisely design the primitive sputtered MoS_2 *n*MISFETs. In this thesis, set of V_{off} and I_{off} were achieved and the promising approach to improve the FET performance is discussed in the following sections.

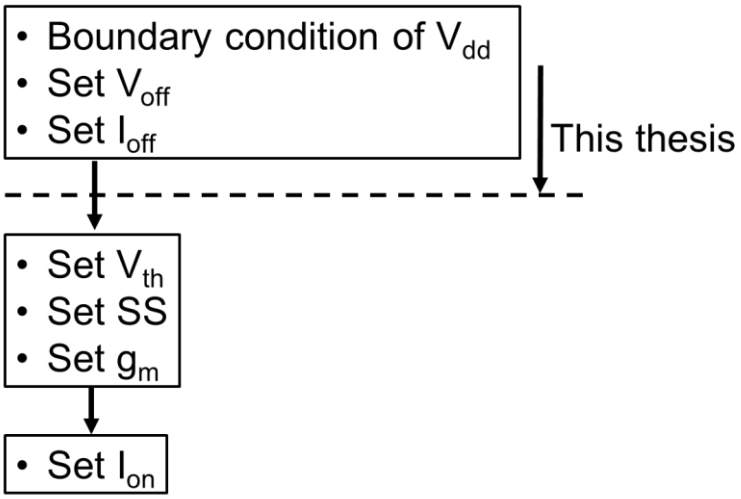


Figure 2.19 Methodology to design 2-D FET in this thesis.

2.7 Summary

In this chapter, the scaling rule and its limit of modern device miniaturization technology with a focus on Si are explained. One of the causes of scale limit is mobility degradation when Si becomes extremely low due to phonon scattering. On the other hand, MoS_2 has high mobility of 200 cm^2/V-s even when it is atomically thin because it has the layer structure and there are no dangling bonds in the out of the plane direction. MoS_2 has flexibility and transparency. Therefore, MoS_2 is expected to apply for IoT and wearable electronics. However, one of the challenges for realizing the industrial application of MoS_2 film is contamination during deposition. RF-magnetron is selected because it can deposit a thin and large MoS_2 film in clean ambient. Although sputtered MoS_2 has sulfur vacancies and small grain size, the bunch of technologies can solve them as mentioned in the following chapters.

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Chapter 3 First report of top-gate sputtered MoS_2-*n*MISFETs with H_2S annealing, TiN contact and Al_2O_3 passivation

3.1 Background

As discussed in chapter 2, sputtered MoS_2 thin film has the small grain size around 10 nm and it leads to an instability against liquids such as deionized (DI) water. This small grain size means that there are many edges in the sputtered MoS_2 film. Because these many edges lead to strong polarity, namely, hydrophilic, water molecules can enter into sputtered MoS_2 film easily [3.1]. Figure 3.1 is scanning electron microscope (SEM) image of MoS_2 film which was peeled by DI water. We have already confirmed that MoS_2 film is peeled if the sidewall of MoS_2 film isn't covered. Wet process is essential for fabricating FET, therefore, this challenge should be resolved by the twice passivation layer.

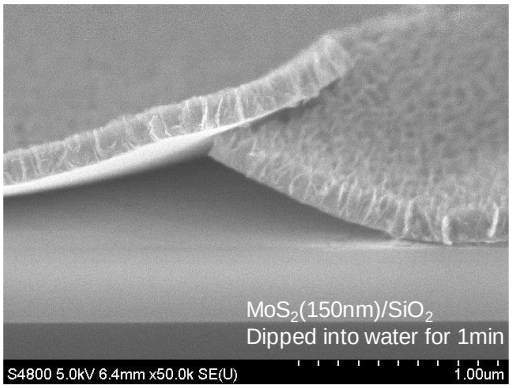

Figure 3.1 SEM image of peeling sputtered MoS_2 film in dipping it into water.

3.2 Experimental procedure

3.2.1 SPM cleaning

To clean and remove particles and organic substances from the structure, SPM is made by H_2SO_4 and H_2O_2 (H_2SO_4 : H_2O_2 = 4 : 1). SPM can remove organic substances because of oxidation effect as following chemical equation,

$$H_2SO_4 + H_2O_2 \rightarrow H_2SO_5 + H_2O \qquad (3.1).$$

Furthermore, HF treatment is used after SPM cleaning for removing oxide film. The density of HF is 1%. In this study, SPM cleaning was conducted at 120 ^oC for 10 minutes.

3.2.2 Photolithography

Photolithography is a prevalent technique that forms a pattern on the substrate utilizing the photoresist and ultraviolet (UV) light. The processes of photolithography are illustrated in figure 3.2 [3.2]. First of all, the photoresist is coated on the substrate and UV light is exposed toward it through photomask which the pattern is designed. Then, the substrate with photoresist is dipped into developers such as tetra-methyl-ammonium-hydroxide (TMAH) and the photoresist is patterned as the photomask is designed because photoresist is developed only where the UV light is exposed if we use the positive photoresist. If we use the negative photoresist, it is developed only where the UV is not exposed. After development, we can introduce an etching process and the substrate is etched only where the photoresist is developed. From the above, we can pattern the substrate as we want. In order to realize more precise exposure, it is necessary to use the light whose wavelength is short. Recently, extreme ultraviolet (EUV) light whose wavelength is 13.5 nm was started to be practicalized [3.3].

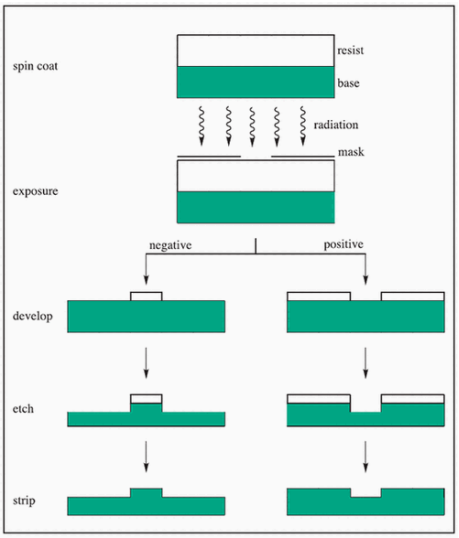

Figure 3.2 Schematic illustration of the photolithography process [3.2].

3.2.3 H_2S annealing

H_2S annealing is introduced to compensate sulfur vacancies and improve the crystallinity in this chapter as shown in Figure 3.3. The temperature and pressure properties of H_2S annealing were discussed [3.4]. H_2S annealing confirmed that it can reduce Full-Wide-Half-Maximum (FWHM) and carrier density down to 3.5 x 10^{-17} cm^{-3} in 1 kPa and at 300°C by Raman spectroscopy, XPS and Hall-effect measurement. These results indicate that H_2S anneal compensate sulfur vacancies and suppress an increase in carrier density. However, Electron mobility of annealed MoS_2 film at 400°C was lower than one at 300°C. This is because the H_2S gas was decomposed more than 400oC. Therefore, H_2S annealing is conducted in 1 kPa and 300°C Finally, Electron mobility was increased from 2.5 up to 12.1 cm^2/V-s using conditions.

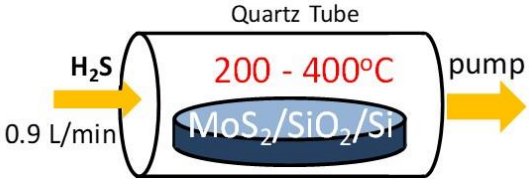

Figure 3.3 Schematic illustration of H_2S annealing [3.4].

3.2.4 Atomic layer deposition (ALD)

ALD is a technique that enables us to deposit one atomic layer by utilizing the self-limiting proper of it. Therefore, ALD has several merits over physical vapor deposition techniques and CVD. For example, ALD can deposit a very thin film on structures. Coverage tends to be high and ALD is expected to be applied toward various areas such as display, Organic electro-luminescence, solar cell and so on. As shown in Figure 3.4, ALD process repeats four steps that are the introduction of precursor, purge, the introduction of another precursor, purge in order to deposit an atoms layer by layer [3.5]. Utilizing several precursors, we can deposit many materials such as Al_2O_3, SiO_2 and so on.

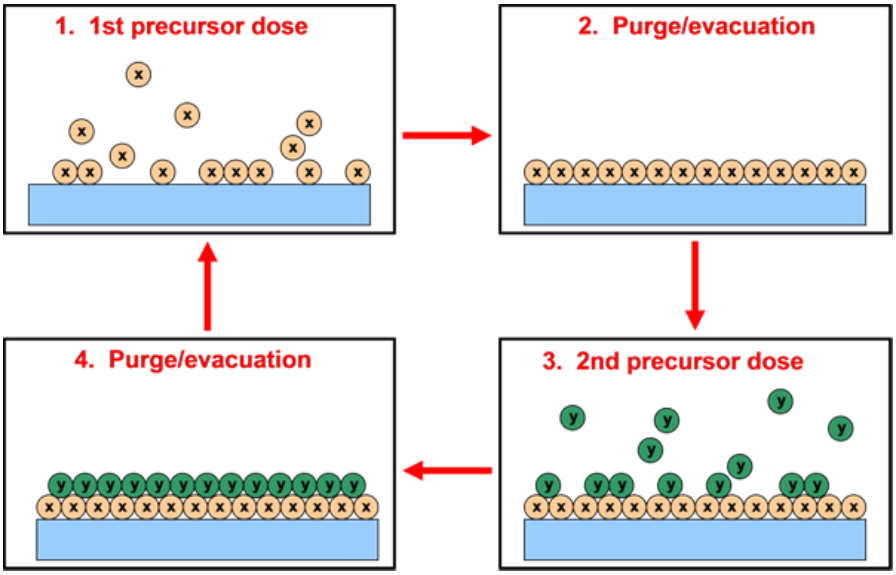

Figure 3.4 Schematic illustration of ALD process [3.5].

3.2.5 Reactive ion etching (RIE)

RIE is plasma etching technology for realizing nano or micro-patterning and any liquids are not used. Figure 3.5 is schematic illustration of RIE process [3.6]. In this study, this process is used for isolation of sputtered MoS_2 film as well because of its instability of liquids. In this process, RF power is applied to the powered electrode for ionizing etching gas and generating plasma, and

the other electrode is ground. Once stabilizing the plasma, DC power is applied to make the ion move to the substrate from bulk plasma and conflict with each other. Then the sputtering and chemical reaction between ions and substrate happens. Thus we can fabricate the precise structure. In the case of RIE, the anisotropic etching is possible as well. The density of bulk plasma depends on the RF-power mainly. Thus, the speed of etching can be controlled by it.

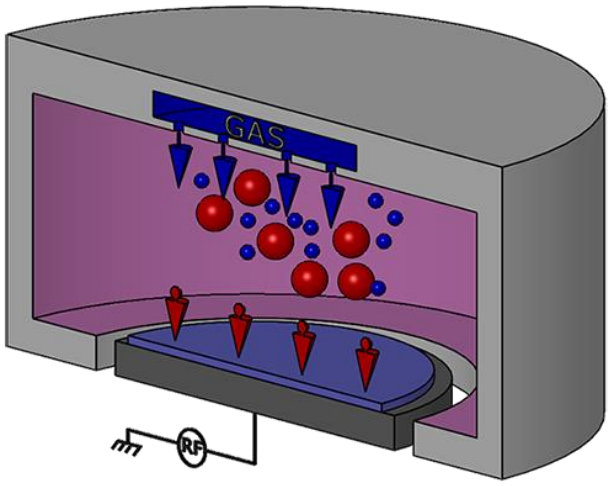

Figure 3.5 Schematic illustration of RIE process [3.6].

3.2.6 Scanning electron microscope (SEM)

When the size of the objective which we want to observe is less than 1 um, it is difficult to observe by optical microscope. SEM is an electron microscope that irradiates an electron beam to the objective in order to observe the surface of it at high magnification. SEM can enable us to analyze the elements if the x-ray detector is attached, too. The electron beam is accelerated at 100~300 kV and the convergent lens and objective lens focus the accelerated electron beam on the objective. Scanning coil moves the spot of electrons to the objective as a prove. Electron detector detects the signal electron which arises from the irradiation point of electron beam. In SEM images, the amount of signal electron is displayed as the brightness. Owing to prevent the

electron and gas molecules from conflicting with each other, the pressure is evacuated down to 10^{-2}~10^{-3} Pa.

3.2.7 Transmission electron microscope (TEM) and scanning transmission electron microscope (STEM)

TEM and STEM are also electron microscope and they enable us to obtain the image of the objective at a higher magnification than SEM. The difference between SEM, TEM and STEM as follows. In the case of TEM, the electron beam which transmits through the objective is focused on the fluorescent screen or CCD camera directly. Therefore, we can observe the inside of an objective at higher magnification by using a transmitting electron. On the other hand, the electron beam scans the surface of an objective and an arising secondary electron is focused in the case of SEM as mentioned in the previous section. Higher acceleration voltage and vacuum are necessary to make the electron beam transmit an objective.

STEM is one kind of TEM, however, the electron beam is scanned at the surface of an objective to get an image same as SEM. Using the detector especially for the dark-field image, we can obtain images in which heavy atoms are projected brightly and it is possible to observe the interface of several materials precisely. Figure 3.6 shows the optical system of TEM and STEM [3.7].

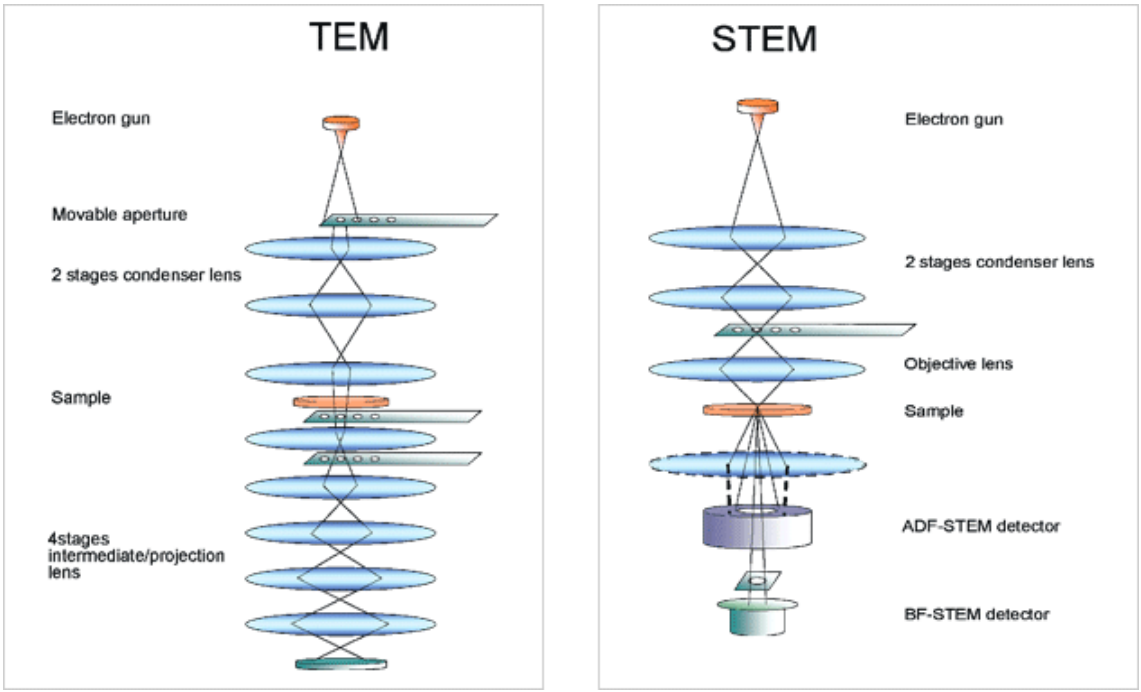

Figure 3.6 Schematic illustration of TEM and STEM [3.7]

3.3 Device fabrication process

Figures 3.7 is process flow of sputtered MoS_2-*n*MISFETs. TiN of 50-nm thick was patterned by lift-off process as the source and drain (S/D) regions for n-type operation, and then the MoS_2 film of 3-nm thick was deposited directly on SiO_2/Si substrate by RF sputtering [3.8]. The conditions were an RF power of 50 W, the distance between the target and substrate of 150 mm, substrate temperature of 400°C, argon (Ar) flow of 7.0 sccm, and partial pressure of 0.55 Pa. And then, the MoS_2 film was annealed in H_2S gas at 400^{o}C in 1 kPa for 10 min for sulfur compensation and crystallinity improvement, simultaneously. For both passivation and dielectric functionalities, the first Al_2O_3 film of 20-nm thick was deposited by Atomic Layer Deposition (ALD) method. After an isolation patterning of MoS_2 channel by the Reactive Ion Etching (RIE) with Cl_2 gas, the second Al_2O_3 film was deposited especially for the passivating sidewall of MoS_2 film. Consequently, the total thickness of Al_2O_3 films is approximately 27 nm because the thickness of the 1st Al_2O_3 film was reduced during an isolation process. TiN top-gate of 150-nm thick was pattered by the RIE with Cl_2 gas. Bird's-eye view and cross-sectional illustration of chip-level-integrated MISFETs are shown in Figures 3.8 and 3.9, respectively. To evaluate the structure of the sputtered MoS_2 film, cross-sectional Transmission Electron Microscopy (TEM), Energy Dispersive X-ray (EDX) spectroscopy and Scanning Transmission Electron Microscopy (STEM) are conducted.

- SPM cleaning at 180°C for 10 min
- S/D photolithography
- TiN (50 nm) sputtering at RT
- S/D-contact resist removal
- MoS_2 (~ 4 nm) sputtering at 400°C
- H_2S annealing in 1 kPa at 400°C
- 1st Al_2O_3 deposition by ALD at 300°C with TMA and H_2O as passivation and dielectric films
- Active-definition photolithography
- MoS_2 RIE and resist removal
- 2nd Al_2O_3 deposition by ALD at 300°C with TMA and H_2O as passivation and dielectric films
- Gate TiN (150 nm) sputtering at RT
- Gate photolithography
- Gate TiN RIE and resist removal

Figure 3.7 Process flow of chip-level integration for sputtered MoS_2-*n*MISFETs with RIE-defined TiN top gate.

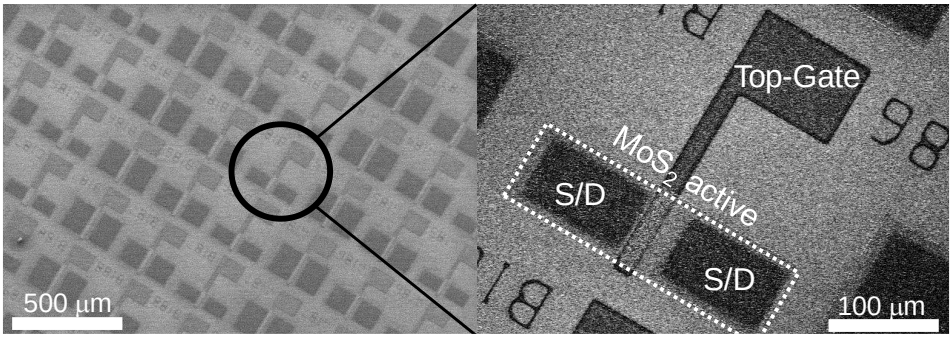

Figure 3.8 Bird's-eye views of chip-level-integrated *n*MISFETs with RIE-defined MoS_2 active.

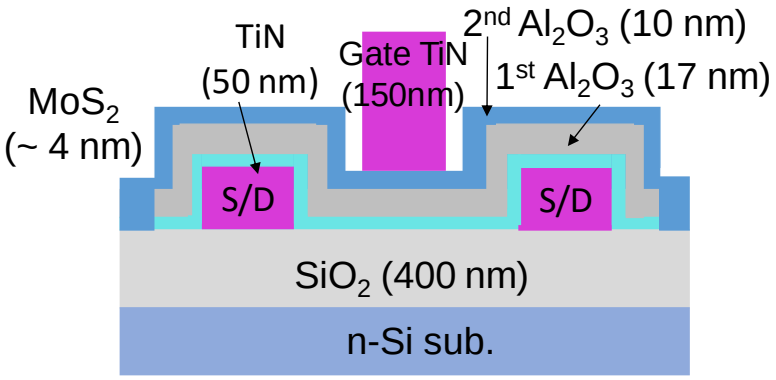

Figure 3.9 Cross-sectional illustration of sputtered MoS_2-*n*MISFET with ALD-Al_2O_3 dielectric film, RIE-defined TiN top gate. This MISFET drives as junction-FET.

3.4 TEM and STEM observations

A cross-sectional TEM image in Figure 3.10 shows overall features of the H_2S-annealed MoS_2 film and ALD-Al_2O_3 passivation film of this *n*MISFET. It is confirmed that about five-layers MoS_2 film with uniform thickness is preserved even after device fabrication processes. The average grain size of sputtered MoS_2 film is approximately 10 nm, defined by grain boundaries whose positions are indicated by black allows shown in Figure 3.10. In Figure 3.11, from the cross points between profiles for both aluminum and carbon atoms detected by EDX depth profile, the total thickness of Al_2O_3 film is approximately estimated as 27 nm. Figure 3.12 shows a high-resolution STEM image of the same sample. The expected clear triangles of the Mo-S atomic arrangements are also shown. This result means that H_2S annealing compensates sulfur resulting in a crystallinity improvement of MoS_2 film, which is successfully preserved during twice Al_2O_3 passivation processes. The thickness of one MoS_2 unit is approximately 0.65 nm and these results correspond with MoS_2-crystal characteristics. If we assume that the relative dielectric constant of Al_2O_3 film on MoS_2 channel is estimated as 5.8, the equivalent SiO_2 thickness of our Al_2O_3 film is calculated as 18 nm [3.9].

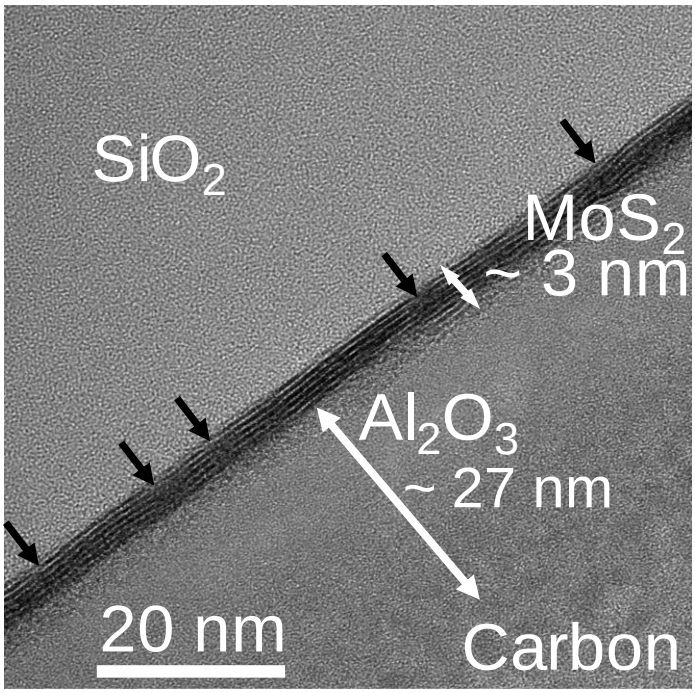

Figure 3.10 Cross-sectional TEM image for H_2S-annealed MoS_2 which has layer structure and ALD-Al_2O_3 films. Black allows show the point of which MoS_2 film breaks.

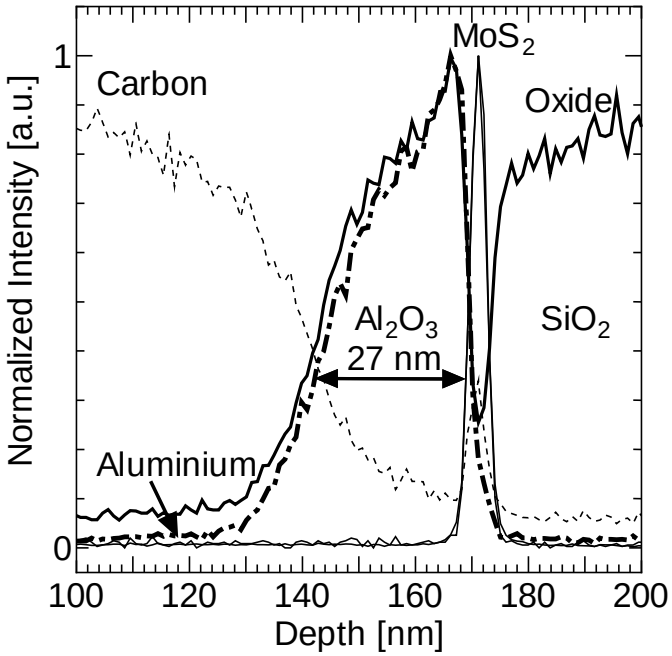

Figure 3.11 EDX depth profile from TEM evaluation in Figure 3.10.

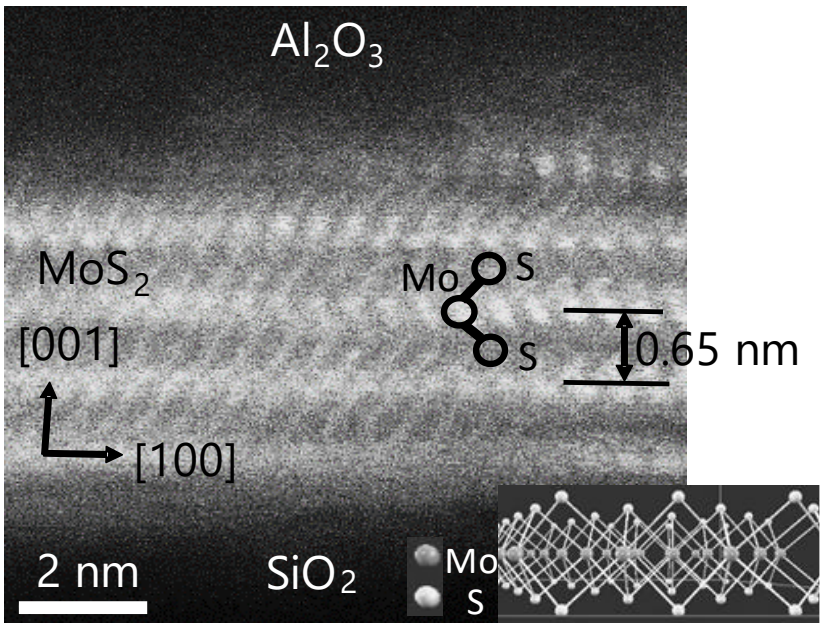

Figure 3.12 High-resolution cross-sectional STEM image from [010] direction for H_2S-annealed MoS_2 film and schematic cross-cut image of MoS_2 crystal.

3.5 I_d-V_{gs} characteristics

Figure 3.13 shows drain current (I_d) – gate voltage (V_{gs}) characteristics of MoS_2-transistor with gate-mask length (L_{ch}) and width (W_{mask}) of 15 and 80 μm, respectively, at drain voltage (V_{ds}) of 0.05 ~ 2.0 V. As shown in this figure, the n-type operation in accumulation mode is confirmed successfully [3.10]. The off voltage (V_{off}) is approximately -3.0 V. The off current (I_{off}) increases as V_{ds} increases and on/off ratio is approximately 20 at V_{ds} of 2.0 V. The origin of small on/off ratio might be large S/D leakage current via crystal defects because the sputtered MoS_2 film has a large number of defects due to the small grain size as shown in Figure 3.14. The original honeycomb structure of MoS_2 can't be observed in this study. Therefore, to improve the crystallinity of sputtered MoS_2 film is still important for reducing leakage current.

Figure 3.15 shows normalized transconductance (g_m) characteristics of the same transistor with Figure 3.14. Maximum g_m is 0.12 μS/μm at V_{gs} of - 2.0 V. Threshold voltage (V_{th}) of - 2.75 V at drain voltage (V_{ds}) of 2.0 V is calcurated and adopted for all V_{ds} values in this paper.

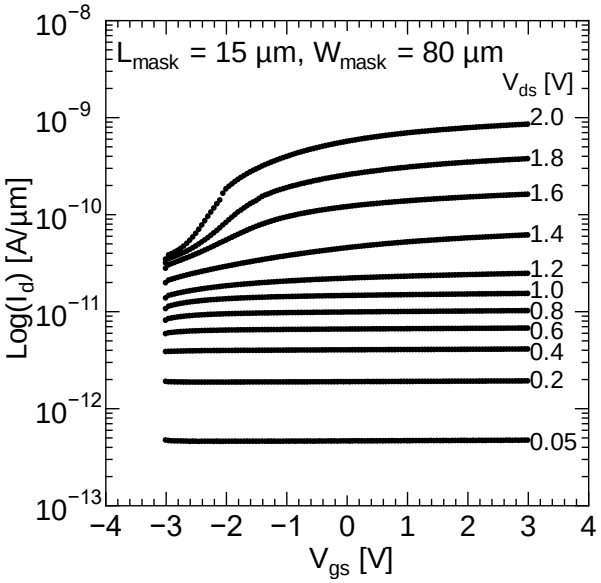

Figure 3.13 Logarithm I_d-V_{gs} characteristics with L_{ch} and W_{mask} of 15 and 80 μm, respectively, at V_{ds} = 0.05 ~ 2.0 V.

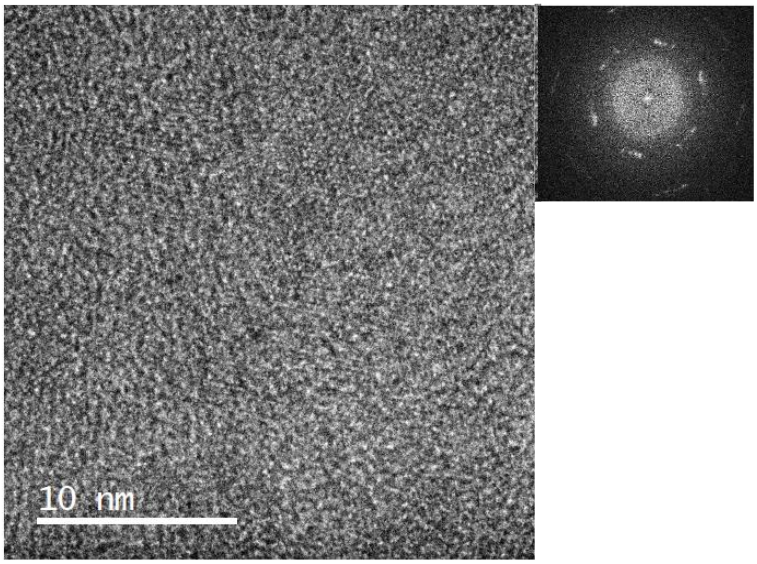

Figure 3.14 Plan image of H_2S sulfurized sputtered MoS_2 film by TEM. The right small image is the results of FFT and polycrystalline MoS_2 film can be seen.

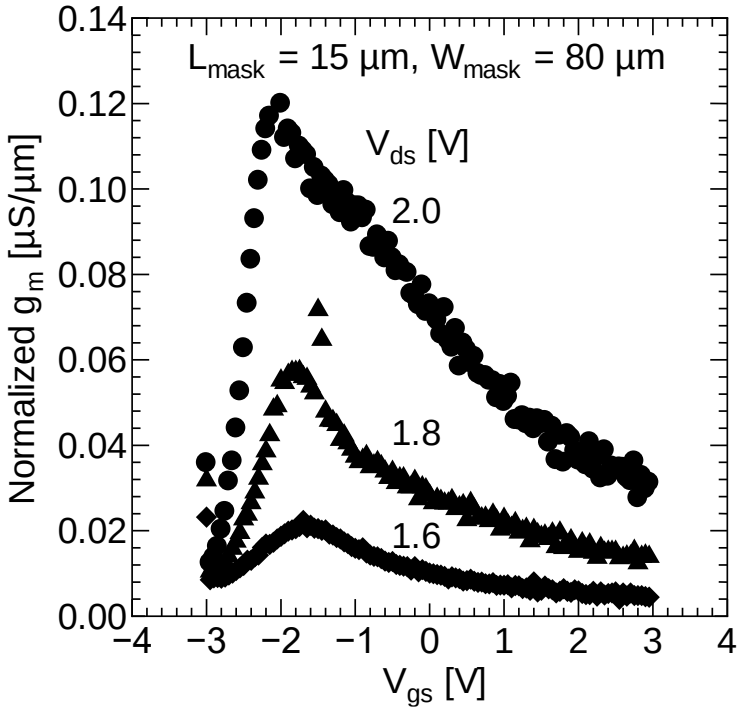

Figure 3.15 g_m characteristics with L_{ch} and W_{mask} of 15 and 80 µm, respectively, at V_{ds} = 1.6, 1.8 and 2.0 V.

3.6 Analysis on the cause of normally-on operation by device simulation

The device simulation is introduced to analyze the cause of normally-on operation and get an insight about how to realize the normally-off operation. Figures 3.16 and 3.17 are the model of simulation and the results, respectively. In this simulation, N_A is a carrier density of MoS_2, Q_f is positive fixed charges of Al_2O_3 film, $Q_{it\text{-}top}$ is an interface trap density between MoS_2 and Al_2O_3 films, and $Q_{it\text{-}bottom}$ is also an interface trap density between MoS_2 and SiO_2 films as shown in Figure 3.16. Table 3.1 shows the parameters of the simulation [3.11,3.12]. Parameter set i was led by the results of the fitting to experiments by simulation. Other parameter sets are calculated by the simulation to evaluate the V_{th}. As a result of the fitting, N_A was as high as 10^{19} cm^{-3} in spite of H_2S annealing which is expected to reduce the carrier density and shift the threshold voltage in positive direction. Higher Q_f and $Q_{it\text{-}top}$ than those in previous reports are also confirmed [3.11,3.12]. The cause of high carrier density is speculated to be carbon contaminations during integration processes rather than insufficient sulfur compensation [3.4]. This carbon contamination can be due to the residual photoresist of S/D photolithography. One possible cause of high Q_f is speculated to be the remaining chlorine atoms during the active definition by RIE onto the first Al_2O_3 film. As a result, the threshold voltage shifts in positive direction further when N_A, Q_f and $Q_{it\text{-}top}$ decrease and the work function of gate metal increases. The two dotted black lines in Figure 3.17 are the result of calculation by (3.2) and match with set i to vi roughly.

$$V_{th} = \phi_{ms} - \frac{Q_f + Q_{it-top}}{C_{Al_2O_3}} + 2\phi_f - \frac{\sqrt{2qN_A\varepsilon_{MoS_2}(2\phi_f + \frac{Q_{it-bottom}}{C_{SiO_2}})}}{C_{Al_2O_3}} \qquad (3.2),$$

$\phi_{ms}(=\phi_m - \chi_{MoS_2} - \frac{E_g}{2} + E_f - E_i)$ is s the difference of work function between MoS_2 and TiN gate metal. $C_{Al_2O_3}$ and C_{SiO_2} are the capacitance of Al_2O_3 and SiO_2, respectively.

ε_{MoS_2} is the permittivity of MoS_2, that is 8.6 x 10^{-13} [F/cm]. $\phi_f \left(= \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)\right)$ [eV] is the Fermi potential. Although there were some assumptions, (1) shows that V_{th} shits in parallel toward positive direction when Q_f and $Q_{it\text{-}top}$ are reduced. N_A is necessary to be less than about 10^{18} cm^{-3} to realize normally-off operation in which V_{th} is positive as indicated by dotted curves in Figure 3.17. Therefore, it is expected to be reduced by removing carbon contamination using acid cleaning. Furthermore, it is valid to reduce Q_f and $Q_{it\text{-}top}$ using the isolation process without chlorine atoms and following post-deposition annealing [3.11,3.12]. Reductions of Q_f and $Q_{it\text{-}top}$ are also effective for realizing low I_{off}.

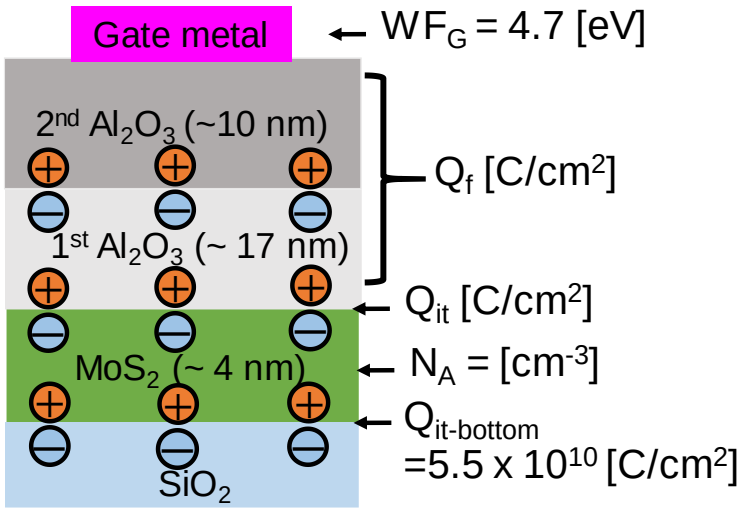

Figure 3.16 Schematic illustration for assumed charges and gate work function in gate stacks.

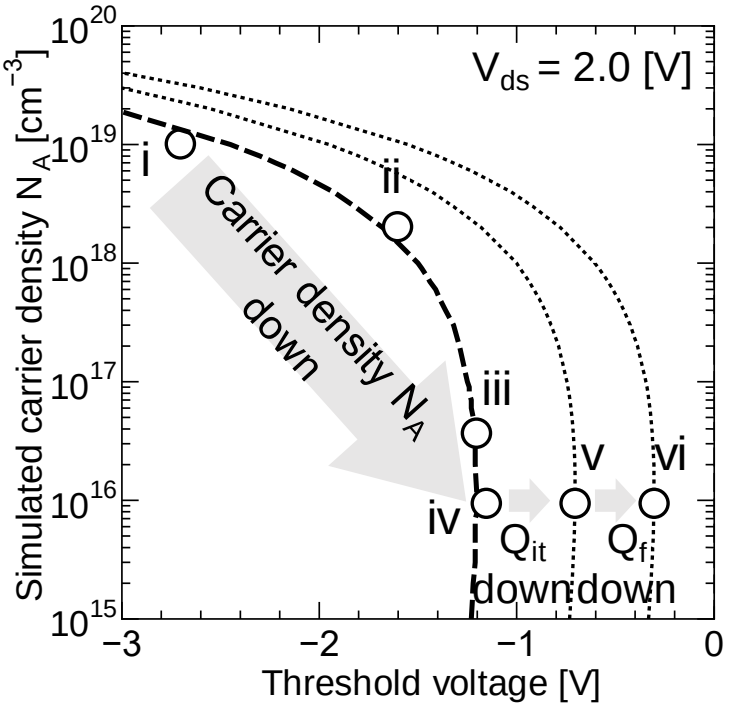

Figure 3.17 Threshold voltages calculated by device simulation considering with parameters in Figure 3.16. The thick dashed line is calculated by physical model and thin dashed lines are based on the analytical equation from the thick dashed line.

Table 3.1 Parameters of device simulation.

	Q_{it} [C/cm^{-2}]	Q_f [C/cm^{-2}]
i ~ iv	1.8 x 10^{12}	2.8 x 10^{12}
v	1.8 x 10^{11}	2.8 x 10^{12}
vi	1.8 x 10^{11}	1.4 x 10^{11}

3.7 I_d-V_{ds} characteristics

Figure 3.18 shows I_d-V_{ds} characteristics with V_{gs} of 1.75 ~ 5.75 V. I_d obviously increases as V_{gs} increases because of electric field effect. However, the contact resistance between MoS_2 and TiN seems to be high. Owing to reduce contact resistance, titanium, molybdenum and scandium are promising candidates of contact metal because these metals have small Schottky barrier height with MoS_2 film [3.13]. In addition, the non-overlap structure of this device causes the high contact resistance. Hence, the overlap structure is also expected to be valid.

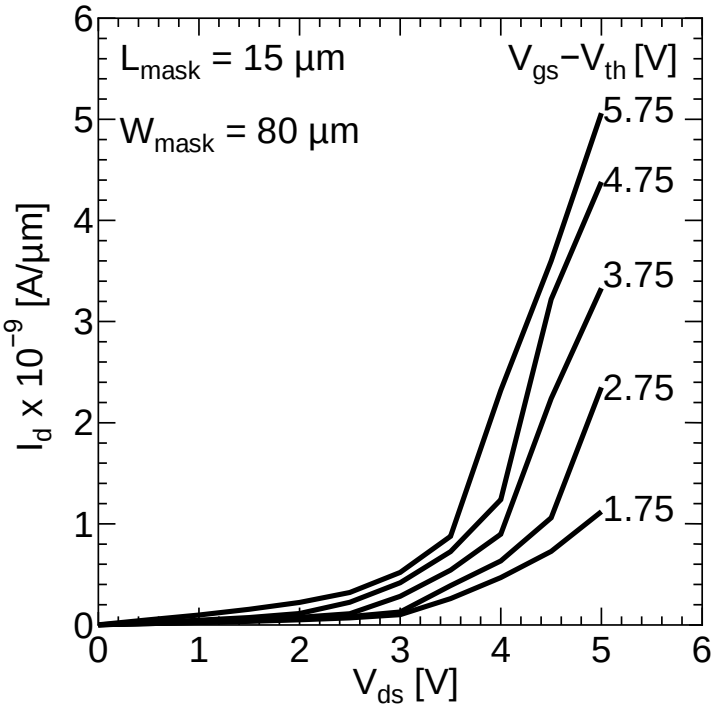

Figure 3.18 I_d-V_{ds} characteristics with L_{ch} and W_{mask} of 15 and 80 µm, respectively, at V_{gs} - V_{th} = 1.75 ~ 5.75 V.

3.8 Resistance dependence on gate length and mobility

In addition, a resistance dependence on L_{ch} value is calculated to extract the parasitic resistances including contact and sheet resistances as shown in Figure 3.19. Because of the successful fabrication of *n*MISFETs, overlap length between gate and S/D ($2\Delta L$) and external resistance (R_{ext}) values are respectively extracted as 14.4 μm and 1.14 x 10^9 Ω-μm. The effective channel length (L_{eff}) is calculated from the following formula,

$$L_{eff} = L_{ch} - 2\Delta L \qquad (3.3).$$

Accordingly, for example, L_{eff} of the device, whose L_{ch} is 15 μm, is calculated as 0.577 μm. $2\Delta L$ has large positive value in spite of the non-overlap structure shown in Figures 3.8 and 9. This is because these MISFETs drive as a junction-FET with S/D region due to sulfur defects during integration processes. The R_{ext} of these MISFETs with a top gate is higher than that of CVD-MoS_2 film with back gate, which is 6.85 x 10^5 Ω-μm [3.14]. Furthermore, the variability of R_{ext} is also high and can cause non-linear relation of Figure 3.19 too. As a result, the peak value of field-effect mobility with deducted R_{ext} is evaluated as 0.11 cm^2/V-s. Figure 3.20 shows the mobility comparison with the channels of silicon and MoS_2 synthesized by three methods [3.4,3.15-3.35]. The mobility of sputtered MoS_2 film is lower than those of exfoliation and CVD methods. If the grain size and R_{ext} are improved, the mobility can be expected to be enhanced. Therefore, to reduce the number of nucleation sites and promote the migration on the substrate are also necessary in order to enlarge the grain size [3.21]. Introducing gate-S/D overlap structure is also effective.

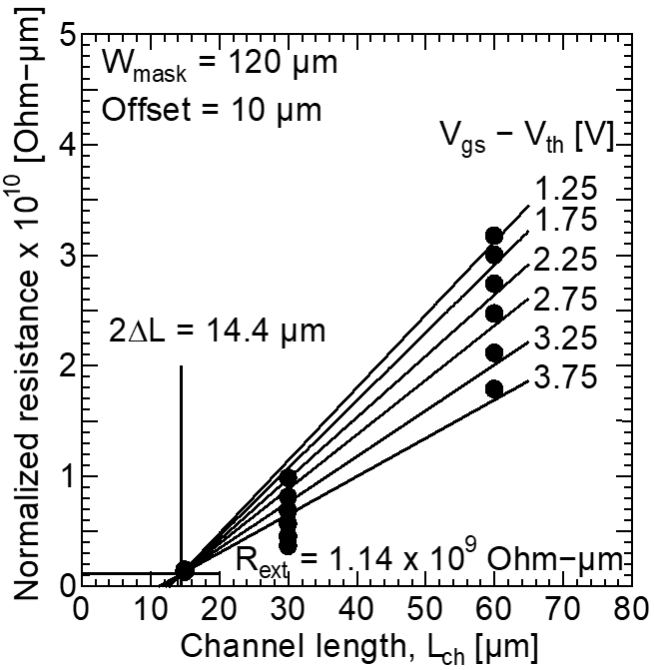

Figure 3.19 Resistance dependence on L_{ch} for W_{mask} of 120 μm.

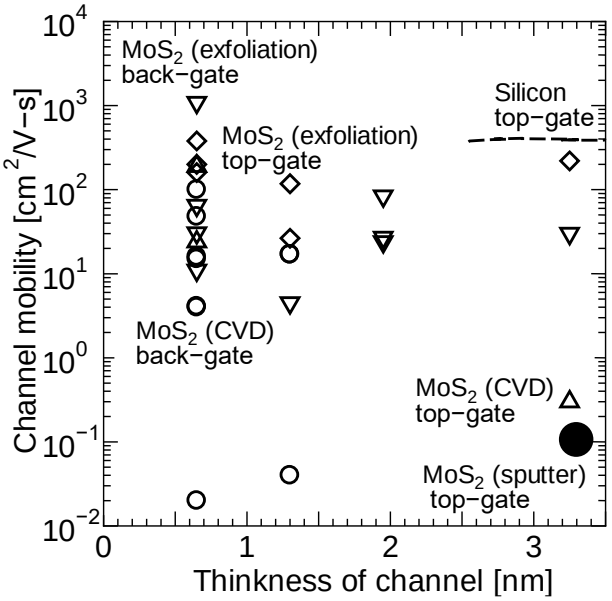

Figure 3.20 Mobility comparison with silicon and MoS_2 synthesized by three methods with top and back gates. Since the mobility of this paper is comparatively smaller than those of almost others, it is required to reduce the resistance value by minimizing contact resistance in our MoS_2 *n*MISFETs [3.4,3.15-3.36].

3.9 Summary

In this chapter, we successfully achieved the top-gate MoS_2 *n*MISFETs and confirmed the operation by adopting a bunch of methods of RF magnetron sputtering, twice Al_2O_3 passivations, and H_2S annealing. The sputtered MoS_2 film was remarkably preserved even after the device fabrication processes. We demonstrated the extraction of the effective gate length and mobility of MoS_2 accumulation *n*MISFETs. Although the mobility is still lower than those using exfoliation and CVD methods, the performance is expected to be improved by reducing R_{ext}, interface-trap density and fixed-charge density of Al_2O_3 film, and this device integration is the substantial first step to realize the integrated circuits with 2D material in the near future.

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Chapter 4 Sulfur Powder Annealing for compensation of sulfur vacancies in sputtered MoS_2 film

4.1 Background

In chapter 3, chip level integrated MoS_2-*n*MISFETs by sputtering, H_2S annealing, and twice Al_2O_3 passivation film is discussed. H_2S annealing plays a role as compensation of sulfur vacancies. It is reported that H_2S annealing improves the composition ratio of sputtered MoS_2. However, H_2S started to be decomposed at high temperature of more than 400°C following chemical equations,

$$H_2S \rightarrow H_2 + S \ (> 441 \ ℃) \quad (4.1),$$

$$8H_2S \rightarrow 8H_2 + S_8 \ (441 \sim 627 \ ℃) \quad (4.2), \text{ and}$$

$$2H_2S \rightarrow 2H_2 + S_2 \ (> 627 \ ℃) \quad (4.3).$$

MoS_2 is reported that it can act as catalysis for decomposing H_2S and the chemical process is different from the temperature [4.1]. As showing (4.2), H_2S is decomposed to $8H_2$ and S_8. S_8 is a large molecule thus the reaction between sulfur and sputtered MoS_2 is expected to be prevented in depth direction. In addition, it is difficult to promote the sulfurization and migration of sputtered MoS_2 film further. In this chapter, the new sulfurization, SPA is proposed. The pressure and temperature dependencies are discussed in terms of the crystallinity, the magnitude of sulfurization and the electrical property in the following sections.

4.2 Experimental procedure

4.2.1 Sulfur powder annealing

In this sulfurization process, two heaters were used, designated 1 and 2, as shown in Figure 4.1. The sulfur powder and sputtered MoS_2 film were placed in a quartz tube. The sulfur powder and the samples were evaporated by heater 2 and annealed by heater 1. The temperature of heater 2 was set to 200°C and the temperature of heater 1 was varied. As shown in Figure 4.2, this process is divided into three time domains, which consist of (i) ramping up the temperatures of heaters 1 and 2 to 700 and 200°C, respectively, under an Ar flow rate of 100 sccm, (ii) sulfurization for 10 min, and (iii) ramping down of the temperature with an increase in the Ar gas flow rate to 1500 sccm over 10 min in order to evacuate the sulfur vapor quickly.

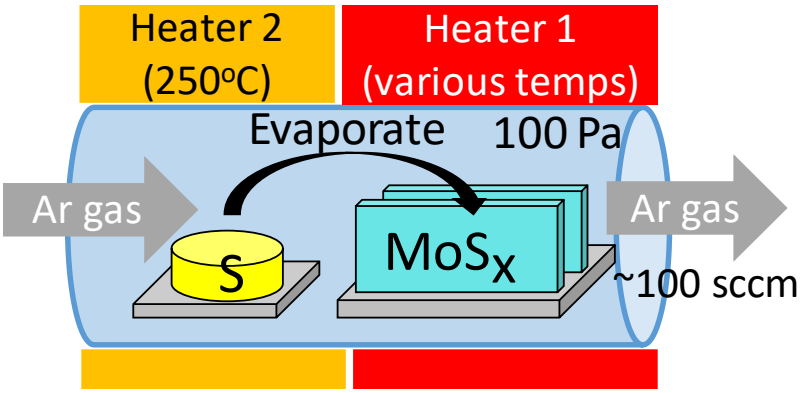


Figure 4.1 Schematic drawing of SPA.

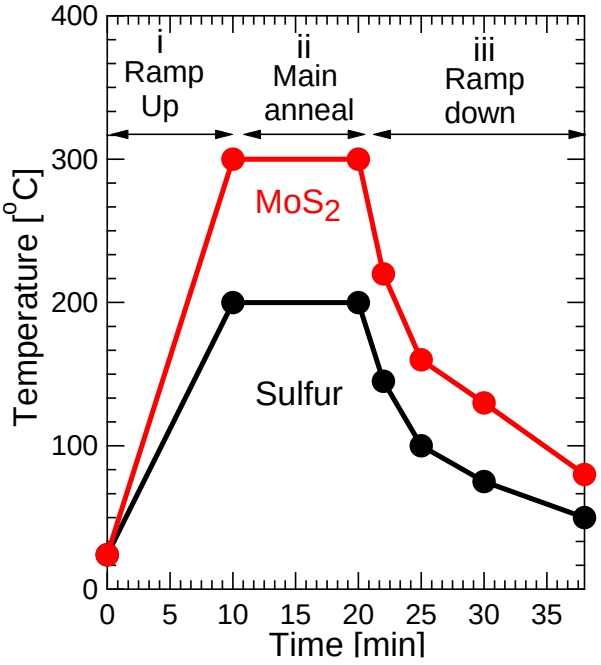


Figure 4.2 Temperature sequence of SPA at 300°C.

4.2.2 X-ray photoelectron spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) enables us to know not only the kind and quantity of atoms but also the condition of chemical reaction. In the case of XPS, the energy distribution of photoelectron which appears by radiation of X-ray is measured. The discipline of the appearing of photoelectron can be described as below.

From the energy of X-ray and photoelectron, the binding energy can be derived;

$$E_b = hv - E_k \tag{4.4}$$

where E_k is the energy of X-ray, hv is the energy of photoelectron, and E_b is the binding energy. "hv" can be selected by us freely when the measurement is conducted. That's why E_b is understood when E_k is measured. E_b is the original value derived from the kind of substance or the condition of electron, so it is possible to understand the condition of a chemical reaction and identify the kind and amount of atoms from this number.

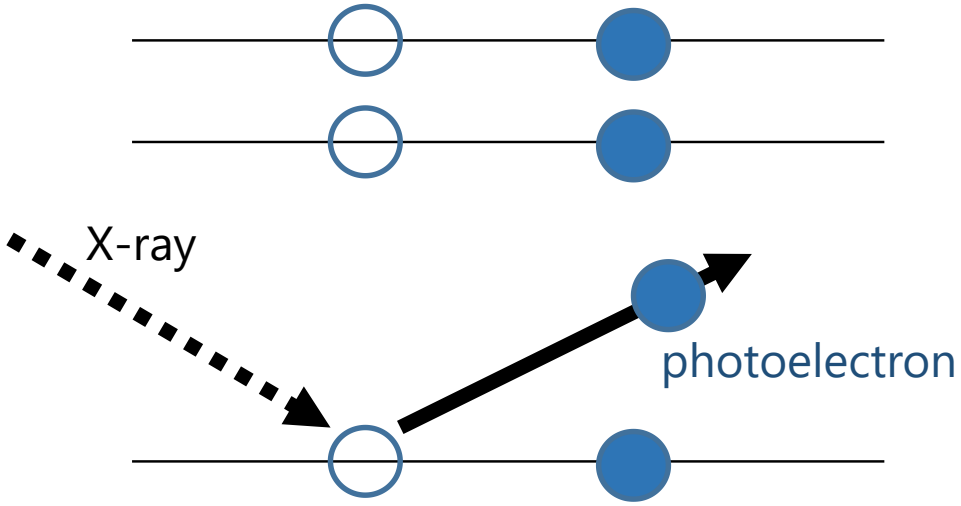


Figure 4.3 Schematic illustration of XPS [4.2].

XPS was performed at a wavelength of 532 nm using an Al K_α X-ray source. The Voigt function (x) was used to fit the X-ray photoelectron spectra of the MoS_2 films. A composition ratio of the MoS_2 film was expressed as shown in the following equation,

$$C_i = \frac{A_i / RSF_i}{\sum_j A_j / RSF_j} \times 100 \qquad (4.5),$$

where C_i is the composition ratio, A_i is the peak area, and RSF_i is the relative sensitivity factor of the atom *i*.

4.2.3 Raman spectroscopy

When an electromagnetic wave is radiated to some matters, scatter happens in addition to some phenomena such as reflection, bending, and absorption because of the interaction between light and matter. Two types of light are classified as Raman and Rayleigh ones as shown in Figure 4.4. First, Raman-scattered light has a different light length from incident light because of molecular motion. On the other hand, Rayleigh scattered light has the same wavelength with incident light. The strength of Raman scattered light is one-millionth times weaker than that of Rayleigh scattered light. However, in the measurement of Raman spectroscopy, the Raman

scattered light is separated and the Raman spectral is obtained. And then, the structure of the molecule level is investigated by the acquired spectra.

Through Raman spectroscopy, the composition ratio or the crystalline structure is proved. In this study, Nd YAG laser (neodymium-doped yttrium aluminum garnet; Nd: $Y_3Al_5O_{12}$) is used for measurement (λ = 1064 nm) [4.3]. The incident light of green laser (532 nm) and ultraviolet laser are second and third harmonic waves of YAG laser. The grating-spaces are 1800, 2400, and 3600 mm^{-1}.

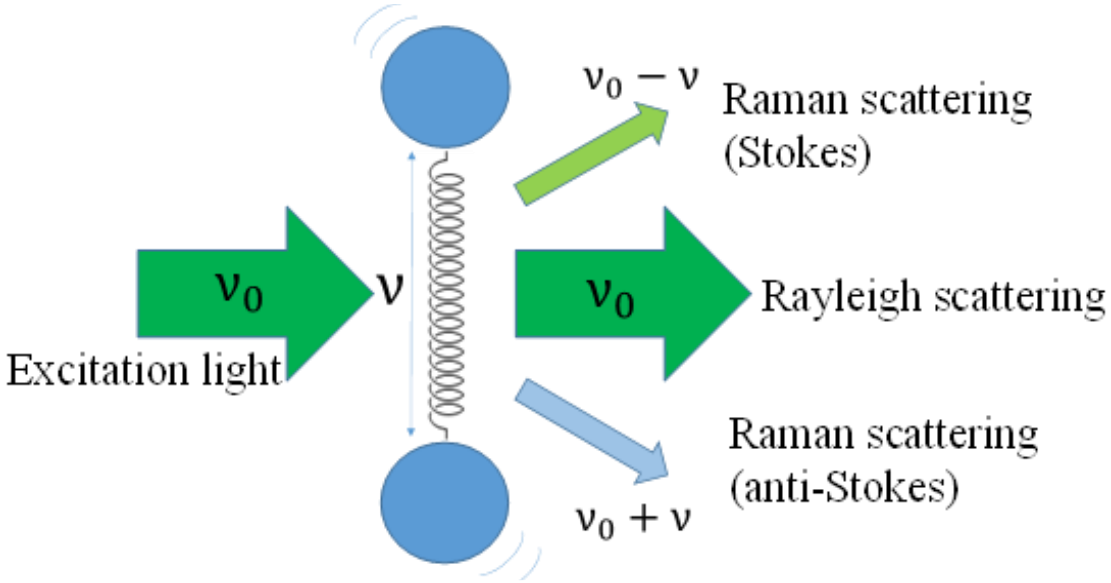


Figure 4.4 Rayleigh and Raman scattering [4.4].

4.3 Device fabrication process

The following procedures are adopted to fabricate the devices for measurement. The outlines of experimental procedures are shown in Figure 4.5. We introduced sputtered MoS_2 film to the sulfurization process. After cleaning by SPM, we deposited MoS_2 film (~4 nm) by 300°C sputtering. The device structures are shown in Figure 4.6 (a) and (b). After that, we introduced the sulfurization process under various temperatures and pressure as showing in Figures 4.1 and 4.2. The motivation in which we examined the pressure property is that the amount of sulfur sublimation is expected to be increased. In the case of our sulfurization process, the sulfur powder is used as the sulfur source and we need to evaporate sulfur powder. Therefore, although in the CVD process, the pressure is usually air ambient, it is possible to enrich sulfur gas and hasten the sulfurization by decreasing pressure even when the temperature doesn't change in terms of the vapor pressure of sulfur as shown in Figure 4.7 [4.5-4.8]. As a physical evaluation, the Raman spectroscopy and XPS were conducted. As an electrical evaluation, the Hall-effect measurement was conducted and then Ag paste was used as metal contact.

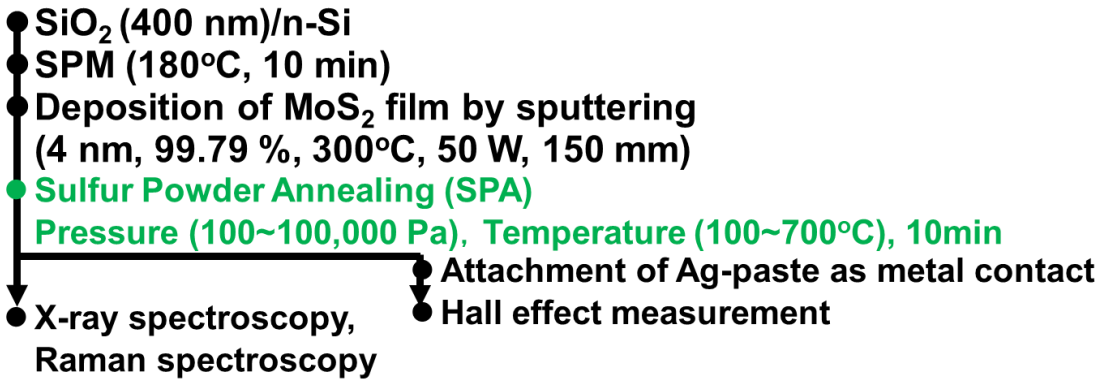
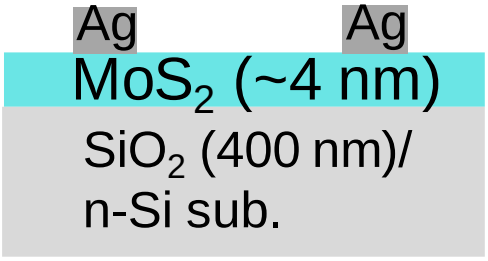
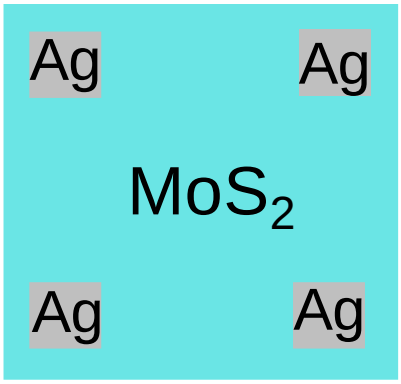


Figure 4.5 Fabrication procedure.



(a)



(b)

Figure 4.6 Schematic Diagram of MoS_2 sample structure with (a) cross sectional and (b) plan views.

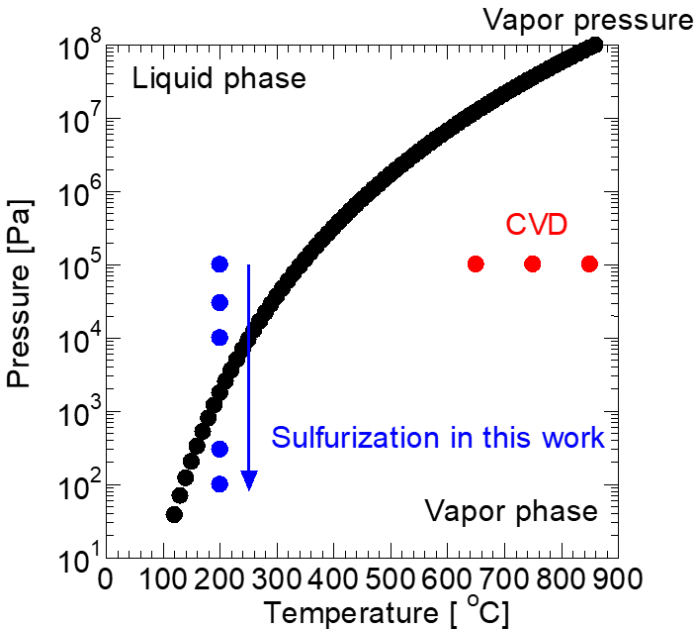


Figure 4.7 Vapor pressure of sulfur and CVD condition of the previous report for fabricating MoS_2 [4.5-4.8].

4.4 Raman spectroscopy results

We evaluated the pressure property toward sputtered MoS_2 film. Figures 4.8 and 4.9 show Raman intensities and Full-Wide-Half-Maximum (FWHM) value from Raman spectra when the pressure is decreased in this sulfurization process at 600^{o}C, respectively. As you can see in Figure 4.8, it is confirmed that Raman peak intensities successfully enhanced when the pressure becomes less than 300 Pa. There are two reasons. First, the amount of sulfur evaporation became bigger even when the temperature is not changed by decreasing temperature in terms of sulfur vapor pressure. Second, the low pressure helps Mo and S atoms move smoothly and the reaction between sulfur and sputtered MoS_2 film was promoted. However, we can see in Figure 4.9 (a) and (b) that the crystallinity wasn't improved by decreasing pressure which indicates that we need to evaluate of temperature property of SPA.

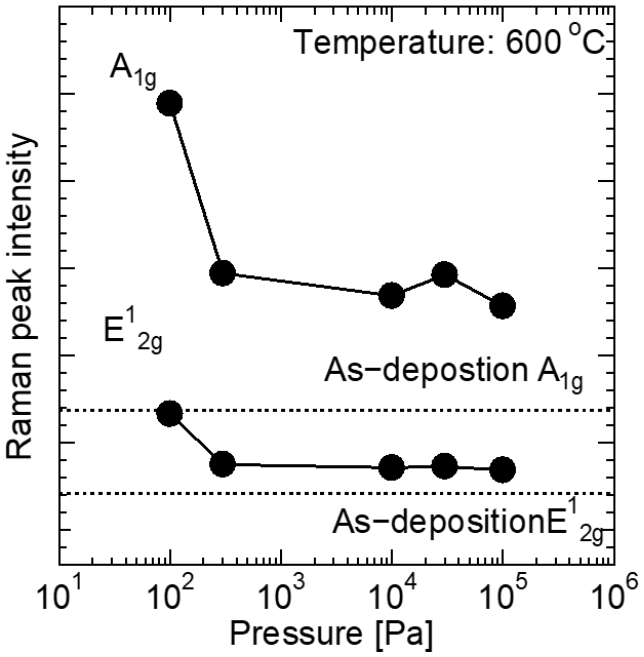
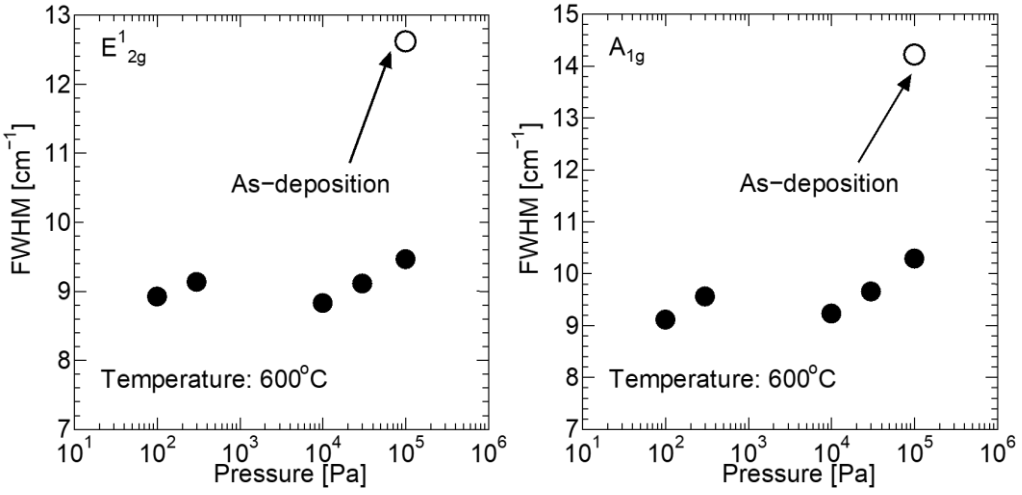


Figure 4.8 Raman peak intensities of MoS_2 film sulfurized at various pressure.



(a) (b)

Figure 4.9 Full width at half maximum (FWHM) value of (a) E^1_{2g} and (b) A_{1g}.

Figure 4.10 is the Raman spectra when the temperature is increased to 700^{o}C respectively. As shown in this Figure, as the temperature becomes high, the Raman peak intensities also increased. Figure 4.11 are FWHM value of (a) both E^{1}_{2g} (out-of-plane mode vibration of sulfur) and (b) A_{1g} (in-plane vibration mode of sulfur and molybdenum) from Figure 4.10. As these figures shows, FWHM decreased as the temperature becomes high. These results mean the sulfurization in sulfur vapor ambient enhances at higher temperature and sulfur annealing acts as not only compensation of sulfur but also improvement of the crystallinity of sputtered-MoS_2 film. Finally, the FWHM gets down to around 7 ~ 8 cm^{-1}. This FWHM gets close to one of MoS_2 film on SiO_2 made by CVD [4.9]. This indicates that the crystallinity of sputtered MoS_2 film could be comparable with CVD MoS_2 film.

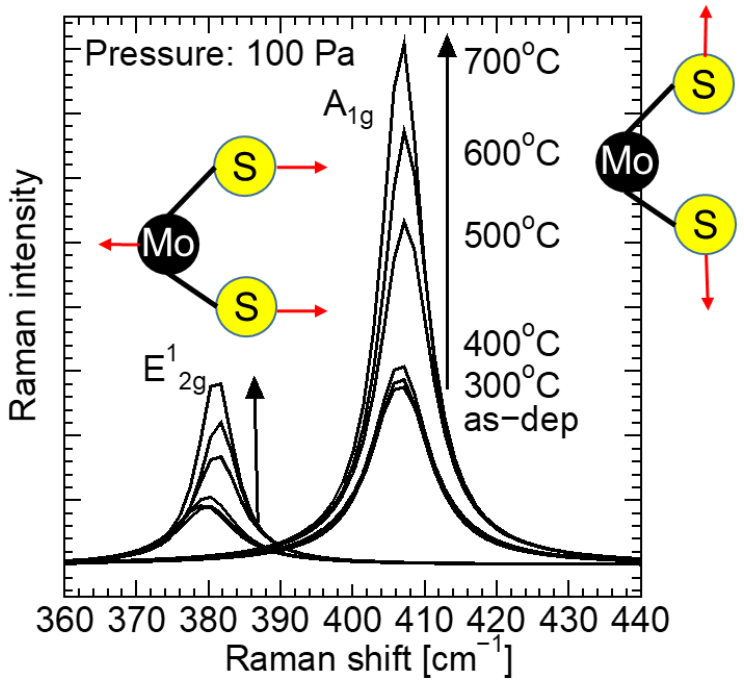
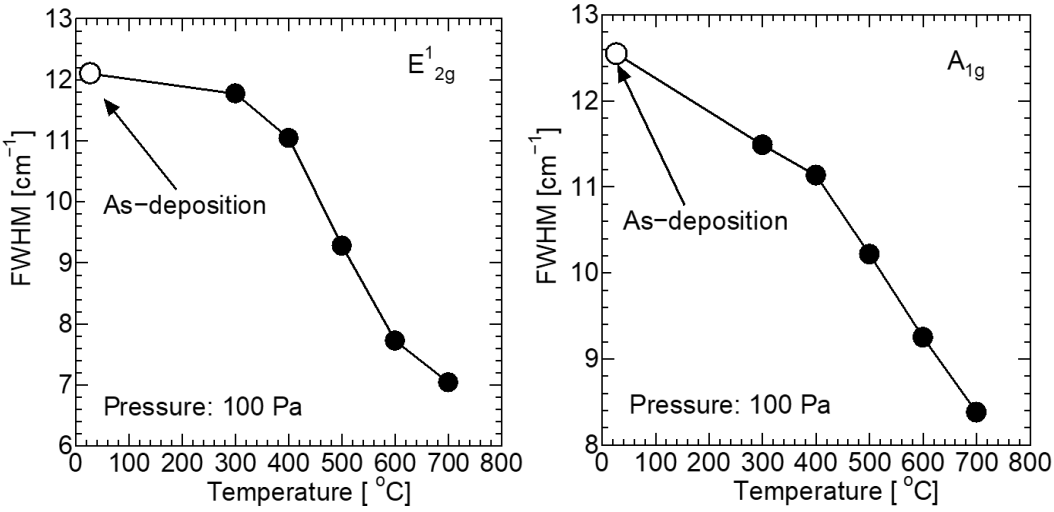


Figure 4.10 Raman spectra of MoS_2 film sulfurized at various temperatures.



(a) (b)

Figure 4.11 Full width at half maximum (FWHM) value of (a) E^1_{2g} and (b) A_{1g}.

4.5 XPS results

Figure. 4.12 is XPS results of 4 nm sputtered MoS_2 film when the temperature is increased. Figure 4.12 (a) and (b) are XPS spectra of non-annealed MoS_2 film. As shown in Figure 4.12 (a), Mo-S and Mo-O chemical bonding spectra were observed in as-sputtered MoS_2 film, which was originated in MoS_2 and MoO_3, respectively. This indicates that as-sputtered MoS_2 film is oxidized after sputtering process as well as previous reports [4.10,4.11]. In addition, Mo-Mo chemical bonding spectrum from Figure 4.12 (a) and S-S peak from Figure 4.12 (b) were also confirmed. This means that there are still non-bonding Mo, namely sulfur vacancy, and S in as-sputtered MoS_2 film. On the other hand, Figure 4.12 (c) and (d) are XPS spectra of the MoS_2 film sulfurized at 700^{o}C. In these figures, we can see that Mo-O, Mo-Mo and S-S spectra decreased and S-Mo spectrum increased comparing with Figure 4.12 (a) and (b). This means that the reduction of MoO_3 and the reaction between Mo and S was confirmed. As a result, we evaluated the contents of MoO_3 in sputtered MoS_2 film calculated from the spectra area. As shown in Figure 4.13 (a), the contents of MoO_3 have been decreasing as an increase in a temperature indeed, which means the reduction of MoO_3. Figure 4.13 (b) is the S/Mo composition ratios of sputtered MoS_2 film. We can see that the composition ratios have been enlarged and got closed to 2.0. This indicates that the reaction between Mo and non-bonding S, reduction of MoO_3 and sulfurization of Mo in sulfur vapor were promoted by increasing temperature and the number of sulfur vacancies became low. As a result, the sulfurization process results in not only the reduction of MoO_3 but also the sulfurization of the Mo atoms to form MoS_2.

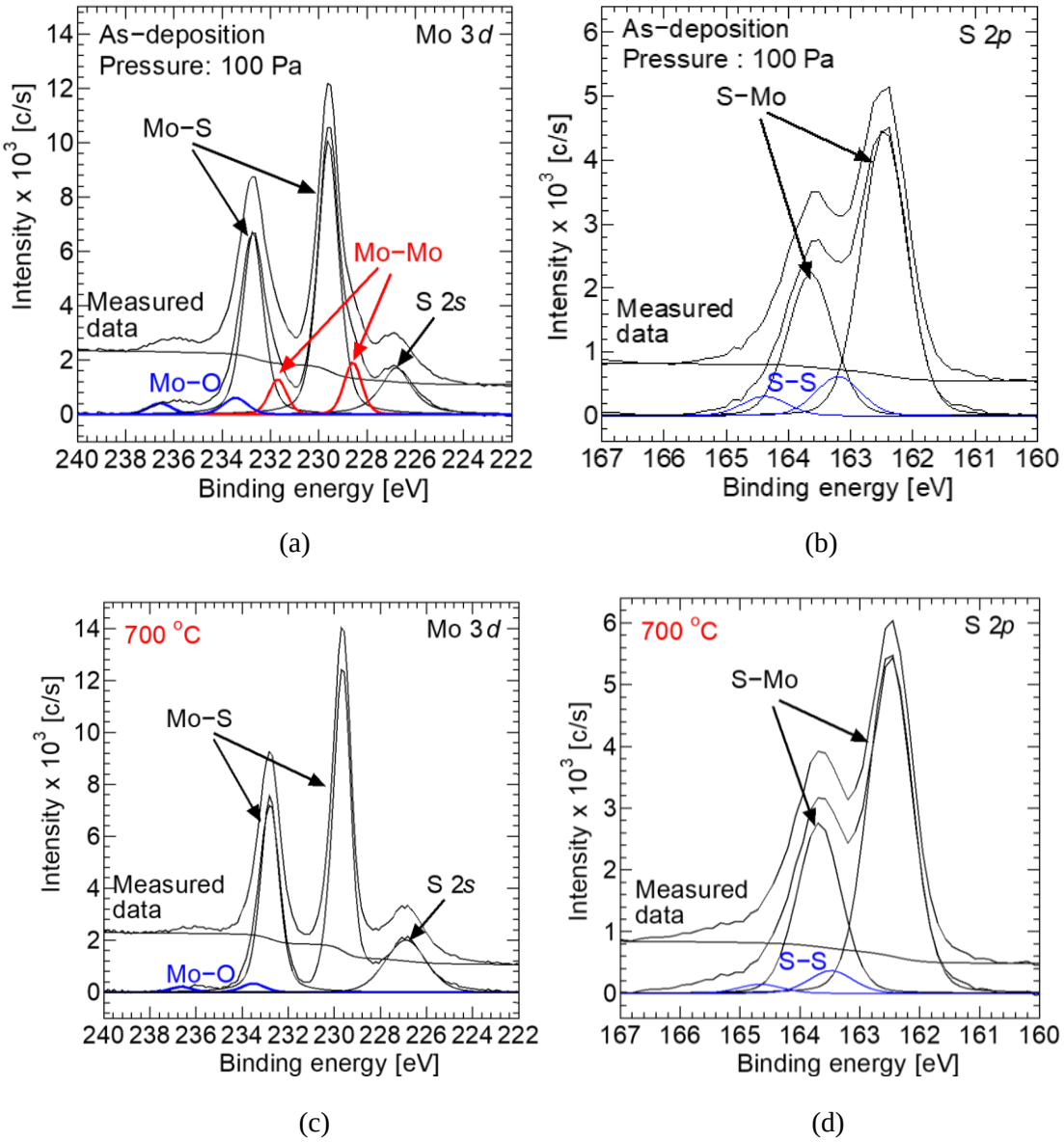
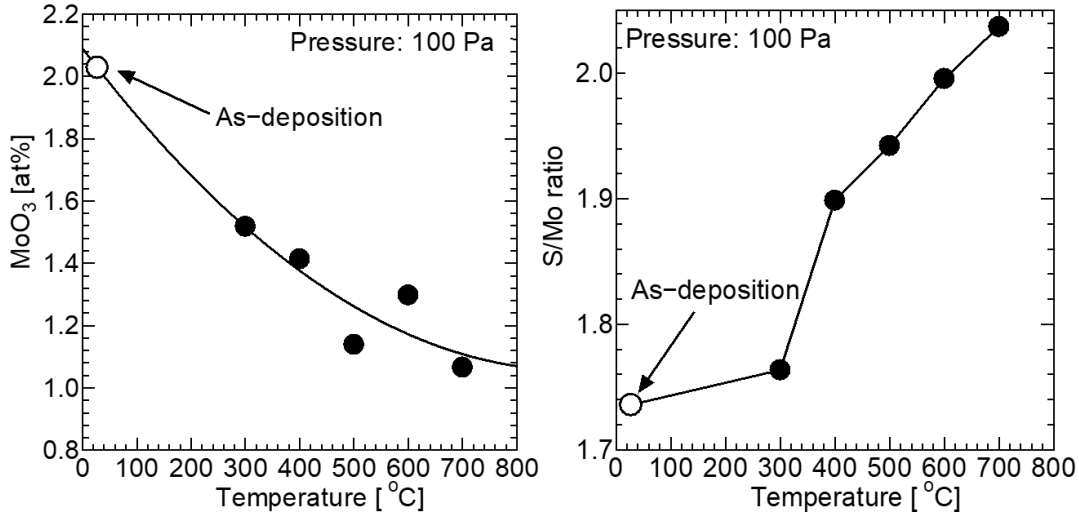


Figure 4.12 XPS results of MoS_2 film when the temperature changes. (a) Molybdenum 3*d*, sulfur 2*s* and (b) sulfur 2*p* of as-sputtered MoS_2 film from XPS spectra are shown. (c) Molybdenum 3*d*, sulfur 2*s* and (d) sulfur 2*p* of sputtered MoS_2 film sulfurized at 700°C from XPS spectra are shown.



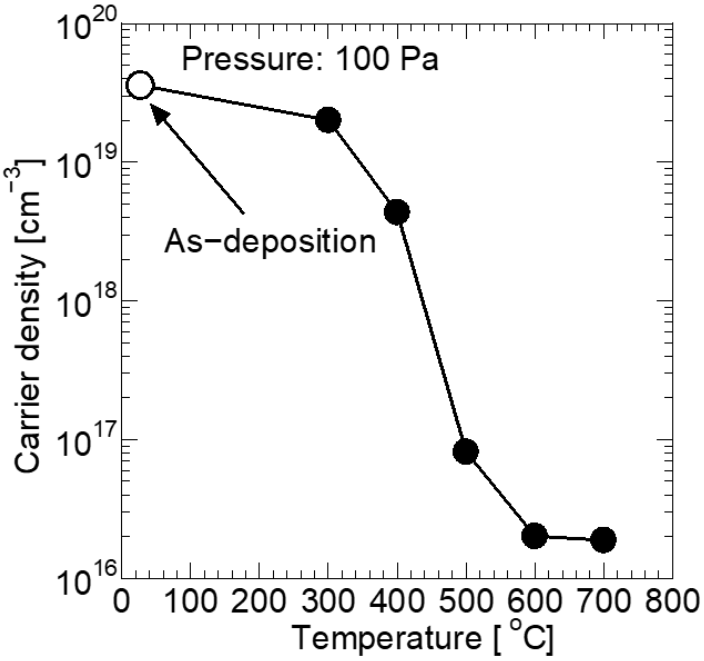
(a) (b)

Figure 4.13 (a) Contents of MoO_3 and (b) S/Mo ratio in sputtered MoS_2 film calculated by XPS spectrum areas.

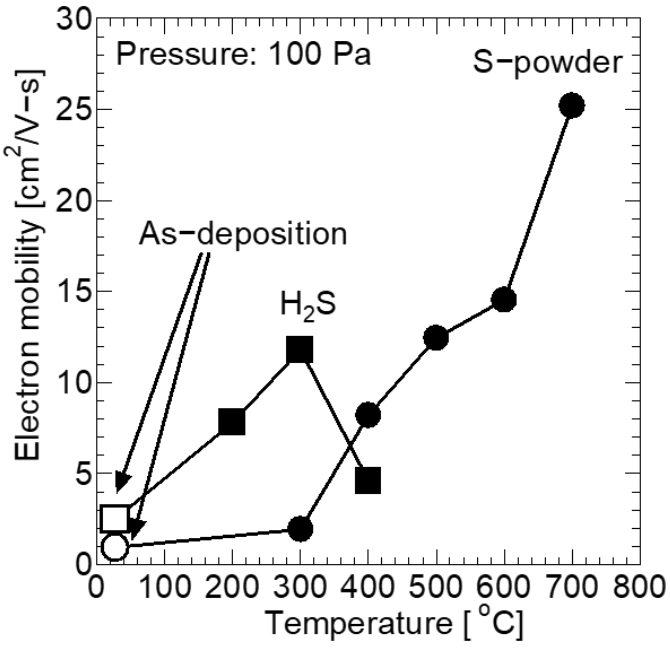
4.6 Electrical property of sulfurized MoS_2 film by Hall-effect measurement

To investigate the electrical property of MoS_2 film fabricated by sputtering method, Hall-effect measurement is applied. Especially, the Ag paste is used as the contact metal for Hall-effect measurement. Like Figure 4.6 (b), the Ag paste is attached in the four corners of the substrate. Moreover, the prove needle is touched on these Ag pastes and the measurement current stream in MoS_2 film. In this measurement, we examine the electric resistivity and check whether ohmic-contact between Ag and MoS_2 is or not first. If we can confirm ohmic contact, we proceed to the Hall-effect measurement.

Figure 4.14 is the results of the Hall-effect measurement, (a) is the carrier density and (b) is the electron mobility with SPA and H_2S annealing, respectively. In the case of SPA sample, when the temperature increases, the carrier density decreases down to 1.8×10^{16} cm^{-3}. This indicates that the number of sulfur vacancy which acts as a donor gets fewer by sulfurization at higher temperature. Furthermore, the electron mobility increased from 1.7 up to 25.2 $cm^2/V\text{-}s$. This improvement of electron mobility would be caused by the decrease of carrier density and improvement of crystallinity by this sulfurization process. On the other hand, H_2S annealing increased the mobility from 200^oC and decreased at 400^oC because H_2S gas can react with MoS_2 film relative low temperature and it starts to be decomposed at more than 400^oC [4.12]. As a result, it was confirmed that sputtered MoS_2 film was sulfurized and the electrical property was improved by SPA. In addition, SPA and H_2S annealing give us the two options. When the low temperature is important, H_2S annealing should be used. On the other hand, when high temperature is admitted, SPA realizes the high quality MoS_2 film at 700^oC.



(a)



(b)

Figure 4.14 (a) Carrier density and (b) electron mobility with SPA and H_2S annealing at various temperatures by Hall-effect measurement.

4.7 Summary

In this chapter, the evaluation for sputtered MoS_2 film which is sulfurized by SPA was conducted in order to compensate for sulfur vacancy and realize MoS_2 normally-off FETs can be operated in the accumulation mode. To promote sulfurization, the pressure property and temperature property was discussed by using Raman spectroscopy and X-ray photoelectron spectroscopy as physical evaluation. Finally, the electrical property was examined by the Hall-effect measurement.

It was unveiled that sulfurization was successfully enhanced when the pressure becomes 100 Pa from Raman peak intensity because the sulfur evaporation and migration were promoted by decreasing pressure. Therefore, we fixed the pressure to 100 Pa in this study.

The temperature property of sulfurization for sputtered MoS_2 film was evaluated by Raman spectroscopy and XPS. As we increase sulfurization temperature from 300^{o}C to 700^{o}C at 100 Pa, we found that sulfurization was promoted and crystallinity was improved from the results of Raman spectroscopy. This means this sulfurization acts as both compensations of sulfur and improvement of the crystallinity of sputtered-MoS_2 film. Moreover, it was found that MoO_3 reduction and sulfurization was promoted by increasing temperature from XPS spectra. Finally, we confirmed that the S/Mo compensation ratio of sputtered MoS_2 calculated the area of XPS spectra got close to 2.0 which is ideal compensation ratio. This matches with results of Raman spectroscopy and XPS.

The electrical property of sulfurization for sputtered MoS_2 film by the Hall-effect measurement was discussed when increasing in temperature. First, we measured the carrier density of sputtered MoS_2 film. And it was founded that carrier density decrease from 3.5×10^{20} down to 1.8×10^{16} cm^{-3}. This result indicates that the increase of carrier density owing to sulfur vacancy was prevented by this sulfurization process. Furthermore, the increase in MoS_2's electron

mobility from 1.7 to 25.2 cm^2/V-s was confirmed and electrical properties became better than H_2S annealed one. This improvement of electron mobility would be caused by the decrease in carrier density and the improvement of crystallinity further. This mobility can be able to drive 8k liquid crystal display in 120 frames per second [4.13].

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Chapter 5 $MoSi_2$ contact for reducing contact resistance of MoS_2-FET

5.1 Background

The output characteristics of the FETs in chapter 3 showed a significant large contact resistance. To decrease this resistance, it is necessary to choose a material whose Schottky barrier height can be minimized. The previous report shows Schottky barrier heights with MoS_2 and various metals and the promising material is Molybdenum (Mo) or Titanium (Ti) [5.1]. Scandium shows the lowest Schottky barrier height and low contact resistance is reported [5.2]. However, Scandium is rear metal and expensive, it is not appropriate in terms of mass-production. The lowest contact resistance is achieved by Mo contact because the covalent bond between Mo and MoS_2 can be formed easily [5.3]. The usage of the same metal material with TMDC as the contact is a promising approach to reduce the contact resistance [5.4]. Therefore, Mo is the most promising contact material.

In addition, we have to consider what is most appropriate contact structure for sputtered MoS_2 film. There are two main contact structures, edge contact and surface contact. In the case of edge contact, the side face of MoS_2 contacts with metal as shown in Figure 5.1 (a). It is known that edge contact has a low contact resistance per area. However, the total amount of current tends to be small because the contact area is limited by a thin thickness of MoS_2 film. Hence, surface contact that MoS_2 film touches with contact metal longitudinally is said to be better than edge contact. Surface contact is divided into two types. The first type is top contact that contact metal is deposited on MoS_2 film as shown in Figure 5.1 (b). In this structure, the process to make the contact pattern on MoS_2 film such as etching, photolithography is necessary and the damage to MoS_2 film by such process is unavoidable. The second type is the bottom contact that MoS_2 film

is deposited on contact metal as shown in Figure 5.1 (c). In this structure, it is important to introduce an acid cleaning before depositing MoS_2 film not to remain an impurity at the surface of contact metal as discussed in chapter 3. However, if the bottom S/D metal is used, this process easily removes the metal. Therefore, we selected $MoSi_2$ film synthesized on an n-doped poly-Si film, because Mo is reported to obtain the lowest contact resistance.

In this chapter, $MoSi_2$ contact characteristics are evaluated by using Transmission Line measurement (TLM) device comparing with n-doped poly-Si contact.

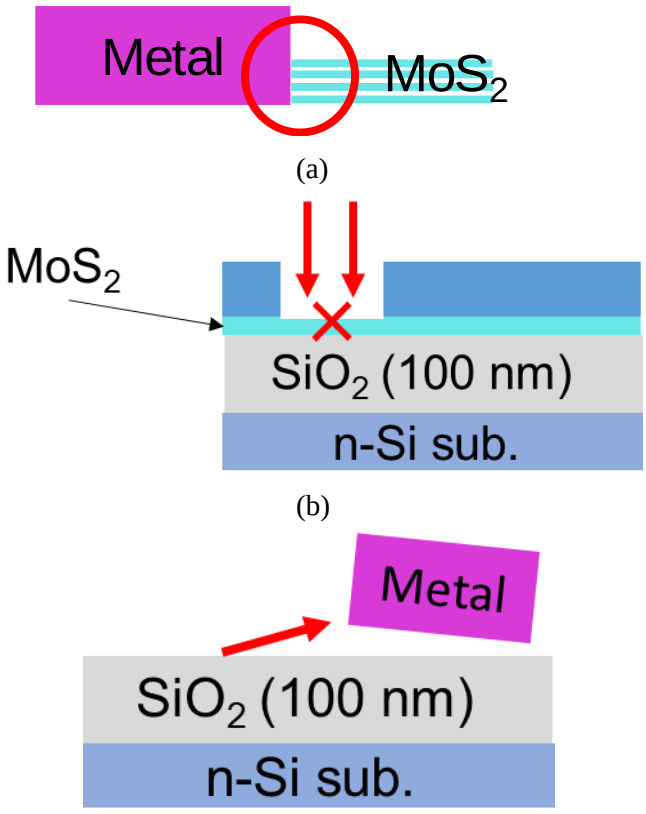

Figure 5.1 Schematic illustrations of (a) edge, (b) top and (c) bottom contact structures with MoS_2 and contact metal.

5.2 Experimental procedure

5.2.1 Chemical dry etching (CDE)

CDE is also a plasma etching technology. The difference with RIE is that the plasma is generated in the separated space with the substrate and conveyed. Accordingly, the chemical reaction is more dominant comparing with RIE and CDE can etch the substrate with less damage [5.5]. CDE is selected for patterning the bottom contacts region in this study. This is because the channel region where MoS_2 film is going to be deposited by sputtering is also fabricated when the bottom contacts are patterned by CDE. Sputtered MoS_2 film was found that the mobility is decreased when the damage of the substrate is large and it is necessary to reduce it by using CDE [5.6].

5.2.2 Transmission length method (TLM)

TLM is widely used for extracting the contact resistance and sheet resistance. In this method, the total resistance (R_T) between the semiconductor and the contact with several distances (L). Then we can show the resistance dependence on the distance as shown in Figure 5.2 [5.7].

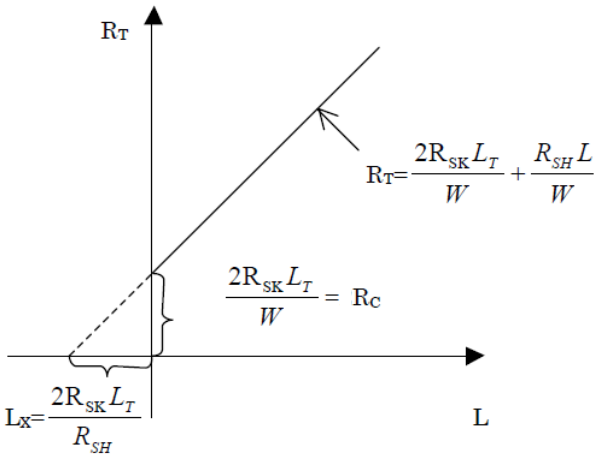

Figure 5.2 Relationship between total resistance and distance [5.6]. R_C is the contact resistance. W is the width of the electrode. L_T is the transfer length. R_{SK} is the sheet resistance under the electrode. R_{SH} is the sheet resistance for another area.

In this figure, the x-intercept and y-intercept mean L_X and R_C, respectively. we assume R_{SK} = R_{SH} in this study and this assumption means the resistances under the electrode are equal to the one of another area. Therefore, we can modify the formulas as follows,

$$L_x = 2L_T \quad (5.1),$$

$$R_C = \frac{2R_{SH}L_T}{W} \quad (5.2), \text{ and}$$

$$R_T = \frac{R_{SH}}{W}(2L_T + L) \quad (5.3).$$

Using these formulas, we can extract the contact resistance and sheet resistance. Moreover, the contact resistivity (ρ_C) is able to be calculated by the following formula,

$$\rho_C = R_C \times L_T \times W \quad (5.4).$$

5.3 Device fabrication process

Figure 5.3 is the process flow for the TLM device. As S/D regions for n-type FET operations, the n-doped poly-Si contact was patterned by chemical dry etching in CF_4 gas. After piranha (H_2O_2 : H_2SO_4 = 1 : 4) cleaning at 180°C for 10 min to remove photo-resist, $MoSi_2$ film was synthesized by sputtered Mo film at 700°C in Ar gas. After introducing piranha cleaning again to remove residual Mo film, MoS_2 film of 10 nm was deposited directly on the substrate by RF magnetron sputtering at 400°C [5.6,5.8,5.9], under the following condition, an RF power of 50 W, the distance between the target and substrate of 230 mm, argon (Ar) flow of 7.0 sccm, and partial pressure of 0.75 Pa. As a passivation layer, Al_2O_3 film with a thickness of 10 nm was deposited by atomic layer deposition (ALD) method. After an isolation patterning of Al_2O_3 film and MoS_2 channel by DHF and HNO_3, respectively. Then Ar gas and forming gas (F.G., H_2: 3%, N_2: 97%) annealings are introduced at various temperatures to improve the interface $MoSi_2$ and MoS_2 film. Figures 5.4 and 5.5 are cross sectional and plan views of TLM devices with Si and $MoSi_2$ contact, respectively.

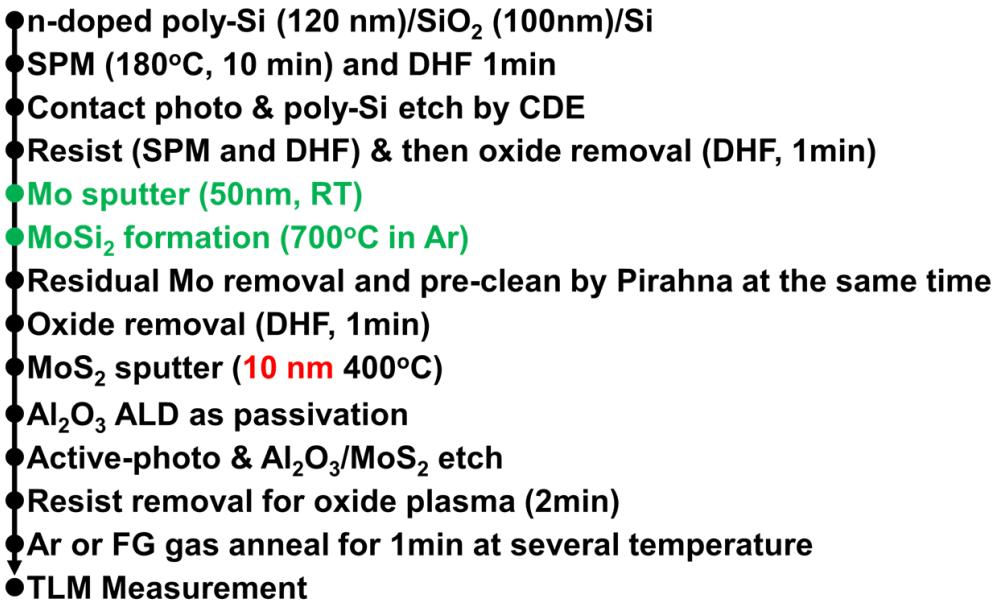

Figure 5.3 Process flow of TLM device.

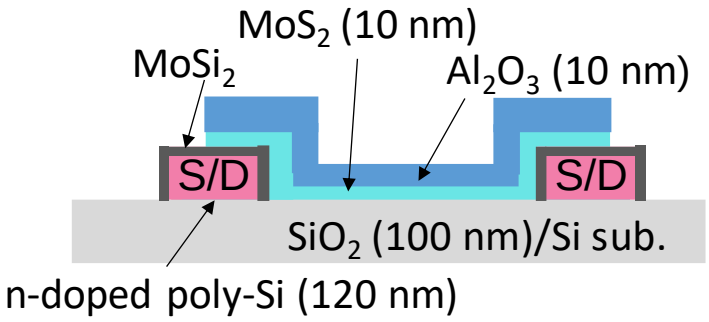

Figure 5.4 Cross sectional schematic image of TLM device.

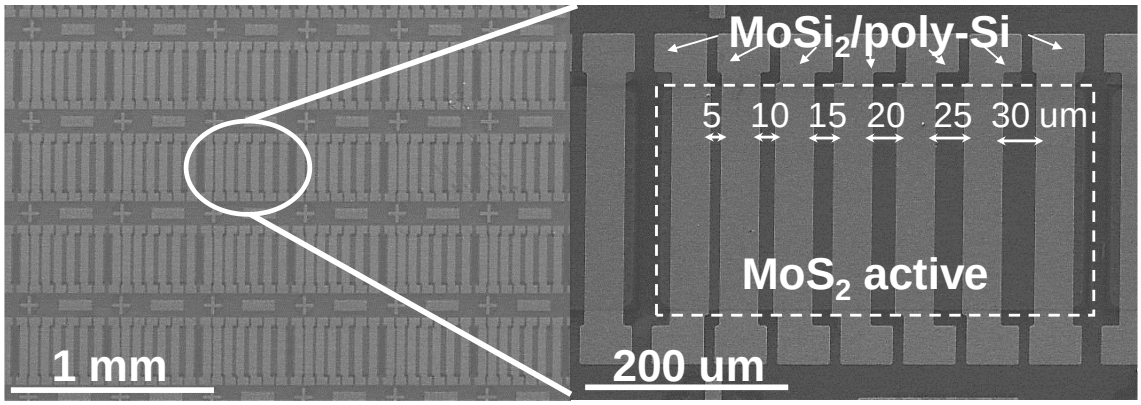

Figure 5.5 Plane views of chip-level-integrated *n*MISFETs with RIE-defined MoS_2 active (dashed line) and TiN/Ti contact metal.

5.4 I-V curve and contact resistance with various F.G. anneal temperature

Figure 5.6 shows the I-V curves of $MoSi_2/MoS_2$ interface annealed at various temperatures in F.G. anneal temperatures. The Ohmic contact is observed above 600°C because the $MoSi_2$ and MoS_2 films are alloyed to each other. However, currents at less than 500°C becomes lower than those even for the as-deposition, because the thermal energy is not sufficient to produce the alloy with still-remaining oxide layer at the interface [5.10,5.11]. Figure 5.7 exhibits a contact resistivity at $MoSi_2/MoS_2$ interface and sheet resistance in MoS_2 film at various F.G. anneal temperatures. The contact resistivity decreases down to 2.6×10^{-2} Ohm-cm^2 at 700°C, whereas the sheet resistance does not increase significantly. Therefore, these results indicate that F.G. gas annealing at high temperature forms an alloy at the interface between MoS_2 and $MoSi_2$ films.

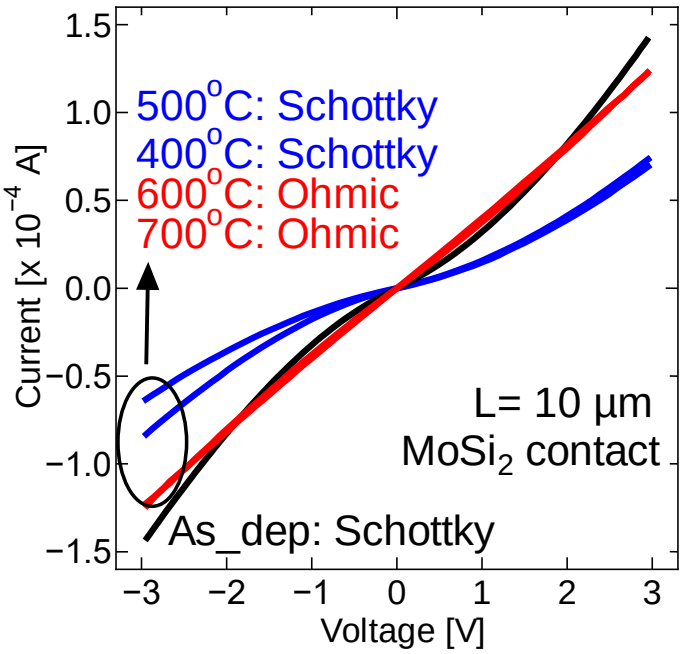

Figure 5.6 I-V curves of $MoSi_2/MoS_2$ contact for various F.G. anneal temperatures.

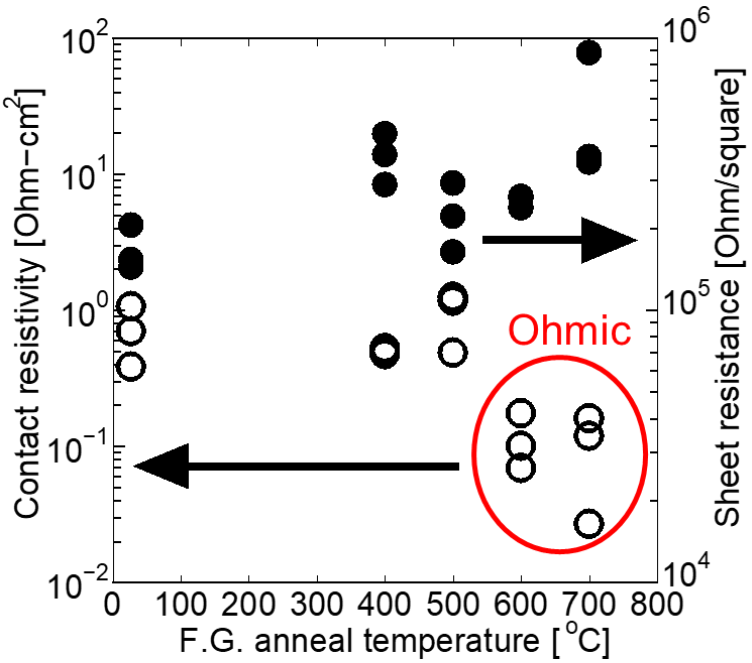

Figure 5.7 Contact resistivity at $MoSi_2/MoS_2$ interface and sheet resistance in MoS_2 film at various F.G. anneal temperatures.

5.5 Activation energy by measurement at low temperature

Figure 5.8 is contact current dependence on the absolute temperature between n-doped poly-Si or $MoSi_2$ and 10-nm MoS_2 film annealed in F.G. or Ar gas at 700°C. In this figure, the fitting results with the following equation are also shown, which is used to extract the activation energies (E_a),

$$Log(I) = Log(I_0) - \frac{E_a}{kT} \quad (5.5),$$

where *k* is the Boltzmann constant and T is a measurement temperature. It is found that $MoSi_2$ contact has a higher current than Si one. Its activation energy is extremely small and independent of the temperature. the activation energy of Si increases when the temperature increases. Furthermore, F.G. annealing enables a lower resistance than that of Ar gas annealing is because of the reduction from MoO_3 to MoS_2 by containing hydrogen resulting in a crystallinity improvement [5.10]. Figure 5.9 is the expected band structures of n-doped poly-Si and $MoSi_2$ contact with MoS_2 film. The bandgap of n-doped poly-Si and MoS_2 film are 1.1 and 1.2 eV, respectively. Electron affinity of n-doped poly-Si, MoS_2 and $MoSi_2$ are 4.2 eV, 4.0 eV and 4.7 eV, respectively. At the interface between $MoSi_2$ and MoS_2, the alloy formed and it becomes the main current path through this interface. Therefore, the current is high and its activation energy is extremely small and independent of the temperature. Regarding Si contact, the vdW gap at the interface between n-doped poly-Si and MoS_2 is expected to act as a tunnel barrier height. Therefore, a tunneling current is dominant at low temperatures. When the temperature increases, the electrons have sufficient energy to exceed the energy barrier. Accordingly, Ea becomes high. As a result, $MoSi_2$ is selected as the contact material for MoS_2 *n*MISFETs.

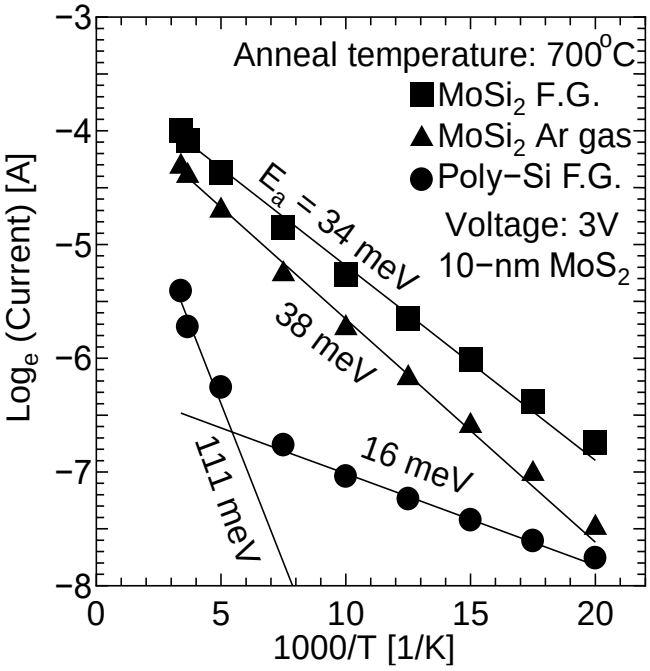

Figure 5.8 Contact current dependence on the absolute temperature between n-doped poly-Si or $MoSi_2$ and 10-nm MoS_2 film annealed in F.G. or Ar gas at 700°C.

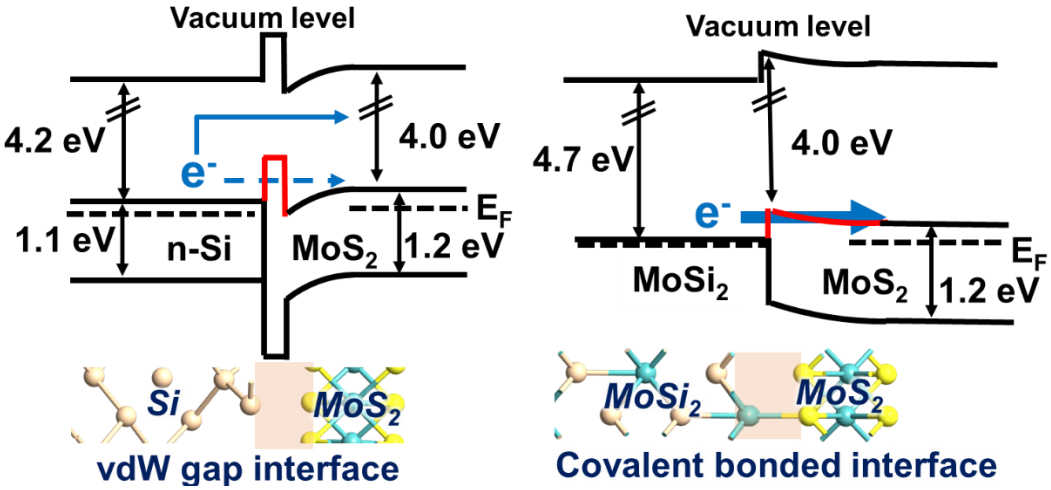

Figure 5.9 Expected band structures of n-doped poly-Si and $MoSi_2$ contact.

5.6 Summary

In this chapter, we demonstrate $MoSi_2$ bottom contact for MoS_2 film. Acid cleaning before depositing the MoS_2 film can be performed and reduce a contact resistance. As a result, $MoSi_2$ contact is successfully formed with acid cleaning and it has the lower activation energy and contact resistance of 2.6×10^{-2} Ohm-cm^2 than that of n-doped poly-Si. This process is expected to reduce contact resistance and carbon contamination when it is introduced to MoS_2-FET. To increase the amount of current further, optimizing the shape of the contact region and increase the contact area are necessary.

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Chapter 6 Normally-off top-gate sputtered MoS_2-*n*MISFET with SPA, F.G. annealing, $MoSi_2$ contact

6.1 Background

In previous chapters, the challenge of sputtered MoS_2-*n*MISFETs is confirmed to be normally-on operation, high contact resistance and small grain size. As a solution for normally-on operation, SPA successfully promotes the sulfurization and decrease the carrier density. Besides, owing to decrease contact resistance, $MoSi_2$ contact is introduced and makes contact resistance decrease down to 2.6×10^{-2} Ohm-cm^2. On the other hand, carbon contamination derived from residual photoresist and high Q_f and Q_{it} cause normally-on operation. Therefore, they are still necessary to be resolved.

In this chapter, SPA and $MoSi_2$ are introduced to the fabrication process for sputtered MoS_2-*n*MISFETs in order to reduce carrier density, carbon contamination and contact resistance. In addition, monolayer Al_2O_3 film, SiN sidewall passivation and F.G. annealing are introduced after the device fabrication process to decrease Q_f and Q_{it}. The discussion about the effect of these improvements on MISFET performance follows.

6.2 Device fabrication process

Figure 6.1 is process flow of chip level integrated *n*MISFETs, and Figure 6.2 is the cross sectional view of MoS_2-*n*MISFET. As S/D regions for n-type operation, the n-doped poly-Si contact was patterned by chemical dry etching in CF_4 gas. After piranha (H_2O_2 : H_2SO_4 = 1:4) cleaning at 120^{o}C for 10 min to remove photo-resist, $MoSi_2$ film was synthesized by sputtered Mo film at 700^{o}C in Ar gas. After introducing piranha cleaning again to remove residual Mo film, MoS_2 film of 2.7 nm was deposited directly on the substrate by the RF magnetron sputtering at 400^{o}C [6.1-6.3]. The conditions were an RF power of 50 W, the distance between the target and substrate of 230 mm, argon (Ar) flow of 7.0 sccm, and partial pressure of 0.75 Pa. MoS_2 film was annealed by SPA at 700^{o}C in 100 Pa for one hour to compensate the sulfur vacancies and improve the crystallinity, simultaneously [6.4]. As a dielectric layer, Al_2O_3 film was deposited by Atomic Layer Deposition (ALD) method. After an isolation patterning of MoS_2 channel by the Reactive Ion Etching (RIE) with Cl_2 gas, SiN film of 50 nm is deposited by sputtering for the passivating sidewall of MoS_2 channel. TiN top-gate of 150 nm was deposited by sputtering and etched by RIE with Cl_2 gas. S/D contacts through Al_2O_3 film were patterned by DHF and lift-off process followed by titanium (Ti) of 20 nm and titanium nitride (TiN) of 30 nm. A plane view of the *n*MISFETs is Figure 6.3. After device fabrication processes, F.G. annealing is introduced at 300^{o}C for 30 min in order to decrease in interface trap density between MoS_2 and Al_2O_3 films [6.5-6.6].

- n-doped poly-Si(120 nm)/SiO_2(100 nm)/Si
- SPM (180°C, 10 min) and DHF (1 min)
- Contact photo & poly-Si etch by CDE
- Resist **(SPM and DHF)** & then oxide removal (DHF, 40 sec)
- **Mo sputter (50 nm, RT)**
- **$MoSi_2$ formation (700°C in Ar)**
- Residual Mo removal and pre-clean by SPM at the same time
- MoS_2 sputter (2.7 nm, 99.9 %, 400°C, 50 W, 230 mm, 0,75 Pa)
- **Sulfur powder anneal (700°C, 100 Pa, 1 h)**
- Al_2O_3 ALD as **single** dielectric layer
- Active photo & Al_2O_3/MoS_2 etch
- SiN sputter (50 nm) and lift off
- Gate TiN sputter (150 nm, RT)
- Gate photo
- Gate TiN RIE and resist removal
- Contact photo and etch (DHF, 1min)
- TiN (30 nm)/Ti (20 nm) sputter & lift off
- **F.G. anneal (300°C, 30 min)**

Figure 6.1 Process flow of chip-level integration for *n*MISFETs with $MoSi_2$ contact, TiN top gate and sputtered MoS_2 channel of 2.7-nm thick, which is patterned by RIE.

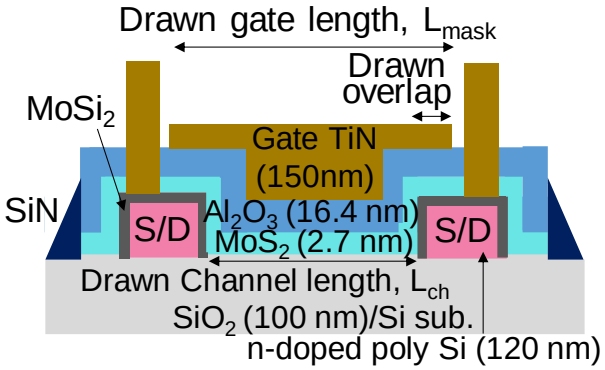


Figure 6.2 Cross-sectional schematic image of *n*MISFET with RIE-defined TiN top gate and sputtered MoS_2 channel of 2.7-nm thick.

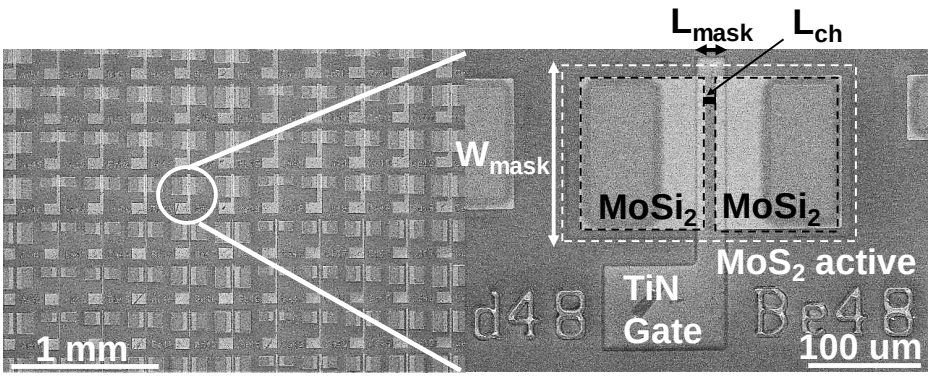


Figure 6.3 Plane views of chip-level-integrated *n*MISFETs with RIE-defined MoS_2 active (dashed line) and TiN/Ti contact metal.

6.3 TEM observations

A cross-sectional TEM image in Figure 6.4 shows overall features of the sulfurized MoS_2 film, ALD-Al_2O_3 passivation film and gate TiN metal of this *n*MISFET. It is confirmed that MoS_2 film with uniform thickness ranging 200 nm wide at least is preserved even after device fabrication processes thanks to SiN passivation film. The thickness of Al_2O_3 film is approximately estimated as 16.4 nm. We extracted the relative dielectric constant of Al_2O_3 film on MoS_2 channel was estimated as 5.8 [6.7] and the equivalent SiO_2 thickness of Al_2O_3 film is calculated as 10 nm. Figure 6.5 is the magnified picture of Figure 6.4. The four-layer MoS_2 film of around 2.7 nm is successfully observed. Hence, the thickness per layer is 0.7 nm approximately and this value matches with theoretical thickness [6.8]. This result means that SPA compensates sulfur vacancies resulting in a crystallinity improvement of MoS_2 film. However, the average grain size of sputtered MoS_2 film is approximately 50 nm, defined by grain boundaries as shown in Figure 6.5 and this value is smaller than CVD's one [6.9-6.11]. Hence, to control the number of nucleation sites and promote the migration on the substrate are promising approaches in order to enlarge the grain size [6.12].

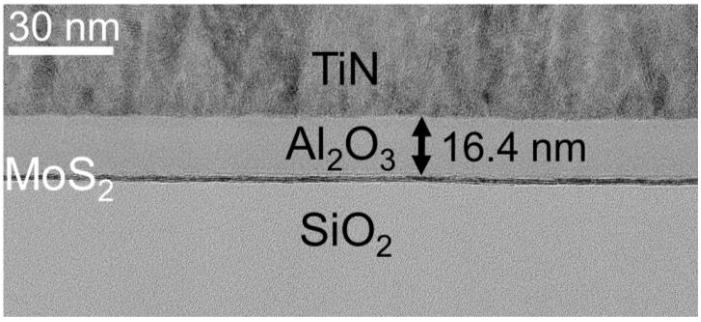


Figure 6.4 Cross-sectional TEM image of MoS_2 channel of MISFET with ALD-Al_2O_3 dielectric film. The MoS_2 film is uniform with almost the same thickness through 200-nm wide at least.

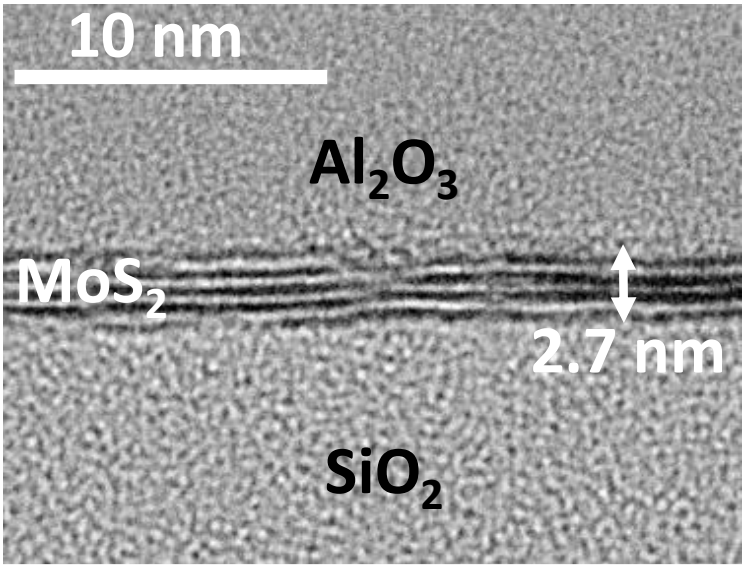


Figure 6.5 High-magnification image of cross-sectional TEM, as shown in Fig. 6.4. A four-layered MoS_2 film is successfully observed and the thickness of MoS_2 film is approximately 2.7 nm.

6.4 I_d-V_{gs} characteristics with SPA and/or F.G. annealing

Figure 6.6 shows log(I_d)-V_{gs} characteristics of MoS_2-*n*MISFET with only-SPA and only-F.G. having L_{ch}, overlap and W_{mask} of 10, 10 and 160 μm, respectively, at V_{ds} of 5 V. Solid line means only F.G. annealing is introduced after the whole device fabrication process is completed to decrease Q_{it} and Q_f. The dotted line means only SPA is introduced after MoS_2 film is deposited by sputtering to compensate for the sulfur vacancies. When only F.G. annealing is introduced, sputtered MoS_2 film has many sulfur defects and it tends to become metallic. Therefore, field effect isn't observed. When only SPA is introduced, the n-type operation in accumulation mode is confirmed because MoS_2 film can act as a channel by sulfur compensation. However, V_{off} has the negative value due to high Q_f and Q_{it} [6.13]. the main cause of 0.18 times of I_d is expected to be the increase in L_{eff} and W_{eff}.

Figure 6.7 shows log(I_d, I_g, I_s)-V_{gs} characteristics of MoS_2-*n*MISFET with both SPA and F.G. annealing (SPA&F.G.) having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{ds} of 1~5 V. Finally, V_{off} has the positive value thanks to SPA&F.G.. Moreover, I_{off} of 10^{-6}~10^{-7} μA/μm is very low, which means that device isolation is conducted well. This result leads to low standby power. However, the on/off ratio is ~10^2 at the most due to the small on current. One of the causes for the small on current is low carrier density of MoS_2 film by SPA. For further improvement, a doping technology to control the carrier density of MoS_2 film at S/D region is required [6.14]. The decrease in I_d is observed in SPA&F.G. compared to only-SPA and the causes are discussed in section 6.8.

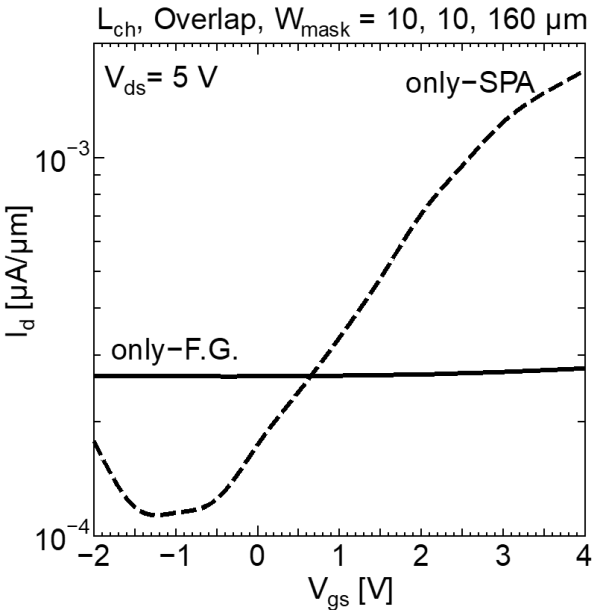


Figure 6.6 Logarithm I_d-V_{gs} characteristics at V_{ds} = 5 V for MoS_2 *n*MISFET with only-SPA and only-F.G. having L_{ch}, overlap and W_{mask} of 10, 10 and 160 μm, respectively.

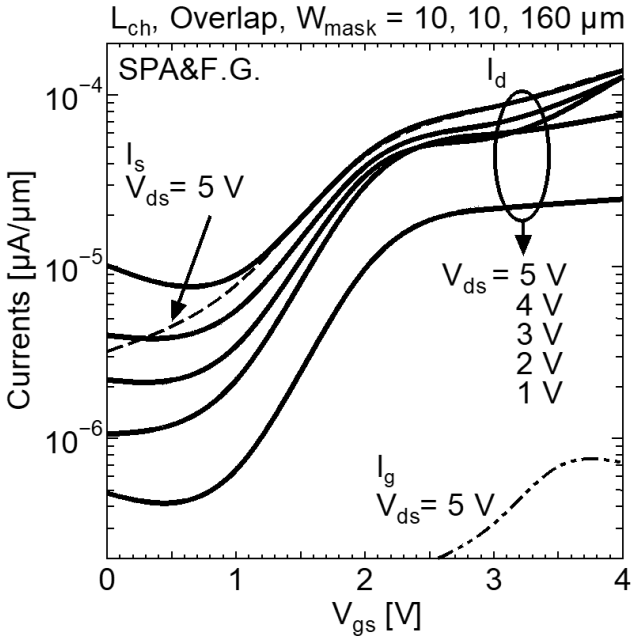


Figure 6.7 Logarithm I_d, I_s and I_g-V_{gs} characteristics at V_{ds} = 1~5 V for MoS_2 *n*MISFET with SPA&F.G. having the same L_{ch}, overlap and W_{mask} with Figure 6.6.

6.5 I_d-V_{ds} characteristics with SPA and/or F.G. annealing

Figure 6.8 is I_d-V_{ds} characteristics with only-SPA and only-F.G. annealing having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{gs} = 0~4 V. It is confirmed that MoS_2 film becomes metallic without SPA, and the leak current exists and pinch-off isn't observed without F.G. annealing because an interface trap density becomes high. Figure 6.9 is I_d-V_{ds} characteristics with SPA&F.G. having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{gs} = 0~4 V. With both annealing processes, I_d obviously increases with an increase in V_{gs} because of electric field effect and it saturates when V_{ds} increases. These results are consistent with Figure 6.6 and 6.7. Although the Schottky junction is still observed, by using $MoSi_2$ contact, junction characteristics seem to be improved compared with TiN contact [6.13]. The undulation in the saturation region is due to parallel transistors that have different contact resistance. As shown in Figure 6.10 (a), sputtered MoS_2 film has a small grain size and there is a region that has a high contact resistance. In addition, our MISFET has an SOI structure, so the effect of self-heating is observed. Therefore, the current in the saturation region is not unstable as shown in Figure 6.10 (b).

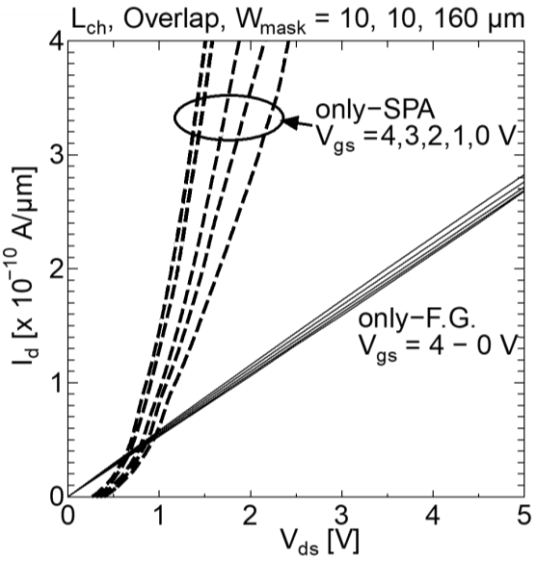


Figure 6.8 I_d-V_{ds} characteristics with only-SPA and only-F.G. annealing having the same L_{ch}, overlap and W_{mask} with Figure 6.6.

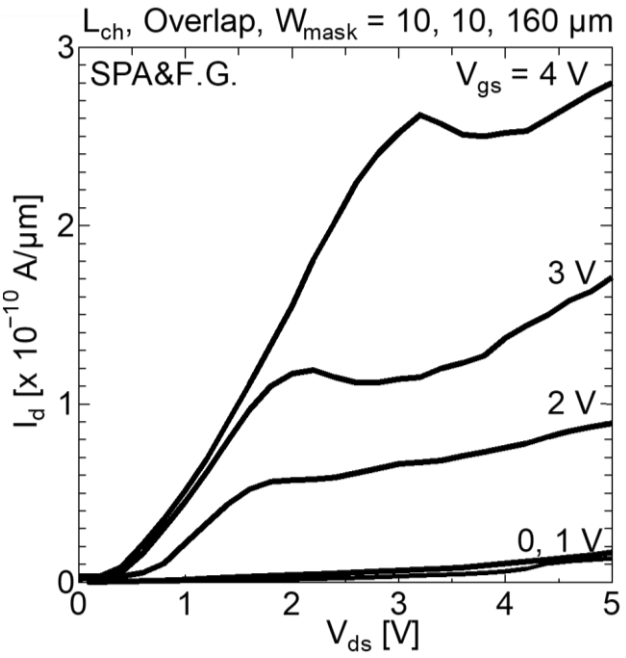
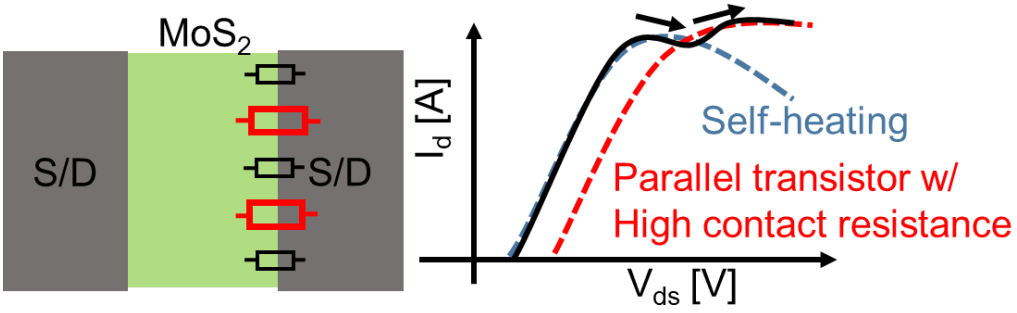


Figure 6.9 I_d-V_{ds} characteristics with SPA&F.G. having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{gs} = 0~4 V.



(a) (b)

Figure 6.10 Schematic illustrations of (a) parallel transistors with high contact resistance and (b) I_d-V_{ds} characteristics having parallel transistors and self-heating effect.

6.6 Parasitic resistance of *n*MISFETs with both SPA&F.G. annealing (SPA&F.G.)

From these devices, Figure 6.11 shows the resistance dependence on L_{ch} of nMISFETs with SPA&F.G. to extract the offset length from L_{ch} ($2\Delta L$) and R_{ext}. Due to the degradation of devices such as the oxidation of MoS_2 film, the same dependence of only SPA was not able to be measured. Because of the successful fabrication of *n*MISFETs, these values are respectively extracted as -1.2 μm and 2.96×10^{10} Ω-μm by (3.3). This $2\Delta L$ is caused by the difference between drawn and actual gaps of S/D regions. In section 3, the absolute value of $2\Delta L$ is 14.4 μm. Therefore, $2\Delta L$ is found to be reduced because SPA&F.G. increase the area of MoS_2 film which acts as a channel. The R_{ext} value of these MISFETs with a top gate is higher than that of CVD-MoS_2 film with back gate [6.15]. Therefore, S/D formation technology such as the doping technology is needed to be investigated.

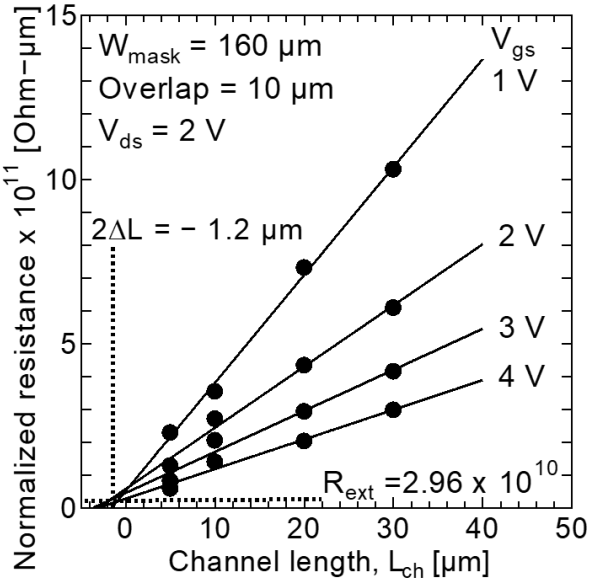


Figure 6.11 Resistance dependence on L_{ch} for W_{mask} of 160 μm, overlap of 10 μm and V_{ds} of 2 V.

6.7 Benchmark of mobility and off current (I_{off}) for MoS_2-FETs

In previous section, the L_{eff} and R_{ext} of MoS_2-*n*MISFETs with SPA&F.G. were calculated. Therefore, the peak value of the field-effect mobility with L_{eff} and deducted R_{ext} is calculated as 0.12 cm^2/V-s. Figure 6.12 shows the mobility comparison with the MoS_2 channels synthesized by three methods [6.10,6.11,6.16-6.23]. As shown in this figure, the mobility of sputtered MoS_2 film is lower than those of exfoliation and CVD methods. Enlargement of grain size of sputtered MoS_2 film, a decrease in contact resistance further and an introduction of doping technology are necessary. However, it is found that this is the first report showing normally-off operation of MoS_2 *n*MISFETs with a top-gate which is integrated in chip size. Figure 6.13 is the benchmark of I_{off} and V_{off} with MoS_2-*n*FETs and Si-FinFETs [6.24,6.25]. In this figure, MoS_2-*n*FETs have the lower I_{off} comparing with FinFETs. Moreover, sputtered MoS_2-*n*MISFET in this study has the compatible low I_{off} with the normally-off operation.

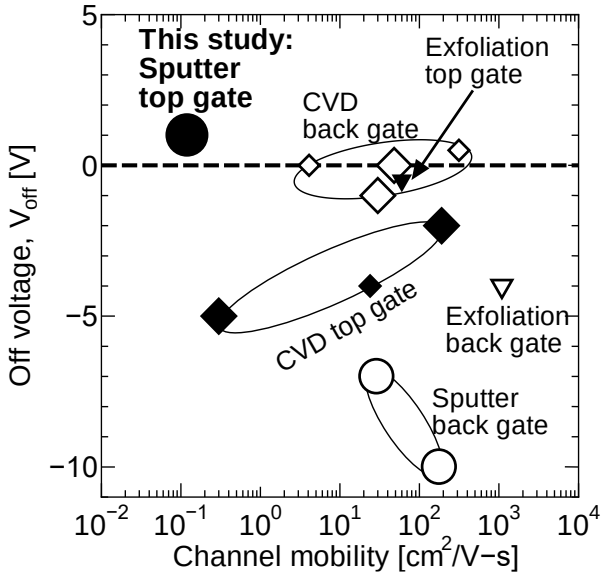


Figure 6.12 V_{off} comparison for MoS_2-*n*FETs. Large symbols mean that MoS_2 film is chip scale and also active region was defined by lithography. On the other hand, small symbols mean that MoS_2 film is not chip scale and also the devices are not patterned by lithography. This result is the first report showing normally-off operation with a top gate structure.

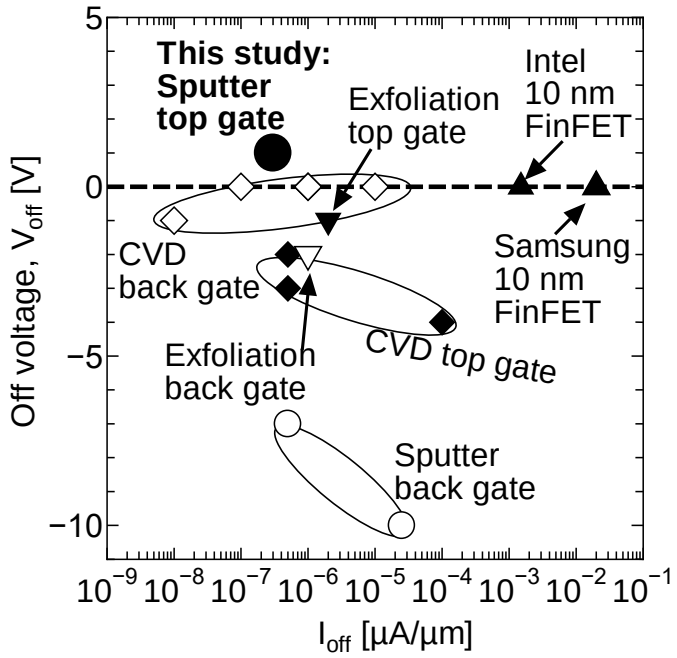


Figure 6.13 Benchmark of I_{off} and V_{off} for Si-FinFETs and MoS_2-FETs. MoS_2-FETs have the lower I_{off} than Si-FinFET one. Our normally-off FET achieves the compatible low I_{off} with other MoS_2-FETs.

6.8 Characteristic difference between only-SPA and SPA&F.G.

In this section, we analyze about the characteristic difference between only-SPA and SPA&F.G. Figure 6.14 shows the result of difference extraction between only-SPA and SPA&F.G. from Figures 6.6 and 6.7 at V_{ds} = 5 V. Only-SPA shows the higher I_d than SPA&F.G. and we could extract the differences that I_d shifts in the negative direction and V_{off} shifts in the positive direction and I_d becomes 0.18 times. The cause of the negative shift of I_d is the decrease in leak current through SiN/MoS_2 film or grain boundaries of MoS_2 by H_2 termination of F.G. annealing. The positive shift of V_{off} is caused by the decrease in Q_f and Q_{it} by F.G. annealing [6.5,6.6]. 0.18 times of I_d means the drop of g_m, which is expressed by the following formula,

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \propto \mu C_{ox} \frac{W_{eff}}{L_{eff}} \qquad (6.1),$$

where μ is the mobility, C_{ox} is the capacitance of the dielectric layer. As (6.1) shows, g_m is in inverse proportional to L_{eff}. F.G. annealing is speculated to achieve improvement of crystallinity, H_2 termination of sulfur defects and MoO_3 reduction toward MoS_2. This leads to increase the area of MoS_2 film, which acts as a channel. Accordingly, the top-view sputtered MoS_2 film with only-SPA and SPA&F.G. can be illustrated as shown in Figure 6.15. Light, normal and dark green mean high V_{th} area, low V_{th} area and leaky MoS_2 area, respectively. The channel region has is the rectangle in which L_{ch} is shorter than W_{mask} as shown in Figure 6.3. Therefore, the decrease in L_{eff} is expected to lead to an increase in g_m as shown in (6.1). Figure 6.16 shows normalized g_m characteristics by W_{mask} of 160 μm and (a) L_{ch}, (b) L_{eff} with SPA&F.G. having overlap of 10 μm. L_{eff} values are calculated using (3.3) and 2ΔL of -1.2 μm extracted in previous section. As the fitting curves show in these figures, the variation of g_m in (b) is smaller than that in (a), which means that the L_{eff} express the channel length more precisely. In addition, it can be confirmed that non-normalized g_m becomes larger as L_{eff} becomes shorter as shown in Figure 6.16 (b).

Moreover, the variation of contact resistance is speculated to be another cause of characteristic difference between only-SPA and SPA&F.G. Figure 6.17 shows I_d-V_{ds} characteristics with only-SPA and SPA&F.G. having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{gs} = 4 V. In this figure, SPA&F.G. has a higher contact resistance than only-SPA. Figure 6.18 shows cross-sectional SEM image of n-doped poly-Si after CDE. In this figure, the roughness at the edge of n-doped poly-Si is observed. This roughness is expected to lead the variation of the contact resistance between S/D regions and MoS_2 channel because our MoS_2 film is atomical thin. In addition, Mo tends to differ in Si when $MoSi_2$ is formed and n-doped poly-Si. Therefore, the direction of the silicide formation tends to be unstable. The twice annealing process for controlling the shape of silicide material is one of the promising solutions because it can form a thin intermediate layer at low temperature, removes residual metal, forms the silicide layer at high temperature.

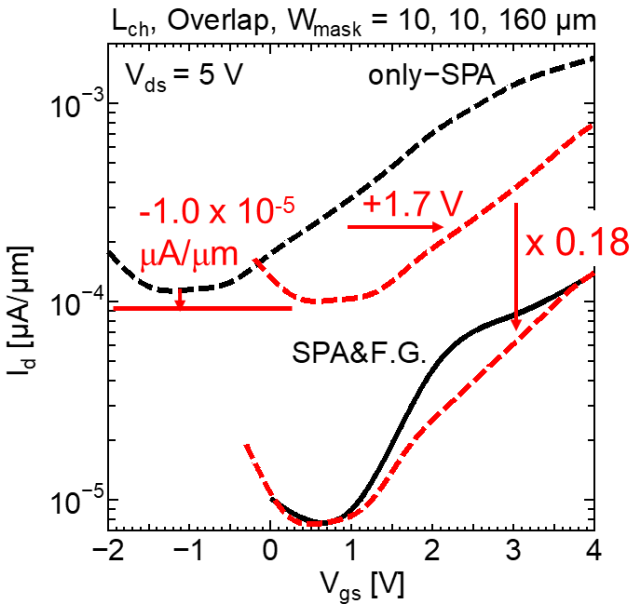


Figure 6.14 Difference extraction between only-SPA and SPA&F.G. from Figure 6.6 and 6.7 at V_{ds} = 5 V.

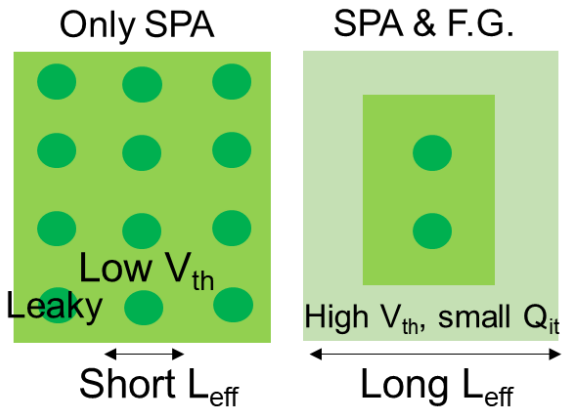
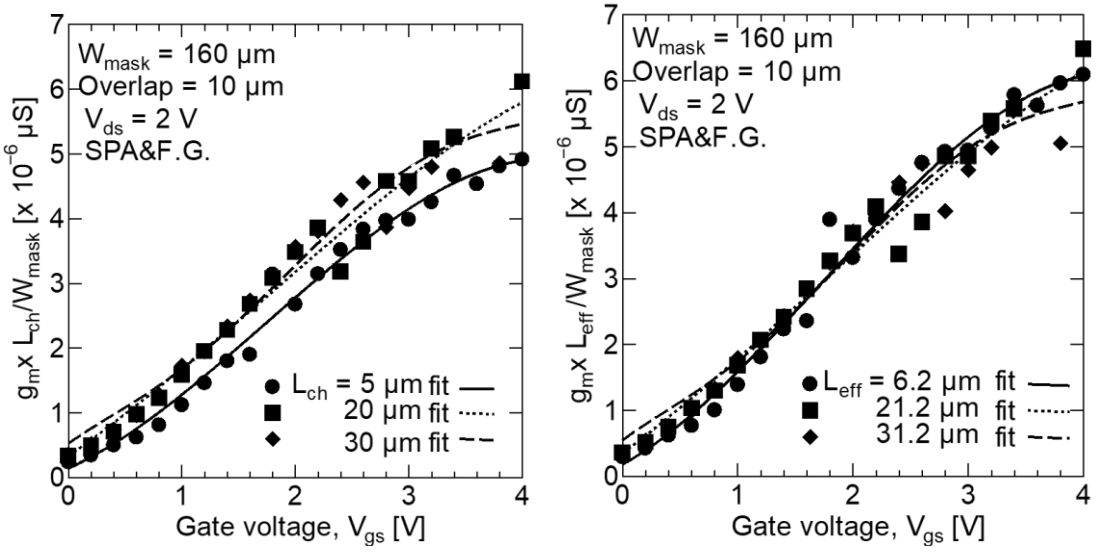


Figure 6.15 Schematic illustration of top-view sputtered MoS_2 film with only-SPA and SPA&F.G.. Light, normal and dark green regions mean high V_{th} area, low V_{th} area and leaky MoS_2 area, respectively.



(a) (b)

Figure 6.16 Normalized g_m characteristics by W_{mask} of 160 μm and (a) L_{ch}, (b) L_{eff} with SPA&F.G. having overlap of 10 μm. The solid lines are fitting curve for L_{ch} of 5 μm and L_{eff} of 6.2 μm. The dotted lines are fitting curve for L_{ch} of 20 μm and L_{eff} of 21.2 μm. The dashed lines are fitting curve for L_{ch} of 30 μm and L_{eff} of 31.2 μm.

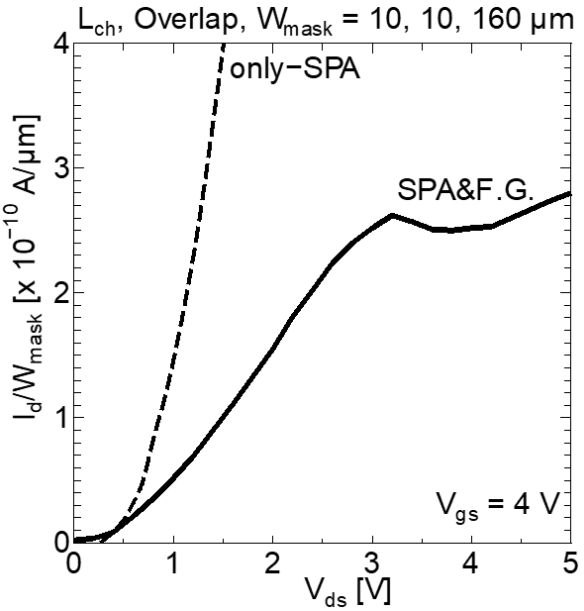


Figure 6.17 I_d-V_{ds} characteristics with only-SPA and SPA&F.G. having the same L_{ch}, overlap and W_{mask} with Figure 6.6 at V_{gs} = 4 V.

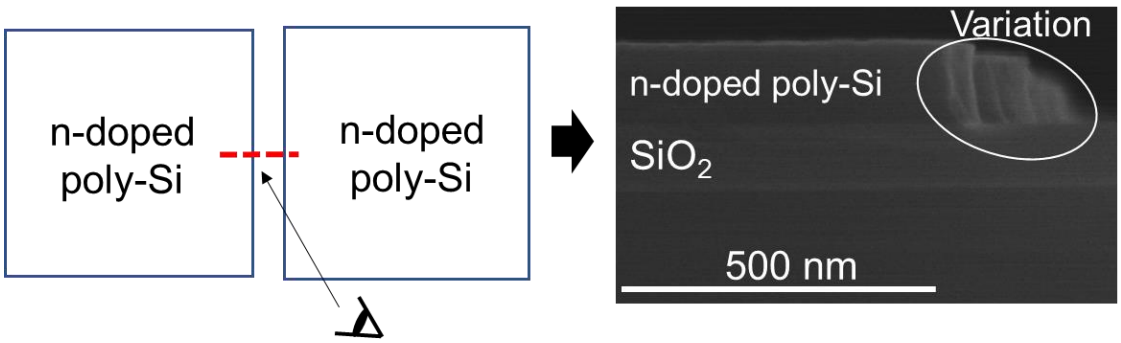


Figure 6.18 Cross-sectional SEM image of n-doped poly-Si etching and resist removal. There is the roughness at the edge of n-doped poly-Si.

6.9 Summary

We successfully realize the top-gate sputtered-MoS_2 *n*MISFETs which are integrated into chip scale and exhibits normally-off operation in the accumulation mode for the first time (the chip size is 2.5 x 2.5 cm^2). This is owing to the improvement of the fabrication process such as piranha cleaning, SiN passivation, and SPA&F.G.. SiN passivation enhances the process endurance of MoS_2 film and realizes the monolayer Al_2O_3 structure. SPA compensates for sulfur vacancies and F.G annealing decreases O_f and Q_{it}. $MoSi_2$ contact with acid cleaning reduced the carbon contamination and contact resistance down to 2.6×10^{-2} Ohm-cm^2. Although the on current of ~10^{-4} μA/μm, the on-off ratio of ~100 and mobility of 0.12 cm^2/V-s are still smaller than those using the exfoliation and CVD methods, the compatible low I_{off} of 10^{-6}~10^{-7} μA/μm is successfully confirmed.

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Chapter 7 Conclusions

7.1 Summary of this thesis

Owing to promote the industrial application of MoS_2 film, the author focuses on the establishment of the device integration process for sputtered MoS_2-*n*MISFETs and improvement in its performance, with evaluating the characteristics of key underlying technologies.

In chapter 3, we successfully confirmed n-type operation of chip level integrated MoS_2-*n*MISFETs with a top gate by a bunch of methods of RF magnetron sputtering, twice Al_2O_3 passivation, and H_2S annealing. This integration process enabled us to extract effective mobility of 0.11 cm^2/V-s was using the resistance dependence on gate length. Although the mobility is still lower than those using exfoliation and CVD methods, the performance was found to be improved by large grain size, low carrier density, low interface-trap density and fixed-charge density of Al_2O_3 film.

In chapter 4, pressure and temperature dependences of SPA were discussed in terms of crystallinity and electrical characteristics. By reducing the pressure in the quartz tube down to 100 PA, the partial pressure of sulfur increases and the amount of sulfur atoms that react with Mo atom also increases. At high temperature around 700^{o}C, the crystallinity and S/Mo composition ratio was improved further. As a result, the carrier density was reduced down to 1.8 x 10^{16} cm^{-3} and electron mobility was increased from 1.7 up to 25.2 cm^2/V-s when temperature and pressure are 700^{o}C and 100 Pa, respectively. As a result, we confirmed the sulfur vacancies were compensated further and these values are superior to H_2S anneal's ones.

In chapter 5, $MoSi_2$ contact was demonstrated by TLM device in order to reduce the contact resistance. Taking a contact area between MoS_2 film and metal account into, surface contact is better than edge contact and we selected the bottom contact not to damage the MoS_2 film when

forming a contact pattern on it. Making $MoSi_2$ region at the interface of n-doped poly-Si, the contact resistance was reduced down to 2.6 x 10^{-2} Ohm-cm^2 and the activation energy became lower than Si contact. This result indicates that $MoSi_2$ at the interface was the main current path.

In chapter 6, we remarkably achieved normally-off sputtered MoS_2-*n*MISFETs with a top gate. The chip area is 2.5 x 2.5 cm^2. In addition to SPA and SiN passivation, F.G. annealing at 300^{o}C for 30 min played an important role in reducing interface trap density and positive fixed charge in order to realize normally-off operation. Although the mobility of 0.12 cm^2/V-s still has room to be improved, the I_{off} of 10^{-6}~10^{-7} μA/μm was lower than Si-FinFETs and compatible low with the previous report of MoS_2 FETs. This is the first report of chip level integrated MoS_2-nMISFETs with a top gate showing normally-off operation and this process could lead to realize high-volume manufacturing of TMDC channel FETs for IoT of human interface devices.

Table 8.1 is the summary of the annealing processes for TLM device and MISFET. The purpose of TLM device is to investigate the $MoSi_2$ contact by a simple process, so SPA was not introduced. Alloying at 700^{o}C achieves the lowest contact resistance thus SPA at 700^{o}C was introduced for the sulfur compensation and the decrease in contact resistance. F.G. annealing is for decreasing Q_{it} and O_{ff}. Therefore, both annealing processes for MISFET are an essential process to realize normally-off operation.

Table 8.2 shows the comparison of several properties with sputtered MoS_2 film and other materials for display application. At present, sputtered MoS_2 film has compatible mobility with amorphous Si. The transmittance of a few layer MoS_2 is reported as more than 80 % at a wide range wavelength [7.1]. The strong point of MoS_2 is that it has high mobility and flexibility and transparency at the same time. Considering the application toward the flexible display, the competitions are oxide semiconductors such as IGZO and organic semiconductors. To overcome these materials, it is necessary to increase the mobility of sputtered MoS_2 film to around 20 cm^2/V-

s which realize 4 k display. Future direction for realizing such mobility is discussed in the next section.

Table 8.1 Summary of annealing process for TLM device and MISFET.

	TLM			
	Purpose	Temp. [°C]	Structure	Result
SPA				
Alloying	**Decrease in contact resistance**	300 ~ 700	MoS_2 /$MoSi_2$	Lowest contact resistance @700°C

	MISFET			
	Purpose	Temp. [°C]	Structure	Result
SPA	/ Sulfur compensation for MoS_2 film **/ Decrease in contact resistance**	700	MoS_2 /$MoSi_2$	/ Sulfur compensation →Normally-off / Improve of I_d-V_{ds}
F.G.	/ Decrease in interface trap density	300	Al_2O_3 /MoS_2	Decrease in trap density →Normally-off

Table 8.2 Comparison of several properties with sputtered MoS_2 film and other materials [7.1].

	Sputtered MoS_2	c-Si	poly-Si	a-Si	Oxide Semi. (Ex : IGZO)	Organic Semi. (Ex : Pentacene)
Band gap [eV]	1.2	1.12	1.12	~1.8	3	~ 3
Mobility [cm^2/V-s]	0.12	~500	>100	0.5	~10	< 10
Flexibility	○	×	×	×	△	○○
Transparency	○	×	×	×	○	○

7.2 Future directions

As mentioned in the previous section, the future direction of sputtered MoS_2 film is related to how to improve the mobility with keeping normally-off operation and low I_{off}. For future work, it should be considered that the growth mechanism of sputtered MoS_2 thin film resulting in enlargement of grain size. In addition, the device structure and process still have room for improvement. Therefore, the author listed the three important parameters as follows.

i. Grain size

As discussed in the previous chapter, the small grain size of sputtered MoS_2 film poses several challenges such as electron scattering, instability in the water, junction leak and so on. Especially, small grain size means that sputtered MoS_2 film has many grain boundaries. It is reported that grain boundary has a deep energy level (approximately 0.6 eV from conduction band maximum) and it acts as an energy barrier or electron trap [7.2]. Hence, to enlarge the grain size is essential and the control of the number of atoms and energy when they arrive at the substrate is expected to be valid because the cause of small grain size is that another atom conflicts before MoS_2 nuclear growth. The key conditions in sputtering are substrate temperature, pressure and distance between substrate and target. Our group has already adjusted these parameters and succeeded to improve the grain size and mobility of a few layer as-sputtered MoS_2 film as shown in Figure 7.1,7.2,7.3 and this good quality film will improve mobility. The grain size is calculated by Inverse Fast Fourier Transform and the grain orientation might be different even with the same size grain. Although we need to investigate the effect of SPA for the grain size, there is still room for enlarging the improvement. Accordingly, to insert the metal mesh and apply the voltage is one of the promising options as shown in Figure 7.4. It enables us to control the number of target ion with adjusting the positive or negative voltage and the amount of it.

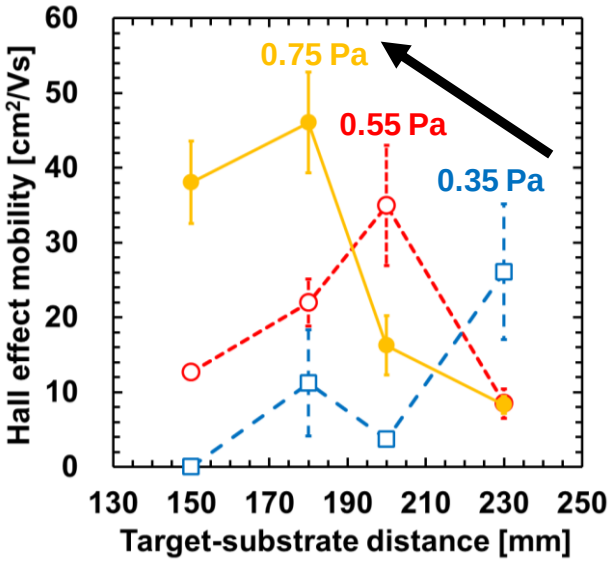
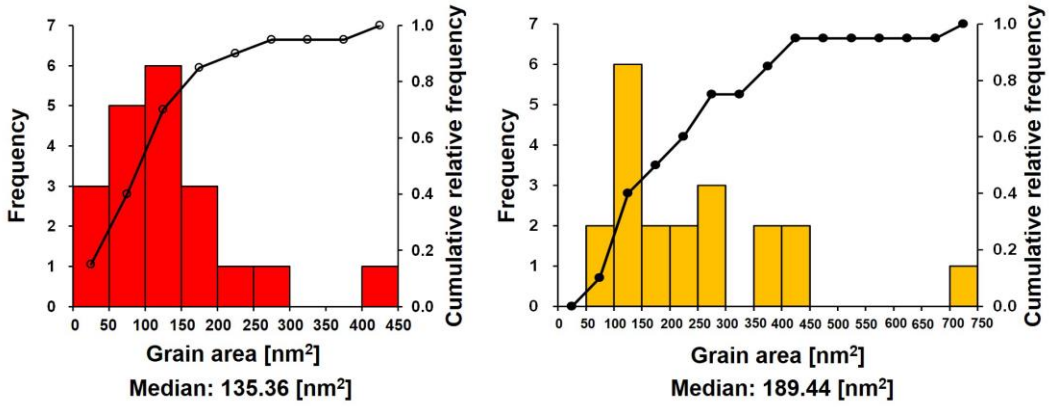


Figure 7.1 Hall-effect mobility dependence on target-substrate distance under Ar pressures of 0.35, 0.55, 0.75 Pa. The MoS_2 film in this study was sputtered with target-substrate distance of 230 mm, pressure of 0.75 Pa and mobility was around 10 cm^2/V-s. Mobility has the possibility to be increased up to ~46 cm^2/V-s [7.3].



(a) (b)

Figure 7.2 Comparison of crystal grain area of (a) 0.55 Pa and (b) 0.75 Pa sample [7.3]. The tendency that the mean grain size of MoS_2 film deposited at 0.75 Pa is bigger than one at 0.55 Pa. The number of samples is 20.

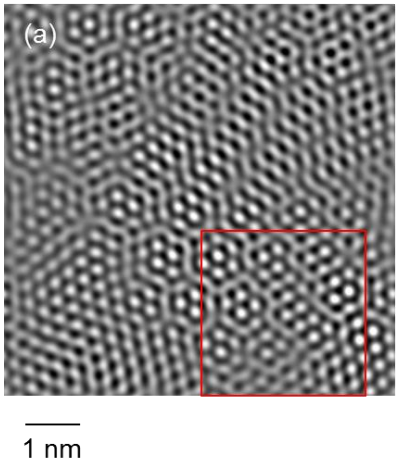


Figure 7.3 FFT filtering result for plan STEM image of as-sputtered MoS_2 film of 6 layers [7.3].

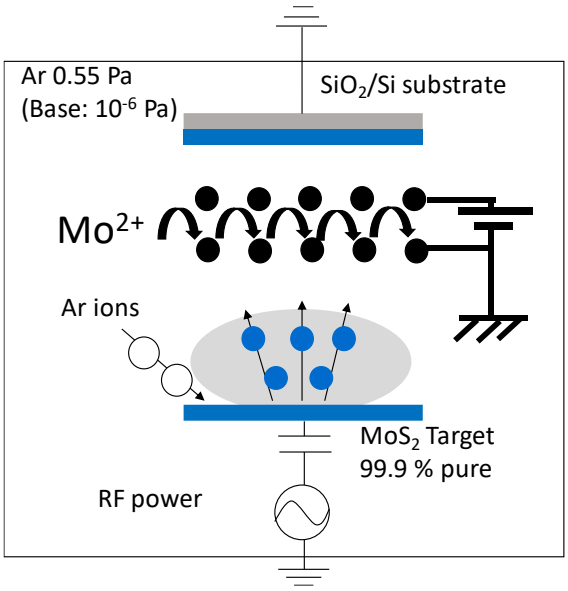


Figure 7.4 Schematic illustration of Mo mesh in the sputter chamber. Mo^{2+} ion is prevented from arriving at the substrate in this figure.

iii. Doping technology

In order to decrease contact resistance further and decease the wafer-wafer variation, doping technology for contact region and optimization of the shape of contact is necessary.

In addition to doping technology, controlling the sulfurization for the contact region is a promising approach to decrease contact resistance. It is reported that sulfur tends to detach when it is annealed in an ultra-high vacuum (UHV) and the sulfur detachment can be prevented with thin ALD-deposited Al_2O_3 film [7.4,7.5]. As shown in Figure 7.5, S/Mo ratio decreased by UHV annealing from 200°C. On the other hand, S/Mo ratio is improved because of migration with 2-nm Al_2O_3 film. Therefore, only sulfur around the contact region can be detached by covering only the above channel MoS_2 film. Sulfur defects act as n-type dopants, so this sulfur detachment is expected to realize the same effect of doping.

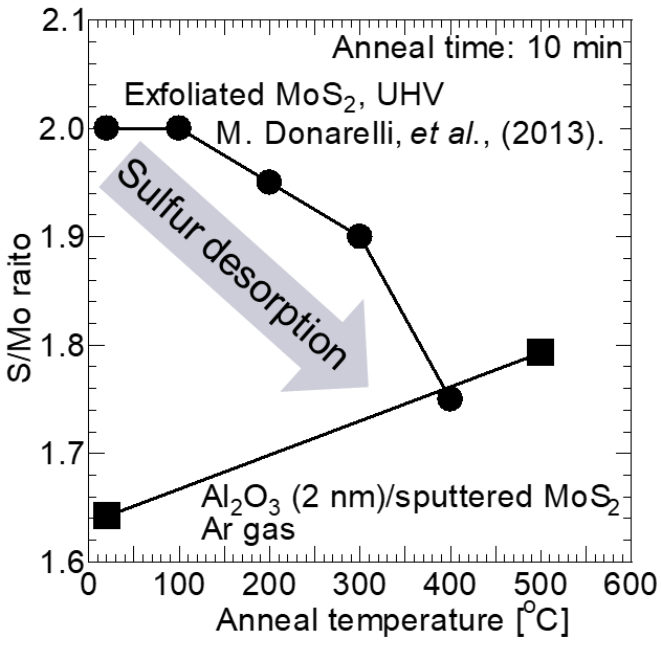


Figure 7.5 S/Mo ratio of exfoliated MoS_2 film and Al_2O_3/MoS_2 at several annealing temperatures [7.4,7.5].

iv. The roughness of SiO_2 substrate

The mobility of sputtered MoS_2 film is deteriorated by the roughness of SiO_2 substrate. It was reported that DHF cleaning make SiO_2 substrate rougher and the mobility was decreased [7.6]. Moreover, an over-etching also damages the SiO_2 substrate when the contact region is patterned on it. Therefore, we have to be careful not to make the roughness of SiO_2 substrate. In this study, DFT cleaning was used twice and the damage from over-etching by CDE is concerned. The new process for the contact region without damaging the substrate has to be introduced.

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Appendix Thermoelectricity of $MoSe_2$

From August 2015 to February 2016, I researched about thermoelectricity of $MoSe_2$ in Professor Andras Kis Laboratory in EPFL, Switzerland as an exchange student. In this appendix chapter, I'm going to explain my research in EPFL.

In thermoelectricity, the Seebeck effect is very important because this effect means that when there is a temperature gradient in one material, the career excites in only the hotter part and the career differs and finally we can get electromotive force from temperature gradient as shown in Figure A.1 [A.1]. In addition, as you can see in Figure A.2, by using two semiconductors, n-type and p-type, connected to a common source of heat supply, we can get current by using only temperature gradient. This is because the hot end has low density of charge carriers (electrons for n-type and holes for p-type), whereas the cold end has a higher density of charge carriers by thermal gradient and this distribution of charges gives birth to an electric field across the junction. Eventually, when a conductor is used to connect the two ends of the junction, charges begin to flow and electric current is produced. Therefore, the energy source is the only temperature so it is expected to be a promising route for power generation.

The Seebeck coefficient is an important parameter of the Seebeck effect and it can be calculated by using the following equation,

$$\mathrm{k_e} = \left(\frac{2\mathrm{T}{K_B}^2}{\mathrm{h}}\right)\left(I_2 - \frac{{I_1}^2}{\mathrm{I_0}}\right) \quad [W/Km] \qquad \text{(A.1),}$$

$$\mathrm{S} = -\left(\frac{K_B}{\mathrm{q}}\right)\frac{I_1}{I_0} \quad [V/K] \qquad \text{(A.2), and}$$

$$I_j = \mathrm{L}\int_{-\infty}^{\infty}\left(\frac{E - E_F}{k_B T}\right)^j \bar{T}(E)(-\frac{\partial f_0}{\partial E})dE \qquad \text{(A.3).}$$

Power Factor (PF) and ZT are also an important parameter and these can get from the Seebeck

coefficient and electrical conductivity, temperature and thermal conductivity.

$$\mathrm{PF} = S^2\sigma \ \ [WK^{-2}m^{-2}] \qquad \text{(A.4)},$$

$$\mathrm{ZT} = S^2\sigma/k_e \ \ [WK^{-2}m^{-2}] \qquad \text{(A.5)},$$

where E_F is Fermi-level, S is the Seebeck coefficient, σ is electrical conductivity, T is temperature, k_e is thermal conductivity, L is device length, q is magnitude of electron charge, h is Planck's constant, k_B is Boltzmann's constant, T(E) is transmission function.

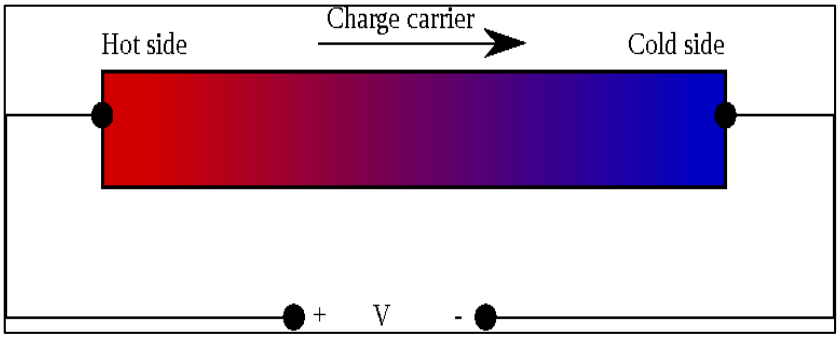

Figure A.1 Principle of the Seebeck effect [A.1].

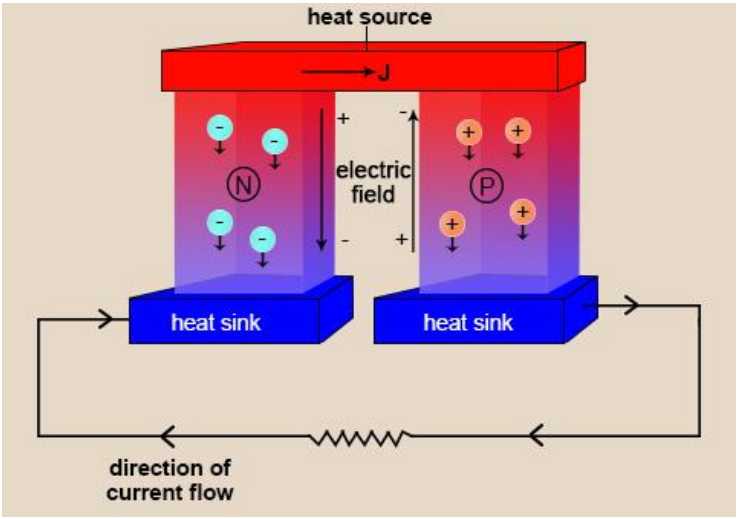

Figure A.2 Principle of circle using Thermoelectric conversion element [A.2].

And recently, two dimensional materials such as MoS_2 have been attracted because these have good thermoelectric properties. For example, the PF of MoS_2 is 8.5 $mWm^{-1}K^{-2}$ at room

temperature and two times higher than that of the most prevalent and commercial thermoelectric material Bi_2Te_3 [A.3,4]. Furthermore, the research for the thermoelectric property of other two-dimensional materials has also been proceeding. Table A.1 and Table A.2 show the results of the calculation for PF and ZT of four materials MoS_2, $MoSe_2$, WS_2, WSe_2 for several temperatures and thickness respectively by using from equation (A.1) to (A.5) [A.4]. In this calculation, Fermi-level is calculated by DFT and these are maximum PF by Fermi-level because the fermi-level of these two-dimensional materials changes by thickness. As you can see in table A.1, monolayer and bilayer $MoSe_2$ show good PF comparing with other materials. Moreover, bilayer $MoSe_2$ shows good ZT comparing with other materials as shown in table A.2. The Seebeck coefficient is an important property for deciding PF or ZT, therefore I chose $MoSe_2$ and these data are just result of calculation so I tried to measure the coefficient experimentally.

Next, I will talk about how to measure experimentally. Actually, the thermoelectricity of MoS_2 has already been measured experimentally by using the devices shown in Figure A.3 [A.5]. In these devices, there are two or four thermometers and one heater. By using the heater, we can give birth to the temperature gradient and measure the Seebeck coefficient and electrical conductivity for back gate voltage or temperature. Eventually, in that previous work, the obtained maximum value of the Seebeck coefficient is 30 mV/K at 280 K yields, which is remarkably larger than other low-dimensional materials, such as graphene (~±100 μV/K), Bi_2Te_3 (~±200 μV/K), semiconducting carbon nanotubes (~300 μV/K), Ge−Si core−shell nanowires (~400 μV/K), and InAs nanowires (~−5 mV/K) [A.5]. Taking into account these previous works such as calculation and experiment for thermoelectric property of two-dimensional materials, my research purpose was to measure the thermoelectric property of $MoSe_2$ applying the device shown in Figure A.4.

Table A.1 Comparison of Power Factor.

	Temperature	**1L**	**2L**	**3L**	**4L**	**Bulk**
MoS_2	300K	0.130	0.140	0.280	0.220	0.032
	150K	0.093	0.093	0.190	0.120	0.012
	77K	0.072	0.072	0.130	0.063	0.012
$MoSe_2$	300K	**0.340**	**0.330**	0.230	0.230	0.022
	150K	**0.151**	**0.200**	0.100	0.100	0.013
	77K	**0.062**	**0.120**	0.062	0.052	0.013
WS_2	300K	0.240	0.280	0.270	0.240	0.022
	150K	0.110	0.160	0.150	0.130	0.010
	77K	0.051	0.081	0.070	0.081	0.010
WSe_2	300K	0.260	0.240	0.190	0.160	0.022
	150K	0.141	0.140	0.081	0.070	0.010
	77K	0.071	0.082	0.050	0.043	0.011

Table A. 2 Comparison of ZT

	Temperature	1L	2L	3L	4L	Bulk
MoS_2	300K	1.35	1.35	**2.23**	1.78	0.350
	150K	0.590	0.590	**1.03**	0.660	0.110
	77K	0.240	0.240	**0.420**	0.210	0.031
$MoSe_2$	300K	1.39	**2.39**	1.66	1.65	0.290
	150K	0.450	**1.06**	0.610	0.570	0.100
	77K	0.130	**0.410**	.0220	0.170	0.030
WS_2	300K	1.52	1.98	2.03	1.85	0.280
	150K	0.411	0.613	0.770	0.721	0.104
	77K	0.120	0.181	0.211	0.271	0.034
WSe_2	300K	1.88	1.92	1.44	1.13	0.260
	150K	0.590	0.750	0.490	0.380	0.091
	77K	0.180	0.270	0.170	0.130	0.031

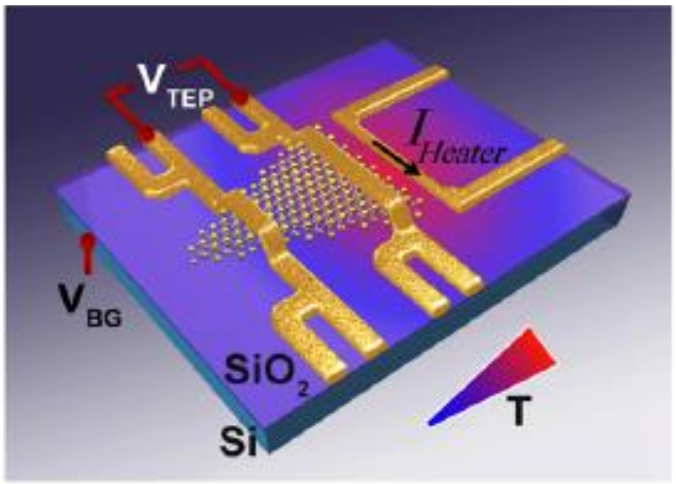

Figure A.3 Schematic diagram of device structure for measuring thermoelectric property [A.5].

Finally, I would like to say thank you to Prof. Andras Kis and his laboratory member. Although it was a first time for me to stay in foreign country by myself, thanks to them, I could have very precious experience and study many things for two dimensional materials. In the laboratory, there was very good condition for researching two dimensional material in terms of both talent and equipment.

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