論文 / 著書情報
Article / Book Information

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著者(和文)	Sun Zheng
Author(English)	Zheng Sun
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Category(English)	Doctoral Thesis
種別(和文)	論文要旨
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（博士課程）
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論 文 要 旨

THESIS SUMMARY

専攻： Department of	電子物理工学　専攻	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of (Philosophy)
学生氏名： Student's Name	Sun Zheng	指導教員（主）： Academic Supervisor(main)	Kenichi Okada
		指導教員（副）： Academic Supervisor(sub)	

要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

The aim of this thesis is to investigate and achieve a fully integrated small-area and low-power RF front-end using advanced CMOS technology toward the future IoT technology. The thesis is organized as follows:

Chapter 1 begins with an overview of the background of the IoT and the different wireless standards for IoT applications. In this part, the importance of the BLE standard is discussed. Based on the newly released Bluetooth standard core specification V5.2, the important specifications have to be analyzed for transmitter and receiver, respectively. According to the analysis, the key performances of some building blockers and design targets are specified. Chapter 1 also analyzed the design challenges for the low-power and small-area BLE TRX design when considering the actual applications.

Chapter 2 introduces an ultra-low-power transformer-based VCO for IoT applications. First, the VCO theory is revised, and some conventional VCO structures, typically low-power structures, are discussed. The impulse sensitivity function (ISF) is adopted to analyze the phase noise characteristics of oscillators. And the simulation method of the ISF function is organized and summarized. The proposed VCO achieves a -114.8 dBc/Hz PN at 1-MHz frequency offset with a 103uW power consumption. A -193 dBc/Hz FoM is achieved at 2.6 GHz oscillation frequency. The low-power operation and large transistor size improve the flicker corner to 16 kHz. The low-flicker noise and good $1/f^2$ PN performance allow the open-loop operation in a maximum 17-ms packet length BLE transceiver. And thus, the power efficiency of the TX can be further improved with the implementation of the proposed VCO. The PGS embedded TF used in this work indicates that the layout can be realized with a smaller on-chip area. The core area of the proposed VCO is only 0.12mm^2, as same as the transformer itself. To mitigate the PN degradation from the voltage ripple introduced by the DC-DC converter in battery-powered portable devices, a supply pushing reduction loop is embedded with the VCO while consuming no additional voltage headroom. The power consumption of this loop is also minimized to 40uW, and the supply pushing is reduced to 2 MHz/V, resulting in a -50 dBc spur with 5MHz sinusoidal ripples. This chapter also presents a good jitter performance and low power consumption injection-locked clock multiplier (ILCM) for IoT applications in 65nm CMOS. A transformer-based ultra-low-power (ULP) LC-VCO is proposed to minimize the overall power consumption. The introduced capacitor feedback path boosts the VCO loop gain, and thus a robust startup can be obtained. The proposed transformer-based VCO achieves -115.1 dBc/Hz at 1MHz frequency offset with a 97uW power consumption, which corresponds to a -194 dBc/Hz VCO figure-of-merit (FoM). Thanks to the proposed low-power VCO, the total ILCM achieves 78 fs RMS jitter while consuming 210uW power. A -269 dB FoM_{JP} of jitter and power is achieved by this proposed ILCM, and a -262 dB FoM_{JRP} is obtained while considering the 520MHz input reference with multiplication factor equals to 5.

Chapter 3 presents a miniaturized Bluetooth Low-Energy (BLE) transceiver (TRX) for short-range Internet-of-Things (IoT) applications in 65-nm CMOS. An integrated Radio-Frequency Input-Output (RFIO) embedded with transmitter/receiver (TX/RX) switch function and on-chip impedance matching is proposed. A hybrid-loop TRX structure based on a wide-BW fractional-N digital phase-locked loop (DPLL) is implemented to achieve the maximum power reduction. A -94 dBm receiver sensitivity is achieved with 2.3mW receiver (RX) power consumption while an RF receiving bypass route integration enhances the input power tolerance. The BLE transceiver delivers -6 dBm output power while consuming 2.6mW and achieves 18.5% maximum TX efficiency at 0 dBm output power. Thanks to the RFIO with harmonic suppression, -56 dBc of 2nd-order harmonic distortion (HD2) and -48 dBc of 3rd-order harmonic distortion (HD3) suppression are achieved with 0.85mm^2 on-chip area. This transceiver satisfied the BLE radio specification without the need for external filters and with low-power consumption, which enables minimum size and long lifetime modules.

Chapter 4 is the conclusions for the thesis and the presented studies. Finally, future works are discussed for further developing the presented research in this thesis, such as the Bluetooth 5 TRX and the high-performance frequency generator. In the Bluetooth 5 TRX design, a current-reused ring oscillator based low-power transmitter design is introduced. And multiple modes of the combination of the LC-oscillator and ring oscillator are conceived to realize both low-power mode and high-performance mode, which are specified in a new standard.

This thesis presents low-power and small-area RF front-end designs for short-range internet-of-things applications. To realize small size and long life-time modules, architecture considerations and key building blocks are discussed. To lower the power consumption and mitigate the supply variation with small on-chip area, a transformer-based low-power voltage-controlled oscillator with supply pushing reduction is presented and discussed in this thesis. An integrated radio-frequency input-output embedded with transmitter/receiver switch function and on-chip impedance matching is proposed. The proposed radio-frequency input-output is designed with minimized noise factor penalty for high-sensitivity receiver operation and harmonic suppression function for satisfying the out-of-band spurious emission requirements.

備考 ： 論文要旨は、和文 2000 字と英文 300 語を 1 部ずつ提出するか、もしくは英文 800 語を 1 部提出してください。
Note : Thesis Summary should be submitted in either a copy of 2000 Japanese Characters and 300 Words (English) or 1copy of 800 Words (English).