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Doctoral thesis

A Study on Rare Earth Gate Dielectrics for SiC MOSFET

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Abstract

Silicon carbide (SiC) is a promising candidate for high efficiency power device application. However, SiC metal-oxide-semiconductor field-effect transistor (MOSFET) using thermally grown silicon dioxide (SiO_2) as gate dielectrics suffer from degraded mobility as well as the reliability issues in threshold voltage (V_{th}). Various process technologies have been proposed to recover the degraded mobility so far. However, the negative shift in the V_{th} was enhanced by these processes. Insertion of rare earth oxide gate dielectrics has been reported to achieve both high mobility as well as high V_{th} at the same time. As the basic mechanism is not fully understood, further research on rare earth oxide gate dielectrics for SiC power devices is mandatory.

As the thermally grown interface structure seems to be origin of the degradation in mobility and the negative shift in the V_{th}, complete inhibition of the surface SiC oxidation or different surface SiC oxidizing process might be used to solve the problem. Therefore, in this study, as rare earth materials, yttrium-silicate (Y-silicate) and cerium oxide (CeO_x) dielectrics for SiC metal-oxide-semiconductor (MOS) capacitors and MOS field-effect transistors (MOSFET) have been investigated based on physical and electrical analyses. Coating with Y-silicate is known to protect the SiC surface from oxidation, thus preserving the initial surface after gate stack formation. On the other hand, CeO_x is known to oxidize the surface by means of radical oxygen species, expecting different type of interface structure.

A thermal stability of the Y-silicate interface layer with a thickness of 0.6 nm has been confirmed at 1000°C annealing. A lower interface state density (D_{it}) is lower, and a higher peak mobility of 19 cm^2/Vs with a high V_{th} of 4.2 V has been obtained compared to a

deposited-SiO_2 with the same process. Although limited improvements were obtained, initial surface treatment might further enhance the properties.

On the other hand, CeO_x interface layer has showed its thermal stability up to 1100°C process temperature. A high peak mobility of 54 cm^2/Vs with a V_{th} of 2.3 V has been obtained with the CeO_x interface layer, both higher than high-temperature NO-processed MOSFETs. Although there exists hysteresis in the gate voltage swing, the interface formation by means of CeO_x layer might be the key to forming the interface structure.

By stacking the rare earth gate dielectrics, namely CeO_x/Y-silicate or Y-silicate/CeO_x, a slight degraded mobility compared to CeO_x interface layer was obtained. However, the V_{th} showed a higher value, keeping the role of both gate dielectrics.

In conclusion, the effect of rare earth oxide interface layers for gate dielectric on SiC to the mobility and the V_{th} has been experimentally investigated. Suppression of the surface SiC oxidation by Y-silicate layer leads to the suppression of the negative shift in V_{th} with slight mobility recovery. CeO_x interface layer improves the mobility over 50 cm^2/Vs with suppression of negative V_{th} shift. The obtained results give insights and guideline to the interface formation structure for SiC MOSFET processes.

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Reference

1 Introduction

1.1 Introduction of SiC semiconductors and device application

SiC is a thermally and chemically stable material. SiC has no liquid state and sublimates at temperatures above 2000 degrees due to its high thermal stability. [1-1] In addition, SiC is the second hardest material after diamond due to its strong Si-C bonding. With these properties, SiC has been utilized in environment of high temperature and corrosion as a ceramic material. [1-2, 1-3]

Recently, SiC has also been focused as a semiconductor material. SiC is classified the IV-IV group element semiconductor, which shows polytypism in crystal growth. [1-4] This polytypism can be expressed by close-packed structure of atom. Typical crystal structures of SiC formed in crystal growth are shown in Fig. 1.1.1. 3C, 4H and 6H are Ramsdell notation, each number means that number of stacked atomic unit layers. C and H are initials of cubic and hexagonal, respectively. Moreover, each polytype has different electrical characteristics.
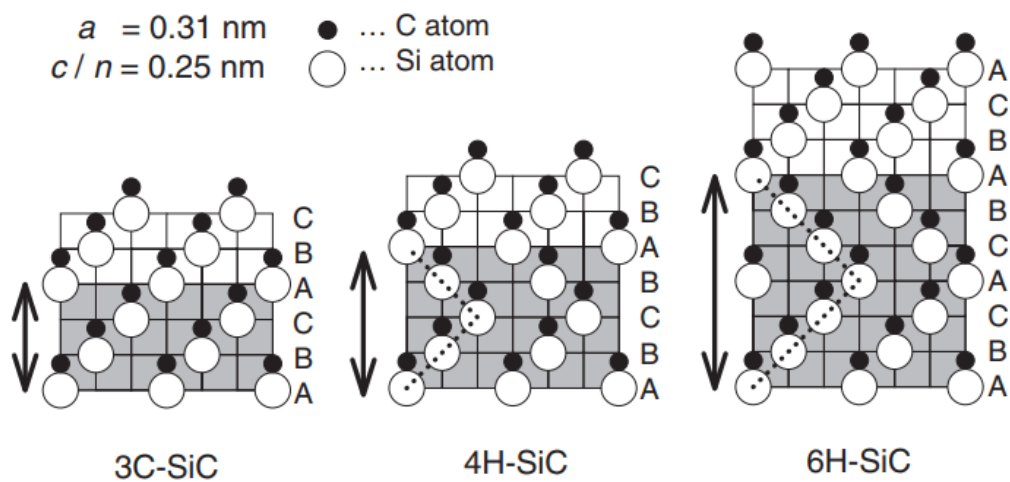

Fig 1.1.1 Arrangements of Si and C atoms for 3C-, 4H-, and 6H-SiC. A, B, and C are occupation sites of hexagonal close-packed structures. [1-5]

Material	Si	3C-SiC	4H-SiC	6H-SiC
E_g(eV) Bandgap	1.1	2.2	3.2	3.0
E_{BD}(10^6V/cm) Breakdown field	0.3	1.5	3.0	3.0
μ(cm^2/Vs) mobility	1450	1000	900	500
v_{sat}(10^6cm/s) Saturated velocity	10	27	22	19
κ(W/cm^{2}K) Thermal conductivity	1.5	5.0	5.0	5.0

Fig 1.1.1 Comparison of physical properties between Si and SiC. [1-6]

The physical properties of SiC are shown in Table 1.1.1. From the table, 4H-SiC has superior bandgap, breakdown field and bulk mobility than other polytypes. These properties of 4H-SiC are suitable for application in power devices. In comparison with Si, bandgap and breakdown field of 4H-SiC are 3 and 10 times higher, respectively. By using SiC instead of conventional Si, it is expected to be able to fabricate a semiconductor that operates stably in a high temperature and high voltage environment.

Particularly, SiC can realize high performance of devices with its high breakdown field. It has been reported that SiC Schottky barrier diodes (SBD) and metal-oxide-semiconductor field-effect transistors (MOSFET) show low on-resistance and significant power loss reduction. [1-7] Fig. 1.1.2 shows the electric field distribution in depleted layer of Si and SiC Schottky barrier diodes when back bias is applied. The maximum electric field (E_B) at junction interface is dielectric breakdown field strength. At this time, the depletion layer width is also maximized. Breakdown voltage is obtained by the area of each triangle. 4H-SiC can reduce a depletion layer width to 1/10 and increase doping
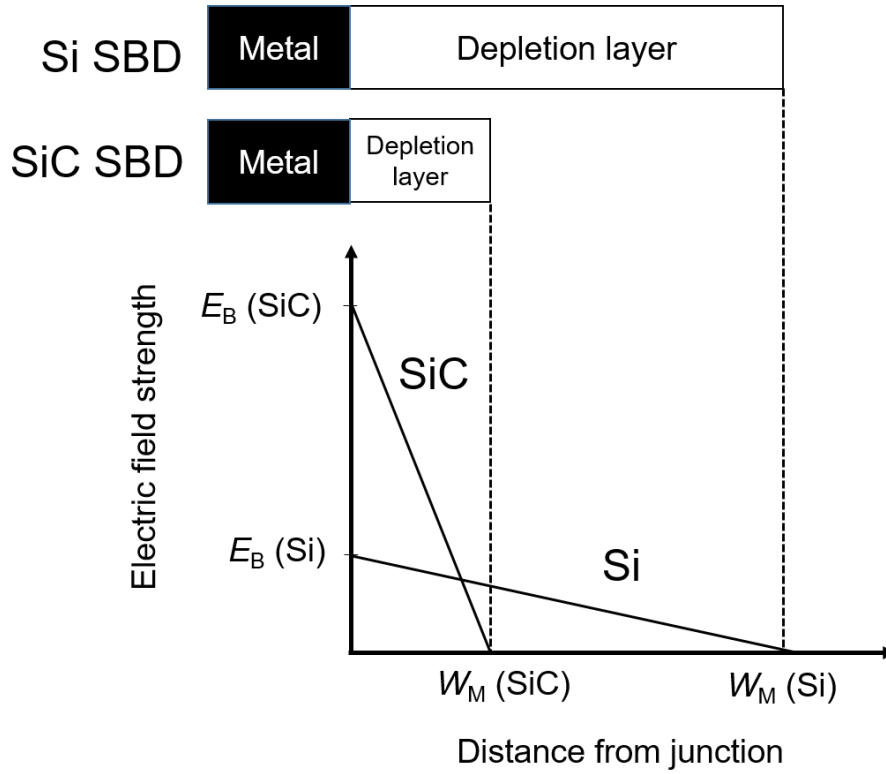
Fig 1.1.2 Electric field distribution in depleted layer of Si and SiC Schottky barrier diodes.

concentration in this region to 100 times. According to this, resistance of drift layer is significantly decreased to 1/300~1/500. On-resistance is dominant in resistance of drift layer, thus large reduction of on-resistance can be realized by SiC.

Fig. 1.1.3 shows the relation between on-resistance and breakdown voltage for Si and SiC. In case of same breakdown voltage, low on-resistance is realized by SiC introduction to devices. On the contrary, in case of same on-resistance, SiC devices can be operated in higher voltage than those of Si. Above mentioned advantages of SiC have been clearly demonstrated with numerous reports. With this superior property, SiC devices are expected to be widely spread to increase power efficiency of industry beyond the limit of Si.

Fig 1.1.4 shows the roadmap of semiconductor application in power devices. For conventional Si power devices, SBD and PiN diode have been used under 200 V and over 200 V blocking voltage, respectively. For switching devices, Si MOSFET can be used up to 600 V blocking voltage. Although Si insulated gate bipolar transistor (IGBT) can realize a higher blocking voltage than Si MOSFET by its bipolar operation, which has suffered from switching loss issue. [1-8] However, unipolar SiC power devices allow application over 5 kV blocking voltage. Additionally, ultra-high voltage application over 5 kV~10 kV is predicted with SiC IGBT/PiN. While performance of Si power devices is reaching its limit, industrial demands are increasing. To realize a society of high energy efficiency, SiC might be the key material of power devices
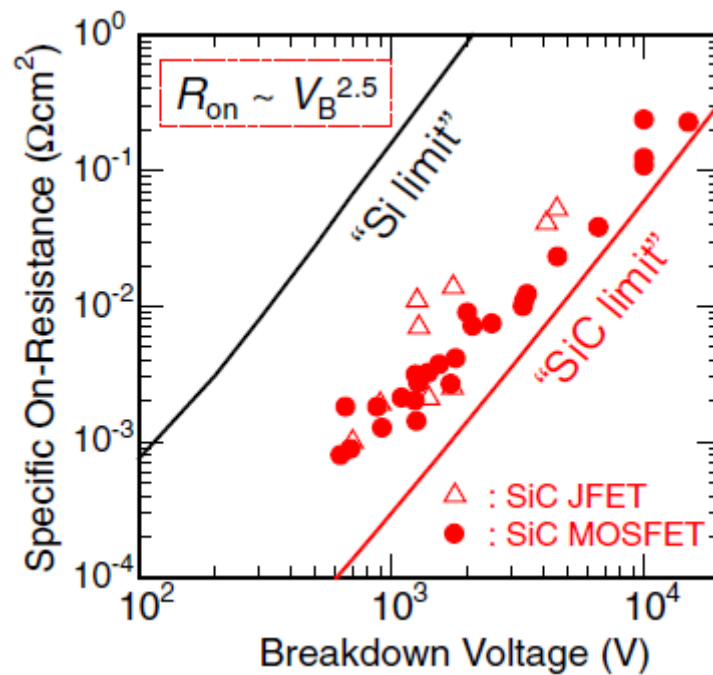
Fig 1.1.3 Minimum specific on-resistance for Si and SiC unipolar devices versus the blocking voltage. [1-9]
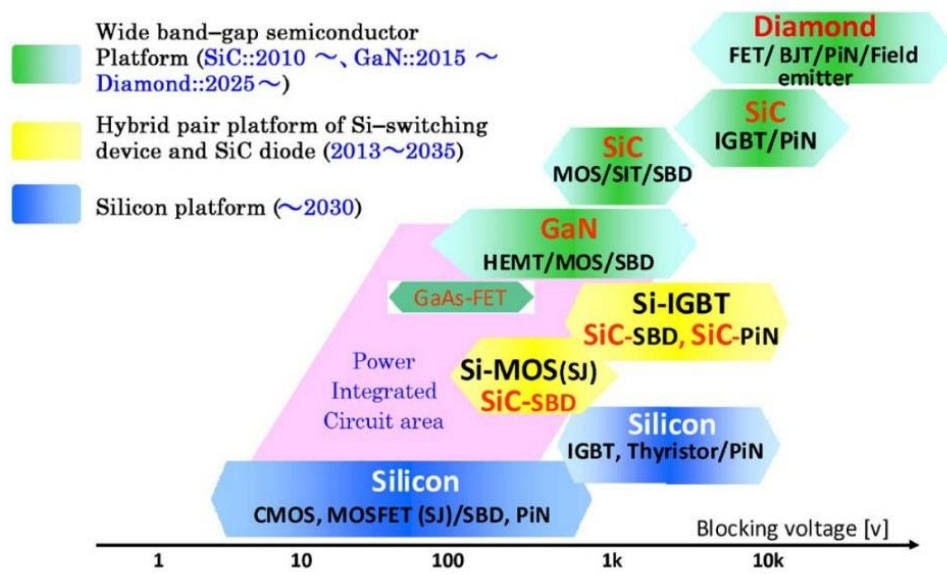
Fig 1.1.4 Application field and trend of semiconductor in power devices. [1-10]

1.2 Issues in SiC devices

1.2.1 Electron mobility degradation

A unique advantage of SiC over other wide bandgap semiconductor is a growth of SiO_2 by thermal oxidation, which is advantageous for device fabrication using traditional Si process. However, thermally grown SiO_2 dielectrics cause degradation of electron mobility in SiC MOSFET. Most of reported the channel electron mobility of SiC MOSFETs using thermally grown SiO_2 still at the level of 10~40 cm^2/Vs as shown in Fig. 1.2.1.1. This low inversion channel mobility inevitably leads to much higher on resistance of SiC power devices. [1-11, 1-12] The mobility of 10~40 cm^2/Vs is insufficient to reach SiC limit, therefore, over 100 cm^2/Vs is required for 1.2 kV blocking voltage
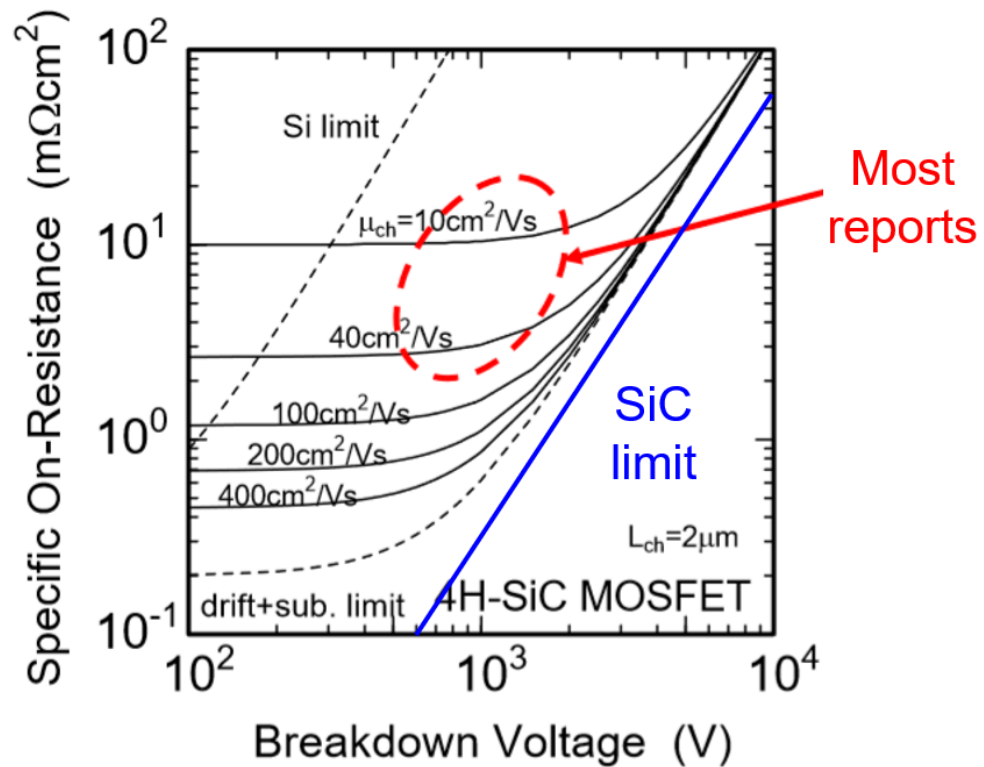
Fig 1.2.1.1 Characteristics of specific on-resistance and breakdown voltage by electron mobility variation.

application. Breakdown voltage of 1.2 kV is mainly applied to rated voltage over 500 V, which is major region of industry such as electric vehicles, motor control or heating. [1-9] Thus, the mobility issue of SiC is critical for application of power devices.

For mobility issue, high interface state density (D_{it}) at SiO$_2$/SiC interface has been reported as one of the causes. [1-13] Especially, carbon-related defects have been considered as one of the causes for high D_{it}. During thermal oxidation of SiC, most of the excess carbon is transformed into CO molecules and diffused from interface. However, some of the carbon atoms can remain at interface and form carbon clusters or graphitic regions. [1-14~16] In addition, oxygen defects have also been considered for high D_{it} issues. The high D_{it} near the SiC conduction band edge is caused by oxide defects located close to the interface, which defects affect mobility degradation. [1-17, 1-18] This kind of defect may result from the oxygen vacancy, or from the dangling bond originates from the lattice mismatch of SiO$_2$ with SiC. Many reports have shown that there is a strong relationship between D_{it} and electron mobility for SiC MOS-devices. [1-19~22] From these reports, an inverse proportional relationship between D_{it} and electron mobility can be summarized for increasing of mobility with reduction of D_{it}. To achieve high electron mobility, reduction of D_{it} below 10^{11} cm^{-2}Vs^{-1} is necessary. D_{it} of 10^{10}~10^{11} cm^{-2}Vs^{-1} is comparable to SiO$_2$/Si interface level, which may be the key factor for increasing mobility of SiC devices.

Electron mobility degradation by high D_{it} is mainly related to coulomb scattering phenomenon. Fig. 1.2.1.2 shows the schematic illustration of mobility degradation in SiC devices. When high density dangling bond is formed at SiO$_2$/SiC interface, some of electrons in current are trapped there. The trapped electrons cause coulomb scattering by repulsive force against other electrons. This phenomenon interrupts current flow and

degrades electron mobility. Furthermore, that occurs more frequently with higher D_{it}. For low D_{it} and high electron mobility, various interface engineering techniques have been introduced.
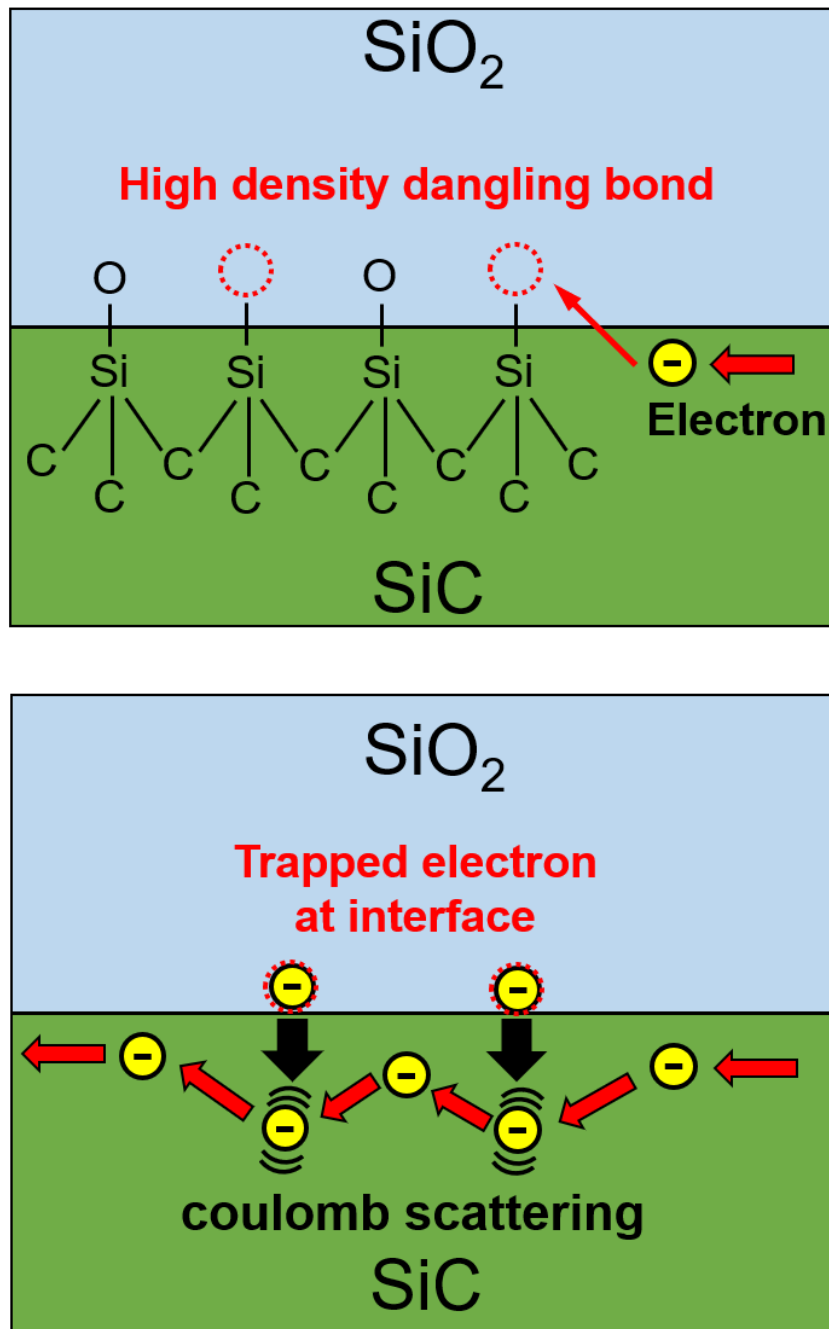
Fig 1.2.1.2 Schematic illustration of electron mobility degradation at SiO_2/SiC interface.

First, interface nitrogen atom passivation by nitric oxide (NO) or nitrous oxide (N_2O) has been commonly performed, which improves the peak mobility up to 40 cm^2/Vs with D_{it} reduction. [1-23~25] By N passivation to SiO_2/SiC interface, dangling bond of Si or C atoms are terminated and carbon residues are also removed by oxygen decomposed from NO or N_2O. Schematic mechanism is shown in Fig. 1.2.1.3.
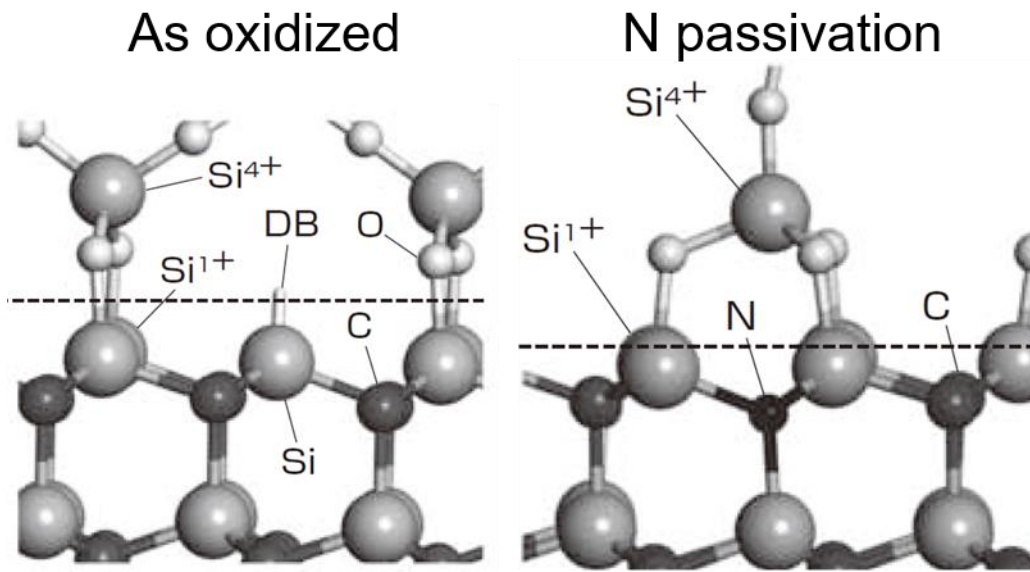
Fig 1.2.1.3 SiO_2/SiC interface before and after N passivation. [1-26]

Besides, various foreign atom incorporations have also been investigated to further improve the mobility. P atoms incorporation by $POCl_3$ annealing into the SiO_2 layer is reported to achieve a high peak mobility of 89 cm^2/Vs. [1-27~29] Although P atoms are not passivated at interface but almost distributed in SiO_2 layer, which reduces D_{it} more than NO annealing. For this D_{it} reduction, interface strain reduction has been expected as a reason. On the other hand, Ba atoms induced oxidation process recovers the peak mobility up to 85 cm^2/Vs by increase of mobile free carriers. [1-30, 1-31] These results

also show low D_{it} values, which is achieved by different mechanism from conventional oxidation process. In addition, a high peak mobility of 134 cm^2/Vs was reported with an La-silicate interface layer accompanied by the nitrogen passivation process. [1-32~34] For interface engineering, gate dielectrics other than SiO$_2$ also have potential.

1.2.2 Negative threshold voltage shift

Although the reduction in the D_{it} can improve the mobility, a negative threshold voltage (V_{th}) shift has been observed after positive bias. The negative V_{th} shift after NO annealing is shown in Fig. 1.2.2.1. Decreasing V_{th} corresponds to the reduction of negative effective charge in the oxide or at the interface for both passivated and un-passivated devices. In addition, more severe shifts have been observed. The examples of P and Ba incorporated MOSFETs are shown in Fig. 1.2.2.2 and 1.2.2.3, respectively. It seems to be related with reduction of interface trap and negative fixed charge, however, a V_{th} close to 0 V is cannot be explained with only that.
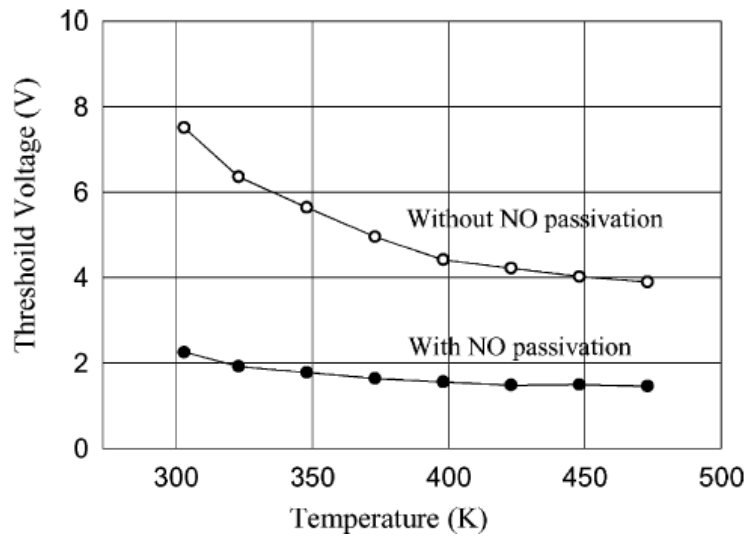
Fig. 1.2.2.1 Temperature dependence of threshold voltage with and without NO passivation. [1-35]

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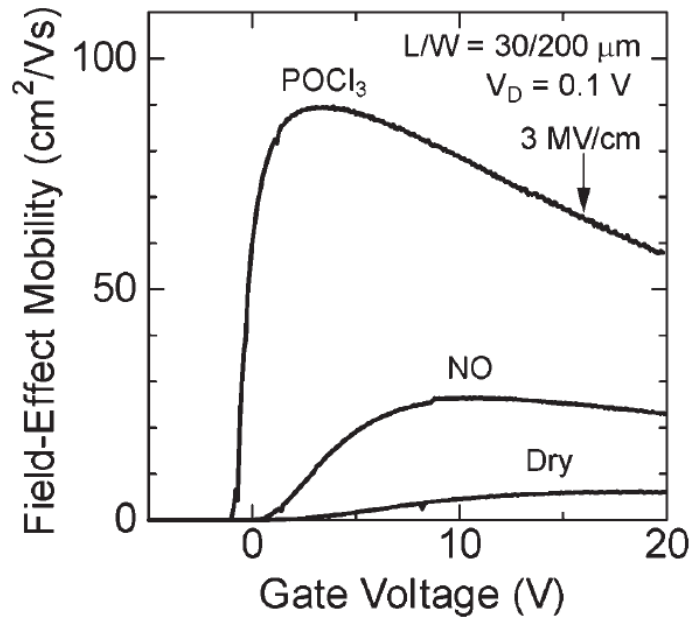
Fig. 1.2.2.2 Field-effect mobility of 4H-SiC MOSFETs fabricated on the Si face by dry oxidation, NO annealing, and the POCl₃ annealing at 1000°C. [1-36]
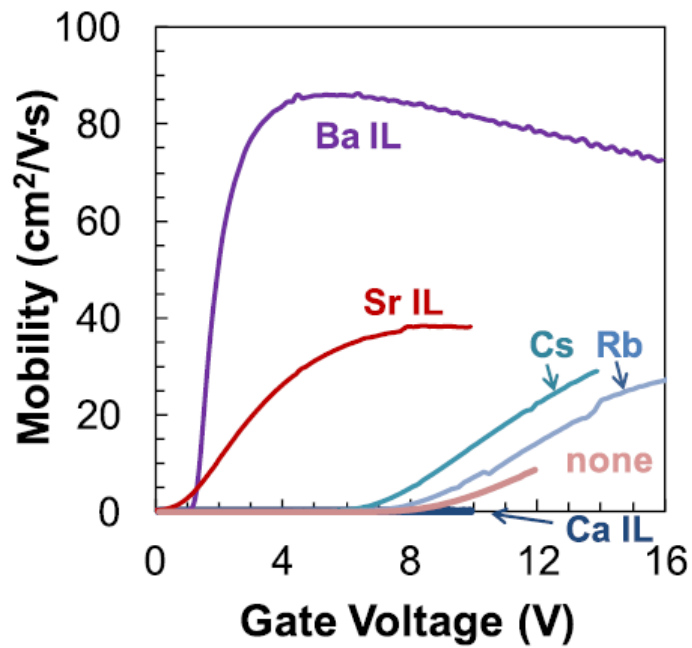
Fig. 1.2.2.3 Field-effect mobility from I_d-V_g transfer characteristics for MOSFETs processed with Rb, Cs, Ca, Sr, or Ba interface layers, compared to an un-passivated thermal oxide (labeled "none"). [1-37]

On the other hand, lanthanum silicate (La-silicate) interface layer shows a high mobility of 134 cm^2/Vs with a relatively high V_{th} of 3 V. [1-32] Fig 1.2.2.4 shows the I_d-V_g characteristics with La-silicate interface layer. Although the D_{it} at the interface between the La-silicate interface layer and the SiC surface is not low enough (over 10^{12} $cm^{-2}eV^{-1}$), rare earth silicate interface layer seems to a promising interface layer for recovering the mobility while keeping the high V_{th}.

The relationship between peak mobility and V_{th} of reported MOSFET is shown in Fig. 1.2.2.5. After dry oxidation without interface treatment, the peak mobility stays at poor value of lower than 10 cm^2/Vs. NO_x gas annealing is added after dry oxidation, the peak mobility is increased to 28 cm^2/Vs. However, the mobility increase accompanies the sacrifice of V_{th}. The V_{th} decreases with the increase of annealing time. Similarly, interface treatment by PSG also leads to a high mobility of 80 cm^2/Vs, V_{th} shifts to negative direction. However, a high peak mobility of 134 cm^2/Vs is achieved by La-silicate interface layer without significant V_{th} decrease. As mentioned above, the La-silicate interface layer showed the high D_{it} over 10^{12} $cm^{-2}eV^{-1}$. Nevertheless, the superior electric properties of rare earth silicate interface layer are attractive for SiC devices.
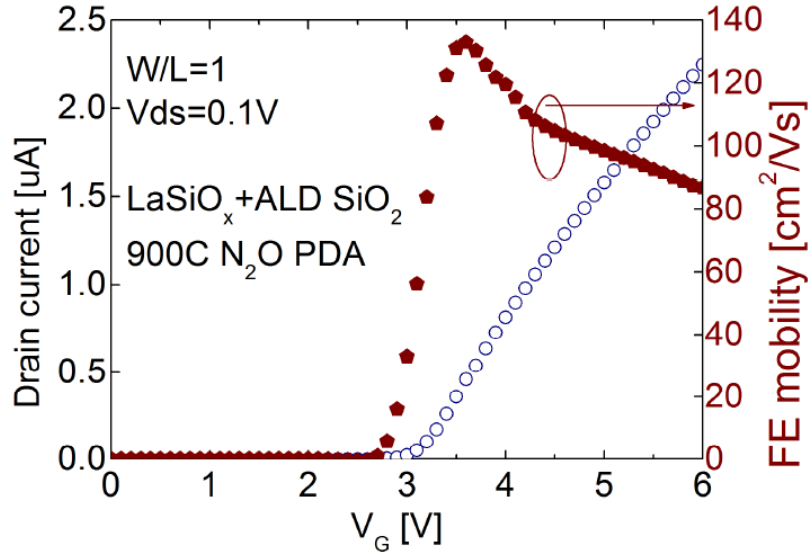
Fig. 1.2.2.4 I_d-V_g characteristics of LaSiO$_x$/30 nm SiO$_2$ MOSFET after 900 °C N$_2$O PDA.

[1-32]
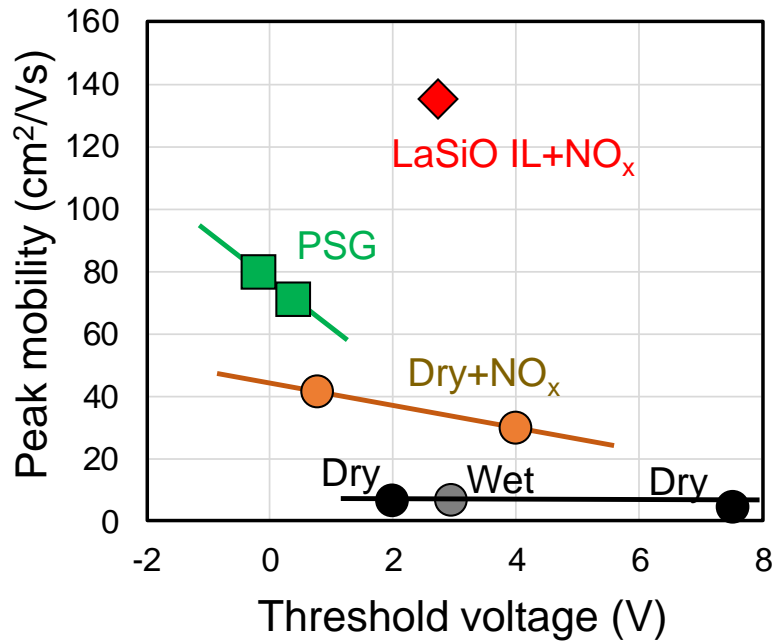
Fig. 1.2.2.5 Reported peak electron mobility with V_{th} of SiC MOSFETs. Each reported data is PSG [1-29], LaSiO [1-32], Dry/Wet [1-38] and NO$_x$ [1-23], respectively. The channel doping is of the order of 10^{16}/cm^3.

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1.3 Material selection for interface layer

1.3.1 Inhibition of surface oxidation

Commonly, rare earth silicate or aluminosilicate glasses have been utilized to promote liquid-phase SiC-based ceramics due to low reactivity to the SiC compounds. Also, among rare earth silicates, yttrium silicate (Y-silicate) has been used as an anti-oxidation coating to SiC compounds because of its equivalent thermal expansion coefficient to the SiC. Fig 1.3.1.1 shows the isothermal oxidation curves of SiC–C/C and SiC/Si–Y_2O_3 coated C/C at 1773 K. Y-silicate coating is effective for anti-oxidation, which leads to reduction of weight loss of SiC. Similarly, the anti-oxidation effect of $Y_2Si_2O_7$ is also clearly known by mass change as shown in Fig. 1.3.1.2.

To investigate an anti-oxidation effect for SiC MOS devices, a Y-silicate layer inhibiting the SiC surface oxidation will be deposited as a gate dielectric on SiC substrates, and electrical characteristics will be also evaluated.
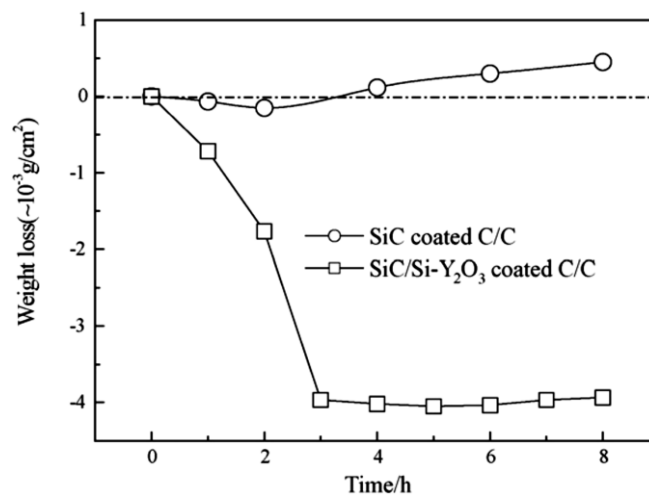
Fig. 1.3.1.1 Isothermal oxidation curves of SiC–C/C and SiC/Si–Y_2O_3 coated C/C at 1773 K. [1-39]
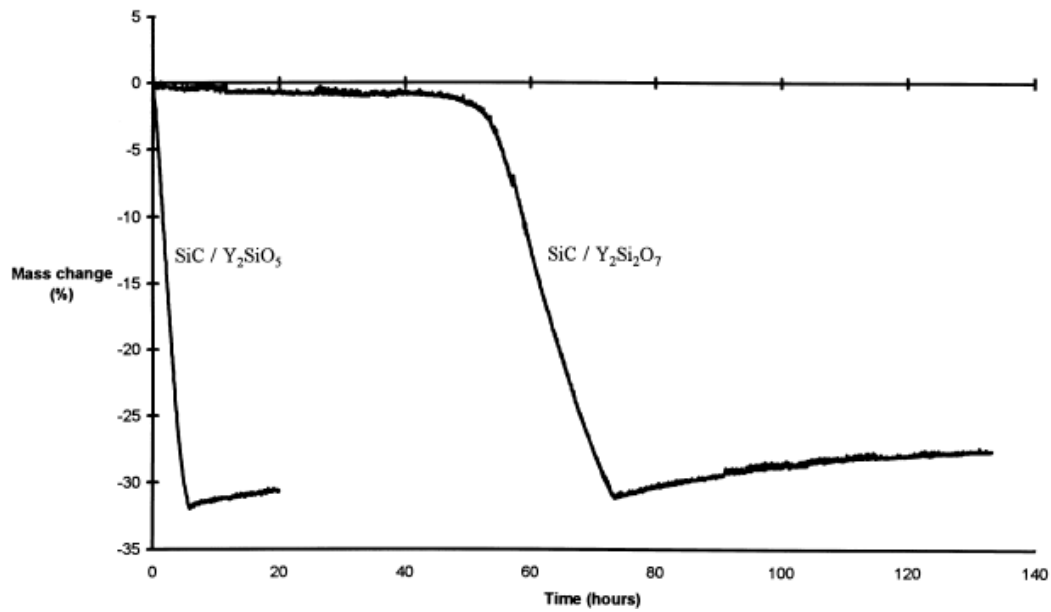
Fig. 1.3.1.2 Isothermal oxidation behaviour of C/SiC with coatings based on Y-silicate at 1600 °C. [1-40]

1.3.2 Surface oxidation by radical oxygen atoms

Among rare earth oxides, CeO_x is known to promote oxidation of adjacent materials by producing radical oxygen atoms. For instance, an interface SiO_2 layer is formed after annealing the CeO_x/Si structure. The interface layer formation is triggered by the supply of oxygen atoms to change the valence number of Ce atoms during the reaction. Although 4H-SiC surface is less reactive to oxygen atoms than Si surface, one can still expect the formation of the interface SiO_2 layer. Since the reaction is based on oxygen radicals, the interface structure might be different from those created by thermally grown SiO_2. Therefore, in this thesis, the effect of CeO_x layer on SiC substrates will be investigated.

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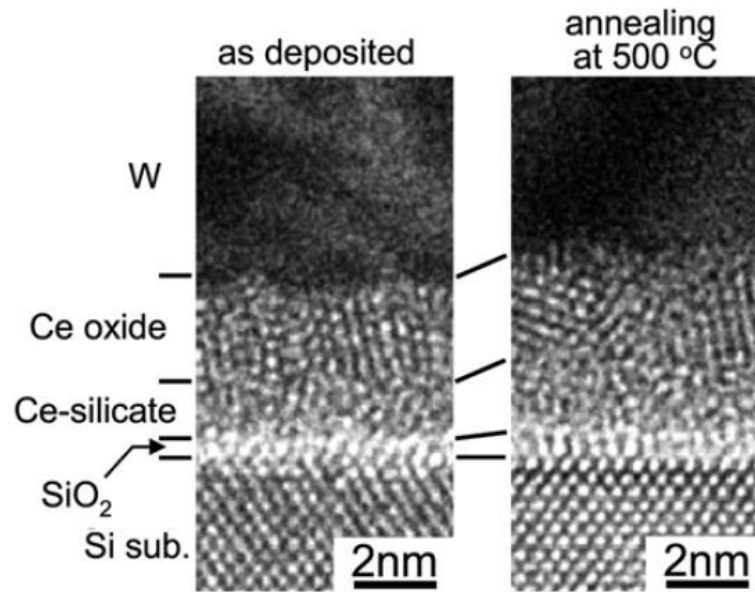
Fig. 1.3.2.1 Cross sectional TEM of W/CeO$_x$/Si before and after 500°C annealing. [1-41]

1.4 Purpose of this study

As the thermally grown interface structure seems to be origin of the degradation in mobility and the negative shift in the V_{th}, complete inhibition of the surface SiC oxidation or different surface SiC oxidizing process might be used to solve the problem. As coating with Y-silicate is known to protect the SiC surface from oxidation, the initial suface can be preserved during the gate stack formation. On the other hand, CeO$_x$ is known to oxidize the surface by means of radical oxygen species, expecting different type of interface structure. The purpose of this thesis is to elucidate the effect of Y-silicate and CeO$_x$ gate dielectrics for SiC MOS capacitors and MOSFET.

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Chapter 2 Fabrication and characterization methods

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2 Fabrication and characterization method

2.1 Experiment procedure

2.1.1 Surface cleaning

A substrate before pretreatment basically has inorganic pollution such as metal and nature oxide film, organic pollution and so on. Sulfuric acid-Hydrogen Peroxide Mixture (SPM) treatment, using piranha solution which is a mixture of sulfuric acid (H_2SO4) and hydrogen peroxide (H_2O_2), is effective for removing organic residue on substrate surface. It will also hydroxylate the substrate surface, making the substrate highly hydrophilic. Hydrofluoric acid (HF) treatment is another pretreatment process for removing inorganic pollutions on substrate. Due to the strong acid property, a hydrofluoric acid can remove most metal residues and oxides on substrate. HF treatment are often performed after SPM treatment. In this study, the solution radio of H_2SO_4 and H_2O_2 was set to 3:1 and fresh solution heating up to 180^oC was used. Samples were treated in H_2SO_4/H_2O_2 solution for 10 min to remove organic pollutions. After SPM treatment, samples were set into 20% HF for 2 min to remove residue particle and metal contamination.

2.1.2 Atomic layer deposition (ALD)

In this study, all gate dielectrics are deposited by ALD process. ALD is a film deposition method by precise film thickness control. A type of precursor is different depending on the target film, and the film grows on the substrate by oxidizing it. The precursor molecules react with surface of substrate, but reaction between precursor molecules is limited by self-limiting characteristic. Consequently, the maximum film thickness deposited on the surface after a single exposure to is determined by the nature of the precursor-surface interaction. [2-1] Using this characteristic, target film thickness

can be achieved by cyclic pulse process.

Figure 2.1.2.1 illustrated the example of basic cycling process for deposition of ALD-SiO$_2$, Firstly, precursor is injected to the reaction chamber and coating the material. After then, any excess is removed by Ar purge. O$_2$ plasma is radiated and reacts with precursor to create another layer on the surface. After reaction between the precursor and O$_2$ plasma, excess O$_2$ is removed by Ar purge again and this process is repeated until target thickness is deposited. Y$_2$O$_3$ and CeO$_x$ layer are also deposited by same principle with SiO$_2$.
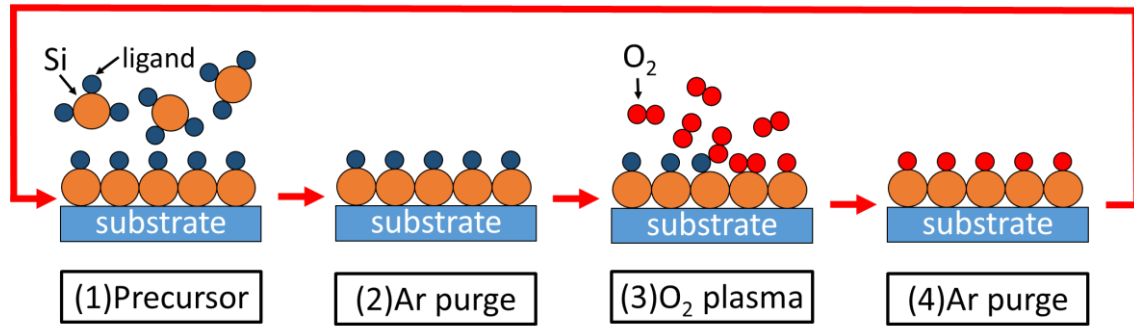
Fig 2.1.2.1 schematic illustration of atomic layer deposition process.

2.1.3 Post-deposition annealing (PDA)

Deposited gate dielectrics are annealed with a lamp annealer. That process is called post-deposition annealing (PDA) for improvement of dielectric property. The samples are heated by light focusing from source. Also, oxidation of SiC substrates for standard samples is also performed in this annealer. A SiC susceptor in the annealer can endure in high temperature, thus high temperature annealing over 1000ºC is available. The temperature curve in annealing process is shown in Fig 2.1.3.1. In this study, ranges of PDA temperature and time are from 900ºC to 1200ºC and from 30 min to 90 min, respectively.
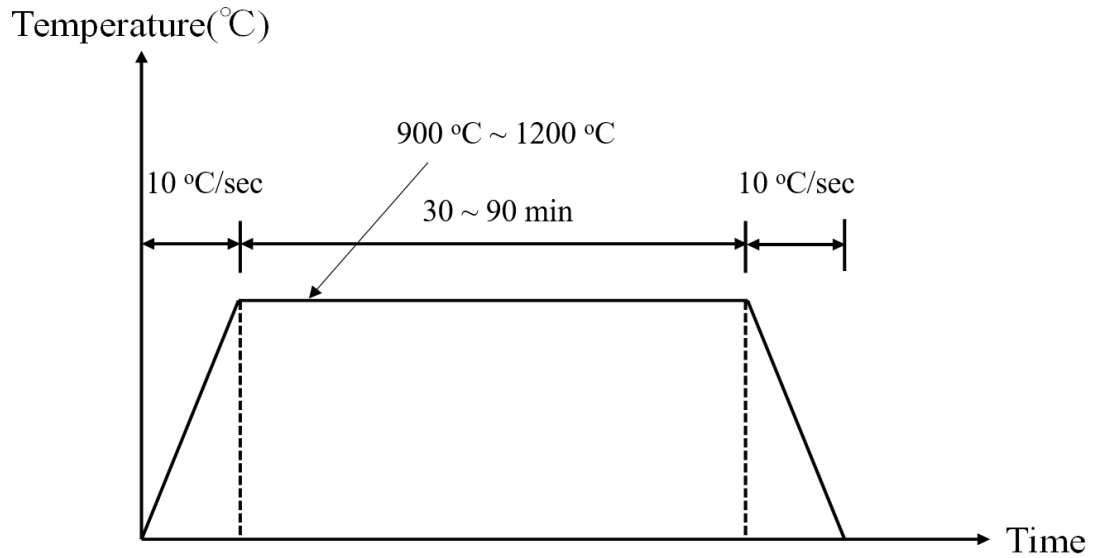
Fig 2.1.3.1 Temperature curve in PDA process.

2.1.4 RF magnetron sputtering

Deposition of gate and source/drain (S/D) electrodes are conducted by radio frequency (RF) magnetron sputtering. The illustration of RF magnetron sputtering is shown in Fig 2.1.4.1. Ar gas flow into the chamber, and a high electric field is applied between substrate and target. Ionized Ar atoms hit the target, and then target atoms are emitted. Emitted target atoms fly through the vacuum chamber and deposited on the substrate. W gate and Ni S/D electrodes were deposited with RF power of 150 W in Ar ambient. In case of TiN deposition, N_2 gas was also added to chamber for nitridation of target. Deposition rate of nitride is low for collision of Ar and N_2 atoms, thus a RF power was set to 300 W.
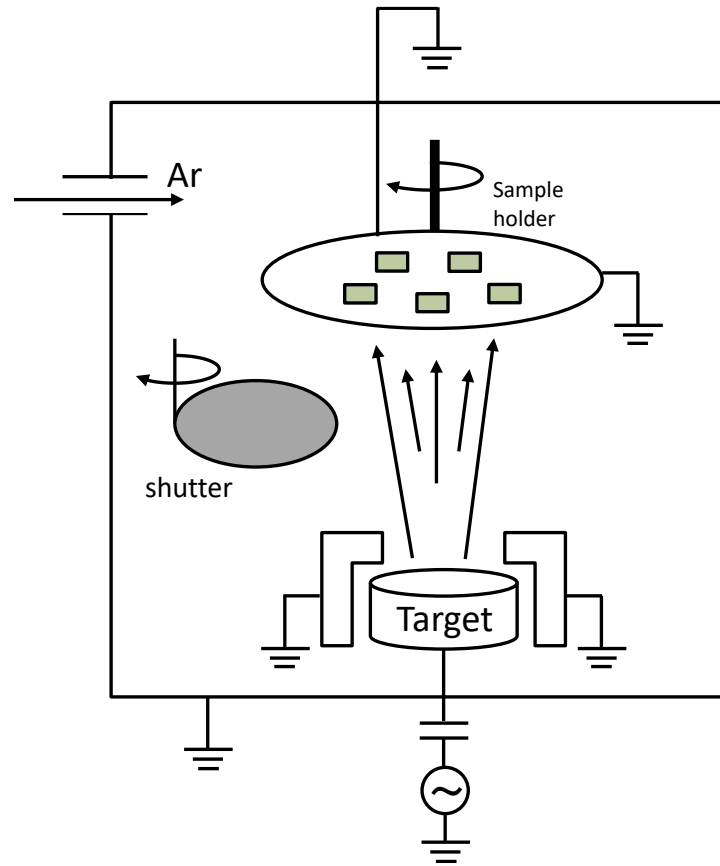
Fig 2.1.4.1 Schematic illustration of RF magnetron sputtering

2.1.5 Photolithography

To patterning the samples, photolithograph process is utilized. First, positive photoresist was coated on the samples by spin coating. Rotation per minute (RPM) was set to 3000 per minute. Then the samples were heated to 115°C to drive off excess moisture in the photoresist, which is so called pre-baking process. Next, the coated samples were aligned and exposed with photomask and ultraviolet (UV). After that, exposed area was developed by dipping in developer. Finally, the samples were treated by post-baking process to solidify the remaining photoresist for the following plasma etching. The processes of photolithography are illustrated in Fig. 2.1.5.1.
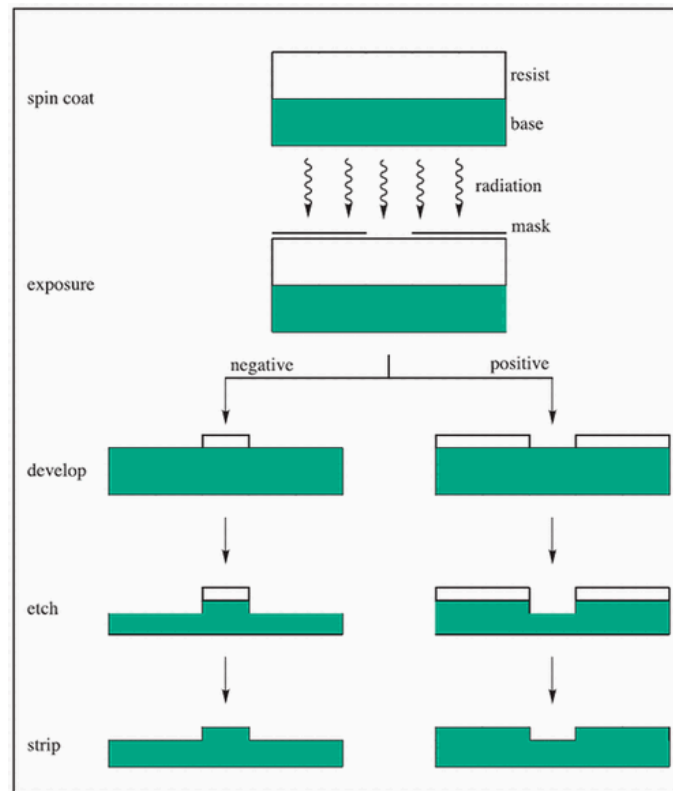
Fig 2.1.5.1 Schematic illustration of the photolithography process. [2-2]

2.1.6 Reactive ion etching (RIE)

  RIE is plasma etching technology for realizing nano or micro-patterning. Figure 2.1.6.1 is schematic illustration of RIE process. In this study, this process is used for isolation of sputtered W and TiN films for gate electrodes. Plasma is generated by applying RF power, after then, etching gas ions move to substrate by applying DC power. The etching gas ions conflict with material of substrate, which is removed by sputtering and chemical reaction. For device reliability, isolation of gate electrodes was performed by slightly over etching than standard condition.
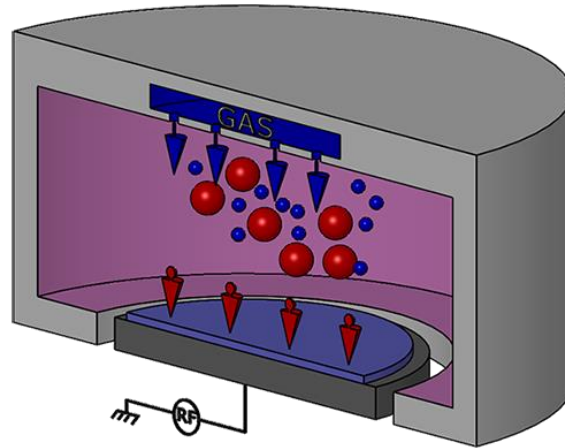
Figure 2.1.6.1 Schematic illustration of RIE process. [2-3]

2.1.7 Post-metallization annealing (PMA)

Post-metallization annealing (PMA) is a thermal treatment conducted by rapid thermal annealing (RTA). After formation of gate and S/D electrodes, the samples were annealed to improve contact property. The temperature curve in annealing process is shown in Fig 2.1.7.1. A rapid heating rates was obtained by high intensity lamps. In this study, annealing temperature of 950°C was used with forming gas (F.G).
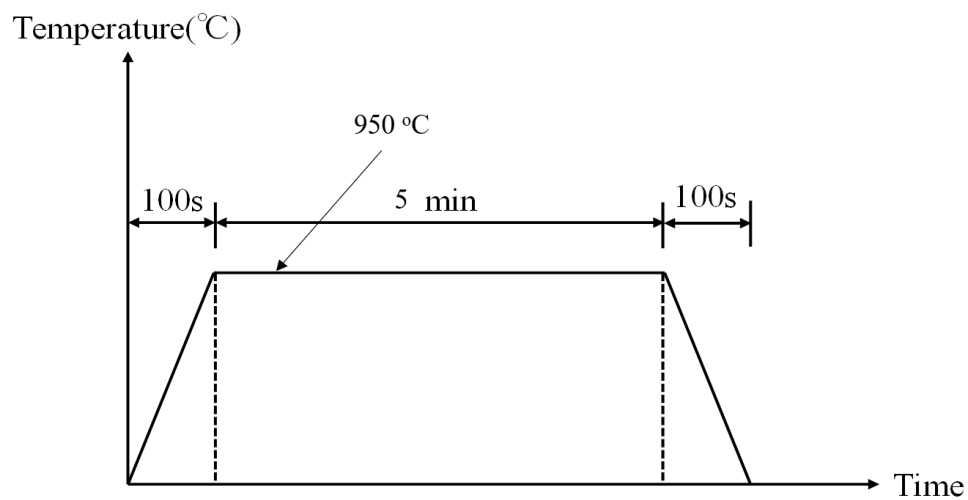
Fig 2.1.7.1 Temperature curve in PMA process.

2.2 Device fabrication

2.2.1 Fabrication procedure for *n*-MOS capacitors

4H-SiC MOS capacitors were fabricated on a Si-face (0001) n-type (N_D=5×10^{15} cm^{-3}) 4° off-axis epitaxial layer. The samples were chemically cleaned by H_2SO_4 and H_2O_2 mixture (SPM) solutions, followed by chemical oxide removal by HF (20%) dipping for 1 min. Gate dielectric layers of Y-silicate (0.6~40 nm), CeO_x, (1 nm) and SiO_2 (40 nm) were deposited by atomic layer deposition (ALD) process at a substrate temperature of 200°C using oxygen remote plasma and precursors; Y(^{i}PrCp)$_3$, Ce(^{i}EtCp)$_3$, and SiH[N(CH$_3$)$_2$]$_3$, respectively. To secure the deposition coverage of the Y_2O_3 and the CeO_x layers, a multi-shot deposition process was utilized. [2-4] A detail of Y-silicate layer deposition will be introduced in chapter 3.4. The samples were then post-deposition annealed (PDA) in either N_2 or NO ambient at various temperatures from 900°C to 1200°C for 30 min and 90 min. A standard sample with thermal oxidation formed by 1200°C (~34 nm), followed by post oxidation annealing (POA) in NO:N_2=20%:80% gas at 1200°C, was fabricated. 50-nm-thick W gate electrodes were deposited by RF sputtering with a 40-nm-thick TiN capping layer to protect the surface against oxidation. The metal layers were patterned by reactive ion etching (RIE) with Cl_2 and Ar chemistries. Finally, 50-nm-thick Ni contact layers were deposited on the backside of the samples by RF sputtering. The capacitors were then post-metallization annealed (PMA) at 950°C in F.G (N_2: H_2=97 %:3 %) ambient for 5 min. The fabrication flow of MOS capacitors is shown in Fig. 2.2.1.1.

n-MOS capacitor (0001)

○ SPM,HF cleaning

○ Y-silicate (0.6~40 nm), CeO$_x$ (1 nm), SiO$_2$ (40 nm) deposition by ALD
Oxidation at 1200°C in O$_2$ for 150 min

○ PDA or POA in N$_2$ or NO ambient
(PDA:900~1200°C for 30, 90 min in N$_2$ or NO)
(POA:1200°C for 90 min in NO)

○ Sputter-W (50 nm),TiN (40 nm) deposition

○ Patterning by RIE

○ Ni (50 nm) back contact deposition

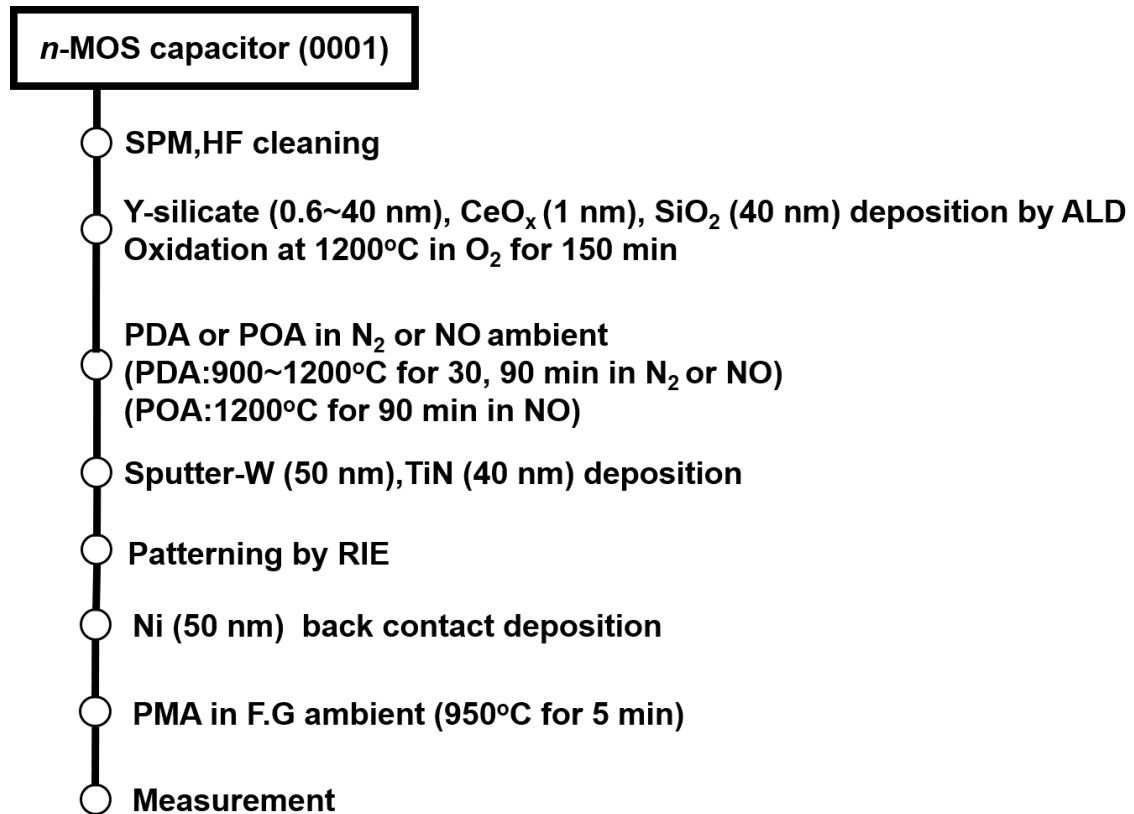○ PMA in F.G ambient (950°C for 5 min)

○ Measurement

Fig 2.2.1.1 Fabrication flow of SiC MOS capacitors.

2.2.2 Fabrication procedure for *n*-MOSFETs

Planar 4H-SiC MOSFETs were fabricated on a Si-face (0001) p-type (N_A=2×10^{15} cm^{-3}) 4° off-axis epitaxial layer. The same structure of gate dielectrics with the capacitors were deposited by ALD. PDA was performed at from 900°C to 1100°C for 30 min, and POA condition is same to capacitors. TiN/W layers were deposited for gate electrodes. After gate patterning, PMA was performed at 950°C for 5 min in F.G ambient for removal of carbon residue in dielectrics by oxygen diffusion from W. Ni was used for S/D contact, and it was annealed at 950°C for 2 min to obtain ohmic property. The fabrication flow of MOSFETs is shown in Fig. 2.2.2.1.

_n_-MOSFET (0001)

○ **SPM,HF cleaning**

○ **Y-silicate (0.6 nm), CeO$_x$ (1 nm), SiO$_2$ (40 nm) deposition by ALD**
  Oxidation at 1200°C in O$_2$ for 150 min

○ **PDA or POA in N$_2$ or NO ambient**
  (PDA:900~1100°C for 30 min in N$_2$)
  (POA:1200°C for 90 min in NO)

○ **Sputter-W (50 nm),TiN (40 nm) deposition**

○ **Patterning by RIE**

○ **PMA in F.G ambient (950°C for 5 min)**

○ **Ni (50 nm) S/D contact deposition**

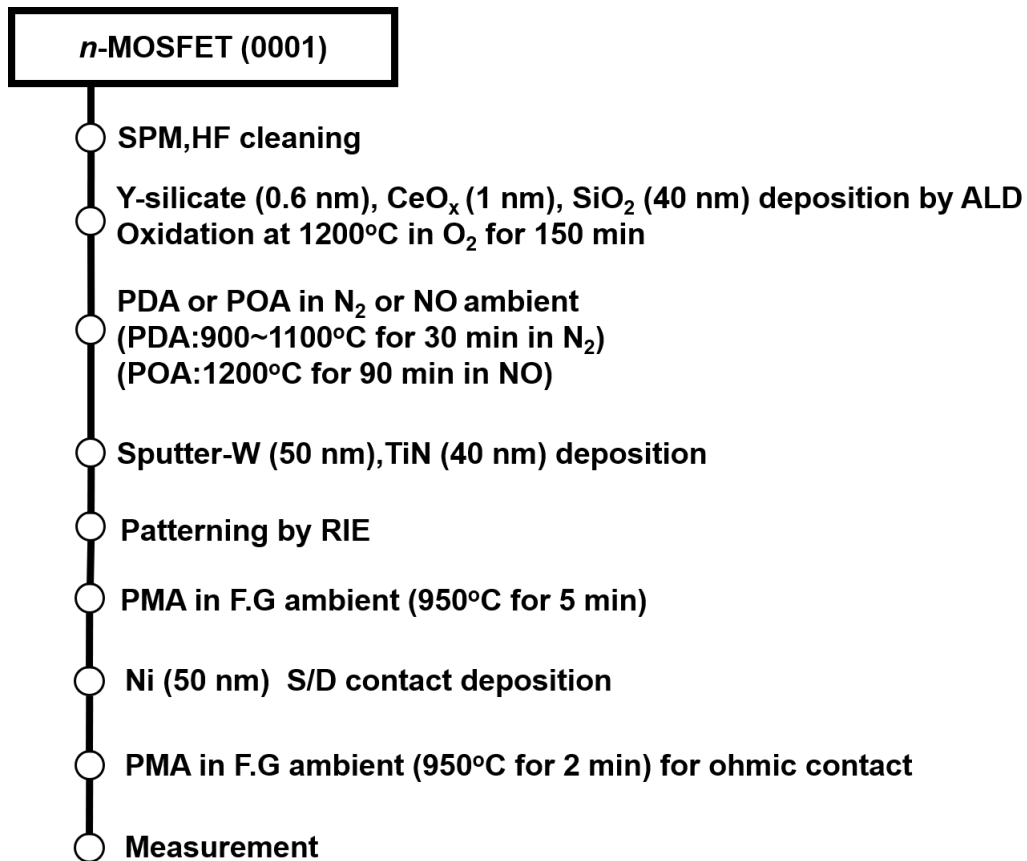○ **PMA in F.G ambient (950°C for 2 min) for ohmic contact**

○ **Measurement**

Fig 2.2.2.1 Fabrication flow of SiC MOSFETs.

2.3 Characterization method

2.3.1 Capacitance-Voltage (C-V) measurement

Capacitance-Voltage (*C-V*) characteristic measurements were performed with frequency of 500 kHz by precision LCR (E4980A, Agilent). The measurement of capacitance was conducted by contact with gate electrode and back electrode of capacitors. The range of measurement voltage was set from -5 V to 10 V for all capacitors. Also, measurement frequency was set to 500 kHz. From measured *C-V* characteristics, various information of devices can be extracted such as interface property, doping concentration and so on. Fig. 2.3.1.1 shows the schematic *C-V* curves.
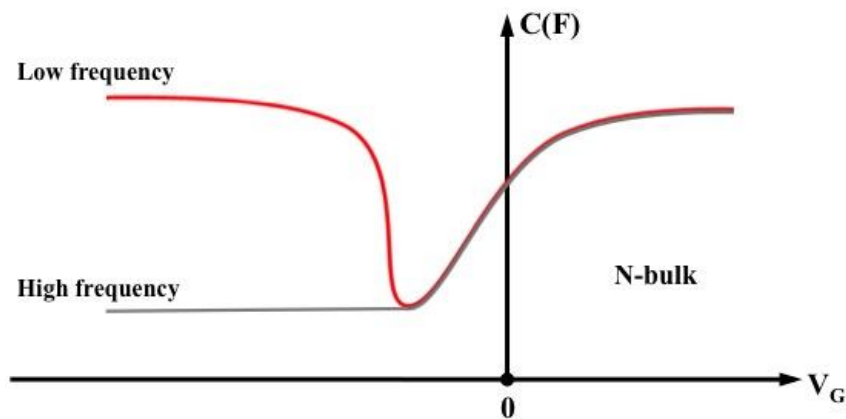

Fig 2.3.1.1 Schematic *C-V* curves in low and high frequency.

2.3.2 Interface state density (D_{it}) by conductance method

The conductance method is one of the methods to determine interface state density (D_{it}). Interface trap capture and emission of carriers can be evaluated by $D_{it.}$

The simplified equivalent circuit of MOS-capacitor applied with the conductance method is shown in Fig. 2.3.2.1 (a). where C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance. Also, where C_{it} and R_{it} are the interface trap capacitance and the interface trap resistance, respectively. The circuit can be simplified to the circuit in Fig. 2.3.2.1 (b), where C_P and G_P are given by [2-5]:

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.1}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.2}$$

Here, D_{it} is determined by maximum G_p/ω, which relationship is expressed by [2-5]:

$$D_{it} = \frac{2.5}{q}(\frac{G_p}{\omega})_{max} \tag{2.3}$$

Measured capacitance and conductance consist of the parallel combination as shown in Fig. 2.3.2.1 (c). G_p/ω can be converted into an equation based on the measured parameters, which is expressed by [2-5]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox}-C_m)^2} \tag{2.4}$$

From this equation, G_p/ω can be obtained by measurement, and D_{it} is also can be calculated.
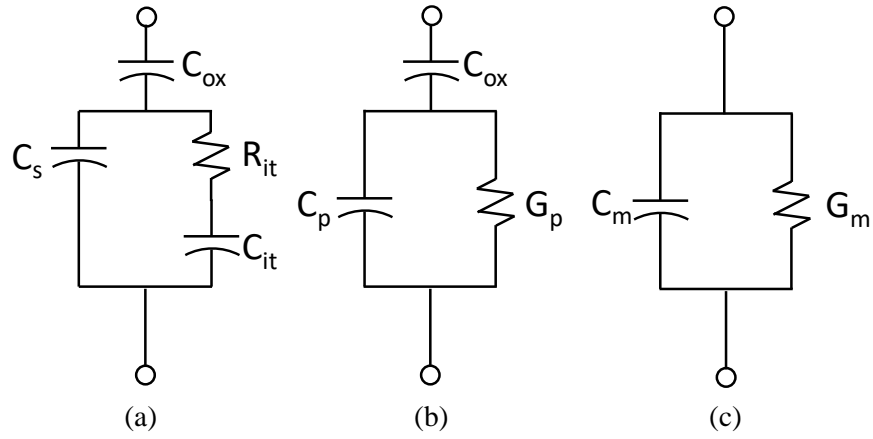
Fig. 2.3.2.1 Equivalent circuits for conductance measurements; (a) MOS-Capacitor with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, [2-5].

2.3.3 Pulse measurement for I_d-V_g characteristics

  In this study, pulse measurement is performed to the drain current (I_d) on gate voltage (V_g) characteristics, I_d-V_g, for MOSFETs instead of DC measurement. This is to minimize the effect carrier trapping to generate the hysteresis in the sweeping measurement and to extract the real mobility obtained by the fabricated interface. Fig. 2.3.3.1 shows the fundamental characteristics of DC and pulse measurements.
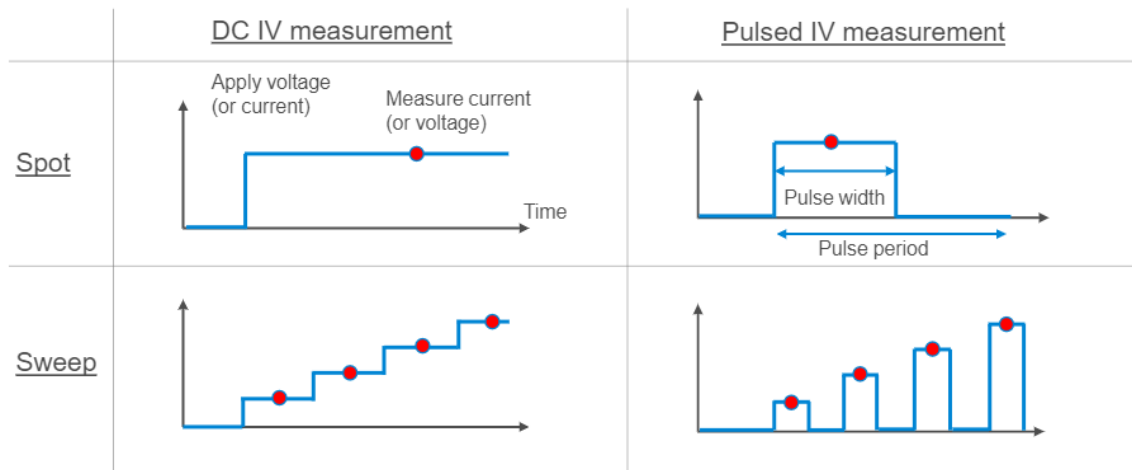

Fig. 2.3.2.1 Fundamental characteristics of DC and pulse measurements.

2.3.4 Effective channel length extraction

A Gate channel length is an important parameter for analysis of MOS capacitor and MOSFET properties. However, that can fluctuate in patterning process from designed length. Therefore, an effective channel length is need to be extracted for accurate evaluation. By Terada method, measured entire channel resistance is expressed by [2-6]

$$R = R_o + (\rho/W)(L_m + \Delta L) \tag{2.5}$$

Where R_o is extrinsic resistance, ρ is channel sheet resistance, W is channel width, L_m is designed channel length and ΔL is the difference between L_{eff} of effective channel length and L_m.

Terada plot for effective channel length is shown in Fig. 2.3.4.1. This measurement was performed in SiC MOSFET with thermally grown SiO_2 dielectric. ΔL was estimated to be 0.28 μm.
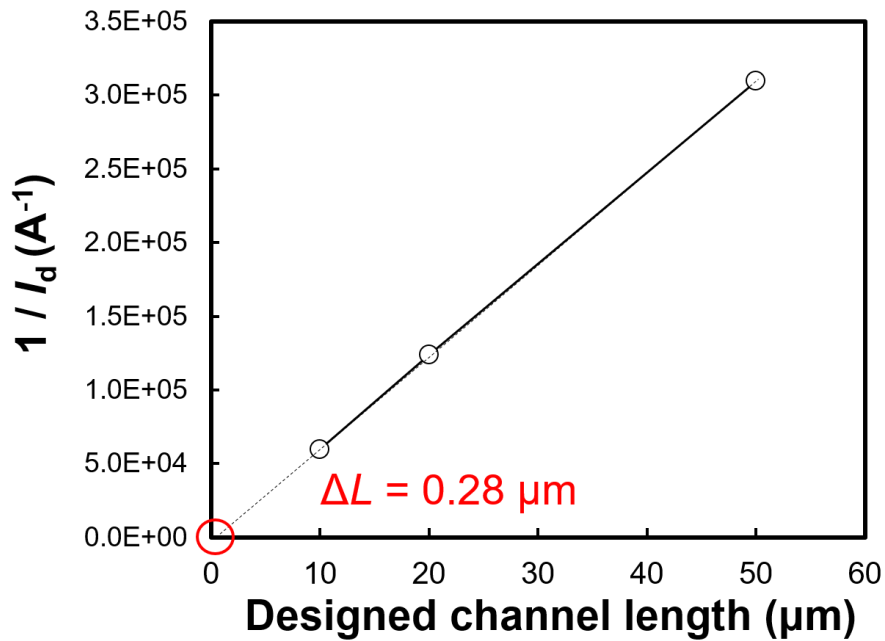

Fig. 2.3.4.1 Terada plot at designed channel length of 10, 20 and 50 μm.

2.3.5 Field effect mobility extraction

When the transistor is operated in the linear region, where V_{ds} is small and I_d increase proportional with V_{ds}. The field-effect mobility is determined from the transconductance, defined by:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \ (V_{ds} = constant) \tag{2.6}$$

Where I_d is the drain current, V_{gs} is the bias voltage between gate and source of MOSFET, and V_{ds} is the bias voltage between drain and source. The drift component of the drain current with $Q_n = C_{ox}(V_{gs} - V_{th})$ is:

$$I_d = \frac{W}{L} \mu_{FE} C_{ox}(V_{gs} - V_{th})V_{ds} \tag{2.7}$$

When the field-effect mobility is determined, the transconductance can be given as:

$$g_m = \frac{W}{L} \mu_{FE} C_{ox} V_{ds} \tag{2.8}$$

Where W and L are the width and length of the channel, C_{ox} is the capacitance of gate insulator. When this equation is solved for the mobility, it is known as the field-effect mobility:

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{ds}} \tag{2.9}$$

In this study, the V_{ds} was control to be 50 mV when measuring the field-effect mobility.

2.3.6 X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is one of the most widely used methods for surface analysis of specimen. When a specimen is irradiated with a soft X-ray corresponding to energy of tens to thousands of eV, electrons are emitted from the core level or valence level. At this time, the emitted electrons are called photoelectron. In order that photoelectrons to be emitted, kinetic energy more than binding energy and work function is required. Since the measured binding energy is the intrinsic energy of the element, the element of the specimen can be analyzed. In addition, the binding energy changes according to the chemical bonding state, information on the chemical bonding state can be obtained. The schematic illustration of XPS measurement is shown in Fig. 2.3.6.1. In this study, XPS measurement was utilized for analysis of Y_2O_3 and CeO_x composition after thermal process.
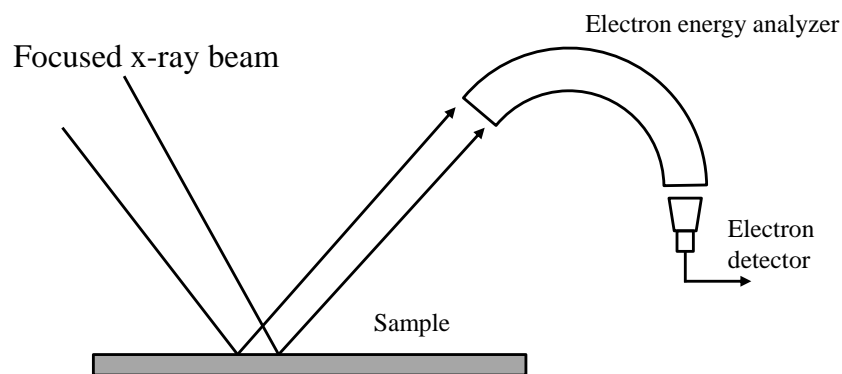

Fig 2.3.6.1 Schematic illustration of XPS measurement.

2.3.7 Transmission electron microscope (TEM)

Transmission electron microscopy (TEM) is a famous method for obtain high resolution image by transmit electron beam through ultra-thin specimen. Fig 2.3.7.1 shows the schematic illustration of TEM. TEM is largely composed of 4 parts, these are electron gun, condenser lens, objective lens and detector. When a potential difference is made from filament to anode, an acceleration voltage is generated, which is generally 60 to 300 kV. The generated electron beam is focused and manipulated by condenser lens, which allows desired size and location for the specimen. The electron beam passed through the specimen is converted into an image through the objective lens and imaging lens. At this time, contrast is formed by difference in scattering electrons. In this study, we observed cross section of MOS devices to confirm formation of Y-silicate or CeO_x gate dielectric by TEM.
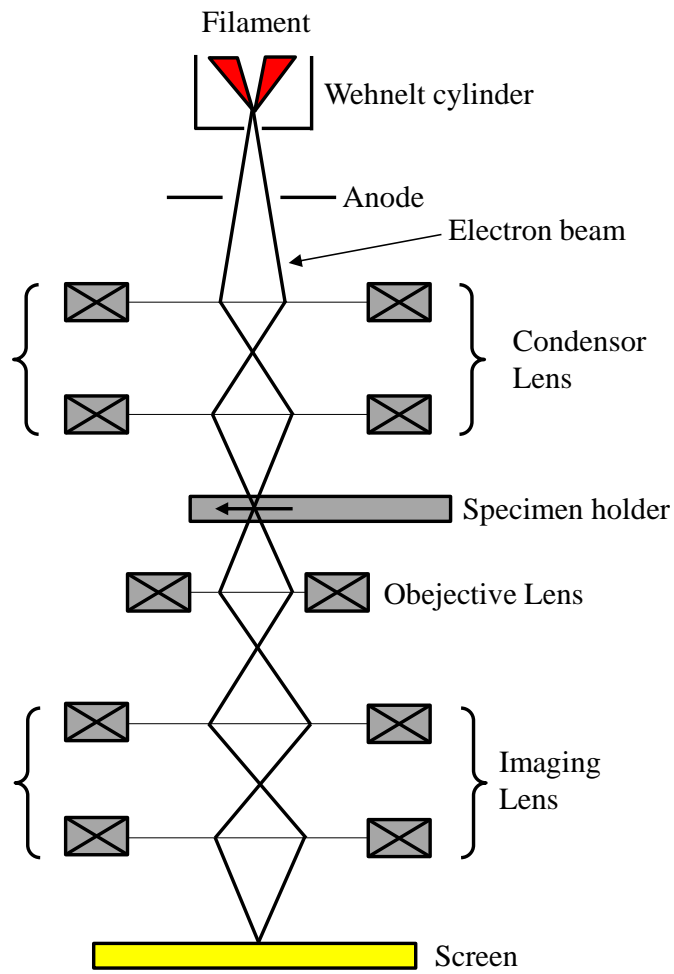
Fig 2.3.7.1 Schematic illustration of TEM device structure.

Reference

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[2-4] J. Song, Y. Lin, T. Hoshii, H. Wakabayashi, K. Tsutsui and K. Kakushima, Jpn. J. Appl. Phys., 59, SMMB01 (2020).

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[2-6] K. Terada and H. Muta, Jpn. J. Appl. Phys., 18, pp. 953-959 (1979).

Chapter 3 Atomic layer deposition by Ar multiple boost injection

3.1 Deposition with low vapor pressure precursors: Y_2O_3 and CeO_x film cases

3.2 A proposal of Ar-boosted multi-shot process

3.3 Film coverage by the number of multi-shot

      3.3.1 Boost time dependency of growth rate

      3.3.2 Effect of precursor multi-shot for growth rate

3.4 Demonstration of Y-silicate deposition

3.5 Summary of chapter 3

Reference

3 Atomic layer deposition by Ar multiple boost injection

With low on-resistance advantage, trench type MOSFET is becoming the mainstream of SiC MOS-structure. However, a strong crystallographic orientation dependent oxidation on 3D-gate structure may result in the formation of an uneven SiO_2 layer, which may pose reliability issues. [3-1] On this point, gate dielectrics formed by conformal deposition processes seem to be prominent ways for replacing the thermally grown SiO_2 ones. ALD has been indicated to be a feasible method to form conformal SiO_2 layer on semiconductor surfaces. [3-2] Also, as the ALD process can be performed at low process temperature, the risk of forming carbon deficiency in the sub-surface SiC channel can be reduced. [3-3] However, several materials of precursor have low vapor pressures, it aggravates film coverages on substrates by low growth per cycle. The film coverage is particularly important for interface property, thus it needs to be improved for reliability of devices.

In this chapter, effect of Ar-boosted precursor multi-shot to film coverage for Y_2O_3 and CeO_x will be introduced. Additionally, properties of Y_2O_3 and Y-silicate films deposited by multi-shot process will be also presented.

3.1 Deposition with low vapor pressure precursors: Y_2O_3 and CeO_x film cases

Y_2O_3 thin films have wide applications owing to its material properties; a relatively wide bandgap of 5.5 eV, a high relative permittivity of $\simeq 15$, and a high refractive index of 1.8. Also, the Gibbs free energy of Y_2O_3 is negatively largest among rare earth oxides, suggesting a stable film property against oxygen vacancy formation. [3-4] Y_2O_3 thin films can be deposited by various physical vapor depositions (PVD) [3-5,3-6] or chemical vapor depositions (CVD) [3-7,3-8]. With the advent of recent ALD to deposit conformal and pinhole-free thin films, many works have been reported to form Y_2O_3 films by the ALD method. With this method, a wide range of applications using ALD-Y_2O_3 has been reported so far, including gate dielectrics for semiconductors (GaAs, graphene and so on) [3-9~15], yttria-stabilized zirconia (YSZ) for fuel cell [3-16~18]. Common precursors used for Y_2O_3 thin film deposition are cyclopentane (Cp) based molecules; bis-isopropylcyclpentadienyl-diisopropylacetamidinate yttrium (Y(^{i}PrCp)$_2$(N-^{i}Pr-amd)) [3-20~22], tris-methylcyclopentadienyl yttirium (Y(MeCp)$_3$) [3-15], tris-ethylcyclopentadienyl yttrium (Y(^{i}EtCp)$_3$) [3-19,3-23], tris-isopropylcyclopentadienyl yttrium Y(^{i}PrCp)$_3$ [3-11,3-24]. For oxidant, either H_2O, ozone or O_2 remote plasma is used to remove the ligands of the precursors and to oxidize the chemisorbed surface Y atoms.

CeO_x has a moderate bandgap of 3.0~3.6 eV and high permittivity of 23~52. CeO_x is known to control the oxygen partial pressure of the adjacent oxide layer by changing the valence number between 3 and 4, and has been applied to control the V_{th} of Si MOS devices [3-25,3-26]. In addition, several CeO_x thin films have also been deposited by ALD with Cp-based precursors.

As Cp-based precursors generally exhibit low vapor pressure, several techniques have been utilized to efficiently deliver the gas into the chamber [3-11~15, 3-19]. One way is the exposure mode, where all the inlet and outlet valves of the chamber are close to confine the precursor in the chamber, allowing the surface reaction within the time of the encapsulation. Another way is to bubble the liquid precursors with an inert carrier gas, allowing efficient precursor carrier into the chamber. The usage efficiency of the precursor of the former method is high, but the time for deposition can be long, which is one of the drawbacks of ALD. On the other hand, the sequence of the latter method is simple and one can easily obtain Y_2O_3 and CeO_x thin films. The growth per cycle (GPC) of Y_2O_3 and CeO_x thin films is reported to be around 0.1 nm/cycle irrespective of any combination of the precursor and the oxidant or deposition method, which is far less than one monolayer of Y_2O_3 and CeO_x molecules. Fig. 3.1.1 and 3.1.2 show the general GPC of the Y_2O_3 and CeO_x thin films.
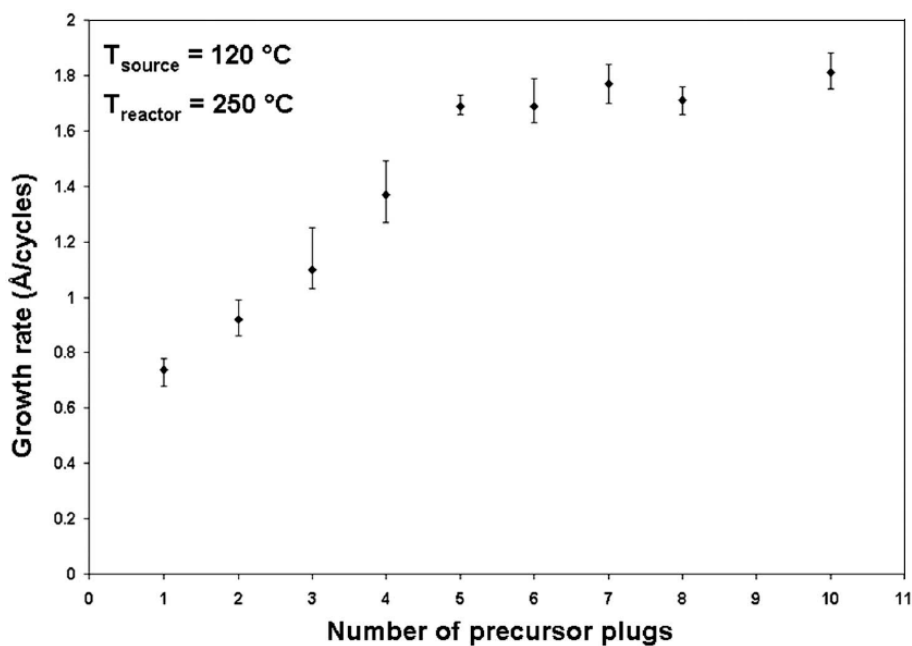

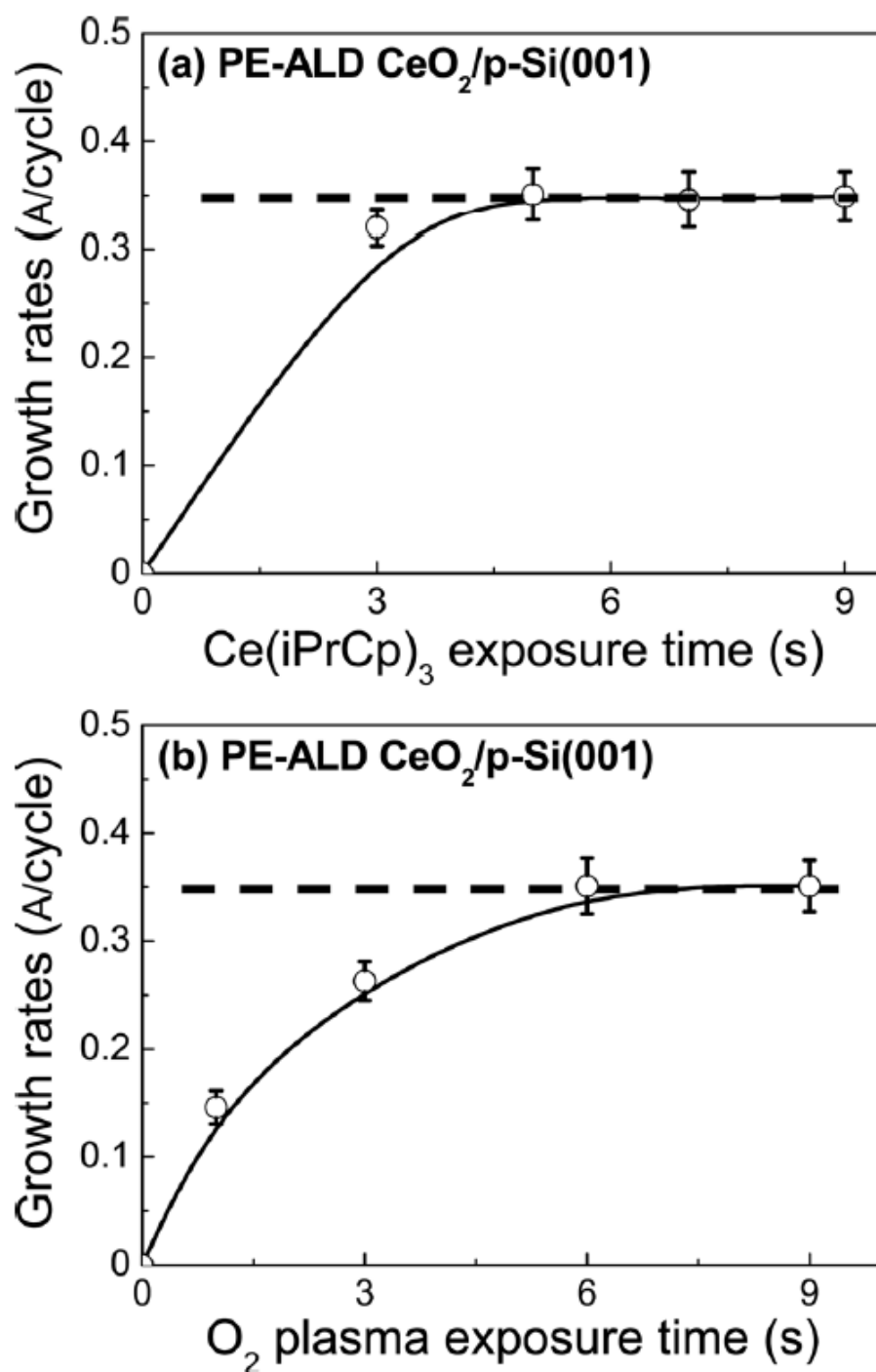Fig. 3.1.1 GPC of Y_2O_3 films with $Y(EtCp)_3$ precursor by H_2O. [3-19]

Fig. 3.1.1 GPC of CeO$_x$ films with Ce(iPrCp)$_3$ precursor by O$_2$ plasma. The temperature of substrate is 250 °C. [3-27]

3.2 A proposal of Ar-boosted multi-shot process

The low GPC values of the Y_2O_3 and CeO_x films were presented above section. The efficiency of the precursor usage might be low if the condition of injection is not optimized. Therefore, we will report a high GPC by using multiple boost injection method.

The precursors and the oxidant are $Y(^iPrCp)_3$, $Ce(^iPrCp)_3$ and remote oxygen plasma, respectively. Fig. 3.2.1 (a) shows the schematic structure of the ALD system used in this study. Three Ar lines, one is to purge the surface of the sample which is directly connected to the chamber, and another is for precursor delivery, and the other one is the boost line, connected to the precursor cylinder for bubbling, is used for the multiple boost injection. All the gas lines were heated to 150 ^{o}C to avoid any condensation of the precursor during the cycle process. The reactor chamber temperature was maintained at 200 ^{o}C which is lower than the decomposition temperature of the precursor. The mass flow rates for Ar purge and precursor delivery lines were 60 and 100 sccm, respectively. During the process, Ar gas through both purge and precursor delivery is supplied, and with the control of conductance of the turbo molecular pump (TMP), the chamber pressure is set to 77 Pa. With this high chamber pressure, one can expect a conformal deposition of the films into trench structures with a high aspect ratio. The cylinder of the precursor was kept at 140 ^{o}C. At this temperature, the vapor pressure of the precursor is less than 20 Pa and this value is lower than the chamber pressure, so one cannot expect any precursor delivery with this setup. The inner pressure of the cylinder can be pressurized slowly by controlling the Ar boost valve (V_{Ar}) in the boost line through a needle valve which is set just after V_{Ar}. After pressurizing the cylinder higher than the chamber pressure, the V_{Ar} is closed, and then the injection valve (V_Y) can introduce the precursors effectively into the chamber. A simple model based on equation (3-1) suggests a high precursor delivery efficiency of

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almost 100 % if the cylinder is pressurized to 0.2 MPa.

$$\eta = 1 - \frac{P_{ch}}{P_Y + P_{Ar}} \tag{3.1}$$

Fig. 3.2.2 (b) shows a typical chamber pressure after injection of the precursor by V_Y for 1 sec. One can see the injection of mixed gas from the cylinder even for a high base pressure (77 Pa) of the chamber. The decay of the pressure was less than 10 s. By repeating the V_{Ar} and V_Y sequence several times before remote oxygen plasma treatment, we can deliver the precursor into the chamber by multiple injections.

For sample preparation, the cleaned Si substrates were set into the chamber for 30 min to reach the temperature of 200°C before deposition. The Ar boost gas was injected into the cylinder first before the precursor is injected into the chamber. With our setup, the cylinder pressure was 0.17 and 0.2 MPa for the V_{Ar} opening time of 1 and 20 s, respectively. After closing V_{Ar} the mixed gas in the pressurized cylinder was released into the chamber by opening the V_Y. The injection time of the precursor, the opening time of V_Y was fixed to 5 s per cycle. The chemisorbed precursor on the surface of the substrates was oxidized by O_2 remote plasma. The O_2 plasma was radiated for 20 s per each cycle with an RF power of 300 W.

(a)

Ar 60sccm (tube heated at 150°C)

Ar 100sccm

Ar 0.2MPa

V_{Ar}

V_Y

p_Y

140°C

P_{ch}

sample(200°C)

TMP

p_Y: vapor pressure of the precursor
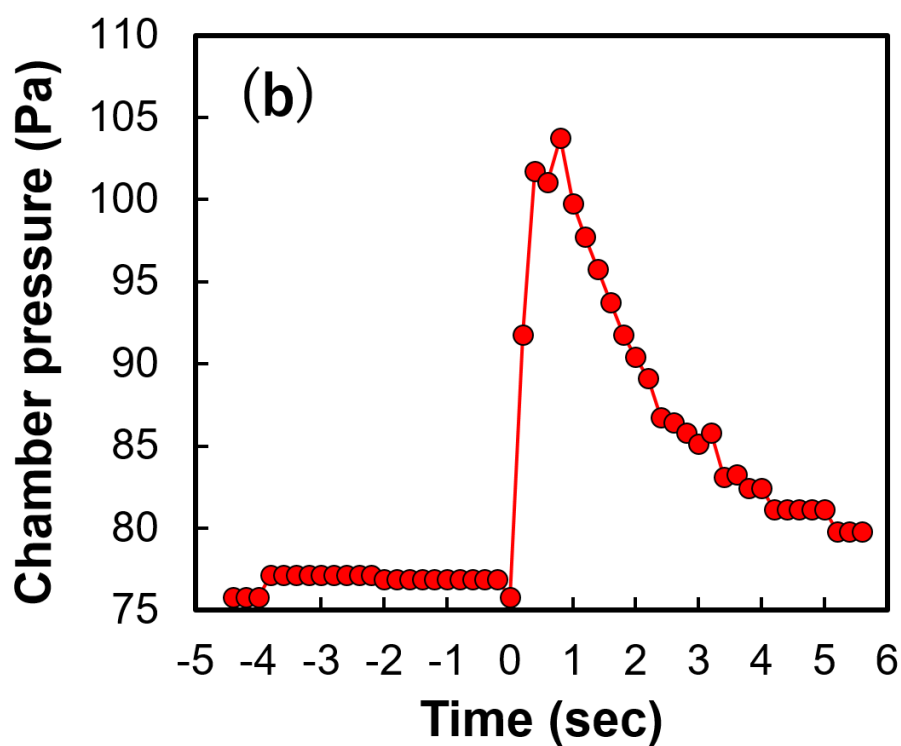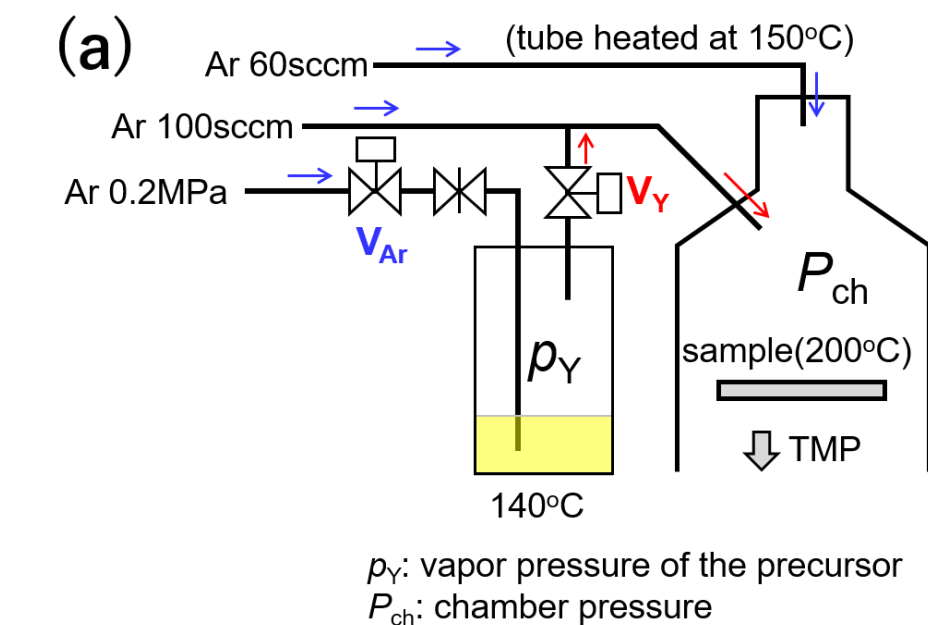P_{ch}: chamber pressure

(b)

Chamber pressure (Pa)

Time (sec)

Fig. 3.2.1 (a) Schematic structure of ALD system assisted by Ar boost. (b) The chamber pressure after the Y(^{i}PrCp)$_3$ precursor injection with 0.5 second-boost.

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3.3 Film coverage by the number of multi-shot

3.3.1 Boost time dependency of growth rate

Firstly, for the Y_2O_3 films, the film thicknesses on different cycles, 50 to 200 cycles, with V_{Ar} opening time of 1 s (a cylinder pressure of 0.17 MPa) or 20 s (a cylinder pressure of 0.2 MPa) are shown in Fig. 3.3.1.1. A linear trend in the thickness on the number of cycles is obtained for both conditions. The GPC of the former condition is calculated to be 0.02 nm/cycle from the slope in the thickness-cycle relationship. This GPC value is a typical value for most ALD processes. Under this condition, a precursor dose of 2.1×10^{15} cm^{-2} can be calculated from the cylinder volume of 100 mL and vapor pressure of 22 Pa deposited on a 6-inch Si wafer. The reactive sticking coefficient of the precursor to the wafer can be calculated as 10^{-1}, which is quite high to those for Al_2O_3 ALD with trimethylaluminum precursor (TMA) of 10^{-3}. On the other hand, for the latter case, a GPC of 0.027 nm/cycle was obtained. We can see a small increase in the GPC with higher cylinder pressure. As the pressure of the cylinder is high enough, a $\eta=1$ can be achieved for both cases. Therefore, the difference in the GPC between the two cases is the difference in the Ar partial pressure. We anticipate that the Ar bombardment to remove the physically adsorbed molecules at the surface may reduce the steric hindrance, resulting to enhance the chemical adsorption and leading to higher coverage. Nevertheless, as the pressure of the Ar gas line connected to the ALD equipment is set to 0.23 MPa, one cannot expect much higher GPC by simply increasing the cylinder pressure.
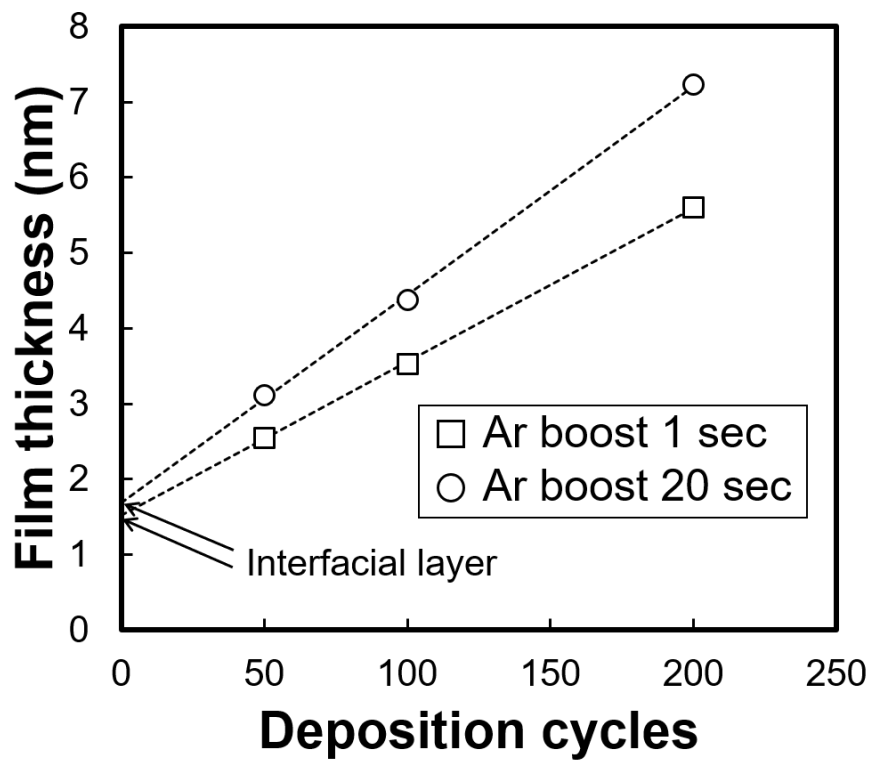
Fig. 3.3.1.1 Y_2O_3 film thickness on cycles for 1 s and 20 s of boost time. The GPC is 0.027 nm/cycle for a boost time of 20 s.

3.3.2 Effect of precursor multi-shot for growth rate

By repeating the set of cylinder pressurization and mixed gas injection into the chamber before oxygen plasma irradiation, a higher dose of the precursor can be exposed to the surface of the substrate. Fig. 3.3.2.1 shows the GPC of the formed Y_2O_3 films under different numbers of shots. The Y_2O_3 film thickness increases with the number of shots and shows a saturation to a GPC at 0.22 nm/cycle. The trend of the coverage with the number of shots can be modeled based on the equation,

$$\frac{dQ}{dt} = r_a - r_d = k_a p(1 - Q) - k_d Q, \tag{3.2}$$

where Q is the surface chemisorption coverage and t is the number of multi-shot. r_a and r_d are the adsorption and desorption rate, respectively. k_a and k_d are the rate constant of adsorption and desorption, respectively and p is the partial pressure of the precursor. Once the coverage is saturated, $dQ/dt = 0$, we obtain a condition of Langmuir isotherm, showing an equilibrium chemisorption coverage, Q^{eq}, and equation 2 can be reduced to the following equation [3-28,3-29],

$$Q^{eq} = \frac{k_a p}{k_a p + k_d} = \frac{1}{1 + (Kp)^{-1}} \quad , \tag{3.3}$$

where K is equal to k_a/k_d. Using equation (2) and (3), the following differential equation is obtained.

$$Q = Q^{eq}(1 - e^{-(k_a p + k_d)t}) \tag{3.4}$$

Q^{eq} of 0.23 nm can be calculated from the monolayer thickness of Y_2O_3 (a=2.65 Å, cubic) [3-30,3-31]. From numerical fit to the data, a $k_a p$ and a k_d of 0.13 and 0.014, respectively, show a good agreement to the obtained GPC for each number of shots. From this relationship, a GPC 0.23 nm/cycle, a monolayer deposition per cycle, can be expected with a larger number of multi-shots.

With the same multi-shot condition, the CeOx films were also deposited at precursor temperature of 130 ℃. The CeO$_x$ film thickness by 40-shot per cycle is shown in Fig. 3.3.2.2. The high GPC of 0.21 nm/cycle is obtained as with the Y$_2$O$_3$ films. From this result, multi-shot process is effective for both Y$_2$O$_3$ and CeO$_x$ films.

Fig. 3.3.2.3 (a) shows the AFM image of the initial surface of the Si substrate before deposition, where a root-mean-square roughness (R_a) is 0.26 nm. Fig. 3.3.2.3 (b)~(d) show the AFM surface images of 5-nm-thick Y$_2$O$_3$ films deposited by single-shot, 5-shot and 10-shot, respectively. The R_a are obtained as (b) 0.39 nm, (c) 0.41 nm and (d) 0.38 nm. The roughness of the Y$_2$O$_3$ films hardly changes by the number of shots. Therefore, one can shorten the processing time by removing unnecessary oxygen plasma exposure. Fig. 3.3.2.4 shows the SIMS profiles of the Y$_2$O$_3$ film formed by the 10-shot process. A uniform carbon atom distribution was observed throughout the film. An optimized process to reduce the carbon atoms in the film may be needed by changing the oxygen plasma condition; power or oxygen gas flow rate, and so on.
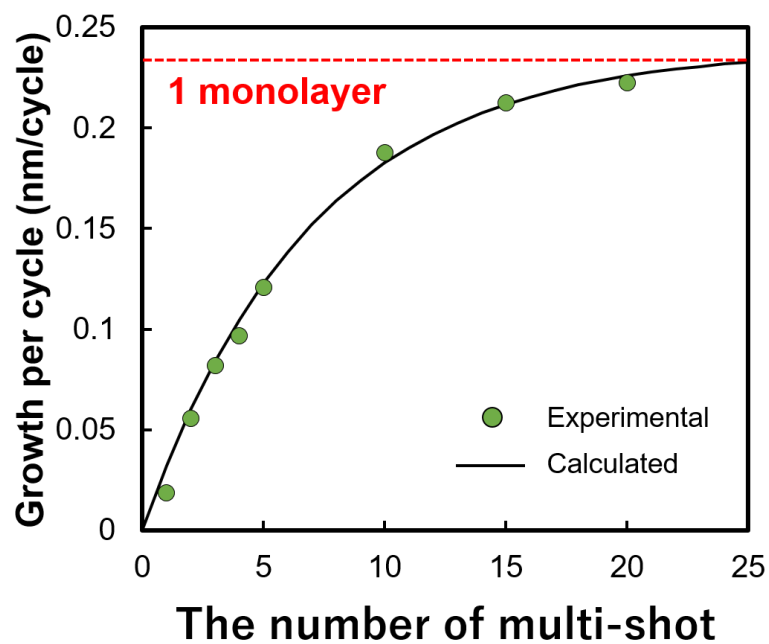
Fig. 3.3.2.1 GPC on the number of multi-shot at an Ar boost of 1 s. The calculated thickness of one monolayer is around 0.23 nm.
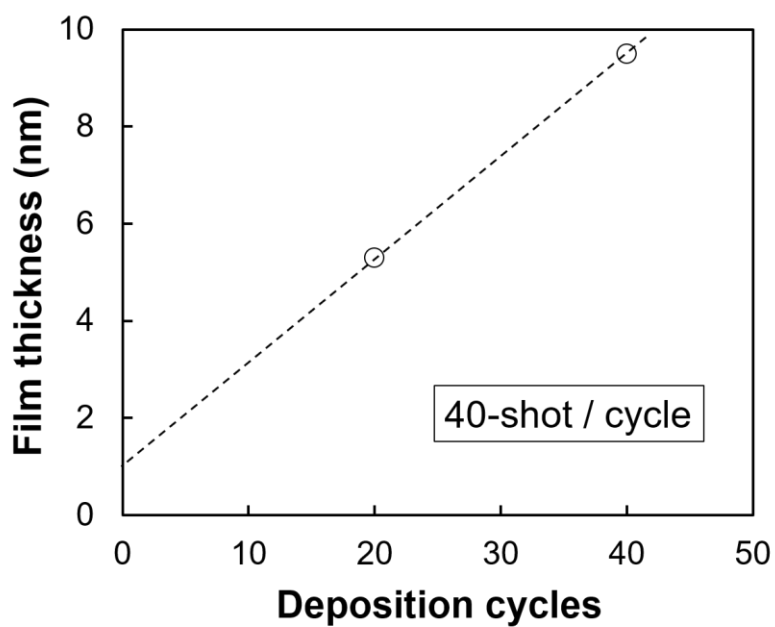

Fig. 3.3.2.2 CeO$_x$ film thickness by 40-shot per cycle at an Ar boost of 1 s. GPC is 0.21 nm/cycle.
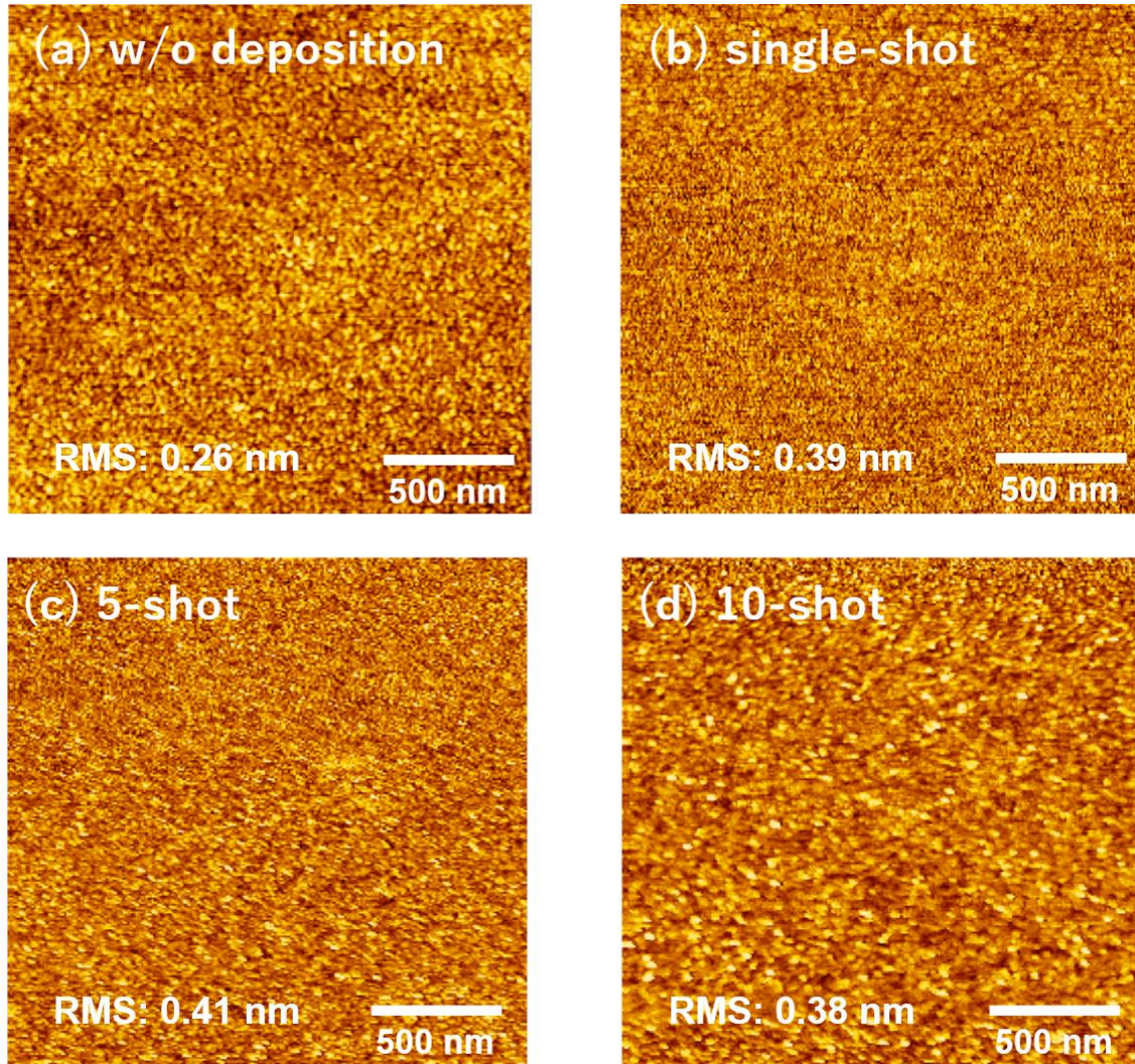
Fig. 3.3.2.3 AFM images of surface for (a) the initial Si substrate, (b) Y_2O_3 deposited by single-shot, (c) Y_2O_3 deposited by multi-shot (5-shot) and (d) Y_2O_3 deposited by multi-shot (10-shot). The Y_2O_3 thicknesses of (b)~(d) are 5 nm.
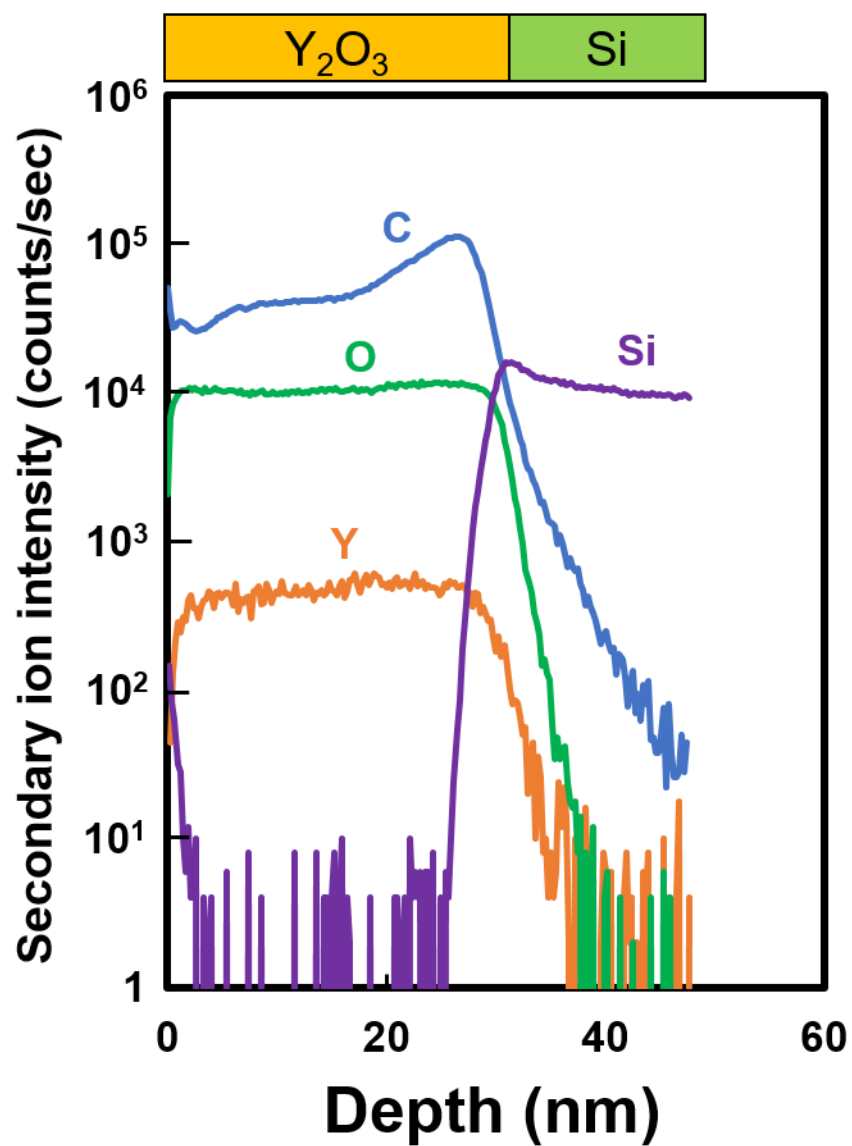
Fig. 3.3.2.4 SIMS profiles of the Y_2O_3 film formed by 10-shot (~32 nm).

3.4 Demonstration of Y-silicate deposition

Rare earth silicates maintain its amorphous structure under the typical semiconductor process temperature range [3-32], which is advantageous for suppression in the leakage current as well as variability [3-33]. The formation of rare earth silicates is commonly conducted by interface reaction between rare earth oxides and a Si substrate under the thermal process [3-34]. However, the interface reaction can aggravate performance in SiC devices which are sensitive to interface property. One of the ways to inhibit the consumption of SiC substrates is to supply Si atoms into the deposited film, forming silicate without any reaction to the substrates.

Yttrium silicate (Y-silicate) films, a typical rare-earth silicate [3-35], are formed by cyclic deposition of Y_2O_3 and SiO_2 in this section. The formation of stable Y-silicate films can extend a range of application for SiC gate dielectrics. Fig. 3.4.1 shows the schematic structure of Y_2O_3/SiO_2 multi-stacked film. The cycles were determined to have the Y/Si atomic ratio of the stacked-layer to be 1:1 by multi-shot process, and the calculated
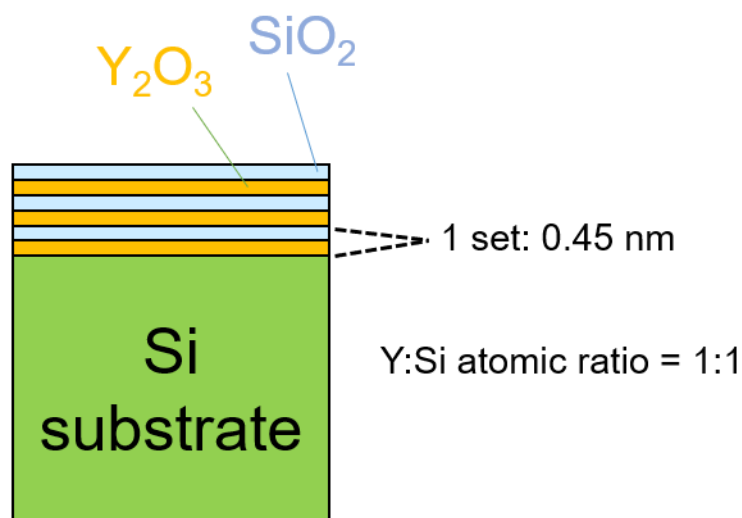

Fig. 3.4.1 Schematic structures of Y_2O_3/SiO_2 multi-stacked films.

minimum thickness of the stacked-layer for the target atomic ratio of 1:1 was 0.45 nm. Moreover, the SiO_2 film was deposited with a tris-dimethylamino-silane (TDMAS) precursor. The temperature of chamber reactor was 200°C.

The stacked-layer with a thickness of 35 nm without annealing process was analyzed by x-ray photoelectron spectroscopy (XPS). Fig. 3.4.2 (a), (b) and (c) show the spectra of Y3d, Si2p and O1s core levels of the stacked-layer with different sputtering times. The peaks of Y3$d_{3/2}$ and Y3$d_{5/2}$ spectra, located at 160.2 eV and 158.2 eV, respectively, are shifted by 1.4 eV from reference positions of 158.8 eV and 156.8 eV of pure Y_2O_3 [3-36]. The shift in the binding energy indicates that most of the Y atoms are in the form of silicate. The Si2p peak at 102.2 eV is separated from 103.3 eV (SiO_2), indicating that the formation of SiO_2 is not apparent. Moreover, the O1s peak at 531.2 eV is also obviously different from the reference peaks of Y_2O_3 (529.5 eV) and SiO_2 (533.0 eV), suggesting that the stacked layer is readily transformed in the form of Y-silicate during ALD process. This fact is in contrast to the Hf-silicate formation by ALD, where annealing process is required to mediate the Hf-O-Si bonding. The bandgap of the stacked-layer was estimated to be 6.4 eV from O1s loss spectrum, which is attractive for various insulator applications. Fig. 3.4.3 shows the XPS depth profile of the stacked-layer obtained by Ar bombardment. The atomic ratio of Y, Si and O remained constant throughout the film at almost 2:2:7 until the Si substrate appeared. From the results, it is confirmed that a uniform Y-silicate layer with a composition of $Y_2Si_2O_7$ can be obtained by the multi-stacking of Y_2O_3/SiO_2 ALD process.
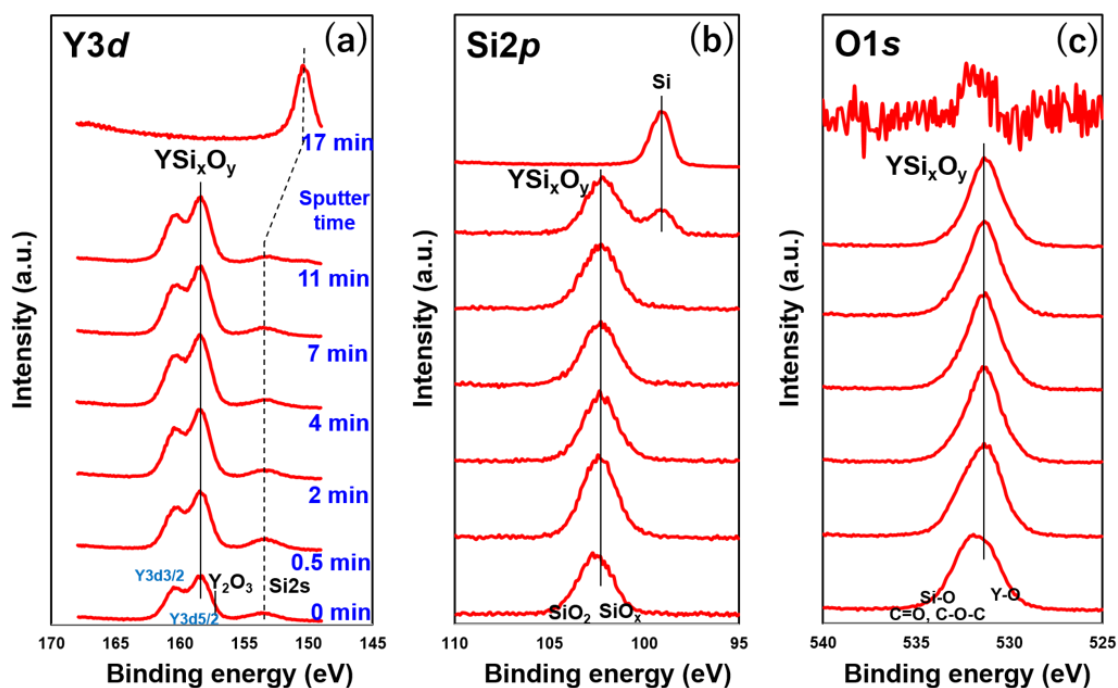
Fig. 3.4.2 XPS spectra of the Y_2O_3/SiO_2 multi-stacked layer ($\sim$ 35 nm, As depo.) for (a) Y3d, (b) Si2p, and (c) O1s regions. The main spectra indicate a Y-O-Si bond.

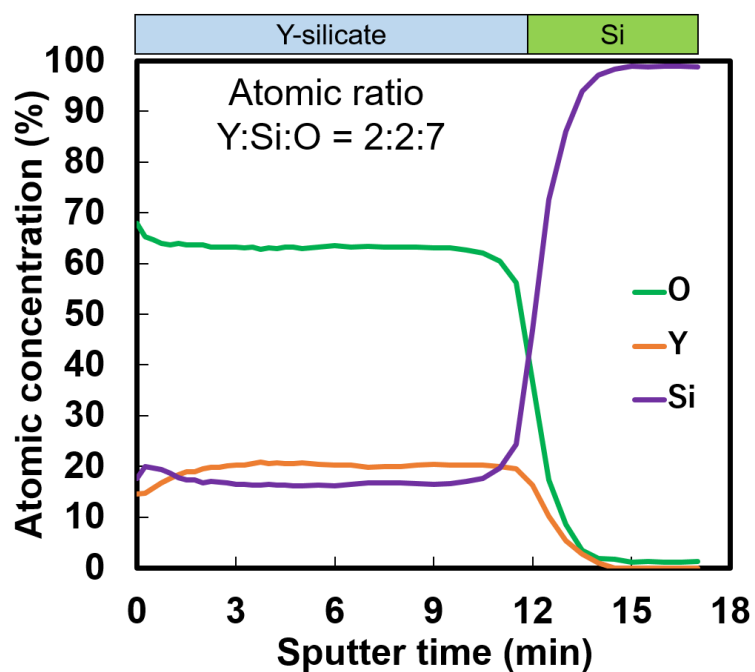

Fig. 3.4.3 XPS depth profile of the Y_2O_3/SiO_2 multi-stacked layer ($\sim$ 35 nm, As depo).

3.5 Summary of chapter 3

We investigated the ALD of Y_2O_3 and CeO_x films by Ar boost technology. A GPC of 0.02 nm/cycle, a typical value for the Y_2O_3 ALD, was obtained by the Ar boost. By repeating the Ar boost precursor injection into the chamber, the GPC was found to increase with the number of shots and showed a saturation to 1 monolayer of Y_2O_3 film. The GPC over the number of shots was well-explained by the adsorption and desorption mode. With 20 multiple shots, the high GPC of 0.22 nm/cycle was achieved. Similarly, the high GPC of 0.21 nm/cycle was obtained in the CeOx films with 40 multiple shots. The films by multiple boot injection did not show any degradation in the surface roughness. Multiple boost injection method has an advantage for effective utilization of the low-vapor pressure precursors for high chamber pressure environment. Finally, Low temperature formation of Y-silicate layer has been confirmed by cyclic deposition of stacked-layer of Y_2O_3 and SiO_2 ALD layers.

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Chapter 4 SiC MOS devices with an Y-silicate interface layer

4.1 XPS analysis for Y-silicate film on SiC substrate

4.2 Thickness of Y-silicate layer on electrical property

4.3 Process temperature of Y-silicate interface layer

4.4 Interface property with a flat Y-silicate interface layer

4.5 Mobility of MOS transistors with a flat Y-silicate interface layer

4.6 Summary of chapter 4

Reference

4 SiC MOS devices with an Y-silicate interface layer

The antioxidation property of Y-silicate to SiC was described in chapter 1.3.1. This property is also suitable for SiC MOS which is sensitive to interface oxidation. The schematic illustration is shown in Fig. 4.1.

In this chapter, we present the electrical characteristics of 4H-SiC MOS devices with the Y-silicate interface layer.
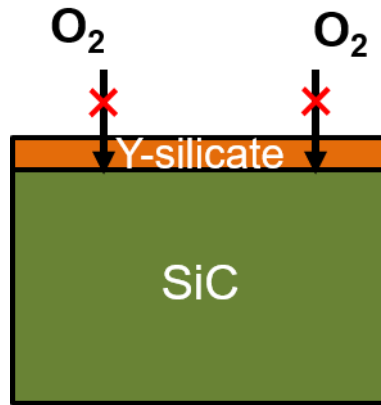

Fig. 4.1 Schematic illustration of oxidation inhibition by Y-silicate layer.

4.1 XPS analysis for Y-silicate film on SiC substrate

Fig. 4.1.1 shows O1s and Si2p spectra of the Y$_2$O$_3$ (3 nm)/SiC sample after annealing at 1000ºC for 30 min in N$_2$. The take-off angle is 90º. In O1s spectra as shown in Fig. 4.1.1 (a), Y-O-Y bonding does not appear. Y$_2$O$_3$ is all transformed into Y-silicate in annealing. On the other hand, Si-O-Si bondings are revealed in both O1s and Si2p spectra, a thick SiO$_2$ of 8.2 nm is formed at the interface. This SiO$_2$ layer may be due to oxygen radicals of Y$_2$O$_3$ layer, therefore, a Y-silicate layer is needed to be formed by SiO$_2$/Y$_2$O$_3$ stacked film in ALD process before annealing.
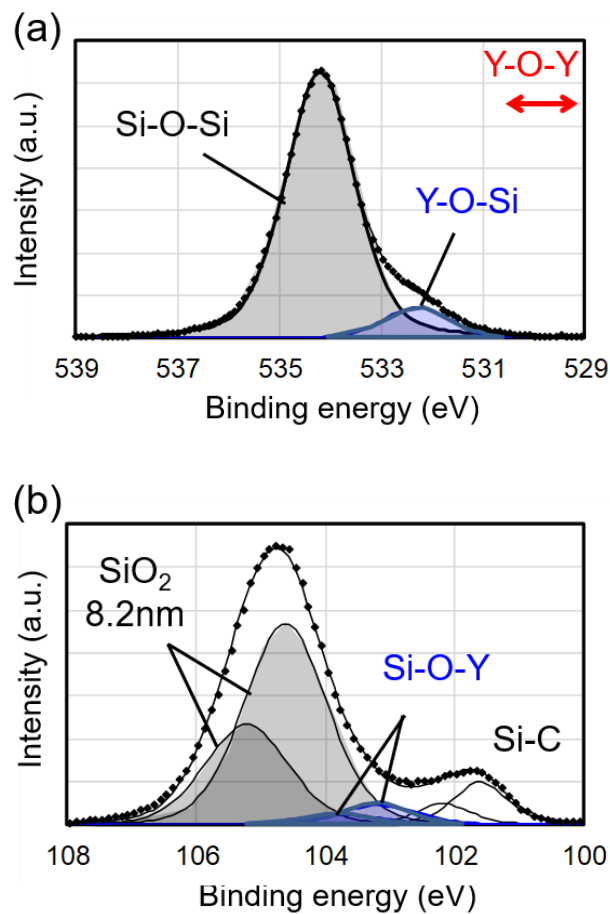
Fig. 4.1.1 (a) O1s and (b) Si2p spectra of Y$_2$O$_3$ (3 nm)/SiC after annealing at 1000ºC for 30 min in N$_2$.

4.2 Thickness of Y-silicate layer on electrical property

For investigation of pure Y-silicate dielectric property, a 40 nm-thick Y-silicate dielectric layer was deposited on a SiC substrate substitute for SiO_2 dielectric. The Y-silicate layer was formed by cyclic deposition of SiO_2/Y_2O_3 stacked layer, thus a $Y_2Si_2O_7$ layer was already formed in ALD process. Fig 4.2.1 shows the $C\text{-}V$ characteristic of the MOS capacitor with 40 nm-thick Y-silicate layer. PDA was performed at 1200°C for 90 min with NO gas. Compared with ideal $C\text{-}V$ curve, the V_{fb} is significantly shifted to positive direction, and the hysteresis voltage (V_{hys}) is also large. This electrical degradation may be caused by large oxide traps or negative fixed charges in the Y-silicate layer.

Contrast to the Y-silicate thick film, the characteristics of 1.2 nm-thick and 2.4 nm-thick Y-silicate interface layer are shown in Fig. 4.2.2. Both thicknesses of SiO_2 layer on the Y-silicate layer are 40 nm. The 1.2 nm-thick Y-silicate layer was formed by 2 set of 0.45 nm-thick SiO_2/Y_2O_3 stacked layer in ALD process as shown in Fig. 3.4.1. The 2.4 nm-thick Y-silicate was formed by 4 set. V_{fb} values of the both $C\text{-}V$ curves are recovered to below 5 V compared with 40 nm-thick Y-silicate dielectric, and the V_{hys} values also decrease with reduction of Y-silicate thickness. Therefore, an ultra-thin Y-silicate layer is necessary for interface engineering as far as possible to prevent electrical degradation.
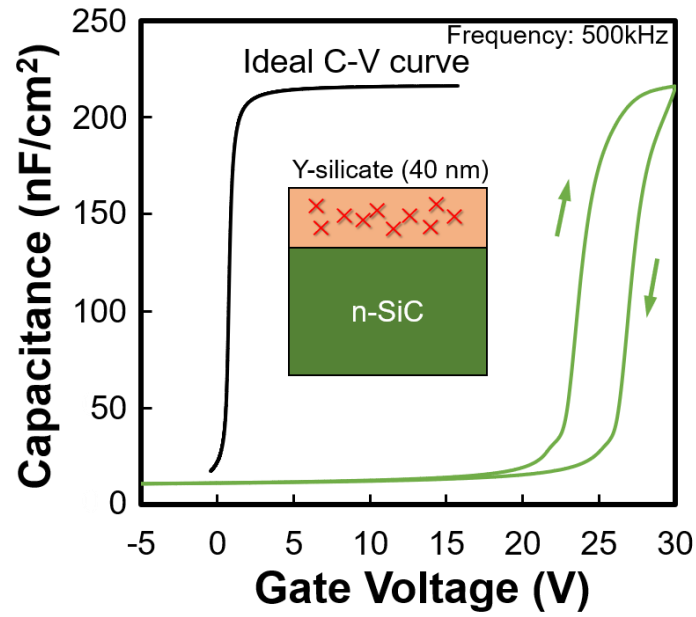
67

Fig. 4.2.1 *C-V* characteristic with 40 nm-thick Y-silicate layer after annealing at 1200ºC for 90 min in NO ambient.
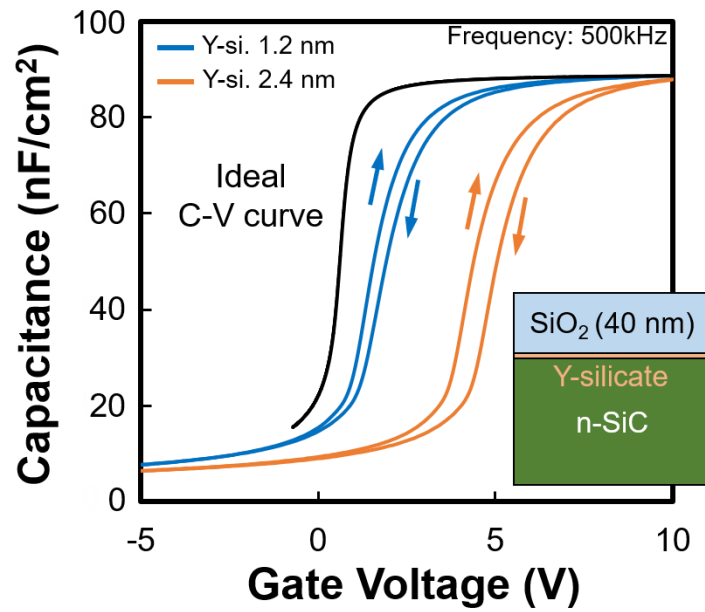

Fig. 4.2.2 *C-V* characteristics with 1.2 nm-thick and 2.4 nm-thick Y-silicate interface layer after annealing at 1200ºC for 90 min in NO ambient.

4.3 Process temperature of Y-silicate interface layer

According to mentioned in chapter 4.2, 0.6 nm-thick Y-silicate layers are deposited at interface of MOS devices as an ultra-thin interface layer. The 0.6 nm-thick Y-silicate layers were formed by reaction of 0.2 nm-thick Y_2O_3 film and 40 nm-thick SiO_2 film in ALD process. First, the stability of the Y-silicate interface layer was investigated. Fig. 4.3.1 (a) and (b) show the transmission electron microscope (TEM) cross-section images with 1000 and 1200°C PDA in NO ambient, respectively. A flat interface is formed with the 1000°C-PDA sample, and a uniform Y-silicate interface layer with a thickness of 0.6 nm is observed. On the other hand, a significant interface roughness arises with the sample annealed at 1200°C. From the contrast in the surface with lattice patterns, the surface of the SiC was partially oxidized to form a nonuniform interface with a spacing of about 5 nm. Therefore, a PDA temperature of 1200°C is too high to keep the Y-silicate interface layer.

Fig. 4.3.2 shows the *C-V* characteristics of MOS capacitors measured at 500 kHz with 0.6 nm-thick Y-silicate interface layer. PDA temperatures for the samples are from 900 to 1200°C. Compared with the small hysteresis (7 mV) of the thermally grown SiO_2 capacitor, the capacitors with Y-silicate interface layers formed by PDA in NO ambient showed a large hysteresis (V_{hys}) of around 0.3~0.4 V, indicating the presence of border traps near the interfaces. Although the presence of the hysteresis, the V_{fb} of the samples stayed at positive values. This fact contrasts with the thermally oxidized capacitor showing a negative V_{fb}. As the TEM image revealed the partial interface reaction at the Y-silicate interface layer, the interface of the sample with the PDA at 1200°C can be the mixture of SiO_2/SiC and Y-silicate/SiC. A small negative V_{fb} shift in the *C-V* curve with the PDA-1200°C sample can be attributed to the presence of SiO_2/SiC interface. As the

Debye length of the SiC epitaxial layer is 53 nm, the *C-V* curve will not show two parallelly connected capacitors; instead, a single negatively shifted *C-V* curve is presented. The slope in the *C-V* curves with the Y-silicate interface layer indicates a high value in the D_{it}. From the conductance method, we obtained a D_{it} value of 6×10^{11} cm^{-2}eV^{-1} in PDA-1200°C sample. However, the value is relatively high compared to the control sample of 1.5×10^{11} cm^{-2}eV^{-1}, which may be due to its non-uniform interface.
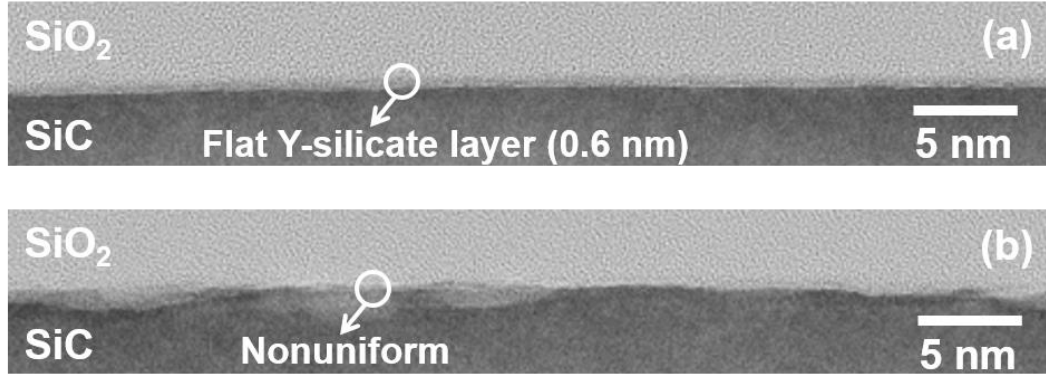
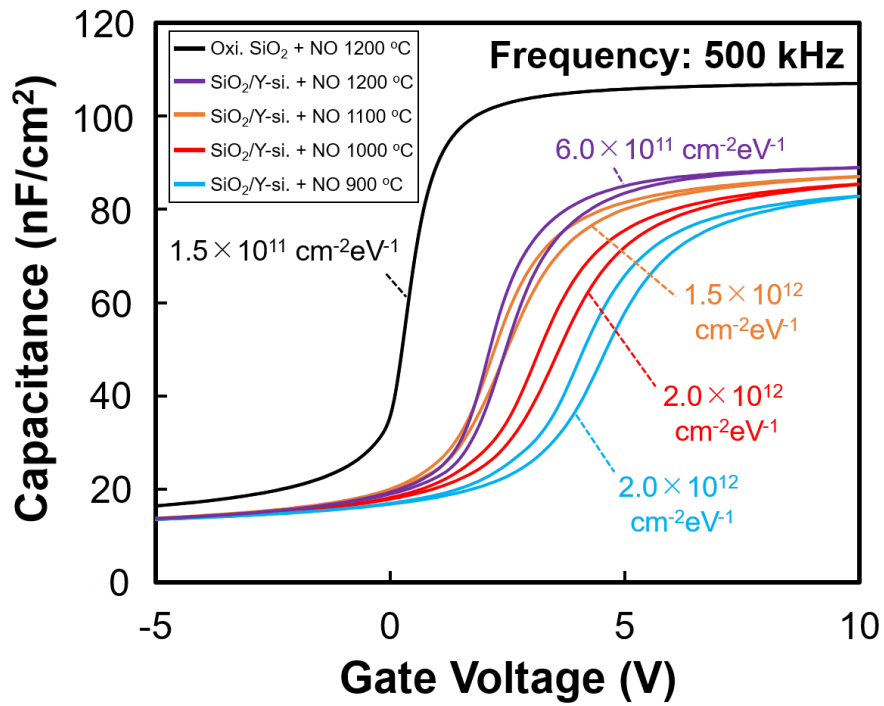Fig. 4.3.1 TEM images of the MOS capacitors with Y-silicate IL. PDA temperature was (a) 1000ºC, and (b) 1200ºC.

Fig. 4.3.2 *C-V* characteristics of MOS capacitors with the Y-silicate interface layer annealed at from 900ºC to 1200ºC for 30 min. The control sample formed by thermal oxidation with NO anneal is shown as a reference. Each D_{it} was measured by the conductance method.

4.4 Interface property with a flat Y-silicate interface layer

In chapter 4.3, we confirmed that a flat Y-silicate interface is formed in 1000°C annealing. To compare properties of dielectrics with flat Y-silicate interface layer and ALD-SiO$_2$ in same annealing condition, those samples were evaluated after 1000°C annealing in N$_2$ ambient.

Fig. 4.4.1 shows the *C-V* characteristics of MOS capacitors with ALD-SiO$_2$ and SiO$_2$/Y-silicate dielectrics after 1000°C annealing in N$_2$ ambient. A V_{hys} with the Y-silicate interface layer is larger than ALD-SiO$_2$ dielectric, this border trap is in accordance with Fig. 4.3.2. However, the D_{it} with Y-silicate interface layer is 1.7×10^{12} cm^{-2}eV^{-1}, which is lower than the ALD-SiO$_2$ dielectric of 2.2×10^{12} cm^{-2}eV^{-1} as shown in Fig. 4.4.2. Although the D_{it} value of 1.7×10^{12} cm^{-2}eV^{-1} is still high, a SiC interface can be slightly improved by Y-silicate layer insertion. From these results, a Y-silicate layer causes a larger oxide trap than SiO$_2$ layer, meanwhile, which reduces an interface trap slightly more than SiO$_2$ layer.
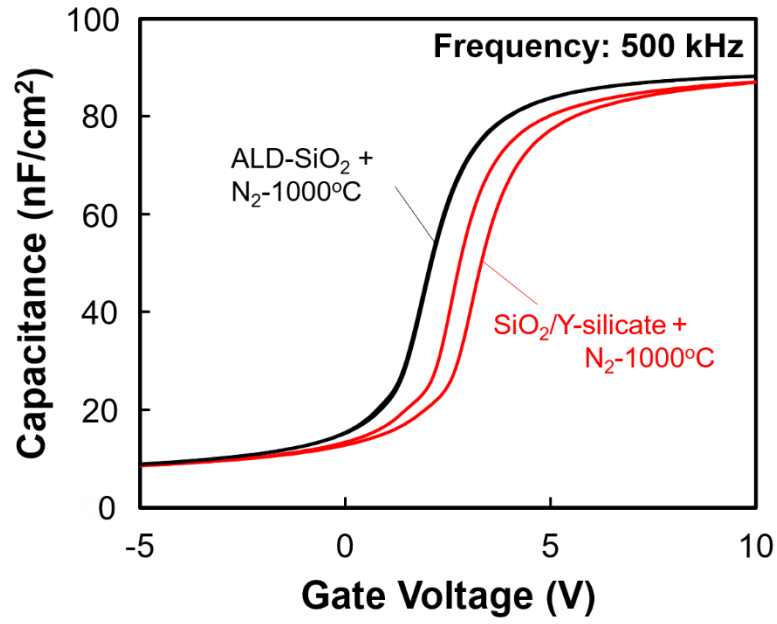
Fig. 4.4.1 *C-V* characteristics of MOS capacitors with Y-silicate interface layer after 1000°C annealing in N$_2$ ambient. For comparison, the MOS capacitor with ALD-SiO2 dielectric was also evaluated.
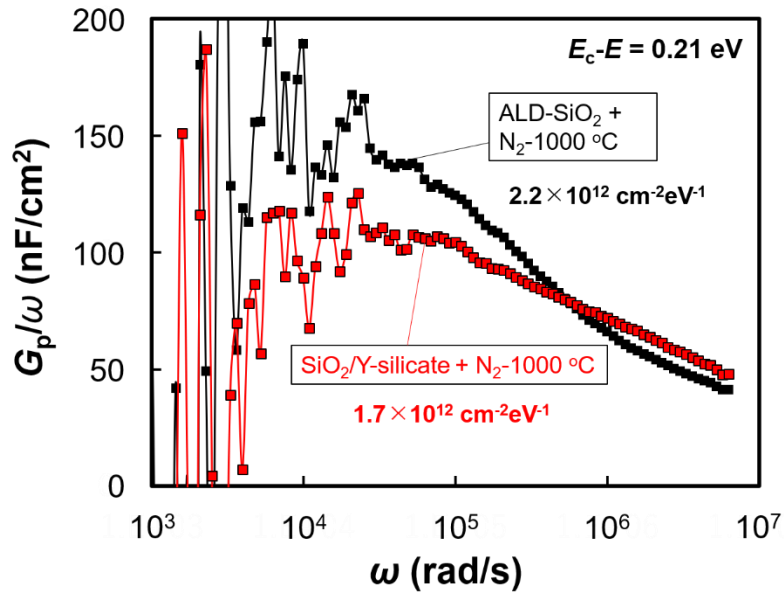

Fig. 4.4.2 D_{it} characteristics of MOS capacitors with ALD-SiO$_2$ and SiO$_2$/Y-silicate dielectrics by conductance method.

4.5 Mobility of MOS transistor with a flat Y-silicate interface layer

Next to the MOS capacitors, field effect mobilities of MOSFETs with ALD-SiO_2 and SiO_2/Y-silicate dielectrics were evaluated. The mobility characteristics is shown in Fig. 4.5.1. With a Y-silicate interface, the peak mobility slightly increases from 14 cm^2/Vs of SiO_2 interface to 19 cm^2/Vs. This mobility increase may be due to the D_{it} reduction as shown in Fig. 4.4.2. The V_{th}, on the other hand, increases from 2.9 V to 4.2 V, which agrees with the high V_{fb} observed in the capacitors. Although the SiO_2 interface keeps a V_{th} without negative shift after 1000ºC annealing, a Y-silicate interface layer can be more helpful to suppress negative V_{th} shift for high temperature annealing.
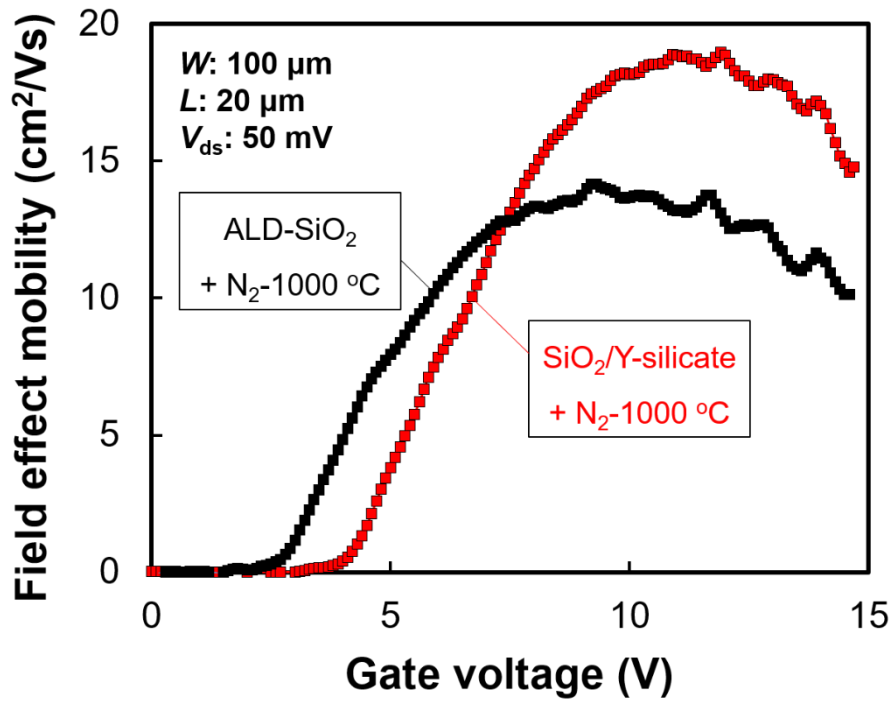

Fig. 4.5.1 Field effect mobility characteristics of MOSFETs with the Y-silicate interface layer. PDA condition is 1000ºC for 30 min in N_2 ambient.

4.6 Summary of chapter 4

The influence of Y-silicate interface layer on the electrical characteristics of SiC MOS devices was investigated. A uniform Y-silicate interface layer was confirmed at the SiO_2 and SiC interface with an annealing temperature of 1000ºC. Although the presence of the hystereses in the C-V curves with the Y-silicate interface layer, the V_{fb} resides at a positive value even at high PDA temperature in NO ambient. The suppression of negative V_{fb} shift by Y-silicate interface layer was also confirmed compared with SiO_2 interface layer even at same annealing temperature of 1000ºC which maintains a flat Y-silicate interface layer. In addition, the D_{it} was slightly reduced by flat Y-silicate interface layer. In SiC MOSFETs, the relative high mobility of 19 cm^2/Vs with V_{th} of 4.2 V was obtained with Y-silicate interface layer after the 1000ºC annealing. A suppression of negative electrical shift and mobility recovery can be achieved by insertion of Y-silicate interface layer. As shown in Fig. 4.6.1, the V_{th} with Y-silicate interface layer is relatively good, however peak mobility is still insufficient.
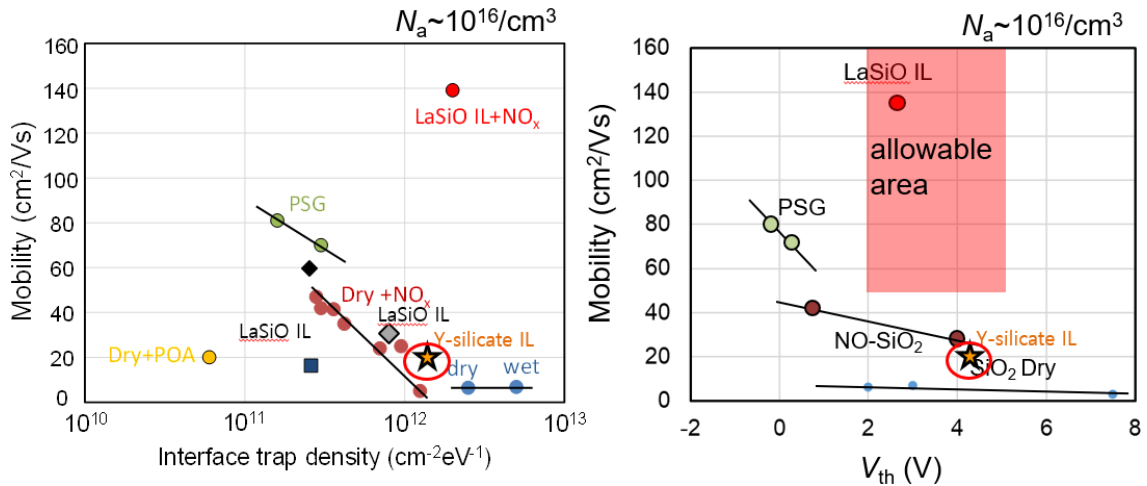

Fig. 4.6.1 Relationship between mobility, D_{it} and V_{th} for Y-silicate interface layer.

Chapter 5 Mobility recovery by a CeO_x layer insertion

5.1 XPS analysis for CeO_x films on SiC substrates

5.2 Cross sectional TEM images of SiO_2/CeO_x dielectrics

5.3 Interface properties of CeO_x interface layers on SiC substrates

5.4 Electron mobility recovery with CeO_x interface layers

5.5 Summary of chapter 5

Reference

5 Mobility recovery by a CeO$_x$ layer insertion

CeO$_x$ is known to promote oxidation of adjacent materials by producing radical oxygen atoms. For instance, an interface SiO$_2$ layer is formed after annealing the CeO$_x$/Si structure. [5-1] The interface layer formation is triggered by the supply of oxygen atoms to change the valence number of Ce atoms during the reaction. Although 4H-SiC surface is less reactive to oxygen atoms than Si surface, one can still expect the formation of the interface SiO$_2$ layer as shown in Fig. 5.1. Since the reaction is based on oxygen radicals, the interface structure might be different from those created by thermally grown SiO$_2$. Therefore, in this paper, the interface oxidation with a CeO$_x$ layer on a 4H-SiC surface was examined by x-ray photoelectron spectroscopy (XPS) analyses. And then, the effect of SiO$_2$ layer capping to the interfacial reaction with the SiC surface was examined. Moreover, the μ_{FE} and the V_{th} of the MOSFET are extracted.
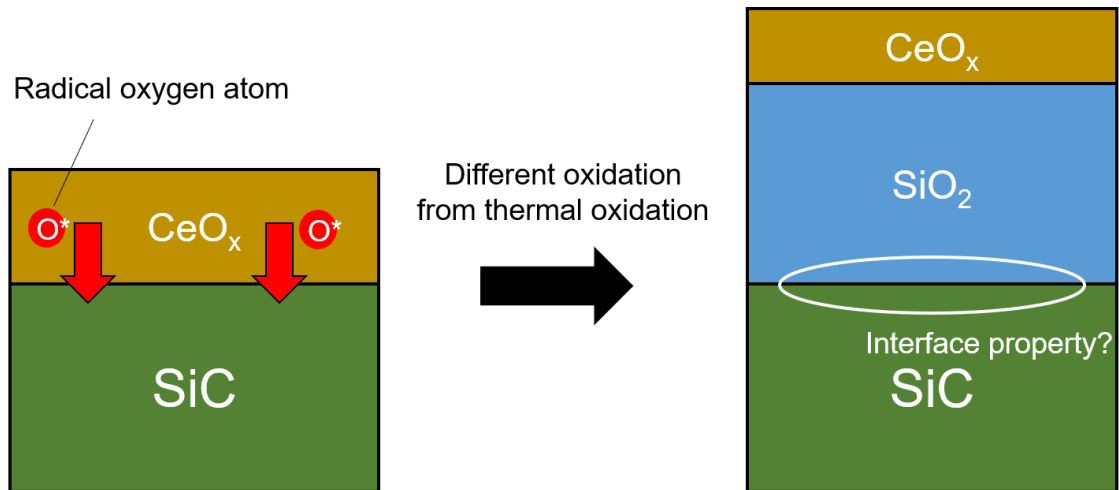

Fig. 5.1 Oxidation of SiC surface by radical oxygen atom in CeO$_x$ layer.

5.1 XPS analysis for CeO$_x$ films on SiC substrates

Fig. 5.1.1 shows C1s spectra of the CeO$_x$ (1 nm)/SiC sample before and after annealing at 1000°C for 30 min in N$_2$. The take-off angle is 90°. The spectra show almost no change after annealing compared with the thermally grown SiO$_2$/SiC and non-annealed CeO$_x$/SiC samples though organic surface contamination is observed. From these results, an additional carbide is not formed with CeO$_x$ layer.

Fig. 5.1.2 shows Si2p spectra with above measurement condition. Besides the formation of suboxides (Si^{1+}) at the interface, no apparent signal of the formation of SiO$_2$ was detected before annealing. The large intensity of SiO$_2$ was observed after the annealing, where the thickness can be deduced to be 5.9 nm, using the escape depth of 3.2 nm in the SiO$_2$ layer. The intensity of the SiO$_2$ is stronger than that of the thermally grown SiO$_2$ layer formed by 1000°C for 20 min under O$_2$ gas flow, where the thickness is only 2.7 nm. The source of oxygen molecules to trigger the interface oxidation can be the residual oxygen gas in the furnace. This fact suggests that CeO$_x$ layer can effectively oxidize the SiC surface even for an oxygen-lean environment, as was observed for the CeO$_x$/Si case.

Fig. 5.1.3 shows O1s spectra of the CeOx (1 nm)/SiC sample before and after annealing at 1000°C for 30 min in N$_2$. The measurement was performed at take-off angle of 15° and 90°. Before annealing, The Ce-OH bonding is observed with the Ce-O bonding. This Ce-OH bonding may be due to Ce(OH)$_x$ layer on the CeO$_x$ layer, which is formed by reaction of CeO$_x$ layer and H$_2$O. Also, the intensity of Si-O-Si and Ce-O-Si bondings corresponds to less than 0.1 nm in thickness at interface. After annealing, the presence of Ce-silicate and CeO$_x$ is observed along with the SiO$_2$ layer. The TOA dependent intensity ratio of the signal from Ce-silicate and CeO$_x$ showed little difference. Therefore, the composition of the CeO$_x$ layer after annealing can be the mixture of Ce-silicate and CeO$_x$.
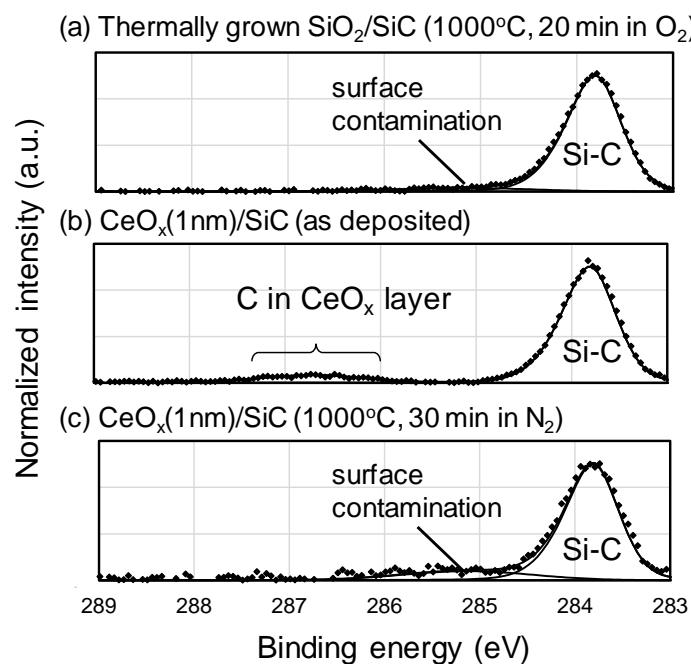
Fig. 5.1.1 C1*s* spectra of (a) thermally grown SiO$_2$/SiC, (b) CeO$_x$ (1 nm)/SiC before annealing and (c) CeO$_x$ (1 nm)/SiC after annealing at 1000°C for 30 min in N$_2$.
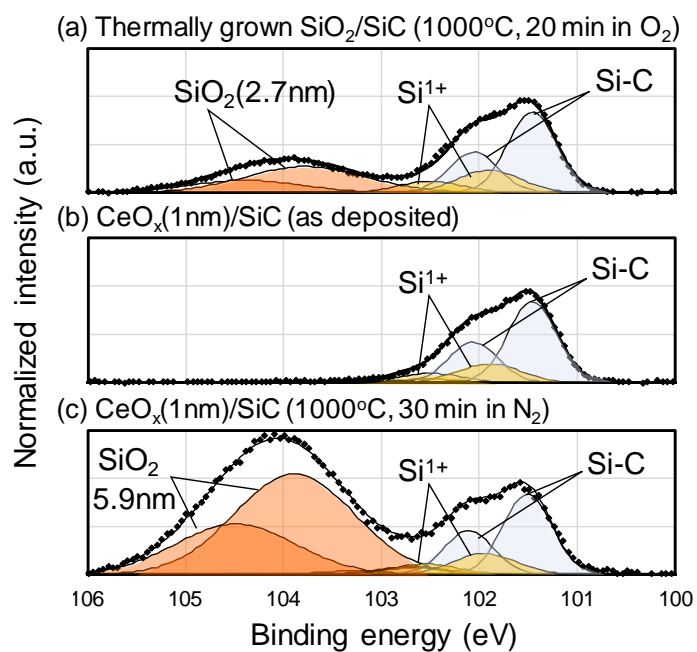

Fig. 5.1.2 Si2*p* spectra of (a) thermally grown SiO$_2$/SiC, (b) CeO$_x$ (1 nm)/SiC before annealing and (c) CeO$_x$ (1 nm)/SiC after annealing at 1000°C for 30 min in N$_2$.
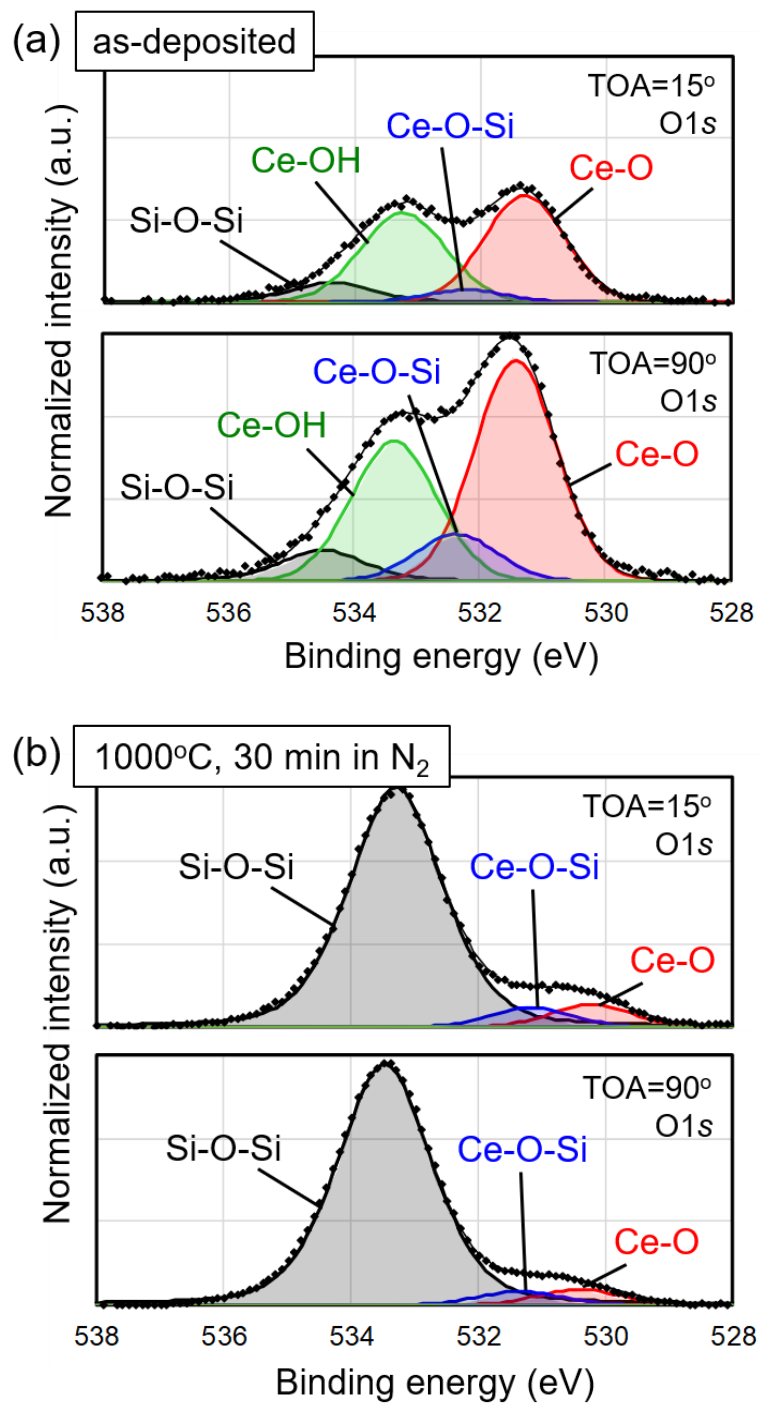
Fig. 5.1.3 O1s spectra of (a) CeO_x (1 nm)/SiC before annealing and (b) CeO_x (1 nm)/SiC after annealing at $1000^{\circ}C$ for 30 min in N_2.

5.2 Cross sectional TEM images of SiO$_2$/CeO$_x$ dielectrics

The diffusion of oxygen species to reach the CeO$_x$ layer and to oxidize the SiC surface during the N$_2$ annealing can be reduced when a 40-nm-thick SiO$_2$ is capped to the CeO$_x$ layer. Fig. 5.2.1 (a) and (b) show the bright field cross-sectional transmission electron microscope (TEM) images of the samples annealed at 1000 and 1100°C, respectively. By comparing the TEM image with no CeO$_x$ layer annealed at 1100°C in O$_2$ ambient, shown in Fig. 5.2.1 (c), one can observe a 1.1-nm-thick interfacial layer with a contrast difference with respect to those of the SiO$_2$ layer and the SiC epitaxial layer. Also, we can confirm that there is no interface roughness difference among the images. From the above XPS analyses, we can assign the interfacial layer to be the mixture of Ce-silicate and CeO$_x$ components. We can also observe that the interfacial layer is in direct contact with the SiC surface, and no interfacial SiO$_2$ layer is formed. Besides, the increase in the thickness of the capped SiO$_2$ layer by 3.5 nm was observed. The origin of the growth in the capped SiO$_2$ layer is unknown at this moment. However, considering that Si or Ge atoms are emitted from those substrates during thermal treatment under mechanical constraints in an oxygen-lean environment with HfO$_2$ gate dielectrics, the emission of Si and C atoms from the SiC is likely to happen. [5-2,5-3]
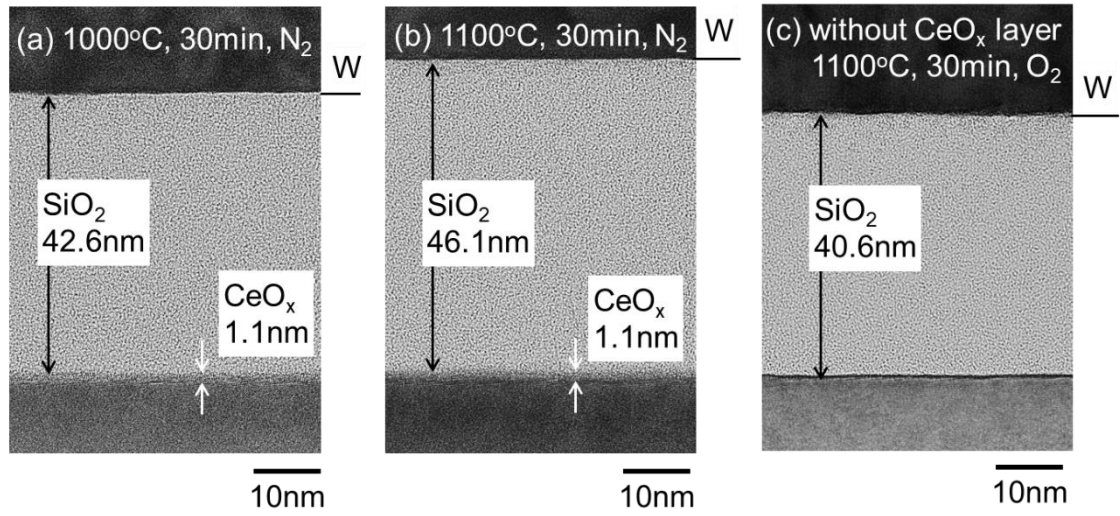
Fig. 5.2.1 Cross-sectional TEM images of W/SiO$_2$/CeO$_x$/SiC substrates annealed at (a) 1000°C and (b) 1100°C in N$_2$ gas flow. (c) TEM image with no CeO$_x$ layer annealed at 1100°C in O$_2$ gas flow.

5.3 Interface properties of CeO$_x$ interface layers on SiC substrates

Fig. 5.3.1 shows the capacitance-voltage (*C-V*) characteristics of SiC-MOS capacitors with 1 nm-thick CeO$_x$ interface layers. The accumulation capacitance gradually decreased along with higher temperature annealing. The reduction in the capacitance is in good agreement with the observed growth of the capped SiO$_2$ layer by the presence of CeO$_x$ layer. All the samples show large hysteresis (V_{hys}) of about 0.6 V, which is significantly higher than the NO-annealed sample of 7 mV. This indicates that a high density of border traps is present and cannot be removed by high-temperature annealing. However, the flatband voltages (V_{fb}) of the samples kept at positive values, which is in contrast to the negative shift observed for the NO-annealed sample. The interface state density (D_{it}) of MOS capacitors extracted by conductance method with the CeO$_x$ layers are shown in Fig. 5.3.2. D_{it} values of 6.8×10^{11} cm^{-2}eV^{-1} and 5.8×10^{11} cm^{-2}eV^{-1} were deduced for 900 and 1100°C annealed samples, respectively. These values, indeed, are higher than the D_{it} of NO-annealed sample of 1.5×10^{11} cm^{-2}eV^{-1}. However, considering that no nitrogen passivation process was conducted and the process temperature is low, the obtained D_{it} can be considered to be decent values.
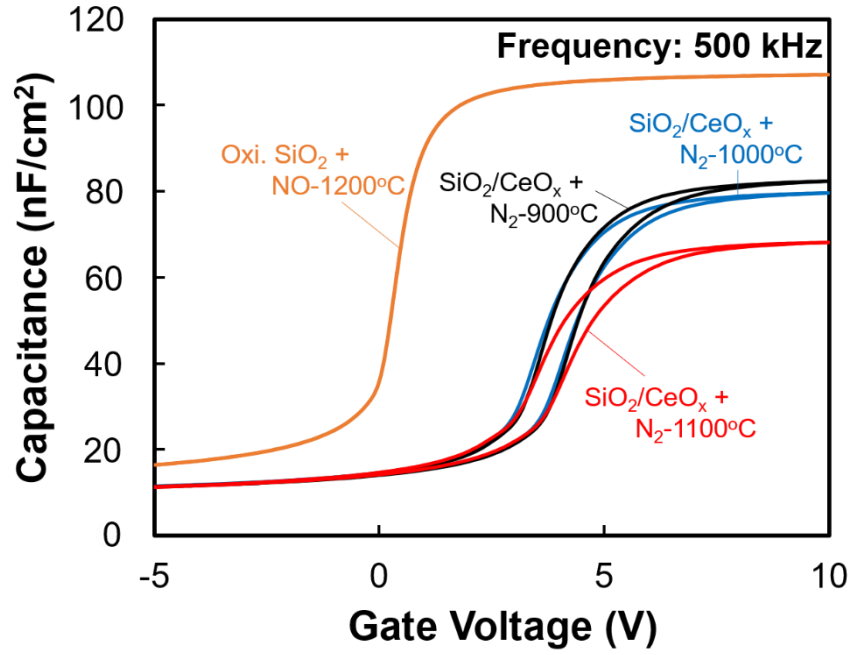
Fig. 5.3.1 *C-V* characteristics of MOS capacitors with CeO_x layer insertion. PDA temperatures are 900, 1000 and 1100°C, respectively.
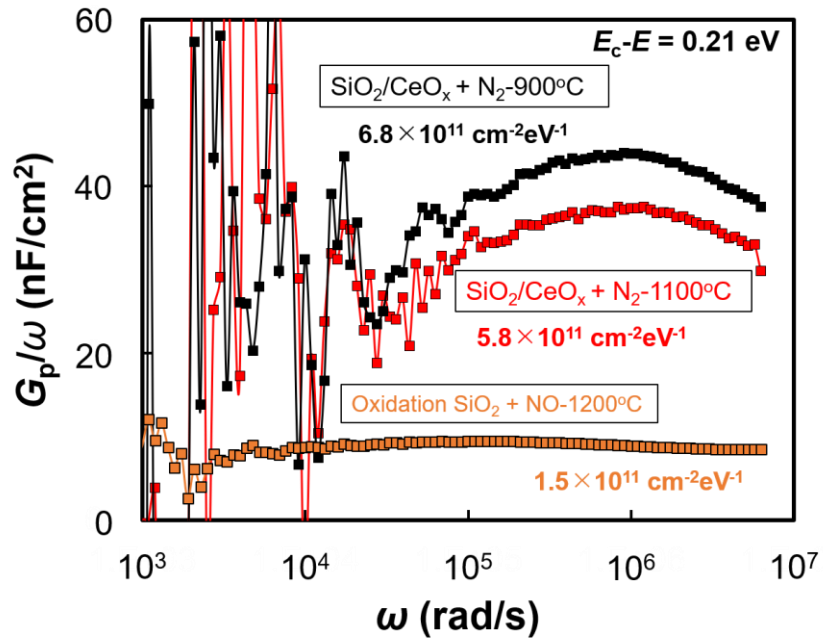

Fig. 5.3.2 D_{it} characteristics of MOS capacitors with CeO_x layer insertion by conductance method.

5.4 Electron mobility recovery with CeO_x interface layers

The μ_{FE} of MOSFETs with the CeO_x layer and subsequent annealing in N_2 gas at various temperatures are shown in Fig. 5.4.1. Due to the presence of hysteresis, the μ_{FE} values were calculated from pulse I_d-V_g measurements with a gate pulse width of 1 ms. A high peak μ_{FE} value of 48 cm^2/Vs was obtained with the 900°C annealed sample, and further enhancement up to 54 cm^2/Vs was achieved with 1100°C annealing. These values are almost double the value obtained with the NO-annealed FET of 25 cm^2/Vs. In addition to the high μ_{FE} values, the negative shift in the V_{th} was well suppressed with the interface oxidation by the CeO_x layer; namely 3.1 V and 2.3 V for 900°C and 1100°C annealed FETs, respectively. This is in contrast to the NO-annealed FET where the V_{th} shifted to the negative direction to 0.6 V. Considering a theoretical V_{th} of 3.0 V with a work function of 4.6 eV for W gate electrode, the obtained V_{th} values with CeO_x layer are reasonable. The basic mechanism for the high μ_{FE} and high V_{th} is still unclear. A recent work on high-density oxygen plasma to form a SiO_2 layer without nitrogen passivation process reports a high peak μ_{FE} of 44 cm^2/Vs with a high V_{th} of 5.4 V, owing to a sharp interface with reduced roughness compared to the thermally grown SiO_2 ones. [5-4] As the CeO_x interfacial layer oxidize the SiC surface by radical oxygen atoms, the surface oxidization process might be the key to obtaining both high μ_{FE} and V_{th}.
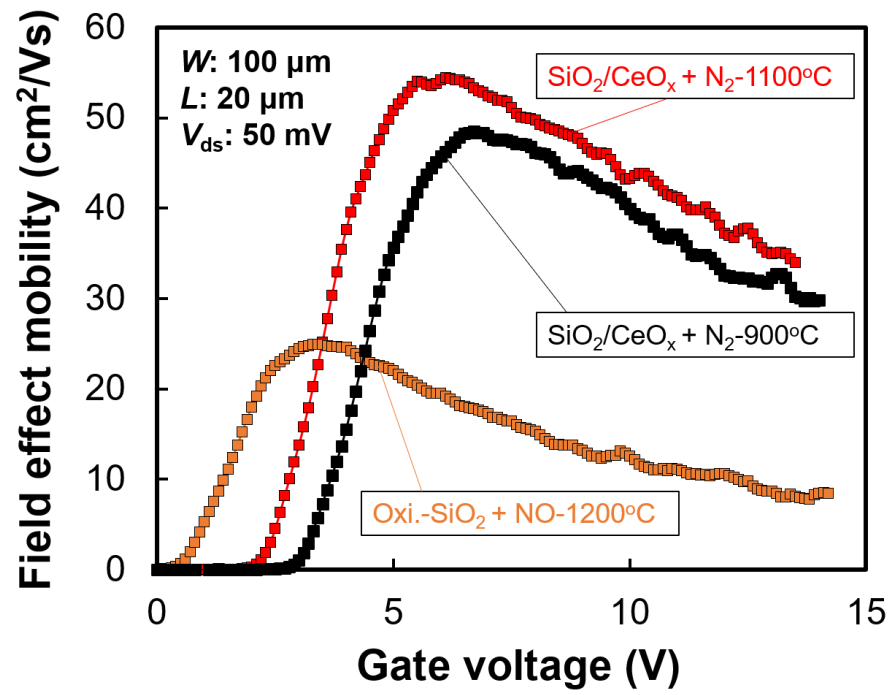
Fig. 5.4.1 Field effect mobility characteristics of MOS capacitors with CeO$_x$ layer insertion.

5.5 Summary of chapter 5

Enhanced oxidation of the 4H-SiC surface in an oxygen-lean environment by a thin CeO_x layer was confirmed. By capping with a 40-nm-thick SiO_2 layer on a 1-nm-thick CeO_x layer, the formation of the interfacial SiO_2 layer was suppressed, and the growth of the capped SiO_2 layer was observed instead. A high peak field mobility of 54 cm^2/Vs was obtained with the structure, which is higher than the commonly used thermally grown SiO_2 layer with NO-based high-temperature annealing. Moreover, the V_{th} kept higher than 2 V, which has an advantage over other mobility enhancement gate oxide formation processes. As shown in Fig. 5.5.1, CeO_x interface layer successfully achieved both high peak mobility and V_{th}.
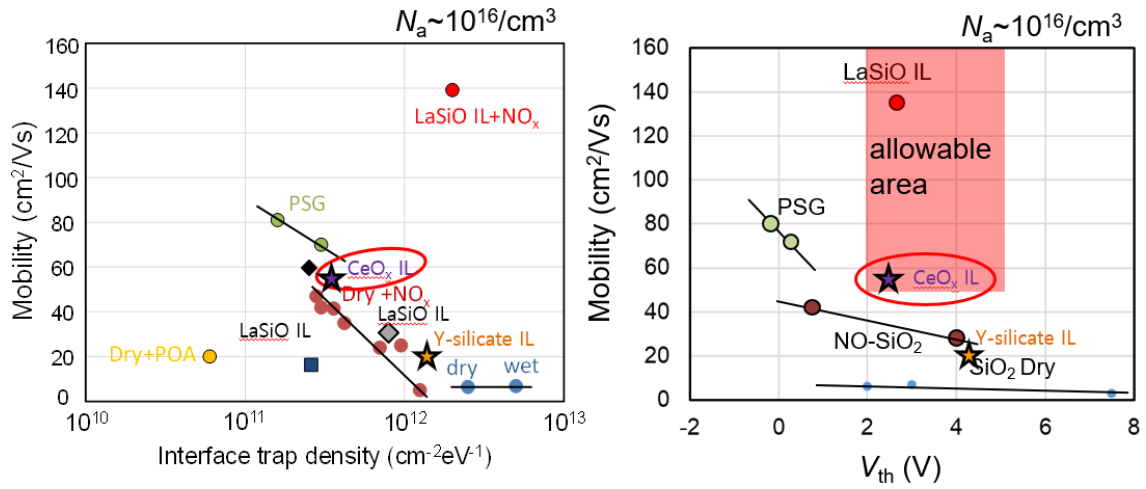

Fig. 5.5.1 Relationship between mobility, D_{it} and V_{th} for CeO_x interface layer.

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[5-1] M. Mamatrishat, M. Kouda, K. Kakushima, H. Nohira, P. Ahmet, Y. Kataoka, A. Nishiyama, K. Tsutsui, N. Sugii, K. Natori, T. Hattori, H. Iwai, Vacuum, 86, pp. 1513-1516 (2012).

[5-2] Z. Ming, K. Nakajima, M. Suzuki and K. Kimura, Appl. Phys. Lett., 88, 153516 (2006).

[5-3] R. Asahara, I. Hideshima, H. Oka, Y. Minoura, S. Ogawa, A. Yoshigoe, Y. Teraoka, T. Hosoi, T. Shimura and H. Watanabe, Appl. Phys. Lett., 106, 233503 (2015).

[5-4] X. Liu, J. Hao, N. You, Y. Bai, Y. Tang, C. Yang and S. Wang, Chin. Phys. B, 29, 037301 (2020).

Chapter 6 CeO$_x$ and Y-silicate gate dielectric stack

6 CeOₓ and Y-silicate gate dielectric stack

Advantages of Y-silicate and CeO_x layer insertion were investigated in chapter 4 and 5. The Y-silicate interface layers were effective for suppression of negative electrical shift, and the mobility was slightly increased. The CeO_x layers on SiC substrates significantly recovered electron mobility, however, the suppression effect for negative V_{th} shift was weaker than Y-silicate layer.

In this chapter, the electrical characteristics of MOS devices with CeO_x/Y-silicate stacked and Y-silicate/CeO_x stacked interface layers will be investigated. In CeO_x/Y-silicate structure, Y-silicate/SiC interface is formed by radical oxygen while blocking the oxygen atom diffusion from SiO_2. Meanwhile, the effect of radical oxygen atom to modify the dielectric/SiC interface is limited. The schematic concept is shown in Fig. 6.1. We investigate how the change of surface oxidation conditions affects the device characteristics.
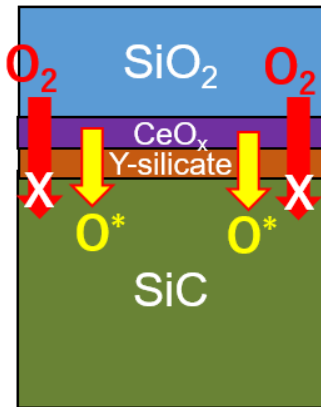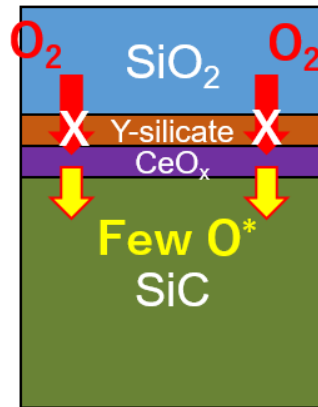

Fig. 6.1 Expected effect for SiC surface with CeO_x/Y-silicate and Y-silicate/CeO_x interface layers.

6.1 Interface properties of stacked oxides

6.1.1 CeO_x/Y-silicate stacked interface layer

 Fig. 6.1.1.1 shows the *C-V* characteristics of MOS capacitors with CeO_x/Y-silicate interface layers. Annealing condition is 900ºC and 1000ºC for 30 min in N_2 ambient. Thicknesses of CeO_x and Y-silicate layer are 1 nm and 0.6 nm, respectively. V_{fb} values with CeO_x/Y-silicate interface layer after 900ºC and 1000ºC annealing increase compared with CeO_x interface layer sample. It implies that negative fixed charge is increased by Y-silicate layer insertion between CeO_x and substrate. The D_{it} characteristics of the both samples are shown in Fig. 6.1.1.2. In CeO_x/Y-silicate interface layer, a D_{it} increases with high temperature annealing. Although the D_{it} values with CeO_x/Y-silicate interface layers are lower than 1.7×10^{12} $cm^{-2}eV^{-1}$ with Y-silicate interface layer (with 1000ºC annealing), however, higher than 6.8×10^{11} $cm^{-2}eV^{-1}$ of CeO_x interface layer (with 900ºC annealing). As the Y-silicate layer under CeO_x layer interrupts a diffusion of radical oxygen atom, the effect of CeO_x layer may become weak. From these results, Y-silicate layer insertion to interface limits D_{it} reduction.
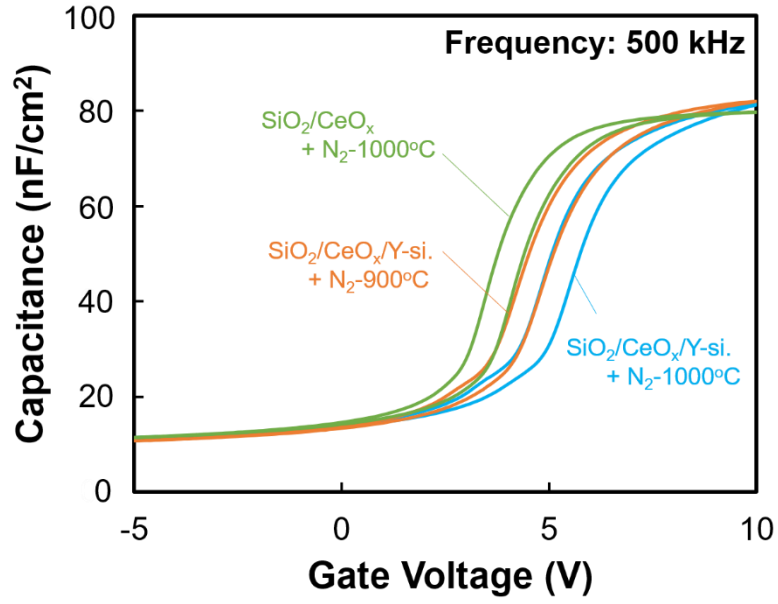
Fig. 6.1.1.1 *C-V* characteristics of MOS capacitors with CeO_x/Y-silicate interface layers. PDA conditions are 900ºC and 1000ºC for 30 min in N_2 ambient, respectively. For comparison, a sample with CeO_x interface layer was prepared.
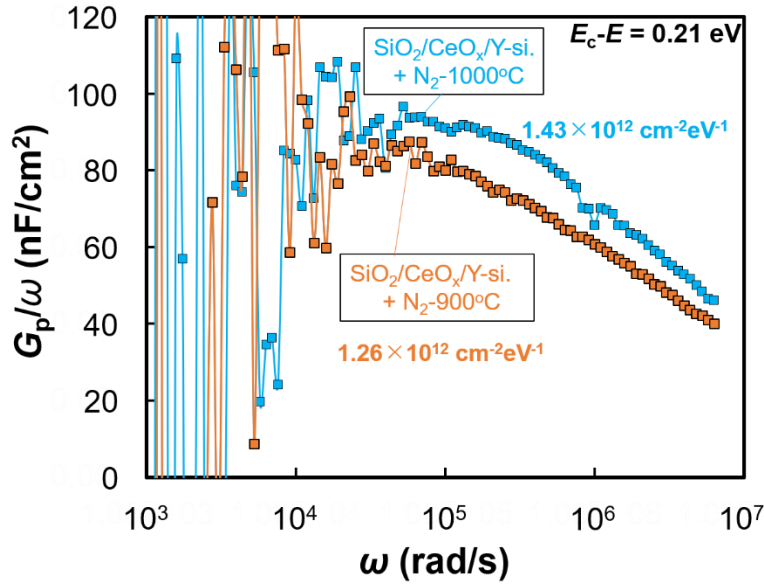

Fig. 6.1.1.2 D_{it} characteristics of MOS capacitors with CeO_x/Y-silicate interface layers by conductance method.

6.1.2 Y-silicate/CeO$_x$ stacked interface layer

Fig. 6.1.2.1 shows the *C-V* characteristics of MOS capacitors with CeO$_x$ and Y-silicate/CeO$_x$ interface layers after annealing at 1000ºC for 30 min in N$_2$ ambient. Thicknesses of CeO$_x$ and Y-silicate layer are also 1 nm and 0.6 nm. The V_{hys} values of both samples are almost same, and positive V_{fb} shift appears with insertion of Y-silicate layer on CeO$_x$ layer. Even if the Y-silicate layer is inserted on the CeO$_x$ layer, effect of increasing V$_{fb}$ can be obtained. Additionally, the D_{it} characteristics of the both samples are shown in Fig. 6.1.2.2. A D_{it} with Y-silicate/CeO$_x$ interface layer is 9.2×10^{11} cm^{-2}eV^{-1} which is higher than 5.3×10^{11} cm^{-2}eV^{-1} of the sample without Y-silicate layer. Radical oxygen effect is weakened by Y-silicate layer, which may have caused insufficient surface oxidation and D_{it} reduction.
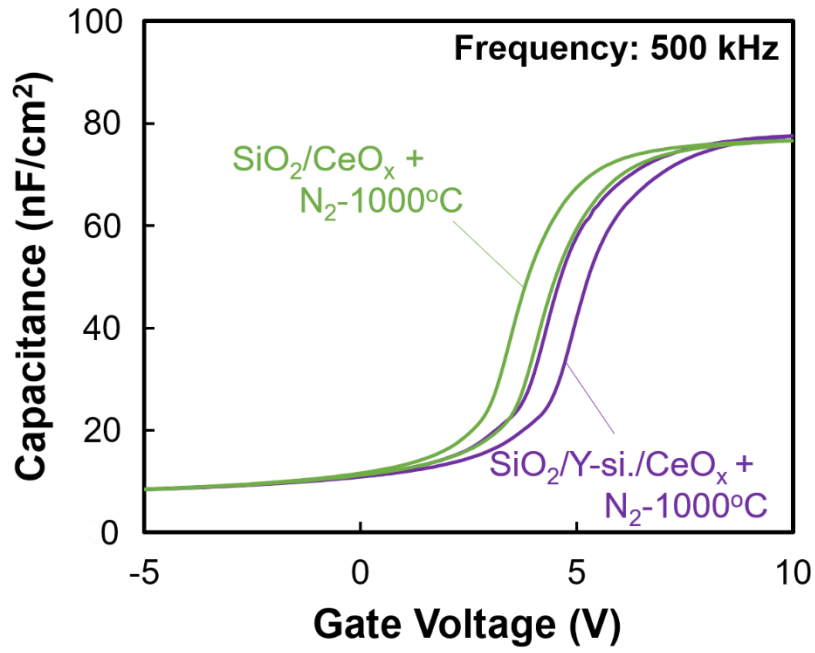
Fig. 6.1.2.1 *C-V* characteristics of MOS capacitors with CeO_x and Y-silicate/CeO_x interface layers after 1000°C annealing for 30 min in N_2 ambient.
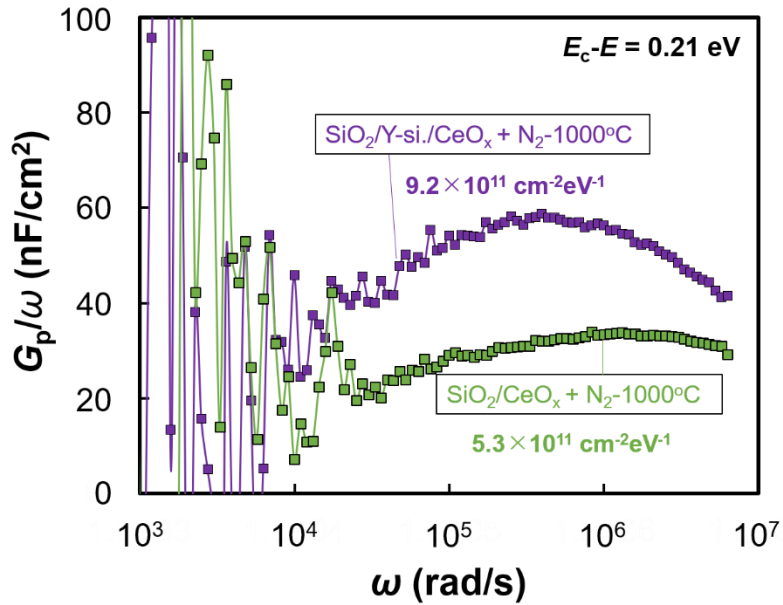

Fig. 6.1.2.2 D_{it} characteristics of MOS capacitors with CeO_x and Y-silicate/CeO_x interface layers by conductance method.

6.2 MOSFET characteristics with stacked interface layer

Fig. 6.2.1 shows the mobility characteristics of MOSFETs with CeO_x/Y-silicate interface layers after annealing at 900°C and 1000°C for 30 min in N_2 ambient. Thicknesses of CeO_x and Y-silicate layer are also 1 nm and 0.6 nm. Peak mobility of 23 cm^2/Vs was obtained with V_{th} of 3.1 V after 900°C annealing, and 19 cm^2/Vs was obtained with V_{th} of 4.2 V after 1000°C annealing. Particularly, the result of 1000°C-annealed sample is completely same to the 1000°C-annealed MOSFET with Y-silicate interface layer for V_{th} and peak mobility as shown in Fig. 4.5.1. From this comparison, there is no effect of CeO_x layer insertion on Y-silicate layer for mobility increase.

Fig. 6.2.2 shows the mobility characteristics of MOSFETs with Y-silicate/CeO_x interface layers after 1000°C annealing for 30 min in N_2 ambient. Although negative V_{th} shift is suppressed from 2.1 V to 3.1 V, a lower peak mobility of 33 cm^2/Vs than 52 cm^2/Vs with CeO_x interface layer is obtained with Y-silicate/CeO_x interface layer. This cannot be attributed solely to the D_{it} increase because the sample of thermally grown SiO_2 with NO annealing showed the peak mobility of 25 cm^2/Vs and the D_{it} of 1.5×10^{11} cm^{-2}eV^{-1}. However, this result clarifies that Y-silicate layer insertion on CeO_x layer degrades a mobility property despite keeping high V_{th}.
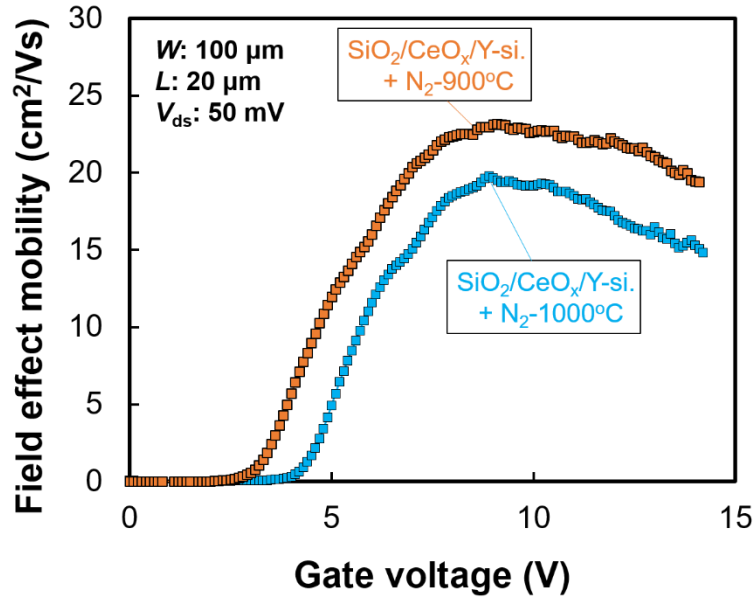
Fig. 6.2.1 Field effect mobility characteristics of MOS capacitors with CeO_x/Y-silicate interface layers. PDA conditions are 900°C and 1000°C for 30 min in N_2 ambient, respectively.
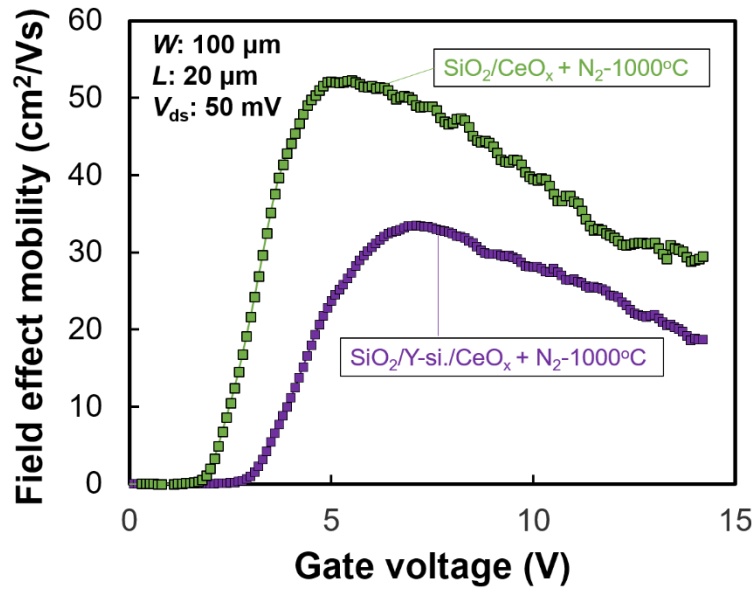

Fig. 6.2.2 Field effect mobility characteristics of MOS capacitors with CeO_x and Y-silicate/CeO_x interface layers after 1000°C annealing for 30 min in N_2 ambient.

6.3 Summary of chapter 6

The electrical characteristics of SiC devices with CeO_x/Y-silicate and Y-silicate/CeO_x interface layers were investigated. Although insertion of Y-silicate layer can suppress negative electrical shift, which interrupted mobility recovery by CeO_x. CeO_x is suitable for SiC interface engineering due to high mobility and suppression of negative electrical shift. However, Y-silicate is also still attractive for large suppression of negative electrical shift and anti-oxidation, which is potential to enhance reliability of SiC devices. Fig. 6.3.1 shows the mobility trend with the results of this chapter.
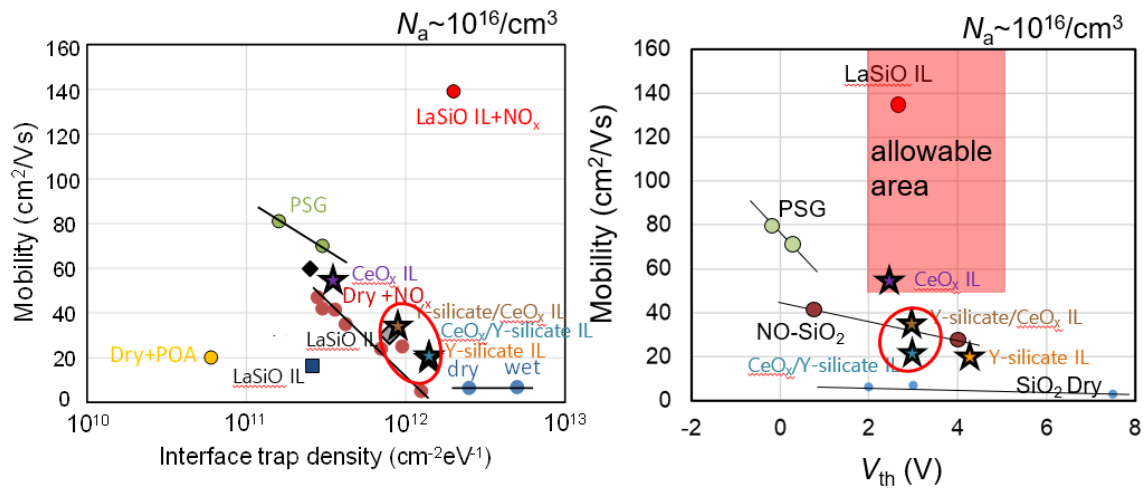

Fig. 6.3.1 Relationship between mobility, D_{it} and V_{th} for CeO_x/Y-silicate and Y-silicate/ CeO_x interface layers.

Chapter 7 Summary and conclusions

7 Summary and conclusions

In this thesis, application of Y-silicate and CeO_x layer was introduced for performance improvement of SiC MOS devices.

In chapter 3, ALD of Y_2O_3 and CeO_x films by Ar boost technology was investigated. High GPC values for stable interface property were obtained in the both films by multi-shot process. Also, low temperature formation of Y-silicate layer was demonstrated by cyclic deposition of stacked-layer of Y_2O_3 and SiO_2.

In chapter 4, an influence of Y-silicate interface layer on electrical characteristics of SiC MOS devices was investigated. Thermal stability of Y-silicate interface layer was confirmed at annealing temperature of 1000°C. Then, suppression of negative electrical shift and small increase of peak mobility from 14 cm^2/Vs to 19 cm^2/Vs were confirmed in MOS devices compared with SiO_2 interface by oxide and interface charge properties of Y-silicate.

In chapter 5, an effect of CeO_x interface layer on electrical characteristics of SiC MOS devices was investigated. CeO_x interface layer was also thermally stable in 1000°C and 1100°C annealing, which induced the SiO_2 growth in ALD-SiO_2 layer by SiC surface oxidation. In addition, the high mobility of 54 cm^2/Vs with the V_{th} of 2.3 V was obtained after 1100°C annealing. Although the D_{it} is still higher than those of the sample with NO-annealed SiO_2, the mobility is 2 times higher and the V_{th} is kept in positive region well. Surface oxidation by radical oxygen can enhance properties of mobility and V_{th}.

In chapter 6, an effect of CeO_x/Y-silicate and Y-silicate/CeO_x stacked interface layers was investigated. The effect for anti-oxidation and suppression of negative electrical shift were demonstrated in Y-silicate layer. However, an insertion of only CeO_x interface layer is the most effective for mobility recovery.

In this study, we confirmed a potential of CeO_x for electron mobility. Although the specific cause of the mobility increase is still unclear, it is considered that radical oxygen caused a different effect on the surface than that of oxygen gas. Fig. 7.1 shows the property of SiC device after surface oxidation with high density O_2 plasma. Surface roughness is hardly existent, which is comparable to initial state after chemical cleaning. In addition, significant low D_{it} of below 10^{11} $cm^{-2}eV^{-1}$ is obtained. Furthermore, this report has mentioned that mobility of 44 cm^2/Vs was obtained with V_{th} of 5 V. O_2 plasma also contains radical oxygen component, therefore, the effect of CeO_x is presumed to be similar to this report.
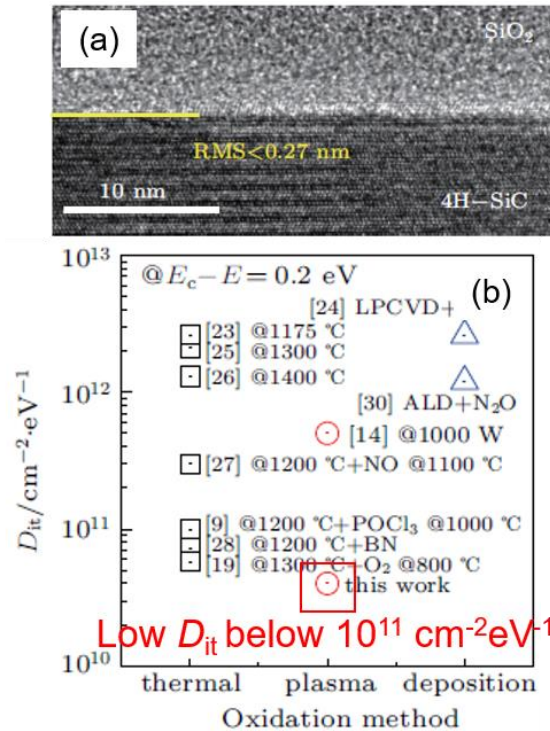

Fig. 7.1 (a) Cross-sectional TEM image of SiO_2/SiC interface after high density O_2 plasma oxidation and (b) its D_{it} characteristic. [7-1]

On the other hand, D_{it} is also related to oxidation temperature. Fig. 7.2 shows the oxidation temperature dependence of D_{it} for SiO$_2$/SiC interface. The D_{it} tends to decrease as the oxidation temperature increases. However, an excessively high oxidation temperature causes a D_{it} increase by rough interface. Compared with this, CeO$_x$ interface layer can reduce D_{it} and increase mobility at low temperature. Therefore, CeO$_x$ has the advantage of not only improving performance but also reducing thermal cost for SiC devices.

The properties of CeO$_x$ interface layer investigated in this study are expected to play an important role in the future of SiC devices. In this study, a peak mobility of 54 cm^2/Vs was reported, but it seems that a higher mobility can be achieved by maximizing the radical oxygen effect. For this effect, CeO$_x$ formation method may be the key to further mobility increase such as thickness variation. In addition, after annealing with SiO$_2$/CeO$_x$/SiC followed by SiO$_2$/CeO$_x$ removal, Y-silicate deposition may lead to high
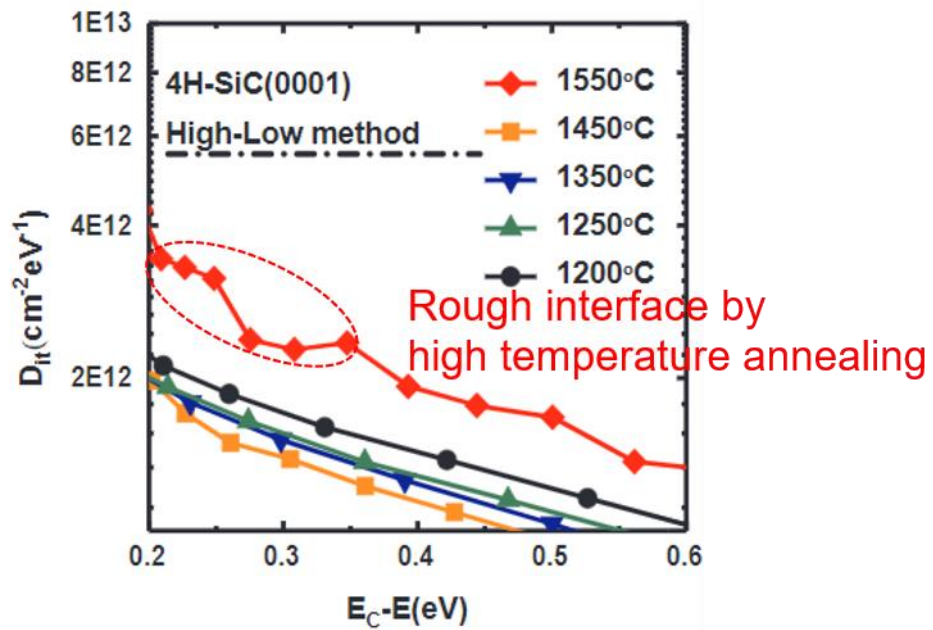

Fig. 7.2 Oxidation temperature dependence of D_{it} for SiO$_2$/SiC interface. [7-2]

mobility and V_{th}. Moreover, it has been reported that D_{it} is significantly decreased below 10^{11} cm^{-2}eV^{-1} with H$_2$ surface etching. [7-3] Add to this, CeO$_x$ deposition after H$_2$ surface etching may achieve a large mobility increase by low D_{it} and sharp interface.

However, there is also a challenge for CeO$_x$ interface layer. As mentioned in chapter 5.2, CeO$_x$ interface layer induced the additional SiO$_2$ growth. Therefore, it is necessary to design the device in consideration of the further growth of SiO$_2$. In addition, this phenomenon is expected to be more critical to trench MOSFET, and there is a concern about formation of a non-uniform dielectrics. To utilize the superior characteristics of CeO$_x$, it is necessary to solve this reliability issue.

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Publications and presentations

Publications (First author)

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[2] Jinhan Song, Atsuhiro Ohta, Takuya Hoshii, Kazuo Tsutsui, Kuniyuki Kakushima "High field-effect mobility with suppressed negative threshold voltage shift in 4H-SiC MOSFET with cerium oxide interfacial layer", Japanese Journal of Applied Physics, 60, 030901 (2021).

Presentation at international conference (First author)

[1] Jinhan Song, A. Ohta, T. Hoshii, H. Wakabayashi, K. Tsutsui, K. Kakushima. "Electrical Characteristics of Atomic Layer Deposited Y-silicate Dielectrics", International workshop on dielectric thin films for future electron device (Tokyo institute of technology, Tokyo, Japan, November 20th, 2019).

Presentation at domestic conference (First author)

[1] Jinhan Song, A. Ohta, T. Hoshii, H. Wakabayashi, K. Tsutsui, K. Kakushima. "Electrical Characteristics of MOS capacitors with SiO_2/Y_2O_3 stacked gate dielectrics by ALD", The 80th JSAP Autumn Meeting, the Japan society of Applied Physics (Hokkaido University, September 19th, 2019).

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