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TOKYO INSTITUTE OF TECHNOLOGY

Embedded Die and Fan-Out Packaging Technologies Enabling High Density and Reliable 2D/3D Integration for System in Package

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A thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy

in the

Department of Electrical and Electronic Engineering

February, 2022

TOKYO INSTITUTE OF TECHNOLOGY

Abstract

Department of Electrical and Electronic Engineering

Doctor of Philosophy

Embedded Die and Fan-Out Packaging Technologies Enabling High Density and Reliable 2D/3D Integration for System in Package

by Kentaro MORI

Moore's law approaches the physical limitations of semiconductor scaling, and advanced system-in-package (SiP) technologies are expected to create new value. With advanced SiPs, improved system-level performance, lower power consumption, smaller size, and lower cost can be achieved by scaling the package-level interconnection pitch and integrating different functional chips into a single package.

This thesis describes novel 2D/3D SiP processes utilized by package-level and wafer-level integrations. First, as package-level integration, a thin package-on-package (PoP) and a reliable embedded high-pin-count large-scale integration (LSI) package based on a coreless substrate are described. Second, as wafer-level integration, a 5-in-1 fan-out wafer-level package (FOWLP) that integrates one logic chip and four memory chips for Internet of Things (IoT) modules, and an innovative 3D fan-out packaging and integration technology with a new photosensitive mold material are described. Finally, a flip chip assembly process with a non-conductive film (NCF) contributes to high-density and reliable through-silicon via (TSV) integration.

This thesis shows that high-density and reliable packaging technologies can be applied to future artificial intelligence (AI) edge computing and large memory modules, and provides a direction for SiP process development.

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February, 2022
Kentaro Mori

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Chapter 1

Introduction

1.1 Semiconductor Industry Status

The greatest invention of the twentieth century, the transistor, was invented in 1947 as a small, high-performance, and reliable electronic device for replacing vacuum tubes [1]. Semiconductors, which have evolved into integrated circuits, have been growing at an exceptionally fast pace for more than 75 years to meet the growing demand for radios, televisions, personal computers (PCs), cell phones, and smartphones [2]. Since the COVID-19 pandemic in 2020, the demand for PCs and tablet devices has increased as people spend more time at home, and the penetration rate of 5G smartphones has increased at almost the same time. These factors have led to a dramatic increase in the volume of data transmission over the internet, and the demand for capital investment in infrastructure, such as cloud services has also increased. In addition, emerging industry trends such as 5G, the Internet of Things (IoT), cyber-physical systems (CPS), artificial intelligence (AI), and autonomous driving will impact the semiconductor industry more than ever. The global market for the semiconductor industry was worth $ 440 billion in 2020, a number which is expected to double by 2030 [3].

The Japanese semiconductor industry had about 50% of the global market in the 1990s. At that time, Japanese semiconductor manufacturers were integrated device manufacturers (IDMs), meaning that they designed, manufactured, and tested their products in one company. Since the 1990s, the miniaturization of integrated circuits has progressed, capital investment has become enormous, and the fabless foundry model, which divides design, manufacturing, and testing, has increased at the expense of the IDM model. Japanese semiconductor manufacturers have been unable to adjust to this change in business model and their market share has dropped to about 10% [4].

1.2 Evolution of Semiconductor Devices and SoC

The expansion of the semiconductor market has been sustained by Moore's law, an index of integration according to which the number of transistors integrated on a semiconductor chip doubles every 18–24 months [2]. Figure 1.1 shows the

application processor (AP) technology node and transistor count in an Apple smartphone (iPhone) [5]. A 16 nm process was used for the iPhone 7 (A10) in 2016, and a 5 nm process was used for the iPhone 12 (A14) in 2020. The number of transistors in an iPhone 12 reached 11.8 billion with a chip size of 88 mm^2. Figure 1.2 shows the relationship between the technology node and the design cost of the AP [5]. The design cost of a 16 nm process was $ 106, whereas that of a 5 nm process was more than five times higher at $ 542. For the current generation of semiconductors, the cost per transistor did not decrease, even with miniaturization.

On the other hand, for recent information and communication technologies (ICT), it is necessary to connect a large processor and large memory at high speed with a wide bandwidth to achieve high-speed computing. System-on-chip (SoC) technology has been used to integrate complementary metal–oxide–semiconductors (CMOS), static random-access memory (SRAM), dynamic random-access memory (DRAM), and other elements within a single semiconductor chip. SoCs have the advantages of miniaturization, high performance, and low power consumption because devices can be connected to each other over a short distance. However, because CMOS and DRAM, which have different manufacturing processes, are made on a single Si wafer, there are disadvantages, such as yield loss, longer development time, and costly design and manufacturing. When the challenges of SoCs became obvious, the roles and functions of electronics packages began to be reconsidered.

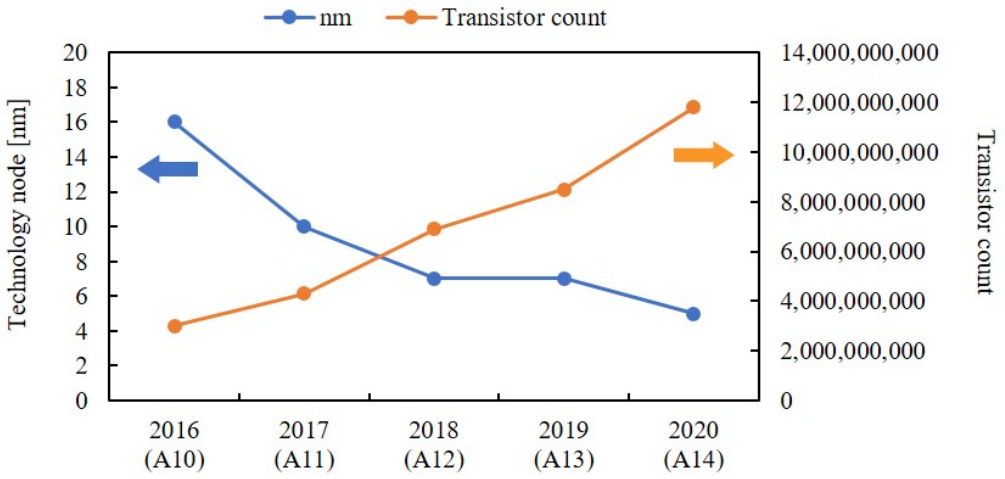


FIGURE 1.1: Technology node and transistor count of iPhone's AP. [5]

1.3 Evolution of Electronics Packaging

Electronics packages have played the roles of electrical connections in signal transmission, chip protection from the external environment, thermal diffusion of heated chips, and help the mounting on printed circuit boards. In addition,

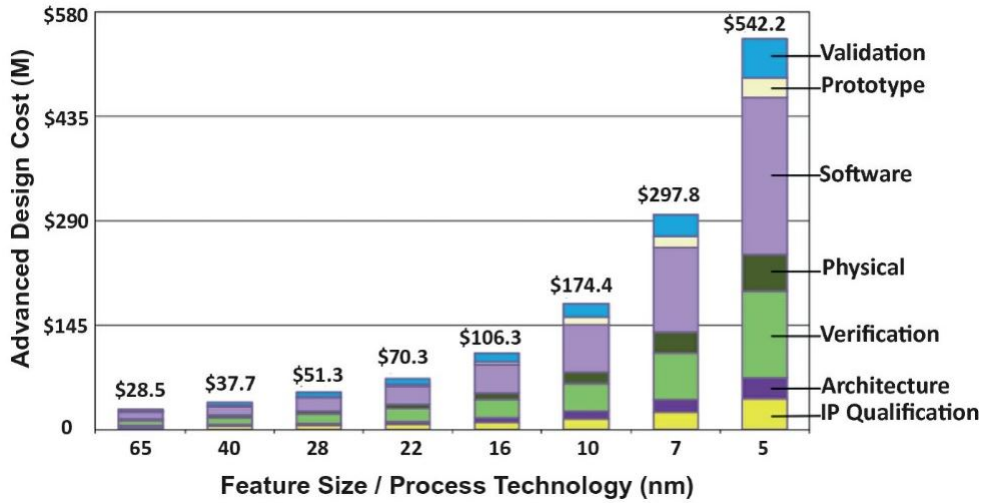


FIGURE 1.2: Design cost versus process technology. [5]

electronics packages have become a technological innovation for high-density, thinner and reliable. In the 1970s, the insertion-type dual in-line package (DIP) with a few dozen pins was mainstream, but from the 1980s, the surface mount became widely used, and the quad flat package (QFP)/ small outline package (SOP) with up to 300 pins was introduced. In the 1990s, a ball grid array (BGA) with area array terminals was introduced to satisfy the demand for more pins. In the 2000s, the wafer-level chip scale package (WLCSP), which was as small as a chip, was developed. In recent years, much attention has been paid to the development of the fan-out wafer-level package (FOWLP), which forms package wiring layers in an area larger than a chip size using a wafer process. Figure 1.3 shows the history of electronics package technology [6]. It can be seen that various types of packages were developed between the 1990s and the 2020s.

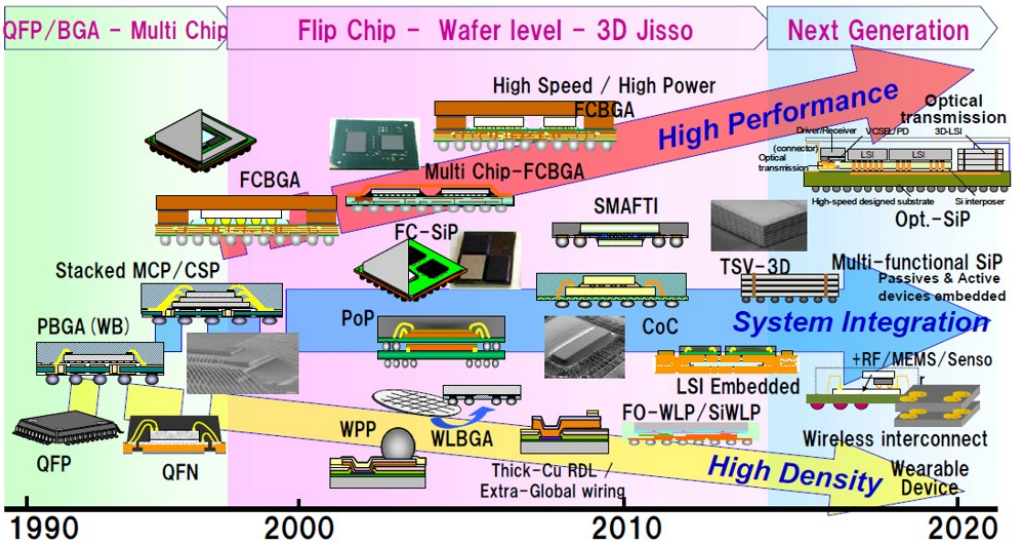


FIGURE 1.3: Pacakge evolution. [6]

1.4 System in Package (SiP)

Electronics packaging has evolved into various types as semiconductor scaling has grown. However, traditional packaging technologies for a single SoC face limitations in terms of system cost and performance. Therefore, the role of assembly and packaging has expanded to include system-level integration functions. This packaging technology is called system-in-package (SiP). SiP is defined as follows [7].

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components and other packages and devices.

Figure 1.4 shows images of a SoC and a SiP. As the scaling of SoCs has approached the physical limits, expectations for SiPs have increased [8], [9]. SoC and SiP have evolved by complementing each other's merits and demerits. Table 1.1 shows a comparative table of SoC and SiP. The main characteristics of SiPs are: system design flexibility, short development time, low cost and large memory capacity. In the 2000s, the main products of SiP were the chip stacked and the package stacked types, which were commercialized for use in mobile products and digital still cameras (DSCs) and contributed to the miniaturization of electronics packages. The performance index of SiP is expressed as follows [10].

$$Performance\ index\ =\ Function\ /\ (Size\ x\ Weight\ x\ Power\ consumption\ x\ Cost) \quad (1.1)$$

While the miniaturization of wiring is important for the front-end processes of semiconductors, the size, weight, power-consumption, and cost are important for SiP. It means that SiPs are required in the entire system to provide higher performance and higher integration.

TABLE 1.1: SoC versus SiP.
✓: pros, × : cons

	SoC	SiP
Power	×	✓
Performance	✓	×
System design flexibility	×	✓
Development time/cost	×	✓
Miniaturization	✓	×
Power consumption	✓	×
Large memory capacity	×	✓

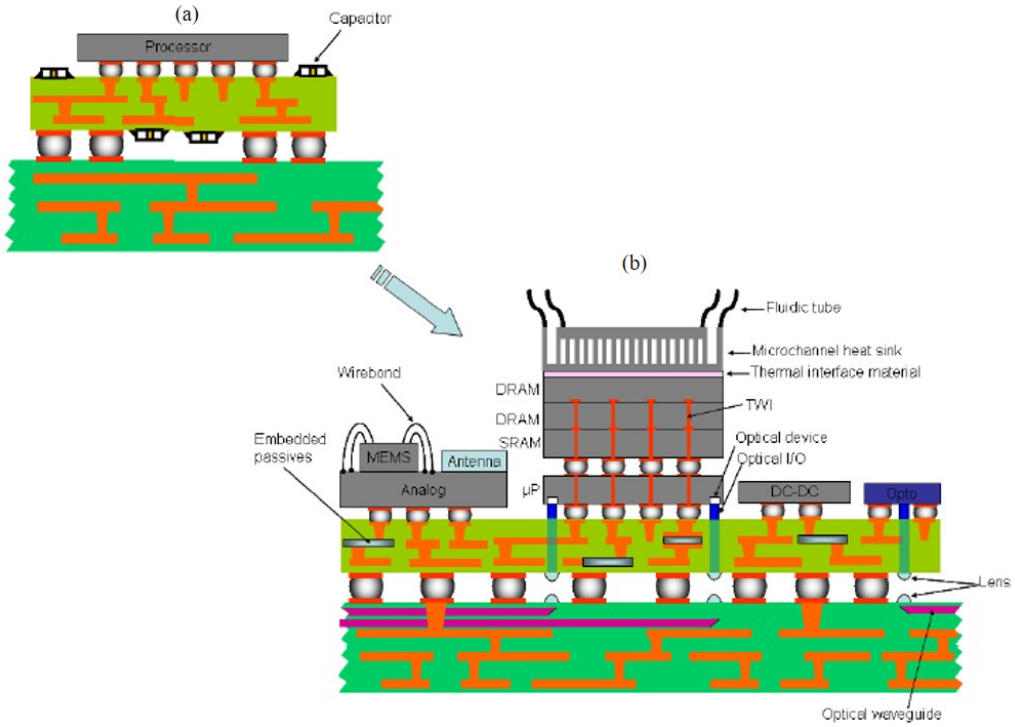


FIGURE 1.4: Package structures. (a) SoC. (b) SiP. [7]

1.5 More than Moore

In 2005, the International Technology Roadmap for Semiconductors (ITRS) suggested two directions for future semiconductor devices: More Moore, which aims to improve the performance by miniaturizing transistors, and More than Moore, which takes a different approach, as shown in Figure 1.5 [11]. More Moore is the continuation of Moore's Law, while More than Moore is the "diversification" of functions in semiconductor technology. More than Moore devices are not necessarily limited to digital circuits but also include analog/radio frequency (RF), passive devices, power devices, sensors, and actuator integration. The fundamental technology for realizing More than Moore is SiP technology, and the evolution of this technology is essential for high performance and functionality in system integration.

1.6 Chiplet Technology and Heterogeneous Integration

SiP technologies contain chiplets and heterogeneous integrations, which are expected to be the key driver for a wide variety of application fields. A chiplet is an integrated circuit block specifically designed to work together with other similar, small chiplets to form a larger, more complex package integration. A chiplet can provide massive yield improvement [12], [13]. Figure 1.6 (a) shows a schematic of a monolithic 32-core processor [13]. The processor has a chip size of 777 mm^2 using a 14 nm process. Figure 1.6 (b) shows the schematic of a 4 × 8-core chip. Each chiplet has a chip size of 213 mm^2 using a 14 nm process, for a total chip area of 852

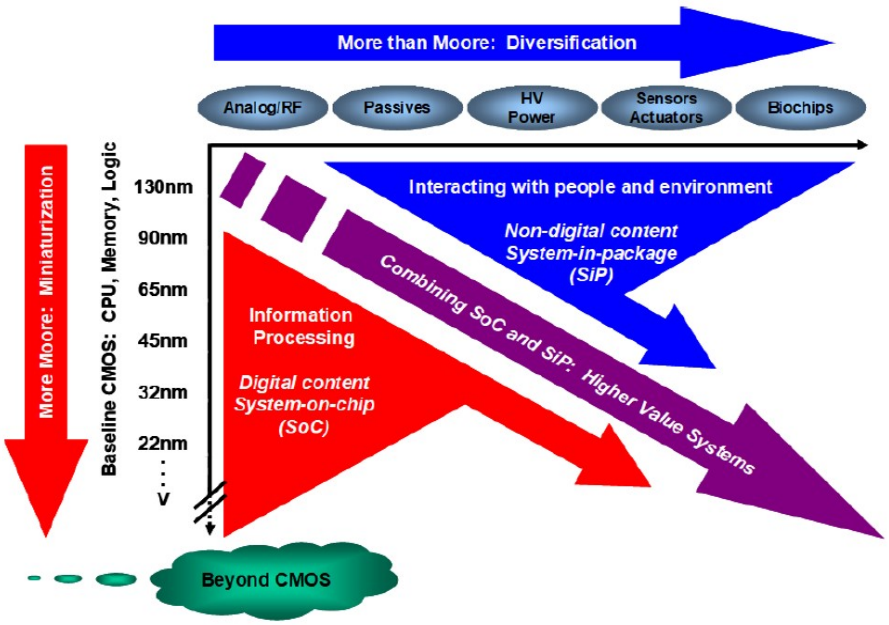


FIGURE 1.5: "More than Moore" and "More Moore". [11]

mm^2. The final cost of this quad-chiplet design is only approximately 0.59 that of the monolithic design, even though it uses approximately 10% more silicon.

Heterogeneous integration technology enables system scaling with better cost-performance by placing logic, memory and sensor horizontally or vertically to integrate a SiP [14], [15]. It also allows for the flexible design and integration of heterogeneous chips with different technology nodes, materials, functions, and chip sizes to achieve novel 2D/3D integration. These have been studied using various package structures.

1.7 Intermediate Process

The intermediate process in semiconductor manufacturing is between the front-end and back-end processes. The front-end process includes the front-end-of-line (FEOL), which forms the device, and the back-end-of-line (BEOL), which forms the multilayer interconnect, whereas the back-end process includes chip assembly and testing. The scope of the intermediate process is generally from the completion of the BEOL to the start of the chip assembly. Intermediate process is not a standardized name, and even among semiconductor manufacturers, there is a difference in opinion as to whether the intermediate process belongs to the front-end or back-end processes. The importance of intermediate processes is increasing every year because of Moore's approach to physical limits and the expectation of More than Moore.

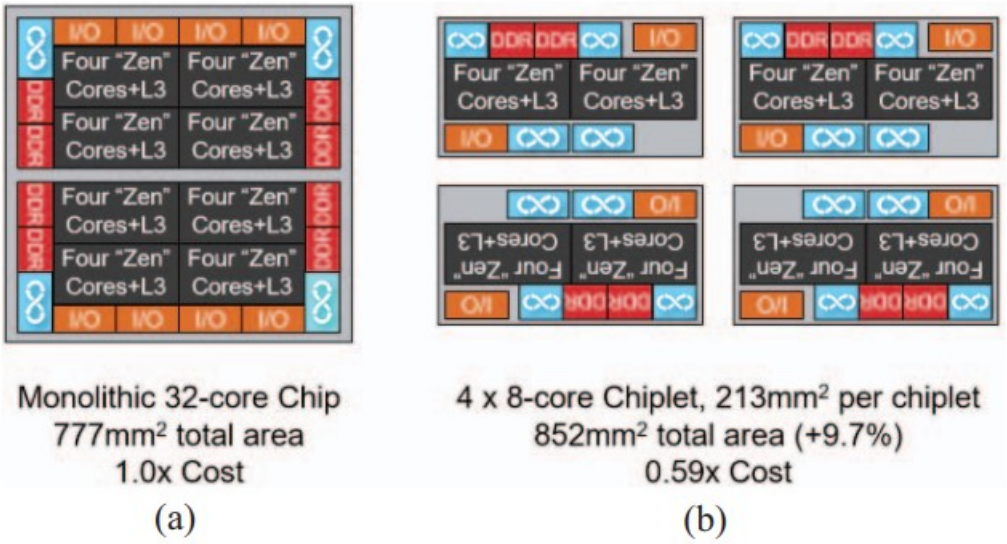


FIGURE 1.6: Cost comparison of (a) monolithic and (b) chiplet. [13]

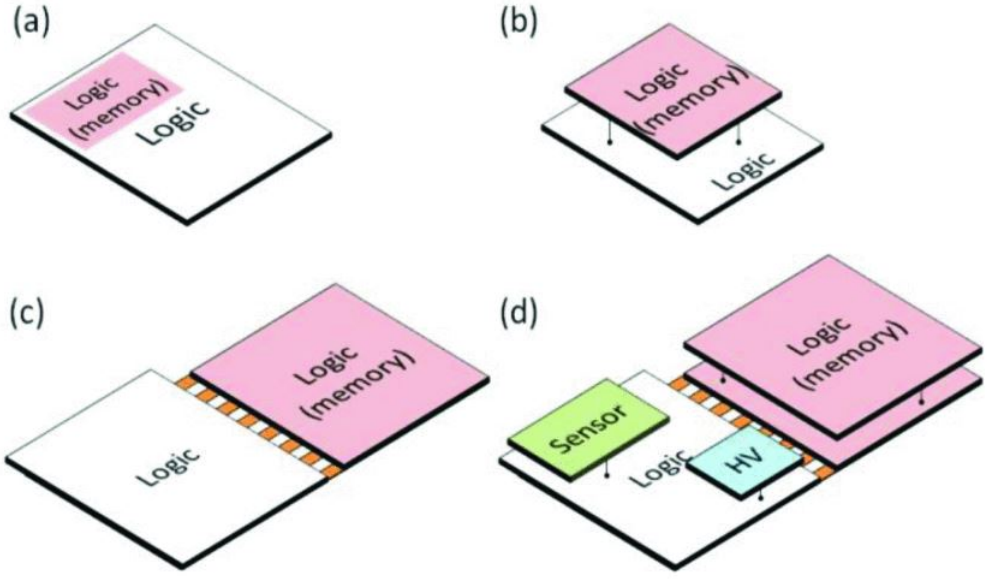


FIGURE 1.7: Schematic of SoC and SiPs. (a) SoC. (b), (c), (d) Heterogeneous integration. [14]

An overview of the intermediate process is provided using 3D/TSV, a type of SiP, as an example. Figure 1.8 shows the 3D/TSV process flow [6]. In this 3D/TSV structure, the TSV formation process is added between the FEOL and BEOL (Figures 1.8 (a)-(c)). This process is called the "Via Middle" process of the TSV manufacturing method. After the completion of BEOL, Cu posts (Cu pillars) are formed on the surface of the electrodes using redistribution layer (RDL) technology with a photosensitive dielectric material and electroplating (Figure 1.8 (d)). The height of the Cu posts was 30–50 μm, and the solder for the interconnection was formed on the upper layer of the Cu posts. Subsequently, the device was bonded to the support substrate with an adhesive at the wafer level (Figure 1.8 (e)), and then, Si back grinding, TSV exposure, and backside electrode formation were performed (Figures 1.8 (f) and (g)). The Si thickness after Si back-grinding was <50 μm. The TSV had a diameter of <ϕ10 μm and a pitch of <40 μm. After tape mounting, the support substrate was removed, and the thin device wafer was diced into chips (Figures 1.8 (h) and (i)). It goes without saying that the development of this new technology, the intermediate process, has increased the added value of electronics packaging. Figure 1.9 shows trends for the technology node and interconnection pitch of a semiconductor package substrate between 2005 and 2020 [16]. There is a technology gap of approximately 1000 times between the two technologies. Development of intermediate process technologies is expected to fill this gap. The trend of finer pitch connections in semiconductor package substrates since 2015 is assumed to be due to the commercialization of new SiPs, such as 2.5D and FOWLP using the intermediate process. Process integration of the FEOL/BEOL/intermediate in the wafer and co-design, including packaging and assembling, is important to achieve higher performance, more functions, and higher device reliability.

1.8 SiP Types

Many different types of SiPs have been proposed for integrating multiple chips, such as logic and memory chips. Each process and structure has unique characteristics and products are expected to be segregated by function, performance, and cost. Further advances are expected by integrating different elemental technologies. Five major SiPs are described in the following sections.

1.8.1 Si Interposer

The demand for high-density integration of logic (FPGAs, CPUs, and GPUs) and high-bandwidth memory (HBM) is increasing, especially in servers. For this connection between logic and memory, 2.5D integration is used, whereby multiple chips are assembled on a silicon interposer with TSV without active elements (Figure 1.10) [17]. A feature of silicon interposers is that they use the BEOL process. The minimum wiring width/spacing of silicon interposers currently in use is 0.4 μm/0.4 μm, which therefore cannot be manufactured according to the design rules

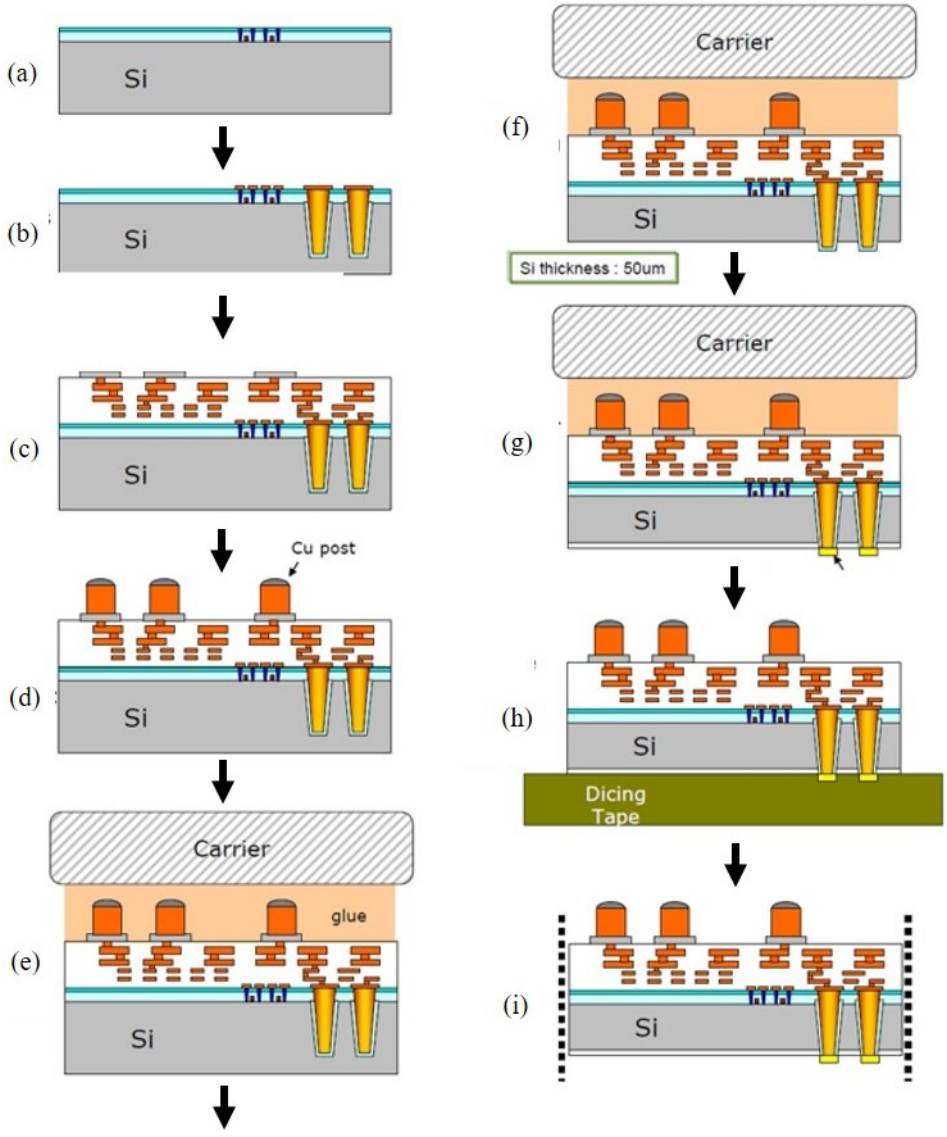


FIGURE 1.8: Via middle process flow. (a) FEOL process. (b)TSV formation (via middle). (c) BEOL process. (d) Cu post formation. (e) temporary bonding. (f) Si back grinding. (g) rear bump formation. (h) tape mouting and debonding. (i) dicing. [6]

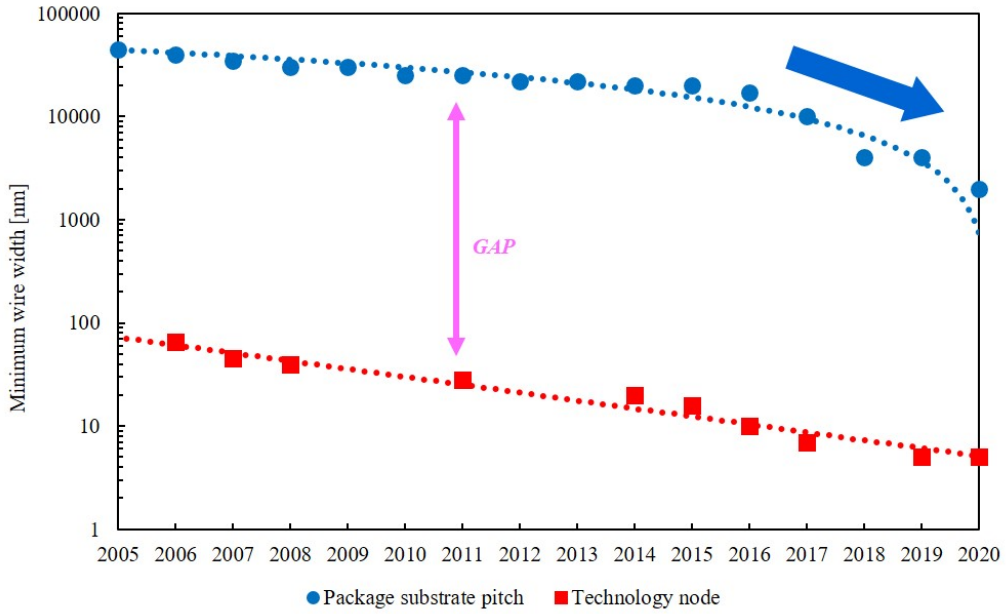


FIGURE 1.9: Gap between technology node and package substrate pitch. [16]

of conventional package substrates. This fine wiring is advantageous in terms of latency and power consumption. However, the size of a silicon interposer needs to be larger than the total area of logic and memory, which results in low acquisition efficiency and low yield for ϕ300 mm wafers. Furthermore, the TSV formation process is still very expensive; therefore, many challenges remain before silicon interposers can be generalized.

1.8.2 High Density Package Substrate

High-density package substrate technology is an extension of the traditional organic package substrate and is characterized by RDL formation on the chip mounting surface, which requires very precise design rules. The minimum wiring width/spacing for RDL is 2 μm/2 μm, and the number of wiring layers is 5. The name of the technology differs, depending on the RDL formation method. It is called 2.1D when the RDL is formed using the normal RDL process [18], and 2.3D when the prefabricated RDL is transferred onto the package substrate [19]. Figure 1.2 shows a comparison table between 2.1D and 2.5D. The 2.1D has the goal of achieving the same performance as the 2.5D at a lower cost without using TSVs. The organic interposer for 2.3D is mounted on a build-up substrate. The bonding process between the organic interposer and the build-up substrate is applied using a pre-applied non-conductive film (NCF) and copper pillars (Figure 1.11). These package-substrate technologies have the potential of spreading rapidly because conventional chip assembly processes can be applied.

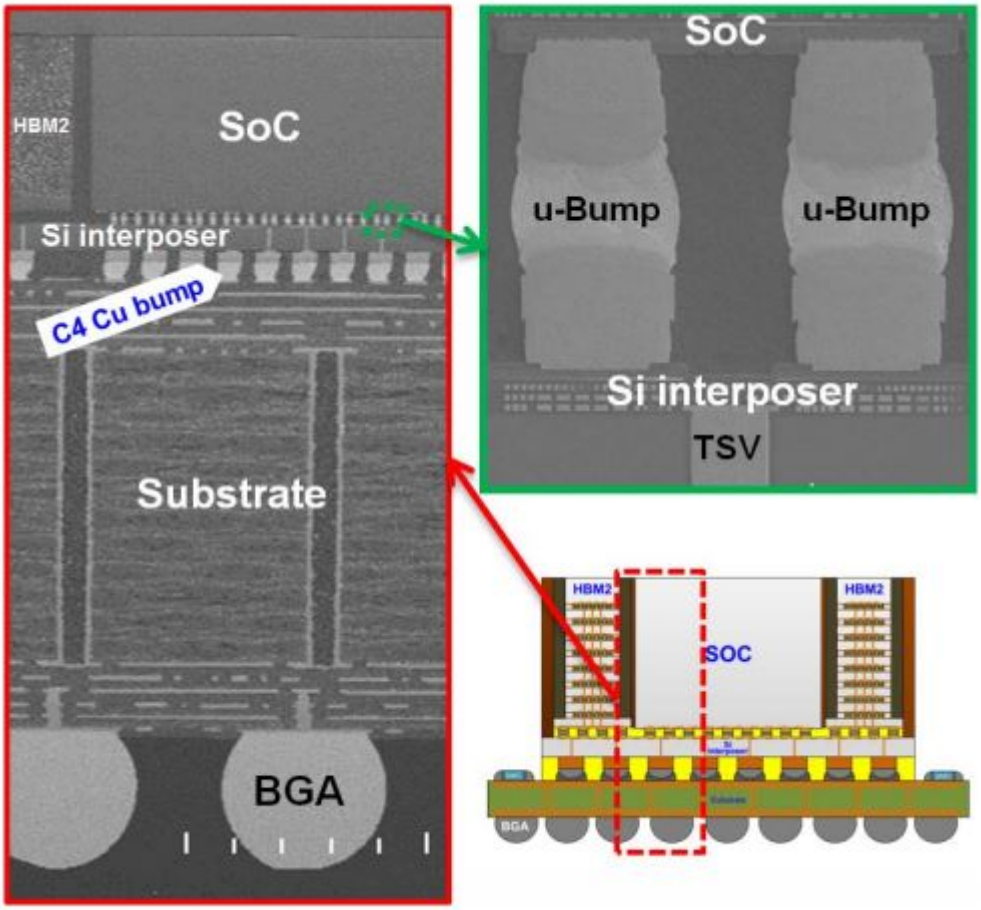
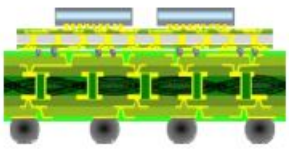
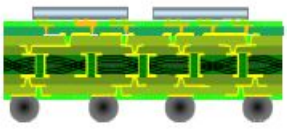


FIGURE 1.10: Cross-sectional image of Si interposer. [17]

TABLE 1.2: Comparisson of 2.5D and 2.1D Package. [18]

Items	**2.5D**	**2.1D**
Schematic diagram		
Production style	Wafer mainly	Panel
Cores	Si interposer, Laminate core	Laminate core
Through via	TSV, TLV	TLV
Weight	Heavier	Lighter
Mechanical strength	Stronger	Weaker
Cost	Expensive	Lower
I/O	Massive	Less

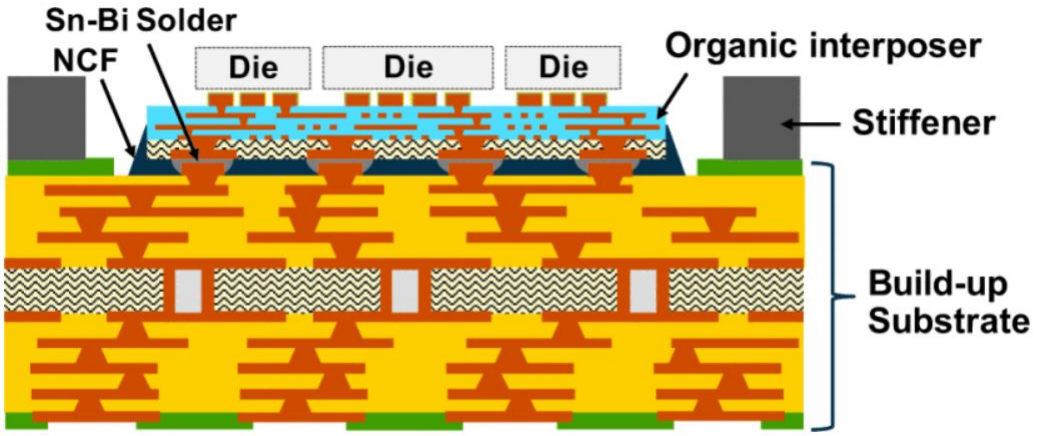


FIGURE 1.11: Schematic of the 2.3D architecture. [19]

1.8.3 Embedded Die

In this package, a package substrate with small embedded silicon interposers is used. These interposers did not have any TSVs. Multiple devices are mounted on the package substrate, and the electrical connections between devices are made through silicon interposers embedded into the package substrate (Figure 1.12) [20]. These small Si interposers are known as bridge dies. A bridge die is made using the BEOL process and has a minimum interconnection width and spacing of 0.4 μm/0.4 μm. There is a cost advantage to placing small micro-interconnects as components only where they are needed and enables high-density interconnects without requiring TSVs.

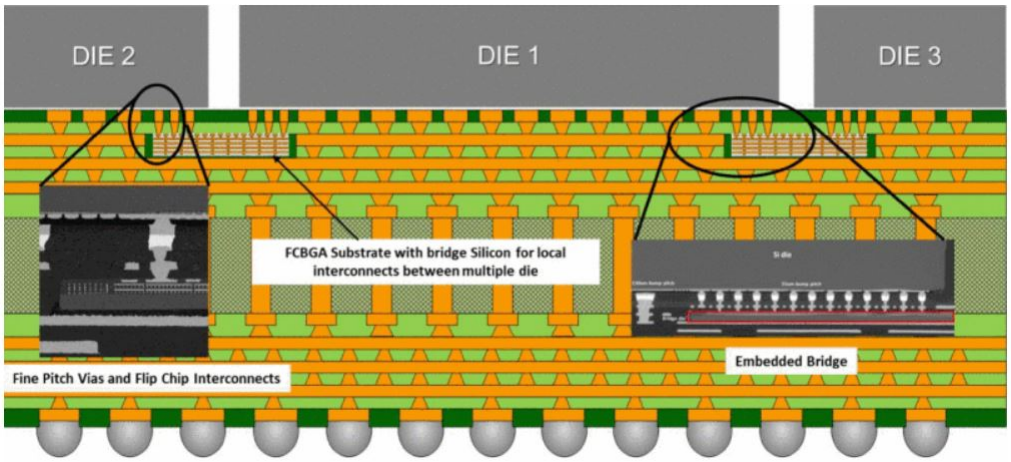


FIGURE 1.12: Schematic of the bridge die architecture. [20]

1.8.4 RDL Interposer

An RDL interposer is also called a fan-out wafer-level package (FOWLP) [21]. While the wiring layer of a silicon interposer is manufactured using the BEOL process, the wiring layer of an RDL interposer is manufactured using the RDL process with a

photosensitive dielectric material and Cu plating without CMP. First, after the chip is mounted on the support substrate, it is encapsulated with mold resin, and then, the support substrate is removed to fabricate the reconstituted wafer, as shown in Figure 1.13. RDLs are then formed on the chip electrode terminals, with a minimum wiring width and spacing of 2 μm/2 μm, with three layers being the most common. In addition, various manufacturing methods have been developed to achieve high yields and densities. Panel-level packages that use a large square support substrate have been aggressively developed for RDL interposers with the goal of reducing manufacturing costs.

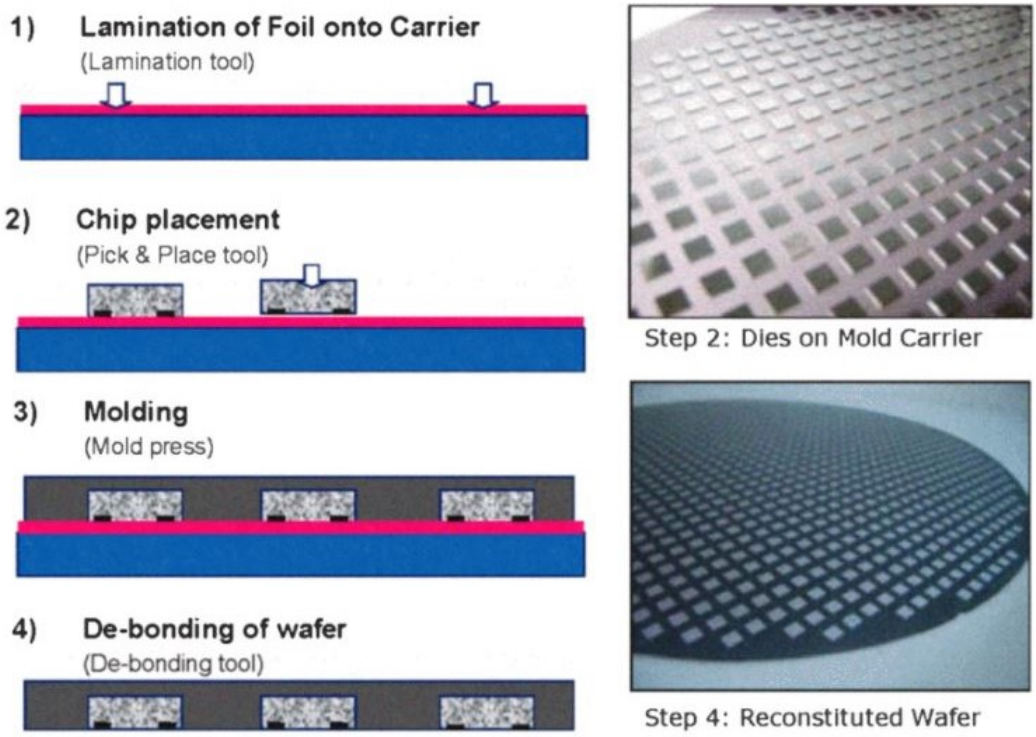


FIGURE 1.13: Process flow of FOWLP. [21]

1.8.5 3D/TSV

The 3D/TSV is a package with a large-capacity DRAM mounted on the backside of a logic chip with TSV formation (Figure 1.14) [22]. In addition, it is expected to have a lower profile than conventional PoP of the package stacking type. In addition, transmission of 3D/TSV only happens in the vertical direction, and its power consumption and latency performance are expected to be significantly better compared with other SiPs. Unfortunately, though, the cost of TSV formation on logic chips and the heat dissipation of stacked chips are unresolved issues. However, if the aforementioned issues can be resolved, this will become the most promising high-performance SiP.

The five SiP technologies mentioned above are summarized in Table 1.3.

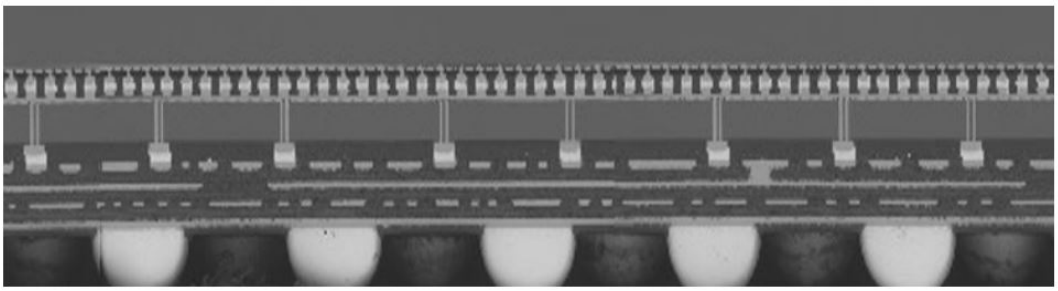


FIGURE 1.14: Cross-sectional image of the face-to-face stacked logic dies connected to package through TSVs. [22]

TABLE 1.3: SiP technologies comparison.

	Traditional	Si interposer	High density package substrate	Embedded Die	RDL interposer	3D/TSV
	MCM	2.5D	2.1D/2.3D	Bride die	Fan-out	
Key Technology	PKG sub.	TSV	PKG sub.	PKG sub.	RDL	TSV
Bump pitch [um]	150	40	40	40	40	-
Line / Space [um]	15 / 15	0.4 / 0.4	2 / 2	0.4 / 0.4	2 / 2	-
TSV	No Need	Need	No Need	No Need	No Need	Need
Package Sustrate	Need	Need	Need	Need	No Need	Need
Wiring process	Pacakge	BEOL	RDL	BEOL/RDL	RDL	BEOL/RDL
Interconnection	C4	ubump	ubump	ubump	Cu plating/ ubump	ubump
Manufacturing cost	Low	High	Medium	Medium	Medium	Very High

1.9 Thesis Focus and Organization

In this thesis, a novel 2D/3D SiP with a unique structure and process that achieves high density and reliability was fabricated using a package-level and wafer-level process integration, with the purpose of solving each issue of traditional SiPs. Figure 1.15 shows an image of the target process of this thesis, which includes an intermediate process, package substrate process and chip assembly.

Figure 1.16 shows the structure of this thesis. In the study of package substrate process technology, a coreless substrate was first adopted for the thinner package of a package stacking structure, and the improvements in electrical characteristics and reduction in package height were evaluated. Next, an actual device chip with a high pin count was embedded in the package substrate, and the reliability of the connection between the chip and the package substrate and the operation of the device were evaluated. In the intermediate process technology, one logic chip and four memory chips were integrated into a single side-by-side package using a low-elasticity mold, and subsequently, the device operation was evaluated. Next, a new photosensitive mold was developed for package stacking, and package reliability was evaluated. Finally, in the chip assembly technology, the chip connection technology for the chip stacking structure was optimized using logic with TSV and high-capacity memory, and the device operation was analyzed.

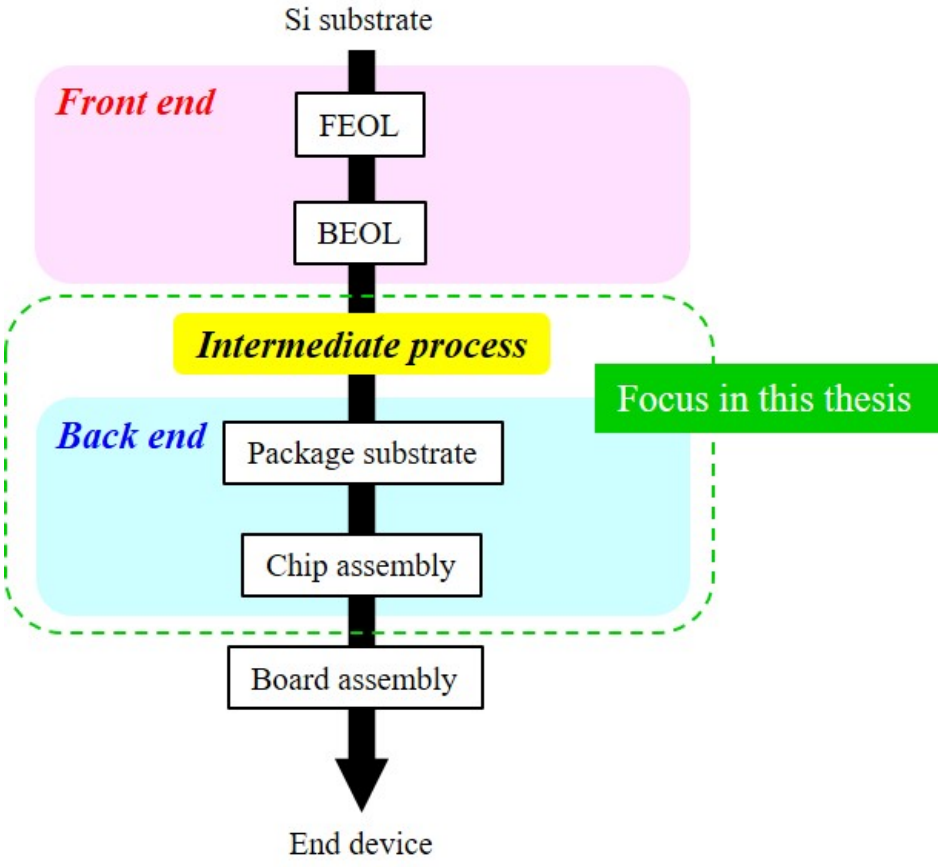


FIGURE 1.15: Focus process of the thesis.

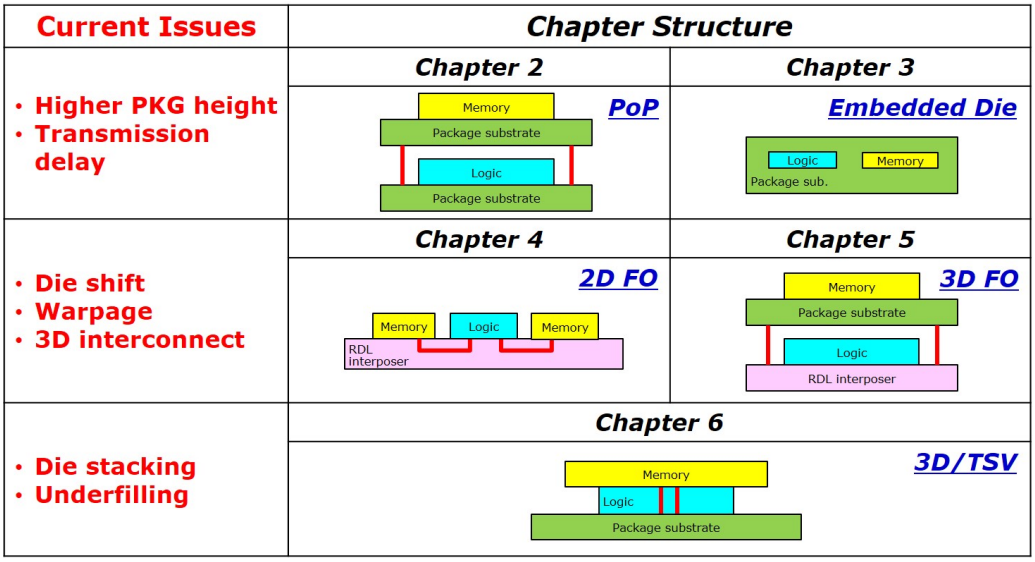


FIGURE 1.16: Chapter structure of the thesis.

Chapter 2

A Package-on-Package Technology using Coreless Substrate with Cu Posts

2.1 Background

Three-dimensional packaging is an attractive approach to miniaturization and high-density component integration for electronic devices, specially for mobile computers, mobile phones and digital cameras. The package-on-package (PoP) assembly technology, in which a memory component is stacked on top of a logic processor, saves a significant amount of motherboard space and increases the combinatorial flexibility of component assembly, and has excellent quality assurance compared with chip-stacking structure [23]–[26]. However, the PoP is thicker than a chip-stacked structure, as shown in Figure 2.1. Therefore, using a thinner interposer substrate to reduce the total package height increases the likelihood of package warpage due to reduction of rigidity.

In a conventional PoP assembly, the top and bottom packages are molded differently. The top one is completely molded, and the bottom one is molded only in the chip mounting area. They thus have different warpage characteristics during solder reflow process because of coefficient of thermal expansion (CTE) mismatch issue. Therefore, controlling the warpage of the two packages is critical for achieving high PoP assembly yield [27]–[31]. Furthermore, in a conventional PoP assembly, the two packages are connected at their peripheries by solder balls under the top package. This limits the potential reduction in assembly height because their ball diameter must exceed the thickness of the chip in the bottom package, as shwon in Figure 2.1 (b).

One approach to overcome these problems is to make the bottom package completely molded as well; this enables the use of smaller solder balls under the top package, resulting in a thinner assembly and finer integration of the two packages. From the above background, several such next-generation PoP assemblies have been developed.

A previously developed ultra-thin coreless substrate is fabricated by completely removing the Copper (Cu) plate after forming a high-density build-up wiring structure on the plate [32]–[34]. The coreless substrate realizes not only the package substrate thickness reduction but also the superior electrical characteristics [35]. A developed thinner bottom package uses this coreless substrate and built-in Cu posts as external terminals [36], [37]. Its substrate is molded using an appropriate resin for the peripheral area as well as for the chip mounting area. This overmolded structure should have less warpage in not only the chip mounting area but also in the peripheral area.

In this chapter, I describes the effect of the wet etching technology used to etch the Cu posts. I also describe a prototype of this thinner bottom package and discuss the warpage and reliability of a PoP assembly with this thinner bottom package.

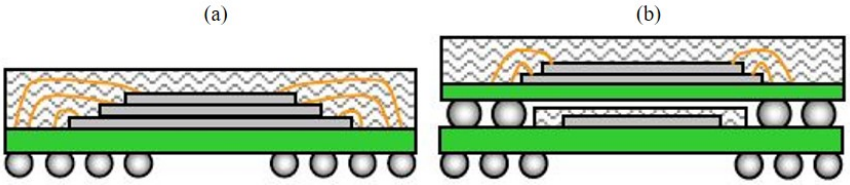


FIGURE 2.1: Three-dimensional package structures. (a) chip-stacking. (b) package-stacking (Package-on-Pacakge).

2.2 Structure and Fabrication

Figure 2.2 shows the fabrication process for the developed bottom PoP package. Firstly, a coreless substrate (one without a rigid core laminate) is replicated on a Cu base plate (Figure 2.2 (a)). In general, the base plate is then removed, leaving only the coreless substrate. However in this study, Cu posts are formed by selective wet etching of the base plate at the end of the substrate fabrication process (Figure 2.2 (b)). Since the post material comes from the base plate, this process is a cost-effective approach to accurately the interposer substrate compared with expensive tall Cu pillars which requires thick film resist patterning and long plating time [38]. Next, the chip is mounted on the side with the Cu posts, and has the interconnection to the coreless substrate with solder bumps or wire bond (Figure 2.2 (c)). The substrate is then completely overmolded (Figure 2.2 (d)). The top surfaces of the posts are exposed by grinding the molded resin, and become the connection terminal to the top package (Figure 2.2 (e)). Finally, solder balls are mounted on the side opposite that with the posts (Figure 2.2 (f)). This package has two significant advantages: it is thinner due to the use of an ultra-thin coreless substrate, and it has the possibility of low warpage due to the use of an overmolded structure.

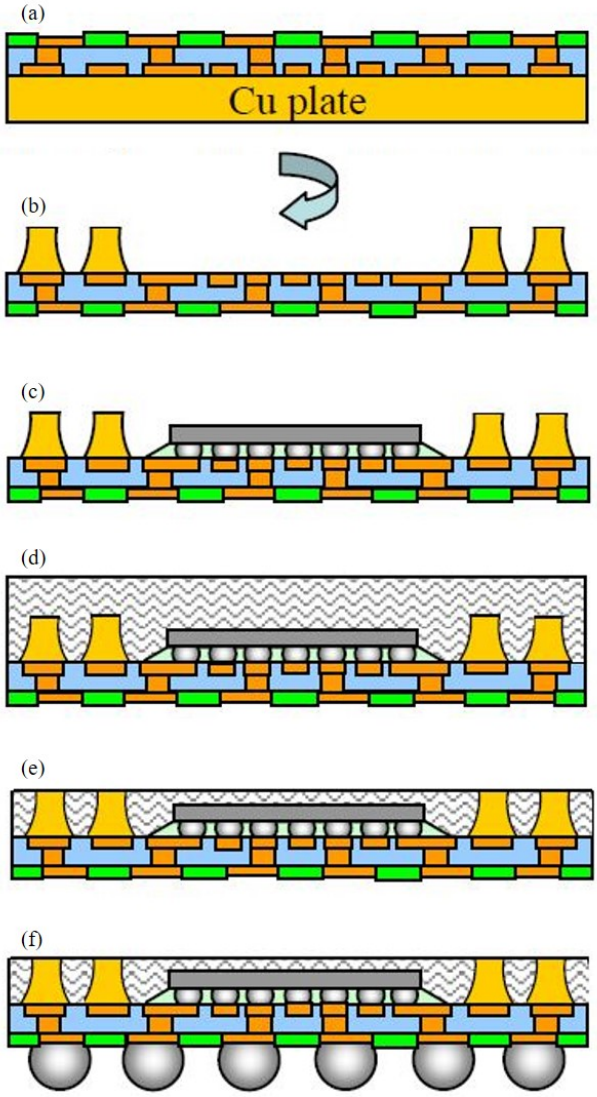


FIGURE 2.2: Target process flow for novel package. (a) multi-layer structure formation on Cu plate. (b) Cu posts formation by Cu plate etching. (c) chip mounting. (d) molding resin formation. (e) molding resin grinding. (f) BGA formation.

2.3 Copper Wet Etching

The Cu base plate was wet etched by spray etching, which is the industry standard for patterning Cu wiring on printed circuit boards. The spray etching of the Cu causes a corrosion reaction in which the metal is oxidatively dissolved. An ammoniacal alkaline solution manufactured by Meltex Corporation was used as the etchant, and the etching reaction can be represented schematically as

$$Cu + Cu(NH_3)_4Cl_2 \rightarrow 2Cu(NH_3)_2Cl \tag{2.1}$$

where the Cu is oxidized and dissolves in the solution. The $Cu(NH_3)_4Cl_2$ is the oxidant, and the $Cu(NH_3)_2Cl$ is a reaction product that does not contribute to the Cu dissolution. Therefore, it is necessary to remove the $Cu(NH_3)_2Cl$ promptly to achieve efficient etching. The posts are formed by spray etching of the area where the etching mask is not formed on the surface of the Cu plate. However, the etchant not only dissolves Cu in the vertical direction, but it also dissolves Cu in the horizontal direction. Thus, the top diameter of the posts formed by wet etching becomes smaller than the bottom diameter because of "side-etching".

Figure 2.3 illustrates the process used to etch the posts. It is necessary to decrease the side-etching since it can negatively affect the narrower pitch and higher aspect ratio of the Cu posts. One purpose of this study is to investigate ways to reduce the side-etching. Spray etching experiments were performed with different values for the etching parameters: spray pressure, etchant temperature, spray direction, and mask shape. Table 2.1 shows the ranges of parameter values. The etching mask was of 10-μm-thick nickel formed by pattern plating. The Cu plate was a 0.5-mm-thick Cu alloy (Cu:99.87%, Fe:0.10%, P:0.03%). The posts were examined using an optical microscope as they were being etched and after etching. Etching depth "D", side etching distance "R", top diameter "T", bottom diameter "B", and height "H", as shown in Figure 2.3 were measured to calculate the etch factor (EF). The EF is the ratio of the etching depth to the side etching distance. The EFs of during and after formation are defined by the following formulas 2.2, 2.3. An increase in the EF means a decrease in the side etching distance. Therefore, the EF should be large to fabricate fine-pitch posts.

$$EF = D/R \tag{2.2}$$

$$EF = 2H/(B - T) \tag{2.3}$$

TABLE 2.1: Spray etching parameters.

Spray direction	up ward, downside
Spray pressure [kgf/cm^2]	0.75-3.0
Temperature [°C]	30-50

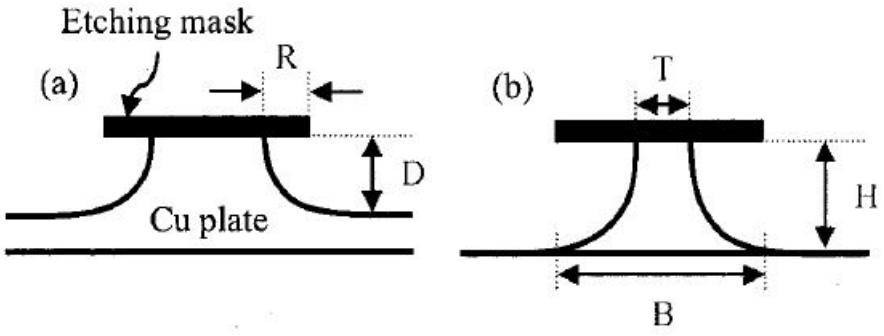


FIGURE 2.3: Schematic of etch factor. (a) Cu post formation in progress. (b) after Cu post formation.

0.5-mm-thick Cu posts were experimentally formed under conditions listed in Table 2.2 to examine the process of EF. Top and cross-sectional views of the posts are shown in Figures 2.4 and 2.5, respectively. The posts were formed after 923 sec of etching as shwon in Figure 2.4 (e) and Figure 2.5 (e). A 10-μm-thick polyimide was used as a base-layer for the Cu posts. Figure 2.6 shows the relationship between the etch factor and the etching time. The EF before etching post formation gradually decreased from 1.7 to 1.5. This indicates that side etching is in progress. After formation, it rapidly increased as the lower layer became exposed and the bottom of the posts was etched preferentially. The EF of the Cu post after 923 sec was 2.2 while the EF of the Cu post after 994 sec was 3.6. As stated before, the larger EF is more effective for Cu post miniaturization. However, as the spray etching process time becomes longer, the top diameter of the Cu post becomes smaller, which may lead to defective connection to the upper package. Therefore, it is important to determine the spray etching processing time by considering not only the EF but also the top diameter of the completed Cu post. From the above evaluation results, the processing time and EF tendency to form 0.5-mm-thick Cu posts were clarified.

TABLE 2.2: Conditions for etch factor experiment.

Spray direction	downside
Spray pressure [kgf/cm^2]	1.5
Temperature [°C]	50
Mask shape	Square
Mask diameter [μm]	1200
Mask pitch [μm]	1250

2.4 Etching Technologies for Cu Posts

2.4.1 Spray Etching

One purpose of this study is to examine how to decrease the side-etching while the Cu posts are being formed. Therefore, the optimization of the wet etching process, especially spray etching was examined. The parameters examined were spray

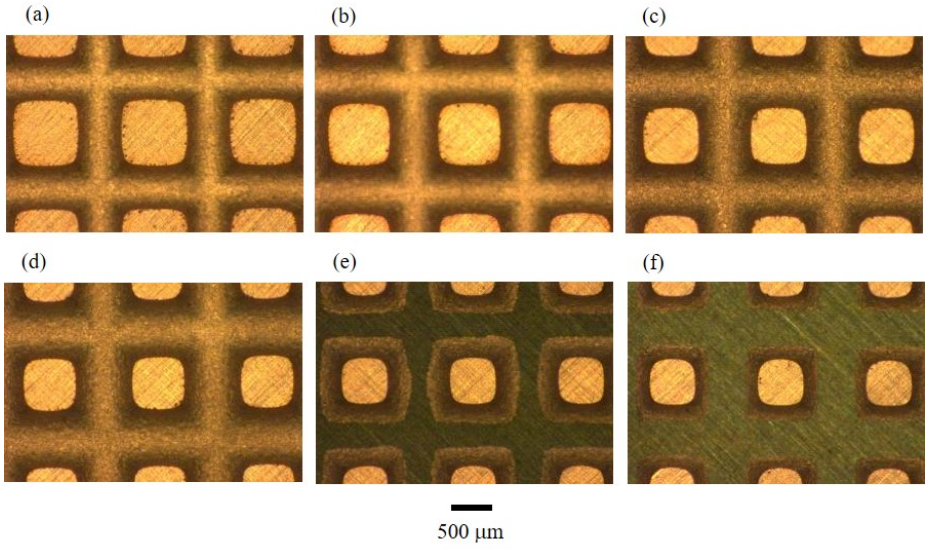


FIGURE 2.4: Top view of posts during and after formation. (a) 639 s. (b) 710 s. (c) 781 s. (d) 852 s. (e) 923 s. (f) 994 s.

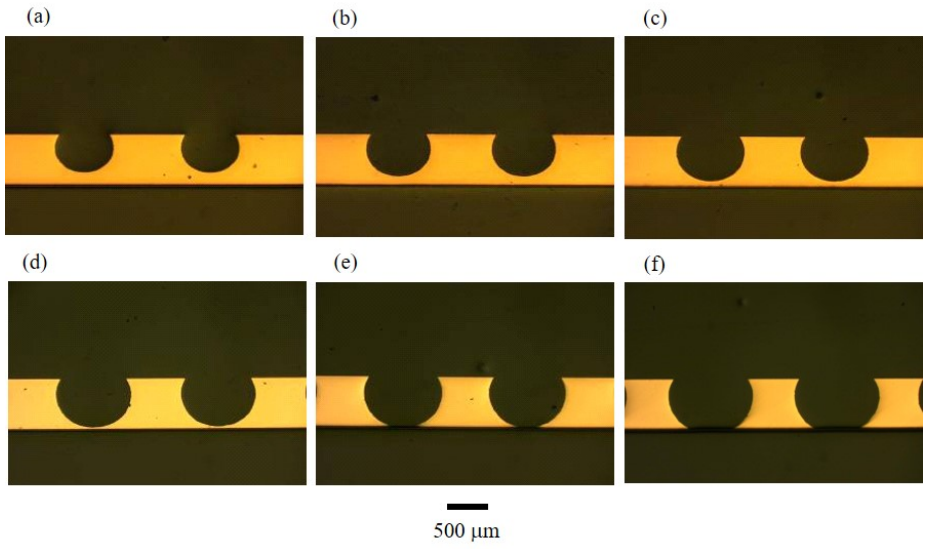


FIGURE 2.5: Cross-sectional view of posts during and after formation. (a) 639 s. (b) 710 s. (c) 781 s. (d) 852 s. (e) 923 s. (f) 994 s.

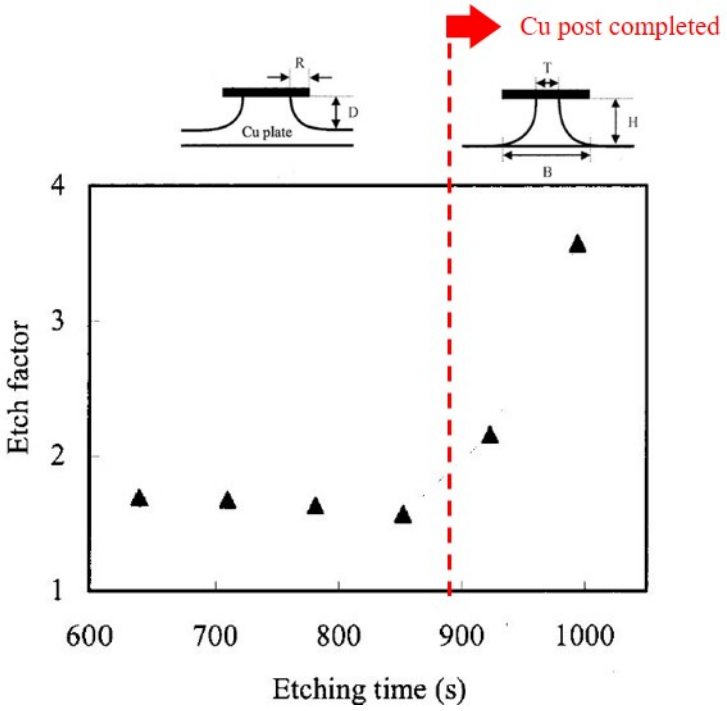


FIGURE 2.6: Relationship between etch factor and etching time.

direction, spray pressure, temperature and etching mask pitch. The etching mask was of 10-μm-thick nickel formed by pattern plating. As a result, spray direction and etching mask pitch were found to deeply influence the side etching. The side etching could be decreased by jetting a Cu etching solution from the downside under the condition that the etching area faces downward, and by narrowing the etching area by making the etching mask pitch smaller. The directions of jetting the etching solution from the upside and the downside are shown in Figures 2.7 and 2.8. For the same etching mask, the amount of side etching is about 15% different depending on the direction in which the etching solution is jetted. The decrease in the side etching is considered to be due to the following reasons:
The amount of etching liquid remaining on the surface of the Cu plate is decreased by jetting the etching solution from the downside.
The amount of etching solution injected in the direction horizontal to the Cu posts is decreased by jetting in a narrow etching area.

The optimized spray etching conditions are shown in Table 2.3.

TABLE 2.3: Spray etching conditions.

Spray direction	downside
Spray pressure [kgf/cm^2]	1.5
Temperature [°C]	50
Etching rate [μm/min]	48.1

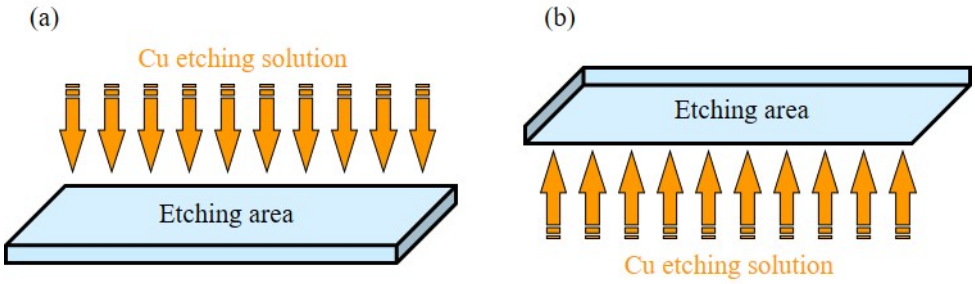


FIGURE 2.7: Images of spray direction. (a) from up side. (b) from down side.

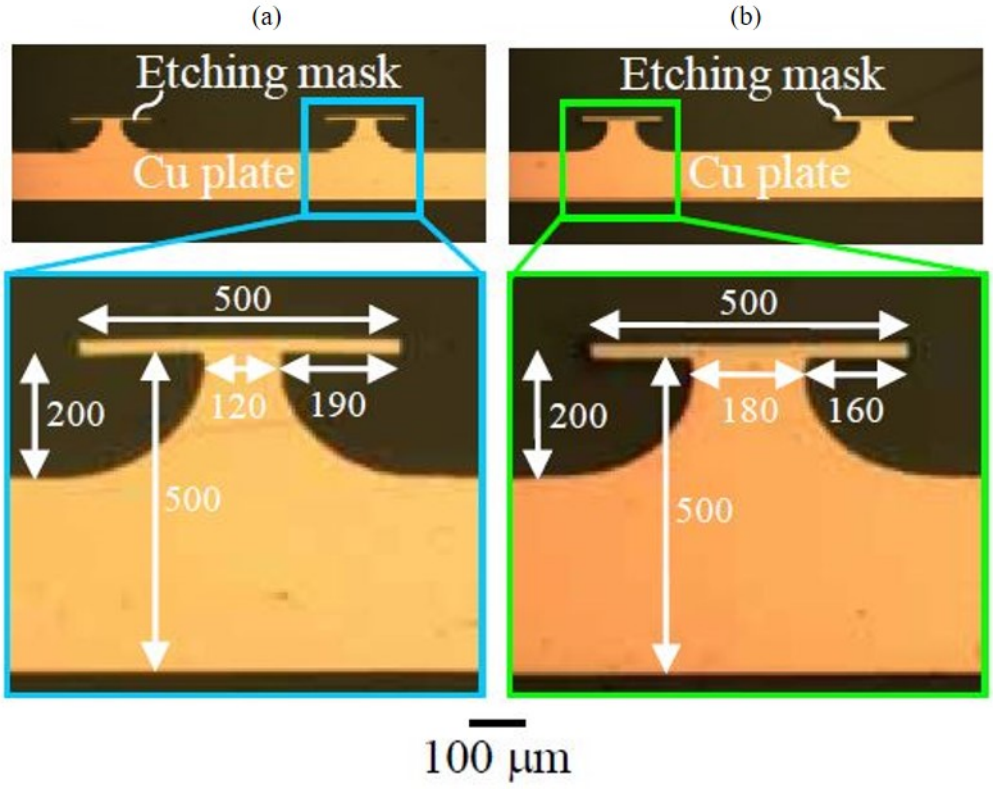


FIGURE 2.8: Influence of spray direction. (a) from up side. (b) from down side.

2.4.2 Bend Etching

Next, two types of novel Cu etching processes, i.e. the bend etching and the assist etching were developed to fabricate the Cu posts with finer pitch and higher aspect ratio. The bend etching concept is to divide the etching process into two steps. The approach is to bend an umbrella-shaped etching mask (Ni) on the surface of the Cu post, formed after the 1st etching step, along the side of the Cu posts to function as a side mask for the posts. The purpose of this process is to prevent side etching by protecting the sidewall of the Cu post with a bent mask in the 2nd etching step. The bend etching process flow is shown in Figure 2.9. The method of bending the umbrella-shaped etching mask is to place highly flexible silicon rubber on the Cu posts after the 1st etching step, and to pressurize it from the upside surface with a vacuum press machine. Figure 2.10 shows the results of bend etching. Since the top diameters of the Cu posts after the 1st and 2nd etching steps were almost equal, it means that the umbrella-shaped etching mask bent to the side of the Cu posts functioned as an etching mask on the Cu posts' side. The results showed that the bend etching technology can decrease the side etching more than spray etching can.

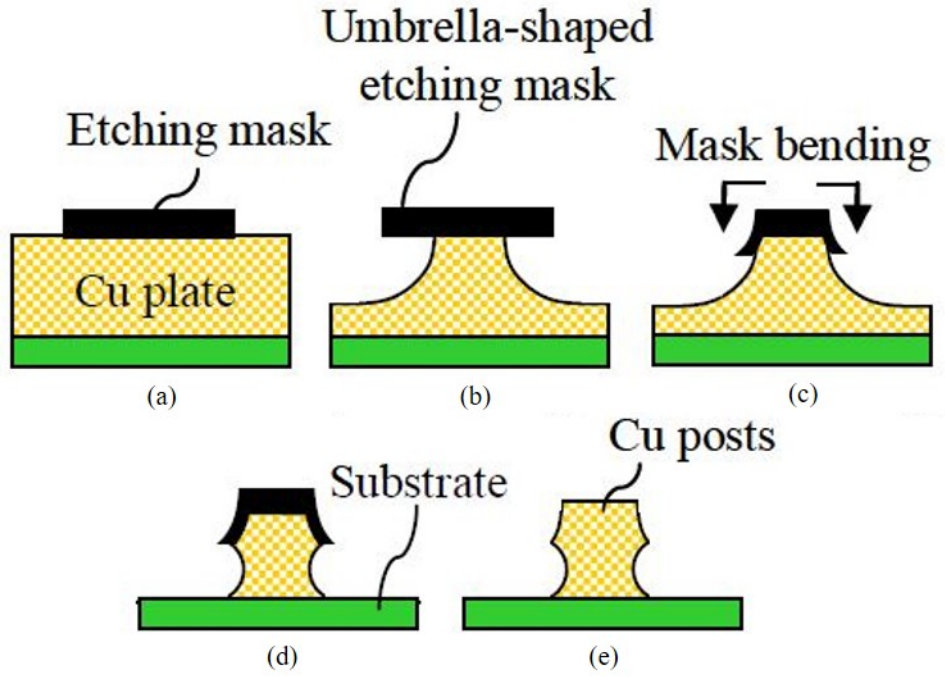


FIGURE 2.9: Process flow for bend etching. (a) mask formation. (b) 1st etching. (c) mask bending Cu posts. (d) 2nd etching. (e) mask removal.

2.4.3 Assist Etching

The assist etching is a fabrication method that combines mechanical and wet processes to form Cu posts with high aspect ratio. The assist etching concept is to form grooves before wet etching, and by so doing to shorten the wet etching

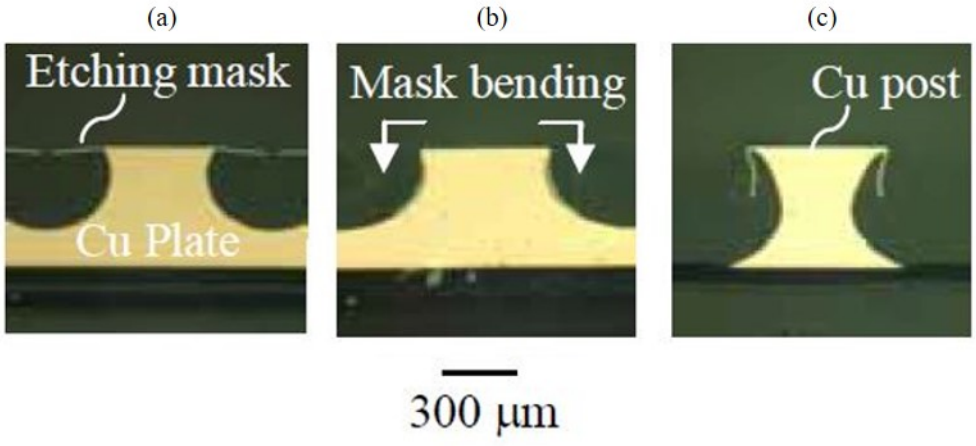


FIGURE 2.10: Cu plate and post by bend etching. (a) 1st etching. (b) mask bending. (c) 2nd etching.

time required until the Cu posts are formed. This approach can dramatically reduce the amount of side etching during wet etching. The assist etching process flow is shown in Figure 2.11. A blade dicing machine was used to form the grooves on the Cu plate in this case, after the etching mask material had been formed on the plate surface. Figure 2.12 shows the results obtained with assist etching. As a result, by forming grooves on the Cu plate, Cu posts were formed with significantly reduced side etching. In blade dicing, which uses diamond abrasives to cut copper plates, there is concern about blade breakage due to clogging. Future development of the assist etching will require improvements in blade durability and process speed.

Figure 2.13 shows the results obtained from the three etching technologies: spray etching, bend etching and assist etching. The assist etching can decrease side etching more than spray etching or bend etching can. Through the assist etching, Cu posts of 0.5 mm pitch and 6.0 aspect ratio which cannot be formed by current wet etching was developed, as shown in Figure 2.14. However, the process cost of this etching process to form grooves is expensive compared with the traditional spray etching process, so that a more cost-effective process for making grooves is needed in the future development.

2.5 Prototype Package

A prototype of the novel package based on the coreless substrate called MLTS (Multi-Layer Thin Substrate) with the Cu posts was successfully developed. Because the specifications of the Cu posts for this prototype are a height of 125 μm and pitch of 500 μm, it is possible to form them by spray etching. In addition, the spray etching is, at present, a lower cost process than bend etching and assist etching. For these reasons, the spray etching was adopted as the wet etching technology used in making the prototype. The Cu posts in the novel package are arranged in five rows, surrounding the chip mounting area. Because the Cu posts are used as external

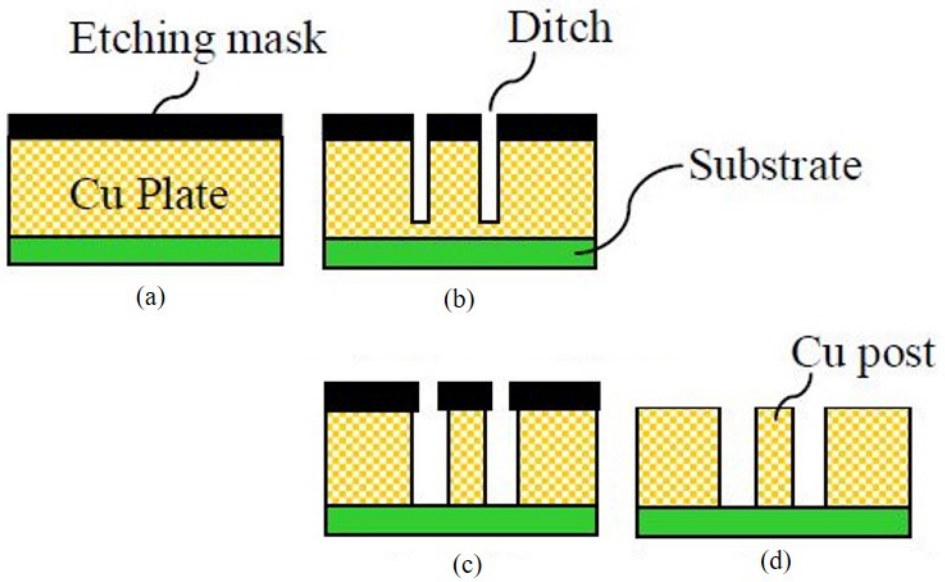


FIGURE 2.11: Process flow for assist etching. (a) mask formation. (b) ditch formation. (c) etching. (d) mask removal.

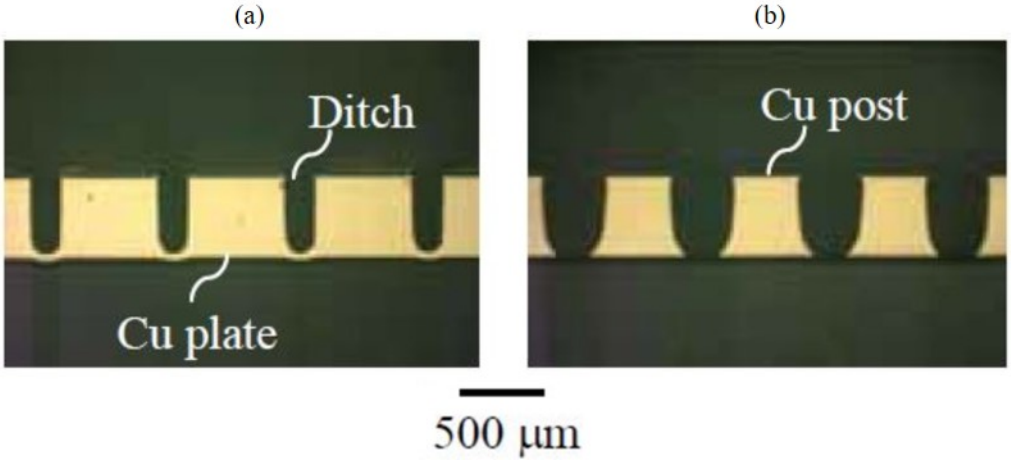


FIGURE 2.12: Cu plate and post by assist etching. (a) ditch formation. (b) etching.

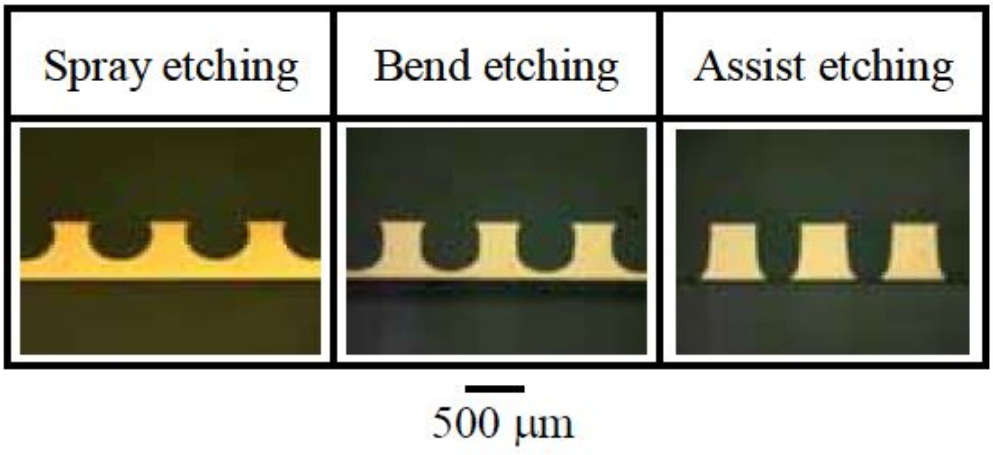


FIGURE 2.13: Summary of etching technologies.

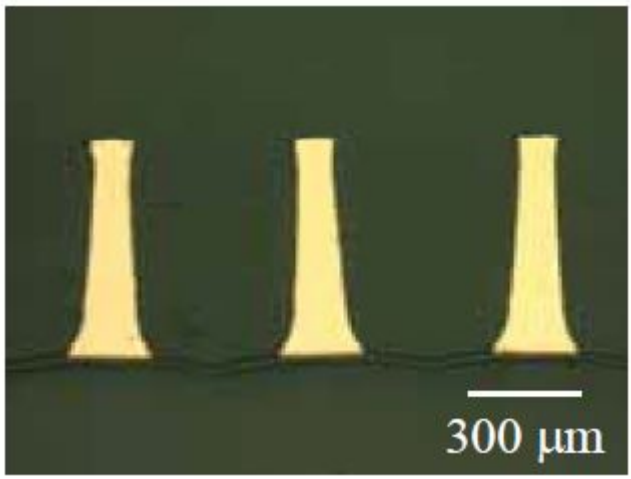


FIGURE 2.14: Narrower pitch and higher aspect ratio Cu posts by assist etching.

terminals to connect the upside package, they are required to be uniform in shape. Next, the pitch, space and shape of the etching mask are adjusted, and the shapes of the Cu posts are compared. Figure 2.15 shows a top view of the five rows of Cu posts. Table 2.4 shows the etching mask parameters. It was found that the shapes of the inner and outer Cu posts of Figure 2.15 (a) were nonuniform, whereas the shapes of the inner and outer Cu posts of Figure 2.15 (b) are uniform. The nonuniformity of the Cu posts was considered to be caused by the excessive etching of the outer Cu posts compared to the inner Cu posts. These results indicated that the design of the etching mask is important to obtain uniform Cu posts. When the mask shape is circular, the space between the masks affects the flowability of the etchant. When the space is 30 μm, the inner Cu posts of five rows have a lower etching rate. When the space is 50 μm, the etching performance become stable at the inner and outer Cu posts and the fabricated shape of the Cu posts are almost equal.

Table 2.5 shows the specifications of developed package. Figure 2.16 shows a top view after each process. After the Ni mask was formed on the copper plate (Figure 2.16 (a)), Cu posts were formed by spray etching (Figure 2.16 (b)). A 50 μm thick chip was then mounted inside the Cu post (Figure 2.16 (c)). The molding resin was laminated on the upside of the Cu posts and the chip (Figure 2.16 (d)). Next, only the top side of the Cu posts was exposed by grinding the molding resin in which the chip is embedded (Figure 2.16 (e)). Figure 2.17 shows a cross-section of the developed package. In Figure 2.17, the chip is mounted on the coreless substrate (MLTS) with the Cu posts and that the top side of the Cu posts was exposed to make interconnection for the upside package. This prototype has 361 pads arranged in five rows with 500 μm pitch. The thickness is only 230 μm. If a conventional build-up substrate with the same number of wiring layers is used in the bottom package substrate of the PoP, the thickness of the package substrate will be about 500-800 μm. Therefore, it is expected that the total height of the PoP structure can

be reduced by 50% or more by applying MLTS to the bottom package substrate of the PoP. This prototype uses die attach film in the chip mounting process. The use of flip-chip bonding should thus be investigated, as the next step.

TABLE 2.4: Etching mask parameters.

	Nonuniform Cu posts	Uniform Cu posts
Pitch	0.4 mm	0.5 mm
Space	30 μm	50 μm
Shape	Square	Circular
Rows	5	5

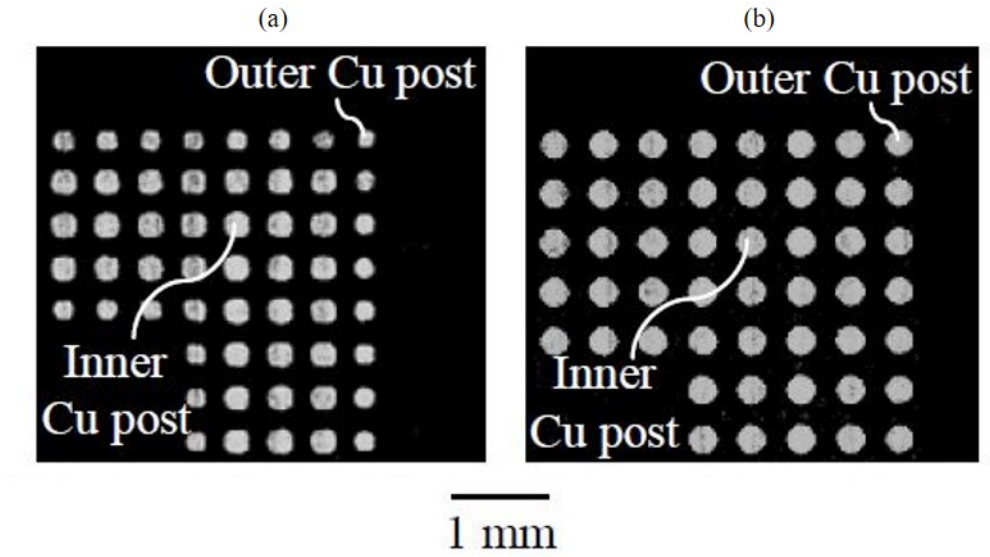


FIGURE 2.15: Influence of etching mask. (a) nonuniform Cu posts. (b) uniform Cu posts.

TABLE 2.5: Novel package prototype specifications.

Package	Size	12 mm x 12 mm
	Thickness	230 μm
	Number of pads	361
	Pad pitch	0.5 mm
Chip	Size	5 mm x 5 mm
	Thickness	50 μm
Cu posts	Thickness	125 μm
	Number of pads	361
	Pad pitch	0.5 mm

2.6 Package Reliability

The reliability of the novel prototype package was evaluated at the package level. Before the reliability test, the packages were subjected to a pre-treatment process.

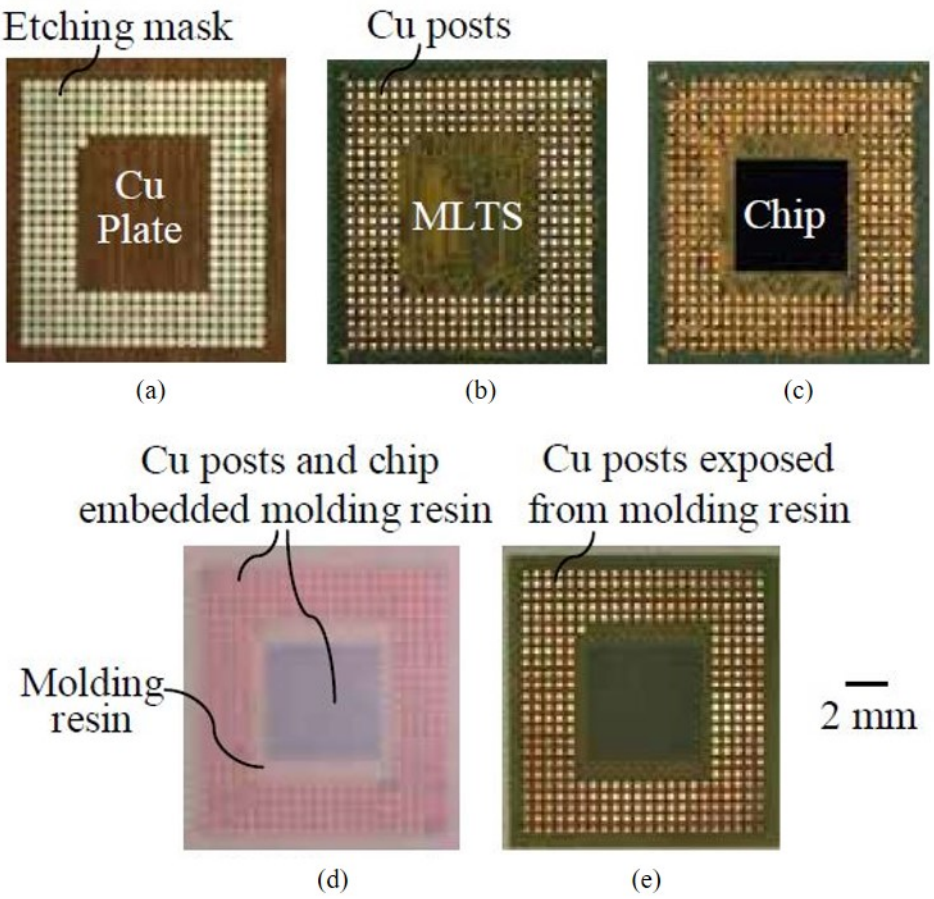


FIGURE 2.16: Top view of novel package process. (a) mask formation. (b) etching. (c) chip mounting. (d) molding resin laminating. (e) molding resin grinding.

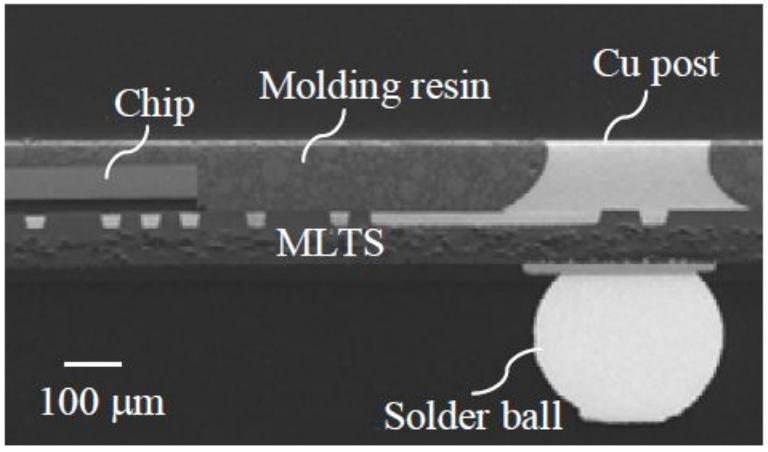


FIGURE 2.17: Cross-section of novel package.

There was no change in the electrical properties for the connection between Cu posts and MLTS wiring before and after the pre-treatment test. The prototype passed the 1,000-cycles package-level thermal cycle test (-40°C, 30 min/125°C, 30 min). The results satisfied the reliability criteria for mobile applications. And, no failures such as delamination or cracking were detected between the the Cu posts and the molding resin. The adhesion of the Cu posts and the molding resin was excellent after the 1,000-cycles thermal cycle test, The test results are shown in Table 2.6. In future development, package reliability including the upper package of the PoP will need to be evaluated.

TABLE 2.6: Reliability test.

Pre-treatment for test
1. Pre-bake : 125°C for 10 hours 2. Moisture absorption : 30°C, 70% RH for 7 days 3. Reflow : Max. 260°C, 4 times
Test condition & result
Thermal cycle test : -40°C, 60 min/125°C, 30 min Result : 1,000 cycles pass (n=6)

2.7 Package Stacking

Next, the upside package was stacked on the developed bottom package to evaluate the connectivity between packages in a PoP structure. Figure 2.18 shows a cross-section of the stacked package. The surface of the Cu posts was connected to the solder balls of the upside package. No open or short failures were observed on all 361 pads. Because the surface of the novel package is a plane, the upside package can accommodate solder balls in a diameter smaller than that of current solder balls used in partially molded packages. As a result, lower total height of this structure can be achieved by using the novel package. Furthermore, the fact that the surface of the bottom package of the PoP is plane means that a higher density SiP can be realized by forming a rewiring layer.

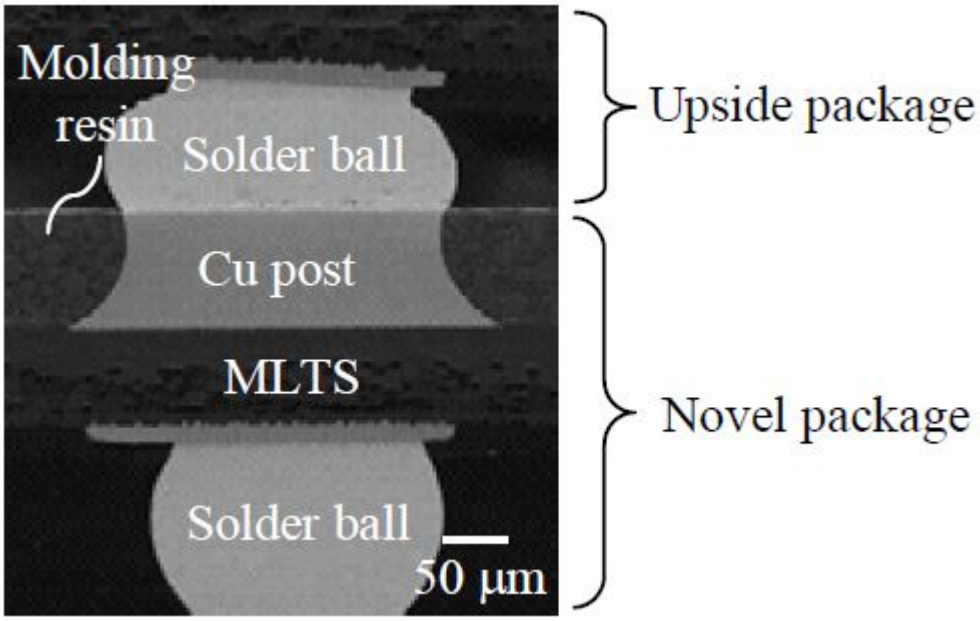


FIGURE 2.18: Novel pacakge stacking.

2.8 Summary

A novel PoP bottom package technology by utilizing an ultra-thin coreless substrate, MLTS, has been successfully developed. Its package is unique in that it has Cu posts for interconnection with the upper package of PoP. The wet etching technology for Cu posts, spray etching, was optimized using 500 μm thick Cu base plates. In addition, two types of novel wet etching processes, bend etching and assist etching, were developed to achieve finer pitch and higher aspect ratio. The results showed that assist etching can decrease side etching more than spray etching or bend etching can. Through the assist etching, I achieved Cu posts of 500 μm pitch and high aspect ratio of 6.0, which cannot be realized by current wet etching. The prototype PoP bottom package had 361 pads arranged in five rows with 500 μm pitch. The thickness was only 230 μm, which is 50% thinner than conventional build-up substrate technology. The prototype passed the 1,000-cycles package-level thermal cycle test. The novel prototype package was found to have small thickness and excellent reliability. I believe that novel packaging technology is one of the best approaches to become a bottom package for PoP with a thin profile and excellent electrical performance.

Chapter 3

Embedded Active Die Package for High-Pin-Count LSI with Cu Plate

3.1 Background

A thin LSI package with high electrical performance has long been required for a range of applications, including mobile equipment, TVs and digital still cameras, to meet the needs for module and system miniaturization. These demands will probably be never ending issues for those who seek convenience and comfort. Embedded die packaging technology is one of the most attractive solutions because of its small thickness and high density interconnects. There are two fabrication processes for embedding active die technologies: embedded die package and fan-out wafer level package (FOWLP). Embedded die packaging technology is based on a printed circuit board (PCB) of panel-level manufacturing infrastructure [39]–[44], while fan-out packaging technology is based on a molded reconstituted substrate of wafer-level manufacturing infrastructure [45]–[47]. In this chapter, embedded die package technology is described, and FOWLP technologies are described in Chapter 4 and Chapter 5.

When we try to fabricate thin embedded active devices with high-pin-count LSIs such as application processor for smartphones, we face many challenges such as: 1) achieving high yield processes to minimize the cost of losing known-good-dies (KGD), 2) controlling warpage for a large package size, 3) providing thermal management because the entire LSI chip is embedded in the package substrate [48]–[50], and 4) showing reliable Cu interconnection between the LSI chip and package substrate [51]–[53].

For these reasons, the embedded high-pin-count LSI technology has remained at the experimental stage, and the only embedded active devices available for practical use are ones with small-pin-count LSIs with a pitch of approximately 300 μm and 200 pads. I have developed a novel ultra-thin package structure for an embedded microprocessor [54]–[60]. The main feature of the developed process is that the first build-up Cu layer is directly fanned out from the Cu posts on the LSI pads to achieve high-density and reliable interconnects. This is realized by use of resin grinding and a semi-additive metallization process after embedding a high-pin-count LSI

chip into thin build-up layers (coreless substrate). A microprocessor LSI with approximately 1500 pads and a 160-μm-pitch staggered layout is used. This chapter describes the concept of the novel package structure, fabrication process, warpage, thermal-resistance evaluations, demonstration with actual LSI device and package-level and board-level reliabilities.

3.2 Novel Embedded Die Packaging Technology

3.2.1 Structure

The structures of a conventional flip chip ball grid array (FCBGA) package, widely-used for high-pin-count LSI, and the newly developed package are compared in Figure 3.1. The developed package has a thin embedded LSI chip and a thick rigid Cu plate on which there are thin build-up layers without any large through-holes usually prepared by mechanical drilling. Its total package thickness is much smaller than that of the conventional FCBGAs. This structure is expected to improve the electrical performance of the LSI package because of the use of the coreless substrate similar to chapter 2 [32]–[35]. In addition, the structure is expected to achieve low thermal resistance because of the Cu plate attached to the LSI chip's rear side. This means that the Cu plate functions as a heat sink. The embedded LSI and build-up layers are connected by direct Cu plating without any additional materials, such as wire bonds, solder bumps and micro bumps. The direct Cu metallization allows a finer pitch layout for the pads of the embedded LSI, and provides reliable package integration. In this chapter, this new package is called a seamless package because it does not use conventional materials (wire bonds, solder bumps and micro bumps) for the interconnection between the LSI chip and the package substrate.

3.2.2 Fabrication Process

A novel ultra-thin seamless package technology consists mainly of wafer- and package-level processes, as shown in Figures 3.2 (a)-(c) and (d)-(i),respectively.

In the wafer-level process, a seed metal layer is sputtered on the wafer on which logic LSIs have been manufactured. After the photoresist is coated and patterned, electroplated Cu is formed on the LSI pads in a 160-μm-pitch staggered layout. Cu posts with a thickness of 15 μm and diameter of 40 μm are then fabricated by removing the photoresist and etching the exposed seed layer (Figure 3.2 (a)). The wafer is thinned to 50 μm and diced after a 20-μm-thick adhesive film is laminated onto the rear of the wafer (Figure 3.2 (b), (c)). The LSI chip is 9 mm x 9 mm in size and has approximately 1500 Cu posts. Top and cross-sectional views of the LSI chip are shown in Figure 3.3, respectively.

In the package-level process, the LSI chip is mounted face up on the 500-μm-thick Cu plate (Figure 3.2 (d)) and embedded into 90-μm-thick epoxy resin having

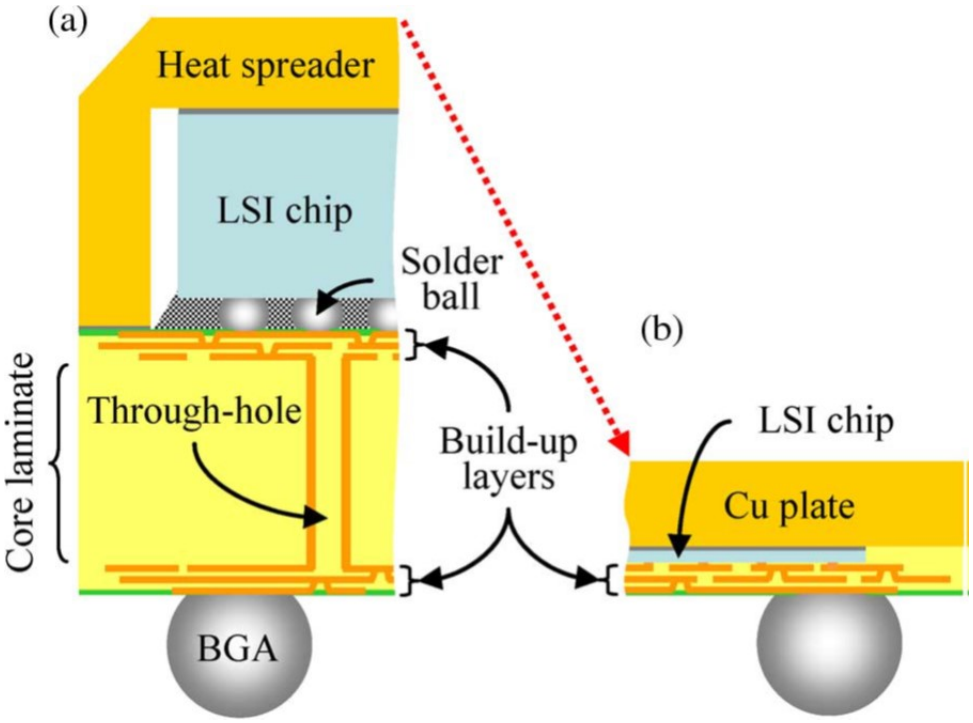


FIGURE 3.1: Comparison of the LSI package structures. (a) conventional FCBGA. (b) embedded die package.

low-viscosity by vacuum lamination process (Figure 3.2 (e)). After the Cu posts are exposed by polishing the epoxy resin (Figure 3.2 (f)), the first 40-μm-pitch Cu build-up layer is fabricated by semi-additive metallization process directly on the Cu posts (Figure 3.2 (g)). This layer is responsible for fanning out the signal lines from the LSI chip to the package. Top views of the resin grinding and the first layer are shown in Figure 3.4. The second and third build-up layers are designated as the ground plane and BGA pads with power lines, respectively (Figure 3.2 (h)). Top views of the second and third layers of build-up are shown in Figure 3.5. The via-holes for these layers are fabricated by cost-effective CO_2 laser technology with a top diameter of 50 μm, thanks to the first layer's fine-pitch fan-out. This embedding LSI process is expected to achieve high-yield manufacturing because it requires no UV laser technology to fabricate via-holes, which has the disadvantages of high initial costs and sensitive process tuning for formation of small-diameter vias with a diameter of 30 μm or less. After solder-resist formation, each package including the Cu plate is separated by dicing. In this study, the blade dicing is used for a package singulation. However, in order to fabricate not only the build-up layers with embedded dies but also mainly the 500-μm-thick Cu plate, high productivity cutting techniques such as wet etching are also examined [59]. Finally, 625 lead-free BGA balls are mounted on the package (Figure 3.2 (i)).

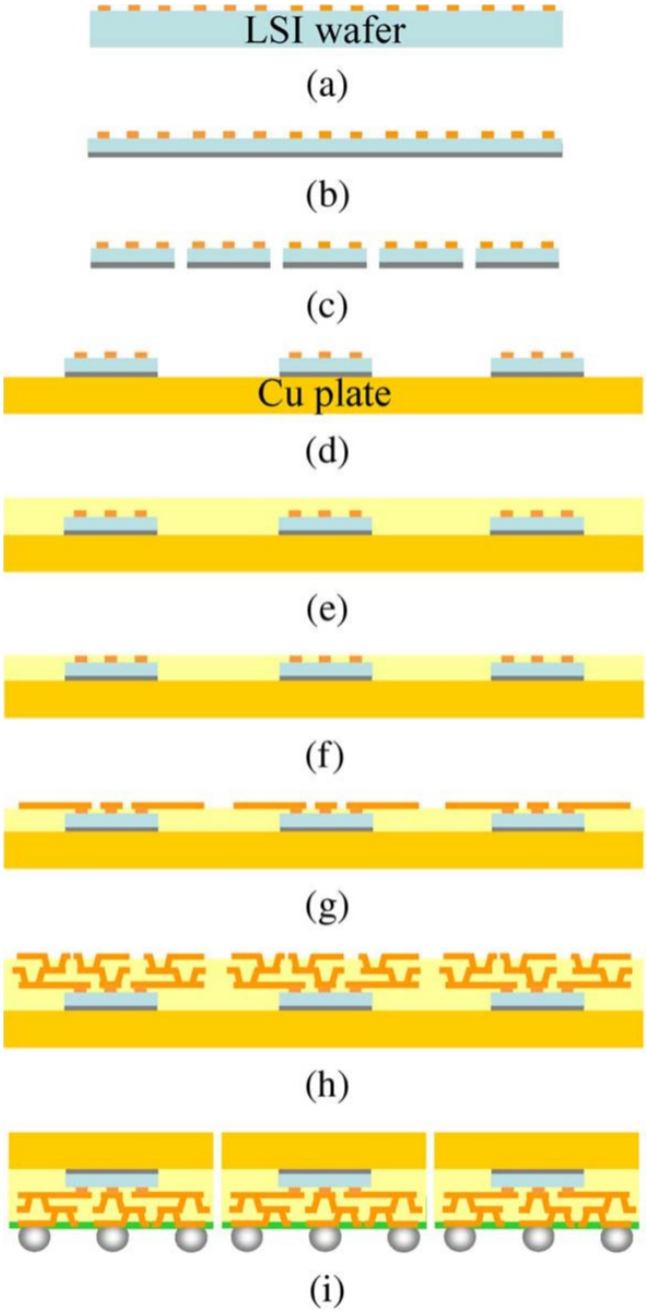


FIGURE 3.2: Fabrication process for seamless package. (a) Cu posts formation on LSI pads. (b) wafer thinning and adhesive film laminating. (c) wafer dicing. (d) LSI chip mounting on Cu plate. (e) resin lamination. (f) resin grinding. (g) first metallization layer formation. (h) formation of remaining layers. (i) BGA formation.

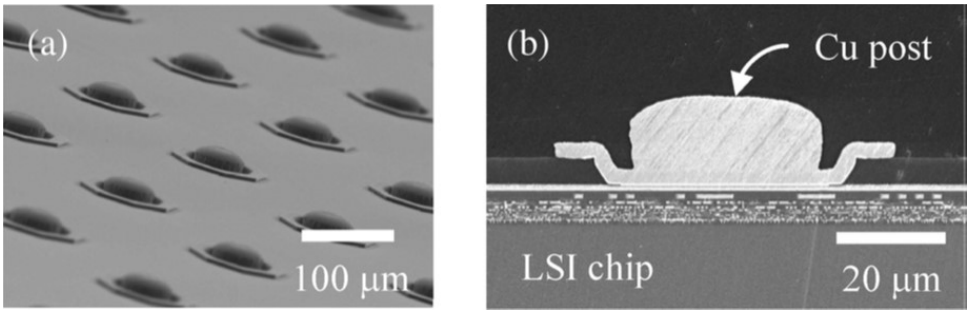


FIGURE 3.3: Cu post formations on LSI pads as (a) top and (b) cross-sectional views.

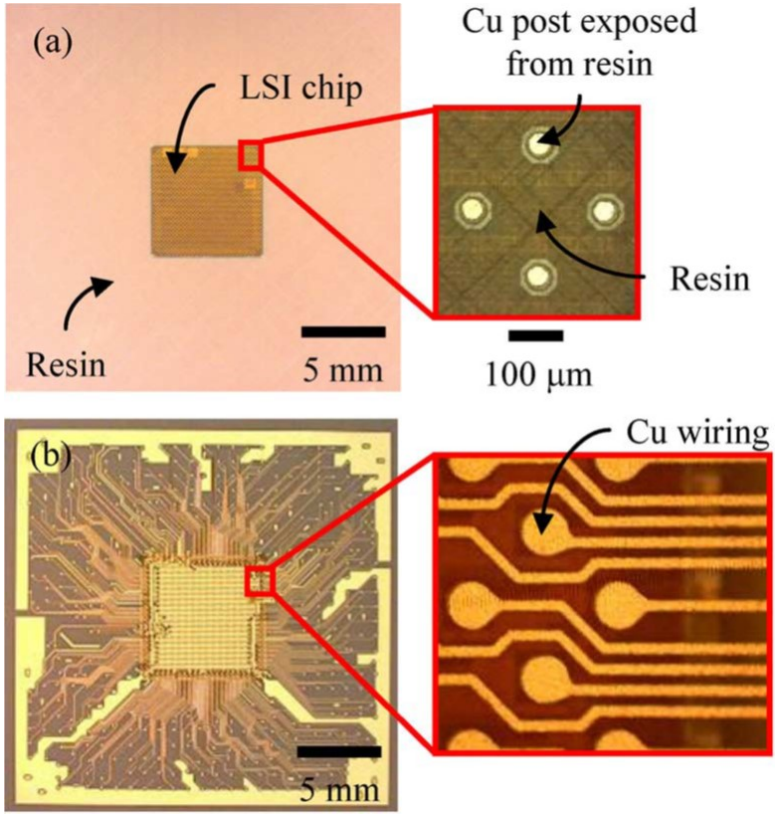


FIGURE 3.4: Top view of novel package process. (a) resin grinding. (b) first metallizationlayer formation.

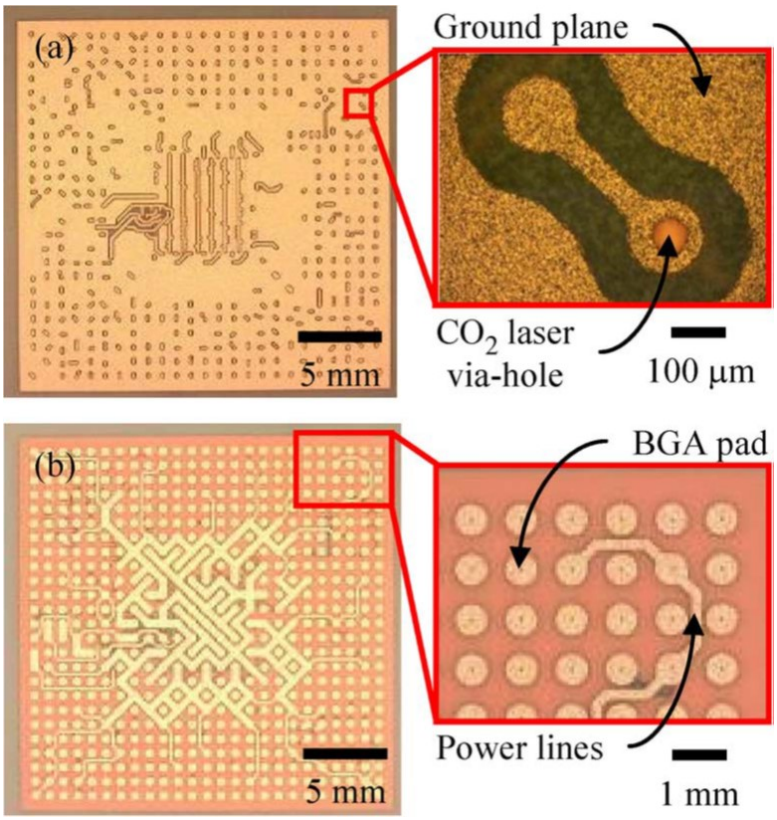


FIGURE 3.5: Top view of novel package process. (a) second metallization layer formation. (b) third metallization layer formation.

3.2.3 Prototype Package

In this section, a thin prototype package based on the previous fabrication process is described. An outline photograph of the prototype package is shown in Figure 3.6. The top-side view shows only the Cu plate. The BGA-side view shows the package substrate with the embedded LSI chip in the center of the package. The specifications of the prototype package are shown in Table 3.1, and a cross-sectional view of the package is shown in Figure 3.7. While the seamless package is 27 mm x 27 mm in size, the embedded LSI chip is 9 mm x 9 mm. Although the package size seems to be large for the chip, the package size and BGA pitch are decided to ensure the compatibility with those of reference FCBGA. This enables the evaluation using an LSI tester and the verification of the system operation using the mother board.

It is clearly observed in Figure 3.7 that the 50-μm-thick LSI chip is completely embedded in the first build-up resin layer and connected to the first metallization layer by direct Cu plating without wire bonds or solder materials. This interconnection point is called a "Seamless Interconnect" in this thesis. The second and third metallization layers are fabricated with conformal vias fabricated by CO_2 laser. Despite the existence of the 500-μm-thick Cu plate, the total package thickness with three metallization layers, excluding the BGA ball height, is only 710 μm as a result of the embedded structure. The thin package substrate with three metallization layers will contribute to excellent power integrity due to the absence

of through-holes. A cross-section of the edge area of the embedded LSI is shown in Figure 3.8. Although the LSI chip is mounted face up on the Cu plate without any cavity structures, the low-viscosity epoxy resin enables void-free embedding, even at the LSI edges, and surface flattening. This process doesn't require the temporary bonding and debonding technology used in the die-first (face-down) FOWLP process described in Chapter 4. This is expected to greatly reduce the manufacturing cost. The microstructure of the interconnects fabricated by direct Cu plating on the Cu posts are analyzed by scanning ion microscopy (SIM) to estimate grain size and crystal orientations, as shown in Figure 3.9. Random orientation and a wide range of grain sizes for Cu wiring and Cu post, sandwiching the seed metal layer, are observed. However, no significant voids and cracks are recognized.

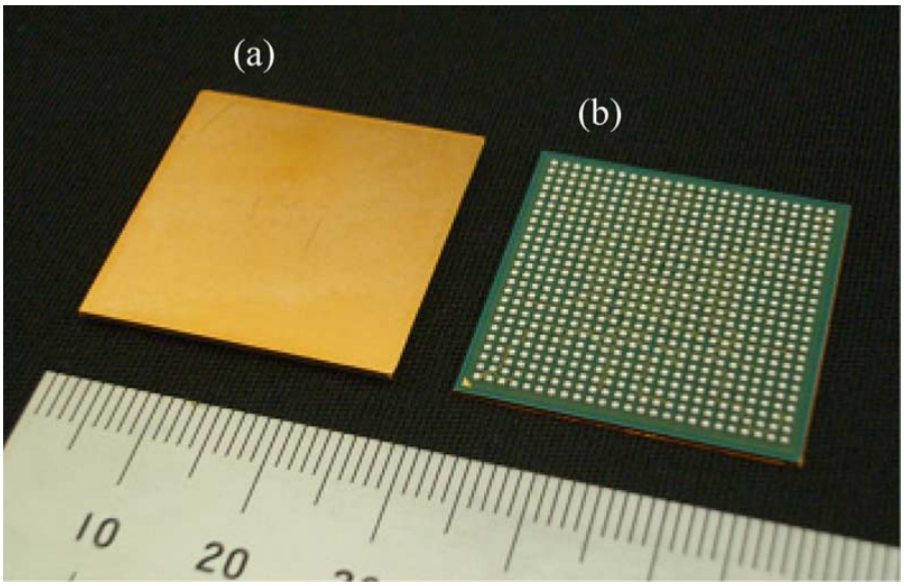


FIGURE 3.6: Prototype photographs as (a) top and (b) BGA views.

TABLE 3.1: Specifications of the prototype.

LSI chip	Size (mm^2)	9 x 9
	Thickness (μm)	50
	LSI pad count	1500
	LSI pad pitch (μm)	160 (staggered area array)
Pacakge	Size (mm^2)	27 x 27
	Thickness (μm)	710
	BGA pad count	625
	BGA pad pitch (mm)	1.0 (area array)

3.3 Comparison with Reference FCBGA

Next, the seamless package is compared with a reference FCBGA package in different aspects. The embedded LSIs have the same specifications as the microprocessor. The cross-sectional views and package specifications are shown in

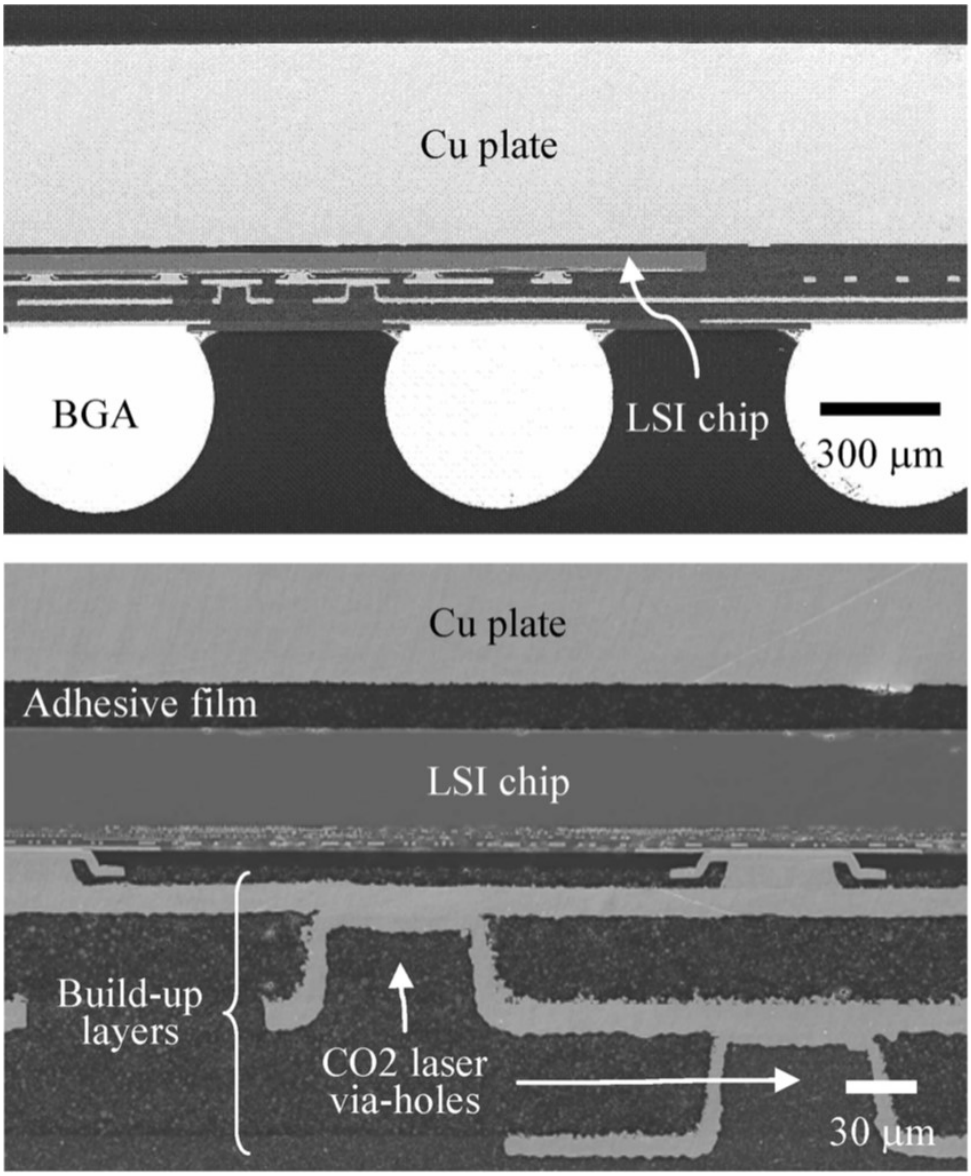


FIGURE 3.7: Cross sections of the prototype.

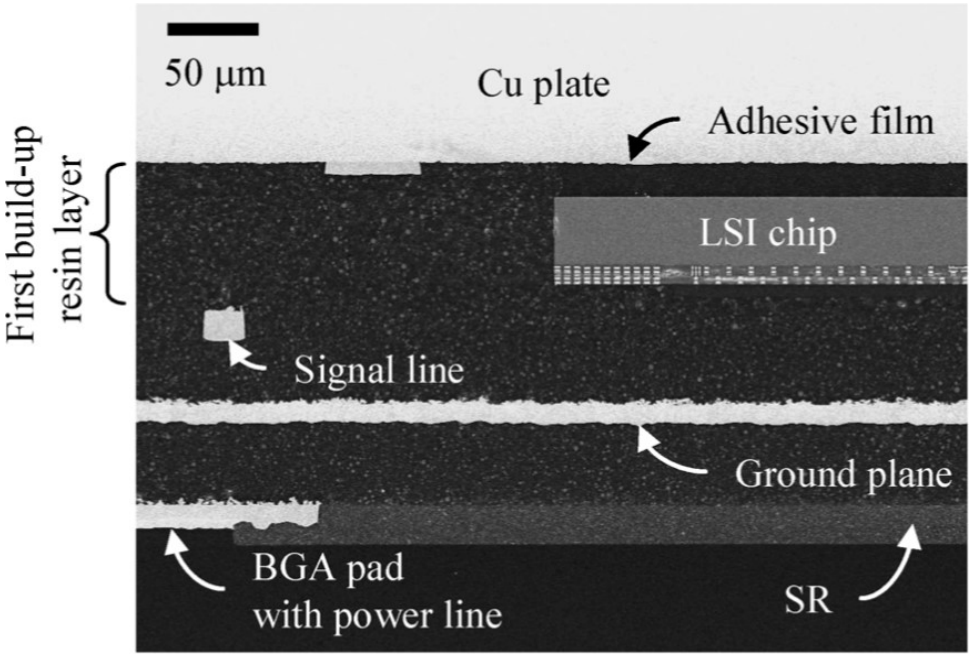


FIGURE 3.8: Cross section of edge area of the embedded LSI.

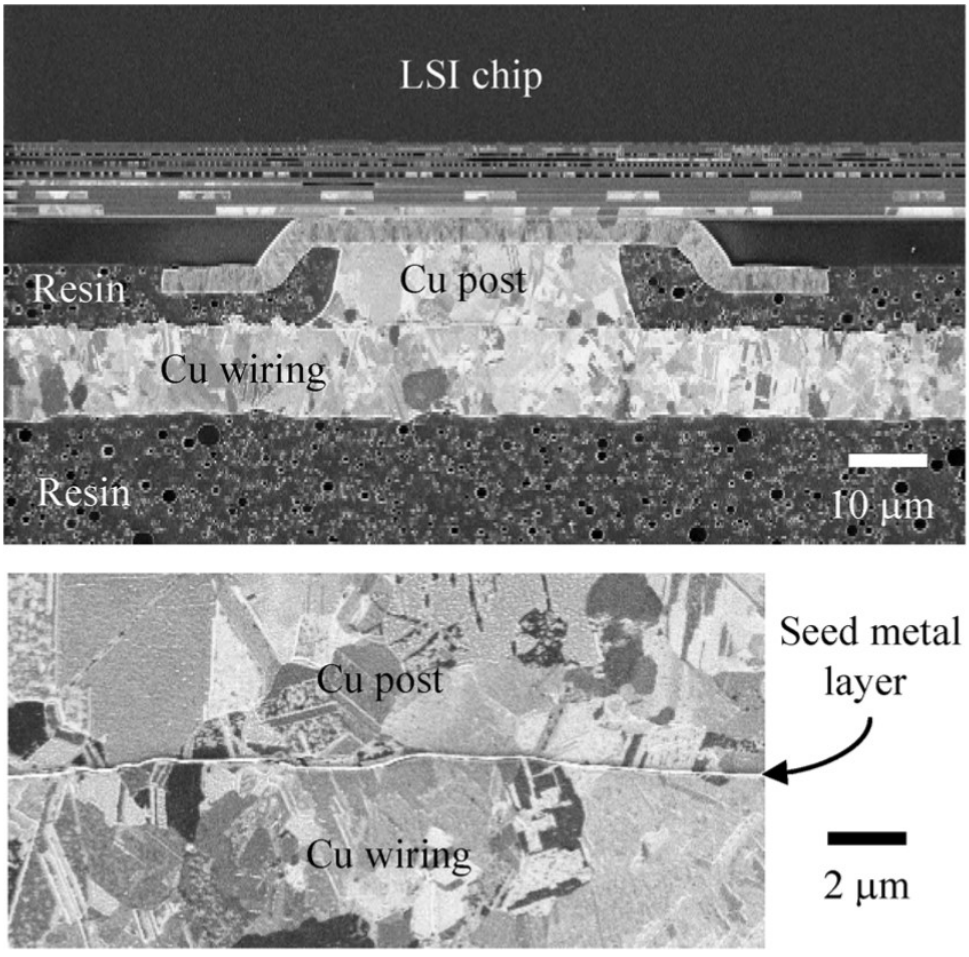


FIGURE 3.9: Cross sections of the interface of Cu post and Cu wiring.

Figure 3.10 and in Table 3.2, respectively. The reference FCBGA consists of a 2-2-2 build-up substrate (total 6 layers) with 800-μm-thick through-holes in core laminate, a 725-μm-thick LSI, and an almost 9-mm-thick heat sink which isn't included in the figure, as shown in Figure 3.10 (a). Thus, the thickness of the seamless package is one-fifteenth of that of the reference FCBGA with heat sink. The result shows that the seamless package technology allows a significant reduction in thickness. Even without the heat sink, the reference FCBGA is 1.9 mm in thickness, which is 2.6 times as thick as the seamless package. The interconnection between the LSI chip and package substrate layers is a Cu direct metallization for the seamless package, as described before, while the LSI chip of the FCBGA is connected to the substrate by solder bumps. A conventional FCBGA structure has many materials besides solder bumps, such as underfill resin, stiffener, lid, and several adhesives between the stiffener and lid or the chip and lid. In contrast, the seamless package structure has a simple Cu direct metallization without solder bumps or underfill resin; therefore, this technology is essentially a low-cost solution compared with FCBGA technology. As a result of its through-hole-less structure, the seamless package with three metallization layers provides almost the same functions as the reference FCBGA with six metallization layers [55], [60]. The results of reducing the number of wiring layers from six in the conventional FCBGA to three by embedding the LSI chip in the coreless substrate will be useful as a guideline for future package structures and designs.

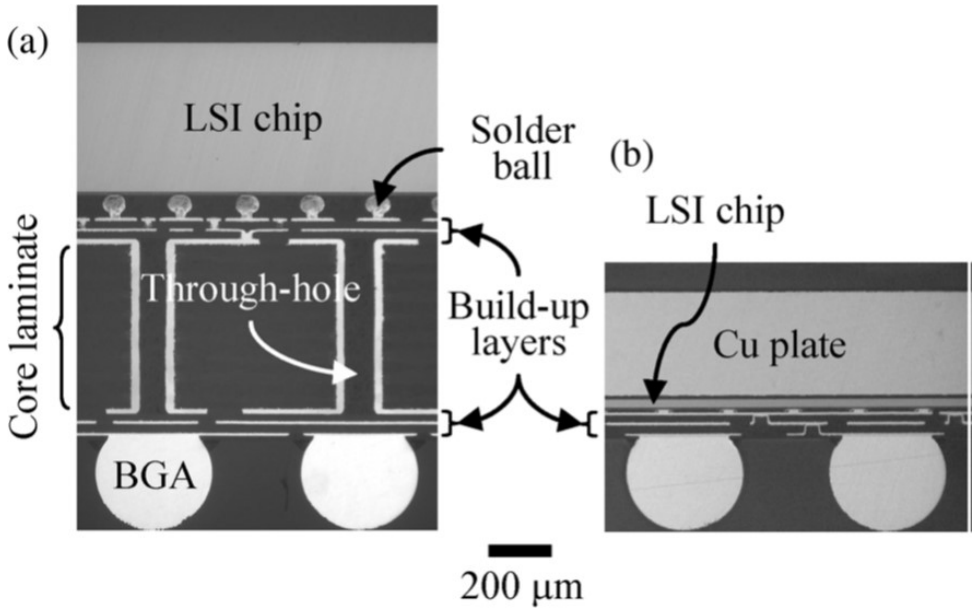


FIGURE 3.10: Cross-sections of reference FCBGA and seamless package. (a) reference FCBGA. (b) seamless package.

TABLE 3.2: Comparison of reference FCBGA and seamless package.

Thickness	Reference FCBGA	Seamless package
Package (mm)	11 (with heat shink)	0.71
LSI chip (μm)	725	50
Package substrate (μm)	1100	120

3.4 Warpage Measurement

The warpage of the seamless package is evaluated by shadow-moire measurement. The temperature range for this measurement is from -55°C to 260°C at the Cu plate surface. The shadow-moire topographies and warpage results are shown in Figures 3.11 and 3.12, respectively. The warpage is measured along the 38-mm-long package diagonal. The seamless package shows excellent warpage characteristics with a maximum value of 82 μm at -55°C and 35 μm at the reflow temperature of 260°C. These values are quite small for the 27-mm-square package.

The warpage of the embedded LSI chip area, 9 mm x 9mm, is different from that of the whole package area at -55°C and 24°C as shown in Figures 3.11 (a) and (b). This distinctive warpage shape is caused by the mismatch in the coefficients of thermal expansion of the embedded Si chip, Cu plate, and epoxy resin used in the build-up layer. However, the warpage values for all the evaluated temperatures are smaller than the critical value of 120 μm; therefore, the seamless package provides a sufficient process margin for system board assembly. In other words, these results indicate that the use of 500-μm-thick rigid Cu plate in the seamless package successfully controls the warpage even for a large package size of 27 mm x 27 mm. Furthermore, to meet the needs for package miniaturization, a much thinner package is fabricated by thinning Cu plate using wet etching process after fabricating the individual package. The 500-μm-thick Cu plate is thinned to 250 and 100-μm-thick by alkali-based solution used in Chapter 2. The warpage characteristics are evaluated by shadow-moire measurement at a temperature range from room temperature to 250°C, as shown in Figures 3.13 and 3.14. When the Cu plate is 250-μm-thick, the total package thickness is only 460 μm, achieving acceptable warpage with a maximum value of 117 μm at room temperature. This means that even if 500-μm-thick Cu plate is thinned to 250 μm in thickness, the Cu plate still supports a build-up substrate embedding LSI chip. On the other hand, the warpage of the package with 100-μm-thick Cu plate is quite large at over 350 μm because of reduced rigidity of the Cu plate. The acceptable warpage value for a 27 mm square package is about ±120 μm. It was found that a 100-μm-thick Cu plate did not meet that criterion. However, it is presumed that the adoption of epoxy resin with the same coefficient of thermal expansion as Cu plate and high elastic modulus is expected to reduce the warpage and to achieve ultra-thin package with the 100-μm-thick Cu plate. In the following sections, thermal management, demonstration and the package reliability are performed for the packages with

500-μm-thick Cu plate.

3.5 Thermal Management

The thermal resistance values of the seamless package and reference FCBGA are evaluated on JEDEC standard thermal test boards. The LSI is heated using 4.4 W of power supplied through the board. A top view of the seamless package mounted on the board is shown in Figure 3.15. The experimental results for thermal resistance are shown in Figure 3.16. The thermal resistance of the seamless package between the junction in the LSI and ambient is 10.8 °C/W at a wind velocity of 0 m/s. This value is almost comparable to 9.6 °C/W for the reference FCBGA with a heat sink, and much smaller than 13.9 °C/W for the reference FCBGA without a heat sink. The thermal resistance at a wind velocity of 2 m/s is decreased compared with that at a wind velocity of 0 m/s in each package. Since the heat sink of the reference FCBGA has many large fins, the significant improvement is observed for the reference FCBGA with a heat sink. However the thermal resistance of the seamless package is still smaller than that of the reference FCBGA without a heat sink in spite of the wind velocity. There are two major reasons for obtaining the low thermal resistance of the seamless package: 1) the Cu plate attached to the embedded LSI chip's rear side contributes to the thermal design as a cooling part, and 2) the heat generated by the LSI is dissipated easily through the mother board because of the short distance between the LSI chip and the mother board.

The thermal simulation is also performed under the same conditions as those for the experiment. There are good agreements between the simulation and experimental results. The contour figures of the simulation results at wind velocities of 0 and 2 m/s are shown in Figures 3.17 and 3.18, respectively. In the seamless package, it is recognized that the heat diffuses through not only the Cu plate but also the board, as shown in Figures 3.17 (b) and 3.18 (b). Although the reference FCBGA without a heat sink shows a similar tendency, the seamless package can dissipate heat more effectively than the FCBGA because of its through-hole-less structures and its cooling part.

From these results, it was found that the Cu plate, which not only controls warpage but also functions as a heat sink, is suitable as a support substrate for embedded die technology. However, as mentioned above, singulation method of the Cu plate is an issue, and various dicing processing technologies, including chemical etching or mechanical etching, need to be developed. In addition, a 600 mm square Cu plate with a thickness of 500-μm-thick is very heavy, which makes transportation during manufacturing a problem. AlSiC, which is about 35% lighter than Cu plate, is expected to be a future support substrate [59].

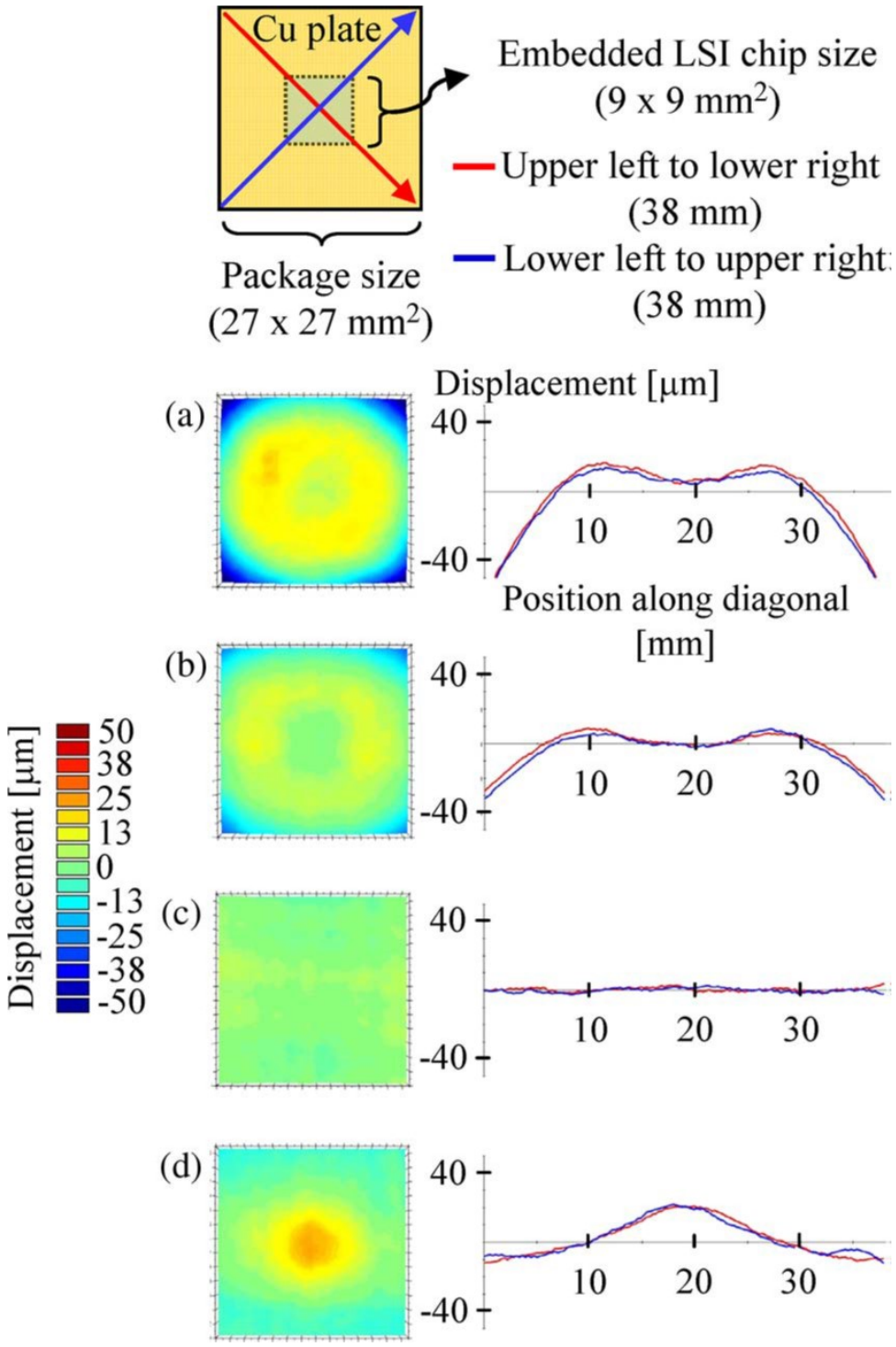


FIGURE 3.11: Topography and warpage of shadow-moire measurement at (a) -55, (b) 24, (c) 162 and (d) 260°C.

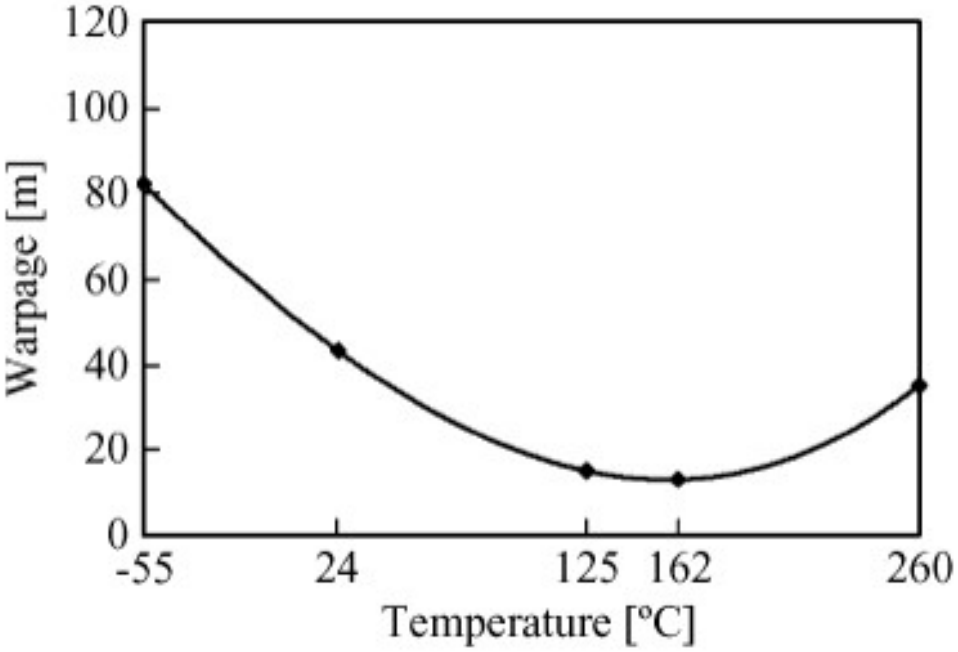


FIGURE 3.12: Temperature dependence of the warpage.

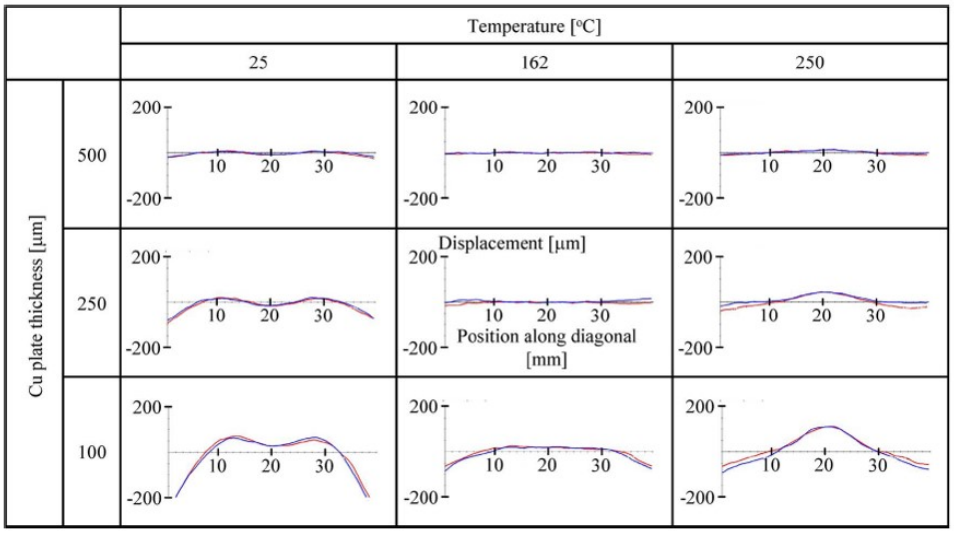


FIGURE 3.13: Warpage versus temperature on 500-μm-thick, 250-μm-thick, and 100-μm-thick Cu plate, extracted by shadow-moire measurement.

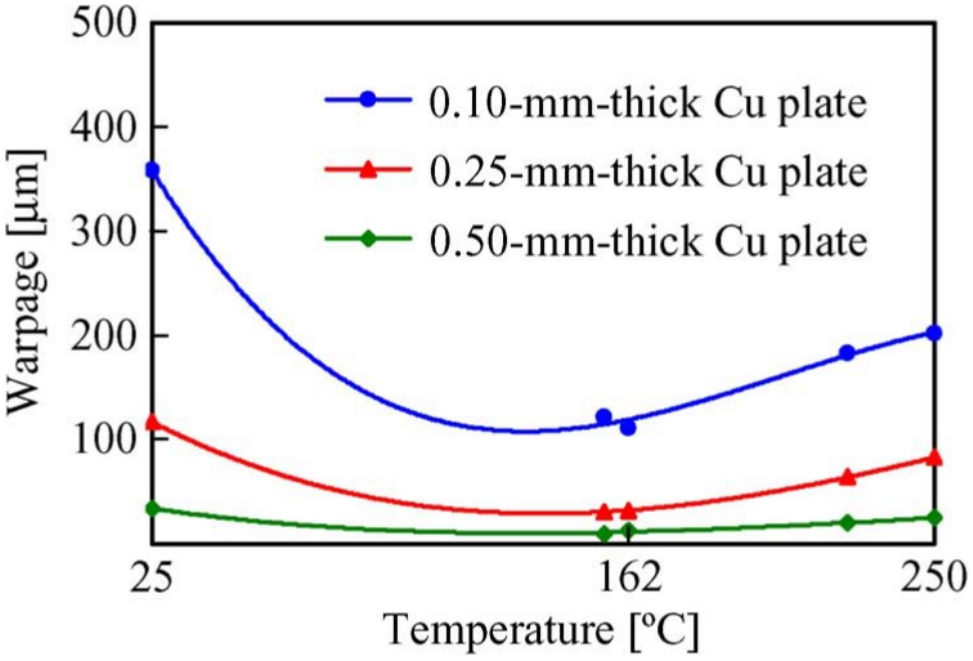


FIGURE 3.14: Warpage versus temperature on 500-μm-thick, 250-μm-thick, and 100-μm-thick Cu plate.

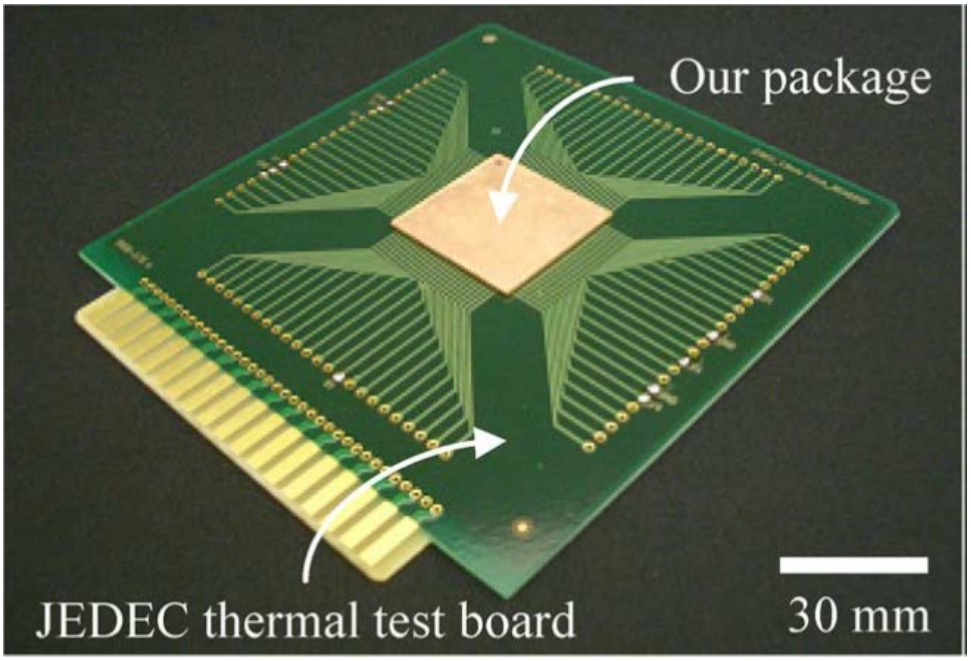


FIGURE 3.15: Top view of seamless package mounted on JEDEC board.

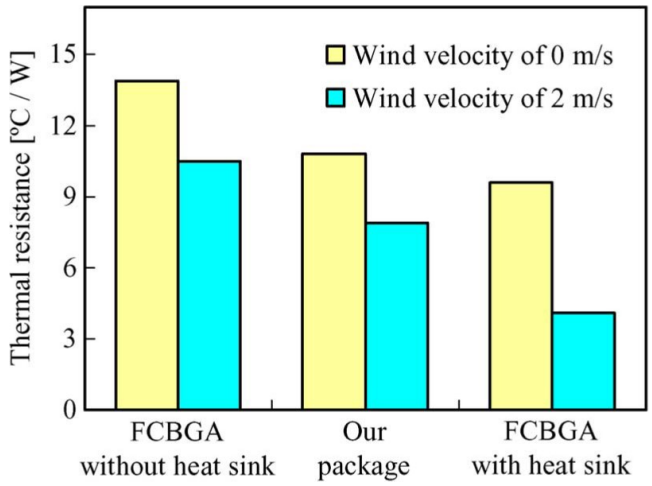


FIGURE 3.16: Experimental results for thermal resistance.

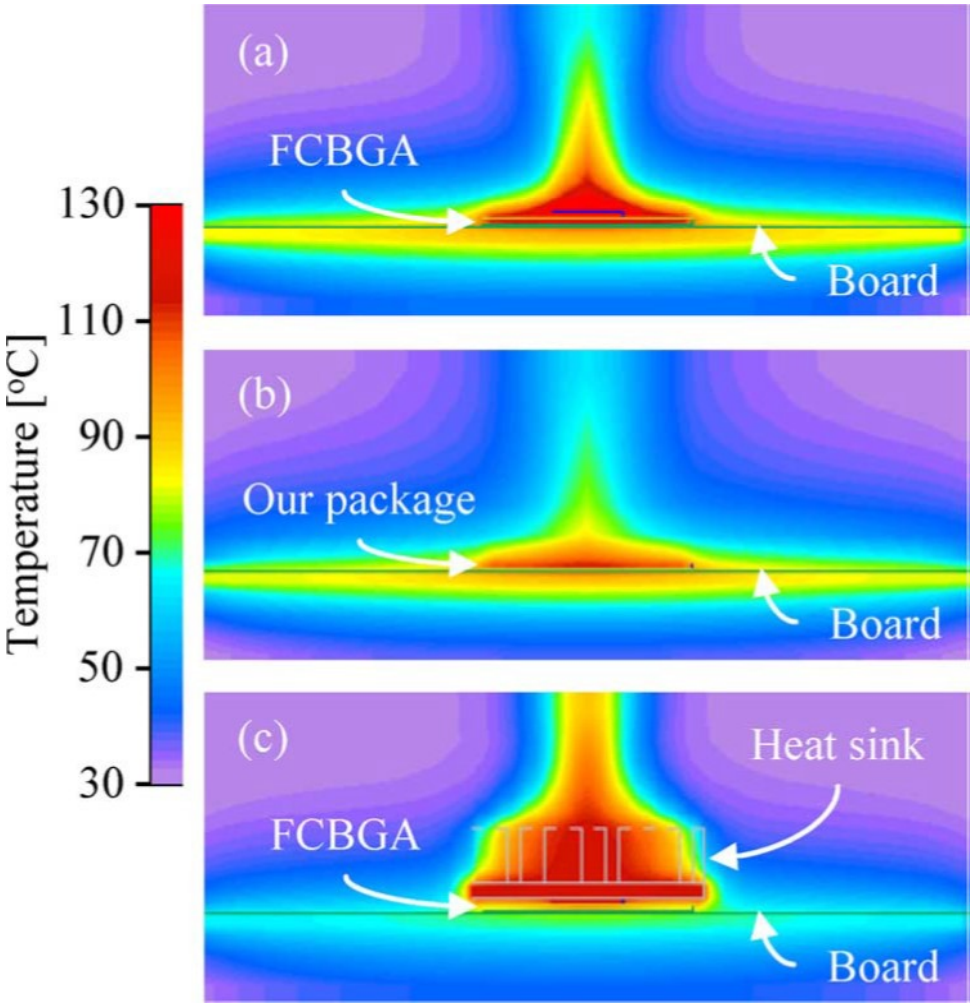


FIGURE 3.17: Contour figures of thermal simulation at a wind velocity of 0 m/s. (a) reference FCBGA without heat sink, (b) seamless package, and (c) reference FCBGA with heat sink.

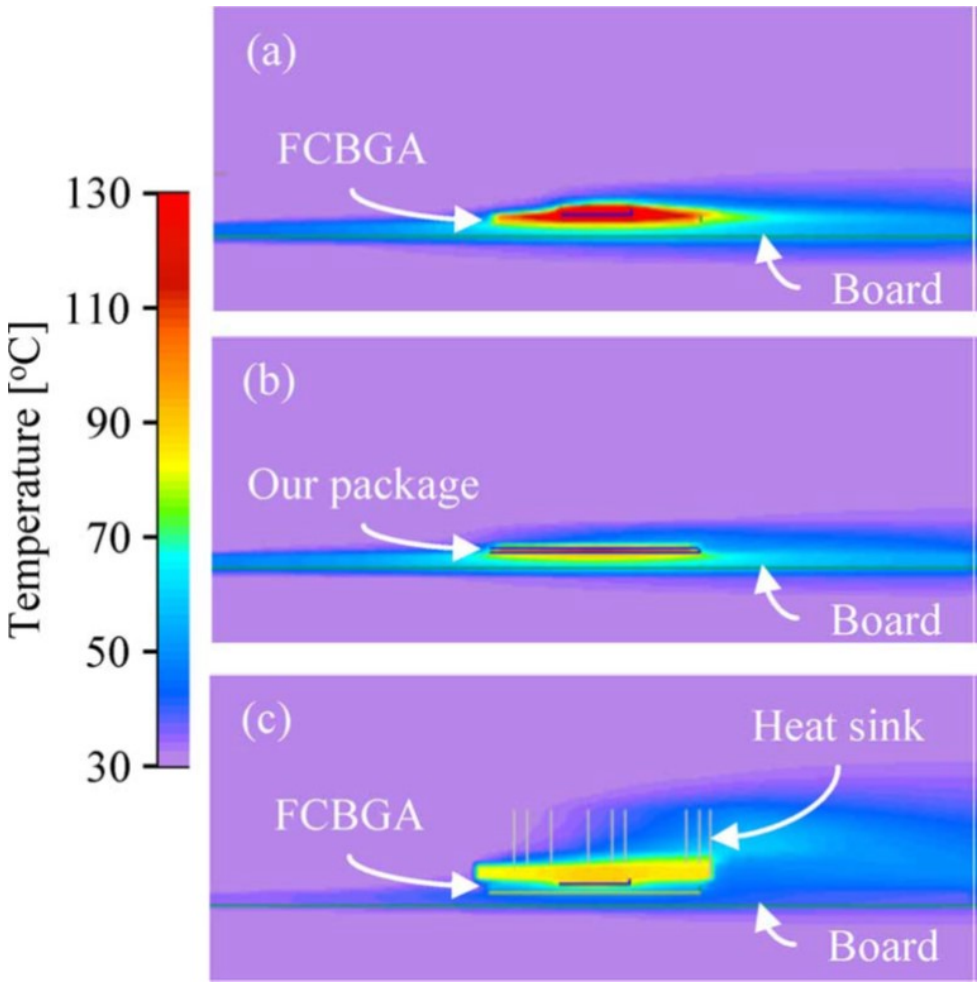


FIGURE 3.18: Contour figures of thermal simulation at a wind velocity of 2 m/s. (a) reference FCBGA without heat sink, (b) seamless package, and (c) reference FCBGA with heat sink.

3.6 Demonstration

The performance of the seamless package is evaluated using an LSI tester. The seamless package is mounted on the LSI test socket for BGA with 625 balls on the printed circuit board, as shown in Figure 3.19. The seamless packages passed not only the open/short test of its fundamental wiring reliability, but also the LSI function tests: the loose function test, at-speed test, scan test, etc. The seamless packages were tested with an LSI tester by using the same test program as for the reference LSI package. Figure 3.20 shows the shmoo plots for the seamless package. The X-axis is the test rate and the Y-axis is the operating voltage. A typical frequency is 400 MHz, a typical test rate is 30 ns, and a typical voltage is 1.20 V. Shmoo plots show the operating margins for frequency and voltage. The higher the number of circles, the better the operating margin. For the seamless package, the minimum test rate was 23 ns and the minimum operating voltage was 0.85 V. This result shows that the seamless package has slightly wider operating margin than FCBGA. These results show that the seamless package has sufficient operating margin to be equivalent to the product.

The packages are then mounted on the personal-computer-like (PC-like) system boards. Since the seamless packages have low warpage characteristics, no specific process tuning is necessary for mounting. A cross-sectional view of the seamless package mounted on the PC-like system board is shown in Figure 3.21. All the BGA balls have almost the same height from one of the package edges to the other. This means that the seamless package achieves a stable connection to the system board. The PC-like system successfully operates with the seamless package.

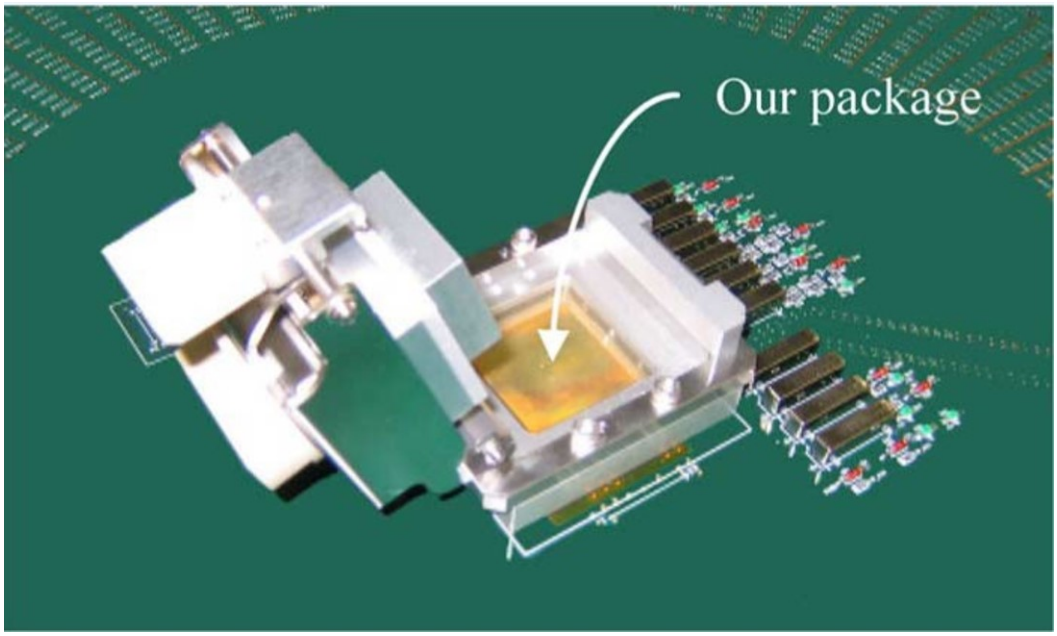


FIGURE 3.19: Top view of seamless package mounted on an LSI test socket for BGA with 625 balls on the printed circuit board.

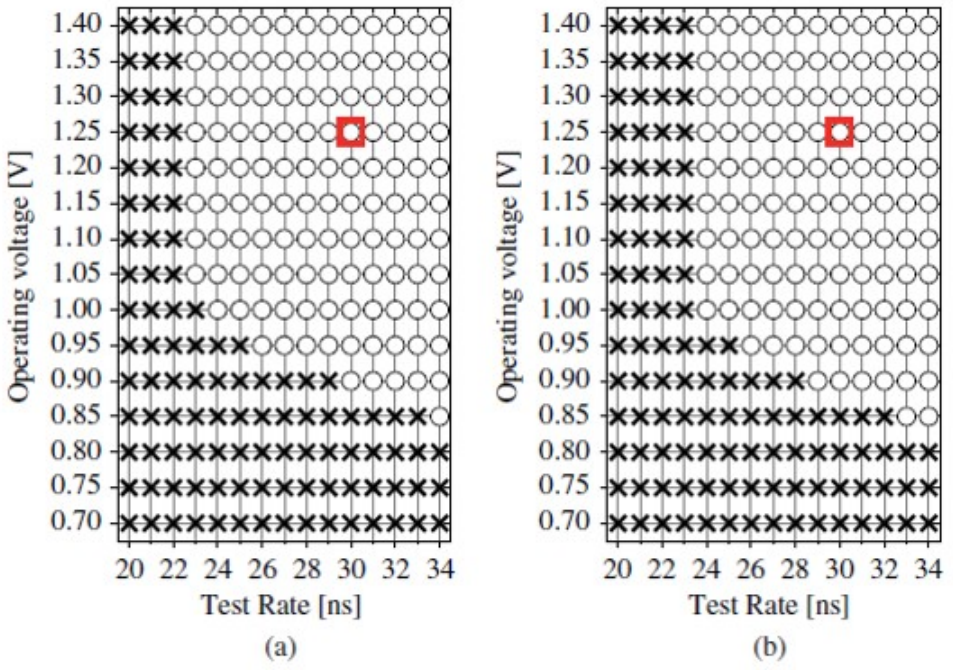


FIGURE 3.20: Comparison of shmoo plots of LSI package for (a) reference FCBGA package and (b) seamless package.

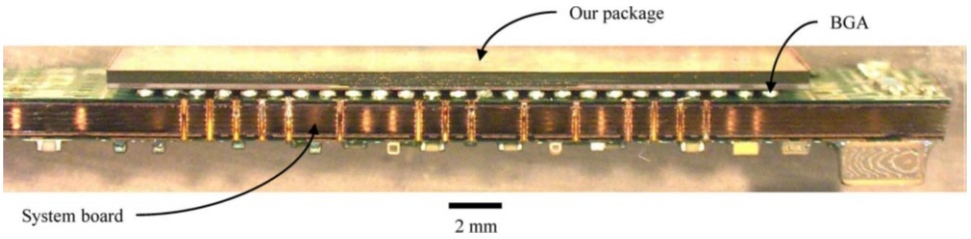


FIGURE 3.21: Cross-sectional view of prototype package mounted on system board.

3.7 Reliability

3.7.1 Package Level Reliability

The reliability of the seamless package at the package level using thermal cycle testing was evaluated. Since a fully functional chip was embedded, an LSI function tester for pass/fail evaluation during the thermal cycling (-40°C for 30 min and 125°C for 30 min), as shown in Figure 3.19 was used. Before the test, the package was pre-treated under the conditions corresponding to JEDEC level 3. Figure 3.22 shows the voltage shifts of four main I/O signals from the initial to 2000 cycles. The voltages of all the I/O signals retain very stable in between two critical values, showing as maximum and minimum in Figure 3.22, for all the cycle range. In conclusion, the package passed all LSI function tests, including an at-speed test, scan test and etc, even after 2000 cycles. This seamless package thus has excellent long-term reliability at the package level.

Next, the grain shape and crystal orientation of the direct Cu interconnection was examined before and after 2000 thermal cycles using electron backscatter diffraction (EBSD) analysis. The analysis revealed that the grain size and crystal orientation distribution after the 2000 thermal cycles remained unchanged from those before the thermal cycling, as shown in Figure 3.23. This means that the microstructures of the interconnection after 2000 thermal cycles had no texture during recrystallization and grain growth generated by thermal stress. After that, the microstructure of the sputtered seed metal layer at the boundary of a Cu post and Cu wiring was observed before and after 2000 thermal cycles by using transmission electron microscopy (TEM). Examination of the image shown in Figure 3.24 showed that the seed layer was 50 nm thick and that the crystal growth from the Cu post surface had a columnar structure. It was found no significant voids or cracks at the interface before and after 2000 thermal cycles.

The seamless interconnect is realized by direct Cu plating at room temperature. Therefore, no residual stress is generated at the bonding interface as in the case of connections using solder balls, and there is no longer any concern about delamination failure of multilayer wiring with fragile low-k layers.

3.7.2 Board Level Reliability

Next, a board level reliability test of the seamless package using thermal cycle testing was evaluated. The seamless package was mounted on the test boards, as shown in Figure 3.25. Since the seamless package itself had low warpage characteristics, no specific process tuning was necessary for mounting. The package warpage on the board was then measured by shadow moiré method. The package showed small warpage characteristics: 43 μm at room temperature, which is quite small for a large (27 mm x 27 mm) package, as shown in Figure 3.26. A 2000 thermal cycle testing (-40°C for 30 min and 125°C for 30 min) was performed using the test boards.

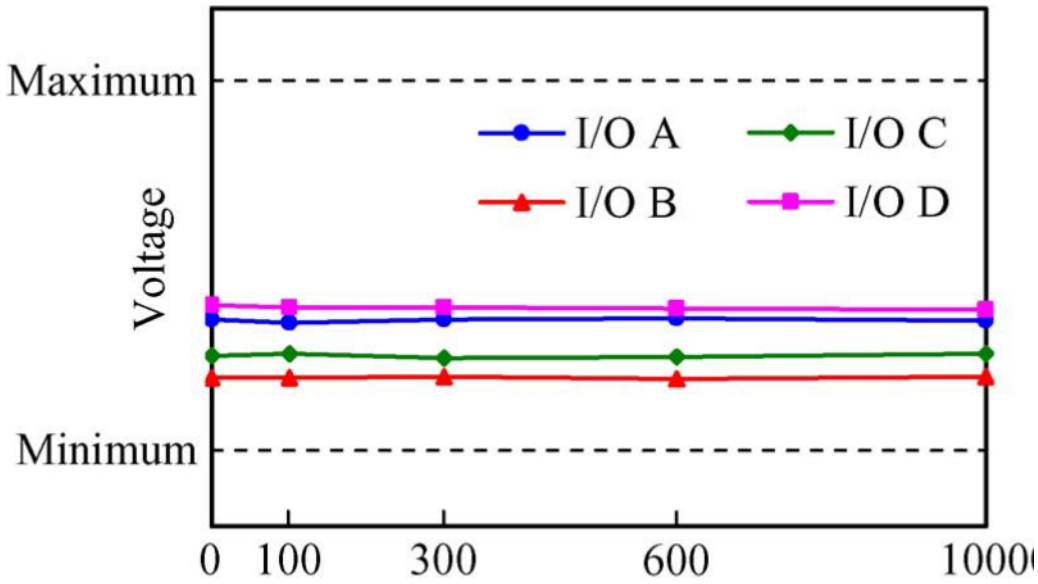


FIGURE 3.22: Voltage shifts of four main I/O signals for 1000 cycles.

The reliability at the board level was analyzed by observing the fracture mode transition of BGA solder ball (Sn:96.5%, Ag:3.0%, Cu:0.5%) between the package and test board after 2000 thermal cycles. It was also compared with FCBGA package having the same chip. The observation was focused on the region of the BGA solder ball under the chip edge as the stress concentration area, as shown in Figure 3.25. Figures 3.27 and 3.28 show field emission scanning electron microscope (FE-SEM) cross-sectional images of the BGA solder ball for seamless package and FCBGA package after 2000 thermal cycles, respectively. A crack of BGA solder ball of seamless package was only at the upper left and only about 40 μm long, while cracks of BGA solder ball of FCBGA package were at three corners and crack at the lower left was about 60 μm long. Observation of the microstructures of the BGA solder balls, particularly the grain size and crystal orientation using EBSD analysis, revealed some degradation for both cases, as shown in Figure 3.29. This degradation was the formation of recrystallization grains grown around cracks in the BGA solder ball in both packages.

Next, a strain gauge was used to estimate the changes in the strain (-40 to 125°C) at the surface of the seamless package and the FCBGA package. The two sensors used to measure the strain were attached at the center and edge of these packages mounted on a product system board. Figure 3.30 shows top view of the seamless package on the board, indicating the locations of attached strain gauges. The entire surface of the seamless package was covered by the Cu plate while that of the FCBGA package consisted of the LSI chip at the center and a build-up substrate around the periphery. For the seamless package, the temperature dependences of the strain at the center and edge were about the same, as shown in Figure 3.31. These uniform characteristics were attributed to the flat Cu plate. In contrast, they were quite different for the FCBGA, as shown in Figure 3.32. The center portion,

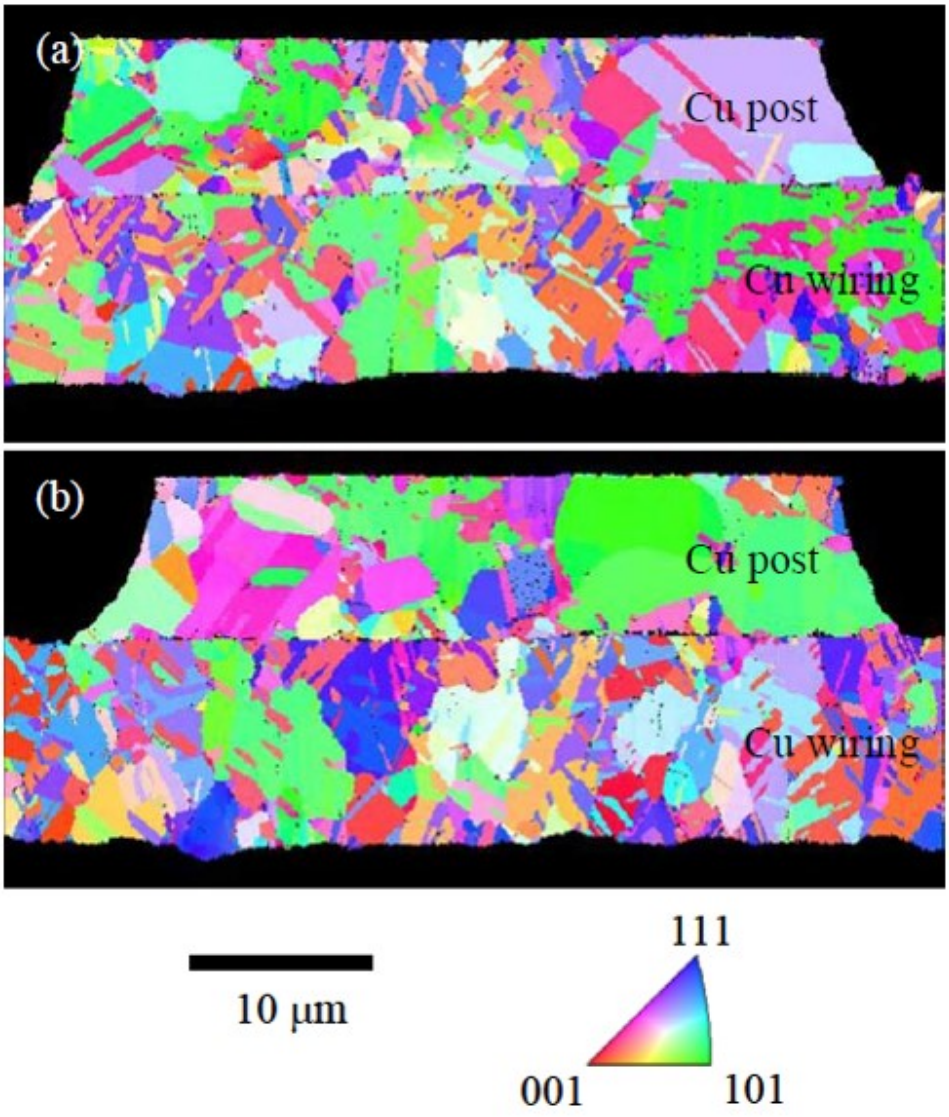


FIGURE 3.23: Maps of crystal orientation for Cu-Cu interconnection (reference direction). (a) before thermal cycling and (b) after 2000 thermal cycles.

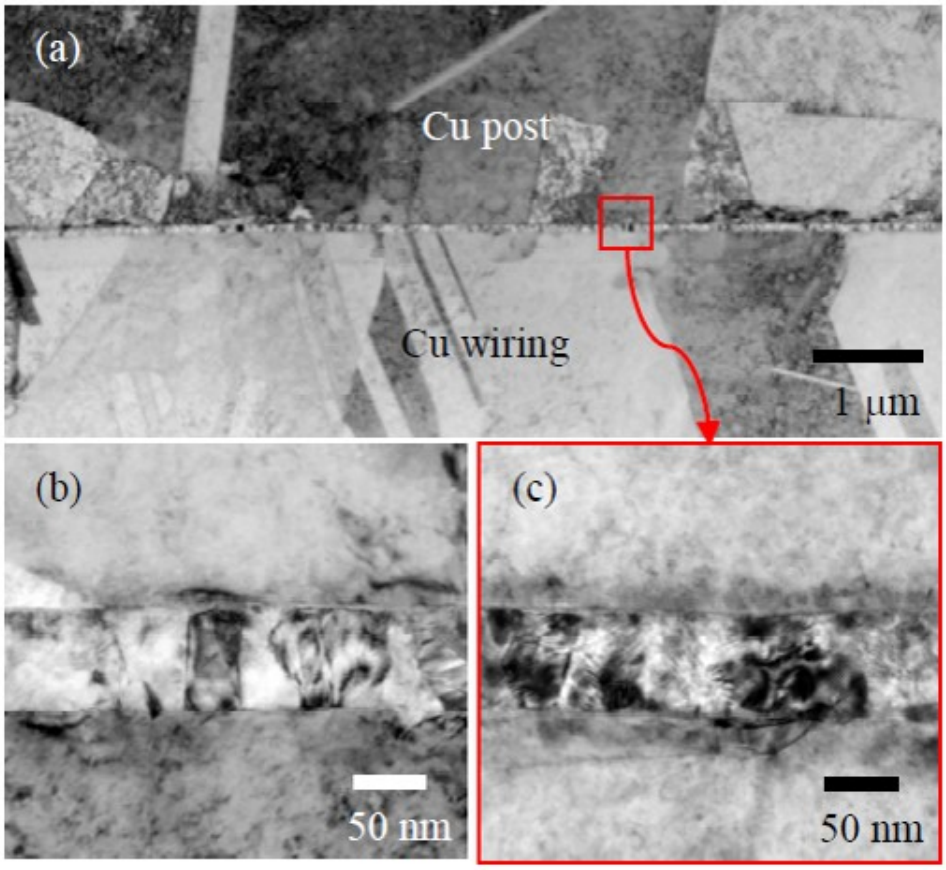


FIGURE 3.24: TEM cross-sectional images of seamless interconnect structure. (a) , (c) after 2000 thermal cycles. (b) before thermal cycling.

corresponding to the silicon chip, showed smaller strain than that for the FCBGA substrate. This indicates that the FCBGA might have some potential risks under thermal conditions.

These evaluations using the thermal cycles testing, the shadow-moiré method and strain gauge measurement indicate a possibility for highly board level reliability of the seamless package, compared to that of FCBGA package. These advantages are all considered to be due to the structure of the chip embedded into the package substrate and the presence of a Cu plate on the back of the thin chip.

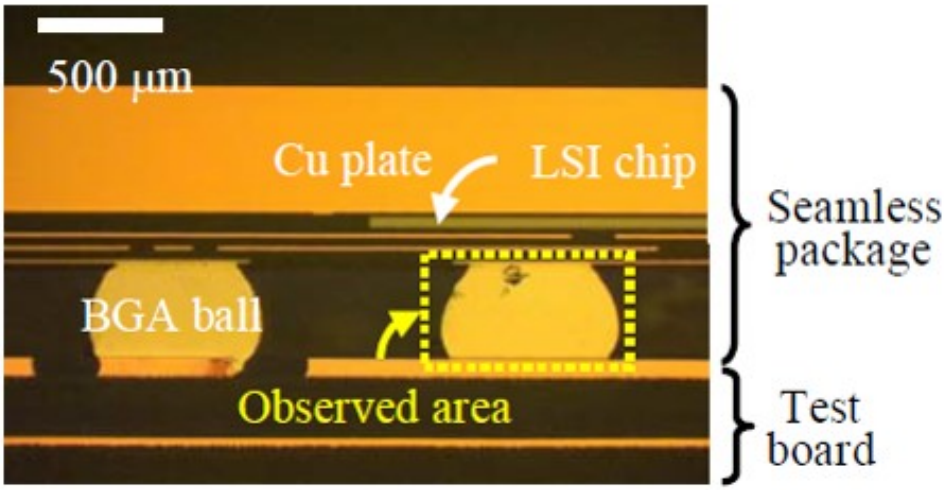


FIGURE 3.25: Cross-sectional view at board level after 2000 thermal cycles.

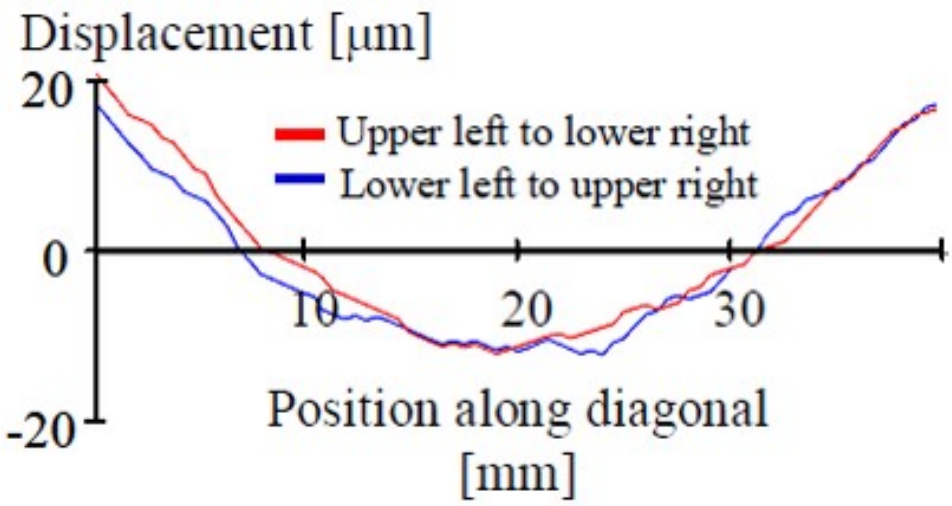


FIGURE 3.26: Warpage of seamless package mounted on system board extracted by shadow-moiré measurement.

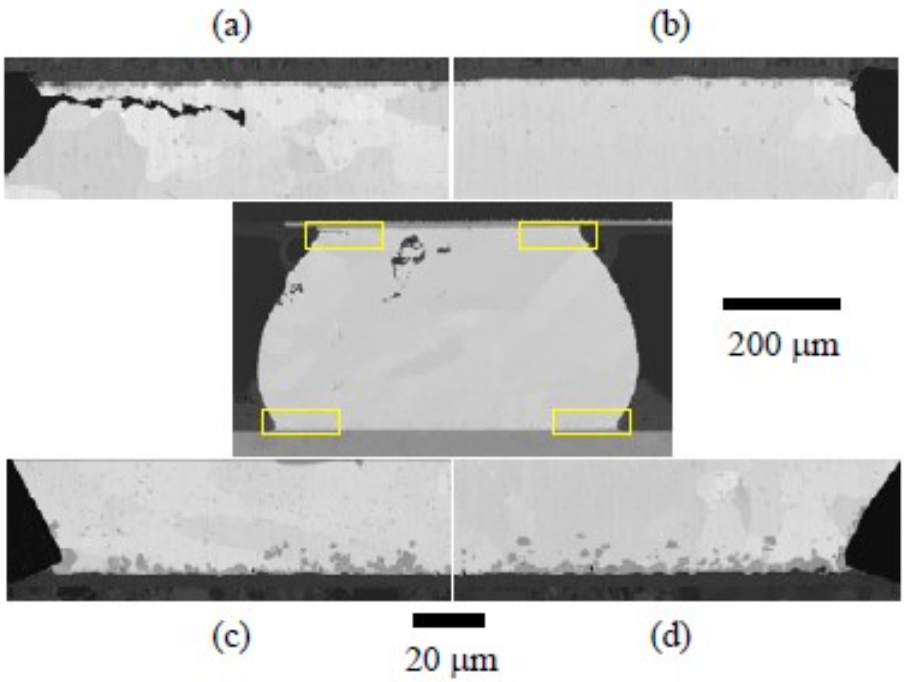


FIGURE 3.27: FE-SEM cross-sectional images of BGA solder ball for seamless package after 2000 thermal cycles. (a) upper left. (b) upper right. (c) lower left. (d) lower right.

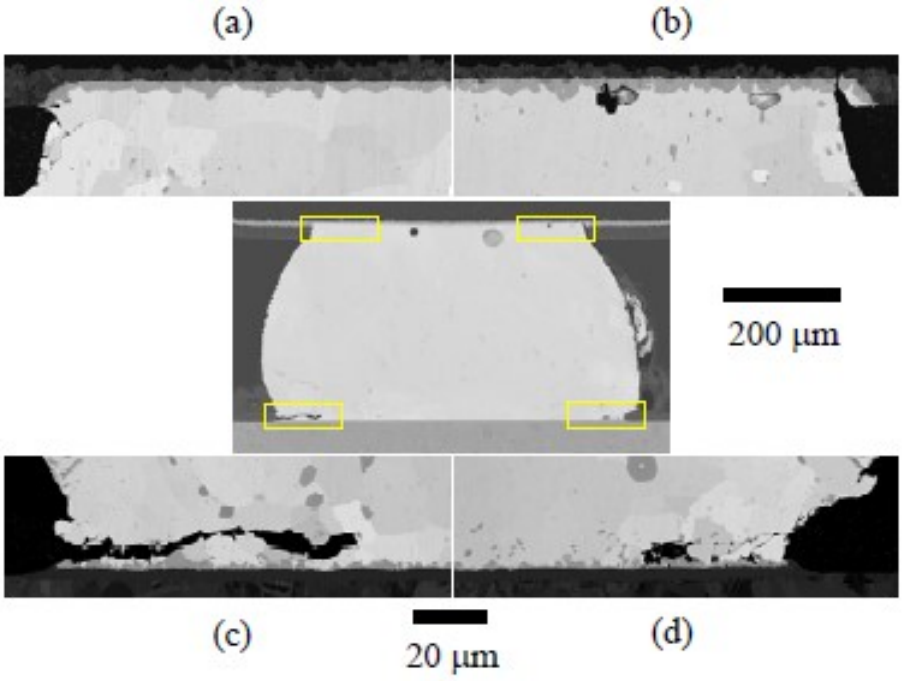


FIGURE 3.28: FE-SEM cross-sectional images of BGA solder ball for FCBGA package after 2000 thermal cycles. (a) upper left. (b) upper right. (c) lower left. (d) lower right.

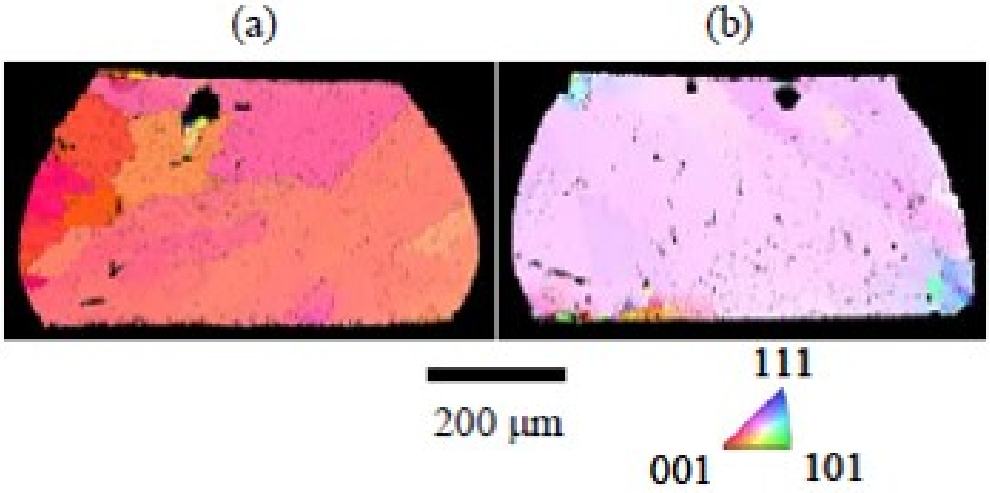


FIGURE 3.29: Maps of crystal orientation for BGA solder ball after 2000 thermal cycles (reference direction). (a) seamless package. (b) FCBGA package.

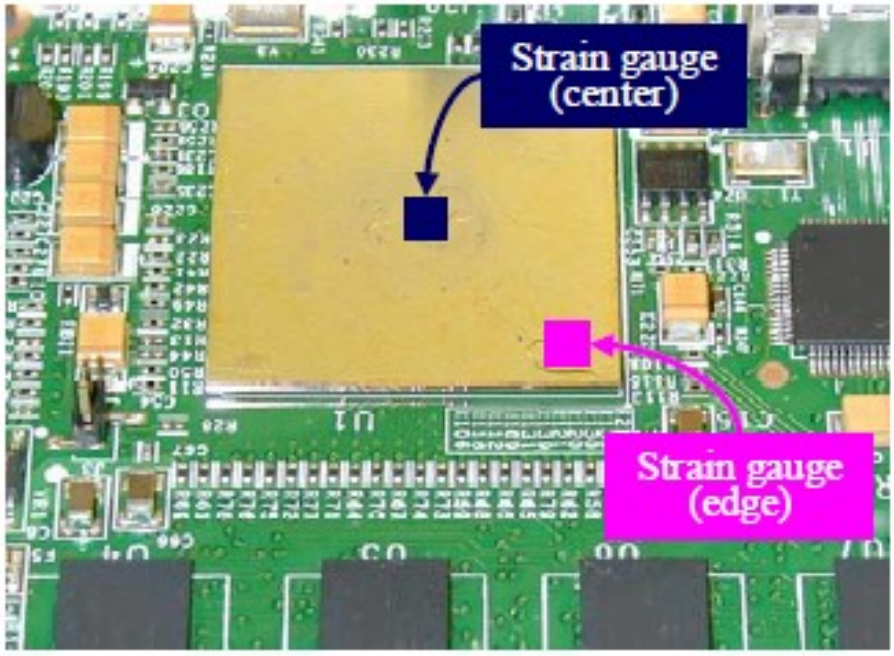


FIGURE 3.30: Top view of seamless package mounted on a product system board.

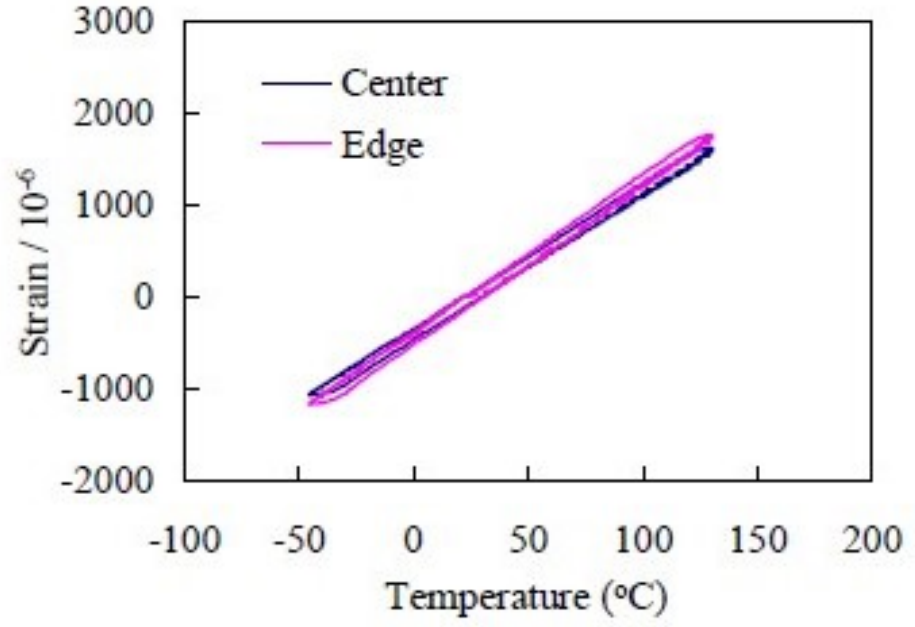


FIGURE 3.31: Strain versus temperature for seamless package.

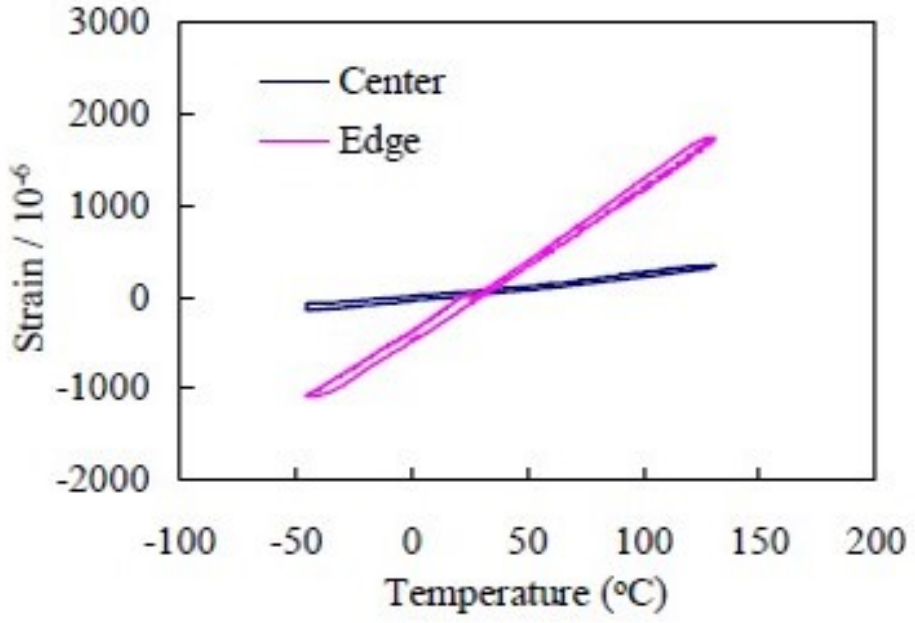


FIGURE 3.32: Strain versus temperature for FCBGA package.

3.8 Strip Line Structure using the Cu Plate

To improve crosstalk tolerance, a strip line structure sandwiching 1st metal layer (signal traces) between the Cu plate and 2nd metal layer (ground layer) was evaluated [60]. This structure improved the electrical performance of the LSI package, due to the absence of large size through-holes in conventional build-up substrates. Furthermore, the ground plane was connected to the Cu plate by additional die-side vias, as shown in Figure 3.33, which improved signal integrity. Near magnetic field over the package was measured at the CPU operating frequency of 400 MHz. The seamless package is mounted on the motherboard of the PC system, and the measurement area for the near field is the top surface of the seamless package, about 0.1 mm away from the Cu plate (Figure 3.34). Figure 3.35 shows the results of the measurements. Resonance of the floating Cu plate is observed in Figure 3.35 (b), but resonance of the Cu plate connected to the ground plane is not observed in Figure 3.35 (a). The results showed that the Cu plate functioned as a ground plane and improved the electrical characteristics of the LSI package.

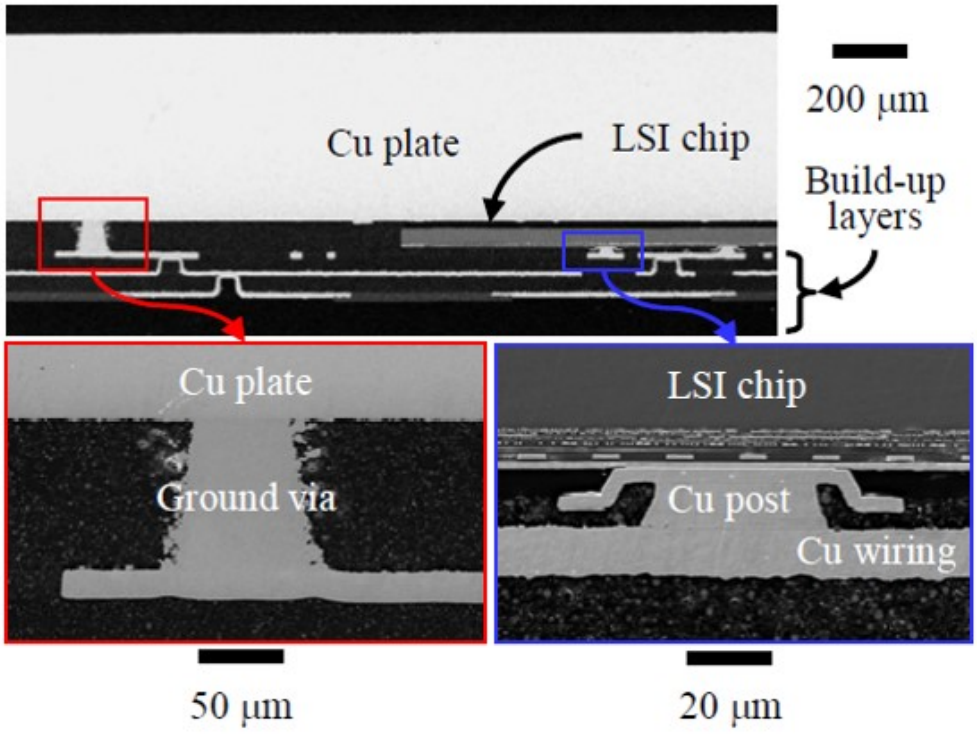


FIGURE 3.33: SEM cross-sectional images of seamless package.

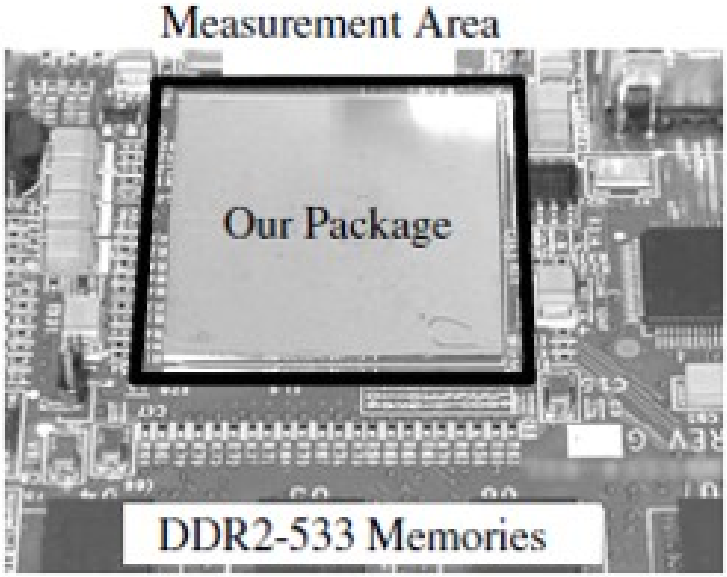


FIGURE 3.34: Measurement area of near magnetic field.

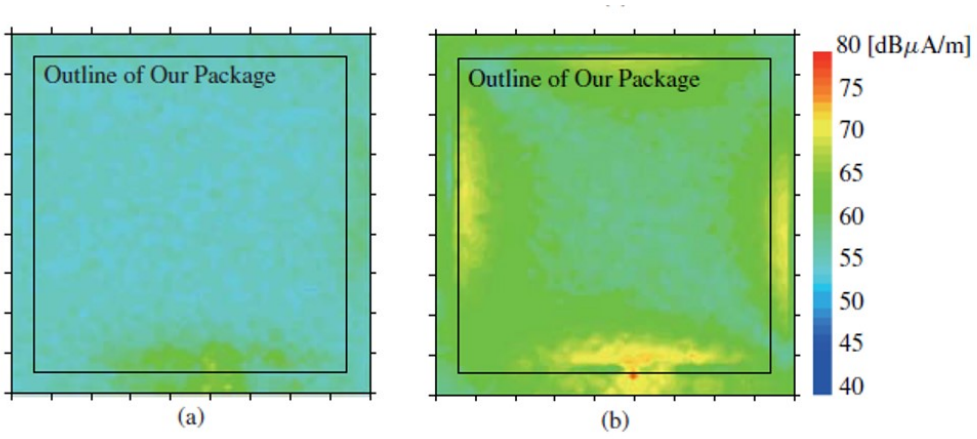


FIGURE 3.35: Results of near magnetic field measurement around the package at 400 MHz. (a) seamless package connecting the Cu plate to the ground plane. (b) seamless package without connecting the Cu plate to the ground plane.

3.9 Summary

A thin, reliable, low-warpage, and low-thermal-resistance LSI package was successfully developed by using novel embedded active die technology. The embedded microprocessor with approximately 1500 pads and a thickness of 50 μm operates in both the LSI tester and in PC-like systems. The total package thickness is only 710 μm, including the 500-μm-thick Cu plate as a cooling part. The thickness is one-fifteenth of that of the reference FCBGA with heat sink. Even without the heat sink, the reference FCBGA is 1.9 mm in thickness, which is 2.6 times as thick as the seamless package. The seamless package shows excellent warpage of only 34 μm at room temperature even for a 27 mm x 27 mm package. When the Cu plate is thinned to 250-μm-thick, the total package thickness is only 460 μm, achieving acceptable warpage with a maximum value of 117 μm at room temperature. For the package with 500-μm-thick Cu plate, low thermal resistance of 10.8 °C/W is achieved at 0 m/s, comparable to the FCBGA with a heat sink. The package passes the 2000-cycle package-level and board-level thermal cycle test (-40°C for 30 min and 125°C for 30 min). The reliability of the seamless package at the package and board level using thermal cycle testing was evaluated. In conclusion, the seamless package passed all LSI functional tests after 2000 thermal cycle test in package-level, and BGA ball strain was confirmed to be less than that of a conventional FCBGA in board-level. In the miniaturization of LSI multi-layer wiring, this seamless interconnect between chip and package is expected to be a promising technology as a way to achieve high-density and reliable system integration.

Chapter 4

5-in-1 Fan-Out Wafer-Level Packaging Technology with One Logic and Four Memory Dies for Internet of Things Modules

4.1 Background

The major package used for central processing units (CPUs) and graphics processing units (GPUs) including artificial intelligence (AI) engines is the flip chip ball grid array (FCBGA), which uses solder bumps or micro bumps to connect the die to the organic substrate [61], [62] (Figure 4.1 (a)). Owing to the increased size of organic substrates accompanying higher performance devices and limitations on interconnection pitch between devices and organic substrates, it is becoming increasingly difficult for conventional packaging technologies to meet the demands for higher performance and speed [63]. Fan-Out Wafer-Level Packaging (FOWLP), which eliminates the organic substrate, is an integrated circuit packaging technology in which the fine redistribution layer (RDL) formed on the LSI chip extends beyond the chip outline [21], [64]. Die-first FOWLPs have been widely used in mobile and consumer applications such as application processors, power management ICs, baseband processors, radio frequency ICs, and microcontrollers. However, the applicable package size of FOWLP is typically approximately 8 mm × 8 mm or less due to the package warpage issue and cost advantages compared over conventional FCBGAs, and it has not been applied to high-performance computing (HPC) [65]. As a result, the more expensive 2.5D technology with silicon interposer is therefore still used, and the range of applications of FOWLP has not grown [17], [66]. To select FOWLP as a package solution for HPC, small die shift, low warpage, and multi-layer fine RDL formation are critical challenges. Compression molding using the epoxy-based liquid compression molding (LCM) material is one of the key

processes that affect the three challenges [67], [68].

In this study, I focus on the mold resin of FOWLP and propose a novel 2D FOWLP structure and process to solve the above three issues (die shift, warpage, and multi RDL formation) [69]. The stress of the mold resin is directly proportional to the elastic modulus according to Hooke's law. By changing the structure of the organic molecular material of the mold resin from conventional epoxy to silicone, the modulus of elasticity is targeted to be less than 1.0 GPa compared to the conventional 20 GPa. I demonstrate a novel die-first FOWLP using a low elastic modulus resin, which is different from the conventional LCM. A 5-in-1 FOWLP containing a GPU die with over 2500 pins as an AI die and four DRAM dies placed side by side is developed in 31 mm × 31 mm package size (Figure 4.1 (b)), and the functional operation is demonstrated.

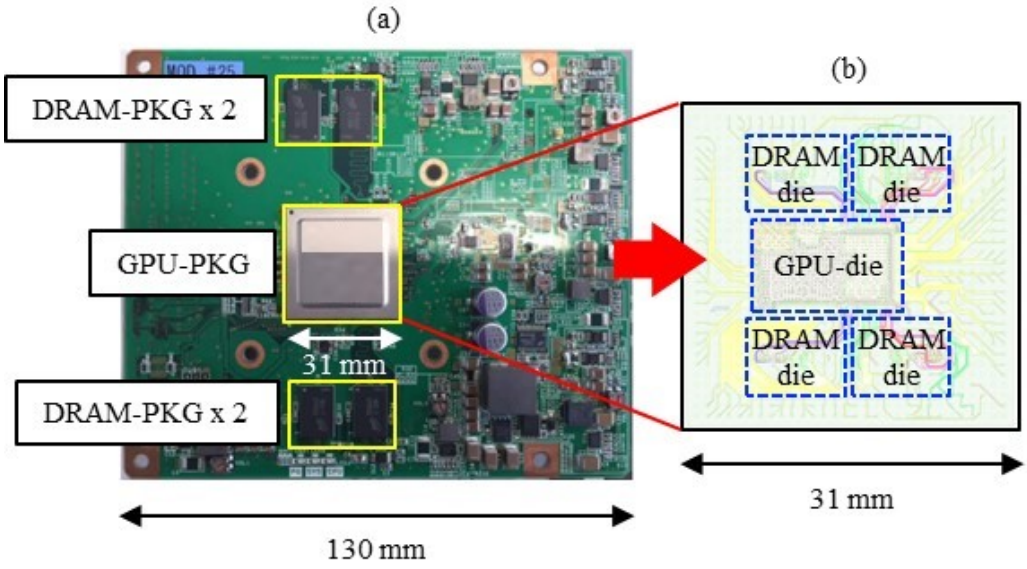


FIGURE 4.1: Objectives of the research. (a) Computer circuit board with GPU-PKG and 4 DRAM packages. (b) 5-in-1 FOWLP with GPU die and four DRAM dies.

4.2 Issues and Solutions for FOWLP

The FOWLP fabrication process consists of three basic flows [70]–[72]. Figure 4.2 shows a simplified illustration of the manufacturing process flows. There are differences in the process to electrically connect the die to the RDL. In the die-first (face-down) process, after the die is mounted face-down on the support substrate, the mold resin is encapsulated and the support substrate is removed. Next, the RDL is formed by Cu plating on the die pad [73], [74]. In the die-first (face-up) process, after the die is mounted face-up on the support substrate, the mold resin is encapsulated and the surface of the Cu pillars on the die is exposed by CMP. Next, the RDL is formed by Cu plating on the Cu pillars, and the support substrate

is removed [75], [76]. In the RDL first process, after the RDL is formed on the support substrate, the die is connected using solder bumps. Next, the mold resin is encapsulated, and the support substrate is removed [77], [78].

In this study, a die-first (face-down) process is selected as the fabrication process because the corresponding mass production technology has already been well established. In addition, unlike other processes, the die-first (face-down) process does not require any components (e.g., Cu pillars, solder bumps) to connect to the RDL, thereby reducing the manufacturing cost. The objective in this study is to realize an unprecedented module that integrates five dies side by side and forms a multilayer RDL in a 31 mm × 31 mm FOWLP. The following are reported as major technical challenges for present FOWLPs.
(1) Die shift
(2) Warpage of reconstituted wafer
(3) Multi-layered fine RDL formation

Die shift refers to the movement of the die from its initial mounting position during resin molding, debonding of the support substrate, and cooling after the reconstituted wafer has been thermally cured [79]–[81]. A reconstituted wafer is a wafer in which dies are mounted on a support substrate and then encapsulated with mold resin. Warpage of the reconstituted wafer is generated by the difference in thermal expansion coefficient between the mold resin and the support substrate (Si or glass or organic or metal, etc.) [82]–[84]. If the die shift and the warpage of the reconstituted wafer are large, it is difficult to form a multi-layered fine RDL.

These issues are mainly affected by the mechanical properties of the mold resin. To solve these issues, a low elastic modulus material is adopted for the mold resin that forms the reconstituted wafer. In addition, a new process is developed to control warpage by placing the Si support substrate on the backside of the mold resin. By using the reconstituted wafer reduced die shift and wafer warpage due to the introduction of new material and process, the process of implementing a multi-layered fine RDL to create a 5-in-1 FOWLP is evaluated.

4.3 5-in-1 FOWLP Technology

4.3.1 Layer-pattern Designs

In order to make the wiring length between the GPU and each DRAM the same, the four DRAM dies were designed to be placed around the GPU die. Signal integrity (SI) and power integrity (PI) simulations were performed using the designed pattern. Frequencies of up to 800 MHz were used in the SI simulation, and voltage and current values of up to 1.5 V and 20 A were used in the PI simulation. The initial design used two RDL layers, but the results of the SI simulation showed that the eye diagram did not meet the criteria (± 0.3 V) for some clocks (Figure 4.3 (a)). Therefore,

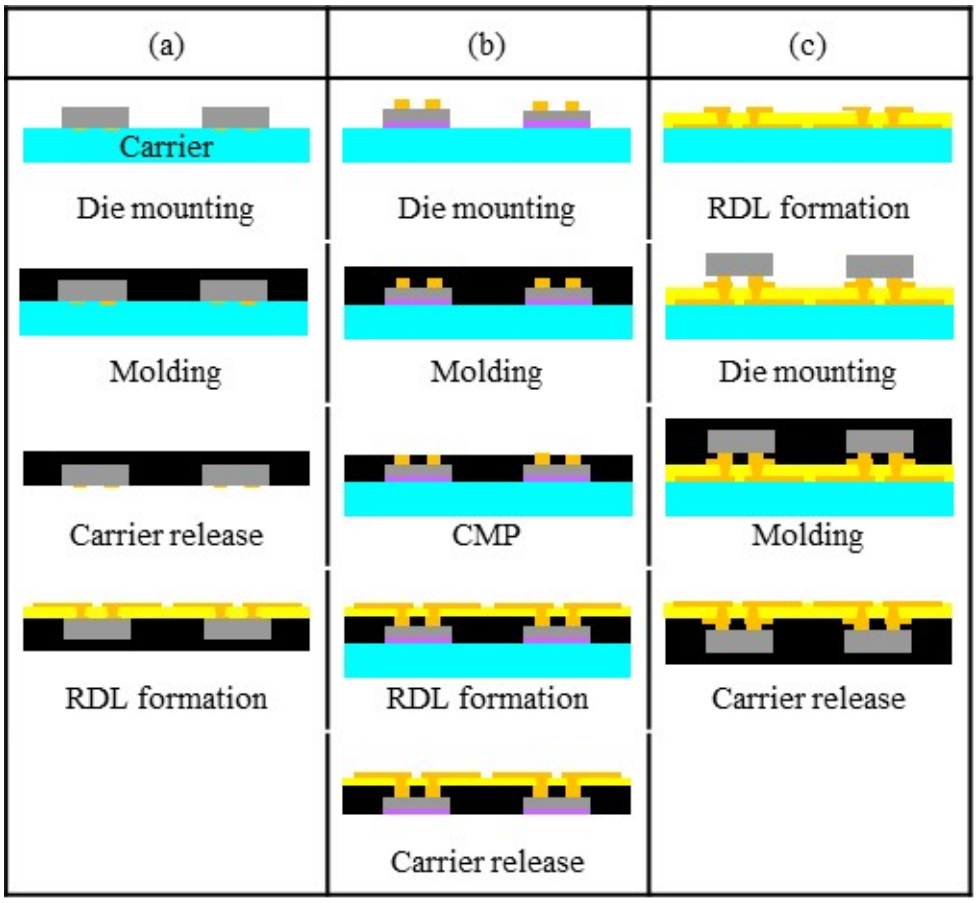


FIGURE 4.2: Comparison with process flow for conventional FOWLP.
(a) Die-first/face-down. (b) Die-first/face-up. (c) RDL-first.

the design was changed to use three RDL layers with an enhanced power supply in the second layer. As a result of the redesign, SI simulation of the three RDL layers obtained a good eye diagram (Figure 4.3 (b)). Figure 4.4 shows the wiring layout with three RDLs of FOWLP. The first layer is mainly signal and power, the second layer is mainly power, and the third layer is mainly power and ground.

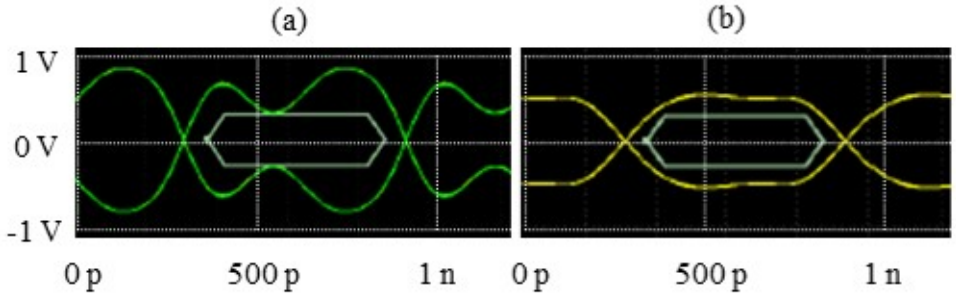


FIGURE 4.3: Comparison of the eye diagrams for signal integrity simulation. (a) Two layers. (b) Three layers.

4.3.2 Mold Material

In order to prevent die shift and realize low warpage, a mold resin with a low elastic modulus that has excellent stress relaxation was employed. Table 4.1 shows the mechanical properties of the developed mold resin. The base of the material is silicone and there is no filler in it. The Young's modulus of the material is about 50 MPa, which is much lower than that of the materials used in conventional FOWLPs (>20 GPa) [85], [86].

TABLE 4.1: Material properties of mold compound.

Item	Unit	General properties
Material type	-	Silicone resin w/o filler
Appearance	Color	Black
Young's modulus	MPa	about 50
Elongation	%	about 50
CTE	ppm/K	about 170

4.3.3 Fabrication Process

Table 4.2 shows the GPU and DRAM die specifications. The GPU has a die size of 14.3 mm × 8.9 mm, a pad pitch of 180 μm and 2500 pads, and the DRAM has a die size of 8.1 mm × 9.4 mm, a minimum pad pitch of 82 μm and 155 pads. Table 4.3 shows the package specifications for the 5-in-1 FOWLP. The package was designed to have the same size and the same number of external pins as the GPU package on the computer circuit board, as shown in Figure 4.1 (a), to demonstrate the operation of the system board. The process flow of the developed FOWLP is

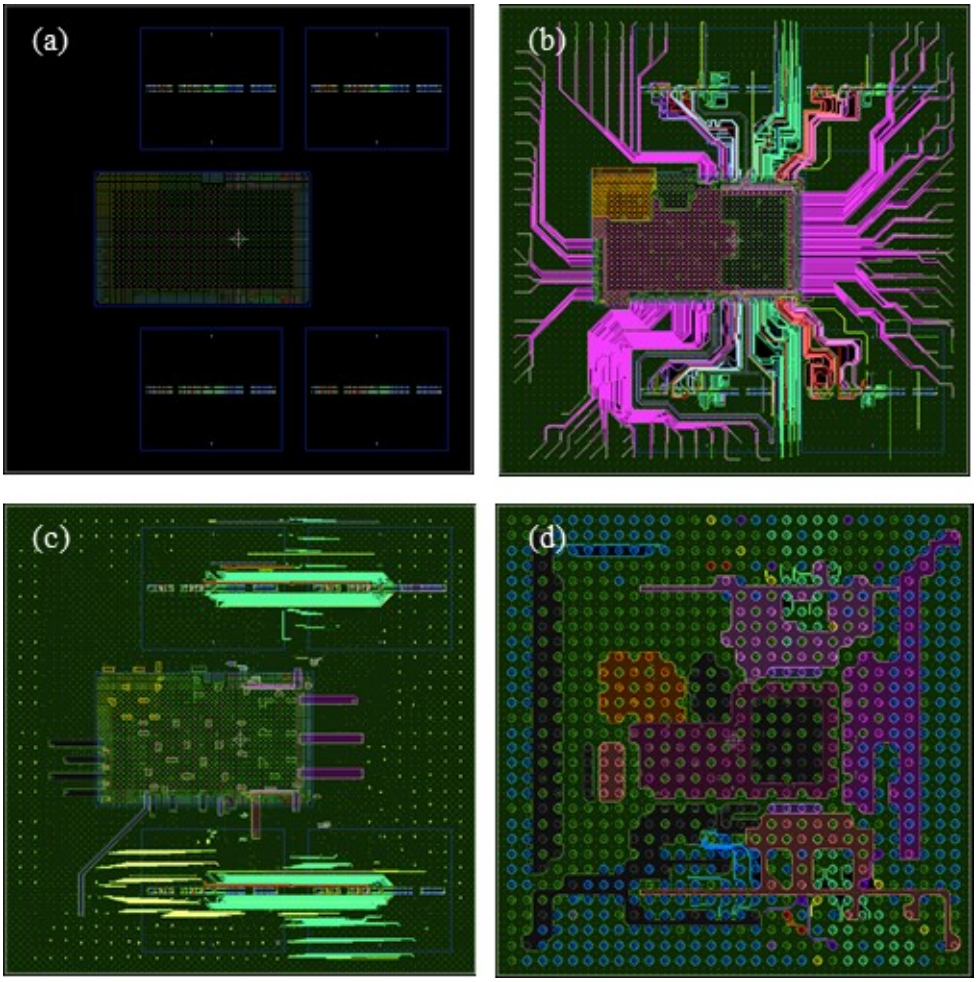


FIGURE 4.4: Layer-pattern designs for the 5-in-1 FOWLP.
(a) Die layout: consists of a GPU die and four DRAM dies. (b) 1st metal layer: mainly used for signal and power traces. (c) 2nd metal layer: mainly used as a ground plane. (d) 3rd metal layer: used for power traces and BGA pads.

shown in Figure 4.5. First, the release layer was deposited on an 8-inch diameter glass substrate, and then the die was mounted face-down using a flip chip bonder. The mounting conditions were a 9 N load, 60°C, and 500 ms. The mold resin was then deposited by a printing method. A metal mask was placed on the top surface of the glass substrate on which the die was mounted, and printing was performed twice at room temperature using conditions of 4 kgf load and 5 mm/s squeegee speed. The thickness of the mold resin on the backside on the embedded dies was controlled to be about 20 μm. After printing, the mold resin was temporarily cured (100°C, 30 min). The mold resin has a low elastic modulus and is expected to prevent die shift and reduce warpage. However, the mold resin cannot stand on its own and has issues with transportability during manufacturing. Therefore, after forming the mold resin, an 8-inch-diameter Si support substrate (725 μm thickness) was bonded to the back of the mold resin using wafer bonder. The bonding conditions used were 8 kN load, 100°C, and 180 s. Next, the mold resin was subjected to full curing (210°C, 4 h). The Si support substrate was used as part of the package product without being removed. Next, the glass substrate was peeled off from the reconstituted wafer with the Si substrate at the interface of the release layer to expose the electrodes of the embedded die. Then, RDLs with three layers of Cu plating were formed using a semi-additive process. Siloxane-based dielectric material with material properties similar to mold resin was used as the insulating layers, and a via of minimum diameter 35 μm was formed on land of diameter 55 μm with an exposure dose of 1600 mJ/cm^2. Ti (45 nm)/Cu (300 nm) was formed as the seed layer by a sputtering system, and the RDL was formed with a minimum line and space rules of 10 μm/20 μm. The three-layer RDL had the Cu wiring thickness of 8 μm and the dielectric layer thickness of 15 μm. Finally, after mounting BGA balls, the 5-in-1 FOWLP was manufactured in 31-mm square pieces by blade dicing process.

TABLE 4.2: Die specifications.

GPU	Size (mm)	14.3 x 8.9
	Pad pitch (μm)	180 (min)
	Pad count	>2500
	Thickness (μm)	150
DRAM	Size (mm)	8.1 × 9.4
	Pad pitch (μm)	82 (min)
	Pad count	155
	Thickness (μm)	150

4.4 Observation of RDLs

Figure 4.6 shows the BGA side and the backside of the developed FOWLP. It can be seen that BGA balls were mounted on the package surface side at a pitch of 1.0 mm, and a Si substrate (725-μm-thick) was placed on the backside of the package. Figure 4.7 shows a top view of the RDL layers, showing the 1st metal (L/S=10

TABLE 4.3: Package specifications.

RDL	Number of layers	3
	Metal 1	L/S = 10 μm/20 μm
	Metal 2	L/S = 20 μm/20 μm
	Metal 3	L/S = 30 μm/30 μm
	Via size (μm)	35ϕ
	Land size (μm)	55ϕ
Package	Size (mm)	31 x 31
	BGA ball pitch (mm)	1.0
	BGA pad count	900 (30 x 30)
	BGA ball height (mm)	0.5

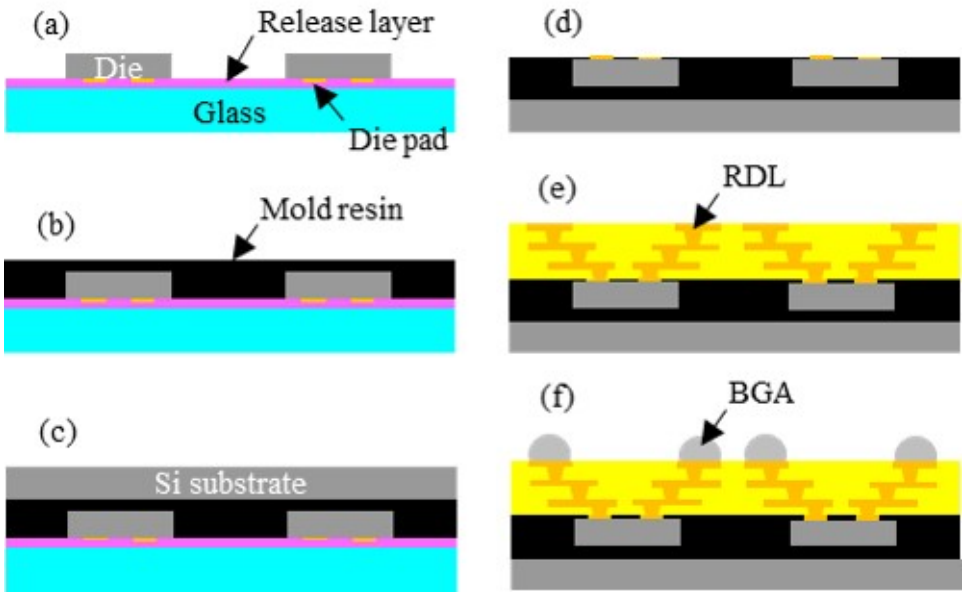


FIGURE 4.5: Process flow of newly developed 5-in-1 FOWLP. (a) Die mounting on a glass carrier with release layer. (b) Molding resin. (c) Si substrate bonding to the backside of the mold resin. (d) Release glass carrier. (e) RDL formation. (f) BGA formation.

μm/20 μm), 2nd metal (L/S=20 μm/20 μm), 3rd metal (L/S=30 μm/30 μm), and BGA balls. Figure 4.8 shows a cross-section of the package, where the Si support substrate (725-μm-thick) is placed on the backside of the GPU die (150-μm-thick) through the mold resin, and the three-layer RDLs with total thickness of 55 μm can be seen from the pads of the GPU die.

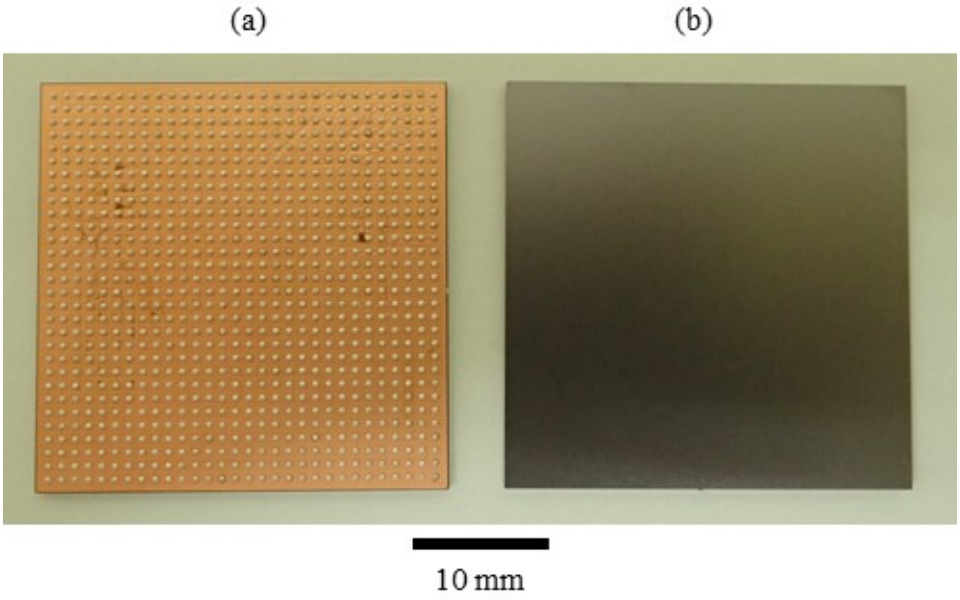


FIGURE 4.6: Photographs of the package as (a) BGA and (b) backside views.

4.5 Die Shift Measurement

Next, the die shift in the manufacturing process was evaluated. In the lithography process of reconstituted wafers, the amount of die shift should be small in order to avoid misalignment failure of pads and vias. The die shift was evaluated by fabricating 21 packages of size 31 mm × 31 mm using an 8-inch reconstituted wafer in this study. Figure 4.9 (a) shows a photograph of the GPU and DRAM after mounting on the glass carrier substrate, and Figure 4.9 (b) shows a photograph after the glass substrate was removed. After releasing the glass substrate, the amount of displacement between the pad position of the GPU in the package and the design target position was measured as the amount of die shift. The land diameter of the embedded die pad is 55 μm, and the via diameter connected to the pad is 35 μm, thus the criterion of die shift is ±10 μm in this study. Figure 4.10 shows the amount of die shift of the GPU at five locations (center, top, right, bottom, left) in the package of the 8-inch reconstituted wafer. This shows that the amount of die shift was less than ±5 μm, which is within the criterion of ±10 μm, indicating that the amount of die shift in the study is very small. This result shows that employing a low elasticity mold resin is effective for reducing the die shift in the reconstituted wafer.

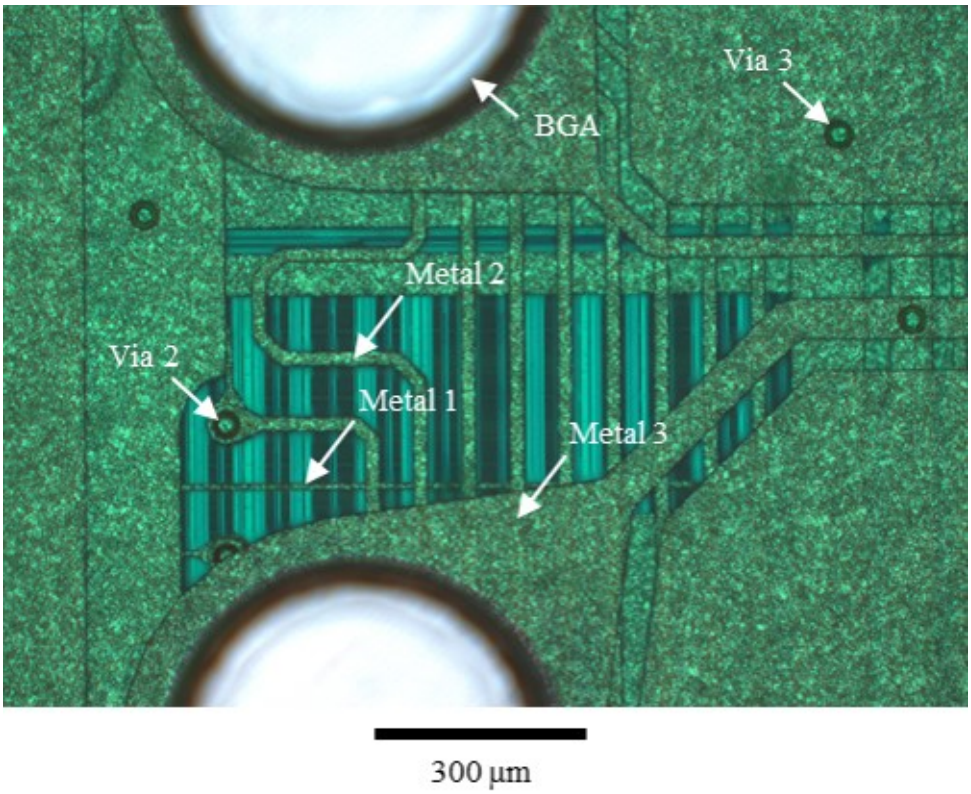


FIGURE 4.7: Top view of the 5-in-1 FOWLP.

4.6 Warpage Measurement

By adapting a low elasticity mold resin, the warpage of the reconstituted wafer was not a serious issue in forming the three-layer RDL. After the FOWLP was completed, the warpage of the package was evaluated at the package level and the mounted board level, respectively. The Si surface on the backside of the package was measured with a 3D laser measuring instrument. Figure 4.11 (a) shows the result of the package level warpage measurement. The amount of warpage of the package was 10.6 μm, which is very small for a package size of 31 mm × 31 mm, and is almost flat. This is thanks to the effect of the rigid Si support substrate placed on the backside of the low elasticity mold resin. Next, the package was placed on a computer circuit board and connected to the board using a reflow soldering processes (max temperature 260°C) with 900 BGA balls, as shown in Figure 4.12 (a). The warpage of the mounted package was measured in the same method. The shape of the package warpage is "Cry", which means that it is pulled toward the mounting substrate, which has a higher linear expansion coefficient than the Si substrate. The warpage was 125.5 μm, which is an increase compared with the package level. However, the amount of warpage was small compared to the pitch of BGA balls (1.0 mm) and BGA ball height (0.5 mm), and the electrical connections of all 900 pins were confirmed.

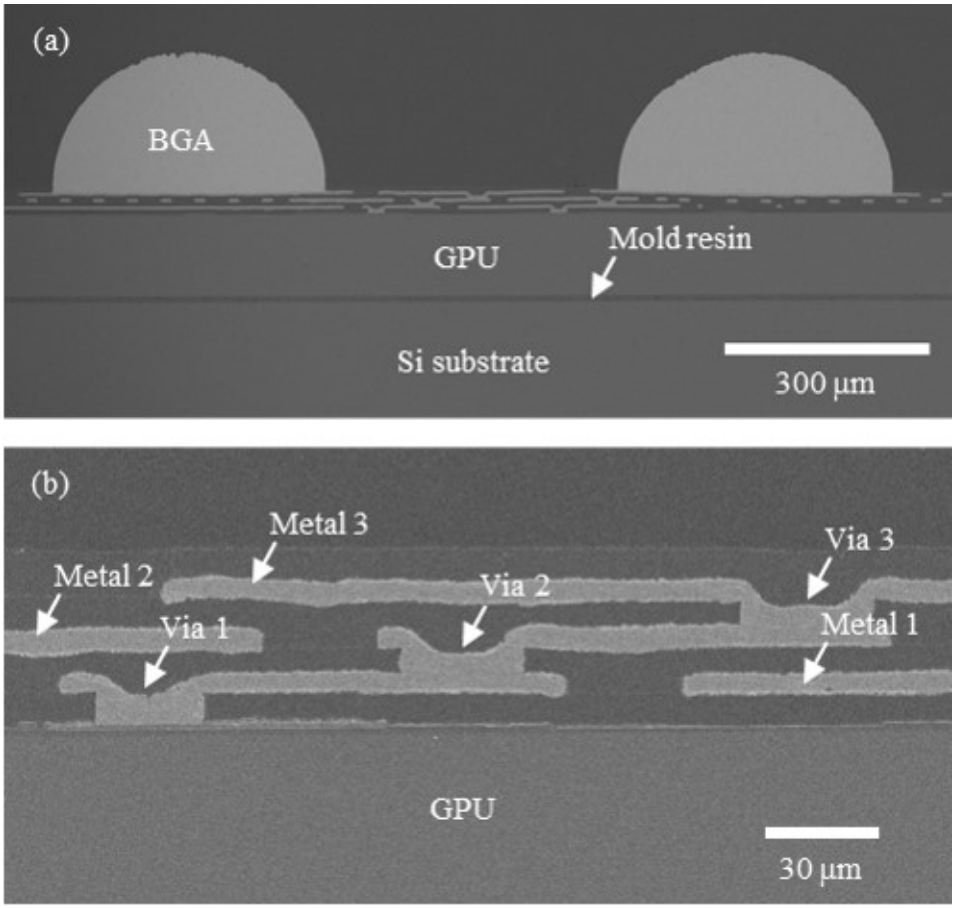


FIGURE 4.8: Cross-sectional views of the 5in1 FOWLP. (a) Package with BGA and Si substrate. (b) RDL area.

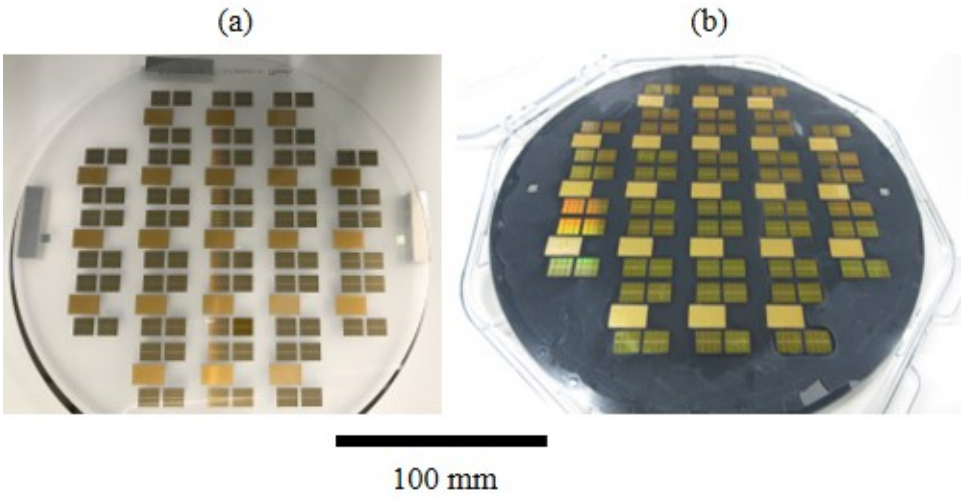


FIGURE 4.9: Photographs taken during production. (a) after die mounting. (b) after release from glass carrier.

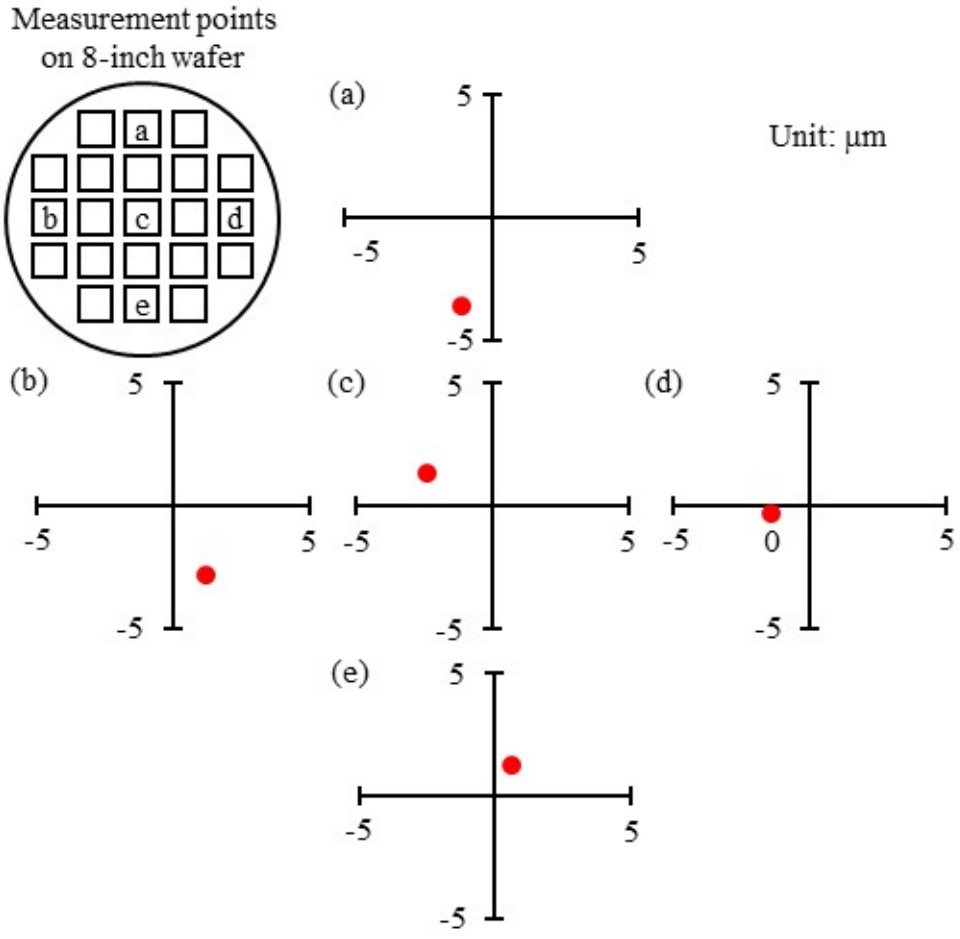


FIGURE 4.10: Die displacement results at five locations (center, top, right, bottom, left) after release from glass carrier.

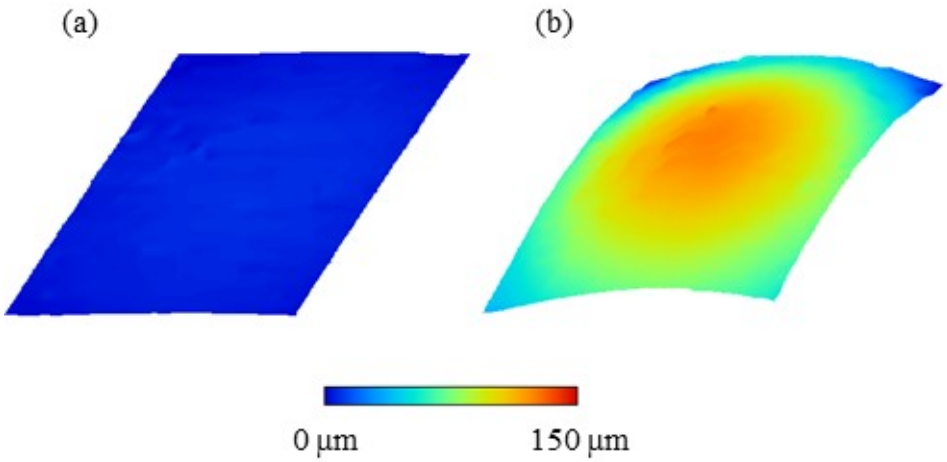


FIGURE 4.11: Warpage measurements. (a) Package level. (b) Board level.

4.7 Operation Verification

The sub-board on which the prototype 5-in-1 FOWLP was mounted was connected to a console equipped with input and output functions, as shown in Figure 4.12(b). A 12 V power supply was then supplied to confirm the operation of the FOWLP. The results confirmed that the GPU operates at an operating frequency of 800 MHz through the three-layer RDLs of the FOWLP at a voltage of 1.0 V.

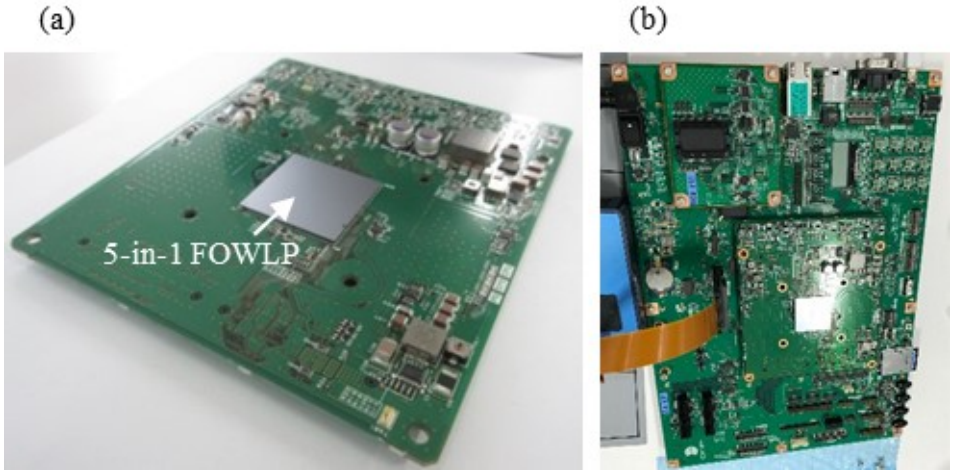


FIGURE 4.12: Top view of the 5-in-1 package mounted on the computer circuit board. (a) 5-in-1 FOWLP mounted on the sub-board. (b) Sub-board connected to the console.

4.8 Thermal Stress Analysis

Stress simulation analysis was performed using a new siloxane-based mold material developed in this study and a standard material currently used in the mass production of FOWLP. Table 4.4 shows the specific properties of the standard material. The simulation was analyzed at the package level model. ADVENTURECluster finite element analysis software was used for the stress simulation. In the simulation, all of the materials behaved as isotropic linear elastic materials. The cure temperature for the siloxane-based mold material is 210°C, while the cure temperature for the standard epoxy material is 260°C. To compare the relative stresses of the materials at different curing temperatures, the effective stress-free temperature was considered to be room temperature. The simulation compared the equivalent stress on the via (35 μm diameter, 10 μm height) on the embedded die under two temperature conditions (-55°C and 125°C). The simulation results showed that the maximum stress at -55°C for the new material was 591 MPa at the top of the via, while that at 125°C was 471 MPa at the bottom of the via. The results revealed that the stress concentration point changes with temperature (Figure 4.13). On the other hand, in the standard epoxy material, the maximum stress occurred at the bottom of the via, regardless of the temperature condition.

Figure 4.14 shows the stress analysis results for the new material and the standard epoxy material at -55°C and 125°C. The RDL between vias of the standard epoxy material was flat, whereas that of the new material was deformed under each temperature condition. In addition, the maximum stress of the new material was about 2.8 times higher at -55°C and about 1.7 times higher at 125°C than that of the standard material, as shown in Figure 4.15. These results showed that the new material had a tendency to increase the maximum stress owing to deformation of the RDL caused by thermal shrinkage because of the high CTE. In future development, the material property values of the siloxane-based dielectric material, such as low CTE and high elasticity, need to be optimized in order to ensure the reliable package.

TABLE 4.4: Material properties of the standard materials.

	Item	Unit	General properties
Mold material	Material type	-	Epoxy resin
	Young's modulus	GPa	22
	Tg	°C	165
	CTE	ppm/K	7
Inter layer dielectrics	Material type	-	Photosensitive phenolic resin
	Young's modulus	GPa	3.4
	Tg	°C	300
	CTE	ppm/K	46

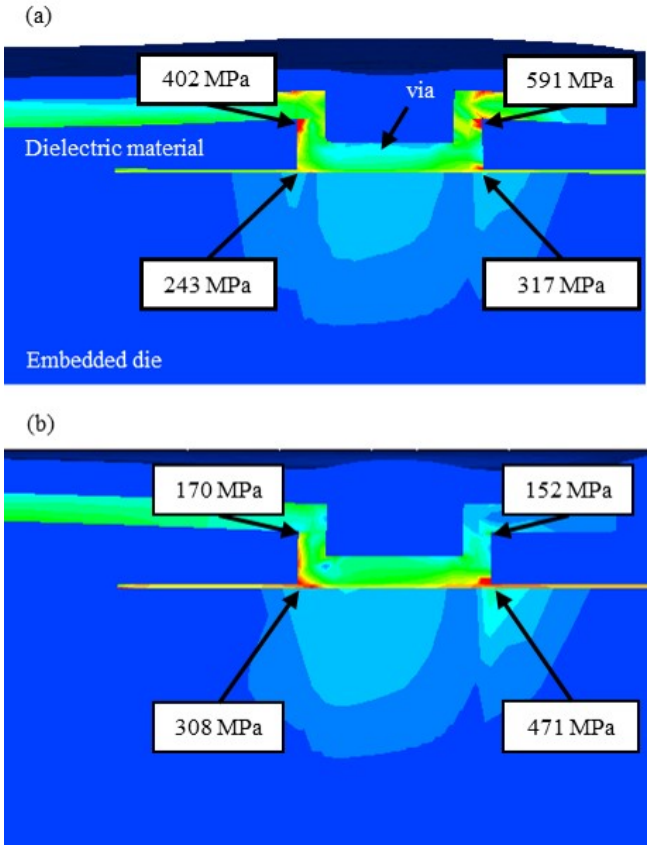


FIGURE 4.13: Stress analysis results of a via on the embedded die with the new material at (a) -55 and (b) 125°C.

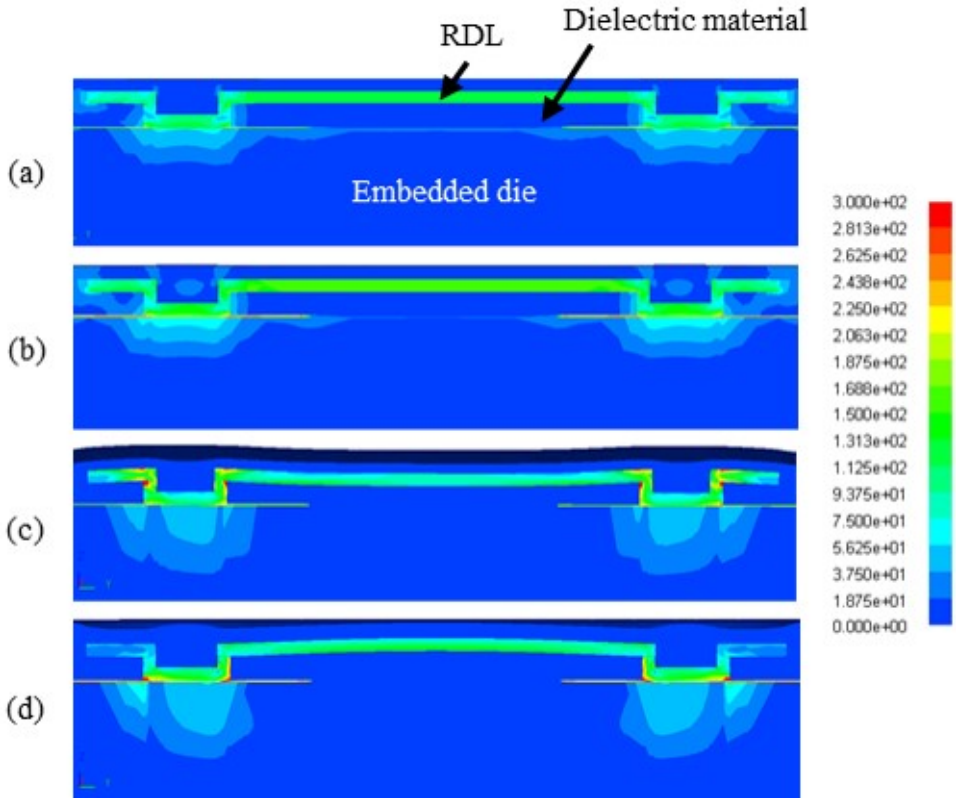


FIGURE 4.14: Stress analysis results of RDL on the embedded die. (a), (b) -55 and 125°C in the standard material. (c), (d) -55 and 125°C in the new material.

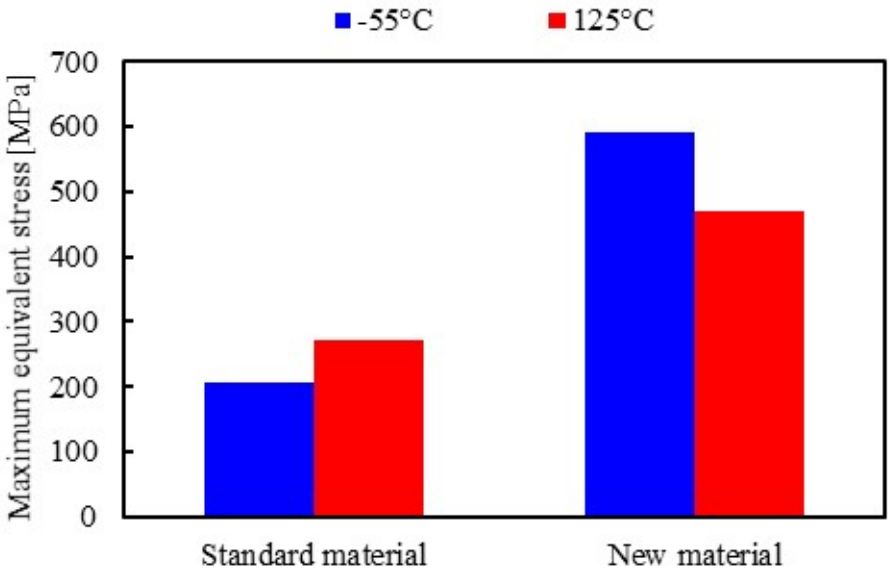


FIGURE 4.15: Comparison of maximum equivalent stress between the new material and the standard material.

4.9 Summary

A new 5-in-1 FOWLP technology consisting of a GPU die with over 2500 pins and four DRAM dies placed side by side was developed. The developed package has a low elastic modulus mold material and a Si support substrate to the backside of the reconstituted wafer. Integrating multiple dies into a single package is expected to significantly reduce the mounting area, provide high-speed transmission, and reduce power consumption. The package achieved a die shift of less than ±5 μm, package warpage of 10.6 μm over 31 mm × 31 mm, and three-layer RDL formation with L/S = 10 μm/20 μm. Function tests with a computer circuit board were demonstrated through a three-layer RDL of the FOWLP.

This study demonstrates the advantages and feasibility of FOWLP with multiple dies for AI edge computing and large memory modules. Outstanding themes/issues to be addressed as a next actions for determining the possibility of using FOWLP for AI edge computing and large memory modules are as follows: 1) development of a mold material with optimized CTE and elasticity to manage both die-shift and package reliability. 2) implementing reliability tests using actual samples to confirm simulation results. 3) quantitative confirmation the improvement in system performance by adopting a 5-in-1 FOWLP.

Chapter 5

3D Integration Technology with Photosensitive Mold for Fan-Out Package

5.1 Background

Fan-out Wafer-Level Package (FOWLP) eliminates wire bonds or solder bumps and package substrate [64], [74], [75], [87]–[89], potentially leading to lower cost, lower profile and better electrical performance, thereby is now extending to 3D integration as well as 2D integration [90]–[93]. Using Package-on-Package (PoP), the present 3D fan-out package technology has already achieved high-density interconnections between logic devices and memory devices in mobile applications, such as smartphones [94]–[96]. The current PoP-based packages using epoxy molding compound (EMC) usually build tall Cu pillars over 200 μm in height by long time-consuming electroplating following thick photoresist patterning process [97]–[101]. In order to interconnect the two packages, the top surface of the Cu pillar needs to be exposed by chemical mechanical planarization (CMP) of the mold surface. The thick photoresist patterning and CMP processes required to fabricate the tall Cu pillars are costly. Therefore, various approaches have been developed to reduce the cost of 3D FOWLP and increase the density of through-molded interconnects (TMI) for 3D integration [102]–[104]. Vertical wire bonding is one of the technologies to achieve lower production costs and improve high-density interconnections [105]–[107]. These process schemes are called "TMI First" in this study. On the other hand, in traditional printed circuit board (PCB) manufacturing field, the technology of forming TMI by Cu plating after opening vias by laser via in EMC has been used [108]–[111]. This process scheme is called "TMI Last" in this study. The current TMI last process does not have the process capability to meet the tall electroplated Cu pillars that the latest TMI first process can achieve [92], [93]. In this study, advanced TMI last process utilizing a newly developed photosensitive mold material for 3D FOWLP integration has been developed to offer an affordable process scheme instead of conventional EMC [112], [113]. Table 5.1 shows a comparison table for through mold interconnect technologie.

In this chapter, the process descriptions are presented for the main packaging processes, including die mounting, photosensitive film lamination, photolithography for photo via opening, and metallization layer formation for Cu redistribution layer (RDL). Furthermore, the reliability assessment was demonstrated with the developed 3D package.

TABLE 5.1: Through mold interconnect technologies. [104], [112]

TMI technology	Cu pillar	Laser via	Wire bonding	Photo via
				
Resin type	EMC	EMC	EMC	Photosensitivity
Thick ptohoresist	Need	No need	No need	No need
CMP	Need	No need	Need	No need
Via pitch	Fine	Coarse	Fine	Fine

5.2 Photosensitive Mold Material

5.2.1 Value Proposition

The newly developed 3D fan-out package is characterized by the utilization of a photosensitive mold material instead of the traditional non-photosensitive EMC containing fillers. The photosensitive mold is mainly composed of silicone and does not contain any fillers. The material has advantages for the application to the 3D fan-out package.

Firstly, in contrast to conventional EMC, the photosensitive mold material enables fine-pitch photosensitive vias and provide high flexibility for applications in hetero-integration technologies by adjusting the exposure amount. Secondly, the sidewall quality on a photo via opening is smooth because it has filler-less, allowing for smaller via formation and finer via pitch. Thirdly, the developed mold material is in the shape of a film, which is suitable for panel-level packaging processes that are expected to reduce manufacturing costs [114]–[117].

Applying a material with the above properties to fan-out package can realize higher design flexibility and improved productivity for 3D integration. Figure 5.1 shows a schematic of the proposed process using photosensitive mold material to realize 3D integration. A thick photosensitive mold film is applied to a substrate with multi dies of different heights, and then the surface is planarized (Figures 5.1 (a) and (b)). The photolithography process is applied to fabricate vias with various specifications of different depths and sizes (Figure 5.1 (c)). A Cu metallization layer (RDL) is fabricated to connect to multi dies and substrate simultaneously (Figure 5.1 (d)). This process, utilizing the new mold material, is unique in that via openings with different depths and sizes can be fabricated using the lithography process, and RDL can be formed for various opened vias using electroplating at the same time.

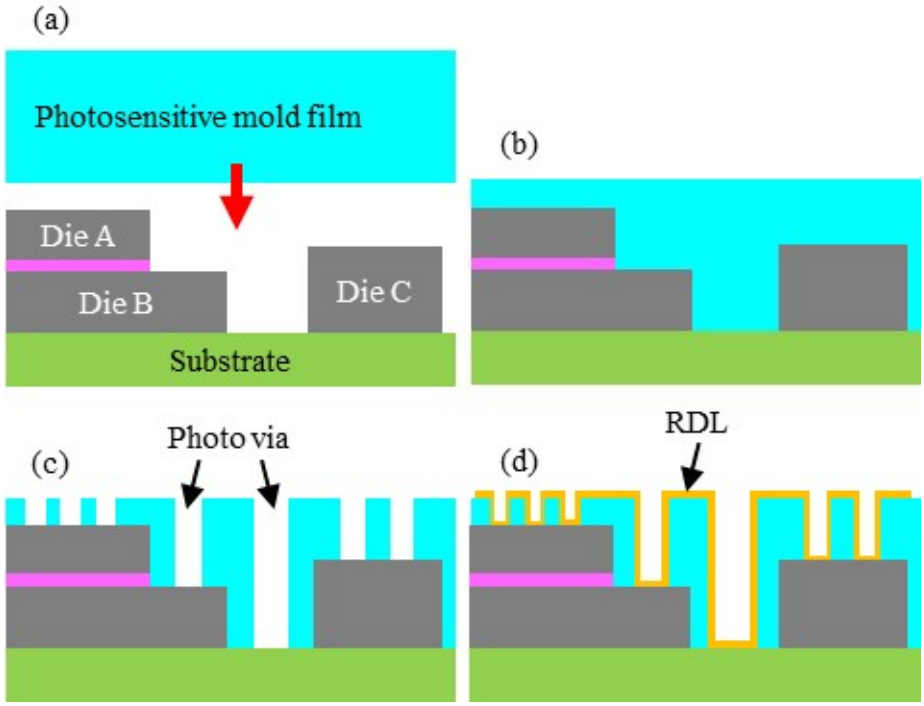


FIGURE 5.1: The proposed process using photosensitive mold material for 3D integration. (a) Mounting of multi dies on base substrate. (b) Thick photosensitive mold film lamination and surface flattening. (c) Via opening. (d) Metallization layer formation.

5.2.2 Comparison with Reference Cu Pillar Process

3D fan-out packages with the tall Cu pillar fabricated by Cu electroplating have already been in high volume production for smartphone application processors [92], [93]. However, the thick photoresist (over 200 μm) and CMP processes needed to fabricate the tall Cu pillars are very expensive approaches. Figure 5.2 shows a comparison of the process flow of interconnection between the die and the Si support substrate for the Cu pillar and the proposed photo via processes. It indicates that the photo via process offers a simplified process flow. The photo via process does not require the Cu pillar and CMP process. The lithography process also allows for simultaneous formation of via openings on the die and on the support substrate. Furthermore, unlike the Cu pillar process, the Cu electroplating in this process does not require Cu bottom-up filling in the vias. It means that low-cost Cu conformal electroplating is available. From the above, this new approach is expected to reduce costs and improve productivity.

5.3 3D Fan-out Package Process

3D packaging process integration with the developed photosensitive mold was evaluated using Si test dies and Si test support substrates. The purpose of this study is to confirm the feasibility and evaluate the reliability test of the 3D integration

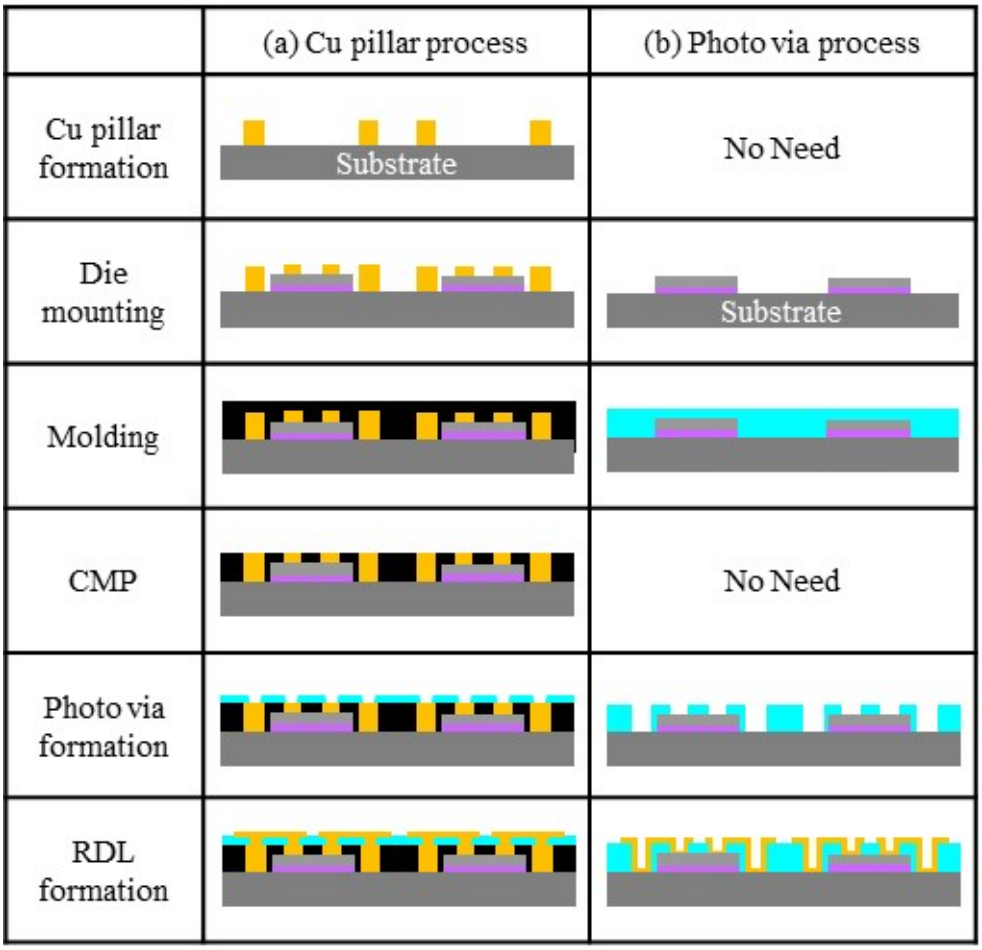


FIGURE 5.2: Comparison of the process flow for 3D FOWLP as (a) Cu pillar and (b) photo via processes.

package. Table 5.2 shows the die specification. It is 10 mm x 10 mm with 100 μm thickness and over 2000 pads with 200 μm pitch on the die. The fabrication process for the package with photosensitive mold was done as shown in Figure 5.2 (b).

TABLE 5.2: Die specification.

Size (mm)	10 x 10
Thickness (μm)	100 (including DAF)
Pad pitch (μm)	200
Pad count	2116

5.3.1 Die Mounting

Firstly, the 100 μm thick test die was mounted face up on 8-inch Si substrate with Cu pad as shown in Figures 5.3 (a) and (b). Cu pad with 300 μm pad pitch was formed by electroplating on the Si substrate before a die with Al bond pad with 200 μm pad pitch was mounted as shown in Figures 5.3 (c) and (d). Die and Si substrate were bonded through Die Attach Film (DAF) with a die bonder, achieving high bonding accuracy of less than ±5 μm. The bonding conditions used were 120°C, 0.1 MPa, and 5.0 sec. A total of 72 dies were mounted on the substrate with a 15.08 mm.

5.3.2 Photosensitive Film Lamination

After die mounting, dies with 100 μm thickness were embedded in a more than 100 μm-thick photosensitive mold film using a vacuum lamination process. The film has a very low viscosity, which makes it possible to embed tall components and flatten their surface. In order to confirm the flatness after the film formation, the film thickness from the substrate to the surface of the film was measured at the die area (y) and die side area (x) using cross-sectional analysis as shown in Figure 5.4. Figure 5.5 shows the results of the film thickness at three points from the center to the edge of the Si substrate. The gap between the film thickness on the substrate (x) and the film thickness on the embedded die (y) was about 4.1 μm at the wafer center. Due to its low viscosity, the film thickness of the wafer edge tends to be thinner. However, the gap trend remains the same at the wafer edge as well as at the wafer center. A gap of less than 5.0 μm is acceptable for the RDL formation. The results show that the 100 μm thick component was completely embedded in the mold material and the surface was nearly flat without CMP process.

5.3.3 Photo Via Formation

After the photosensitive film was cured to achieve a thickness of 110 μm on the substrate, vias with depth of 10 μm on the Al pad of the embedded chip (shallow via) and vias with depth of 110 μm on the Cu pad of the substrate (deep via) were formed by the lithography process (Figure 5.6 (a)). Figure 5.7 shows the relationship between exposure amount and top diameter of different depth vias. The diameter

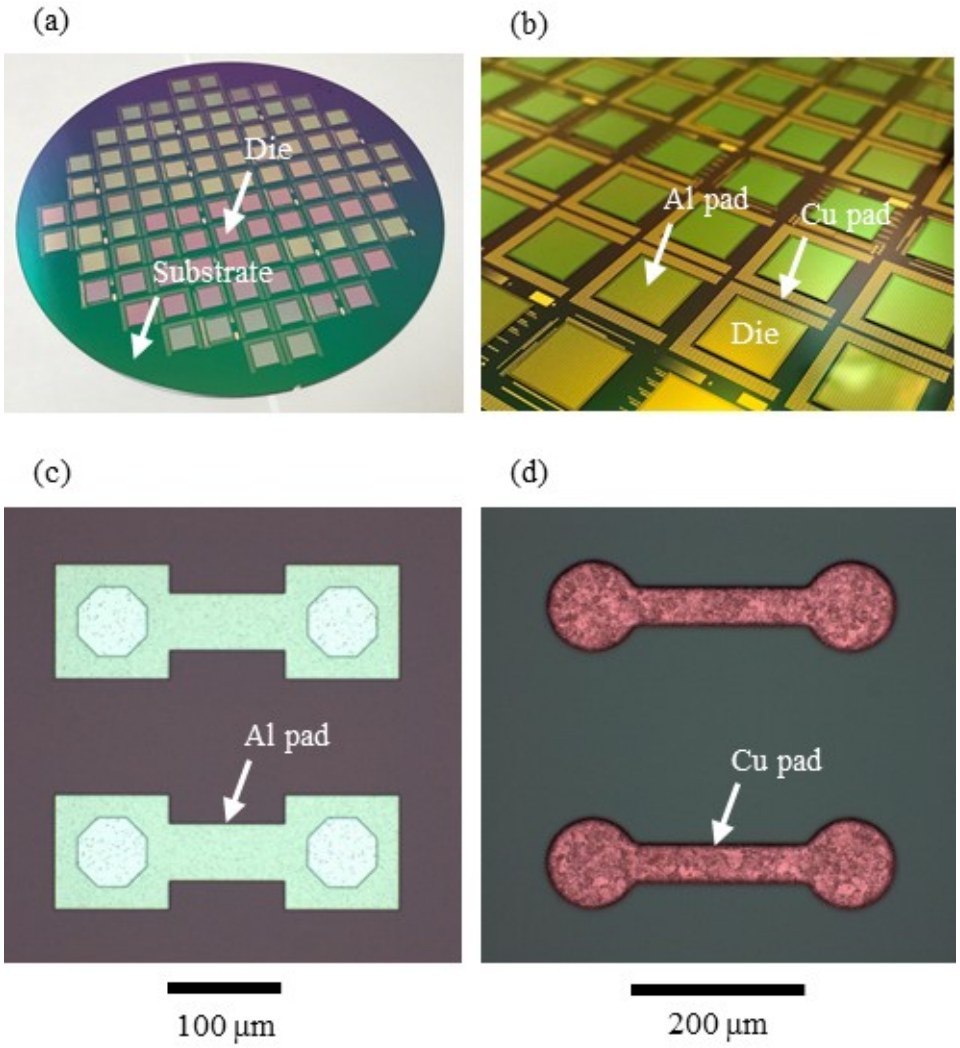


FIGURE 5.3: Photograph of die mounting. (a) 8-inch Si wafer with 72 dies mounted. (b) top view after mounting. (c) Al bond pad on the die. (d) Cu pad on the substrate.

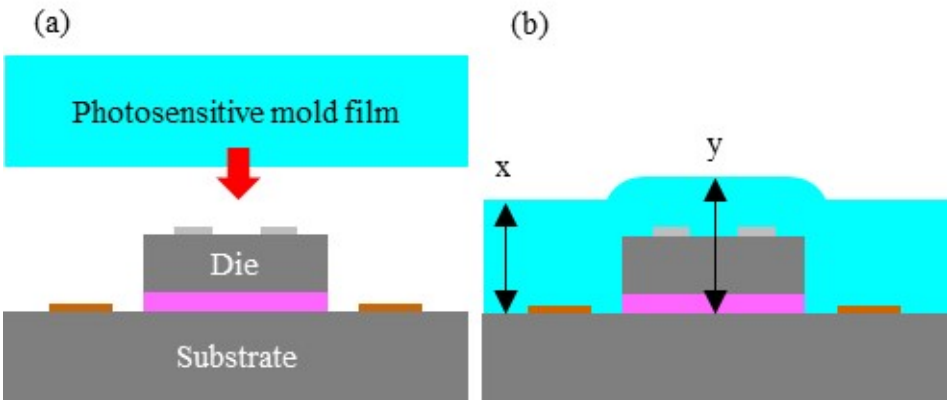


FIGURE 5.4: Film lamination process as (a) before film and (b) after film laminations.

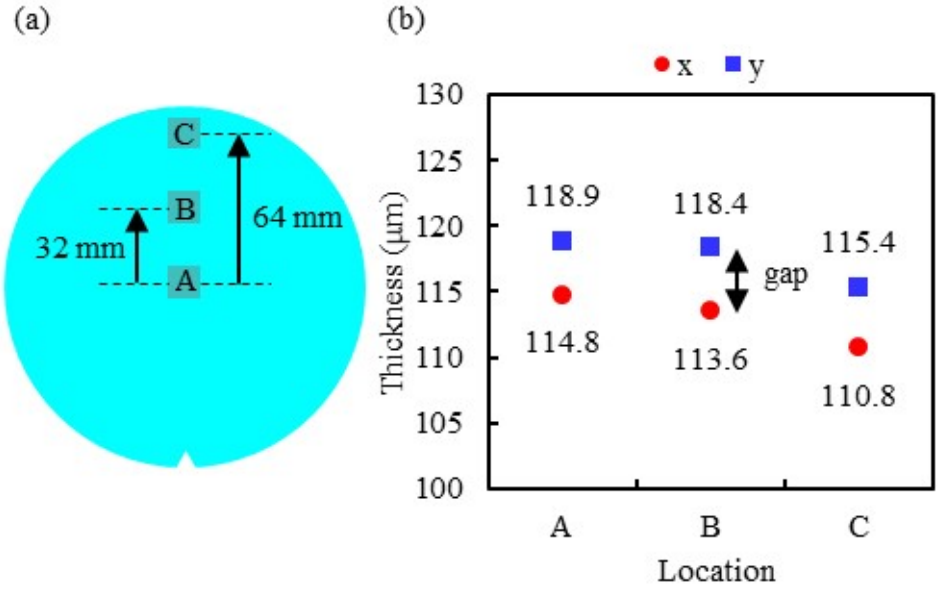


FIGURE 5.5: Thickness measurement of the photosensitive film after film lamination. (a) location of die. (b) results of thickness measurement.

of the vias tends to decrease as the amount of exposure increases. This tendency is a reasonable result because this material is of negative type, in which light-irradiated areas do not dissolve during the development process using a solvent. This means that the larger the exposure, the smaller the via diameter. To fabricate vias of different depths and sizes, two lithography processes can be selected. One approach is a multiple exposure process using photomasks designed for each via depth as described in Figure 5.7 (a). It means that two different photomasks are required to open vias of two different depths in the exposure process. In the other process, all via openings with different depths are fabricated in a single exposure using one mask with exposure conditions that target the deepest via openings described in Figure 5.7 (b), In this study, the mask diameters for shallow vias and deep vias were respectively designed at 60 μm and 100 μm. The exposure condition for the fabrication of shallow vias was adopted as 400 mJ/cm^2. The shrinkage from the mask diameter was confirmed as 6 μm. Similarly, the exposure condition for the formation of deep vias was adopted as 1600 mJ/cm^2. The shrinkage from the mask diameter was also confirmed as 20 μm (Figure 5.7 (a)). On the other hand, if the exposure amount of shallow vias is the same as that of deep vias (1600 mJ/cm^2), the shallow vias can be fabricated simultaneously with the deep vias by considering the large shrinkage of the shallow vias (27 μm) (Figure 5.7 (b)). This one-time process is a cost-effective solution for greater productivity improvement. Figure 5.8 shows a photograph after via opening. It confirms that both shallow and deep vias were via openings. Even if the exposure amount for shallow vias is the same as for deep vias (1600 mJ/cm^2), shallow vias can be formed with a larger shrinkage amount (27 μm).

Next, using the optimized exposure condition (1600 mJ/cm^2) for forming deep

vias, the via opening of various sizes was evaluated with three film thicknesses (70 μm, 85 μm and 110 μm) and five mask diameters (60 μm, 70 μm, 80 μm, 90 μm and 100 μm) as shown in Figure 5.9. The result shows that deep vias with an aspect ratio (AR) of 2.9 or higher cannot be formed. The AR of a via is the ratio between the depth of the hole and the diameter of the hole. As a result, the target deep via with the film thickness of 110 μm and the mask of 90-100 μm was selected.

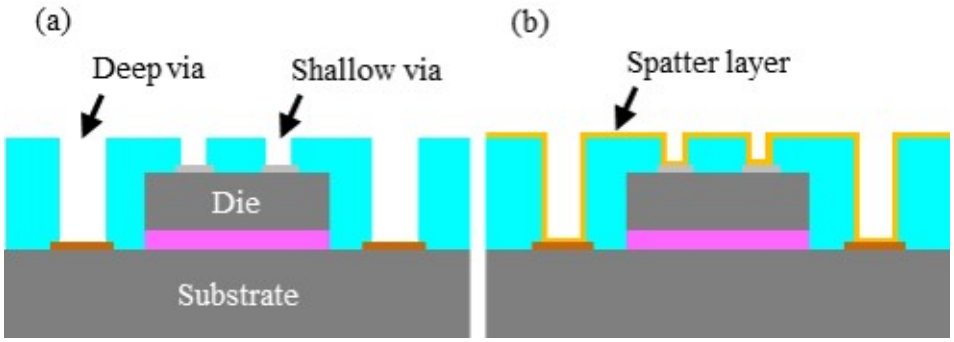


FIGURE 5.6: Via formation flow. (a) Via opening. (b) Ti/Cu sputtering deposition.

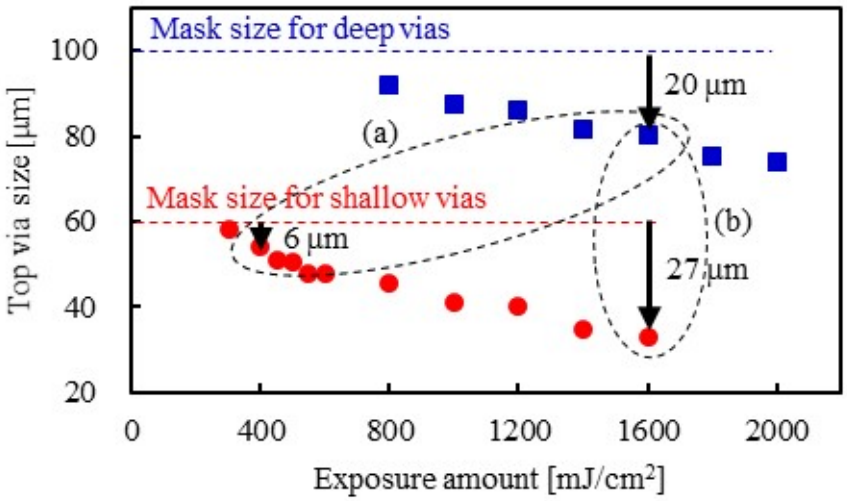


FIGURE 5.7: Relation between the exposure dose and via top diameter. (a) multiple exposure process, (b) one-time process.

5.3.4 RDL Formation

Cu RDL was fabricated to connect Al bond pads on the die with Cu pads on the substrate using Ti/Cu sputtering deposition, photoresist patterning, Cu electroplating, photoresist removal, and etching of sputter-deposited Ti and Cu. Sputtering deposition was performed on the entire surface of the wafer with opened vias using physical vapor deposition (PVD) as shown in Figure 5.6 (b). The target thicknesses of the Ti and Cu were 50 nm and 350 nm, respectively. To evaluate the actual thickness of sputtering deposition, the thickness of sputtered Ti layer on the

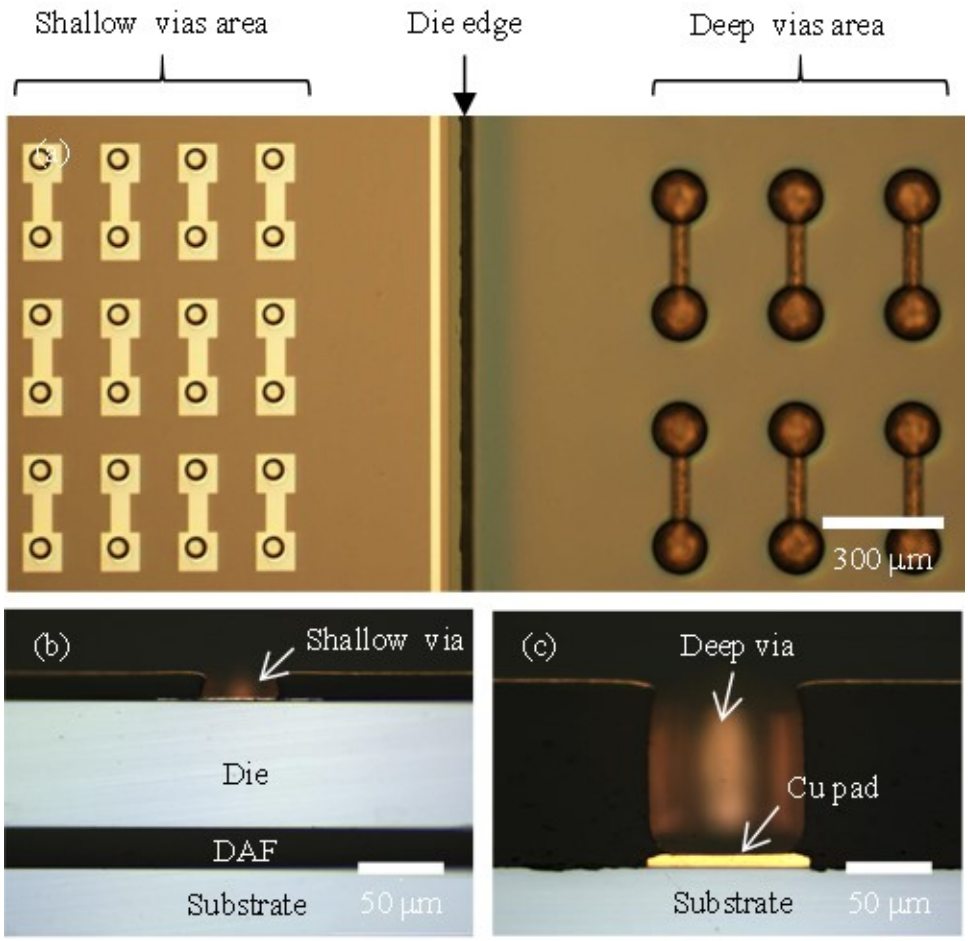


FIGURE 5.8: Photograph taken after via opening. (a) Top view of the embedded die edge. (b) Cross-sections of shallow vias. (c) Cross-sections of deep vias.

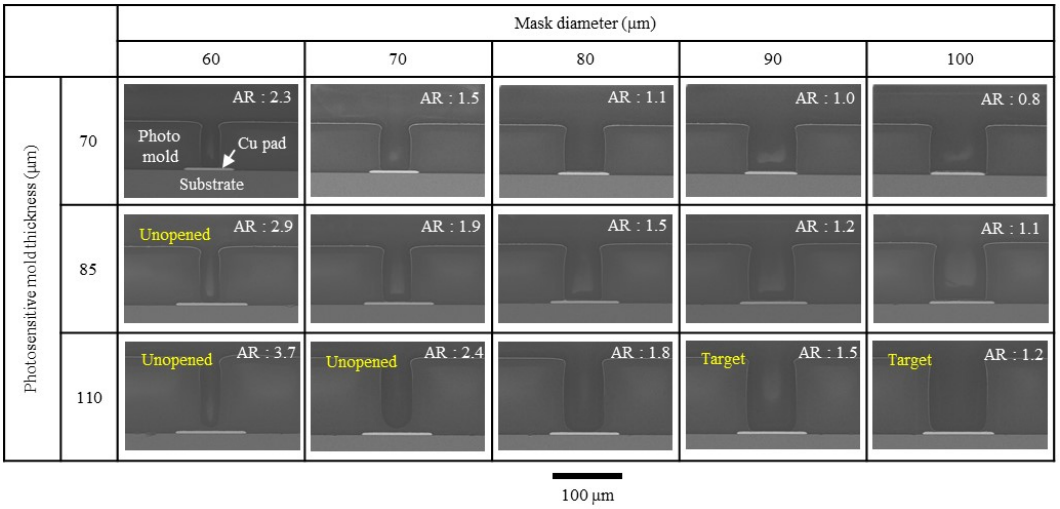


FIGURE 5.9: Evaluation of the dependence of the deep via opening on the photosensitive mold thickness and mask diameter.

surface and bottom of shallow via and deep via were measured using cross-sectional analysis as shown in Figure 5.10. The thicknesses of the surface at the shallow via and deep via were the same, 45 nm, whereas the thickness of the bottom of the deep via was thinner than that of the bottom of the shallow via. The thickness of the bottom of the shallow via was 35 nm, and that of the bottom of the deep via was 20 nm as shown in Figure 5.11. The result showed that the deeper the via, the thinner the thickness of sputtering deposition at the bottom of the via. It means that controlling the sputtering deposition thickness at the bottom of deep via is critical for achieving the robust Cu RDL interconnection, in the case of sputtering deposition using PVD on a wafer with different via depths. The proposed RDL process combines photosensitive molding with Cu conformal electroplating to achieve low cost and high productivity. However, when using Cu conformal electroplating, it is difficult to achieve high density interconnect because stacked vias cannot be applied. In order to achieve further high density interconnect, Cu filling electroplating needs to be introduced in RDL formation.

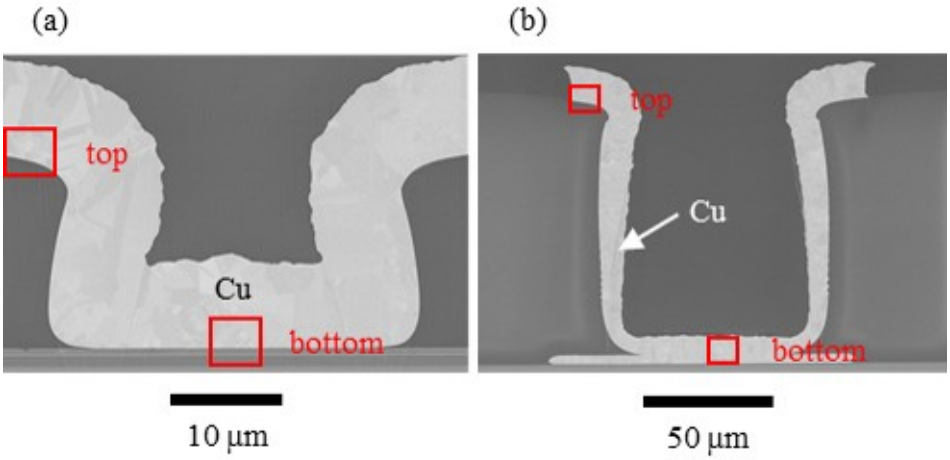


FIGURE 5.10: Measurement point of the thickness of sputtered Ti layer. (a) Cross section of shallow via. (b) Cross section of deep via.

5.4 Prototype Package

The specifications of the prototype package are shown in Table 5.3 and a top view of the package is shown in Figure 5.12. The size of the package is 15 mm x 15 mm and the size of the embedded test die is 10 mm x 10 mm. The developed package is based on the fabrication process described in Figure 5.2 (b). Figure 5.13 shows a photograph of the embedded die edge. A die is embedded face-up in the photosensitive mold. RDL interconnects the deep via on the substrate with the shallow via on the embedded die. There is no large step at the edge of the die. The gap (Δh) in this process is less than 5 μm. The void-free gap filling and flat surface are observed after film lamination. Formation of the shallow via

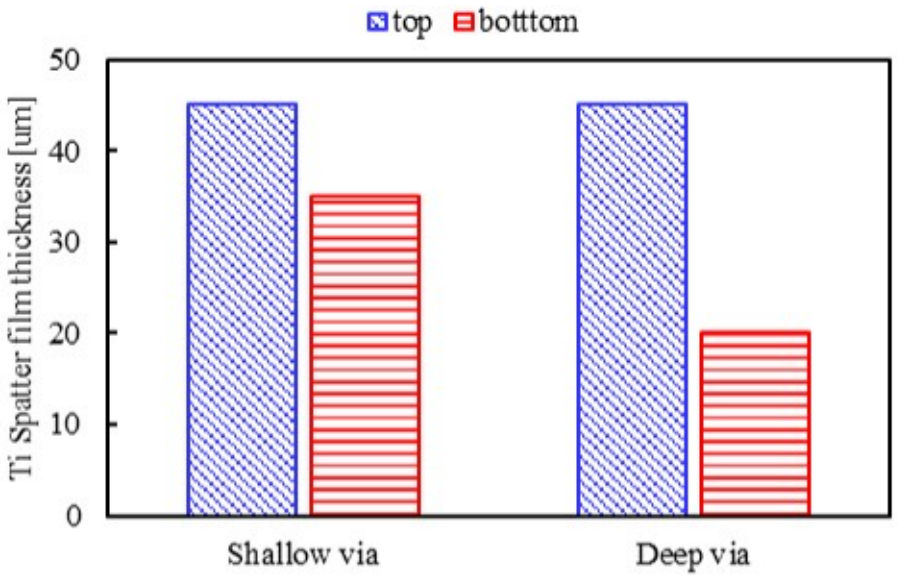


FIGURE 5.11: Thickness measurement of the Ti sputter layer of shallow via and deep via.

openings with height of 10 μm and top diameter of 35 μm is confirmed. In addition, formation of the deep via openings with height of 110 μm, top diameter of 80 μm, and aspect ratio of 1.4 is confirmed. The deep vias can be placed with a 150 μm pitch. The 3D integration using photo via can provide higher pin counts compared to the conventional Cu pillar process. Deep vias can be placed at 100 μm from the die edge, significantly minimizing the keep-out zone for through-mold via layout to accommodate smaller package sizes and more pins in 3D stacked devices. Figure 5.14 shows the X-ray image of the prototype package. It shows that the shallow via and the deep via are properly fabricated with RDL.

TABLE 5.3: TEG Specifications.

Die		Size (mm)	10 x 10
		Thickness (μm)	100 (including DAF)
Package		Size (mm)	15 x 15
		Thickness (μm)	835
Via	Shallow	Pad count	2116
		Pad pitch (μm)	200
	Deep	Pad count	768
		Pad pitch (μm)	300

5.5 Package Warpage

The new matarial developed in this study has characteristics of a higher CTE and a lower elastic modulus compared to the conventional materials dedicated for a usual FOWLP. Thermal stress on Cu RDL due to its high CTE is usually regarded as a concern for its thermal cycling reliability. Therefore, thermal stress simulation was

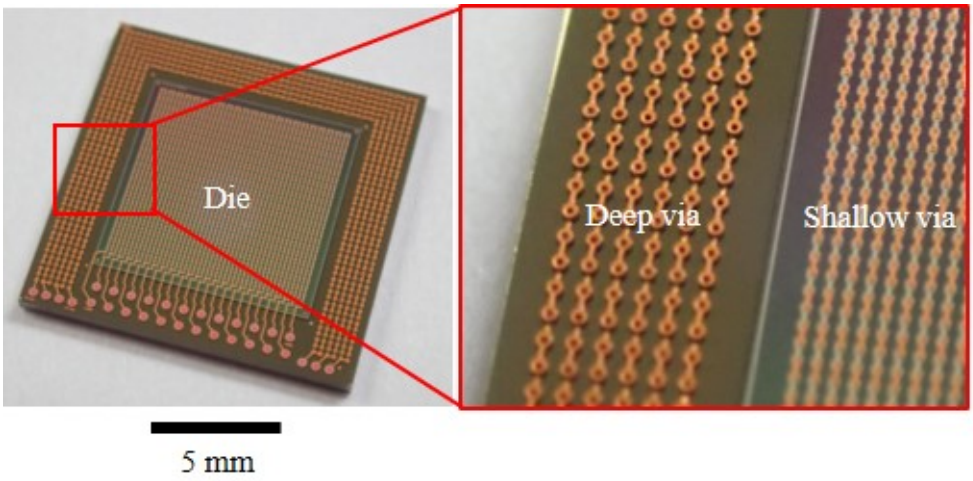


FIGURE 5.12: Photograph of the developed prototype package.

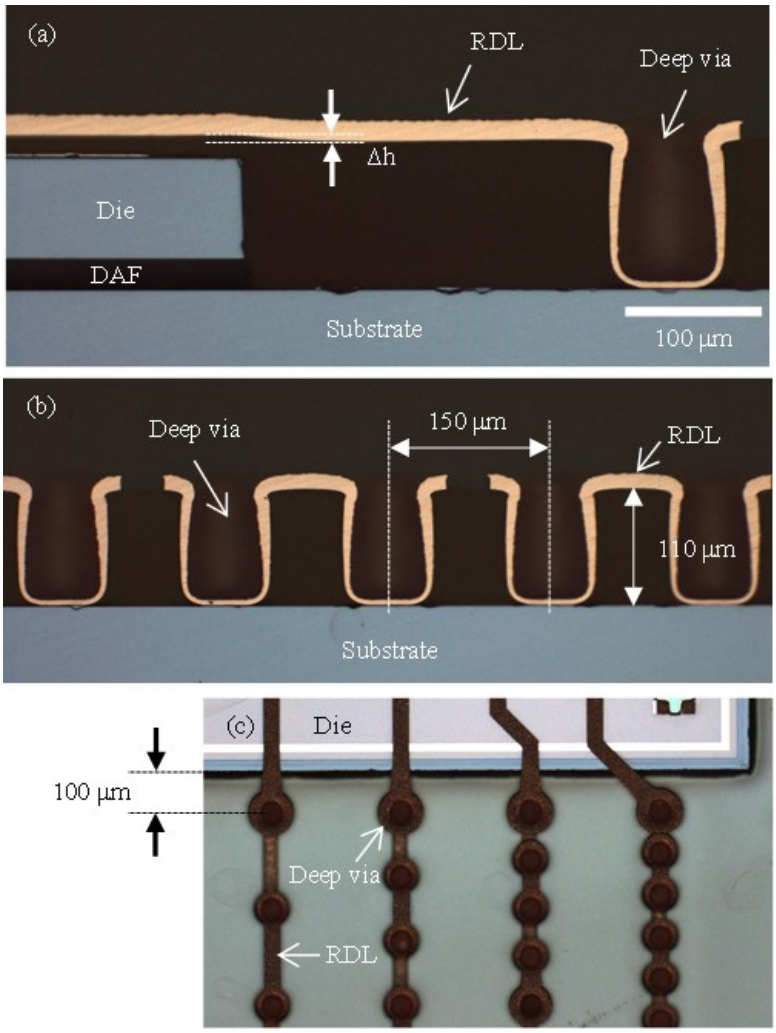


FIGURE 5.13: Photograph of a developed prototype package. (a) Cross-sections of the embedded die edge. (b) Cross-sections of deep vias. (c) Top view of deep vias.

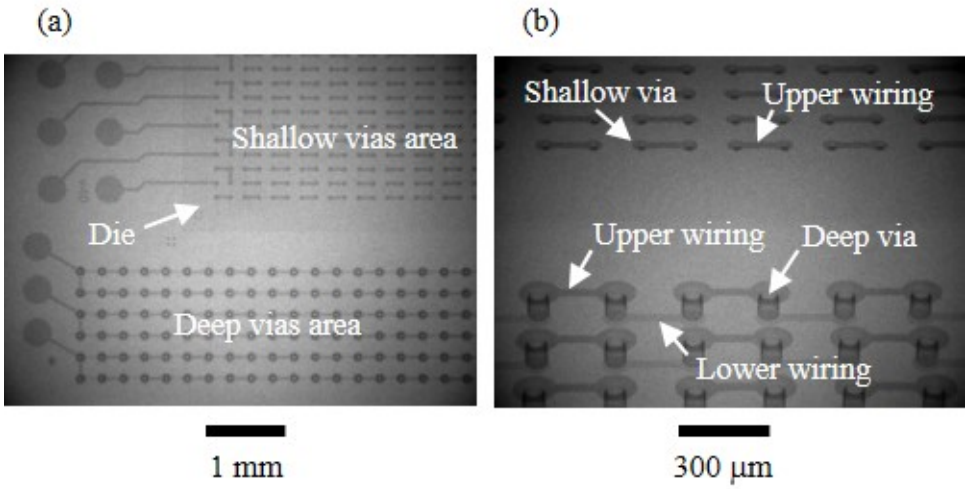


FIGURE 5.14: X-ray images of a developed prototype package as (a) top and (b) bird's-eye views.

performed with the developed material and compared with a standard material for 3D FOWLP structures. A detailed 3D-solid package-level model including a silicon substrate, embedded die, shallow vias, deep vias, and RDL lines was employed to calculate warpage of the package and to evaluate stress distribution around the vias due to a mismatch in CTE between the different type of materials. Stress simulation was performed using ADVENTURECluster finite element analysis software. In the simulation, all of the materials worked to be isotropic linear elastic. In order to compare the relative stress induced by the two types of the molding materials with different curing temperatures, the effective stress-free temperature was defined as room temperature. The thermomechanical stress was calculated at the maximum and minimum temperatures in temperature-cycle testing. The package warpage was evaluated by measuring from the center to the edge of the package surface. Table 5.4 and Figure 5.15 show the 3D-solid package model and specific properties of the novel developed material and a standard material. This analysis addressed a quarter area with a package size of 15 mm. Figure 5.16 shows the measured warpage values for the two different molding materials at the developed and standard materials at –55°C and 125°C. The results showed that the new material (x) reduced the warpage displacement by about 47% in the range of -55°C to 125°C compared to the standard material (y). Therefore, the application of this material to FOWLP is expected to reduce the wafer warpage during manufacturing.

5.6 Package Reliability

Reliability assessment of the developed packages was performed. Daisy chains connecting over 2000 vias with 200 μm pitch on the die and over 700 vias with 300 μm pitch on the substrate were created and their electrical resistance was measured. Before the test, all package samples are assessed at moisture sensitivity level-3

TABLE 5.4: General properties of the developed material and standard material.

Item	Unit	Standard material	Developed material
Material type	-	Epoxy	Silicone
Young's modulus (25°C)	GPa	22	0.095
Tg	°C	165	105
CTE (α1)	ppm / K	7	220

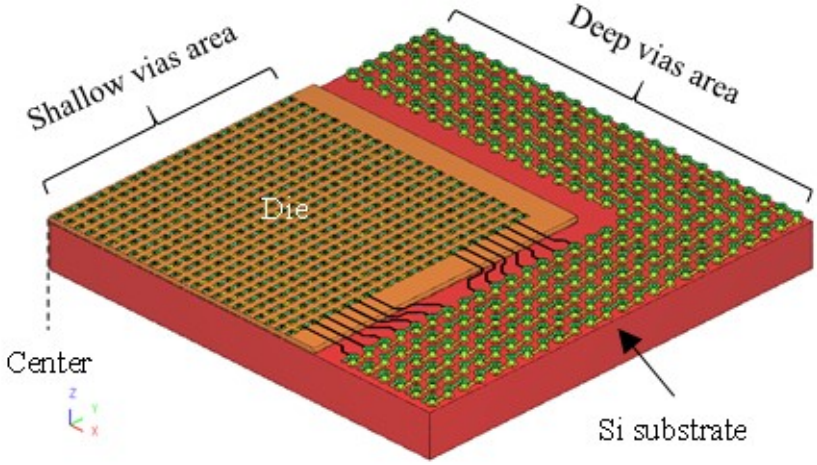


FIGURE 5.15: 3D-solid package model.

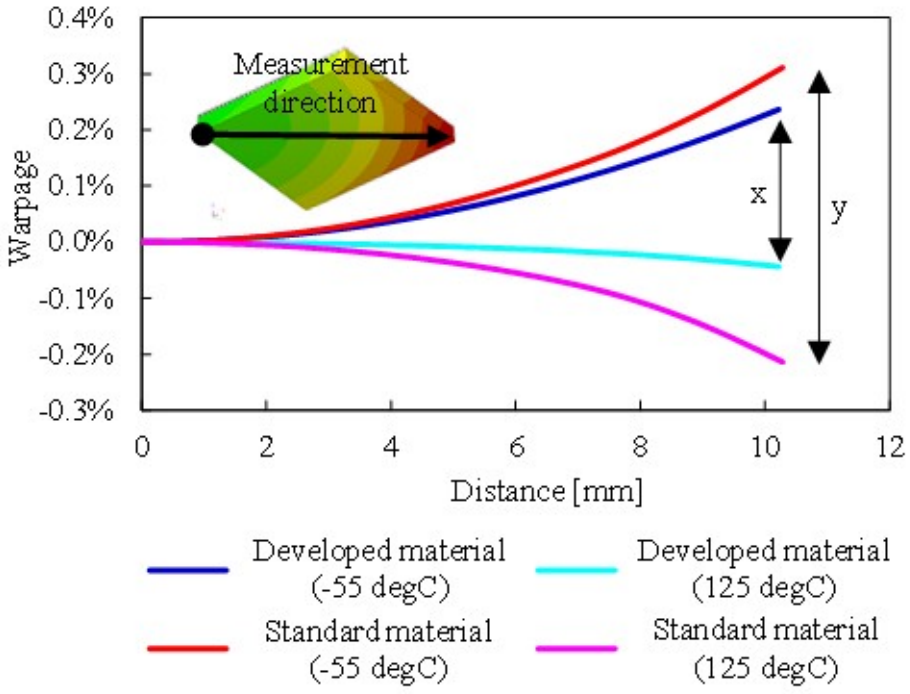


FIGURE 5.16: Warpage versus distance.

conditions (MSL 3) as shown in Table 5.5. A 1000-cycle package-level thermal cycle test (TCT), a 1000-h high-temperature storage test (HTS), and a 96-h pressure cooker test (PCT) were performed as shown in Table 5.6. Physical properties of electroplated Cu vary drastically depending on its micro-texture. The orientation of grains, grain size distribution and strain mapping of the Cu films were evaluated before and after 1000 thermal cycles using EBSD. EBSD measurements were performed at incident beam energy of 15 kV and specimen tilt of 60°. Orientation mapping was done over a 75 μm x 35 μm area. Grain boundaries were defined by a minimum of 5°orientation change from one grain to contiguous ones. 1000-cycle package-level TCT showed tiny cracks at the top edge of the shallow via openings in Figure 5.17 (d). Residual stress around the crack was confirmed from grain reference orientation deviation (GROD) in Figure 5.17 (e). As shown in Figure 5.18, that the grain size after the 1000 thermal cycles was enlarged compared with that before the thermal cycling, which causes tiny cracks along the grain boundaries. On the other hand, as shown in Figure 5.17 (f), the crystal orientation distribution after the 1000 thermal cycles remained unchanged from those before the thermal cycling. This means that the microstructures of the interconnection after 1000 thermal cycles had no texture during recrystallization generated by thermal stress. The failure criterion for the reliability test was defined as the electrical resistance of the daisy chain within $\pm$10% from the initial value. As a result of reliability test, the prototype package with photosensitive through mold interconnects passed a 1000-cycle package-level thermal cycle test, a 1000-h high-temperature storage test, and a 96-h pressure cooker test.

TABLE 5.5: Pre-treatment conditions.

	Process	Test condition
1	Pre-bake	125°C for 10 hours
2	Moisture Absorption	30°C, 70%RH for 7 days
3	Reflow	Max. 260°C, 3 times

TABLE 5.6: Package-level reliability test.

Test Item (Test condition)	End point
Temperature Cycling / TC (-55°C/125°C)	1000 cycles
High Temperature Storage / HTS (150°C)	1000 h
Pressure Cooker Test / PCT (121°C/100% RH)	96 h

5.7 Material Issues

Finally, material issues of the developed photosensitive material are described. Thermal stress analysis confirmed that the developed material with high CTE elongated in the vertical direction during thermal cycling. Tensile stress might be applied to Cu RDL lines along the sidewall of the vias and around the top corner of

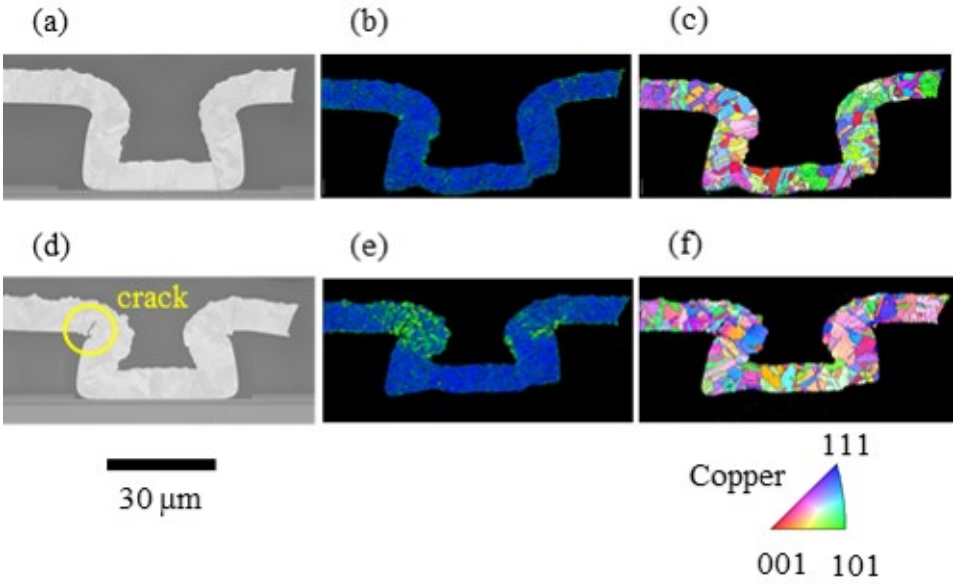


FIGURE 5.17: SEM image, orientation image (normal direction) and GROD maps of shallow via. (a, b, c) initial, (d, e, f) after 1000 thermal cycles.

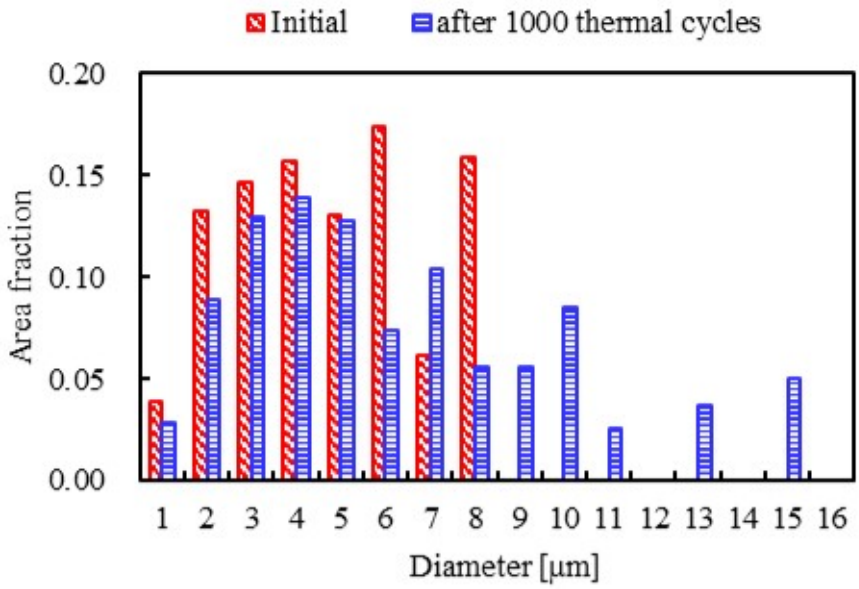


FIGURE 5.18: Comparison of grain size change of shallow via before and after 1000-cycle package-level thermal cycle test.

the vias opening due to thermal stress, as shown in Figure 5.19. Actual post-thermal cycle testing confirmed that tiny cracks were observed with their growth from the top edge of the vias opening in Figure 5.20, which can be predicted form the stress simulation results in Figure 5.19. Such Cu cracking can be problematic in products requiring high reliability or harsh test environments. For more reliable packaging dedicated to automotive grade applications, the Cu cracks as observed in Figure 5.20 might be a reliability detractor. In the next phase of the development of the photosensitive mold materials, more CTE reduction will be a significant matter to alleviate the reliability concern while a lower modulus of the present material is kept as it is. Further advances in photosensitive mold materials and processes will contribute to the expansion of the 3D FOWLP product lineup.

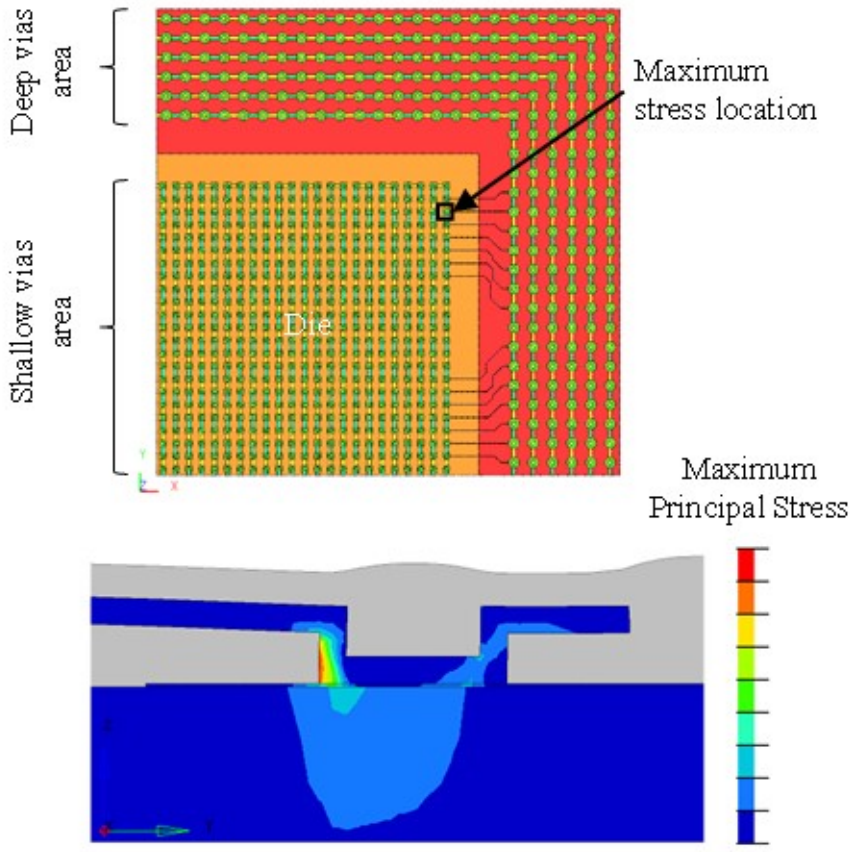


FIGURE 5.19: Distribution chart for principal stress.

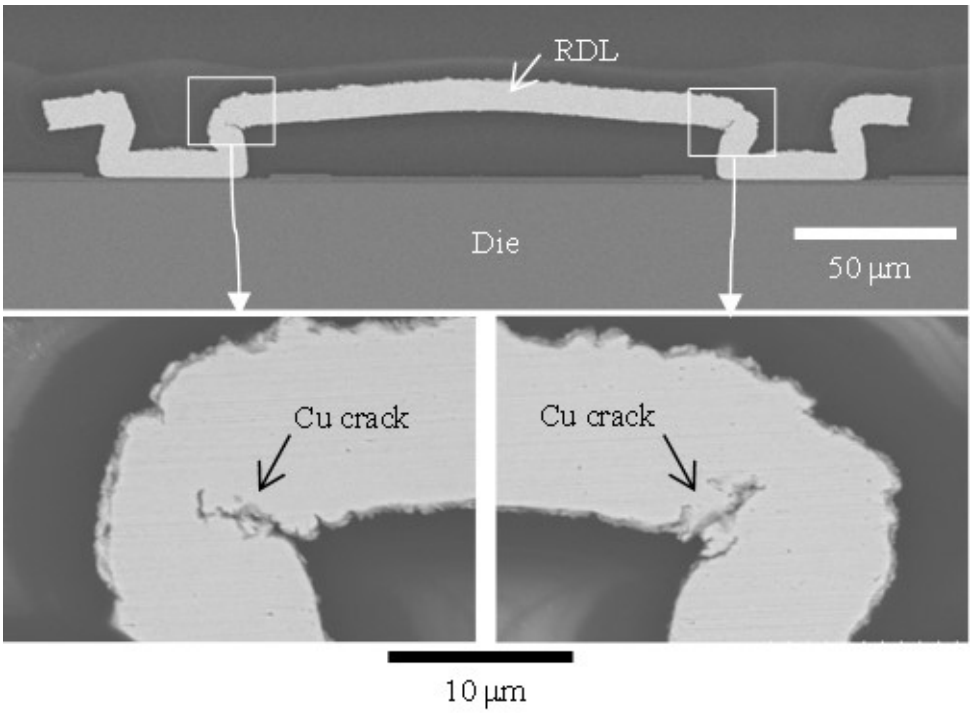


FIGURE 5.20: Test sample cross-section of after 1000 thermal cycles.

5.8 Summary

3D packaging and integration using photosensitive mold is promising technology to reduce costs and improve productivity for future SiP integration. By applying a mold material with characteristics such as photo via opening, low viscosity, filler-less, thick, and film shape to fan-out package, an innovative 3D integration with high design flexibility can be expected. The feasibility of the 3D integration packaging process was confirmed and the reliability assessment of the package was evaluated for photovias with different diameters and depths. Reliability assessment results for the 3D package test samples have confirmed that no failures are observed after a 1000-cycle package-level thermal cycle test, a 1000-h high-temperature storage test, and a 96-h pressure cooker test. After a 1000-cycle TCT, electron backscatter diffraction (EBSD) analysis was adopted to analyze the thermal stress and crystal orientation distribution on the Cu Redistribution Layer (RDL). Thermal stress simulation has revealed that warpage displacement of the photosensitive material is about 47% less than that of the standard material. The developed photosensitive mold showed high density and reliable 3D interconnections, and the possibility of applying it as a future 3D package integration was confirmed.

Chapter 6

High Density and Reliable Die Stacking Technology with Non Conductive Film for 3D/TSV

6.1 Background

The Moore's law is approaching physical limitations of CMOS scaling, and various three dimensional (3D) integration have been proposed as solutions to achieve high performance SiPs [118]–[122]. The wide band transmission between the logic and the memory is becoming indispensable for not only mobile products, but also a network field such as servers, data centers and cloud computing. 3D integration with Through Silicon Via (TSV) in the logic die is considered as the key solution, which provides benefits leading to wide band transmission, low power consumption and miniaturization downsizing of products [123]–[126].

Advanced flip chip bonding process using Cu pillars is one of the key technologies to realize 3D/TSV integrations [127]–[130], and to enable heterogeneous integrations which combines different functional devices such as application processors, power management ICs, baseband processors, radio frequency ICs and microcontrollers. Especially, to develop effective underfilling technologies for 3D integration is essential to relieve mechanical stresses so that the reliabilities of interconnections between die and package substrate can be enhanced [131]–[134].

However, 3D structure with a thin logic device as a bottom die and Wide I/O DRAM as a top die has many challenges in its assembly process such as: (1) to achieve void-free underfill formation under the thin logic die, (2) to prevent underfill resin creeping issue on the back side of the thin logic die not to interfere with the memory die stacking, (3) to fill space with the underfill resin under overhangs of the memory die when the memory die is larger than the logic die in order to avoid void generation in molding process. In this study, Non Conductive Film (NCF) laminated on organic substrates before flip chip bonding was selected as the underfill material to address these challenges. Although some types of Non Conductive Paste (NCP) have already been used as standard preapplied underfill materials [135]–[139], the

disadvantages of the process using NCP were mentioned. For example, "underfill resin creeping" and "underfill voids" are said to be typical issues in case of a thin die assembly using NCP. The stability of the NCP material's viscosity is also a frequent issue. The underfill technology using NCF provides an promising approach to solve such concerns and realize high density and reliable 3D/TSV structures.

This chapter mainly describes the new 3D/TSV assembling technology, especially thin die bonding process with NCF on substrates as pre-applied underfill method [140]–[143]. In order to prove the quality of this 3D/TSV package, package reliability tests were evaluated. Finally, 28 nm logic device and Wide I/O DRAM were assembled into 3D structure with this new technology, and transmission speed and power consumption were evaluated.

6.2 High Density and Reliable Packaging Technology

6.2.1 Test Vehicle

The target 3D structure consisted of Wide I/O DRAM with micro-bumps, the logic device with high density TSVs and fine pitch Cu pillars and an organic package substrate, as shown in Figure 6.1. NCF was adopted as an pre-applied underfill material to protect flip chip interconnections between the logic die and the substrate. Table 6.1 summarizes major specifications of the logic test elementary group (TEG), the memory TEG and the substrate in this study. The logic TEG was fabricated by so called via-middle process described in Chapter 1. It had with 1200 TSVs, a size of 6 x 6 mm^2, a thickness of 50 μm and 40 μm/50 μm under bump metallization (UBM) pitch in x-y directions. Cu pillars on the front-side of the logic TEG were placed along peripheral four rows (100 μm pitch for each row) and on the center area of the die. Cu pillars and solder caps (SnAg) were formed by electroplating. The interface between logic die and memory die was designed in compliance with JEDEC standards. Wide I/O DRAM had a thickness of 260 μm, a size of 9 x 9 mm^2 and micro-bumps in the center area of the die. The target of total package thickness including BGA balls was 1.0 mm or less.

6.2.2 Underfill Process

The developments of underfill materials and the related assembly processes are key technologies to achieve a high density and reliable flip chip bonding, especially for protecting low-k layers. Characteristics of each underfill method are shown in Table 6.2. The traditional capillary underfill (CUF) has been widely used, however, when the gap between the package substrate and the die is narrow, the underfill resin injected from die edge doesn't flow uniformly under the die. As a result, underfill voids are occurred. NCP has been already applied to a lot of commercial products as the pre-applied resin to realize void free and fine pitch requirements. However, there are some challenges in handling a thin die such as 50 μm or less,

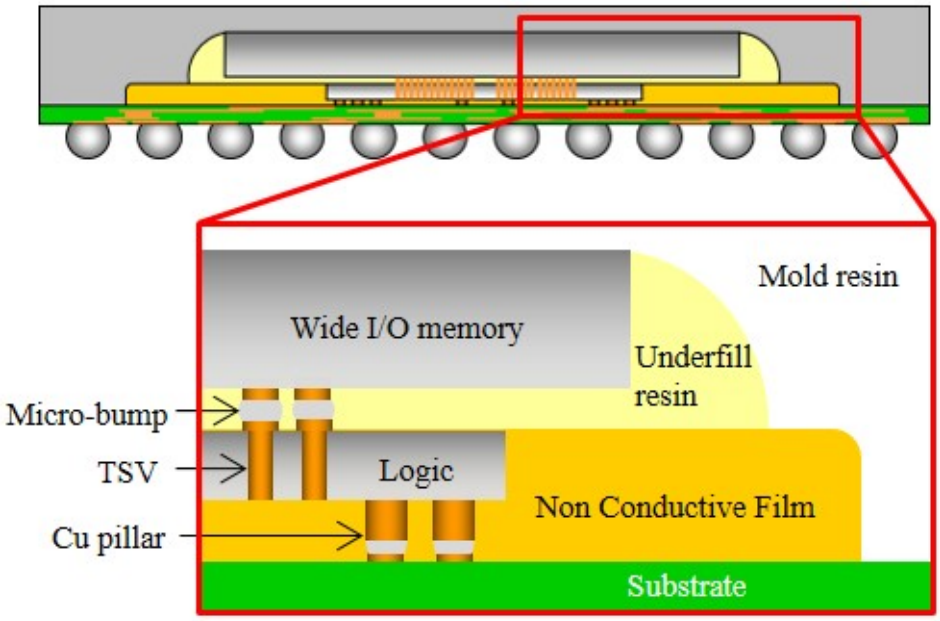


FIGURE 6.1: Target package structure.

TABLE 6.1: Specification of logic and memory Test Elementary Groups (TEGs).

		Logic TEG	Memory TEG
Die	Size [mm^2]	6 x 6	9 x 9
	Thickness [μm]	50	260
TSV	Diameter [μm]	10	-
	Depth [μm]	50	-
	Pitch [μm]	40, 50 (x, y)	-
	Process	Via-middle	-
Front-side	Pad layout	Center, peripheral	Center
	Pad count	900	1200
	Pad pitch [μm]	100 μm staggered	40, 50 (x, y)
Back-side	Pad layout	Center	-
	Pad count	1200	-
	Pad pitch [μm]	40, 50 (x, y)	-
Substrate	Thickness [μm]	220	
	Metal layers	4 metal layers (1/2/1 buildup substrate)	
Package	Size [mm^2]	14 x 14	
	Height [mm]	<1.0	
	Substrate	700 pin BGA	

because it requires very tight optimization and fine tuning in dispensing resin to prevent a creeping issue on the back-side of the die as shown in Figure 6.2 and resin void issue under the thin die. If the creeping resin reached TSV area, it would contaminate UBM on the TSVs and affect micro-bump interconnections between the logic die and the memory die in the worst case. On the other hand, if the resin volume became smaller than the optimized value to reduce the creeping, the die edges would not be protected sufficiently. It would cause a degradation in interconnection reliability. For these reasons, apparently CUF and NCP have some challenges for thin die with TSV.

TABLE 6.2: Features of underfill technology.

	CUF	NCP	NCF on Substrate	NCF on Wafer
Void free	-	++	++	++
Fine pitch	-	++	++	++
Fillet control	-	-	++	++
Cost	++	++	+	-

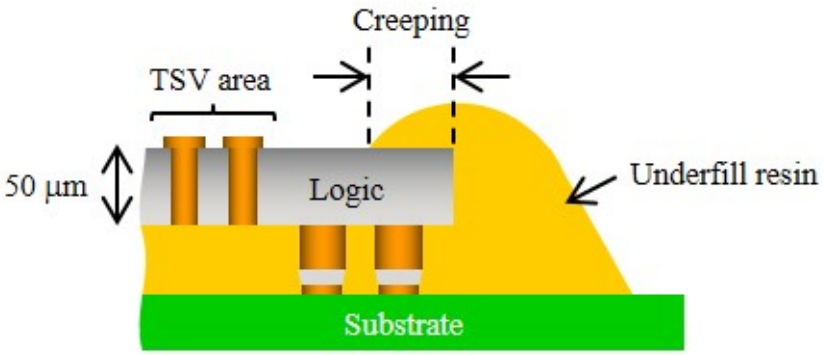


FIGURE 6.2: Underfill resin creeping issue on back-side of thin die.

In case of NCF, there are two options to supply NCF to packages. The method of applying the NCF to the wafer has some potentials to control resin flows and fillet sizes in flip chip bonding. However, there are still many technical challenges in the wafer lamination process such as 1) to prevent air traps around high bumps, 2) to ensure visibility of alignment marks on dies, and 3) to prevent wafer damages during wafer dicing process. Besides, unless yields of logic wafers were as high as mature wafer processes, the assembly cost would be expensive because NCF is also supplied to defective dies. For die-stacked 3D integrations, when the memory die is larger than the logic die, preventing voids under the overhang of the memory die is also a challenging issue. To solve this risk, the NCF lamination to the substrate is the preferred method, and its effectiveness was proven in this study.

6.2.3 Flip Chip Bonding Process With Non Conductive Film

The packaging technology for 3D/TSV can be categorized into front-end, intermediate and back-end processes. Figure 6.3 shows a schematic of the process flow. This flow includes 1) FEOL, TSV via formation, insulation, Cu filling and BEOL as front-end process, 2) Cu pillar formation, temporary bonding, wafer thinning and back-side metallization, wafer mounting and debonding as intermediate process, and 3) wafer dicing, die bonding and molding resin as back-end process.

The NCF is attached to the substrate in a lamination process before the logic die is flip-chip mounted. The NCF size should be larger than a memory die to prevent void issues under overhangs of the memory die. Next, a logic die is bonded to the substrate with the thermal compression bonding using Cu pillars. Then, NCP is dispensed on the backside of the logic die, and the memory die is stacked on the back side of the logic die with the thermal compression bonding using micro bumps. In this study, a memory die with a thickness of 260 μm was used. Since the memory die was thick enough, there is no creeping problem. For this reason, NCP was chosen as the underfill material for the memory die. Although NCF is preferable for thin die bonding, NCP has an advantage for recognitions of alignment marks on the back-side logic during the die bonding because NCP can be dispensed by avoiding alignment marks. After flip chip bonding, molding and BGA ball attachment were conducted to complete assembly for 3D/TSV integration.

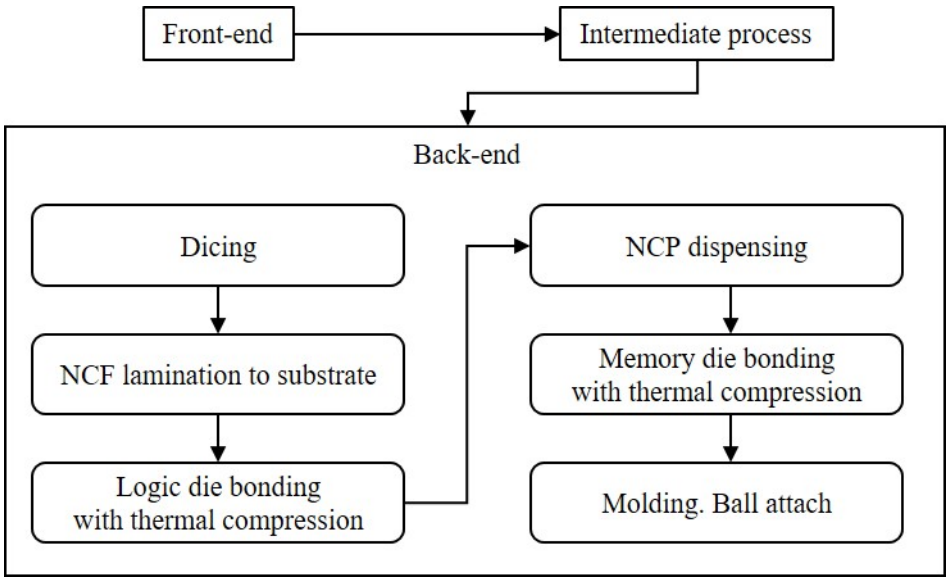


FIGURE 6.3: Assembly process flow of 3D integration with Wide IO memory.

To ensure robust interconnections between the logic die and the package substrate, surface treatments of both sides should be chosen carefully. Direct Immersion Gold (DIG), Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG), Immersion Tin (IT) and solder coating on substrate are considered as the candidates in flip chip boning process. In this study, the solder coating technology

was chosen to provide reliable interconnections between the logic die and the pacakge substrate, because it didn't require additional traces for plating and was a low-cost process. Figure 6.4 shows the surface morphology and the cross section of Cu lead after solder coating. It can be seen that solder was coated on the surface and sides of the Cu wiring. The detail of the die bonding process flow with NCF is shown in Figure 6.5. After NCF is laminated on a package substrate (Figure 6.5 (a)), a die is placed on a bonding position after prebake process to reduce the viscosity of NCF (Figure 6.5 (b)). After that, the die is compressed to the substrate by the predetermined force and heat through a fluorocarbon polymer film (Figure 6.5 (c)). The polymer film works to prevent the sticky issue between a bonding tool (attachment tool) and NCF, and to obtain continuous flatness on the back surface of the logic die (Figures 6.5 (d)). The bonding tool which is larger than the die also contributes to the smooth surface topology to ensure the bonding of the memory die. In the thermal compression bonding with NCF, it is very important to control the gel time and the viscosity of the pre-applied material, especially for thin die stacking. Fig. 6.6 shows the two main failure modes of NCF process.

If the hardness of NCF increased due to curing reaction at high temperature during the process, before Cu pillar contacted to Cu lead of the substrate, no-wet issue would be occurred at flip chip joints, as shown in Figure 6.6 (a). A no-wet causes open failure. On the other hand, if the hardness of NCF increased after Cu pillar contacted to Cu lead of the substrate, melted solder on the Cu pillars would be deformed and pushed away from the bonding positions by NCF flow, as shown in Figure 6.6 (b). This failure is called a solder splash. The solder splash causes short failure.

Additionally, the solder thickness on the Cu pillars at the flip chip joint, as shown in Figure 6.6 (a), is the most important design parameters to ensure the reliability. A Design On Experiment (DOE) was conducted to investigate the effect of key parameters (temperature, pressure and bonging time) on the flip chip joints. Based on DOE results, it was concluded that the target solder thickness should have been between 3 μm and 5 μm to obtain the ideal flip chip joints, as shown in Figure 6.7. Samples for the reliability test described below were assembled with the optimized conditions.

6.3 Physical Analysis

3D assembly of an unique structure which had a large top die (9 x 9 mm^2) and a small bottom die (6 x 6 mm^2) was demonstrated to validate the benefits of new thin die stacking technology. Figure 6.8 (a) shows outline photographs after the 1st die (logic die) was bonded, Figure 6.8 (b) show outline photographs after the 2nd die (memory die) was bonded. The logic die was bonded on the NCF, which was larger than the logic die and laminated on the substrate in advance. The die edges were completely surrounded by NCF fillet, and any failure modes such as the creeping

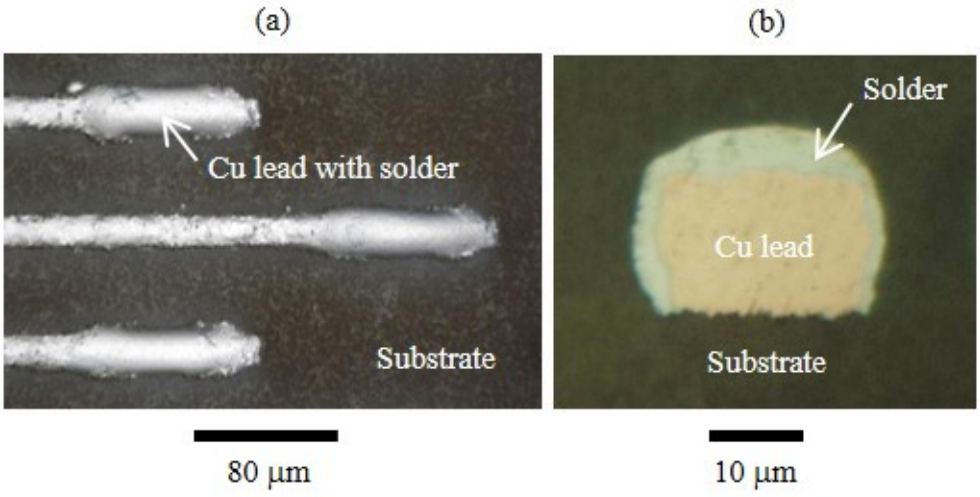


FIGURE 6.4: Solder coating technology as (a) Top and (b) cross-sectional views.

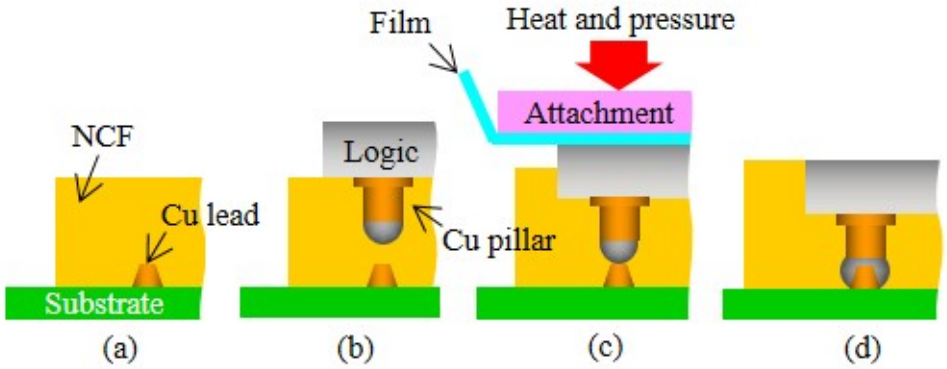


FIGURE 6.5: Process flow of Cu pillar die bonding with NCF.

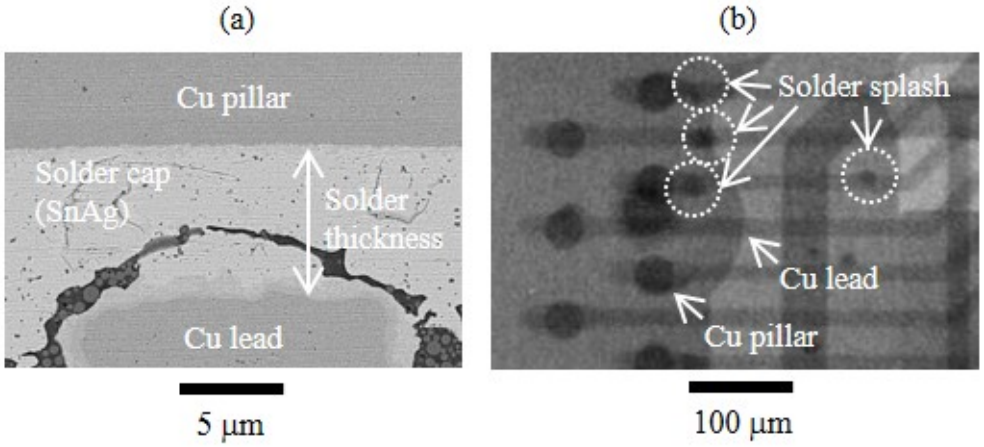


FIGURE 6.6: Typical failure mode of Cu pillar bonding with thermal compression. (a) no-wet issue. (b) solder splash.

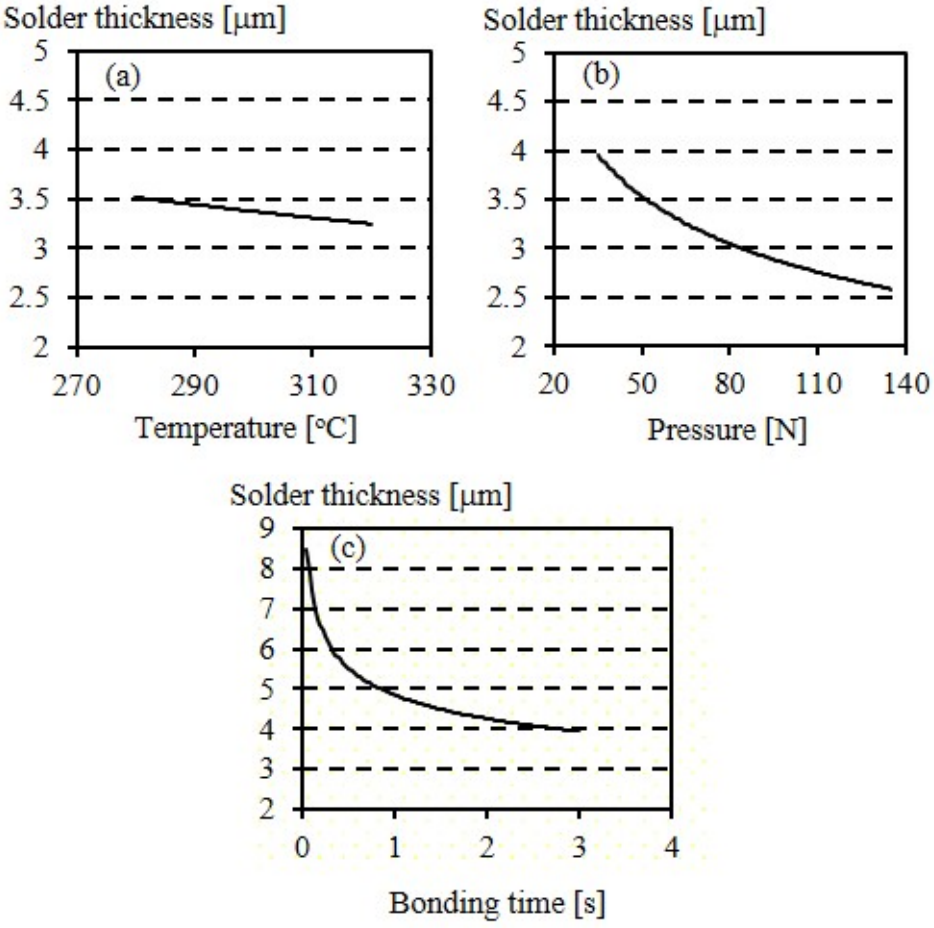


FIGURE 6.7: Effects of (a) temperature, (b) pressure and (c) bonding time on solder.

issue and contamination issue to TSV area were not observed, as shown in Figure 6.8 (a). On the back-side surface of logic die, UBMs which were connected to 1200 TSVs were exposed in the center of the die. In the next step, the memory die was bonded to the logic die, and NCP fillet sufficiently covered the periphery of the memory die, as shown in Figure 6.8 (b). The cross-sectional view of the package after molding resin and BGA ball formation is shown in Figure 6.9 (a). The 260 μm-thick memory die was stacked on the 50 μm-thick logic die. Cu pillars, TSVs and micro bumps had the role of electrical connections. The space under overhangs of the memory die was completely filled with NCF. Thus, the optimization of the NCF size contributes to the realization of a void-free structure. In spite of the multi-die stacked structure, the total package thickness including BGA ball achieved 1.0 mm max. Figures 6.9 (b) and (c) show the Cu pillars interconnections between the logic die and the package substrate, the micro-bumps interconnections between the memory die and the logic die. The solder coating technology on Cu leads of the substrate realizes sufficient solder wettability at the flip chip joints, as shown in Figure 6.9 (b). The memory die and the logic die had also a good soldering connection, despite the bump pitch of 40 μm/50 μm, as shown in Figure 6.9 (c). The underfill void is another contributing factor which affects the package quality. In this new assembly process, any underfill void under the logic die or the memory die was not detected by observations after horizontal polishing, as shown in Figure 6.10.

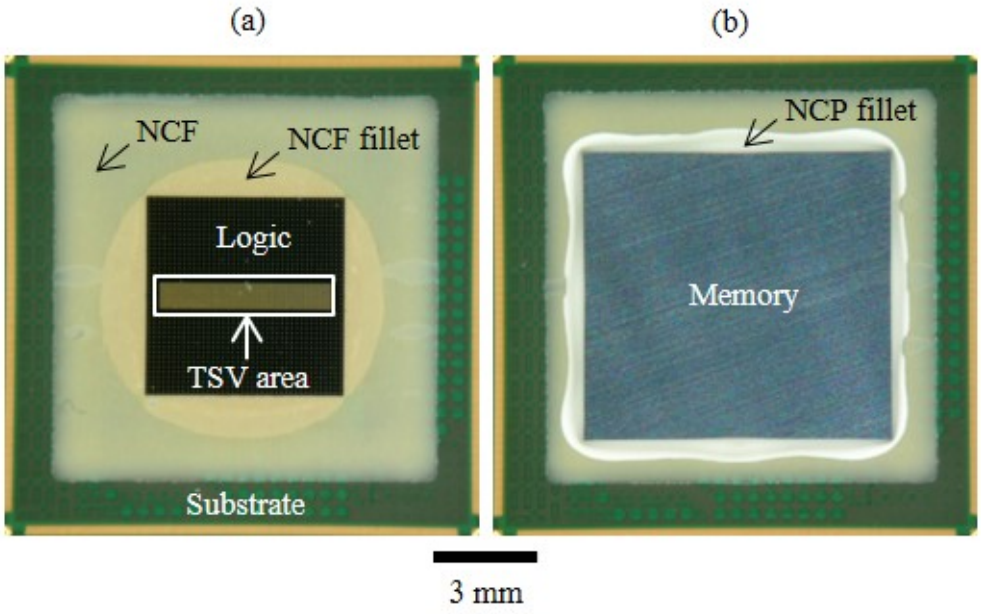


FIGURE 6.8: Prototype photographs. (a) after the 1st die (logic die) bonding. (b) after the 2nd die (memory die) bonding.

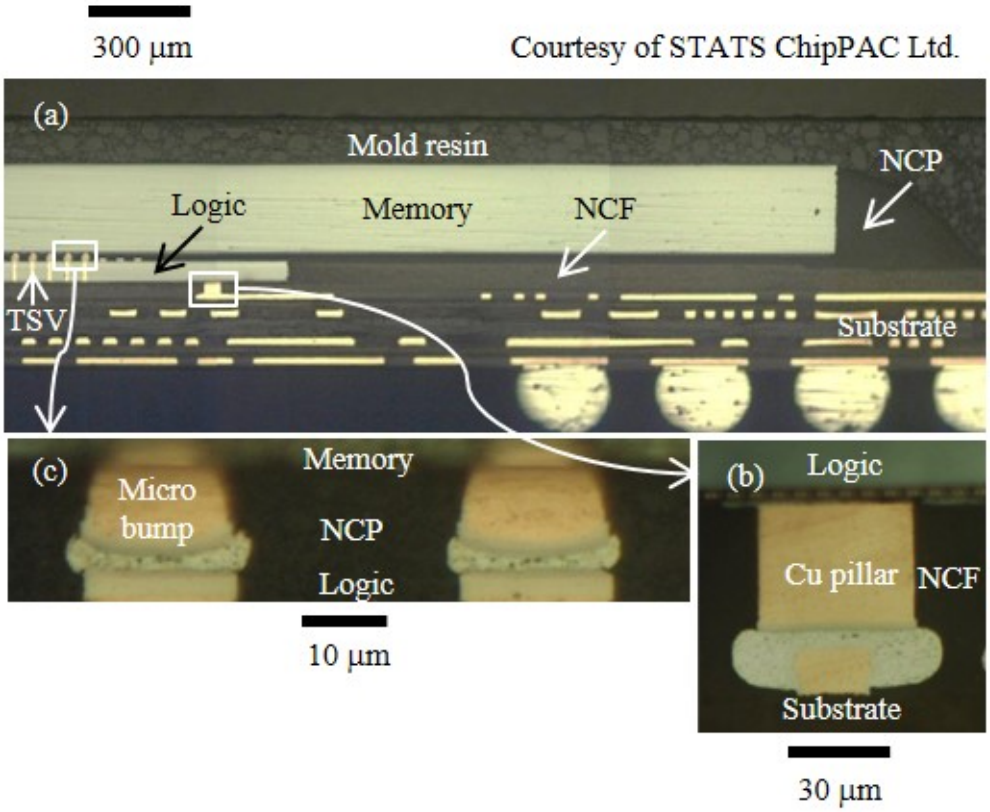


FIGURE 6.9: Cross-sections of the package.

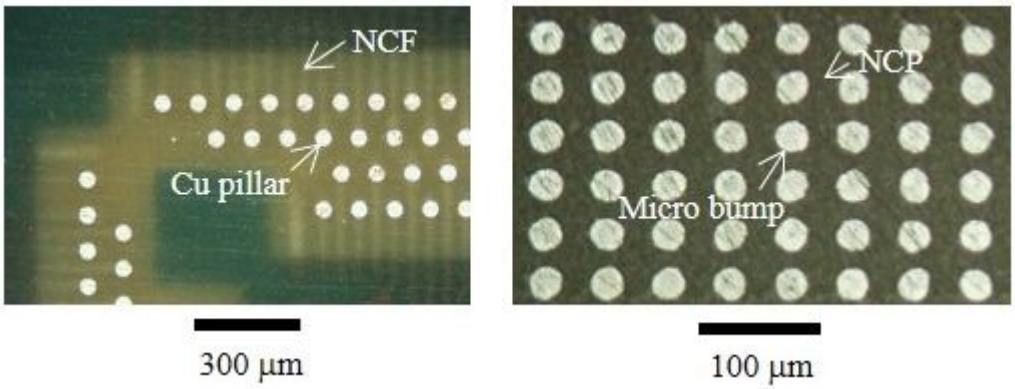


FIGURE 6.10: Observations of underfill void using pre-applied material (NCF and NCP).

6.4 Warpage Measurement

In general, the mobile applications require the small packages in addition to high electrical performances. In order to solve this challengeable requirement, various package structures, processes and materials have been proposed. The package warpage is one of the critical behaviors and it depends on package types. In this work, the warpage profile was measured between room temperature and 260°C. The warpage result is shown in Figure 6.11. The warpage data was measured using a laser microscope at nine points on the package. The result shows excellent performance in the warpage behavior. The maximum warpage was approximately 60 μm.

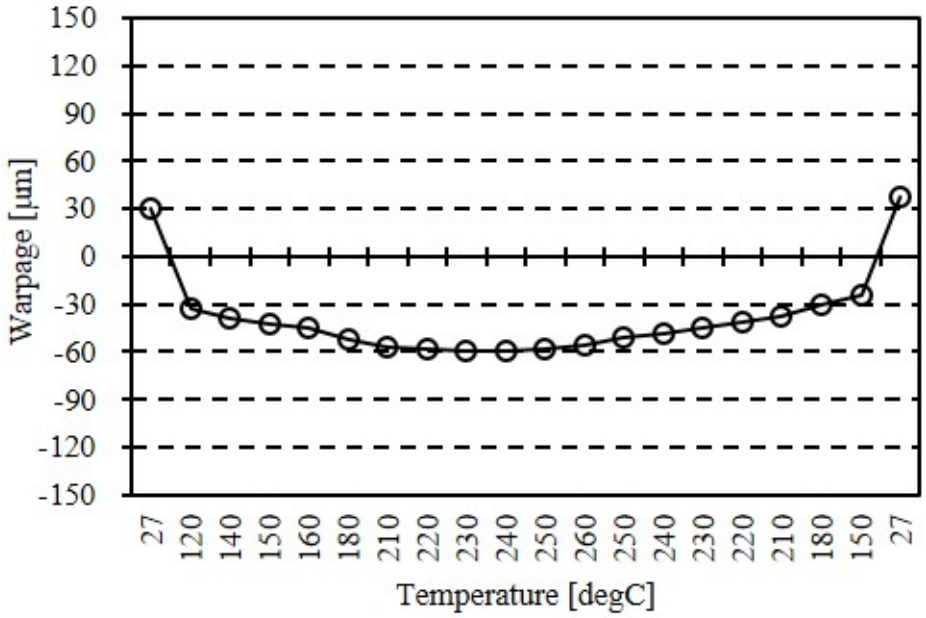


FIGURE 6.11: Package warpage between room temperature and 260°C.

6.5 Package Reliability

The reliability of the developed 3D package was evaluated by temperature cycling (TC), high temperature storage (HTS), high humidity test (HHT), unbiased highly accelerated stress test (uHAST) and pressure cooker test (PCT). Table 6.3 summarizes the reliability test conditions and results. Before the reliability tests, all samples were subjected to the moisture sensitivity level 3 (MSL3) (30°C/60% RH, 168h) and three times at peak reflow temperature 260°C. Any delamination or void in packages was inspected by Scanning Acoustic Tomograph (SAT) analysis. Figure 6.12 shows SAT images before and after MSL3, and no delamination or void was observed. In this test vehicle, daisy chains were laid out to assess the connections among the logic die, the memory die and 1200 TSVs. For all test items, the resistance of each daisy chain

was measured periodically. In these tests, the criterion of resistance increase was set to be within 10% of each initial value. Figures 6.13 (a) and (b) show resistance of the daisy chain loop including TSVs measured in TC and HTS. In all reliability tests, the change in resistance was less than ± 3%. In conclusion, all the samples passed 1500-cycle TC, 1000h HTS, 1000h HHT, 500h uHAST and 300h PCT, confirming the excellent long-term reliability.

TABLE 6.3: Test items and results of package level reliability.

Test Item (Test condition)	End point	Rsults
Temperature Cycling / TC (-55degC/125degC)	1500 cycles	45/45 pass
High Temperature Storage / HTS (150degC)	1000 h	45/45 pass
High Humidity Test / HHT (85degC/85%RH)	1000 h	45/45 pass
Unbiased Highly Accelerated Stress Test / uHAST (130degC/85%RH)	500 h	45/45 pass
Pressure Cooker Test / PCT (121degC/100%RH)	300 h	22/22 pass

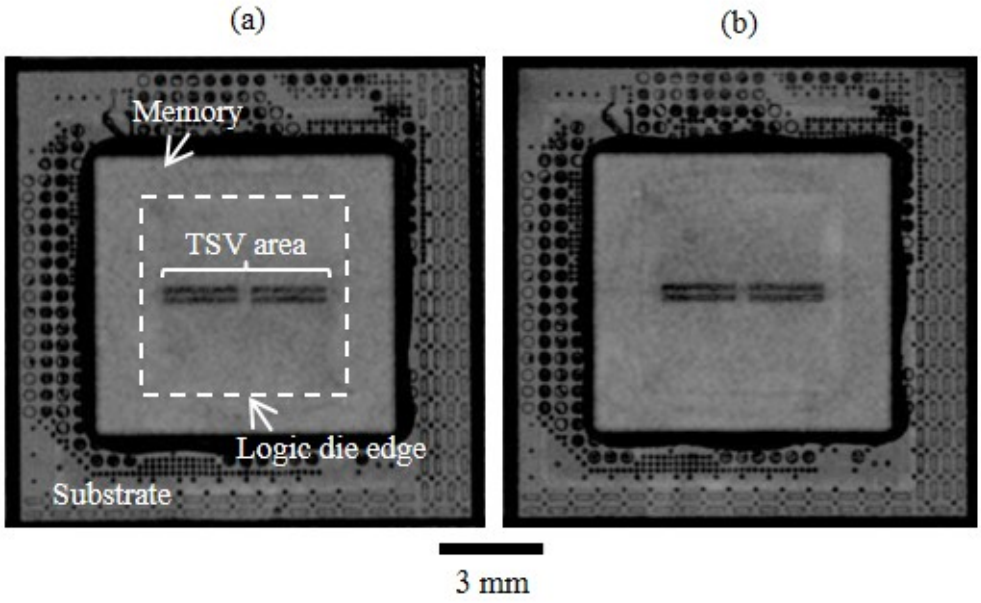


FIGURE 6.12: SAT images of the package. (a) before MSL. (b) after MSL

6.6 Demonstration

The primary advantage of die stacked 3D integration using TSV is the capability to realize SiPs composed of different wafer technologies. The 3D package combining 28 nm logic and Wide I/O DRAM was assembled to evaluate the actual performances

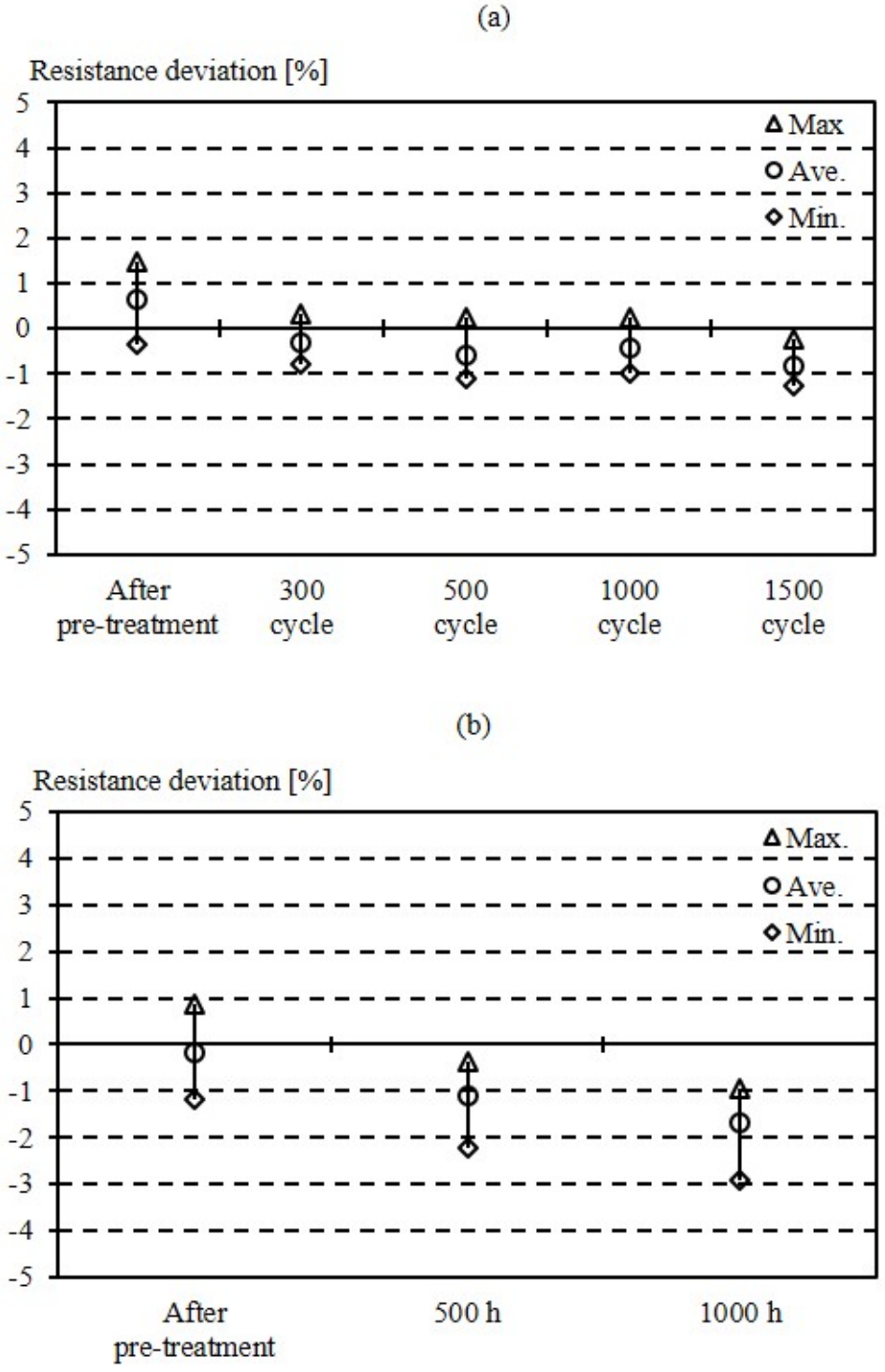


FIGURE 6.13: Resistance deviation during reliability tests. (a) TCT. (b)HTS.

of the newly developed unique assembly process. This 3D package had the extremely small logic device as a bottom die and the large memory device as a top die. The logic device was fabricated with 28 nm technology, and accompanied with 1200 TSVs, a size of 2 x 6 mm^2 and a thickness of 50 μm. The memory device was a 4 Gbit 512 DQs monolithic Wide I/O DRAM, and accompanied with a size of 9 x 9 mm^2 and a thickness of 260 μm. Figure 6.14 shows typical outline photographs after the small logic die was bond to a substrate and after the memory die was stacked on the bottom die. Although the bottom die was quite small compared to the top die, the space between the bottom die and the top die could be completely filled with NCF in the developed assembly process. After the unique assembly, electrical performances of the samples were evaluated using LSI testers. The connectivity of 1200 TSVs, DRAM bit quality, at speed test and current consumption were also carefully examined. Figure 6.15 shows the shmoo plots for the function-tested package. X and Y axes indicate the operating voltage and the frequency. The shmoo plots show the 3D vehicle had sufficient operation margin. In conclusion, the test vehicle proved to be able to achieve 12.8 GB/s operation at Vmin 1.07 V. In addition, the power consumption was evaluated by measuring IDD4R, which is a burst read current of 12.8 GB/s at 50% data toggle. The average power per bandwidth was 0.41 mW/Gbps. It was also showed 89% reduction of IO power compared to 6.4 GB/s LPDDR3, as shown in Figure 6.16.

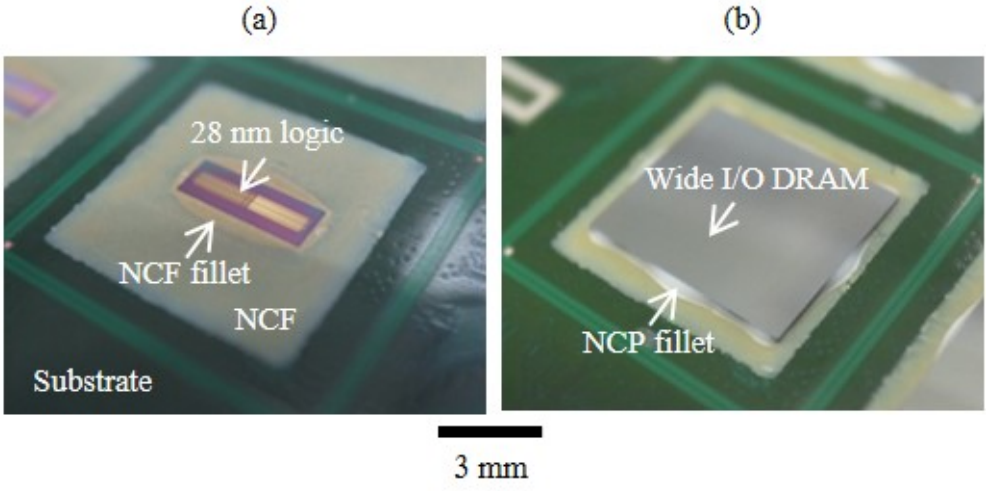


FIGURE 6.14: Prototype photographs. (a) after 28 nm logic bonding and (b) after Wide IO DRAM bonding.

6.7 Thermal Challenges

Figure 6.17 shows the thermal analysis result of a worst case operation for both PoP and 3D/TSV structures [141]. In the 3D/TSV case, a large thermal gradient was observed in the DRAM due to the hot logic die (SoC). In the PoP case, on the other hand, the heat was dissipated sufficiently. Since this thermal gradient

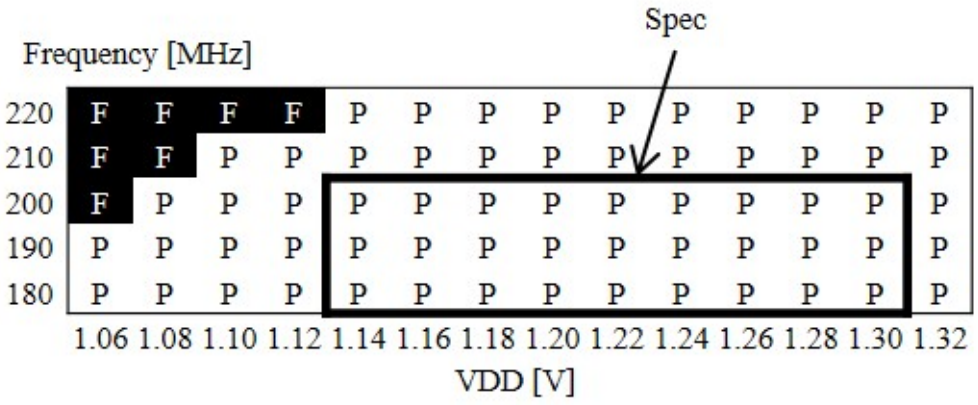


FIGURE 6.15: Shmoo plot of the 3D/TSV package with Wide IO DRAM.

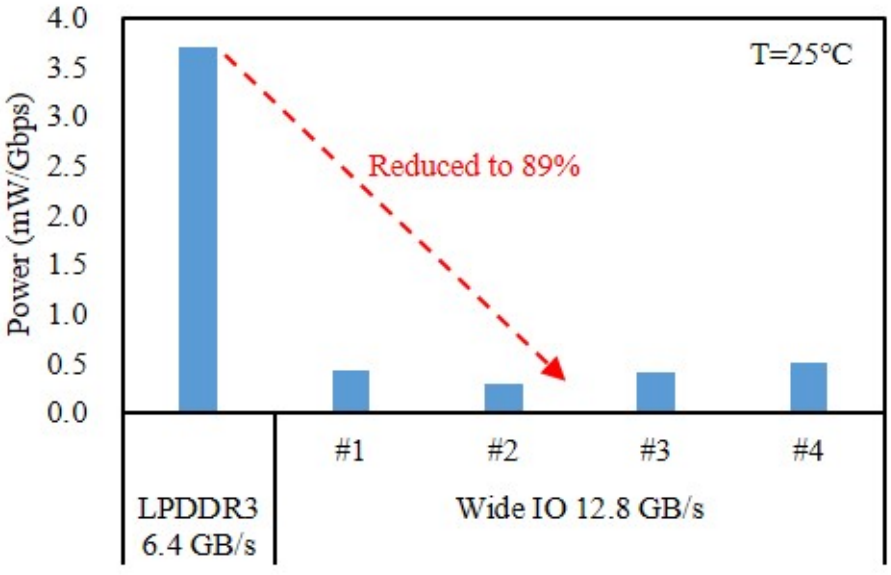


FIGURE 6.16: Measured IO power consumptions.

is caused by the floorplan of the SoC, it is difficult for the DRAM thermal sensor to detect the worst temperature. This thermal problem can lead to local refresh errors in the induced hot spots. There are three ways to solve this problem. The first approach is to use thermally resistant memory such as MRAM or ReRAM. The second approach is to change the package structure to 2.1D/2.3D or 2.5D to improve heat dissipation while maintaining the advantages of 3D/TSV. The third approach is to implement thermal management on the SoC side to realize such a 3D stacked memory system. When multiple logic and memory devices are integrated in 3D package using TSVs, the selection of structures, materials, and integration methods will become increasingly important to manage thermal diffusion and hot spots.

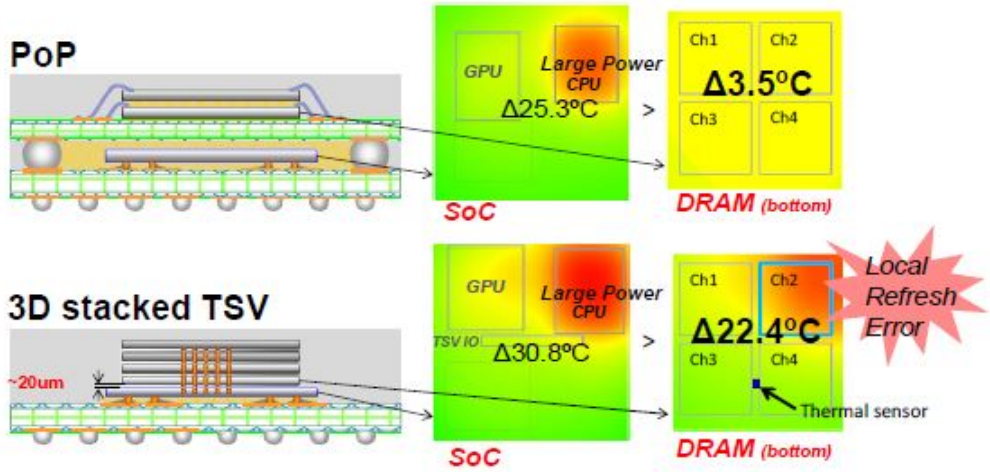


FIGURE 6.17: Examples of thermal analysis for PoP and 3D/TSV structures.

6.8 Summary

The innovative assembly process using NCF and solder coating technology has been developed for high density and reliable 3D/TSV integration. All of the samples passed 1500-cycle TC, 1000h HTS, 1000h HHT, 500h uHAST and 300h PCT. Furthermore, using this technology, 28 nm logic device and Wide I/O DRAM were assembled into 3D structure, and the 3D test vehicle achieved transmission rate of 12.8 GB/s and 89% reduction of I/O power consumption compared to LPDDR3. As a result, the new robust process for 3D/TSV integration has been established using different devices, different sizes and different materials. This unique process technology is expected to become a promising way to achieve high density and reliable 3D integration in the future.

Chapter 7

Conclusions

7.1 Thesis Summary

In this thesis, five novel high-density and reliable SiP structures and processes are described. First, in the PCB process, a thin PoP structure was developed using the coreless substrate described in Chapter 2, and a thin, reliable, and high-heat-dissipation embedded die was developed using the Cu base plate introduced in Chapter 3. Next, as RDL process, a low-die-shift and low-warpage 2D FOWLP was developed using a low-elasticity mold, as described in Chapter 4, and a low-cost 3D FOWLP was developed using a photosensitive mold, as introduced in Chapter 5. Finally, as part of the chip assembly process, a reliable chip assembly process for thin chips with TSVs was developed using NCF, as reported in Chapter 6.

In Chapter 2, a novel PoP technology for achieving a small package thickness and low package warpage was developed. The developed package structure is based on an ultrathin coreless substrate, called a multilayer thin substrate (MLTS). MLTS was fabricated by completely removing the Cu base plate after the formation of high-density build-up layers on the base plate. In this study, however, Cu posts were formed by selective wet etching of the Cu base plate. Because the novel package has built-in Cu posts as external terminals, the overall substrate can be molded for the peripheral area as well as the chip mounting area. This overmolded structure contributes to the warpage reduction of the PoP bottom package. The developed PoP bottom package had 361 pads arranged in five rows with 500 μm pitch. The thickness was only 230 μm, which is about 50% thinner than conventional build-up substrate.

In Chapter 3, a thin, reliable, low-thermal-resistance LSI packaging technology by embedding a high-pin-count LSI chip into thin build-up layers was developed using MLTS technology. The embedded LSI chip is a microprocessor with approximately 1500 pads and a thickness of 50 μm, and it was completely laminated by the first build-up of the epoxy resin. The total package thickness is only 0.71 mm including a 0.5-mm-thick Cu plate for cooling, which is much thinner than a conventional FCBGA package with a heat sink. The developed package showed excellent warpage characteristics of only 34 μm at room temperature for a size of 27 mm $\times$ 27 mm. A low thermal resistance of 10.8°C/W was achieved for the

packages with a 0.5-mm-thick Cu plate at a wind velocity of 0 m/s, which is almost comparable to that of an FCBGA with a large heat sink. The functions of using an LSI tester and a personal computer-like system board have been successfully demonstrated. They also passed a 2000-cycle package-level thermal cycle test.

Figure 7.1 shows a summary of Chapters 2 and 3, whereby the comparison object in Chapter 2 is a PoP bottom package using a build-up substrate with large through-holes, and the comparison object in Chapter 3 is an FCBGA. Both packages showed an improved performance index for SiP over conventional packages for their respective compared parameters. However, the embedded die in Chapter 3 is more expensive to manufacture because the yield of the PCB process affects KGD.

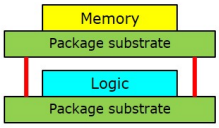
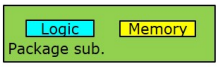
		Chapter 2	Chapter 3
		Thin Package Substrate	Embedded Die
Target structure			
Base technology		**PCB technology**	
SiP type		3D	2D
Comparison object		PoP using buildup substrate	FCBGA
Current issues		**Package Height, Transmission Delay**	
Approaches		✓ **Coreless substrate** ✓ **Cu etched post**	✓ **Coreless substrate** ✓ **Embedded die** ✓ **Cu direct plating** ✓ **Cu base plate**
Features for comparison	Functional Density	Excellent	Excellent
	Package Warpage	Good	Excellent
	Thermal Performance	Good	Excellent
	Thin Package	Excellent	Excellent
	Robust Reliability	Good	Excellent
	Low Inductance	Excellent	Excellent
	Manufacturing Cost	Excellent	Poor

FIGURE 7.1: Summary of Chapter 2 and Chapter 3.

In Chapter 4, a 5-in-1 FOWLP that integrates one fully operative artificial intelligence (AI) chip with approximately 2,500 pins and four memory chips for IoT modules was developed. Three typical issues with FOWLP are (1) die shift, (2) wafer warpage, and (3) fine RDL formation, which all can be solved by adopting a low elastic modulus mold resin and bonding a Si substrate onto the backside of the reconfigured wafer. The developed package provided a die shift of less than ±5 μm, a package warpage of 10.6 μm over an area of 31 mm × 31 mm, and a three-layer RDL formation with L/S = 10 μm/20 μm. Function testing of the AI chip and memory chips using a computer circuit board was successfully demonstrated.

In Chapter 5, an innovative 3D fan-out packaging and integration technology with a newly developed photosensitive mold material was presented. This technology does not require tall Cu pillar electroplating or laser drilling. A test die was mounted on a substrate facing upward, and then, the entire substrate was laminated with a photosensitive mold film thicker than 100 μm. A lithography process was executed on the mold film to form openings with a depth of 10 μm on the embedded die and a depth of 110 μm on the support substrate. The Cu RDL

formed electrical contacts between the die and the substrate through photosensitive vias with different diameters and depths. The developed 3D package passed 1000 thermal cycles from -55°C to 125°C.

Figure 7.2 shows a summary of Chapters 4 and 5, whereby the comparison object in Chapter 4 is a 2D FOWLP using a conventional EMC, and that in Chapter 5 is a 3D FOWLP using Cu pillars. Both packages have the same or a better SiP performance index than the conventional package. However, both mold resins are still in the development stage and need to be improved for improved reliability.

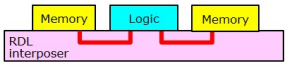
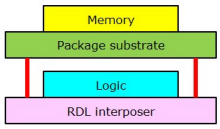
		Chapter 4	Chapter 5
		2D FOWLP	3D FOWLP
Target structure			
Base technology		RDL technology	
SiP type		2D	3D
Comparison object		2D FOWLP with EMC	3D FOWLP with Cu pillars
Current issues		Die shift, Warpage	Costly 3D interconnect
Approaches		✓ Low Elasticity Mold ✓ Backside Si support substrate	✓ Photosensitive Mold ✓ One time via opening ✓ Cu conformal electroplate ✓ Fine pitch via
Features for comparison	Functional Density	Excellent	Excellent
	Package Warpage	Excellent	Excellent
	Thermal Performance	Good	Good
	Thin Package	Good	Good
	Robust Reliability	Average	Average
	Low Inductance	Good	Good
	Manufacturing Cost	Good	Excellent

FIGURE 7.2: Summary of Chapter 4 and Chapter 5.

As reported on in Chapter 6, an innovative flip chip assembly process with a NCF contributed to a high-density and reliable 3D/TSV integration. The target package had a two-tier structure consisting of a logic device and wide I/O DRAM. The logic device was fabricated by a via-middle process accompanied by 1200 TSVs with a thickness of 50 μm and a 40 μm/50 μm bump pitch layout. The thermal-compression bonding method with a Cu pillar was applied to both connections, i.e., between the memory die and the logic die and between the logic die and an organic substrate to achieve high reliability. In this study, a 28 nm logic device and Wide I/O DRAM were assembled into a 3D structure with this new technology and 12.8 GB/s transmission and an 89% reduction of I/O power compared with LPDDR3 were demonstrated.

Figure 7.3 shows a summary of Chapter 6, whereby the comparison object in Chapter 6 is a chip on chip (CoC) package for chip stacking without TSVs. 3D/TSV thermal issues and the increased cost of forming TSVs on logic devices are future challenges. However, this study showed that 3D/TSV assembly technology with NCF can be applied to future edge computing and large memory modules and provides a direction for 3D/TSV assembly development. Figure 7.4 shows a summary of the five newly developed SiPs.

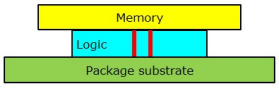
		Chapter 6
		3D/TSV
Target structure		
Base technology		Die stacking
SiP type		3D
Comparison object		CoC
Current issues		**Die stacking, Underfilling**
Approaches		✓ **Non-Conductive Film (NCF)** ✓ **Micro bumping bonding**
Features for comparison	Functional Density	Excellent
	Package Warpage	Excellent
	Thermal Performance	Poor
	Thin Package	Excellent
	Robust Reliability	Good
	Low Inductance	Excellent
	Manufacturing Cost	Poor

FIGURE 7.3: Summary of Chapter 6.

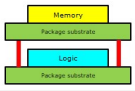
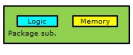
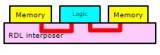
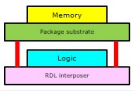
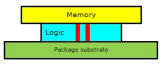
Chapter	Chapter 2	Chapter 3	Chapter 4	Chapter 5	Chapter 6
SiP structure	Thin package substrate	Embedded Die	2D FOWLP	3D FOWLP	3D/TSV
					
Key Technology	***Coreless***	***Embedded Die***	***Low Elasticity Mold***	***Photosensitive Mold***	***NCF assembly***
Comparison object	Conventional PoP	FCBGA	Conventional 2D FOWLP	Conventional 3D FOWLP	CoC
Process	PCB	PCB	RDL	RDL	RDL/TSV
Dimension	3D	2D	2D	3D	3D
TSV	No Need	No Need	No Need	No Need	Need
Package Substrate	Need	Need	No Need	No Need	Need
Interconnect	C4	Cu plating	Cu plating	Cu plating	ubump
Manufacturing cost	Low	Low	Middle	Middle	High
Bump pitch [um]	150	150	80	80	40
L/S [um]	20 / 20	20 / 20	10 / 10	10 / 10	-

FIGURE 7.4: Summary of developed SiP structures in this thesis.

7.2 Packaging Technology Directions

The energy-efficient performance of real computing systems has improved at a rate of approximately doubling every two years over the past 15 years. This trend is expected to continue in the future [144], [145]. Energy-efficient performance is achieved not only through advances in transistor and integration technologies but also through innovations in design and architecture. Computational throughput is correlated with the number of transistors. SiP technologies such as chiplets and hetero-integration, which drive more than Moore, will continue to contribute to the trend of increasing the transistor count. Packaging technologies will require miniaturization of the interconnect pitch and TSVs to realize future high-end high-function/performance SiPs.

A miniaturization of the interconnect pitch between chips or between chips and interposers will be required. To improve the data transfer performance between logic and memory, the connection method has evolved from wire bonding technology and flip chip technology using solder bumps. In recent years, flip chip technology has evolved to μbumps using Cu pillars, which has contributed to the improvement of system performance. Furthermore, with the introduction of embedded die and FOWLP, direct Cu plating was adopted for the interconnect between the chip and the fan-out layer, and a minimum interconnect pitch of 20 μm was achieved. In the future, owing to further miniaturization of the interconnect pitch, and wafer-to-wafer (W2W) and die-to-wafer (D2W) technologies will become the mainstream interconnect method instead of the conventional die-to-die (D2D) technology [146]. In W2W, direct bonding will be used to connect Cu electrodes to Cu electrodes, as shown in Figure 7.5 [147]. Figure 7.6 shows a summary of the evolution of interposer and interconnection. The interconnection between chip and interposer is expected to evolve from wire bond, flip chip to Cu plating and finally to Cu-Cu direct bonding in the future.

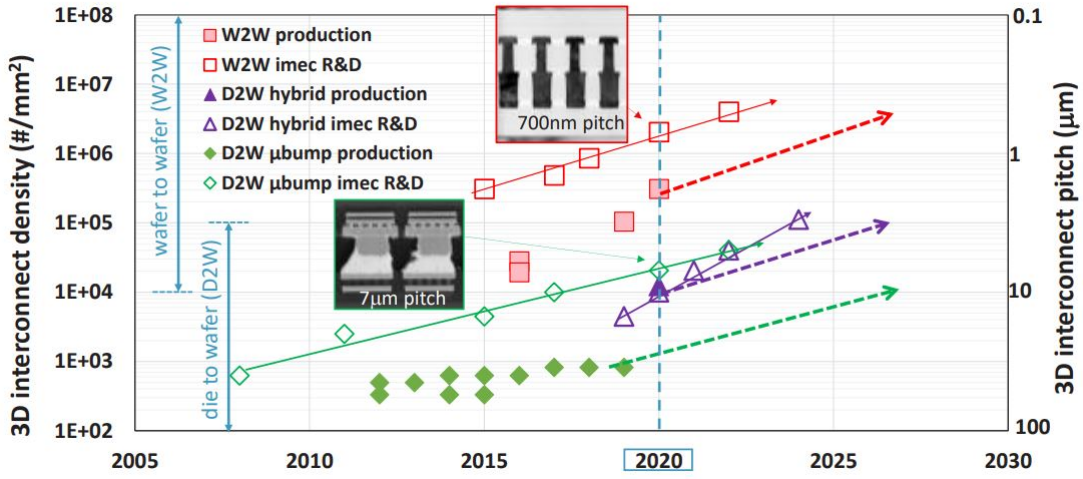


FIGURE 7.5: Interconnect roadmap.

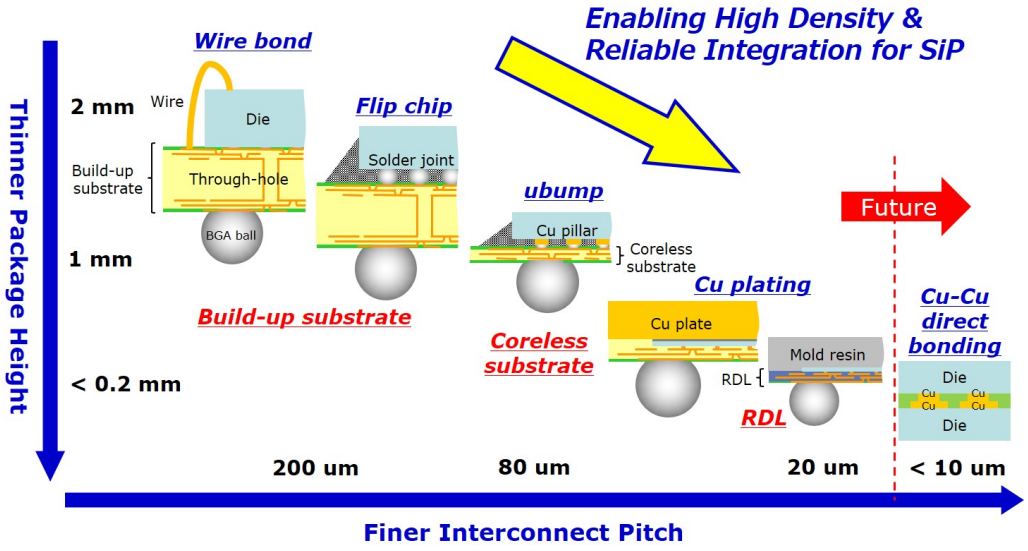


FIGURE 7.6: Evolution of interposer and interconnect.

The next step is TSV scaling. TSVs have been applied to Si interposers without active devices and stacked memory. In the future, TSV will be applied to logic device in more cases. By forming TSVs within the W2W process, it will become possible to realize TSVs with diameters of 1 μm or less, as shown in Figure 7.7 [146], [148]. In a Logic-TSV, thermal management is of primary importance, and the selection of package structures and materials with high heat dissipation is required.

With the miniaturization of interconnect pitch and TSVs, new technical issues are expected to arise in the processes of temporary bonding/debonding, back-grinding, TSV formation, RDL formation, and dicing in the intermediate process described in Chapter 1. In the future, it will become increasingly important to coordinate front-end, intermediate, and back-end processes, and to design chips and packages in a coordinated design, as shown in Figure 7.8.

7.3 Future Prospects of SiP

Since the early 2000s, Japanese semiconductor device manufacturers have focused on the importance of SiP using 3D stacked packaging technology as a method for realizing system LSI with a short delivery time and low development cost. The main development items for the SiP process were back-end process technologies that encompassed package substrate using PCB technology and chip assembly. Subsequently, in the 2010s, with the introduction of new TSV and FOWLP technologies, the importance of intermediate processes at the wafer level began to be recognized, and SiP process development items shifted from back-end process technology to intermediate process technology. Over the past 20 years, the evolution of packaging technology has provided an opportunity for reconsidering the role of

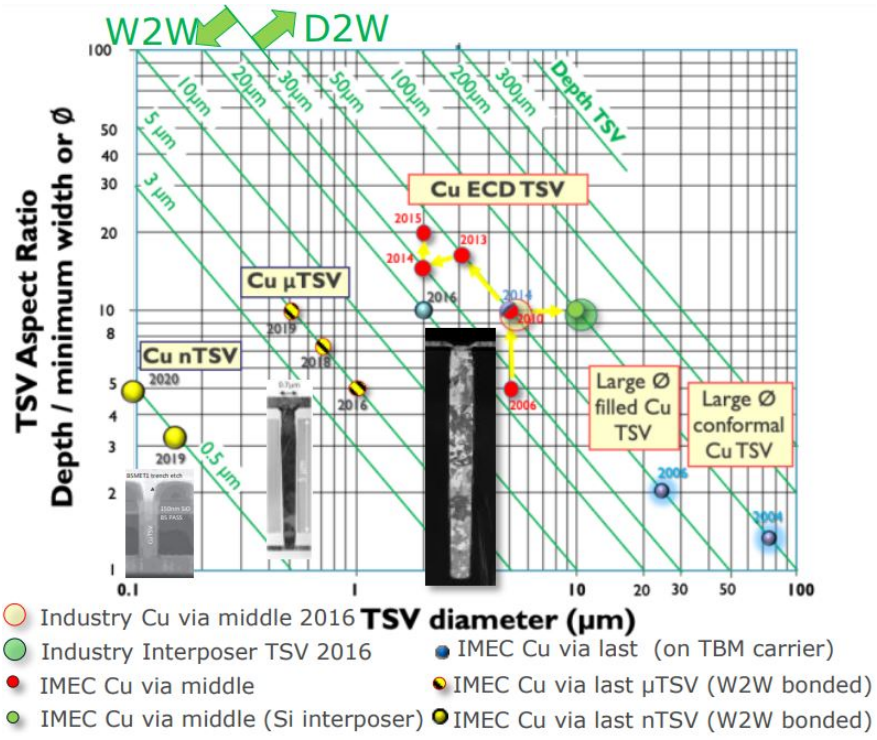


FIGURE 7.7: TSV scaling.

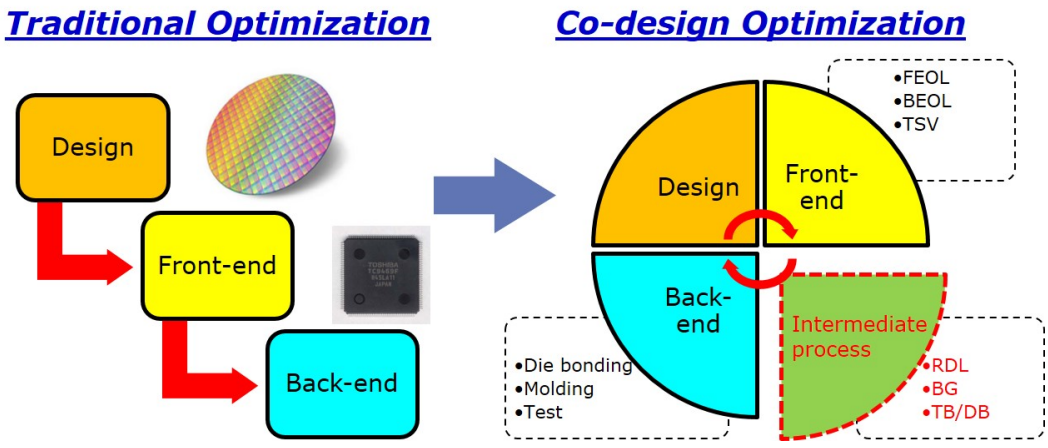


FIGURE 7.8: System Optimization.

back-end processes in semiconductor manufacturing technology and to create a new field of intermediate processes.

The evolution of intermediate process technology is expected to lead to the future growth of SiP. As Si interposers and stacked memory with TSVs have reached maturity, and the use of TSVs in logic is increasing, there is no doubt that 2.5D/3D integration using TSV technology will become the mainstream of future SiP. However, chip-to-chip connection technology using embedded die (bridge die) technology based on package substrate technology and high-density package substrate technology such as 2.1D/2.3D, in which fine wiring equivalent to BEOL or RDL wiring is placed on a conventional buildup substrate, will continue to be promising as a low-cost solution. Furthermore, to build the heterogeneous integration that More than Moore is aiming for, different devices, chip sizes, and materials must be efficiently packaged into a single package to achieve high-speed data transfer and low-power operation.

As previously mentioned, various packaging technologies and their combinations are expected to help realize various SiP applications. In the following section, two future SiP applications are described. One is an SiP for cyber-physical systems (CPS), and the other is an SiP for power devices.

First, a promising SiP product is a package that combines logic (CPU, GPU) and memory (DRAM) used in CPS. CPS is a framework for creating added value by collecting data in the physical world, analyzing it in the cyber world using digital technology, and then feeding it back into the physical world, as shown in Figure 7.9 [149]. Therefore, there are high expectations for SiPs in terms of realizing high-speed processing and low power consumption by the combination of a logic chip that calculates the collected data with a high-bandwidth, large-capacity memory chip into a single package. 2.5D, FOWLP, and 3D/TSV are expected to be used in SiP for CPS.

Second, the expected SiP products in the future are modules that use power devices related to energy issues. As the switching frequency of next-generation power devices (SiC, GaN) increases at high speeds (over 100 kHz), low inductance and high heat dissipation packaging technologies are required. As a package technology realizing these requirements, improvements in switching speed and miniaturization by modularization are being considered using embedded dies and FOWLP for power devices.

I believe that the elemental technologies for electronics packaging developed in this study will contribute to further research, the development, and practical applications of future high-performance and multifunctional SiP products.

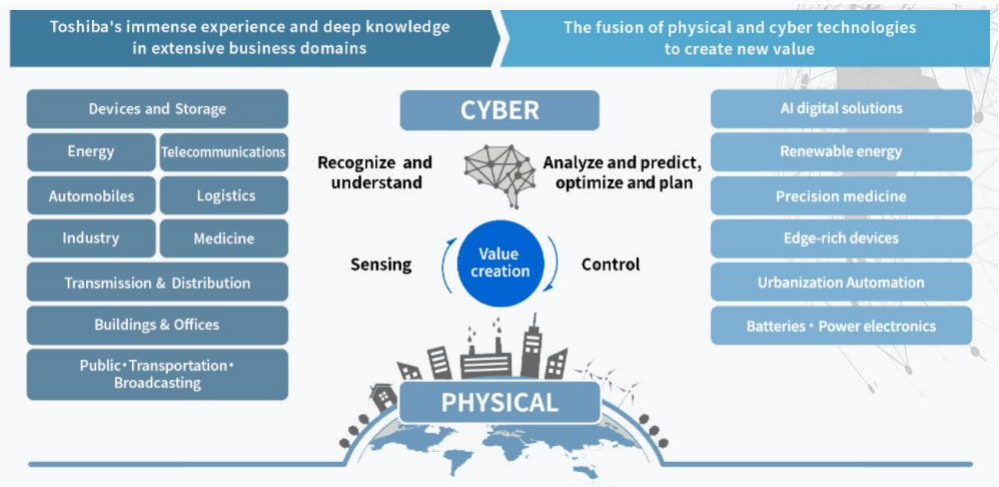


FIGURE 7.9: TOSHIBA Cyber Physical Systems. [149]

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List of Journals with peer-review

Journals that published the main part of this thesis

1. Kentaro Mori, Katsumi Kikuchi, Shinji Watanabe, Daisuke Ejima, Jun Tsukano, Tomoo Murakami, and Shintaro Yamamichi. "A Novel Package-on-Package Technology Using Coreless Substrate with Cu Posts." Journal of The Japan Institute of Electronics Packaging 11, no. 1 (2008): 66-71.

2. Kentaro Mori, Daisuke Ohshima, Hideki Sasaki, Yuki Fujimura, Katsumi Kikuchi, Yoshiki Nakashima, Mitsuru Enomoto, Ryu Miki, Takeya Hashiguchi, Takuo Funaya, Tomohiro Nishiyama, Shintaro Yamamichi. "Embedded Active Packaging Technology for High-Pin-Count LSI With Cu Plate." IEEE Transactions on Components, Packaging and Manufacturing Technology 1, no. 1 (2010): 60-68.

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4. Kentaro Mori, Soichi Yamashita, and Masahiro Sekiguchi. "5-in-1 Fan-Out Wafer-Level Packaging Technology with One AI Chip and Four Memory Chips for Internet of Things Modules." Transactions of The Japan Institute of Electronics Packaging 14 (2021): E21-002.

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1. Yoshiki Nakashima, Katsumi Kikuchi, Kentaro Mori, Daisuke Ohshima, and Shintaro Yamamichi. "Warpage Mechanism of Thin Embedded LSI Packages." Transactions of The Japan Institute of Electronics Packaging 3, no. 1 (2010): 47-56.

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1. Kentaro Mori, Katsumi Kikuchi, Shinji Watanabe, Daisuke Ejima, Jun Tsukano, Tomoo Murakami and Shintaro Yamamichi. "A Novel Package-on-Package Technology having Ultra-Thin Coreless Substrate with Cu posts." In Proceedings of the International Conference on Electronics Packaging 2007, April. 2007.

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6. Kentaro Mori, Soichi Yamashita, Takafumi Fukuda, Masahiro Sekiguchi, Hirokazu Ezawa, and Shuzo Akejima. "3D Fan-Out Package Technology with Photosensitive Through Mold Interconnects." In 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), pp. 1140-1145. IEEE, 2019.

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Awards

MES 2006 Research Encouragement Award
ICEP 2007 Outstanding Technical Paper Award