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題目(和文)	結晶性向上プロセス及びサイドコンタクト技術を用いた PVD成膜高移動度TMDC膜二次元チャネルFET技術
Title(English)	2D-Channel FET based on High-Mobility TMDC-Film Formation with PVD Method using Crystal-Quality Improvement Process and Side-Contact Architecture
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論 文 要 約

THESIS OUTLINE

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要約
Thesis Outline

A technology node of the most advanced logic has already reached 5 nm, and future technology node will see adoption of nanosheet structures, which will further enhance drivability and reduce a cell size. In the next generation transistors, a channel thickness has to be smaller than 5 nm to suppress short channel effects and enhance gate controllability, but mobility degradation and characteristic variation become sever. As a candidate to meet the requirements, 2D transition metal dichalcogenide (TMDC) films have great attentions because of high mobility and excellent interfacial properties even at an atomically thin thickness. Before 2D channel FETs can reach their full potential, several key challenges remain. This paper highlights a synthesis method with chip-level size, a crystallinity-improvement process for 2D semiconductor films, and a dedicated contact architecture.

Ch. 3 focuses on a 2D ZrS_2 film, which has been predicted to have excellent electrical properties among 2D semiconductors in recent years, and try to demonstrate a large-area deposition of that film using a combination of sputtering method, which is one of the physical vapor deposition (PVD) methods, and sulfur vapor annealing for compensation of sulfur vacancies. PVD ZrS_2 films formed with different deposition conditions are characterized by RAMAN spectroscopy, X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), and Hall-effect measurement. XPS and TEM measurements show that a layered poly crystalline ZrS_2 film was successfully formed over a centimeter-level SiO_2 substrate and a crystal orientation of that film is greatly affected by a substrate temperature of sputtering. The Raman spectra of ZrS_2 films with different sulfur annealing temperatures indicates a high temperature improves a crystallinity of the film. From the Hall effect measurement, it was found that electrical properties of the film were successfully controlled by sputtering conditions where sputtering power and substrate temperature greatly affected electrical properties of the film. Eventually, average values of a Hall-effect mobility 1,250 $cm^2V^{-1}s^{-1}$ and a carrier density 8.5 x 10^{17} cm^{-3} were remarkably achieved.

For an improvement of crystallinity and an interface of TMDC films, Chapter. 4 investigated a novel crystallinity improvement process of sulfur-based TMDC films with using sulfurization annealing through a thin Al_2O_3 passivation film which suppresses influences from the environment. It was found that a crystallinity of a sputtered MoS_2 film was achieved by the sulfurization, even through an Al_2O_3 passivation film and a higher Hall-effect mobility of 100

$cm^2V^{-1}s^{-1}$ was achieved with a 3-nm Al_2O_3 passivation film as compared to 25 $cm^2V^{-1}s^{-1}$ for an as-deposited MoS_2 film. The sulfur annealing of a ZrS_2 film through an Al_2O_3 passivation film was also investigated with using the conditions optimized with a MoS_2 film. RAMAN results indicated that the sulfur annealing through an Al_2O_3 film greatly improved a crystallinity of a ZrS_2 film compared to the annealing without the passivation film, and XPS results shows that the sulfur annealing through the passivation film efficiently promotes Zr-S chemical bonding.

In order to investigate a contact architecture with a high immunity to further scaling dedicated to 2D materials, Ch. 5 tried investigates a ZrS_2-Ni side contact for the first time. It was confirmed that an annealing process with argon significantly enhances a current value, and the contact resistance of the side contact is calculated to be about 10^4-10^5 W-mm which is competitive with most reported contact resistances of two-dimensional semiconductors. Furthermore, an exposure to the atmosphere just before metal deposition causes non-uniform I-V characteristics and it can be mitigated by annealing process.

Ch. 6 demonstrates chip-level-integrated 2D-chnnel MISFETs using a ZrS_2 film formed by a combination of a sputtering method and a sulfur vapor annealing. ZrS_2 MISFET arrays were successfully fabricated over a centimeter-size SiO_2 substrate. In I_d, I_s, and I_g-V_{gs} characteristics, since an I_d directly corresponds to an I_s value and an I_g is sufficiently suppressed, the ALD Al_2O_3 film shows good insulation behavior even on a ZrS_2 film. The FETs shows an ambipolar operation attributed to both electron and hole carriers, and different threshold voltages are obtained with and without F.G. annealing. It was speculated that the ambipolar operation of the ZrS_2 FETs is explained by the Schottky-barrier-FET model, where Schottky barriers for electrons and holes are controlled by a gate-electric field in contact areas, and the positive shift of the threshold voltage is due to a decrease in positive fixed charges at the Al_2O_3/ZrS_2 interface and a change of the ZrS_2/TiN band alignment at the contact area by annealing process. It was noted that the FETs performed both electron and hole conductions for the first time, which is an important milestone for the realization of n/p-type unipolar ZrS_2 FETs.

The results of this paper are fundamental technologies for an integration of 2D materials in future stacked-nanosheet FETs will contribute to an enhancement of advanced logic LSI performances.