

論文 / 著書情報  
Article / Book Information

題目(和文)	
Title(English)	A Study of Fractional-N Oversampling Frequency Synthesizers Using Digital-Assisted Calibration
著者(和文)	QiuJunjun
Author(English)	Junjun Qiu
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第12279号, 授与年月日:2022年6月30日, 学位の種別:課程博士, 審査員:岡田 健一,高木 茂孝,本村 真人,徳田 崇,伊藤 浩之,飯塚 哲也
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第12279号, Conferred date:2022/6/30, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Category(English)	Doctoral Thesis
種別(和文)	要約
Type(English)	Outline

# 論文要約

## THESIS OUTLINE

系・コース :	電気電子	系 コース	申請学位 (専攻分野) :	博士	(philosophy)
Department of, Graduate major in			Academic Degree Requested	Doctor of	
学生氏名 :	QIU JUNJUN		指導教員 (主) :		岡田健一
Student's Name			Academic Supervisor(main)		

This thesis focusses on the study of fractional-N oversampling PLL design with the digital-assisted calibration methods.

1. Introduction
  - 1.1 Internet of Things
  - 1.2 Trends of Integrated Circuits
  - 1.3 Trends of PLL Design
  - 1.4 Thesis Organization
2. Conventional Sampling PLL Design and Limitation
  - 2.1 Fractional-N PLL Introduction
  - 2.2 PLL Design Basics
  - 2.3 Sampling PLL Design
  - 2.4 Limitation of The Conventional PLLs
3. Uniform Oversampling PLL Design
  - 3.1 Introduction
  - 3.2 Circuit Implementation
  - 3.3 Measurement Results
  - 3.4 Conclusion
4. Other Oversampling PLL Design
  - 4.1 Introduction
  - 4.2 Circuit Implementation
  - 4.3 Simulation and Measurement Results
  - 4.4 Conclusion
5. PLL Application in Receiver Baseband Circuit
  - 5.1 Introduction
  - 5.2 Prior Demodulation Method
  - 5.3 Implementation and Simulation
  - 5.4 Performance Evaluation
  - 5.5 Conclusion
6. Conclusion and Future Work
  - 6.1 Conclusion
  - 6.2 Future Directions