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Article / Book Information

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Category(English)	Doctoral Thesis
種別(和文)	論文要旨
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（博士課程）
Doctoral Program

論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Wireless communication plays an irreplaceable role in people's life. In wireless communication, the transceiver (TRX) is necessary for signal transmission and reception. The frequency synthesizer, working as the crucial block in the TRX, determines the transceiver performance. Furthermore, the frequency synthesizer also determines the performance in the data converters and carrier and timing recovery circuits. A wide loop bandwidth, low jitter and low power frequency synthesizer are in high demand for wireless communication support.

This thesis focuses on the study of oversampling phase-locked loop (OSPLL) design. In the conventional PLL design, only the rising edge information is utilized for phase detection. This limited the phase-detection frequency equal to the reference frequency and limited the achievable loop bandwidth. With the Gardner loop bandwidth rule, the loop bandwidth is limited to be 1/10 of the reference frequency with the type II PLL. Even with the other PLL architecture, like injection lock PLL, the loop bandwidth is limited to be less than half of the reference frequency.

To overcome this limitation, the uniform OSPLL is firstly proposed to fully utilize the reference voltage and time information to boost the phase-detection frequency to be oversampling ratio times of the reference frequency. Digital to analog converter (DAC) and digital to time converter (DTC) are utilized for the voltage and time-domain compensation to realize a finer phase-detection resolution. Furthermore, the look-up-table (LuT) based calibration method is proposed to follow the reference change in real-time adaptively. The phase detector resolution is improved with the proposed architecture. To suppress the slope related noise, a cosine function-based weight is added before the loop filter to tune the loop gain with different sampling points. The proposed OSPLL is fabricated in 65nm CMOS technology. The measured performance shows that it realizes around 200kHz loop bandwidth with 5.79ps jitter performance in near-integer mode with 32kHz reference for 2.4GHz output.

To further suppress the in-band phase noise, nonuniform oversampling phase detection is proposed. The fixed-voltage step-based sampling is utilized to accommodate the sampling frequency of phase detection based on the reference signal slope. The proposed nonuniform OSPLL(NUOSPLL) effectively suppressed the phase noise contributed by comparator voltage because the slow slope signal part is avoided to do the phase detection. To compensate the variable loop delay and slope related noise, adaptive loop gain calibration is proposed. With different sampling point, the loop gain automatically tunes and minimize the jitter at corresponding points. The simulated jitter performance of nonuniform OSPLL(NUOSPLL) is 5 ps with a 32 kHz at fractional-N mode with 200kHz loop bandwidth, the measured power consumption is 4 mW.

Following the story, to avoid the sine peak region for the phase detection, the reference-switch OSPLL(RS-OSPLL) is proposed to connect the phase-0 and phase-90 references to the PLL loop. A Digital circuit-based reference slope detection method is proposed in the RS-OSPLL to generate the switch enable signal. The non-overlapped clock control is implemented to avoid the time conflict between the switch enable signal and the phase detection clock. With the simulated jitter performance of RS-OSPLL is 4.3ps with a 32kHz at fractional-N mode with 200kHz loop bandwidth.

As an extension, the PLL circuit theory can also be applied to the digital baseband circuit. In super-heterodyne RX, the inter-mediate frequency is recovered after ADC. The proposed digital baseband

circuit contains carrier recovery for the carrier frequency synchronization, timing recovery for the optimal sampling point down-conversion, and the decoder block for symbol demodulation. The carrier recovery is designed with a proposed modified Costas loop and the timing recovery is designed with the typical Gardner timing recovery loop. The feedback loop, like PLL operation, is adopted in both carrier recovery and timing recovery loops. The proposed DBB circuit is fabricated in 65nm CMOS technology. It realizes a less than 0.0001% BER performance at the 15dB signal to noise ratio additive white gaussian noise (AWGN) channel.

The thesis also points out the future directions for OSPLL and wireless circuit design. The phase modulation function can be integrated with OSPLL for the wireless support. This calls for the lower jitter performance which is the future direction for OSPLL. For the future wireless communication, the lower power consumption system, size and cost reduced system on chip devices and high configurable wireless system to support multi-channel operation can be predicted for the future application.