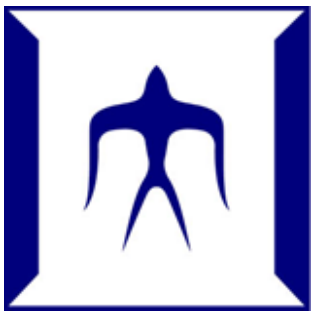
論文 / 著書情報
Article / Book Information

題目(和文)	
Title(English)	Ultra-Low-Power Ka-Band CMOS Transceiver Using Mutually Coupled Inductors for Small Satellite System
著者(和文)	FU Xi
Author(English)	Xi FU
出典(和文)	学位:博士(学術), 学位授与機関:東京工業大学, 報告番号:甲第12243号, 授与年月日:2022年9月22日, 学位の種別:課程博士, 審査員:岡田 健一,白根 篤史,廣川 二郎,德田 崇,伊藤 浩之,藤井 威生
Citation(English)	Degree:Doctor (Academic), Conferring organization: Tokyo Institute of Technology, Report number:甲第12243号, Conferred date:2022/9/22, Degree Type:Course doctor, Examiner:,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis



Ultra-Low-Power Ka-Band CMOS Transceiver Using Mutually Coupled Inductors for Small Satellite System

by

Xi Fu

A Ph.D. dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Electronic Engineering

in the

School of Engineering

of

Tokyo Institute of Technology

Supervised by

Prof. Kenichi Okada & Atsushi Shirane

Summer, 2022

To my family

Acknowledgment

It has been five years since the day I came to Japan. I think I am very lucky to have become a member of Okada Laboratory for pursuing my MS and Ph.D degrees at Tokyo Institute of Technology. My life in Okada Lab. is always full of happiness and support. Having the precious opportunity to discuss and realize ideas with excellent and intelligent people in Okada Lab is luck, and I always feel excited.

I would like to thank many people who have helped me throughout my study at Okada Laboratory, Tokyo Institute of Technology.

As an ordinary student in the lab of Prof. Kenichi Okada, I would like to express my deep gratitude and sincere appreciation to my supervisor, Prof. Okada, and Prof. Akira Matsuzawa. Without their approval, I cannot participate in Tokyo Institute of Technology and become a member of the Okada laboratory. During the past five years, Prof. Okada has given me valuable advice and comments on my life and research. Even though his hectic schedule, he was always there to help me whenever I met trouble spot or had any questions about my research. His unbelievable passion and unbeatable ambition push me a lot to fulfil my goals to the greatest extent. To my sincere heart, he is an actual world-class teacher, and I cannot be more proud to be his student.

I would also like to thank Prof. Akira Matsuzawa for his invaluable guidance, countless pieces of advice, and also the rich knowledge that he shared with me throughout my research.

I would also like to express my thanks to Prof. Atsushi Shirane. He has already taught me not only how to consider circuit design in satellite communication but also the weekly meeting, each seminar, and every presentation helping me find the severe problem and solve them. His advice and opinions about my research are precious. Also, I would like to thank Yoshino Kasuga, Makiko Tsunashima, Ayumi Okubo, Teruki Someya, and Kiyoshi Yanagisawa. They support me in accessing the necessary resources for my life in Tokyo.

I would also like to thank the Ph.D committee members, Prof. Takashi Tokuda, Prof. Jiro Hirokawa, Prof. Hiroyuki Ito, and Prof. Takeo Fujii, for taking their time from their busy schedules to examine my dissertation.

I would give my sincere thanks to my seniors, Yun Wang, Zheng Li, Rui Wu, Ban-

gan Liu, Jian Pang, Anugerah Firdauzi, Zheng Sun, Haosheng Zhang, Yuncheng Zhang, Ibrahim Imad Abdo, Hans Herdian, Junjun Qiu, Hongye Huang, Chun Wang, Dexian Tang, Waleed Madany for their time and support of my research. Without their assistance, I cannot complete my master's degree at Tokyo Tech.

Also, I appreciate my lab mates Dongwon You, Xiaolin Wang, Ashbir Aviat Fadila, Yi Zhang, Sena Kato, Chun Wang, Takeshi Nakamura, Xueting Luo, Rattanan Saengchan, Carrel, Zixin Chen, Qi Li, Xiaofan Gu, Dingxin Xu, Zhongliang Huang, Atsuhiro Kawaguchi, Joshua Alvin, Hiro Tamura, Kota Hatano, Muhammad Amar Maruf, Michihiro Ide for their worthy discussion and academic research on circuit design.

Last but not least, I would like to express my deepest gratitude to my parents, Xiaoqiang Fu and Chaying Xu. They always support me and take care of me when I have trouble. Their endless love and self-sacrifices have made me the person I am today.

Abstract

The dissertation presents a study of millimeter-wave satellite communication systems targeting low power consumption and high link speed by improving the performances of ground base station transmitters and LEO satellite receivers. Designed for future 6G networks with extreme coverage extension, a high link speed transmitter utilizing a mutually coupled inductor based high linearity power amplifier is introduced in this work. The high bandwidth and high modulation efficiency transmitter with high-quality factor 4 path transformer combining and high accuracy output matching power amplifier realized 9.5dBm average output power with 2% EVM in 150MHz 64APSK modulated signal. In terms of the ultra-low-power and high link speed receiver in the LEO satellite terminal, this work utilized mutually coupled inductor to reduce the system power consumption. By implementing the mutually coupled inductor, the input matching value can be reduced and thus, the system can support a smaller common gate input transistor with lower power consumption. The satellite receiver realized 5.5% of the typical power consumption compared with the conventional phased-array receiver.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Nowadays, wireless communication has been involved in high data rate applications for supporting interactive video services, massive connections, virtual reality, augmented reality, etc. However, with the increasing demand for wireless communication speed, the frequency band allocation is becoming more crowded than ever before. The 5G infrastructure deployment in the last couple of years is a sign that there is a new era of communications connected every time. In many countries, such as China, India and Japan, the RF frequency below 6GHz is used for 5G communication systems due to the lower free-space-path-loss (FSPL) and the low-loss antenna for broader coverage. However, these mentioned frequency bands are crowded with many applications, and the limitations for link speed cannot be easily solved.

To address the challenges, millimeter-wave bands (from 30GHz to 300GHz) has been raised great interest in a lot of countries with the applications in 60-GHz WiGig [1–11], 5G New Radio [12–28], and sensing Radar [29–33]. As we all know, the bandwidth is tens to hundreds of times wider than the sub-6GHz frequency bands. Those millimeter-wave bands have been regulated by the 3rd Generation Partnership Project (3GPP). The phased array is an essential technology for the operation of 5G communication transceivers to overcome the higher FSPL in the millimeter-wave applications. Moreover, with the increase of transistor operations frequency, the wavelength is smaller than before, which means the circuit area-efficient is much more than before, and the fabricated cost is much smaller than before. As we all know, the 5G technology is not the final terminal in the evolution of communication systems but the base for future 6G networks. In the following years, there will be a constant evolution to deal with a broader range of applications.

The potential high-speed network for a future communication network is 6G, and it will be introduced in the following several years. The exiting 5G wireless network still has some issues that cannot be solved now, such as increasing link speed requirements.

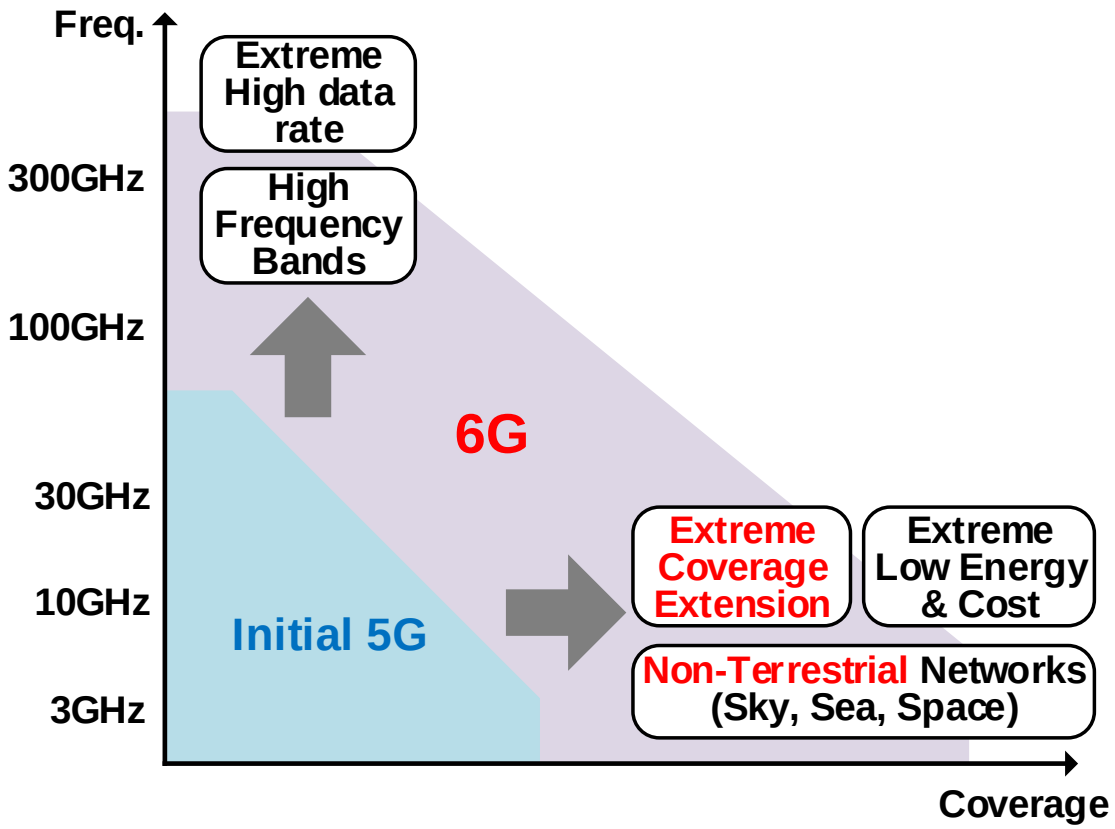


Figure 1.1: The initial 5G and future 6G wireless communication system feature and applications.

As shown in Fig.1.1, the requirements such as the extremely high data rate and extreme coverage extension cannot be solved by the presented 5G performance and need to be increased more in the future 6G network. This figure shows two main features of the future 6G wireless network: the higher link speed and the more comprehensive coverage extension.

In terms of the higher link speed feature, one current vision of future 6G, Fig.1.2 shows the applications which will be more promising in the future. Using an extremely high data rate 6G wireless communication network can solve the current issues. Moreover, light field and wireless displays demand several hundred Gbps communication speeds that cannot be covered by the current 5G wireless communication network. In addition, the requirement of uncompressed video streaming for AR and a massive sensor network for an automotive network still cannot be solved by the current technologies.

Considering extreme more comprehensive coverage extension, in Fig.1.1, the requirements of low cost and low energy per bit communication should also be considered at the

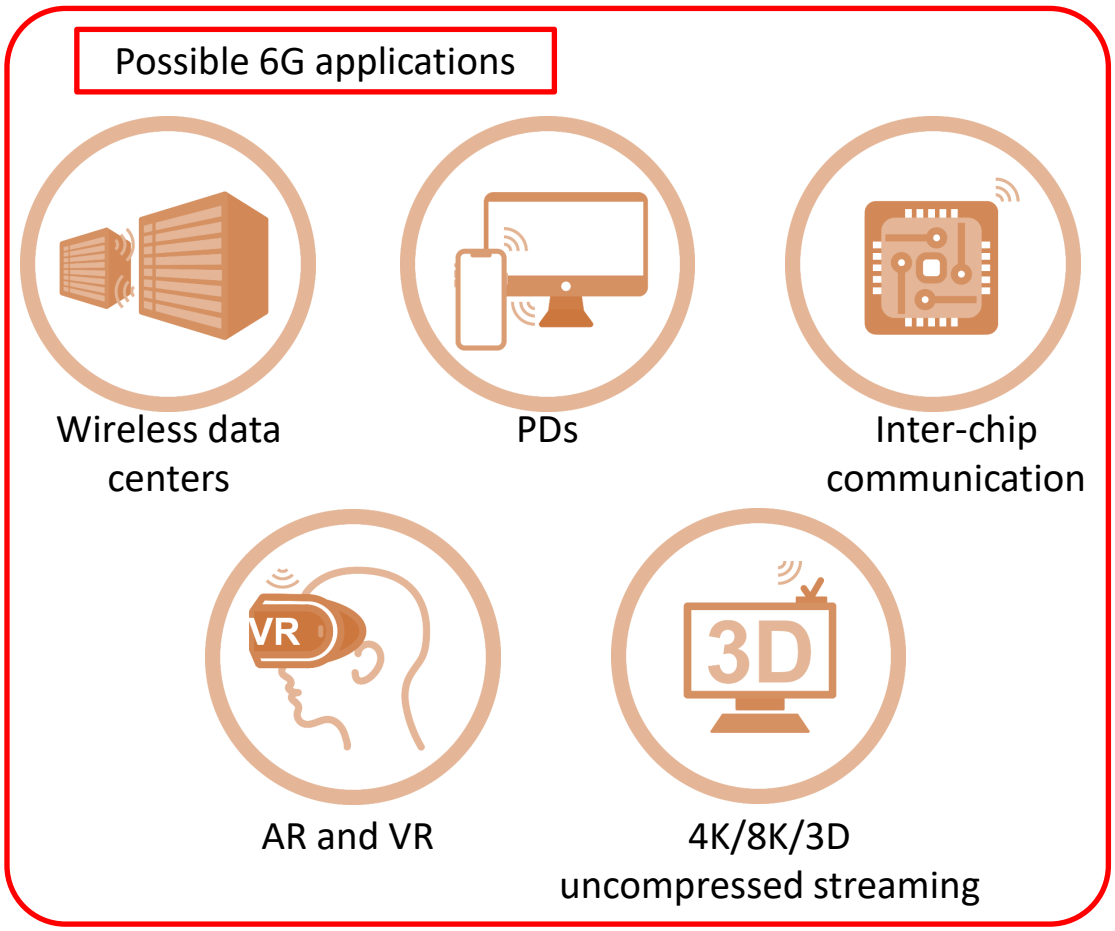


Figure 1.2: The possible future 6G applications with extreme high data rate characteristics.

same time. The reason for that is that the wider coverage extension usually uses satellite wireless networks to provide worldwide network access. The power consumption and operation cost are the key issues in the satellite communication system, and the following contents will discuss the wireless satellite system.

1.1 LEO Satellite Communication System

Many people already have a high-speed network through optical, wired, and wireless connections. No matter which one of them can provide low-latency, high-speed, and huge-capacity networks, as we all know, there are still a considerable number of countries. The town and countryside cannot access those practical and convenient networks limiting

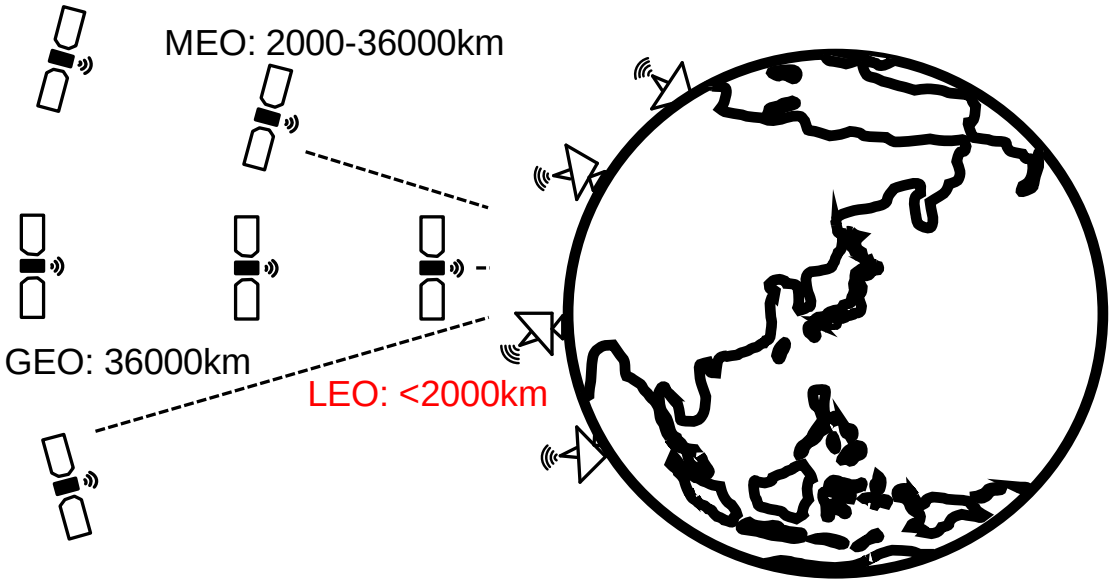


Figure 1.3: One of the possible solutions for wide coverage 6G network: satellite communications with GEO, MEO, and LEO systems.

the development in those places.

The Ka-band for Satcom is about 4GHz. The wider bandwidth will result in higher channel capacity, as can be shown by the well-known Shannon-Hartley theorem:

$$C = BW * \log_2\left(1 + \frac{S}{N}\right) \tag{1.1}$$

where C is the channel capacity in bits per second, B is the bandwidth, and S/N is the signal-to-noise ratio.

A communications satellite can deal with those issues to the greatest extent. It can create a communication channel between a source transmitter, the satellite and a receiver at different locations on Earth. Fig.1.3 shows the orbit of GEO satellite communication. Utilizing satellites to facilitate network connection would bring those advantages:

- *Wide coverage*: Satcom is not sensitive to the ground conditions such as high mountains and wide seas. It is suitable for providing large-scale coverage in areas where people are scarce. Communication can be carried out at any point in the coverage area on Earth [34–39].

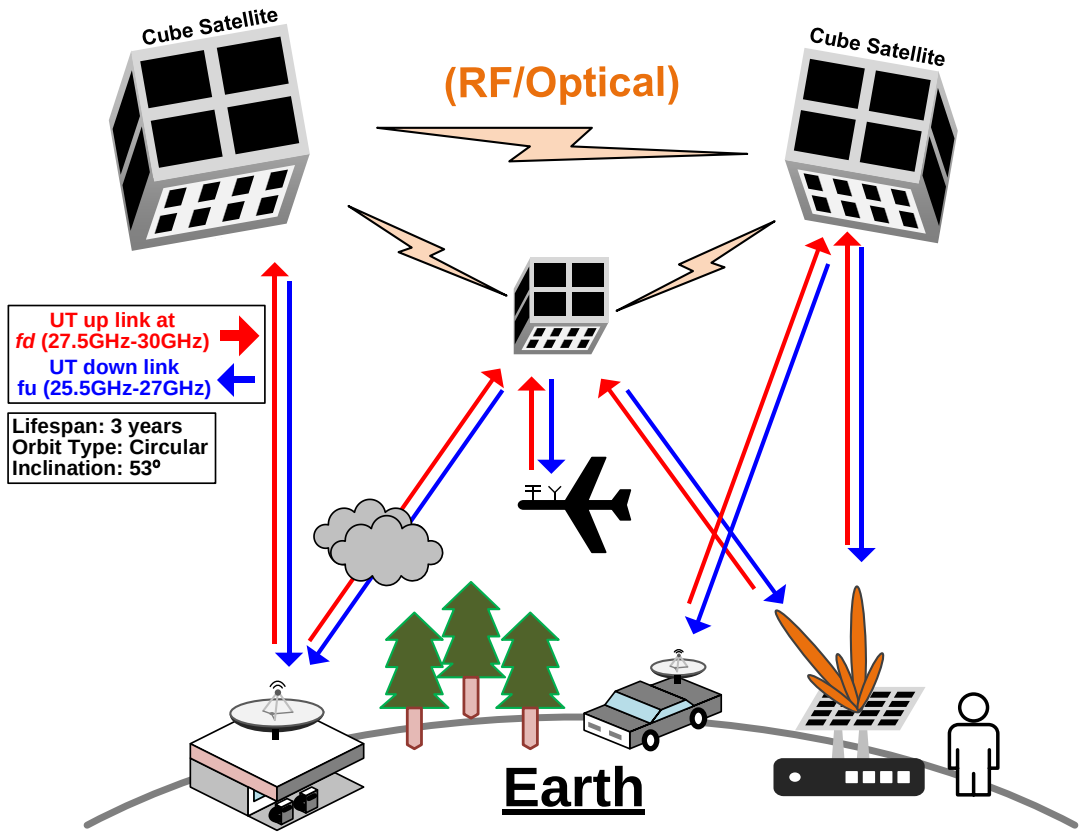


Figure 1.4: A typical application scenario for high-speed low-cost low-latency LEO satellite wireless system.

- *High quality*: Satcom's electromagnetic waves mainly propagate outside the atmosphere, which is very stable for wave propagation. Although there are still some waves in the atmosphere affected by the weather, it is still a highly reliable network communication system.

- *Low cost*: Terrestrial networks can be costly to deploy in some remote regions, and mobile satellite services are still widely viewed as a more affordable communications technology over other existing satellite platforms.

- *Large capacity*: Available frequency bands for Satcom are broad, including microwave with high-speed communication. In general, the bandwidth for Satcom is from 500-800MHz, while simultaneously, Ku bands are from 27-31GHz.

- *Reliability*: In an era of increased communications traffic, maintaining a high level of service reliability is always a key requirement for effective communication

network. Carrier integrated providers need to work with a satellite provider with a reliable network that caters to applications such as remote asset monitoring ensuring reliable, always-on connectivity.

Satellite communication makes use of two kinds of artificial satellites for transmitting the signals. They are passive and active satellites.

- *Passive Satellites*: If we put a hydrogen balloon with a metallic coating over it, up in the air, it technically turns into a passive satellite. This kind of balloon can reflect microwaves signals from one place to the other. Similarly, passive satellites in space are the same. These satellites just reflect the signal back towards the Earth without amplification.

- *Active Satellites*: Active Satellites, contrasting passive satellites, intensify the transmitted signals before re-transmitting it back to Earth. It guarantees exceptional signal strength. Passive satellites were the earliest communication satellite but now about all the new ones are active satellites.

In terms of the satellite communication system, the communications satellites usually have one of three primary types of the orbit:

- *Low Earth orbit (LEO)*: The region of LEO is usually about 1600 to 2,000 kilometers above the earth's surface. As a result of low altitude, the coverage area of those satellites is narrow compared with other high orbit satellites. Consequently, even for the local applications, a large number of satellites are needed for communication.

- *Medium Earth orbit (MEO)*: Those MEO satellite orbits are from 2,000 to 36,000 kilometers above the earth. Its coverage area is larger than the LEO, while the disadvantages of longer time delay and weaker signal propagation.

- *Geostationary orbit (GEO)*: Geostationary satellite has an orbit of 36,000 kilometers above the earth's surface. Because of the "stand-still" characteristic in the sky, ground antennas need not track the satellite motion across the sky. GEO satellite is relatively inexpensive.

Compared with the wireless communication network provided by GEO and MEO satellites, the LEO satellite wireless network can realize high-speed, low-cost, and low-latency global wireless network access [40–42]. One advantage is the low orbit (500km), which provides low FSPL between the ground base station and satellite wireless terminals.

Another reason is the low latency between the user terminal and the satellite terminal, around 20ms in the actual application situation. The launching cost is dominated by the satellite terminal size, flying orbit, and weight of the satellites, and thus the LEO satellite terminal has a very cheap the commercial cost, which is an excellent advantage in the future 6G network and can do well in the expansion for the future 6G network.

Fig.1.4 represents a typical application scenario for a high-speed, low-cost, low-latency LEO satellite wireless system. This figure shows that the uplink frequency band is from 27.5GHz to 30GHz and the downlink frequency band is from 25.5GHz to 27GHz. The typical application scenario utilized cube satellites to provide wireless network access for all applications, such as infrastructures, airplanes, automotive cars, and human beings handed mobile terminals.

The cube satellites have meager launching costs and can easily be implemented in the LEO orbit to provide the network worldwide. The cube satellites can also communicate to provide information about the operation orbit and the control command for each satellite. Also, the cube satellite constellations can help each other realize a latency network between different sides of the earth.

1.2 Overview of This Thesis

As shown in Fig.1.5, this thesis focuses on achieving a high-speed, vast coverage satellite communication network utilizing CMOS technology for low-cost features in the millimeter-wave frequency bands. To increase the system link speed, the millimeter-wave bands are more attractive than the sub-6GHz bands for the wider bandwidth they can provide.

Another critical feature of providing a high-speed network is the higher spectral efficiency. Thus, the high order modulation scheme will be the dominant part in solving this issue and can provide several times more speed than the typical modulation scheme such as FSK, PSK, and QPSK.

A phased array is crucial for providing a more comprehensive network extension with limited power consumption for broader network coverage. The phased array can also help the radiation pattern focus on one point to increase the equivalent isotropic radiated power (EIRP) for higher performance at the system level.

Chapter 2 of the thesis starts the design consideration of the LEO satellite wireless transceiver for the future 6G network. It mainly discusses the background for the future 6G network and the LEO satellite design feature. Chapter 3 includes the Ka-band satellite wireless transmitter for the ground base stations. It includes the measurement results and circuit implementation, such as the power amplifiers, the driver amplifiers, the mixers, and the low pass flitter.

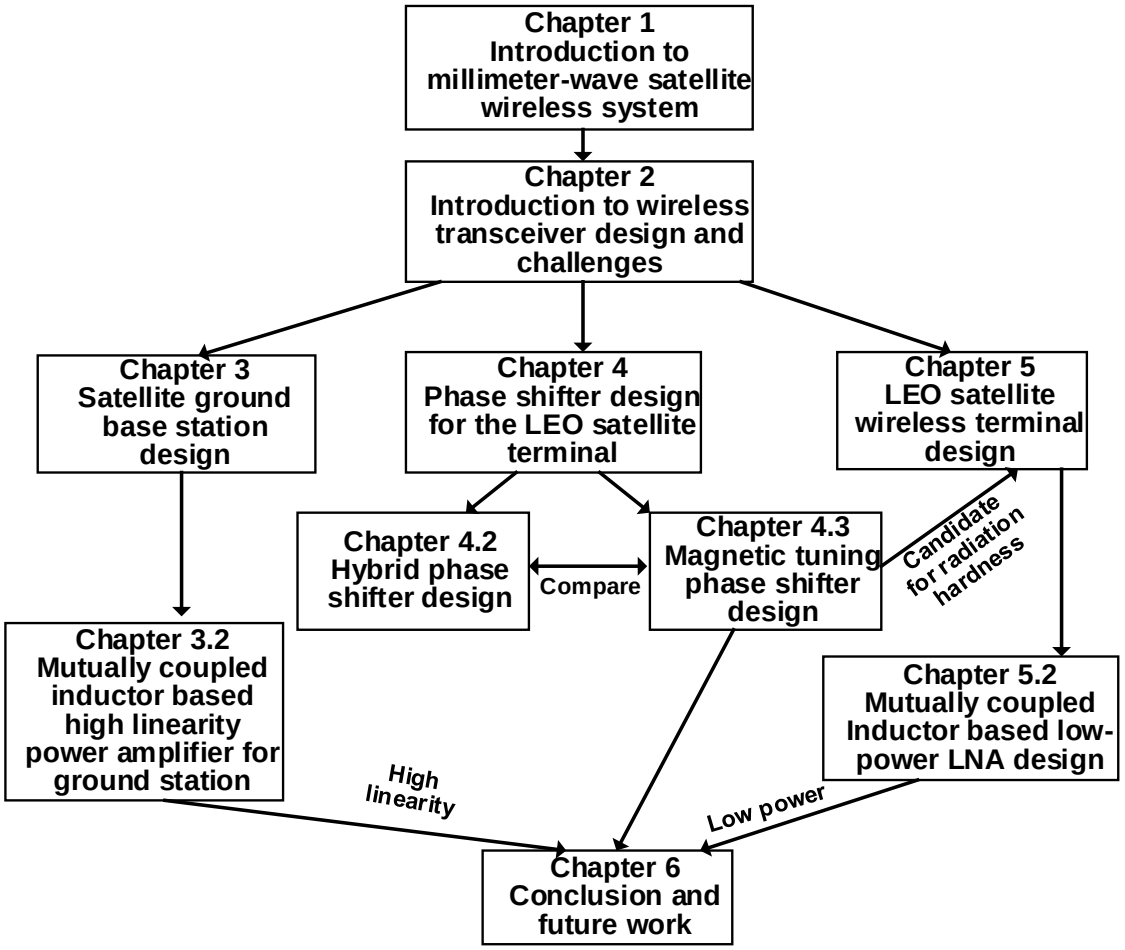


Figure 1.5: The chapter organization and overview of this doctor thesis.

Moreover, Chapter 3 represents the satellite ground base station terminal design, including the high-linearity Ka-band transmitter and power amplifier analysis and design. In Chapter 2.3, the detailed design methodology and analysis are shown for the high-linearity power amplifier.

In addition, Chapter 4 shows the phase shifter design considerations of the LEO satellite communication system. This chapter includes the design of different phase shifters. The Chapter 4.2 shows the design of the vector-summing phase shifter and the hybrid phase shifter (the reflective-type phase shifter and switch-type phase shifter). In the Chapter 4.3, the proposed magnetic-tuning phase shifter is presented and analyzed. The conclusion and the mentioned three-phase shifters are shown in the final section.

Chapter 5 discusses the LEO satellite's satellite terminals (the Ka-band phased-array

receiver). Like in Chapter 3, this chapter also presents the considerations of the satellite terminal receiver, the circuit implementations, and the measurement results of the system. The thesis conclusion and future works are included in the final chapter with an overview discussion.

Chapter 2

Satellite System Considerations and Challenges

2.1 System Design Considerations

There are many limitations for the system design to design a proper satellite transceiver system, such as noise figure (NF), linearity, bandwidth, digital modulation scheme, and system noise temperature. The noise figure, noise temperature, and bandwidth will directly influence the receiver sensitivity at the satellite terminal. The linearity digital modulation scheme will influence the system link speed and the maximum communication distance. The system should be carefully designed and implemented to have good trade between the mentioned parameters.

2.1.1 Noise and Linearity

Noise is one of the biggest challenges in RF system design. It limits the ability to detect minimal signals from very far distances. The thermal noise floor can be calculated as follows [43]:

$$Noise\ Floor = KTB \tag{2.1}$$

where K is Boltzmann constant, T is the temperature in Kelvin, and B is the bandwidth. The wide bandwidth of higher data rate systems causes the noise floor to rise as the total noise power becomes larger.

Several papers represent current noise performance metrics, e.g., noise temperature, input-referred voltage, and current noise, NF, or noise factor (F). Noticeably the NF or F

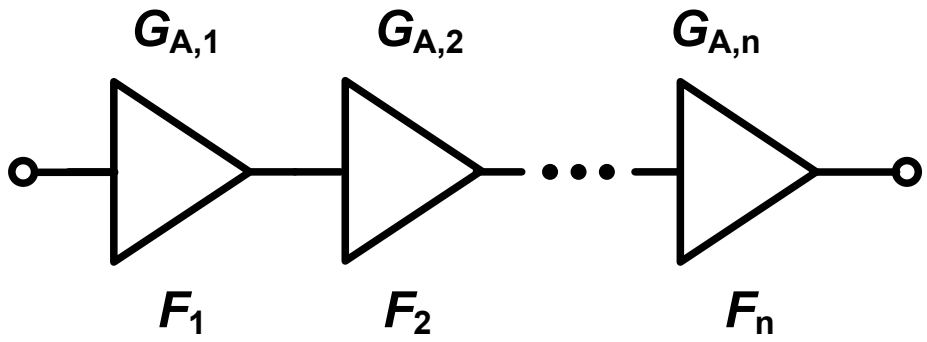


Figure 2.1: Cascaded amplifiers with gain and noise figure.

is the SNR-friendly noise metric. Thus, F can be defined as follows:

$$F = \frac{SNR_{\text{in}}}{SNR_{\text{out}}} \tag{2.2}$$

and at the same time, NF can be defined as:

$$NF[\text{dB}] = 10\log_{10}(F) \tag{2.3}$$

Ideally, this ratio should equal 1. However, every component in the system contributes to the noise causing the NF value to degrade. The NF value is usually expressed in dB.

The total NF of a system that consists of several cascaded stages can be calculated as

$$NF_{\text{total}} = 1 + NF_1 - 1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \cdots \tag{2.4}$$

where NF_j and G_j are the noise figure and gain values of the j^{th} stage. This equation shows that the noise contribution of each stage depends on the gain of the preceding stages [44].

Typically, the first few stages contribute most of the noise, and thus, they are the most critical. However, if there is a loss or attenuation stage, it can amplify the noise contribution of the following stages. Fig.2.1and Fig.2.2 show the cascaded amplifiers with gain and noise figure. Fig.2.2 show the device noise model.

While a linear model for small-signal operation can approximate analog and RF circuits, nonlinearity leads to interesting and important phenomena that the small-signal model cannot predict. There are lots of upper limiting phenomena to restrain the big sig-

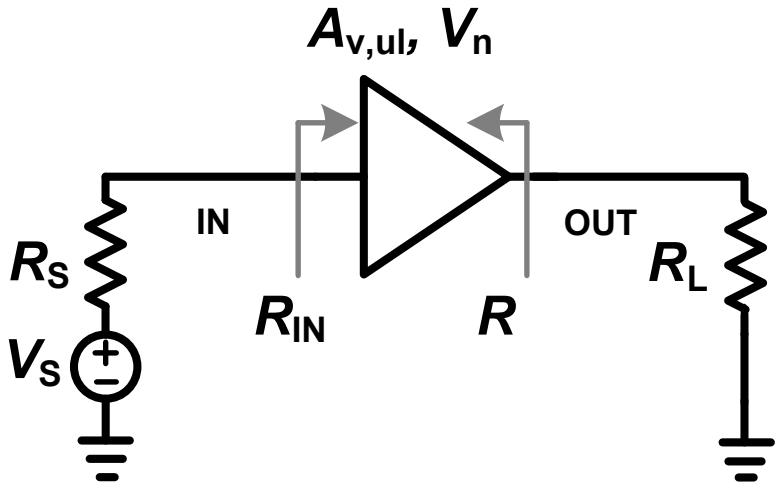


Figure 2.2: Device noise model.

nal. Among all the limitations, mostly, linearity is the most critical part of the transceiver system. It gives rise to numerous gain compression, desensitization, cross modulation, and IMD problems. For a practical transmitter, the output y(t) can be written as a function of the input x(t) as in the equation:

$$y(t) = \alpha_1 + \alpha_2 x(t)^2(t) \ + \alpha_3 x(t)^3(t) \ + \cdots \tag{2.5}$$

For small-signal model operation, the linear part dominates the linear operation. However, the other parts start to affect the output considerably by increasing the input power. In consequence, a single tone cosine signal $x(t) = Acos(\omega t)$ is inserted at the input of the system:

$$y(t) = \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2 x(\omega t) \ + \alpha_3 A^3\cos^3(\omega t) \ + \cdots \tag{2.6}$$

by using trigonometric identities, the output will become:

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) + \cdots \tag{2.7}$$

This result includes several important pieces of information. Firstly, signals at integer multiples of the input signal frequency appear at the output. These signals are called harmonics, and their amplitudes are proportional to the amplitude of the input signal

raised to the corresponding power. When the input frequency is high, these harmonics are very easy to suppress due to the big frequency difference with the desired signal. Secondly, the gain experienced by the input signal is $\alpha_1 + 3\alpha_3 A^2/4$, which means that if $\alpha_1\alpha_3 < 0$, the gain will be compressed at high input signal amplitudes. The point at which the gain is compressed by 1dB compared to the small-signal gain is used to evaluate the linearity of the components of the system and is called the 1dB compression point [45].

A theoretical calculation can be done using the coefficients of to find the value of the 1dB compression point simply by equating the gain to 1dB less than the ideal linear gain α_1

$$A_{1\text{dB}} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.8}$$

When systems send a modulated signal, the signal is frequency-spanned, not a sing tone. It can be thought of as a series of multi tones, which cause inter-modulation. In this time, for the simplest observation, two tones will be input. By substituting the signal $x(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$ into last equation:

$$\begin{aligned} y(t) = {} & \alpha_1(A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)) \\ & +\alpha_2(A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t))^2 \\ & +\alpha_3(A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t))^3 + \cdots \end{aligned} \tag{2.9}$$

can be derived

Again by applying trigonometric identities, a more meaningful form can be obtained. To simplify the analysis, the most important obtained components are analyzed here:

$$\frac{3\alpha_3 A_1^2 A_2}{4}\cos((2\omega_1 - \omega_2)t) + \frac{3\alpha_3 A_1 A_2^2}{4}\cos((2\omega_2 - \omega_1)t) \tag{2.10}$$

They result from the third-order nonlinearity, occurring at frequencies that are not multiples of any input frequencies. Commonly known as the third-order intermodulation (IM3) components, these frequencies are more important than any other IMDs because they are too close to the signal to filter out.

Commonly, for communication systems, the Signal-to-Noise-and-Distortion Ratio (S-NDR) is used to evaluate the IM3 influence on the system. The SNDR is dominated by noise at low input power values. When the input power is high, the SNDR gets dominated by IM3. A critical parameter to evaluate the IM3 effects is the third intercept point (IP3). It is the intersection point between the desired output signal power and the IM3 signal power. The input power at the IP3 is called IIP3, while the output power at that point is called OIP3.

To calculate the IP3, two sinusoidal signals with the same amplitude should be input to the nonlinear amplifier. Then, the amplitude of the IM3 signal can be simplified to $3\alpha_3 A^2/4$. The IIP3 point can be obtained by equating this value to the fundamental signal:

$$|\alpha_1 A_{\text{IIP3}}| = \left|\frac{3}{4}\alpha_3 A_{\text{IIP3}}\right| \tag{2.11}$$

Solving this equation:

$$A_{\text{IIP3}} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.12}$$

Note that the equation is similar to Equ.2.4. And by dividing the two equations:

$$\frac{A_{\text{IIP3}}}{A_{\text{1dB}}} = \sqrt{\frac{4}{0.435}} \approx 9.6\ \text{dB} \tag{2.13}$$

an interesting relation that enables us to use both values freely.

In reality, the value of OIP3 may exceed the supply voltage, and with the influence of the higher-order nonlinearities, the fundamental signal and the IM3 signal intercept at a point quite far from the defined IP3 point. So, extrapolation is used to estimate the IP3 point that matches the definition, as can be observed in Fig.2.3.

In a transceiver system, several stages with different gain and linearity are expected to be connected in a cascade. The overall linearity, represented by the IP3 point, can be estimated as follows:

$$\frac{1}{A^2_{\text{IIP3}}} = \frac{1}{A^2_{\text{IIP3,1}}} + \frac{\alpha_1^2}{A^2_{\text{IIP3,2}}} + \frac{\alpha_1^2\beta_1^2}{A^2_{\text{IIP3,3}}} \tag{2.14}$$

where $A_{IIP3,j}$ is the input amplitude at the IP3 point of the j^thcascaded stage. α_1 and β_1 are the ideal linear gains of the first and second stages, respectively. It can be observed that the linearity of later stages must be higher not to degrade the first stage's linearity. It is because the IP3 of each stage is scaled down by the gain of all the previous stages. Here, the equation (2.10) is always valid for any other nonlinearity component description, i.e., IP3, P1dB, etc [46].

2.1.2 Bandwidth and Link Speed

As mentioned in the introduction, increasing frequency and bandwidth is the basic way to improve the data rate of the transmitter system. At high frequency, the available bandwidth resources will increase because we can utilize 10% of the center frequency. The data rate of a multi-level signaling communication system can be calculated by using

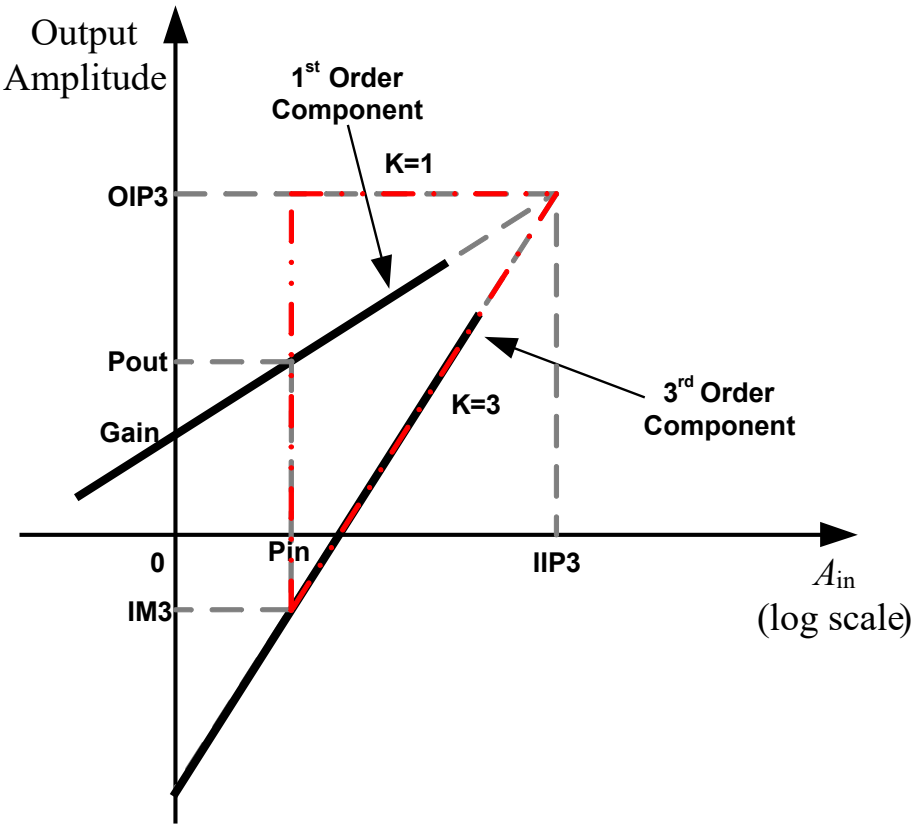


Figure 2.3: Calculation of IP3 by extrapolation.

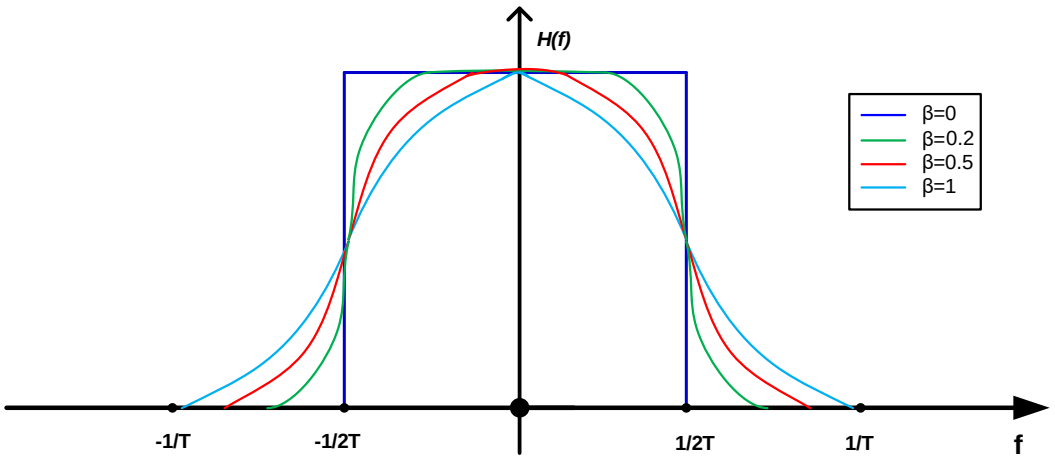


Figure 2.4: Frequency response of raised-cosine filters with various roll-off factors.

Nyquist's formula:

$$C = 2B\log_2(M) \tag{2.15}$$

Where C is the channel capacity in bits per second, B is the baseband signal bandwidth, and M is the number of different symbol values. The value 2B can be replaced by the symbol rate (symbols per second or baud).

However, a high-bandwidth transmitter is difficult for the designer to design due to the limitation of the mixer and power amplification. Infinitely increasing the bandwidth seems impossible. Consequently, we would like to facilitate a shift in the different PA stages to improve the bandwidth, simultaneously, the data rate of our system.

Of course, the frequency spectrum is not rectangular in practice. As a result, raised cosine filtering is used to limit the infinite time-domain characteristics [47]. The kind of filtering results in some excess bandwidth can be represented by the roll-off factor, generally from 0.25 to 0.35. Designers should carefully consider the factor's effect on the system design procedure. Fig.2.4 also represents the frequency response of a raised-cosine filter with various roll-off factors.

2.1.3 Digital Modulation Scheme

Compared to analog modulation, digital modulation has more noise immunity and better compatibility. For this reason, modern wireless communication systems are mainly based on digital modulation. Furthermore, digital data could utilize encryption and error-correcting algorithms before or after the baseband. Our daily products, such as personal

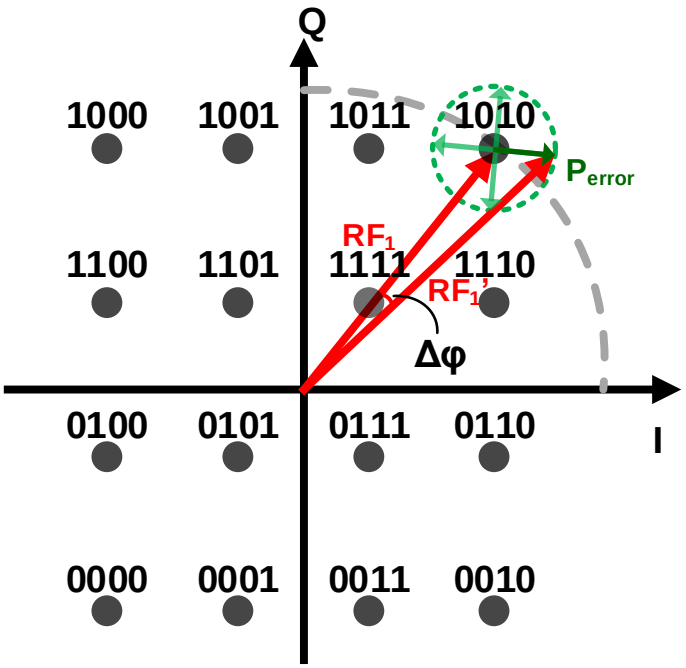


Figure 2.5: The constellation figure of 16-QAM modulated signal and the EVM results in complex plane.

computers, smart mobile phones, tablets, and cars, include those digital data processing center that determines the system performance to a large extent.

Many digital modulation schemes can be utilized for different types of modulation systems. Typically, for simple communication systems such as onboard direct connection, amplitude shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK) will be used for the system communication. The ASK modulation is for the amplitude modulation in analog domains. The FSK is for the frequency modulation domains, and the PSK is for the phase modulation domains.

In terms of an advanced modulation scheme, one symbol can represent several bits (N) with several signal levels (M). This one is called M-array digital modulation. The values of N and M have a relationship in the following equation:

$$N = \log_2(M) \tag{2.16}$$

This thesis will utilize two typical digital modulation schemes for analysis and measurement: the quadrature PSK (QPSK) and M-array quadrature amplitude modulation (M-QAM). The quadrature signal means the signal has 90-degree phase shifting for the

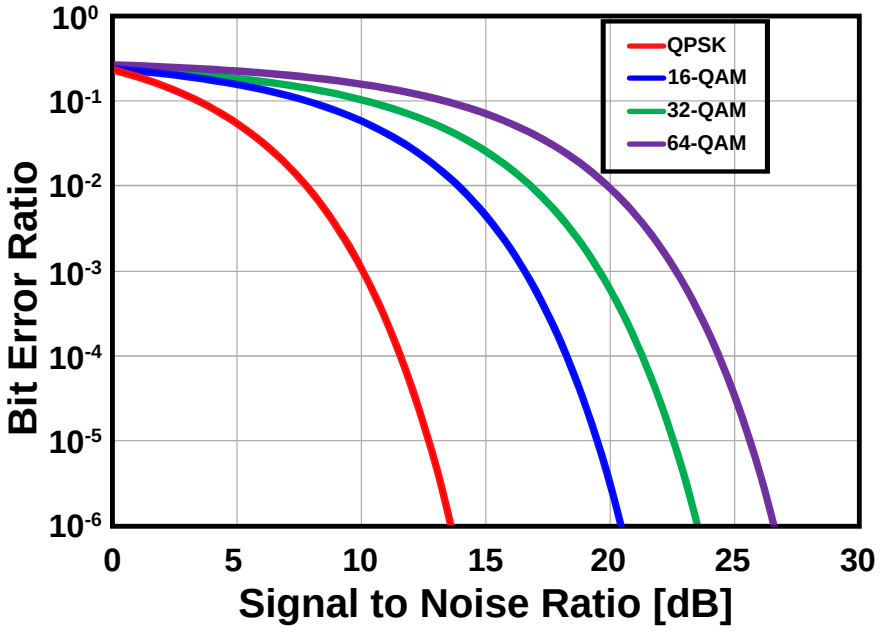


Figure 2.6: BER versus SNR for different digital modulation schemes.

modulated signal in the same carrier frequency. Even if the amplitude level is the same for different signal symbols, the quadrature modulated method can help to distinguish two symbols that have different signal phases. Thus, this method will increase the spectrum efficiency twice compared with the conventional PSK or FSK modulation schemes. QPSK modulation scheme can support 2 bits in one symbol, and the QAM modulation scheme can help with more than 2 bits modulation scenarios with a higher signal-to-noise ratio (SNR).

The QAM modulation scheme can use different amplitudes and phases to form the symbol. The link speed can be increased considerably but keep the same occupying bandwidth. As shown in Fig.2.5, the 16-QAM modulation is composed of 16 constellations with 4 bits of information in one symbol.

Several indicators have been introduced in the past to evaluate the communication system performance. Bit Error Rate (BER) is one of the most common indicators as it shows the ratio between the number of bit errors and the total number of transmitted bits during a time interval. A BER of 10^{-3} is considered acceptable for wireless communication to take place.

To make the BER value more relative to the wireless system design process, BER can be connected directly to the signal-to-noise ratio (SNR). The BER directly relates to SNR that can be derived using probability functions. Fig.2.6 shows the result of that

relationship as a plot with the 10^{-3} point emphasized by the dark grey line. A 9.5dB SNR is required to achieve QPSK wireless communication, while a 16.5dB SNR is required to achieve a 16-QAM link.

Another way that is commonly used to evaluate the digitally modulated wireless link is the error vector magnitude (EVM) [48]. As shown in Fig.2.5, The resulting error vector is normalized to peak signal amplitude and then converted to decibels by using the following formula:

$$EVM(\text{dB}) = 10\log_{10}\left(\frac{P_{\text{error}}}{P_{\text{reference}}}\right) \tag{2.17}$$

Where P_{error} is the average RMS power of the error vector, and $P_{reference}$ is the power of maximum point in the constellation. The EVM can be also represented using the percentage as in:

$$EVM(\%) = \sqrt{\frac{P_{\text{error}}}{P_{\text{reference}}}} \cdot 100\% \tag{2.18}$$

Both formulas are used commonly in the evaluation of the communication system performance.

SNDR is defined as a ratio between signal power and noise power plus distortion power. In digital communication system design, distortion power contains3^rd order intermodulation product (IM3) because IM3 is the hardest nonlinear term to filter out. However, in this work, the design takes account of third order harmonics for nonlinearity effect [49]. SNR is defined again with power as bellow:

$$SNR = 10\log_{10}\frac{S}{N} \tag{2.19}$$

And signal to distortion ratio (SDR):

$$SDR = 10\log_{10}\frac{S}{D} \tag{2.20}$$

Lastly, SNDR is represented as:

$$SNDR = 10\log_{10}\frac{S}{N+D} \tag{2.21}$$

Where D means the sum of harmonics power. And simply, in this work, D will only include 3^{rd} order harmonic power.

By squiring its root mean square value noise at the output of the system can be derived as:

$$N = P_{\text{RS}} + 10\log B + NF + G \tag{2.22}$$

Here, PRS is the available source noise power spectral density at 290K, and it becomes

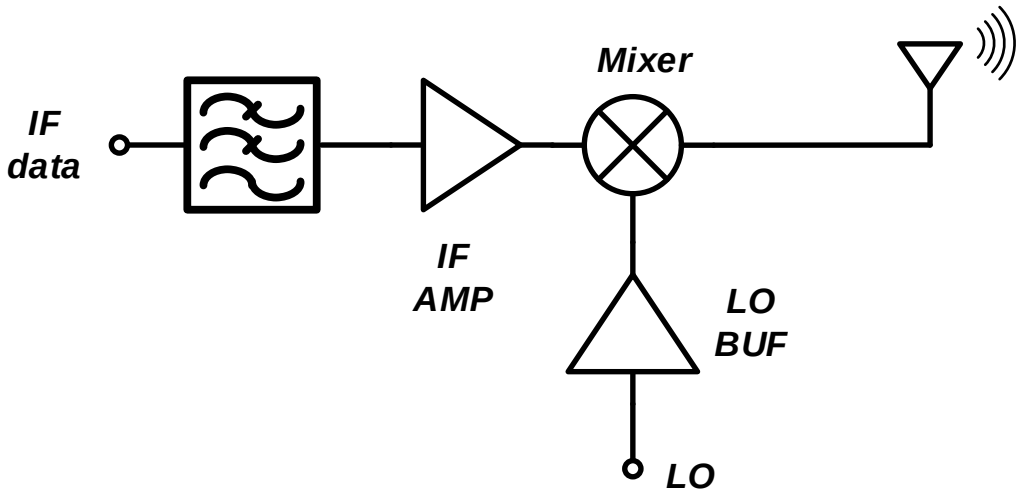


Figure 2.7: Simple block diagram of SATCOM transmitter system.

-174dBm/Hz with matched input of the system to the source resistance. B and NF are system bandwidth and system noise figures, respectively. Fig.2.7 typically show a transmitter system.

2.1.4 Phased-Array and Beamforming

The phased-array system plays a dominant role in the future 6G network communication system, especially in the extreme wider coverage version by the LEO satellite terminals. The difference between the conventional isotropic antenna and the phased-array antenna is shown in Fig.2.8. Considering an ideal conventional isotropic antenna, the radiation pattern for all directions is the same. The radiation pattern will focus on an exact direction with a phased-array antenna with many elements. The other radiation strength in the other direction will not be constant and smaller than the center radiation pattern. The gain difference between the ideal isotropic and phased-array antenna is called the direction gain.

The phased-array antenna with many elements will also help suppress the sidelobe radiation pattern and increase the directivity of the antenna system. More antenna arrays mean a higher radiation pattern in the main direction and a narrower beam in the main direction. The phased-array system is typically realized by implementing different RF signal phases among the different antenna elements. The beam direction can also be controlled by setting phases in different elements.

The Fig.2.9 shows the actual implementation of the phased-array system. The RF

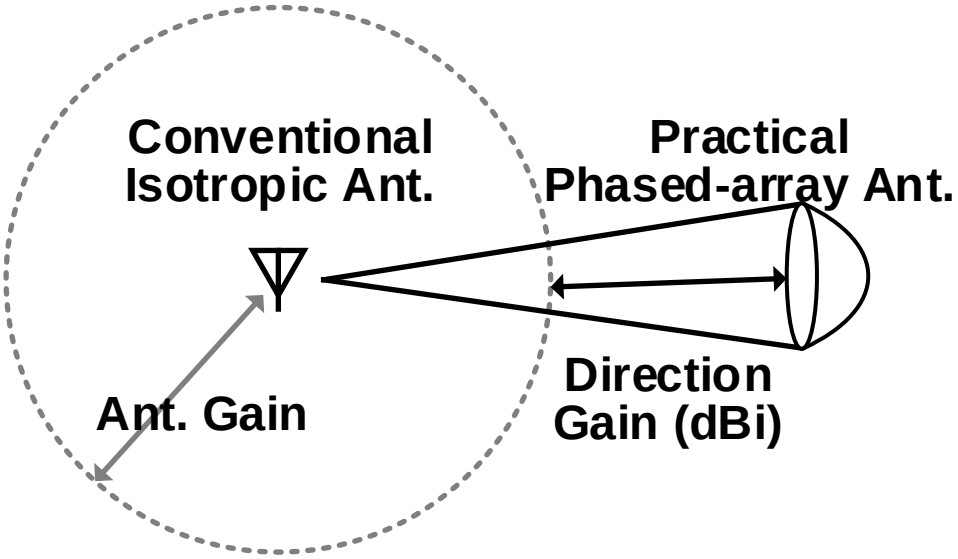


Figure 2.8: The conventional isotropic antenna and practical antenna with direction gain.

radiation signal will be added at the receiver side by implementing different phase-shifting for different elements. For the certain beam angle θ, the phase difference ϕ between different elements can be expressed with the following equation:

$$\phi = K_{\mathrm{f}} d \sin\theta \tag{2.23}$$

Noted that the equation is just for a half-wavelength spaced linear element array. The beam angle will differ for the different distances between the transmitter elements. The K_f is the propagation constant for the frequency f, and it can be calculated with the following equation:

$$K_{\mathrm{f}} = \frac{2\pi}{\lambda} \tag{2.24}$$

Where λ is the wavelength of the carrier frequency. The in-phase amplitude will add the RF signal at the receiver side. Thus the additional antenna gain will be added to the transmitter, which is $20logN_t$ with N element linear array for the transmitter.

In terms of the receiver, a similar thing will happen. Usually, we will utilize many elements on the receiver side to increase the receiver's antenna gain. However, different from the transmitter array, the noise floor will be added on the receiver side, and thus the receiving antenna gain is just $10logN_r$.

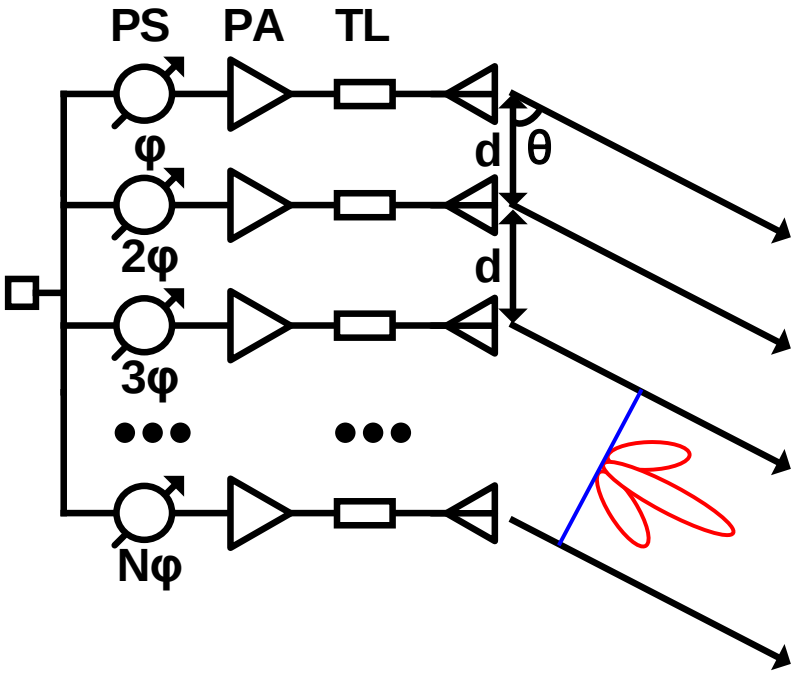


Figure 2.9: A linear array transmitter with a beamforming technique.

2.1.5 Noise Temperature Calculation

The system noise temperature is an essential part of the link budget equation, which is necessary for the design of satellite communication. First of all, the system noise temperature is the sum of all the noises evaluated at the beginning of the satellite receiver. Then it can be recognized as the temperature of a passive resistor producing a noise power density at the input of the receiver circuit.

The system noise itself is defined at the receiver front end. The noise can come from the receiver antenna, the antenna environment, the feeding loss, and the front end. The radio noise from the free space path can be used for the reference noise temperature T_{ref}. When the noise source is coming from active components, the temperature is calculated as noise figure NF or noise factor F, and thus, the reference temperature T_a can be expressed as following:

$$T_{\mathrm{a}} = T_{\mathrm{ref}} * (F - 1) \tag{2.25}$$

and

$$F = 10^{\frac{NF}{10}} \tag{2.26}$$

Where the T_{ref} is a typical value of 290K, which is from the ground earth environment. Usually, the active system will add the noise temperature for the inevitable NF by the transistor circuit.

When the noise source is coming from passive comments, the insertion loss IL will directly add to the noise figure, and thus the passive system noise temperature can be calculated as following:

$$T_{\mathrm{p}} = T_{\mathrm{ref}} * (10^{\frac{IL}{10}} - 1) \tag{2.27}$$

When the noise source is coming from the antenna, the noise temperature is typically divided into the antenna losses and the radio noise. The antenna losses are the degradation values from the feeding line or the antenna absorptive structures. The radio noise comes from natural sources such as galactic noise (3K) or cold sky temperature (20K). So, the total system noise temperature can be written as following:

$$T_{\mathrm{s}} = T_{\mathrm{ant}} + T_{\mathrm{a}} = T_{\mathrm{ant}} + T_{\mathrm{ref}} * (F - 1) \tag{2.28}$$

2.2 System Design Challenges

The future 6G network will utilize the satellite communication system to support extensive network coverage. However, to make it realistic, many challenges should be suppressed by new technology, new design methods, and new materials. The thesis will consider three main challenges in making this satellite communication system realistic.

Firstly, the system power consumption is mainly limited by the available solar panel area, which cannot be very large for a small cube satellite constellation. Secondly, the extremely large FSPL will make the transmitter design difficult because the equivalent isotropic radiated power (EIRP) should be high to support high FSPL. Thirdly, the satellite terminal will be influenced by the sky's cosmic radiation, which will decrease the satellite communication system performance, especially the link speed. In conclusion, the mentioned three main issues should be considered in the realistic system simulation and design.

2.2.1 System Power Consumption

In terms of system power consumption, the essential technique is to reduce the transmitter and receiver power consumption simultaneously. On the one hand, the power consumption is mainly limited by the operation cost for the ground base station, which can be

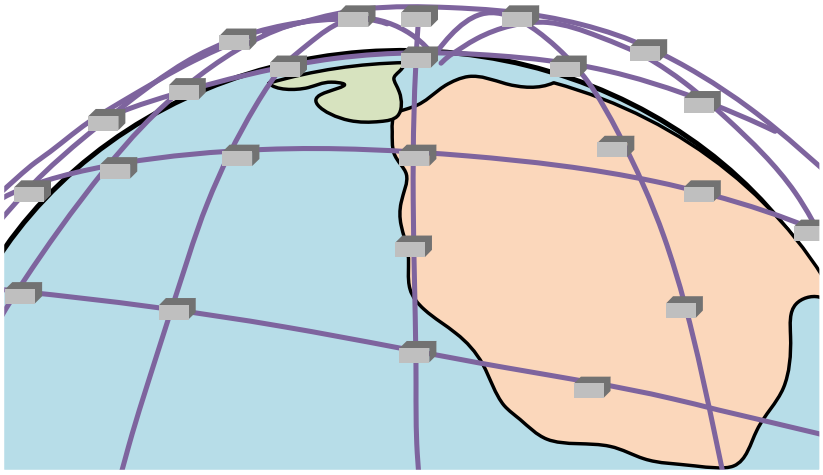


Figure 2.10: The tremendous small satellite constellations supporting the future 6G network for global network coverage.

mitigated in any situation. Thus, in this work, we mainly focus on the design of the receiver terminal, also called the satellite terminal.

On the other hand, as shown in Fig.2.10, there are a considerable number of satellite constellations in the cosmic space to provide network access. One reason is that the LEO satellite terminal can reduce the communication latency but needs more satellites to cover comprehensive coverage. To reduce the launching cost caused by the number of the satellite constellation, the size and mass of a single satellite should be reduced as small as possible to keep the total cost acceptable.

Considering the limited the small satellite solar panel area, the produced average orbit power is also limited. Fig.2.11 shows the trend of average orbit power versus satellite mass for a small satellite constellation. From this figure, we compared the mentioned two values with many small satellite projects such as the Starlink, the Topsat, the Asit-1, the Tubsat B, the Dove-s, and the SOMP. We can quickly figure out there is a clear trend that the smaller satellites are becoming more and more popular for future 6G networks. Thus, our goal is to make the cube satellite (<3kg) realistic in the future.

Fig.2.12 illustrates a typical implementation of small cube satellite. The upper side is the phased-array antenna. One is for the satellite transmitter, and another is for the satellite receiver. This work will focus on the receiver part only to make the story simple. The high efficient solar panel area covers the surrounding area. Even though all the surround is covered, the available solar panel area is around 100cm^2. To calculate the available

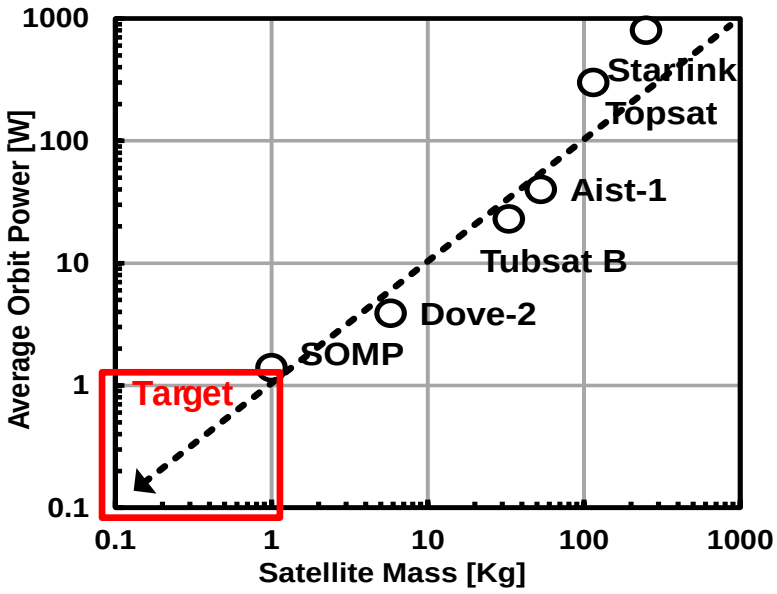


Figure 2.11: The trend of available average orbit power versus satellite mass for small cube satellites.

average orbit power, we should consider the satellite's angle, the time operated at the backside of the sun, the power loss in the battery, and the efficiency of the solar panel material.

In this work, the available orbit power is targeted at 3W. Thus the power consumption required for each element should be lower than 4mW for 256 antenna arrays (1W for Rx, 2W for Tx). However, the typical receiver power consumption is around 60mW, which is such a high value. We need to think of a new design method and system architecture to satisfy the mentioned requirement.

2.2.2 System Free Space Path Loss

When the high-frequency electromagnetic wave propagates through space, it suffers many losses due to many effects such as free space path loss, refraction, diffraction, reflection, and absorption. Assuming an RF signal in line-of-sight short-range transmission, the path loss is dominated by the free space path loss. The free space path loss calculation is based on the equation that the electromagnetic wave propagates in all directions, which satisfies the inverse-square law. When the antenna gain is equal to 1, and then the FSPL can be represented as following:

$$FSPL = \left(\frac{4\pi d}{\lambda}\right)^2 \tag{2.29}$$

Figure 2.12: The limitation of power consumption caused by the satellite mass and solar panel area.

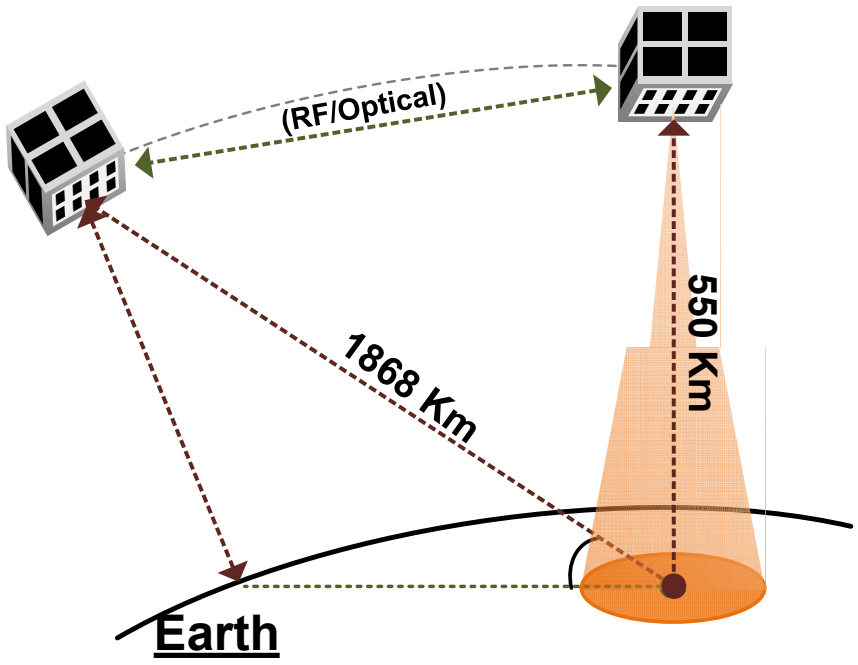


Figure 2.13: The satellite communication system FSPL with the communication distance.

Where the d and λ, and f are the communication distance and RF signal wavelength. With the increasing frequency, the FSPL will continue rapid growth in the millimeter-wave spectrum, promising frequency bands with broader bandwidth for the future 6G network. The equation also shows that the FSPL is proportional to the square of communication distance. In satellite communication systems, the higher distance with higher FSPL should also be considered in detail for analysis and design. As shown in Fig.2.13, the FSPL for 29GHz at 550km communication distance is 176dB.

According to the mentioned equation, the higher frequency induces higher FSPL. Let us analyze the reason here. Considering the antenna design and size. It is well-known that at millimeter-wave frequency bands (shorter wavelengths), the unity gain is realized with a smaller antenna area. Assuming the smaller antenna for the higher frequency at the receiver side. Then the tiny antenna will capture less power, and thus, the FSPL will increase with the higher frequency.

To solve the mentioned high FSPL issue, a high gain with a high directivity antenna is necessary. As we all know, antenna gain measures the antenna's electrical efficiency and directivity. It is usually defined as the ratio of the power produced by the antenna to the power produced by a lossless isotropic antenna and expressed in dBi. The existence of directivity reduces the path loss, and we can quickly figure out the value from the Friis

transmission equation:

$$\frac{P_{\mathrm{r}}}{P_{\mathrm{t}}} = G_{\mathrm{t}}G_{\mathrm{r}} * FSPL = G_{\mathrm{t}}G_{\mathrm{r}} * \left(\frac{\lambda}{4\pi d}\right)^2 \tag{2.30}$$

The value $\frac{P_{\mathrm{r}}}{P_{\mathrm{t}}}$ is the ratio between the input power of the receiving antenna to the output power of the transmitting antenna. The G_{t} is the antenna gain of the transmitter, and G_{r} is the receiver's antenna gain. Bu using a high directivity antenna on both the transmitter and receiver side, the issue caused by high FSPL can be solved.

2.2.3 Circuit Radiation Hardness

In the conventional geostationary communication satellites, a parabolic antenna is utilized, and a transceiver module is placed inside a metallic cavity so it can tolerate cosmic radiation. On the other hand, LEO satellites need beam-steering functionality by using a phased-array antenna. Only a thin shield layer can be inserted between antennas and ICs to avoid redundant mass and insertion loss. Thus, radiation-hardening is the critical requirement for such cube satellite phased arrays. For RF building blocks in a phased array, the total ionizing dose (TID) is more critical than the single event effects (SEE).

Fig.2.14 shows an estimated result for non-radiation-hardened design regarding TID degradation on beam pattern for 256 element phased-array transceiver, resulting in 3.8dB main-lobe degradation. Moreover, the TID influences the main lobe value of the beam pattern in amplitude value and influences the sidelobe value of the beam pattern.

As shown in Fig.2.15, in the conventional application such as the national space station and the large size satellite, the way to realize high radiation hardness is to protect the IC chip inside the body of the satellite as much as possible. Usually, some satellite sides will be utilized for the solar panel area, especially for cube satellites.

The remaining sides can be used for parabolic antennas. Some antennas should focus on the earth ground station to provide broad coverage network access. Other antennas will be set in the direction of other small satellites to provide the inter-satellite communication link with a high-frequency RF signal. Both antennas hide their front ends inside the satellite body for radiation hardness consideration.

Fig.2.16 represents the consideration of radiation hardness for a phased-array antenna but with a long-distance RF feeding line. As we all know, the LEO satellite communication system needs the beam-steering function to provide fast beam sweeping among different ground base stations. The phased-array antenna cannot be hidden inside the satellite body for higher radiation hardness performance. Thus, the thick shield layer can be inserted between phased-array antennas and ICs to avoid high radiation.

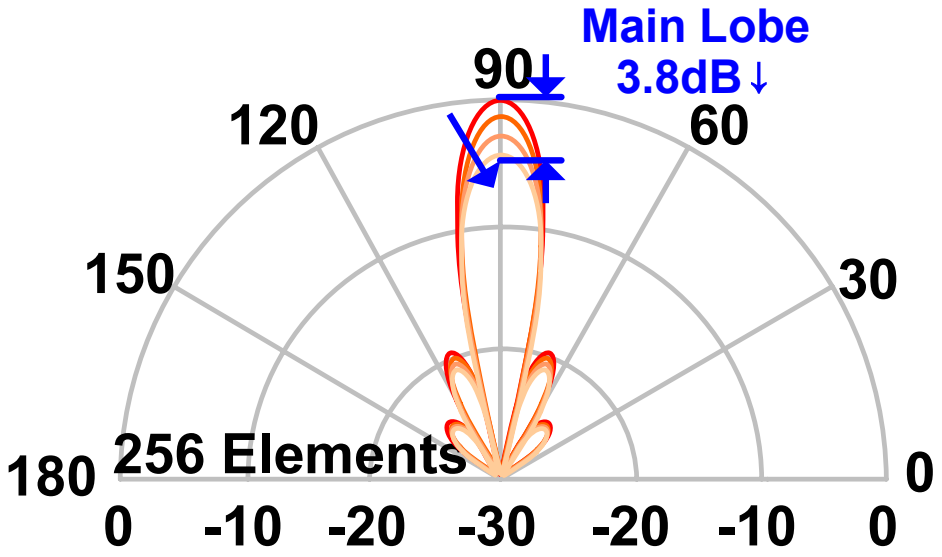


Figure 2.14: Estimated result for non-radiation-hardened design regarding TID degradation on the main beam pattern.

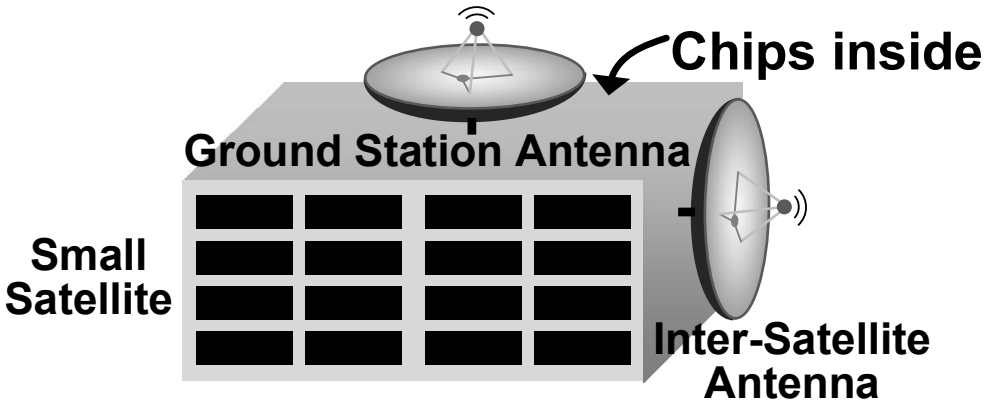


Figure 2.15: The conventional radiation hardness technique with a high mass parabolic antenna with chips inside the metallic cavity.

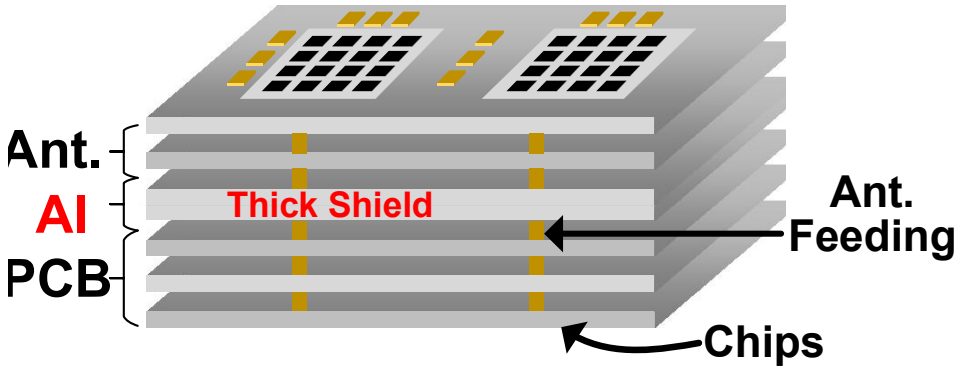


Figure 2.16: The considerations of radiation hardness for the phased-array antenna but with long-distance RF feeding lines.

However, with the increasing insertion loss and cost of manufacturing brought by the thick shield layer, it is impossible to have an excellent receiver performance with the limitation of small power consumption. Thus, with the limitation mentioned before, the chips with radiation hardness inside themselves will be a possible solution with all the limitations shown before.

This work introduces a thin phased-array antenna PCB with TID tolerance ICs under the PCB for radiation hardness consideration. As shown in Fig.2.17, The realistic example of phased-array antenna implementation with TID tolerance CMOS chip is made by Megtron-6 material, which has a low loss for millimeter-wave frequency bands.

The TID from the cosmic space will pass the Megtron-6 PCB with an equivalent thin shield layer. The electronic antenna ground can work as a standard shield for radiation hardness consideration. The remaining TID will continue passing the antenna PCB and accumulate inside the CMOS chip, which means the CMOS chip should be radiation tolerant itself.

To illustrate the actual TID value on the CMOS chip for a radiation hardness consideration, this module with a copper shield layer is simulated to represent the system performance. Considering the satellite environment of 3-year lifespan, 550km orbit altitude, circular orbit type, and 53-degree inclination angle, The simulated TID results are shown in Fig.2.18.

According to Fig.2.18, for a 24um copper shield, the TID to the CMOS chip is about 2.7Mrad. This work's CMOS chip TID tolerance should be more significant than 2.7Mrad with acceptable performance tolerance. Compared with the 3.3Mrad result without any copper shield, the TID immunity from the thin copper PCB shield layer is only 0.6M-

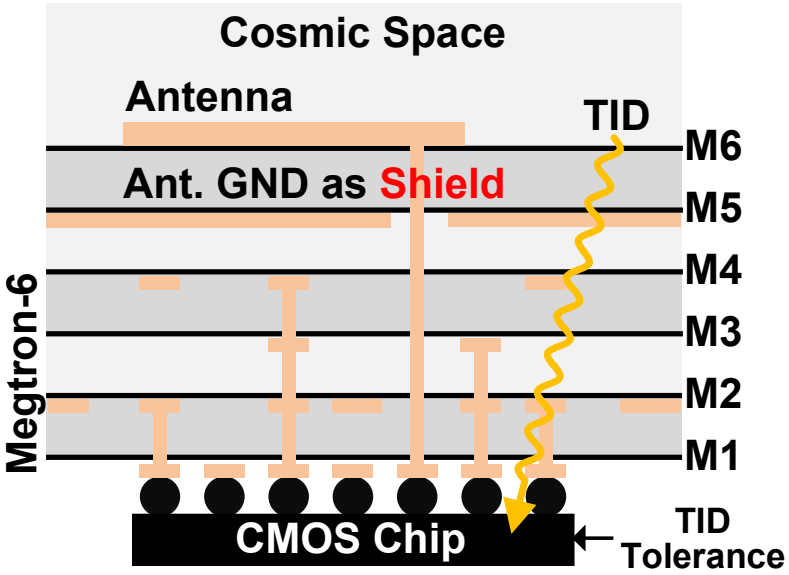


Figure 2.17: A realistic example of phased-array antenna implementation with TID tolerance CMOS chip inside the satellite body.

rad. The blue area in this figure represents the typical PCB shield thickness in a realistic situation.

2.3 Satellite Transceiver Architecture

The design considerations such as noise, linearity, bandwidth, link speed, digital modulation scheme, phased-array antenna, and noise temperature calculation have been mentioned before. Moreover, the system design challenges such as limited power consumption, high free space path loss, and necessary radiation hardness have also been discussed.

This section will focus on the system design requirements such as noise figure, IIP3, gain flatness, link speed, and EVM. Besides, the system architecture, including the ground station transmitter and satellite receiver terminal, will be represented, and a rough analysis will also be included in this section.

2.3.1 Communication Link Budget

As shown in Fig.2.19, in this work, compared with conventional satellite communication networks, the Ka-band with higher available bandwidth is utilized in this satellite

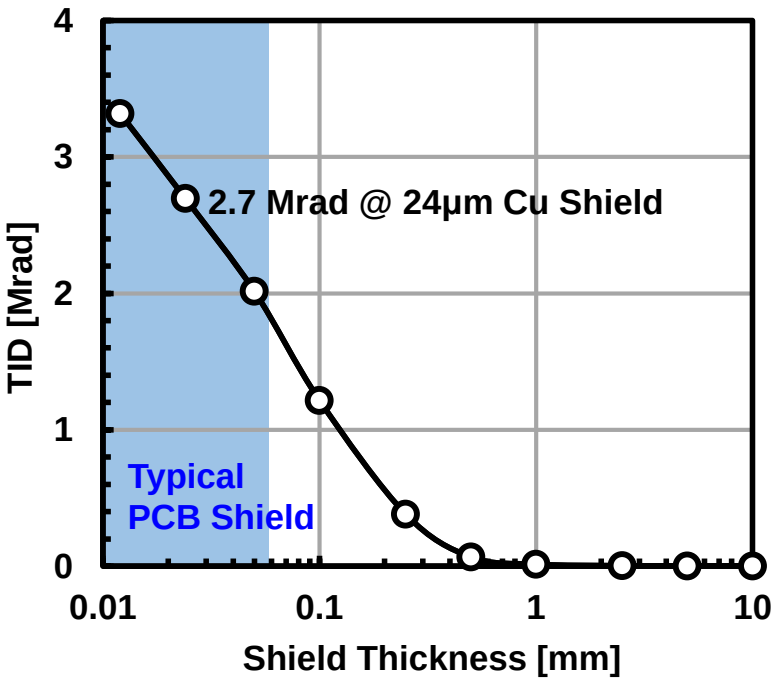


Figure 2.18: The simulated TID results versus the copper shield thickness in the phased-array antenna PCB.

transceiver. The higher operation bandwidth induces a higher link speed for all ground base station terminals.

The satellite orbit is an LEO orbit with a 500km altitude and 53-degree inclination angle, which has low latency, but high FSPL communication features [50, 51]. The satellite flight velocity is around 7.5km/s and the satellite pass time is only 4.1 minutes. Thus, the phased array is necessary for the beam control to support many ground station terminals simultaneously.

The communication distance is also different, ranging from 500km to 1123km for different view angles. According the equation mentioned in Equ.2.29, the minimum and maximum FSPL is -183dB and -176dB for 29GHz carrier frequency. In terms of the link budget calculation, we usually use the following equation for estimation:

$$EIRP = \left(\frac{E_s}{N_0}\right) + FSPL - \frac{G}{T} + 10\log_{10}(R_s) + 10\log_{10}(k) + Margin \tag{2.31}$$

Where the $\left(\frac{E_s}{N_0}\right)$, FSPL, G/T, R_S, and k is the receiver acceptable demodulated signal to noise ratio, the system free space path loss, the receiver antenna gain to system noise temperature, the communication baud rate, and the Boltzmann constant.

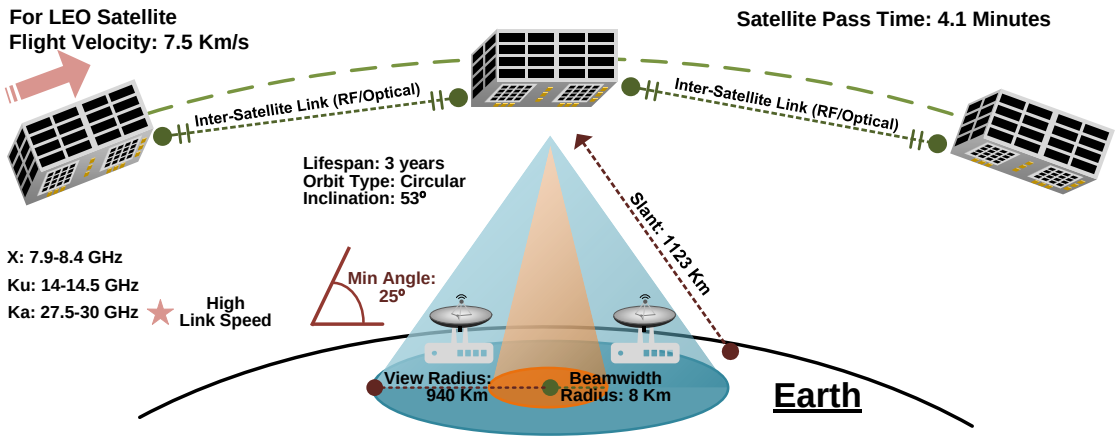


Figure 2.19: The satellite orbit information and the communication distance for the link budge calculation.

This subsection will analyze the equation's variables more practically by introducing estimated numerical values to evaluate the link budget for the SATCOM system. As the value mentioned in previous sections, this thesis chooses the 290k earth temperature, a 500km altitude LEO for satellite orbit, and the Ka-Band spectrum for the SATCOM link budget analysis. It is also necessary to choose the center frequency of 29GHz and the frequency bandwidth 200MHz inside the Ka-Band, which will be used.

According Equ.2.29, the decibel value of FSPL can be written as following equation:

$$FSPL = 20\log_{10}\left(\frac{c}{4\pi}\right) - 20\log_{10}(d) - 20\log_{10}(f) \tag{2.32}$$

Where c is the speed of light in a vacuum and d is the communication distance between the ground station and satellite terminals. This work d equals 500km to 1123km, accounting for estimated elevation and azimuth angle.

Fig2.20, represents the calculation value of the link budget, to support 200MHz baud rate 256APSK modulated signal, the receiver $\left(\frac{E_s}{N_0}\right)$ should be larger than 19dB. Considering the receiver G/T value is limited by the phased-array antenna gain of 24dBi, the transmitter EIRP should be larger than 66dBW with a high-performance parabolic antenna. Thus one necessary external power amplifier is necessary in this work for driving the high-performance parabolic antenna. The parabolic antenna should have 45dB gain and the power amplifier should have a 25dBW output saturated power with 40dB power gain.

Parameters	Values	Comments
Pout	12dBm	Transmitter average output power
EIRP	66dBW	Effective Isotropic Radiated Power
FSPL	-183dB	The worst case free space path loss
RL	-11dB	Rain Loss
k(dB)	229dB	Boltzmann constant
G/T	2dB	Receiver gain to system noise temperature
C/N	103dBHz	Carrier to noise ratio
Rs(dB)	-83dB	the baud rate
Margin	1dB	System margin
E/N	19dB	Normalized signal-to-noise ratio

Table 2.1: The summary of the calculated link budget for future satellite communication network.

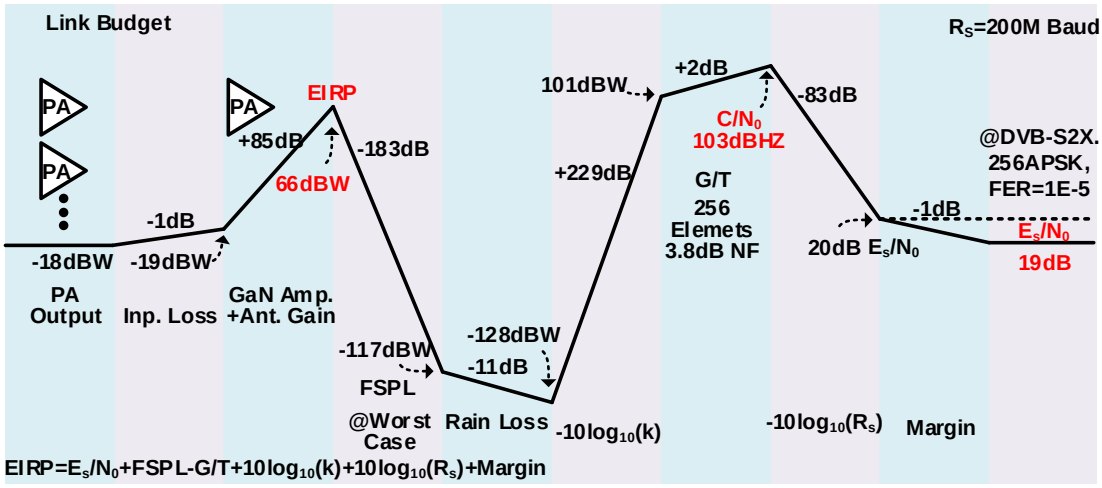


Figure 2.20: The detailed information of the satellite communication system link budget: including the EIRP and the receiver E_sN_0.

2.3.2 Transmitter and Receiver Architectures

The satellite communication system for the future 6G network is mainly composed of two-part: the ground base station part and the cube satellite terminal. The ground base station is for sending the RF signal to the cube satellite, and the satellite terminal will serve as a transponder or a receiver.

Fig.2.21 shows detailed architectures for the system. The uplink center frequency is 29GHz, and the downlink center frequency is 26.5GHz. In this work, we will mainly focus on the uplink due to the limited length of this thesis paper.

The I and Q signal first passes the low pass filter to eliminate the high-frequency spur at the ground base station. Then, the signal gets into the double-balanced mixer for upconverting the baseband signal to 29GHz. One stage adder and one stage driver amplifier are included in the RF signal chain to drive the power amplifier fully.

Then, the RF signal passes the power amplifier, which increases the average amplitude of the RF signal to 12dBm, which supports the 256APSK modulated signal. The output power is added inside a four-way combiner which makes the output matching difficult. The RF signal is injected into a parabolic antenna for higher EIRP to increase the communication distance with high FPSL. The parabolic antenna can also change its beam direction by auto-machine. After that, the high-frequency modulated signal is propagated in the sky and goes inside the small cube satellite.

In terms of the small cube satellite terminal side, the 29GHz modulated signal is received by the phased-array antenna. In this work, the total number of phased-array ele-

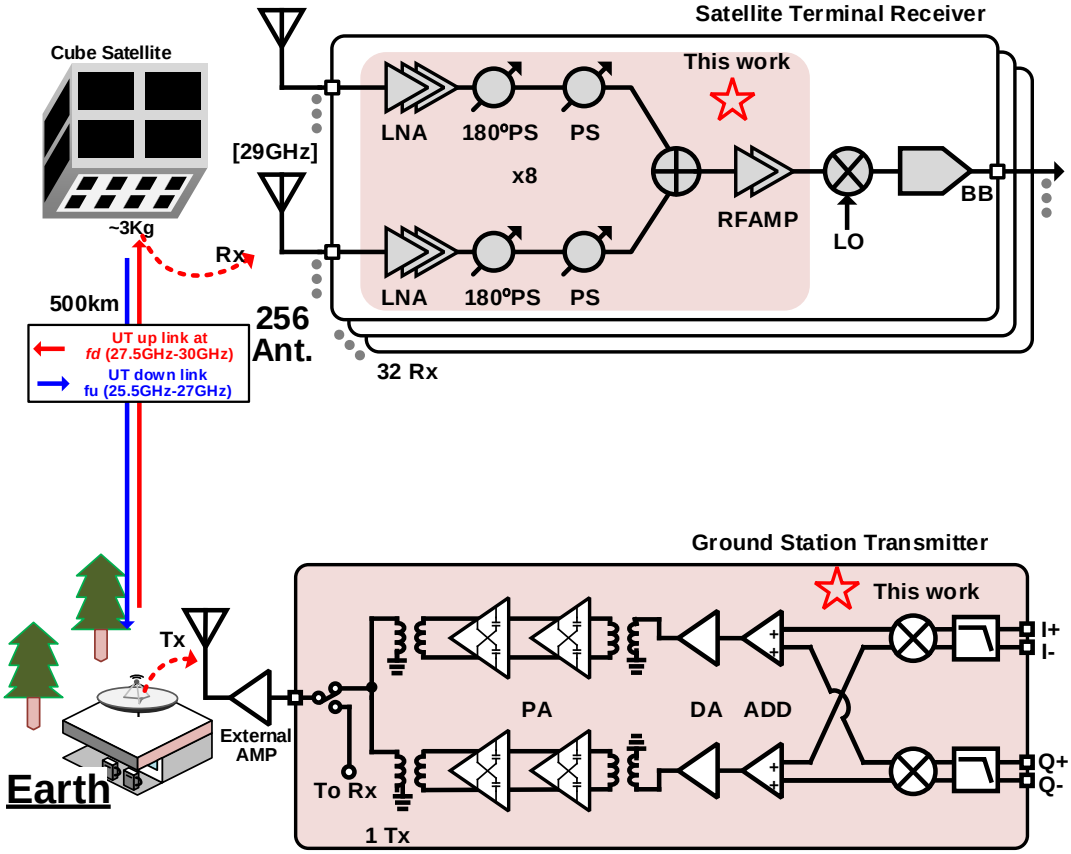


Figure 2.21: The transmitter and receiver architecture for the satellite communication system.

Ground Station Term.	Requirement (Tx)	Satellite Term.	Requirement (Rx)
Psat	>18dBm	NF	<5dB
Temperature	-	Temperature	-40°C - 125°C
Power Consumption	<2W	Power Consumption	<4mW/Element
TX ACPR@2%EVM	>30dB	Size	<3000cm^3
Link-speed: >1Gbps			

Figure 2.22: The transmitter and receiver specification for the satellite communication system.

ments is 256, and thus, the receiver antenna gain is 24dBi. The input of LNA is connected with the patch antenna by a feeding line in the PCB. One element front-end includes a multi-coupling balun-based LNA, a 180-degree phase shifter, and a magnetic tuning phase shifter.

The front-end amplifies the RF signal, and then the 256 paths RF signal is combined at the output of the combiner. Then, the RF signal is amplified at the integrated RFAMP to mitigate the chain path loss influence. The receiver architecture is a conventional heterodyne receiver with only one local oscillator for signal mixing. The signal is converted to a digital signal and processed by DSP or CPU in the final step.

As shown in Fig.2.22, the requirements for the satellite ground station terminal are mainly for the high-linearity. For example, the saturated power for CMOS power amplifier should be large than 18dBm for driving the external GaN amplifier. High ACPR also shows the transmitter has high linearity. In terms of the requirements of the satellite terminals, the most dominant parts are the noise figure and power consumption which should be lower than 5dB for system and 4mW for each RF element.

Chapter 3

Direct Conversion Transmitter for Ground Base Station

This chapter discussed the direct conversion transmitter for the ground base station terminal. The system consideration of the satellite base station terminal is discussed first, including the power amplifier design and operation classes. Secondly, the doubled-balanced mixer and LO structure are introduced and discussed. The measurement results of the proposed transmitter for the satellite ground station terminal is presented and compared with state-of-the-art millimeter-wave transmitter in literature for satellite and 5G application. Finally, a brief conclusion is presented.

3.1 System Structure of Transmitter

As shown in Fig.3.1, the proposed satellite transmitter is based on the direct-conversion (also called zero-IF) transmitter. Firstly, the input I plus, I minus, Q plus, and Q minus signals are flittered by a low pass flitter to avoid the high-frequency spur and high-frequency harmonics induced by the DACs.

Next, the baseband signals pass a double-balanced mixer for upconverting RF signals. A poly-phase shifter generates the LO with 0-degree and 90-degree phase RF output signals. Then, the RF signal is added to the output of the driver amplifier, which is the critical component for driving the power amplifier.

The single-ended RF signal is divided into the differential signal by two high-quality factor balun, following with the input stage of the main power amplifier. The main power amplifier is based on a 4-way power combiner for high linearity features. The measured-based transmission line and capacitors are added at the end of the balun output for matching blocks to make the optimized matching at the output point.

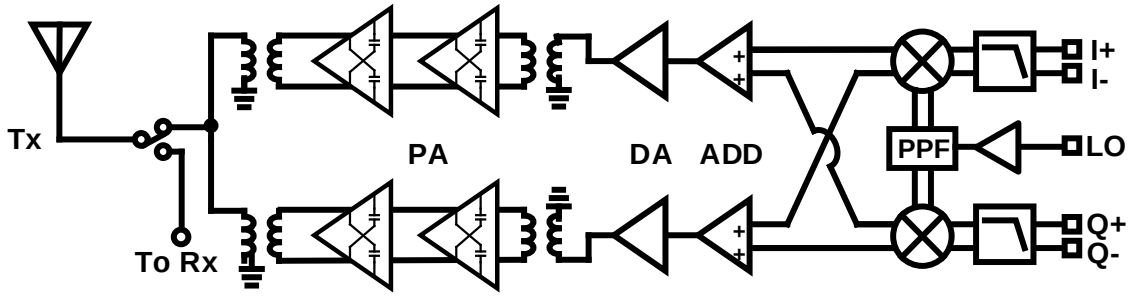


Figure 3.1: The detailed direct-conversion transmitter for the future 6G satellite communication system.

3.2 Mutually Coupled Inductor Based Power Amplifier Design

3.2.1 PA Design Consideration

PA dominates the transmitter performance in the SATCOM system, especially the communication distance, emission power, system PVT-tolerant, and even the bandwidth. As a result, the chapter will discuss the consideration of PA in operation classes, architecture, and topology. The measurement results of the proposed power amplifier are also briefly presented in the chapter.

As shown in Fig.3.2, a typical power amplifier is constructed by three-part: input matching block, core amplify transistors and output matching block. The input matching block transforms the gate capacitor impedance to 50 Ohm. Output matching block transforms the 50 Ohm real impedance to the complex conjugate value of the transistor output impedance.

To increase the output power and voltage swing, the designer would usually like to duplicate the transistors or improve their sizes. However, with the transistor size increasing, the parasitic capacitance simultaneously increases, and the operation frequency drops due to significant parasitic parameters [52]. Therefore, the transistor size needs to be optimized, namely, the trade-off between the output power, gain, and operation point. For bias circuits, they are still critical for power amplification.

The matching blocks transform the source or load impedance to the desired impedance extracted from the power transistor. The ideal LC or transmission line matching is lossless; however, the matching block typically introduces 1-dB insertion loss due to the low-

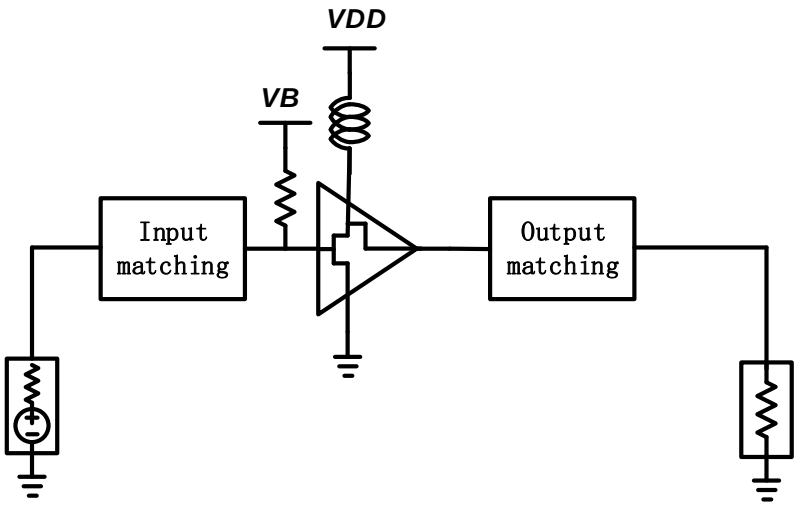


Figure 3.2: Typical power amplifies structure with detailed bias conditions and input-output matching.

quality factor at high frequency. The power amplifier matching network prefers power matching the gain matching.

The maximum gain impedance matching delivers the highest gain. When the amplifier is operating in a low-signal mode, it is encouraged to increase the gain in the design regardless of the amplifier linearity. However, when the amplifier is operating in a large-signal mode, the matching blocks have a significant influence on the linear region.

Usually, the gain and power matching are not with the same impedance. It makes a trade-off between the amplifier gain and linearity [53]. Fig.3.3 shows the typical relationship of the amplifier power matching and gain matching.

Fig.3.4 and Tab. 3.1 shows the power amplifier operation class versus the conduction angle [54]. The power amplifier's maximum efficiency improves when decreasing the conduction angle; on the other hand, the harmonic tones are generated with a smaller conduction angle. The class A amplifier has the lowest harmonic tones and the lowest efficiency. Class AB amplifier generates the highest fundamental tone output power with reasonable maximum efficiency. Due to the speed constraints, it is challenging to design the switch-mode power amplifier at millimeter-wave frequencies. Therefore, millimeter-wave power amplifiers mostly operate at class AB mode for high linearity and maximum efficiency.

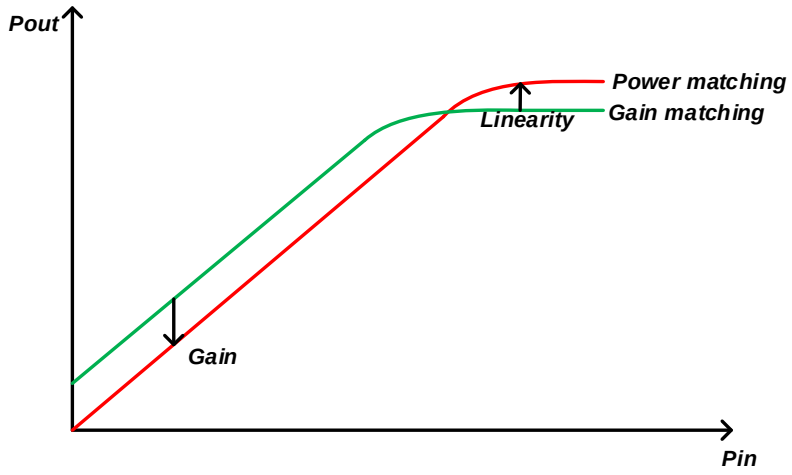


Figure 3.3: Relationship of the amplifier power matching and gain matching.

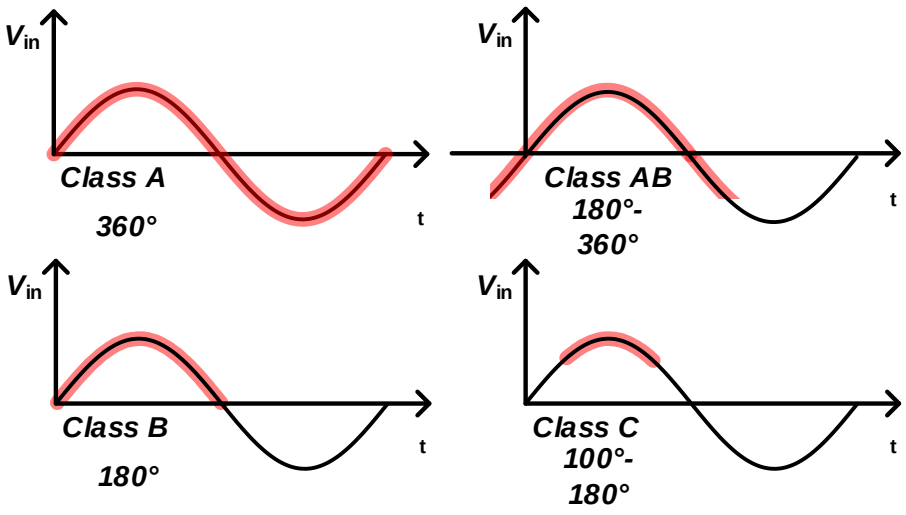


Figure 3.4: The load line and conduction angle of the power amplifier operation class.

Class	Conduction angle	Power consumption
Class A	360°	Very high
Class AB	180°-360°	High
Class B	180°	Low
Class C	100°-180°	Very low

Table 3.1: The SATCOM transmitter operation class load, transistors conduction angle, and power consumption.

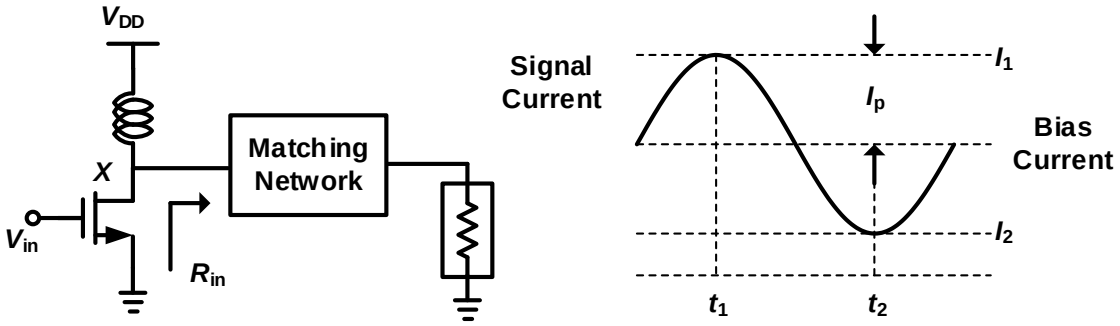


Figure 3.5: Definition of class A PA with schematic and signal current figure.

3.2.2 PA Architecture

In order to emphasize PA merits in class A operation, designers would like to present the definition of class A PA. Shown in Fig.3.5 is an example. We note that the transistor(s) remain on and operate linearly across the entire input and output range. At the same time, the conduction angle, which is defined as the percentage of the signal period during which the transistor(s remain on multiplied by 360°) is always 360°.

Now, let us compute class A amplifiers' maximum drain (collector) efficiency. To reach the maximum efficiency, we allow V_x in Fig.3.5 to reach $2V_{DD}$ and nearly zero at the low point. Thus, the power delivered to the output matching block would approximately equal to:

$$\frac{(\frac{2V_{DD}}{2})^2}{2R_{in}} = \frac{V_{DD}^2}{2R_{in}} \tag{3.1}$$

which is also delivered to R_L if the matching block is lossless. At the same time, the

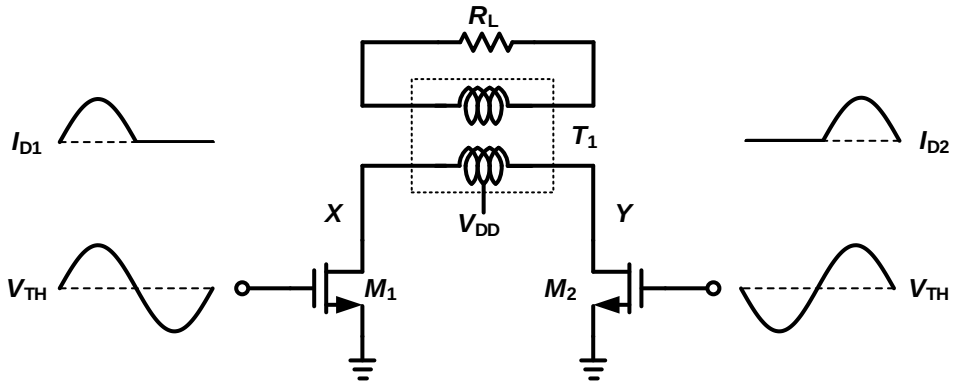


Figure 3.6: Definition of class B PA with detailed schematic and input-output waveform.

inductive load carries a constant current of V_{DD}/R_{in} from the supply voltage. Thus,

$$\begin{aligned}\eta &= \frac{\mathrm{V_{DD}^2/(2R_{in})}}{\mathrm{V_{DD}^2/R_{in}}} \\ &= 50\%.\end{aligned} \tag{3.2}$$

The outer 50% of the supply power is dissipated by M_1 itself.

For class B power amplifiers, they are defined as two parallel stages, each of which conducts for only 180°, thereby achieving a higher efficiency than the class A counterpart. Shown in Fig 3.6 is an example where the drain currents of M_1 and M_2 are combined by transformer T_1. We may view the circuit as a quasi-differential stage and a balun driving the single-ended load. In this case, the gate bias voltage of the devices is therefore chosen approximately equal to their threshold voltage, say, 0.3V in TSMC 65nm process [55].

Fig.3.6 presents class B circuit for efficiency calculation. We recognize that a half-cycle sinusoidal current, $I_{D1} = I_p sin\omega_0 t\,, 0 < t < \pi/\omega_0$, producers a similar current in the secondary. Thus the total current flowing through R_L in each full cycle is equal to $I_L = (m/n)I_P sin\omega_0 t$, producing an output voltage given by:

$$V_{\mathrm{out}}(t) = \frac{m}{n} I_{\mathrm{p}} R_{\mathrm{L}} \sin\omega_0 t, \tag{3.3}$$

and deliver an average power of:

$$P_{\mathrm{out}} = \left(\frac{m}{n}\right)^2 \frac{R_{\mathrm{L}} I_{\mathrm{p}}^2}{2} \tag{3.4}$$

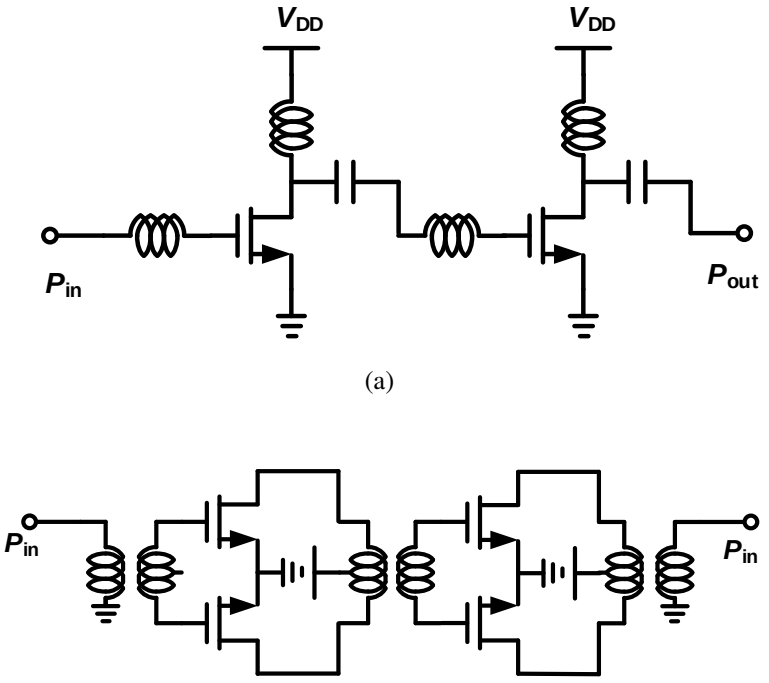


Figure 3.7: Single-ended power amplifier (a) and differential power amplifier (b).

At the same time, the average power provided by V_DD is equal to:

$$P_{\text{supp.}} = 2\frac{I_{\text{p}}}{\pi}\text{V}_{\text{DD}} \tag{3.5}$$

Dividing equation. 3.4 by equation. 3.5 gives the drain (collector) efficiency of class B stages:

$$\eta = \frac{\pi}{4\text{V}_{\text{DD}}}\left(\frac{m}{n}\right)^2 I_{\text{p}}R_{\text{L}} \tag{3.6}$$

As expected, usually, it approximately equals 79% to 81%.

Mainly, PAs have been designed as a cascade of single-ended stages. Two reasons account for this choice: the antenna is typically single-ended, and single-ended RF circuits are much simpler than their differentials counterparts.

Fig.3.7 shows the three-stage single-ended power amplifier architecture. Single-ended PAs, however, suffer from two drawbacks: First, their output power is limited by the single transistor. The second drawback of single-ended PAs stems from huge transient currents that they pull from the supply to the ground, which would destroy the transistors to a large extent.

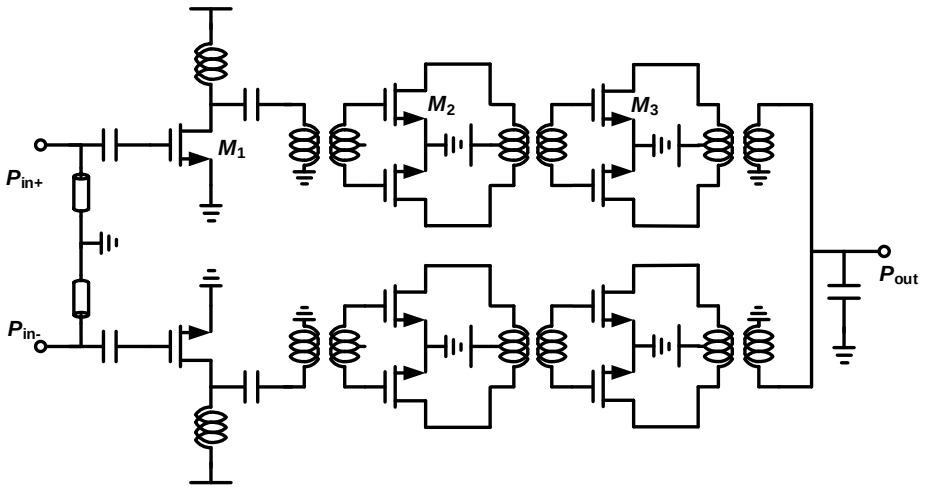


Figure 3.8: Power amplifier in transmitter structure for future 6G satellite communication system.

The differential architecture power amplifier can achieve higher output power. The two-stage power amplifier has symmetric two paths for a differential signal. The single-ended input is converted to the differential by using the input balun, the inter-stage matching uses a transformer, which also provides a VDD supply at the center tap of the transformer.

The output impedance matching also employs a balun for converting the load impedance to desired impedance. The differential power amplifier is 3-dB higher than a single-ended one. However, due to the higher insertion loss of the balun and unbalance of the differential signal, the differential power amplifier linearity may be degraded.

3.2.3 Mutually Coupled Inductor Based PA Design for SATCOM

As discussed in the last section, the differential architecture is chosen with a common source in the SATCOM design. Fig.3.8 show the circuit schematic of the single-path SATCOM differential power amplifier.

The power amplifier consists of three stages: driver, high-bandwidth, and power output stage. The transistor sizes are 120um/0.065um, 132/0.065um, and 308um/0.065um for the first, second, and third stages.

The input matching network uses the series transmission line and shunts capacitor for transforming the source 50 impedance to drive amplifier input conjugate impedance. A

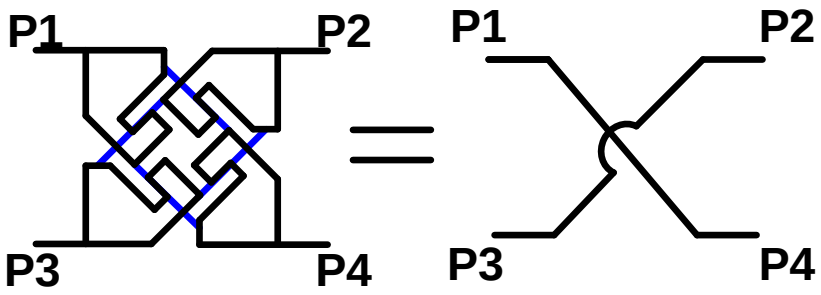


Figure 3.9: Fully symmetric cross circuit for interconnection in the chip layout.

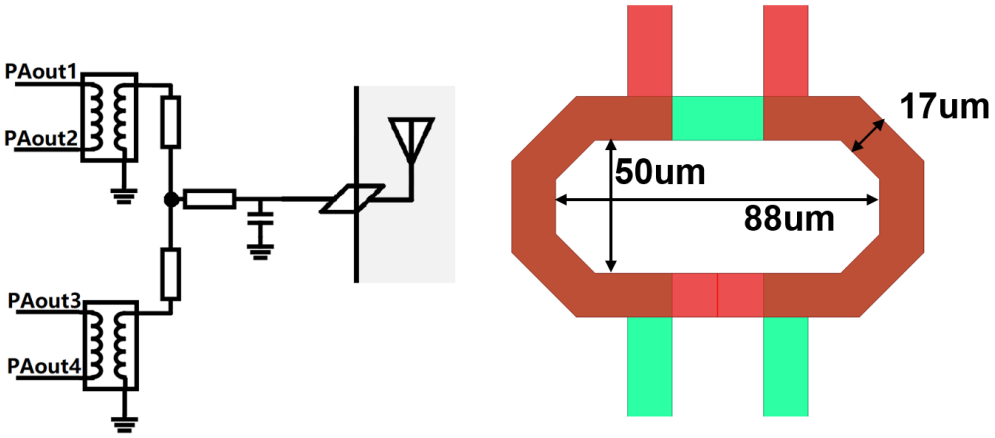


Figure 3.10: The design for output balun with HFSS and detailed layout values of the simulated balun.

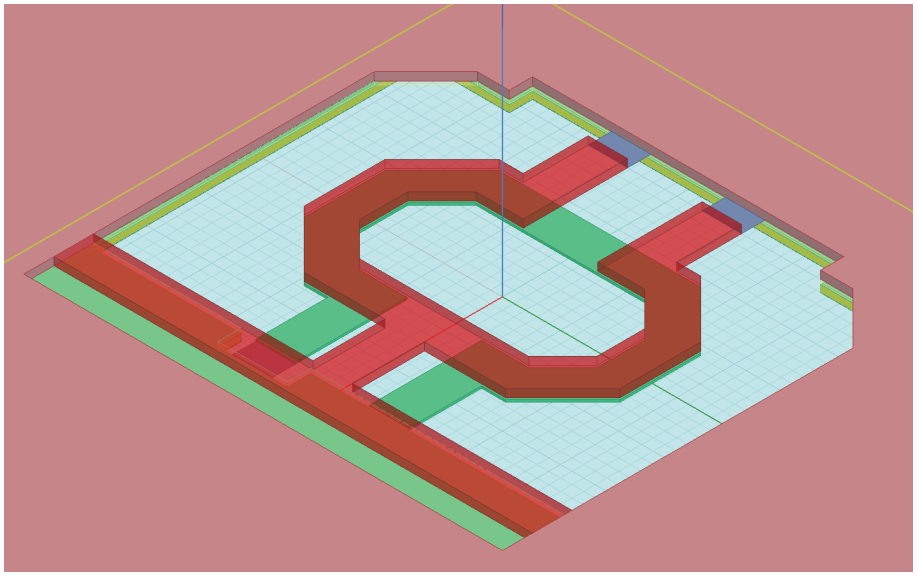


Figure 3.11: The design for Balun's 3D views in HFSS with the ground layer.

series capacitor is placed for DC-cut and transistor bias.

The power stage differential signal is converted to single-ended using an on-chip balun [56, 57]. The balun is carefully designed for low-loss impedance matching [56–62]. The differential architecture can neutralize the capacitance by cross-connecting the one output to another input through a capacitor, which is equivalent to the gate-drain capacitance.

Since the differential phase and amplitude mismatch may cause gain and power degradation, the fully symmetrically is facilitated at the differential circuits design. Fig.3.9 presents the fully symmetric cross circuit used in capacitive neutralization circuit [63–65].

The output mutually coupled inductor is shown in Fig.3.10, and Fig.3.11 should be designed to convert the differential signal to single-ended and provide the optimal impedance for the transistor output with a low insertion loss. The transformer 3D model views are shown in Figure 3.20. The transformer is a single turn with a vertical structure for a high coupling coefficient and friendly layout.

The PA performance is characterized by a 50 Ohm on-wafer measurement setup under 1.05V supply voltage with fixed class AB bias. The PA small signal measurement uses Keysight PNA-X. Fig.3.12 shows the measured S-parameter results.

Designers can quickly determine the peak gain of 27dB and 3-dB bandwidth from 24GHz to 36 GHz. The PA large-signal measurement uses a Keysight signal generator and power meter.

The measured results are shown in Figure 3.24. The amplifier achieves 20.1 dBm saturated output power and 18.2 dBm 1-dB compression point at 29 GHz. The peak power-

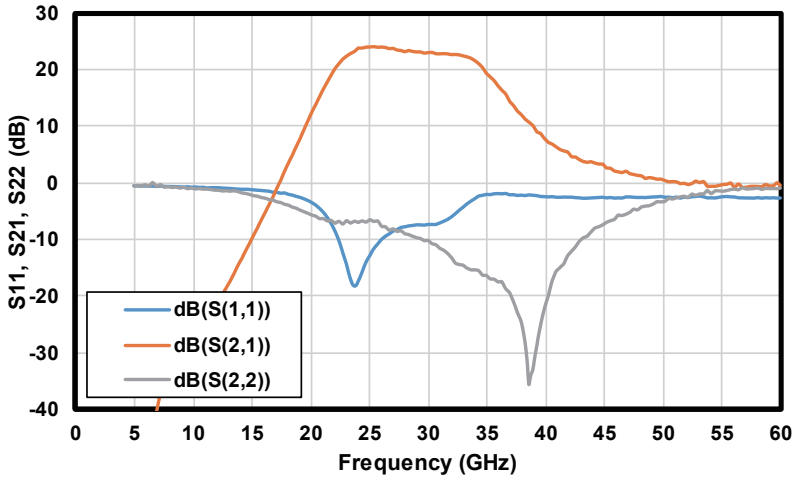


Figure 3.12: The S-parameter results for the high-bandwidth power amplifier.

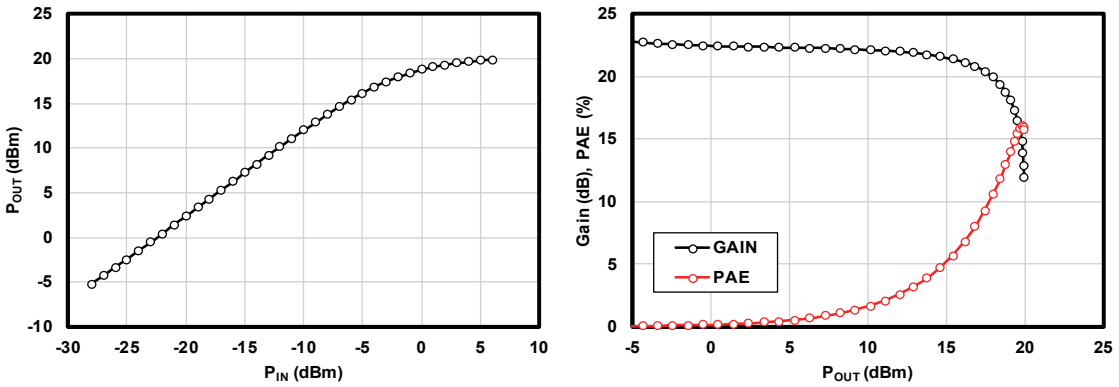


Figure 3.13: The Gain, PAE, and Psat measurement results for the proposed high-bandwidth power amplifier.

added efficiency is 17 %, and PAE at P1dB is 15%. This PA exhibits high-performance linearity and power delivery. The implemented 28 GHz differential power amplifier is shown in Figure 3.22. The amplifier occupies a core area of 0.17 mm^2 [66].

3.3 Mixer Design

3.3.1 Mixer Design Considerations

As trusted by many people, Mixers perform frequency translation by multiplying two waveform (and possibly their harmonics). As such, mixers have three distinctly different ports. Fig.3.15 shows a generic transceiver environment in which mixers sense the RF

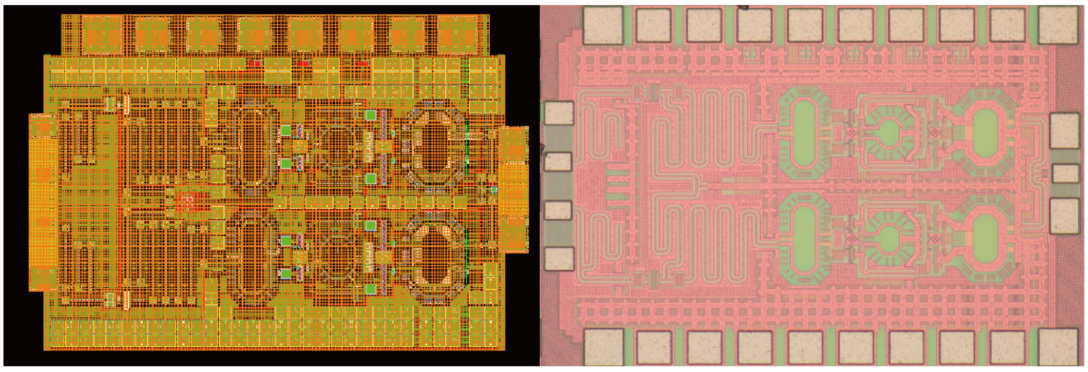


Figure 3.14: The layout of the power amplifier and the detailed micrograph of the power amplifier TEG.

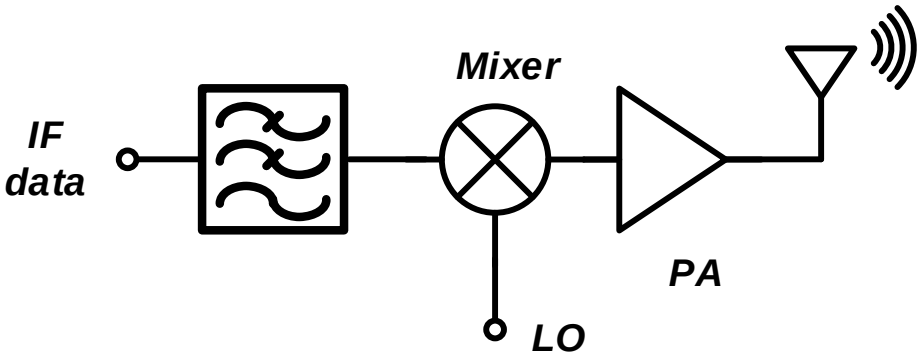


Figure 3.15: Role of mixers in a generic transmitter.

signal at its "RF port" and the local oscillator waveform at its "LO port."

The output is called the "IF port" in the "baseband port" in a direct-conversion RX. Similarly, in the transmit path, the upconversion mixer input sensing the IF or the baseband signal is the IF port or the baseband port, and the output port is called the RF port. The input driven by the LO is called the LO port.

The following equation shows the calculation results of up-conversion for the heterodyne case when the IF signal:

$$x(t) = \cos(\omega_{\mathrm{IF}} t) \tag{3.7}$$

is multiplied by the LO signal $\cos(\omega_{\mathrm{LO}} t)$

$$\begin{aligned} \varphi_{\mathrm{DSB-SC}} &= \cos(\omega_{\mathrm{IF}} t)\cos(\omega_{\mathrm{LO}} t) \\ &= \frac{1}{2}[\cos(\omega_{\mathrm{IF}} + \omega_{\mathrm{LO}})t + \cos(\omega_{\mathrm{IF}} - \omega_{\mathrm{LO}})t] \end{aligned} \tag{3.8}$$

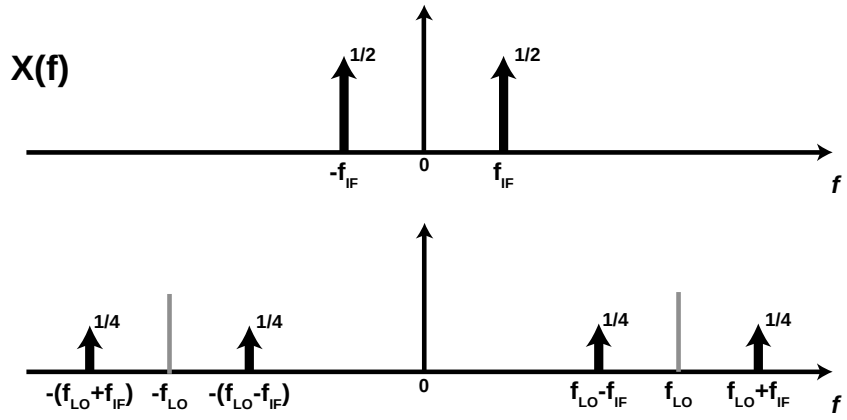


Figure 3.16: Up-conversion operation in the frequency domain.

The multiplication result has two components on both sides of the LO frequency at the same distance that equals the IF frequency, and the resultant signal is called Double-sideband (DSB) signal. Only one of these components is transmitted, causing the Single-sideband (SSB) conversion loss to be 3dB even in the ideal lossless case [67].

In practical cases, the LO signal leaks from the LO port to the RF port, causing an inevitable frequency component appearance at the frequency of LO. Fig.3.16 shows the up-conversion operation on the frequency spectrum.

Down-conversion can be simply performed by multiplying the RF signal again by LO as in the following:

$$\begin{aligned} \varphi_{\mathrm{DSB-SC}} &= \cos(\omega_{\mathrm{IF}}t)\cos(\omega_{\mathrm{LO}}t)\cos(\omega_{\mathrm{LO}}t) \\ &= \frac{1}{2}\cos(\omega_{\mathrm{IF}})t(1+\cos(2\omega_{\mathrm{LO}})t) \\ &= \frac{1}{2}\cos(\omega_{\mathrm{IF}})t + \frac{1}{2}\cos(\omega_{\mathrm{IF}})t(\cos 2\omega_{\mathrm{LO}}t) \end{aligned} \tag{3.9}$$

The IF signal is retrieved with another 3dB loss, and some high-frequency components appear with the desired output. However, the high frequency and the low amplitude lower the effect of the rear components on the desired output.

The explained mixing procedure assumes the fundamental frequency component of the LO signal to be inputted to the mixer, so the RF signal is up-converted to $f_{LO} + f_{IF}$ or $f_{LO} - f_{IF}$.

Owing to device capacitances, the mixer suffers from unwanted coupling (feedthrough) from one port to another [Fig.3.17]. For instance, if the mixer is realized by MOSFET

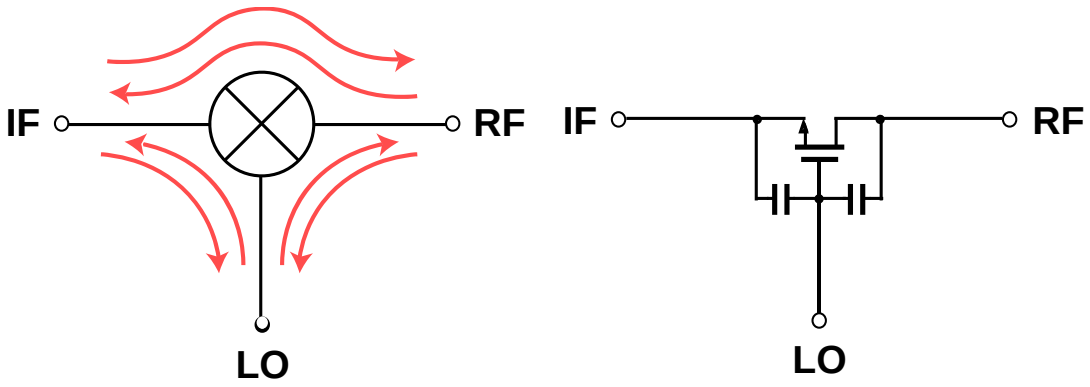


Figure 3.17: Feedthrough mechanisms in a mixer and feedthrough paths in a MOS mixer.

[Fig.3.17], then the gate-source and gate-drain capacitors create feedthrough from LO port to the RF and IF ports [68–70]. Interestingly, the feedthrough is entirely determined by the symmetry of the mixer and LO waveforms. It would disappear owing to the LOFT cancellation methods.

The optimized biasing conditions with the DC analysis of the mixer core are shown in Fig.3.18. When looking at the conventional CMOS switch biasing, it is observed easily and similarly.

However, before talking about the DC bias analysis, one critical phenomenon, junction capacitance, would be referred to in the paragraph [71]. Junction capacitance between the heavily doped source (or drain) and the lightly doped body P-well can be calculated as in the following formula:

$$C_{\mathrm{j}}(V_{\mathrm{A}}) = \frac{C_{\mathrm{j0}}}{\left(1 - \frac{V_{\mathrm{A}}}{V_{\mathrm{bi}}}\right)^{\frac{1}{m+2}}} \tag{3.10}$$

Where C_j is the junction capacitance, VA is the applied voltage difference between drain or source and transistor body, C_{j0} is the junction capacitance when VA is 0, V_{bi} is the builtin junction voltage and m is the process related gradient coefficient. From this formula, it can be clearly understood that the only way to reduce this capacitance is by increasing the applied voltage.

In order to reduce the junction capacitance, the bias voltage should be high enough. Of course, effectively, this biasing condition can be seen as a zero-biased transistor with the body connected to a negative voltage. However, it is unrealistic to issue negative voltage in CMOS processes.

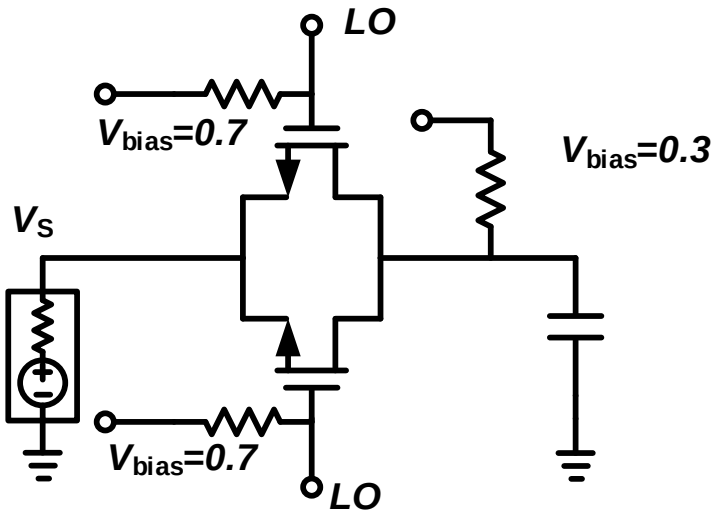


Figure 3.18: DC condition analysis of the SATCOM mixer.

It should be noted that the threshold voltage of the transistor changes due to these biasing conditions in the following way:

$$V_{\text{th}} = V_{\text{th0}} + \gamma(\sqrt{|V_{\text{SB}} - 2\phi_{\text{F}}|} - \sqrt{|2\phi_{\text{F}}|}) \tag{3.11}$$

where V_{th} is the threshold voltage, V_{th0} is the threshold at zero bias, γ is the body effect parameter, V_{SB} is the source-body voltage, and ϕ_F is the surface potential. This small increase in the threshold voltage can be dealt with easily by optimizing the bias voltages.

Conveniently and effectively, a transmission line could be utilized for a matching block. Adjust the transmission length to match the LO input capacitance impedance at the LO port. Besides, the feedthrough of IF is too large at the output, and it needs to be adequately suppressed.

A 50fF capacitor with a high impedance at IF frequencies are connected as a DC block component, and a shunt transmission line shorted to the ground is used to filter out the IF frequency components. As shown in Fig.3.20, the shorted stub input return loss is high at the IF frequencies and very low at the desired frequency band.

3.3.2 Mixer Design for SATCOM

Due to the high-performance levels of double-balanced mixers, they are usually realized to provide low LOFT in RF or frequency mixing applications. The action of the double-

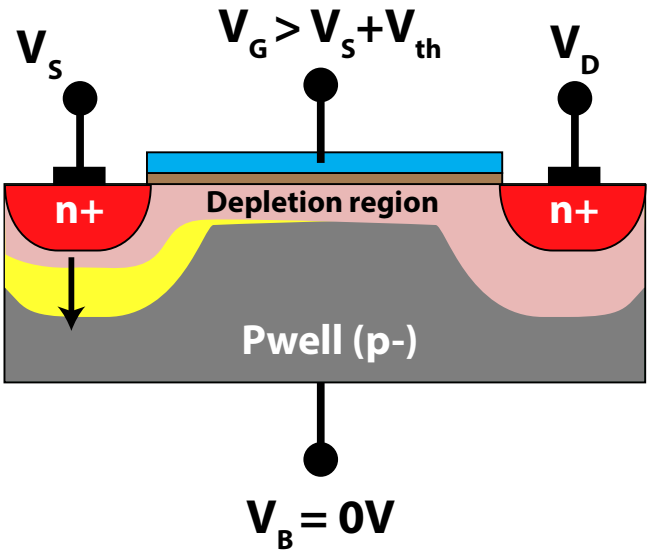


Figure 3.19: Source-body voltage effect on the depletion region and its capacitance.

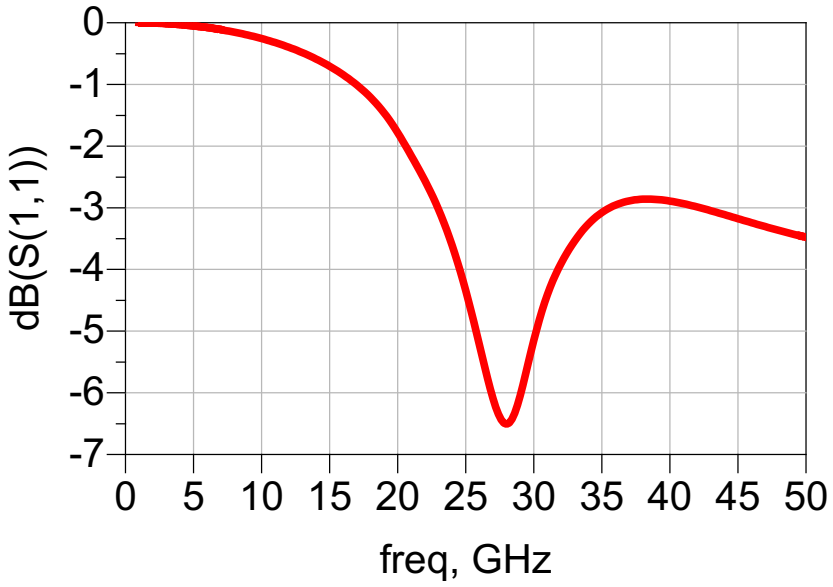


Figure 3.20: The input return loss for the output matching block.

balanced mixer means that the input RF and local oscillator signals are âĂIJbalanced out, and their level is considerably reduced at the output.

Fig.3.21(a) shows SATCOM's design of double-balanced mixers structure. Such a topology introduces two negative feed-throughs at each output, one from V_{LO} and another from $\overline{V_{LO}}$. The output signal remains intact because, when V_{LO} is high:

$$V_{\text{out1}} = V_{\text{RF}}^{+} \tag{3.12}$$

and

$$V_{\text{out2}} = V_{\text{RF}}^{-} \tag{3.13}$$

That is

$$V_{\text{out1}} - V_{\text{out2}} \tag{3.14}$$

is equal to:

$$V_{\text{RF}}^{+} - V_{\text{RF}}^{-} \tag{3.15}$$

for a high LO and

$$V_{\text{RF}}^{-} - V_{\text{RF}}^{+} \tag{3.16}$$

for low LO.

At the same, Fig.3.21(b) operates with both balanced LO waveforms and balanced RF inputs.

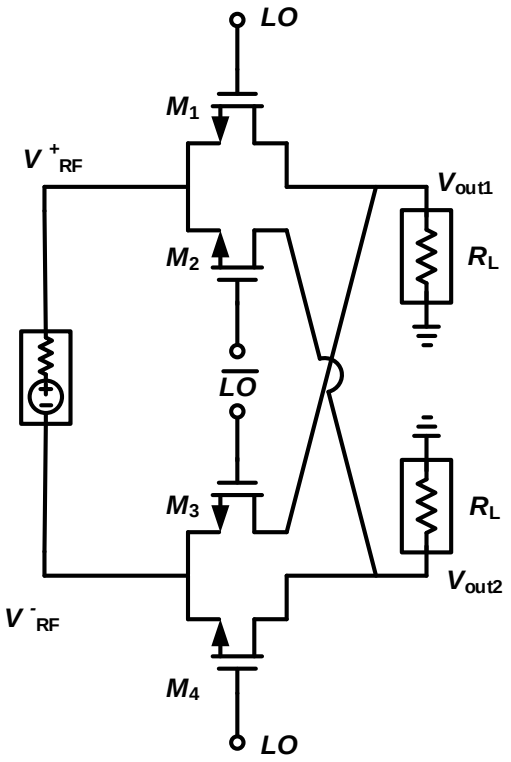
Utilizing double-balanced mixers in the SATCOM system, the designer can increase the transmitter linearity and isolation between all ports and own better suppression of spurious products (all even order products of the LO).

The double-balanced mixer consists of all NMOS transistors with sizes of 80um/0.065um. The input matching network uses the series transmission line and shunts capacitor for transforming the source 50 impedance to drive mixer input conjugate impedance. A series capacitor is placed for DC-cut, and a 5K Ohm resistor for transistor bias [72].

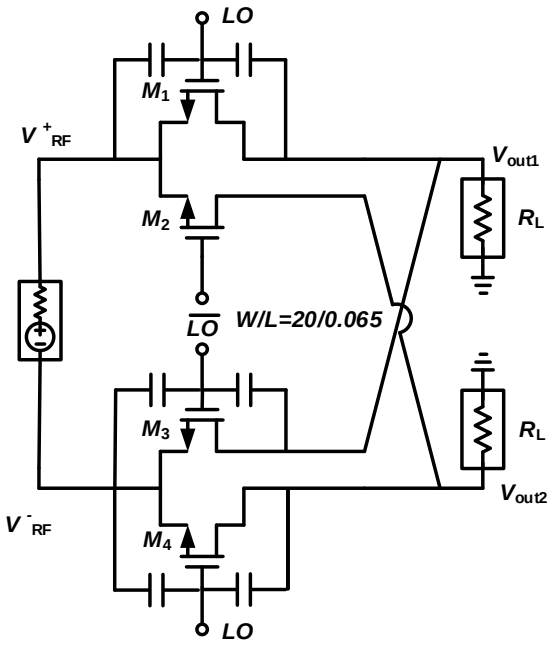
Since the differential phase and amplitude mismatch may cause gain and power degradation, the fully symmetrically is facilitated at the differential circuits design. Fig.3.22 presents the fully symmetric circuit layout of SATCOM's mixer.

The mixer performance is characterized by a 50 Ohm on-wafer measurement setup under 1.05V supply voltage with fixed bias, including the DC block part. The mixer noise figure (NF) measurement has not been measured. Shown in Fig.3.23(a) is an example for the NF parameters in simulation results.

The designer can quickly figure out the noise figure of -8dB at 29GHz, and the system NF gradually increases with the frequency improvement.



(a)



(b)

Figure 3.21: SATCOM's doubled-balanced mixers (a) and SATCOM's doubled-balanced mixers for calculation.

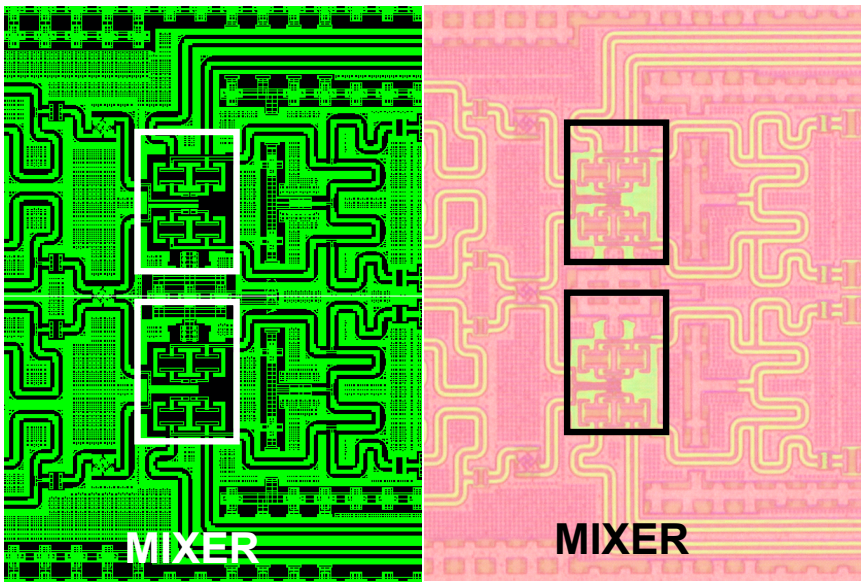


Figure 3.22: The layout and picture of the SATCOM mixer.

The measured results are shown in Fig.3.23(b). This mixer exhibits high-performance linearity and power delivery at the input power of -20dBm. According to the extension cord, the designer can figure out the IIP3, -1.8dBm. The implemented 29 GHz double-balanced mixer is shown in Fig.3.22 , the amplifier occupies a core area of 0.27 mm^2.

3.4 LO Design

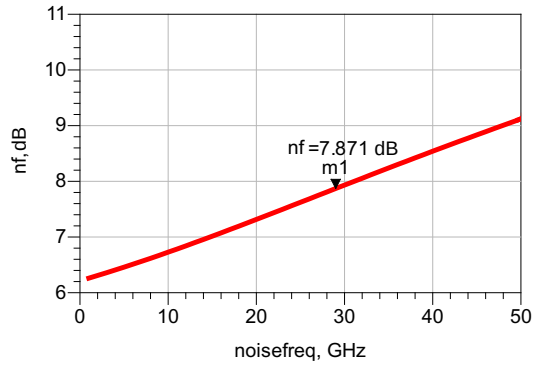
As we all know, direct RF conversion utilizes four different phases of LO signal, with 0° 90° 180° and 270° respectively. In order to drive those two differential signals, the LO part should consist of the poly-phase shifter with input and output buffer to match the impedance between RF mixers and input LO signal [73].

The path structure of LO is shown in the Fig.3.24. From the picture, an input balun is added to the LO path to change the single-ended signal to a differential one.

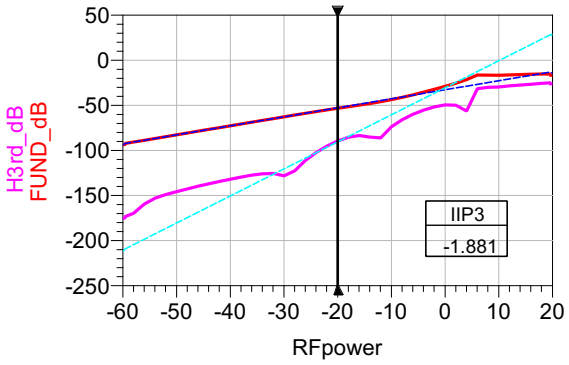
3.4.1 LO Input Balun

From Fig.3.25, LO signal input is optimized with low insertion loss balun to change the single-ended signal to a differential one. Simultaneously, the balun should provide the optimal impedance for the transistor input and the pad signal.

The transformer (balun) is designed in the electromagnetic (EM) simulator with 3D modeling and a finite element method (FEM) solver. The balun 3D model views are



(a)



(b)

Figure 3.23: The SATCOM's mixer NF (a) and the SATCOM's mixer IIP3 (b).

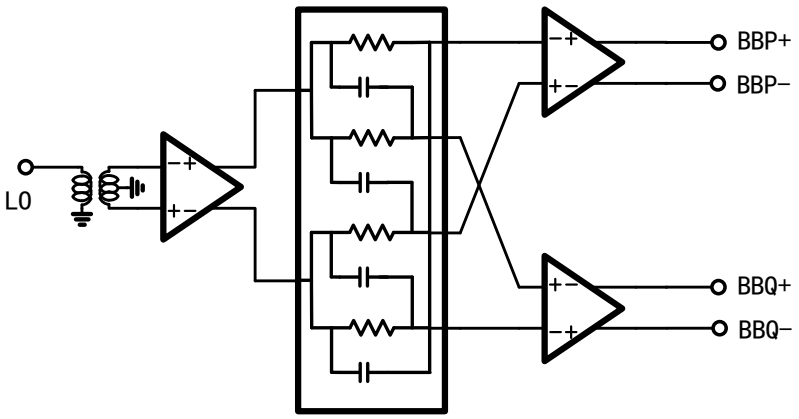


Figure 3.24: The structure of local oscillator part.

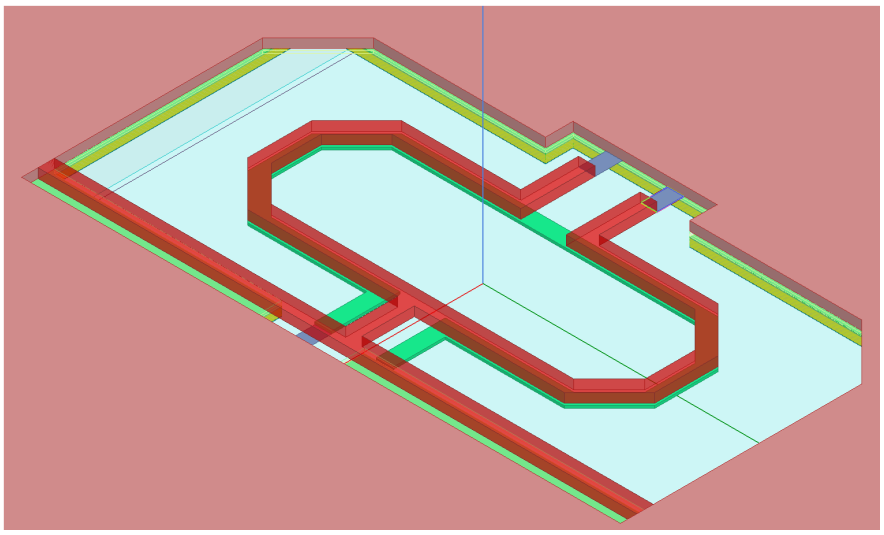


Figure 3.25: The 3D model view of the LO input balun.

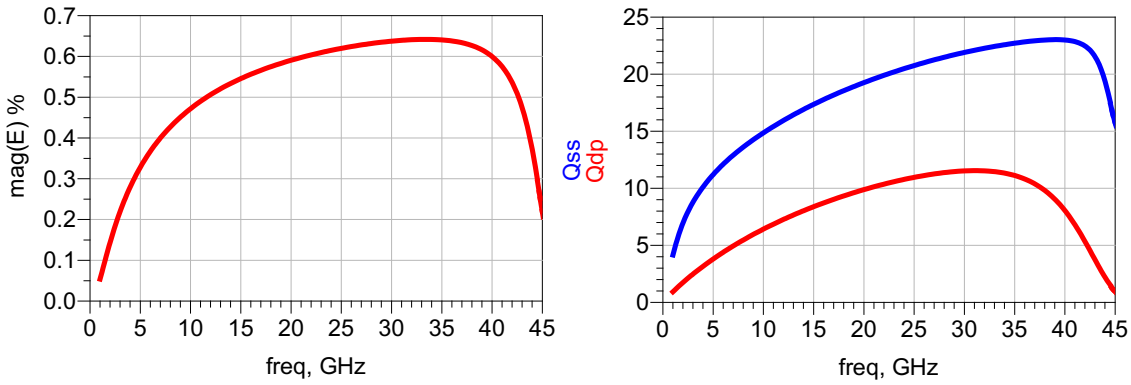


Figure 3.26: Balun efficiency and quality factor.

shown in Fig.3.25.

The transformer is a single turn with a vertical structure for a high coupling coefficient and friendly layout. The simulated insertion loss is 0.7 dB at 29 GHz. The transformer simulated efficiency and quality factor are shown in Fig.3.26 [74].

3.4.2 Input Buffer and Output Buffer

The primary purpose of the input buffers is to provide better matching to the poly-phase shifter and compensate for the balun losses. They are designed using conventional common-source topology from the single-ended side and using neutralized differential amplifier from the differential side.

The bandwidth should be somewhat wide (around 5GHz) to be able to change the LO frequency when needed. The input return loss and gain of the buffer is shown in Fig.3.27(a) and Fig.3.27(b) showing usability in the 27-31GHz region. Fig.3.27(c) shows the input buffer circuit diagram of the final TEG that is to be measured.

A differential output buffer is issued in the LO architecture due to the capacitance impedance at the mixer's input. The primary purpose of the output buffer is to provide better matching to the mixers and compensate for the loss at the LO path.

Like the input buffer, the output buffer also utilizes conventional common-source topology from the single-ended one and uses a neutralized differential amplifier from the differential side.

From the Fig.3.28(a) and Fig.3.28(b) designer can easily figure out the bandwidth form 27GHz to 31 GHz (almost 4 GHz width). Fig.3.28(c) show the circuit diagram of the output buffer at the same time.

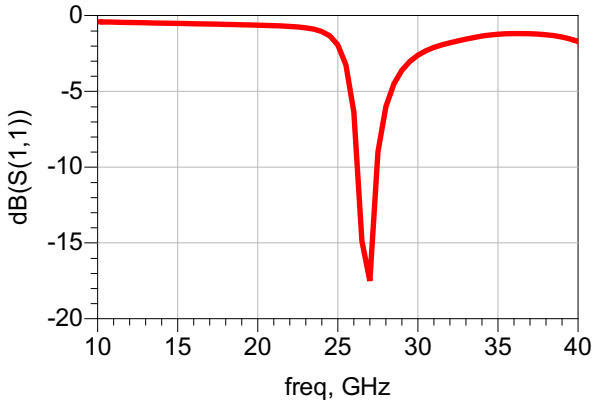
3.4.3 Poly-Phase Shifter

For the quad-phase generation, a constant-magnitude PPF is adopted in this work. Varactors controlled by the 10-bit DACs are utilized in the PPF. The quadrature-phase mismatch after fabrication can be compensated by tuning the varactor [75].

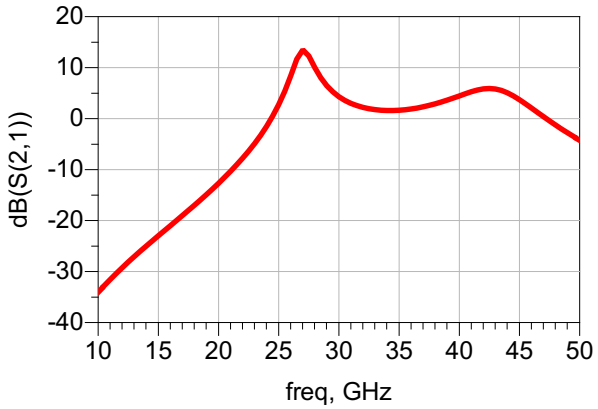
Fig.3.29 shows the circuit schematic for the PPF. The R_{ON} andR_{Cap} define the RC value of PPF, and it can decide the accuracy of PPF's phase.

3.5 RF Switch Design

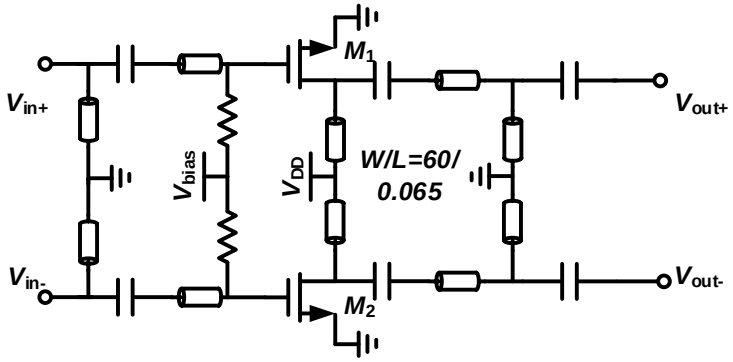
The RF switch is also a critical component for the direct-conversion TX for saving the number of antennas. Fig. 3.30 illustrates the proposed switched parallel resonance net-



(a)

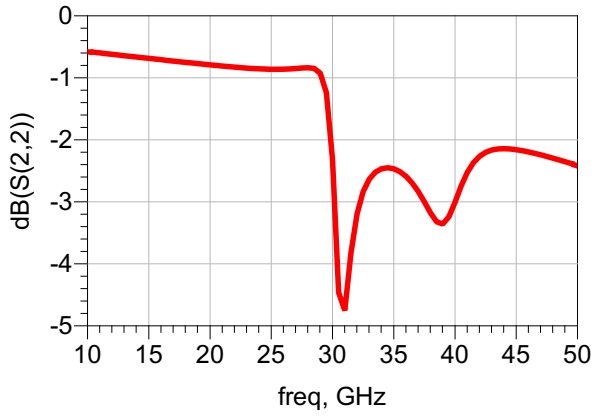


(b)

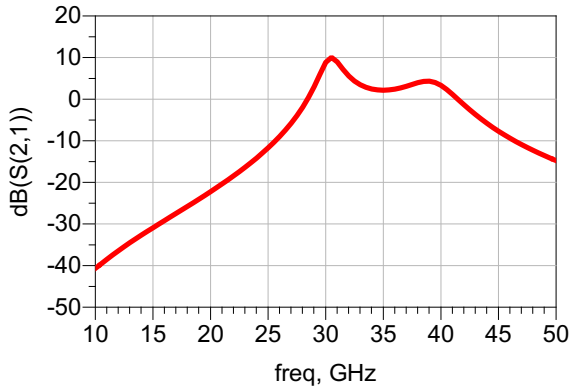


(c)

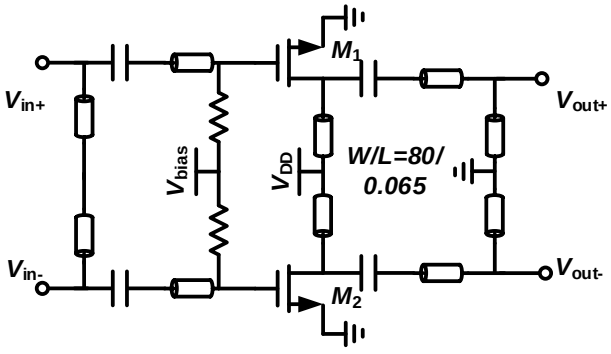
Figure 3.27: The input return loss for LO input buffer (a), the gain for LO input buffer (b), and input SATCOM buffer circuit topology (c).



(a)



(b)



(c)

Figure 3.28: The input return loss for LO output buffer (a), the gain for LO output buffer (b), and output SATCOM buffer circuit topology (c).

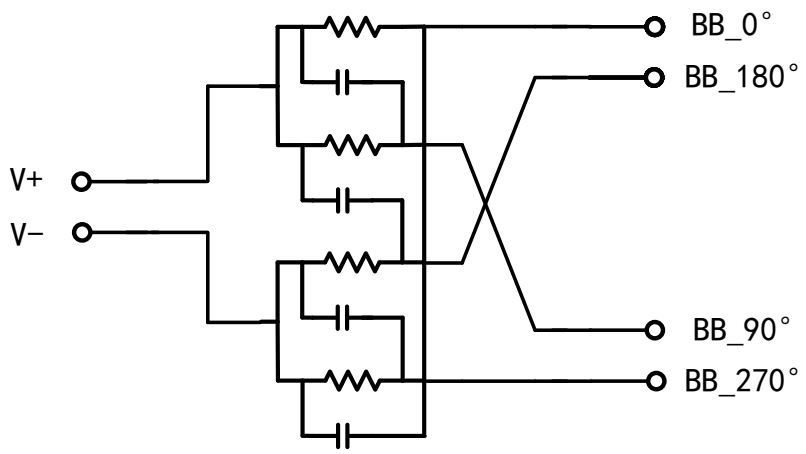


Figure 3.29: Circuit schematic for the PPF.

work architecture. The proposed RF switch is composed of three ports, six body-floating transistors, and one isolation inductor.

Fig. 3.31 shows the operation principle of the proposed RF switch. To route RF signal from port IN to port OUTA, transistors M_1, M_3, and M_5 are turned on, with M_2, M_4, and M_6 are turned off. Transistors M_1, M_3, and M_5 act as on-resistors R_{on}, whereas M_2, M_4, and M_6 off-capacitors C_{off}. Thus, the path for RF signal from port IN to port OUTA is formed. Meanwhile, The branch from port IN to port OUTB is connected to the ground by transistor M_5 directly. To route RF signal from port IN to port OUTB, transistors M_1, M_3, and M_5 are switched from R_{on} to C_{off} and M_2, M_4, and M_6 from C_{off} to R_{on}, respectively.

To maximize RF switch port-to-port isolation, a single-ended inductor is inserted between the two branches. The on-resistor R_{on}, the off-capacitor C_{off}, and the isolation inductor formed a parallel LC resonance tank. The port IN is implemented close to the isolation inductor to provide a high-Q value of the LC resonance tank. Utilizing the thickest top metal layer for the isolation inductor is also benefit to the high-Q value. To relieve the influence of the distributed connection between M_1, M_3, and M_2, they are grouped together in the final layout.

Fig. 3.32 presents the isolation inductor size and simulated results of inductor value with the Q-factor. According to the figure, the core size of the isolation inductor is $0.116\,\text{mm} \times 0.111\,\text{mm}$. From Fig. 3.32 (b), at the center frequency of 15 GHz, the Q-factor of the isolation inductor is 15 with an inductor value of 1.1 nH. The implemented single-ended isolation inductor inner metal width, inner radius, and turns number is $7\,\mu$m, $26\,\mu$m, and 2.5 turns, respectively.

The proposed high-isolation low-loss RF switch introduced in this work is fabricated

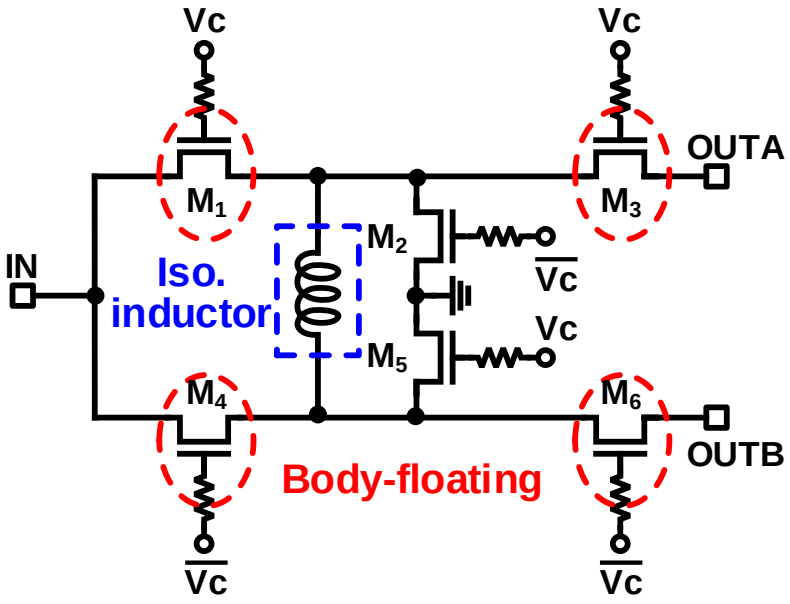


Figure 3.30: Proposed SPDT RF switch schematic with switched resonance network.

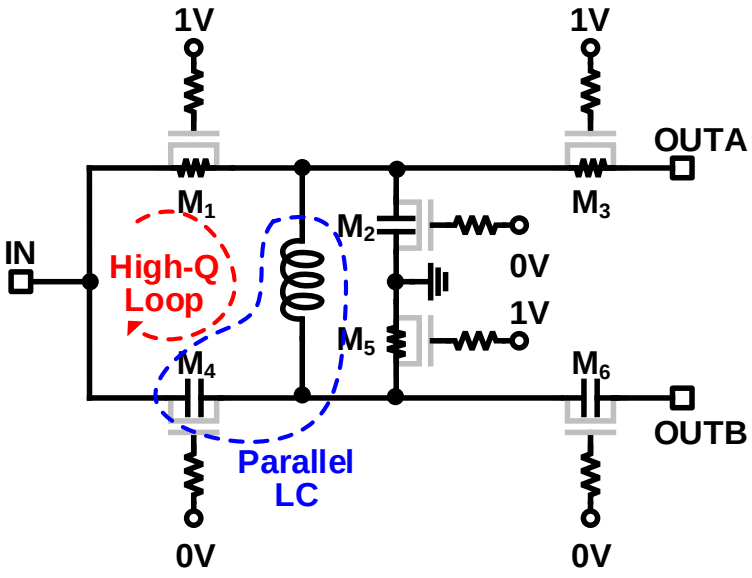


Figure 3.31: SPDT RF switch equivalent schematic with signal routed from port IN to OUTA.

in a standard 65-nm RF CMOS technology. The die micrograph is shown in Fig. 3.33. The on-chip core size of the proposed RF switch is 0.19 mm×0.18 mm. To control the RF switch bias voltage, an integrated SPI block with 10 bit DAC is utilized to provide

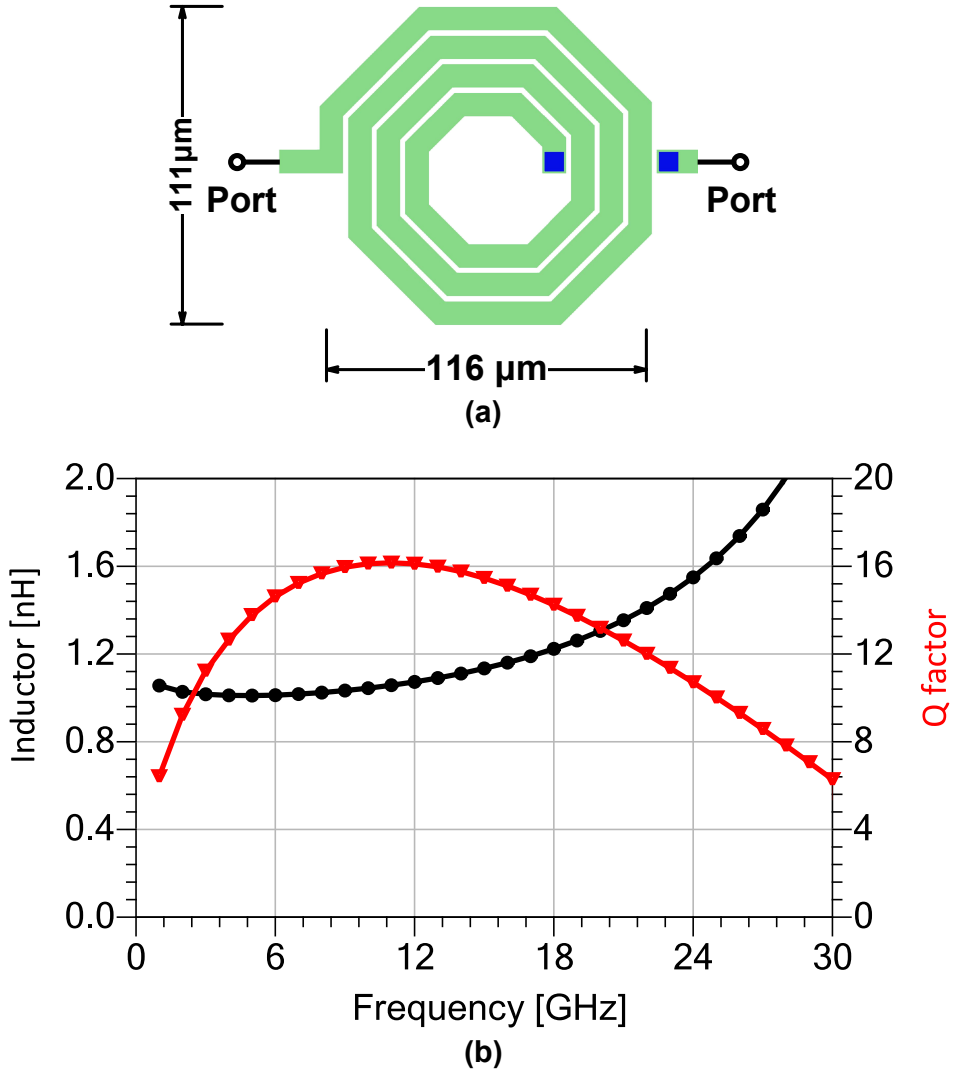


Figure 3.32: Implemented path isolation inductor size and simulated results.

the control signal Vc 0 V or 1.0 V. The RF switch electromagnetic field analysis is mainly processed by EMX CAD tools.

3.6 Measurement Results

In order to measure actual case performance, this measurement will utilize an RF probe station to finish. Firstly, measurement setup is introduced, following with measurement result. The measurement result includes the linearity, noise figure, power consumption, and other critical performance. Lastly, results analysis and a comparison table with current works are presented.

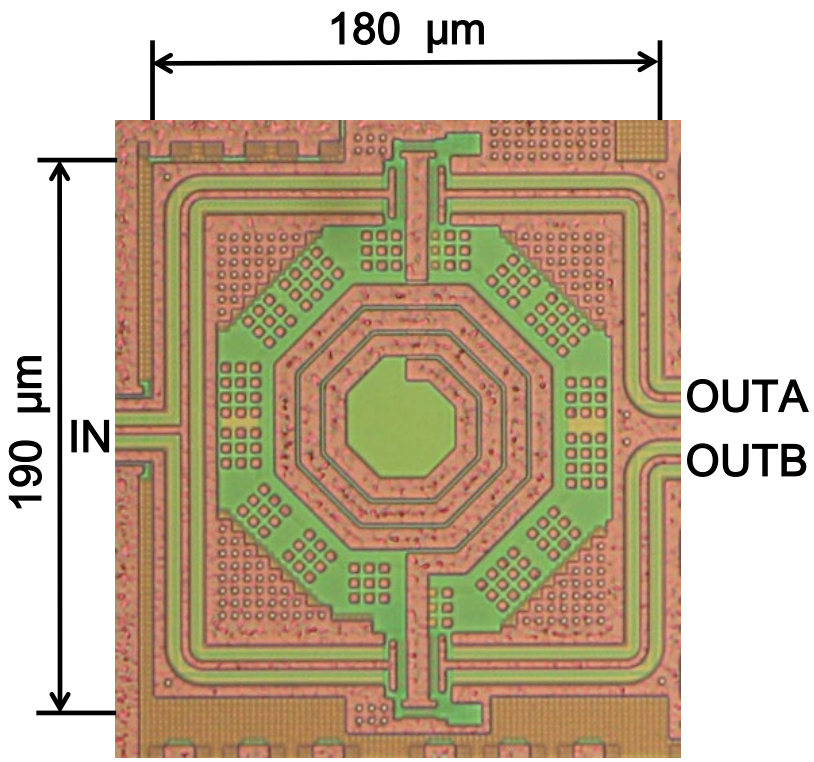


Figure 3.33: The proposed SPDT RF switch chip micrograph.

The micrograph photo of the DUT is shown in Fig.3.34. It was fabricated using 65nm CMOS with a total area of around 3mm^2 excluding the pad area. The measurement setup is the same as up-conversion as only some connections need to be changed (biasing values should also be optimized).

The illustration of the up-conversion transmitter measurement setup is shown in Fig.3.35 The DC bias voltages and VDD are supplied using a semiconductor parameter analyzer. The LO signal is generated using a signal generator. The output signal is evaluated by signal analysis (Keysight DSO91304A).

In this section, the measurement results and their analysis are discussed. By changing the output and input power, designers can draw the figure between output and input power and obtain the IIP3 information. Fig.3.36 show the information with IIP3 equaling to 5dBm.

The designer fabricated another mixer named M2-0240 to down-conversion the modulated signal to measure the system EVM. The measurement setup is shown in Fig.3.37 and the measurement is shown in Fig.3.38.

At QPSK modulation, according to Fig.3.38 we can quickly figure out that the EVM

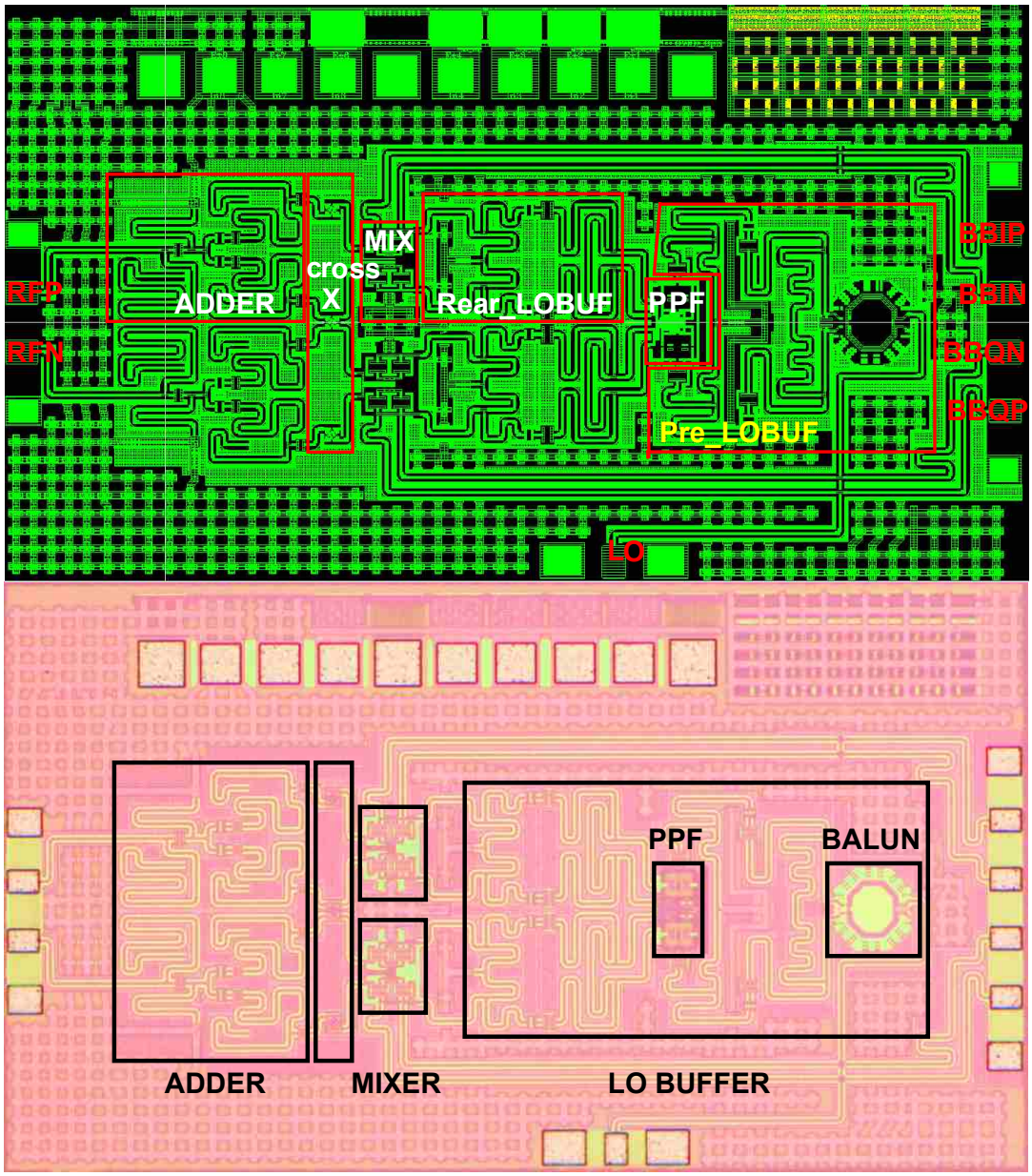


Figure 3.34: System layout and die photo.

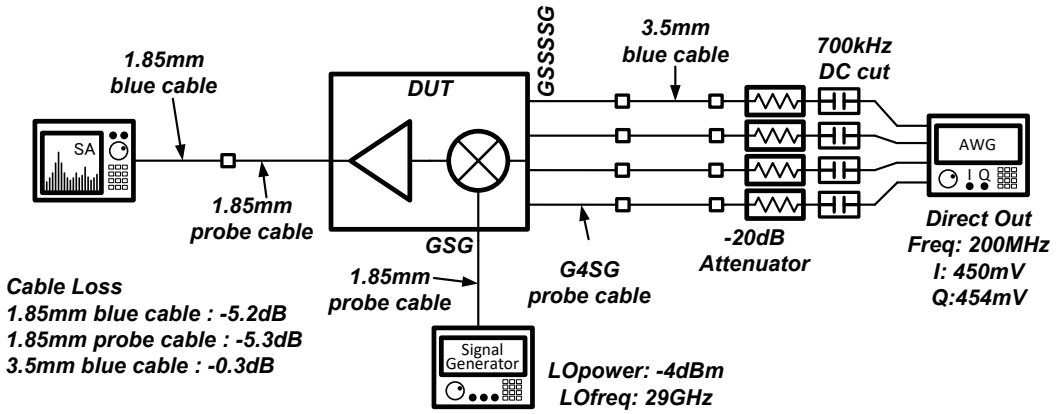


Figure 3.35: Up-conversion mixer measurement setup of the proposed ground base station of the satellite transmitter.

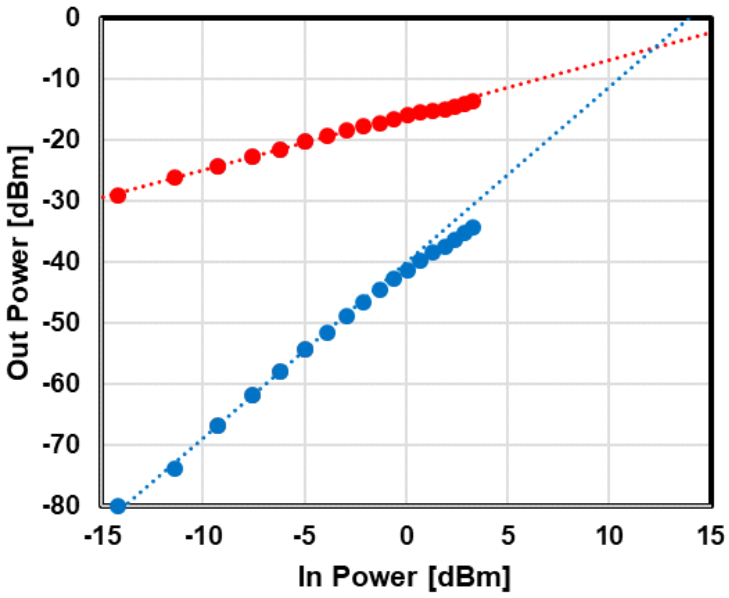


Figure 3.36: SATCOM system linearity results.

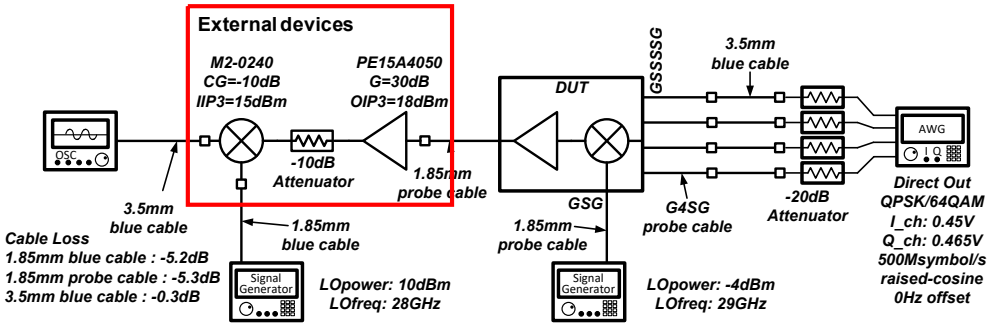
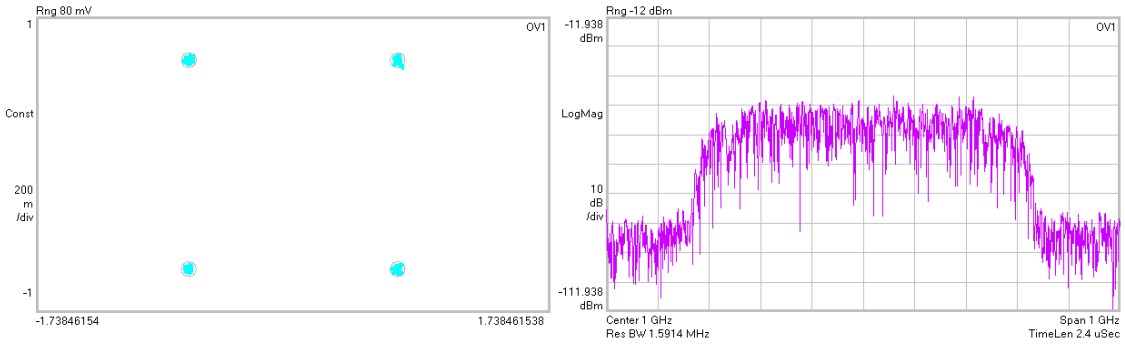


Figure 3.37: Measurement setup for EVM measurement.



Demodulated OSC signal

Demodulated signal performance	
EVM	1.7%
Mag error	1%
Phase error	0.79deg
SNR	35.36dB

Figure 3.38: SATCOM transmitter EVM measurement results.

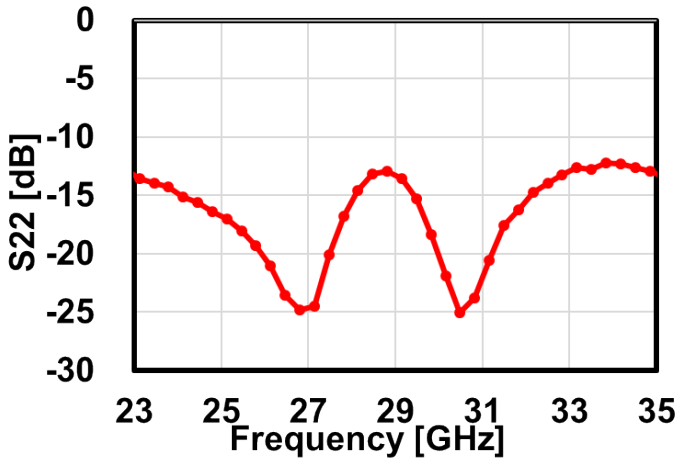


Figure 3.39: SATCOM transmitter output return loss with frequency from 23GHz to 32GHz.

is equal to 1.7%, with mag error and phase error 1% and 0.79degree, respectively. By putting vector network analysis (VNA), the output return loss will be issued in the Fig.3.39, and the results are lower than -13dB at the frequency from 27GHz to 31GHz.

3.7 Conclusion

For the fair evaluation, in Table 3.2, the comparison of SATCOM transmitter system performance comparison is shown. The operating band is almost the same on different paper from this table. Our works are more likely to fulfill high bandwidth, leading to high operation speed and link speed between satellite and Earth's receivers.

According to the transmitter output power parameters, The designers can quickly figure out our satellite transmitter can operate at a very long distance which is helpful for GEO satellite communication.

	This work	ADI Discrete TRX [76]	LG 2018 [77]
Technology	65nm CMOS	N/A	28nm CMOS
Operating band	26.3-31.6GHz	27.2-31.2GHz	25.8-28GHz
Bandwidth	200-600MHz	100MHz	100-500MHz
Psat	20.1dBm	25dBm	9.5dBm
TX Pout @ 2% EVM	8dBm	10dBm	2.5dBm
Power cons.	0.67W/CH	2W/CH	0.68W/CH
Area	1x2.5mm^2	N/A	1x2.6mm^2

Table 3.2: The performance comparison table of the SATCOM transmitter system with ADI discrete TRX and LG TRX

Chapter 4

Phase Shifter Design for Satellite Terminal

The SATCOM has been demonstrated as a ground-breaking technology for providing low-cost, low-latency global internet access services [78, 79]. The phased-array and beamforming techniques are becoming promising solutions to overcome the high free-space-path-loss (FSPL) for the Ka-band frequency allocation [80–84]. Thus, recently, many researchers have been focused on high-performance phased-array transceivers.

In phased-array systems, the phase shifter is the key block that directly influences the beamforming accuracy and quality. A high-resolution and low-insertion-loss phase shifter is necessary to support accurate beam steering with low sidelobe level and low noise figure (NF) for the SATCOM system. Thus, there are many pieces of research about low-insertion-loss and high-resolution phase shifters [85–89].

Active phase shifters based on the vector-summing technique have been reported [90–97]. Those active phase shifters are capable of realizing low-insertion-loss and high-resolution features. However, active phase shifters utilize variable power amplifiers (VGA) for I and Q phase generation with extra power consumption. Also, the system linearity is limited by the power amplifiers. Due to the satellite power limitation, active phase shifters are not suitable for the SATCOM applications. Several digital to analog converters (DAC) are applied for different phase-shifting states to control the active phase shifter, which also increases the control algorithm complexity.

Passive phase shifters based on the switch type and the reflective type are preferable under the power consumption limitation [98]. They can be integrated with a large-scale phased-array system, dramatically reducing the total power consumption. Nonetheless, for STPS, more cascade phase-shifting stages are needed for higher resolution but with higher signal insertion loss and more active area. In terms of RTPS, the existence of

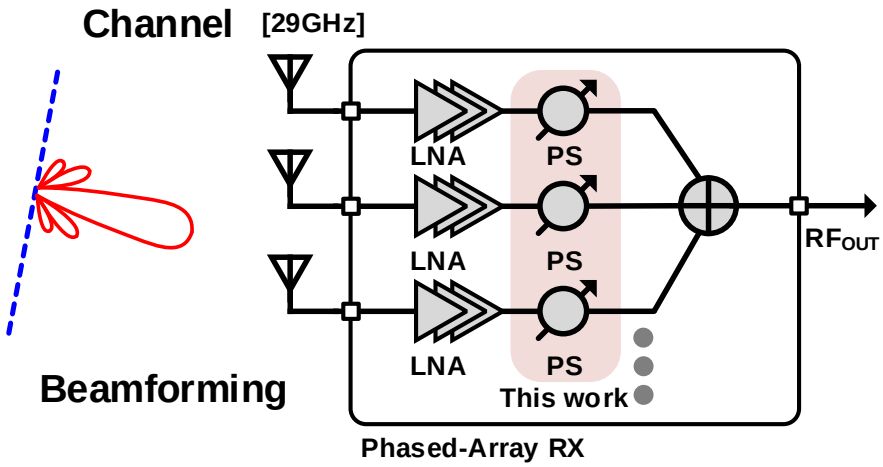


Figure 4.1: Typical phased-array receiver front-end topology.

parasitic effects inside the load terminals limits the cover range. The RTPS coverage can be increased by inserting more RTPS stages but with higher signal insertion loss.

4.1 Phase Shifter Design Considerations

High-performance phase shifters with low insertion loss, high resolution, and radiation hardness are critical components for a phased-array beamforming receiver system. During the past few years, phased-array receivers have been utilized to support high-speed internet access for the SATCOM applications. As shown in Figure 4.1, a typical phased-array receiver front end is composed of high-gain phased-array antennas, low-noise amplifiers (LNA), phase shifters, and path combiners.

4.1.1 Effect of Insertion Loss

According to Figure 4.1, phase shifters play a significant role in the block diagram of the millimeter-wave receiver front end for beam steering. The insertion loss of phase shifters influence the system NF_{total} (from the antenna port to the combiner output port) with the following equation:

$$NF_{\text{total}} = 1 + (NF_{\text{LNA}} - 1) + \frac{NF_{\text{PS}} - 1}{Gain_{\text{LNA}}} + \cdots \tag{4.1}$$

where NF_{LNA}, NF_{PS}, and $Gain_{LNA}$ are the linearity values of the LNA noise figure, the phase shifter noise figure, and the LNA power gain, respectively. The dB value of NF_{PS} can be calculated from the following equation:

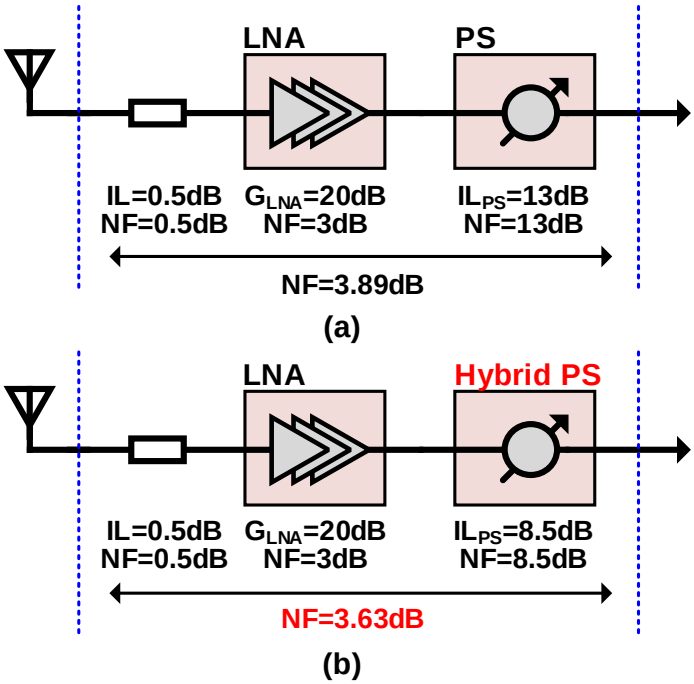


Figure 4.2: Analysis for system NF with the (a) conventional and the (b) proposed hybrid phase shifter.

$$NF_{\mathrm{PS}}(\mathrm{dB}) = IL_{\mathrm{PS}}(\mathrm{dB}) \tag{4.2}$$

where $\mathrm{IL_{PS}}$ is the dB value of the phase shifter insertion loss. According to the mentioned equations, a higher insertion loss of phase shifter represents a higher NF for the system.

Figure 4.2 demonstrates a typical phased-array receiver front-end block with detailed gain and NF value for level diagram analysis. Compared with the traditional phase shifter with 13 dB insertion loss, the proposed hybrid phase shifter with the nonuniform matching reduces the system NF from 3.89 dB to 3.63 dB. Moreover, a system topology with higher insertion loss needs more RF buffer stages to compensate for the chain loss. Those additional stages increase the power consumption for large-array SATCOM applications. Owing to the limitation of the power supply, the phase shifter with high insertion loss is not suitable for the SATCOM system.

4.1.2 Effect of Phase Error

It is widely known that the SATCOM transceiver distances between the low earth orbit satellites and the terrestrial base stations are usually 500 Km to 1000 Km. The distance

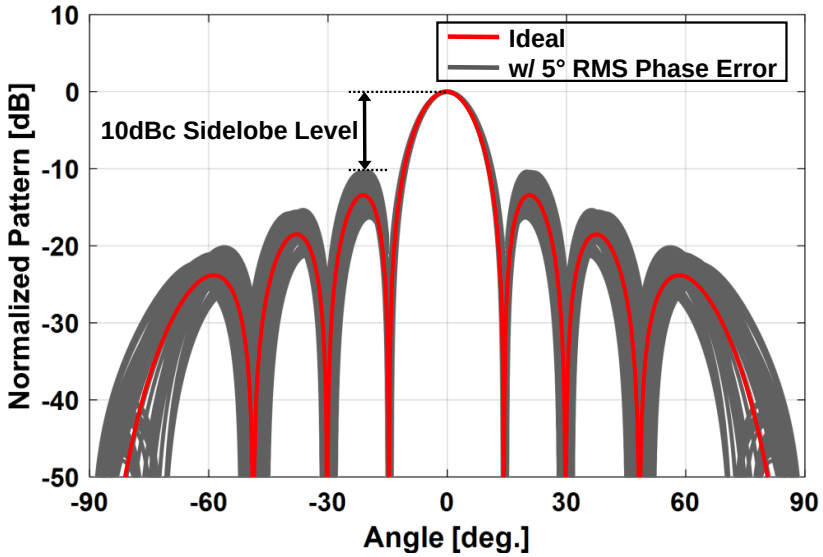


Figure 4.3: Impact of the RMS phase error across array elements on sidelobe level for an eight-element uniform linear array.

inevitability causes high FSPL. To suppress the high FSPL, phased-array systems with multi-elements are preferable for a practical application. However, the phase errors between each element cause degradation of beamforming quality, such as the sidelobe level. Thus, high-resolution phase shifters with low RMS phase errors are critical for improving the beamforming quality in the SATCOM application.

A uniform phased array with eight elements is utilized for the beam pattern simulation to figure out the impact of RMS phase errors on the radiation beam pattern. More than 50 trails are simulated to illustrate the detailed impact. Figure 4.3 presents the impact of 5° RMS phase error across eight elements on sidelobe level. The red curve represents the ideal case without any phase errors between each element, and the gray curve indicates the beam pattern results with random phase errors. From this figure, to maintain a -10 dBc sidelobe level with acceptable amplitudes for unwanted RF signal, the RMS Phase error should be kept lower than 5°.

The mentioned simulated beam pattern results are with the phase error only. In the actual case, the impact of the amplitude error should also be considered. In other words, the desired beam pattern will be further degraded by the amplitude error. Consequently, to keep the sidelobe level lower than -10 dBc, the RMS phase error for the phase shifter should be designed with more margins.

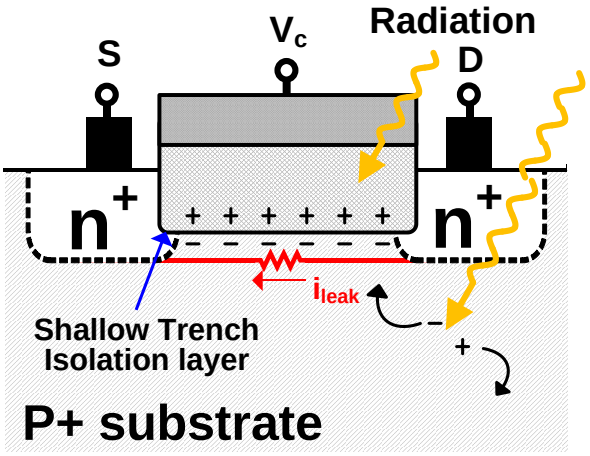


Figure 4.4: The influence of comic ray to the CMOS transistor.

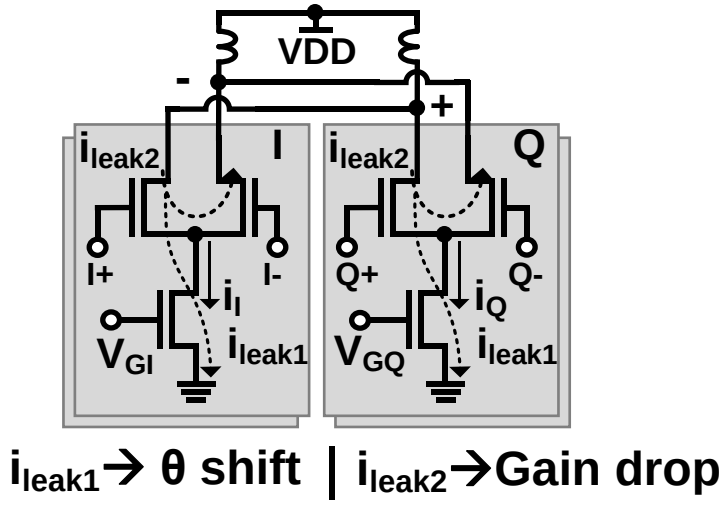


Figure 4.5: The influence to vector-summing phase shifter by the total ionizing dose

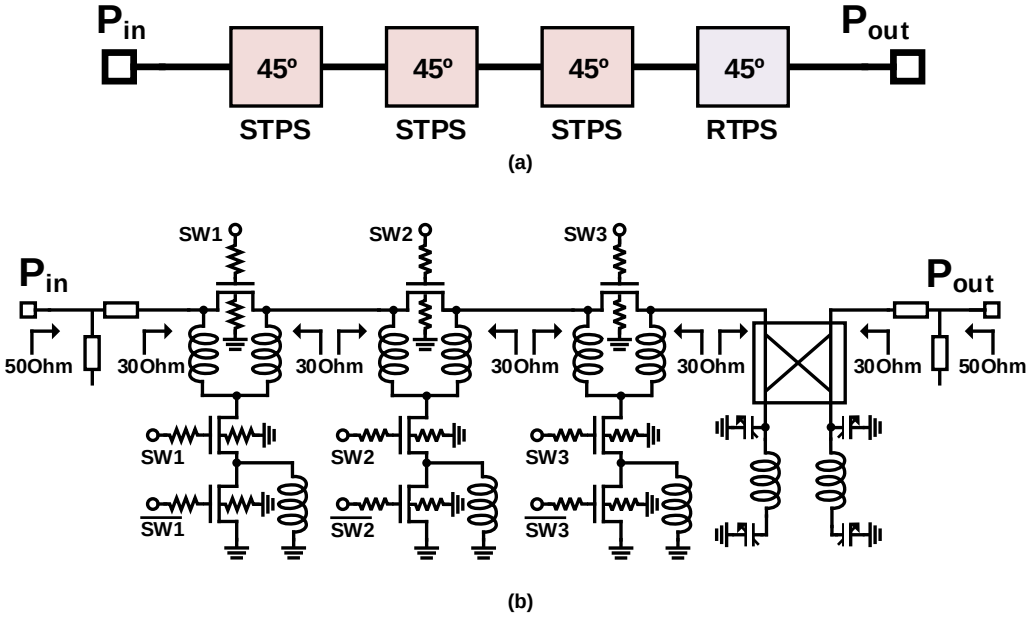


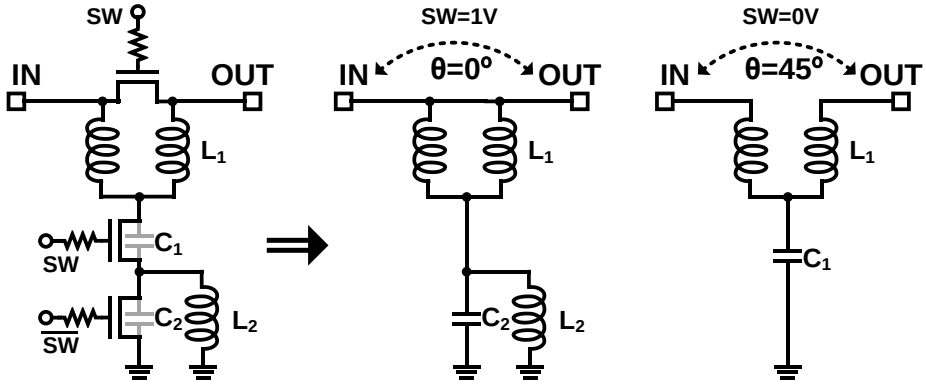
Figure 4.6: (a) Conception of the proposed hybrid phase shifter and (b) proposed detailed circuit schematic of the phase shifter with a nonuniform matching technique.

4.1.3 Effect of TID

As shown in Fig.4.4, the TID will cause leakage current effects on the CMOS transistor for the advanced CMOS process. Fig.4.5 represents the TID influence on the vector-summing phase shifter. From this figure, typically, there will be two leakage currents induced by the cosmic ray: the leakage current one and the leakage current two.

The leak current one is the current from the output of the vector-summing port to the ground. The current will influence the output phase at the same bias setting, especially when I or Q paths are biased at 0 volts for 0degree and 90degree phase shifting.

The leak current two is the current between the output plus and output minus ports. From this figure, we can quickly figure out that this current's existence will induce the amplitude gain degradation. Thus leakage current one and leakage current two will cause the phase shifter phase and gain degradation. The degradation is the main contribution to system TID tolerance performance.



For Δθ=45°:

$$L_1=\frac{Z_0}{\omega}\tan\left(\frac{\Delta\theta}{2}\right) \quad L_2=\frac{1}{C_2\omega^2} \quad C_1=\frac{\sin(\Delta\theta)}{Z_0\omega} \quad C_2=\frac{2L_1}{Z_0^2}$$

Figure 4.7: Working principle of the proposed coarse STPS stage.

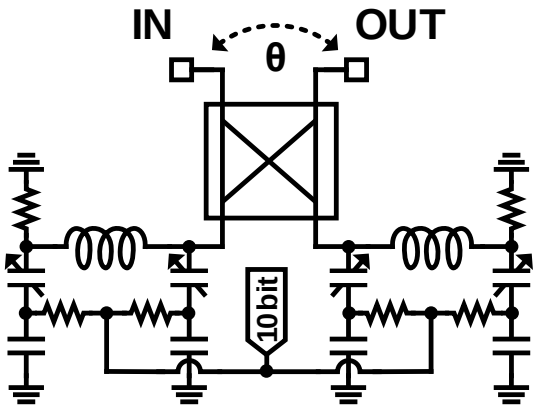


Figure 4.8: Variable capacitor implementation of the RTPS stage.

4.2 Hybrid Phase Shifter

4.2.1 Hybrid Phase Shifter with Four 45° Stages

Figure 4.6(a) illustrates the proposed low-insertion-loss and high-resolution hybrid phase shifter with a nonuniform matching technique. As mentioned in Section 1, for the same coverage, the insertion loss of STPS is small than RTPS without considering the resolution. To reduce the total signal insertion loss, the first three stages are composed of three identical 45° STPS stages. The fourth 45° stage is an RTPS for the high-resolution fea-

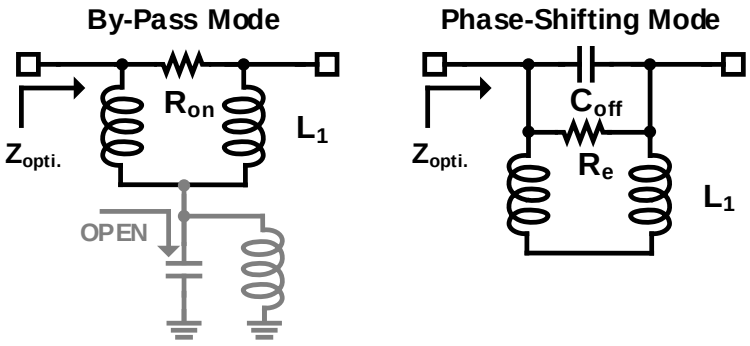


Figure 4.9: The detailed schematic of the proposed nonuniform matching equivalent circuits.

ture. Thus, the proposed hybrid phase shifter realizes the features of low insertion loss and high resolution at the same time.

Figure 4.7 shows the working principle of the coarse STPS. Those three 45° STPSs are all in typical cross-coupled bridged-T topology. The equivalent circuit of the coarse stage is shown in Figure 4.7. The 45° desired phase shifting can be obtained by switching the phase-shifting state from the by-pass mode to the T-type phase-shifting mode. To fulfill desired phase shifting (45°), the detailed design parameters C_1, C_2, L_1, and L_2 can be derived by the equations shown in Figure 4.7 [99].

As shown in Figure 4.8, the 45° RTPS includes one hybrid coupler, two LC identical reflective loads for fine-tuning. One node of variable capacitors is connected to the ground for biasing, and another node is controlled by a 10 bit DAC with 1024 phase steps. Consequently, in the ideal case, the phase resolution of the hybrid phase shifter is 0.04°. However, in the actual case, the resolution is limited by the RMS phase error, which is 0.8°.

4.2.2 The Nonuniform Matching and Body-Floating Techniques

The nonuniform matching technique is integrated with the proposed hybrid phase shifter to reduce the coarse stage insertion loss. Figure 4.9 indicates the nonuniform matching equivalent circuits. The NMOS transistor sizes are larger than the usual case. Thus, the insertion loss of by-pass mode is reduced by a smaller equivalent on resistor R_{on}. According to the first equation in Figure 4.7, compared with the standard matching value, the proposed inductor L_1 value is smaller. Due to the larger transistor size and small inductor value, the phase-shift mode Q value and equivalent shunt resistor R_e are larger and smaller than the usual case. Thus, the insertion loss of phase-shifting mode is also reduced.

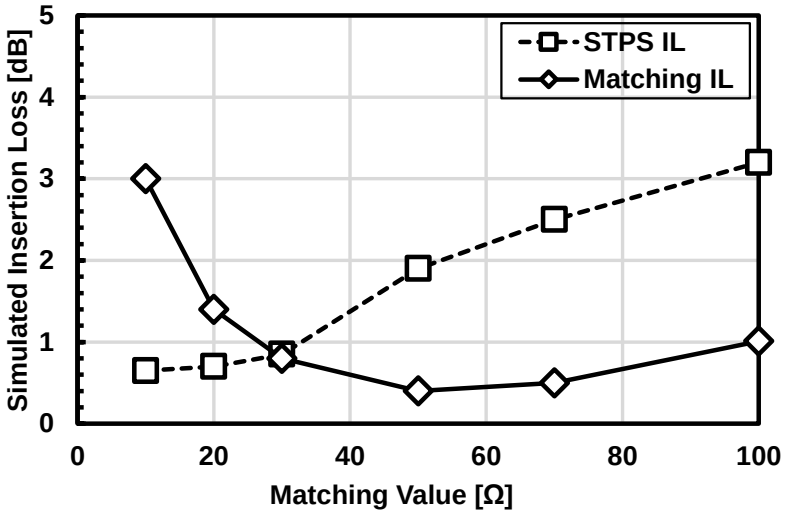


Figure 4.10: The simulated one stage STPS insertion loss and T-junction matching loss with matching target values.

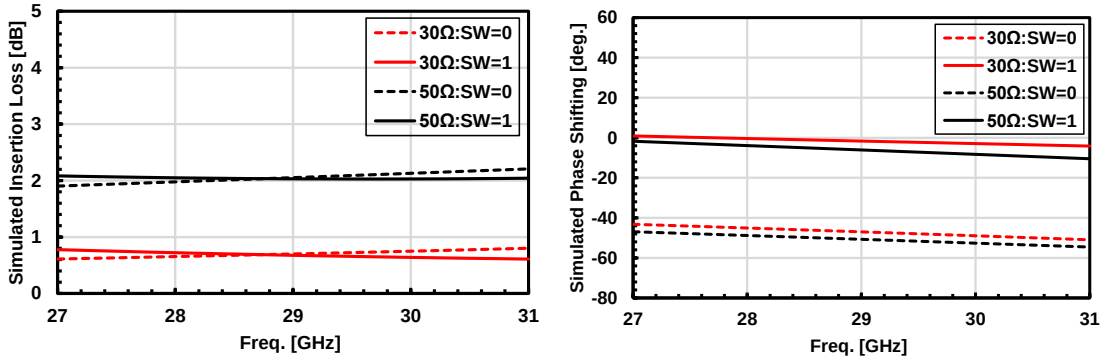
To figure out the optimized matching value of the proposed circuit with minimized insertion loss, the simulated one-stage STPS insertion loss and one T-junction matching loss are shown in Figure 4.10 with a different matching value. The one-stage STPS insertion loss increases with a higher targeted matching value. The insertion loss caused by the necessary T-junction matching decreases before 50 Ω and increases after 50 Ω. Considering the trade-off between STPS and T-junction insertion loss, a 30 Ω matching value is selected to minimize the total insertion loss.

Figure 4.11(a) and 4.11(b) represents the simulated insertion losses and phase-shifting for 30 Ω and 50 Ω matching. According to the simulated results, the proposed nonuniform matching technique dramatically reduces the one-stage STPS insertion loss, from 2 dB to 0.8 dB with the same phase-shifting value.

4.2.3 Measurement Results

The transistor gates of the coarse stage are digitally driven by three inverters to reduce the control complexity. All gate biases are provided through 10 kΩ resistors. Considering the fine-tuning stage, only one DAC bias is utilized to control the phase-shifting (another is fixed at 0 V).

The proposed hybrid phase shifter with a nonuniform matching technique in this work is fabricated in a standard 65-nm CMOS technology. The detailed die micrograph is shown in Figure 4.12. The on-chip core size of the proposed hybrid phase shifter is 0.14 mm^2.



(a) (b)

Figure 4.11: The simulated one stage insertion loss (a) and phase shifting (b) with30 Ω and 50 Ω matching techniques.

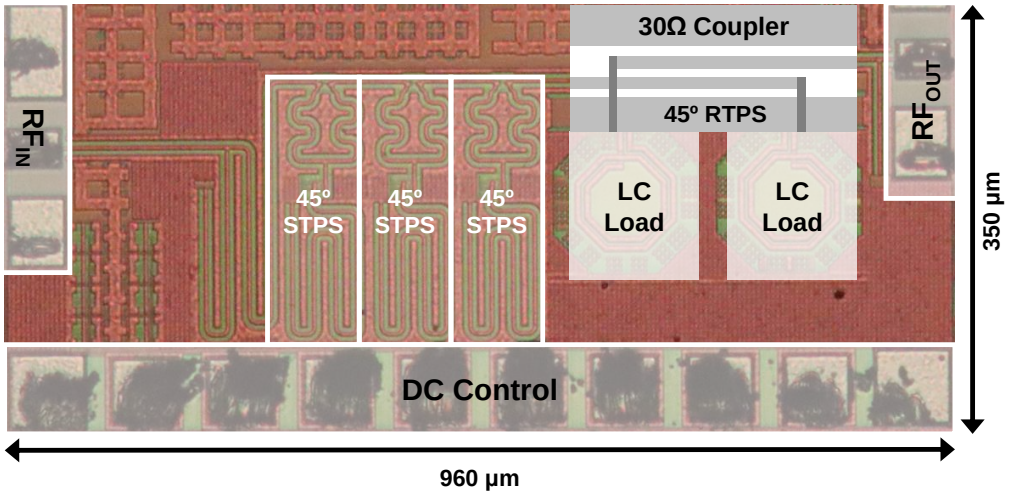


Figure 4.12: The proposed hybrid phase shifter die micrograph.

As shown in Figure 4.13, the proposed hybrid phase shifter performance is measured on a probe station with a 25 °C ambient temperature. The S-parameters of port IN and OUT are measured by a vector network analyzer (Keysight N5247A) with input and output GSG RF probes. The power supply of the inverter buffers is provided by a DC power analyzer (Keysight N6705A). The STPS and RTPS control signals are generated by a parameter analyzer (Keysight 4175B).

Three STPSs phase-shifting responses are measured by the same mentioned setup with different switch bias states. Figure 4.14(a) shows the detailed measured values for each STPS stage. According to this figure, the cover range of three coarse STPSs is 135°

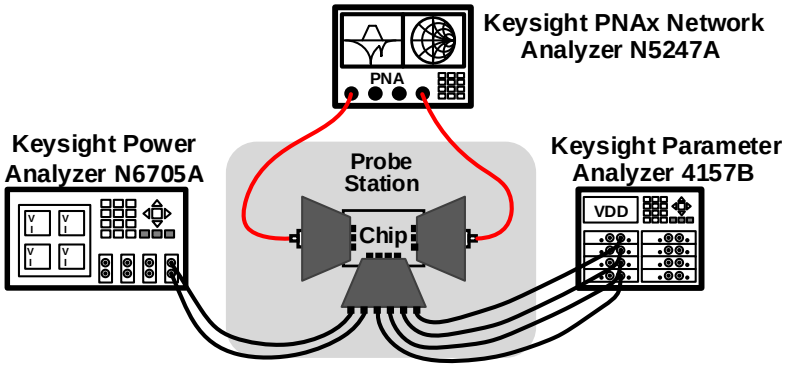


Figure 4.13: The illustration of the on-wafer measurement setup for the proposed hybrid phase shifter.

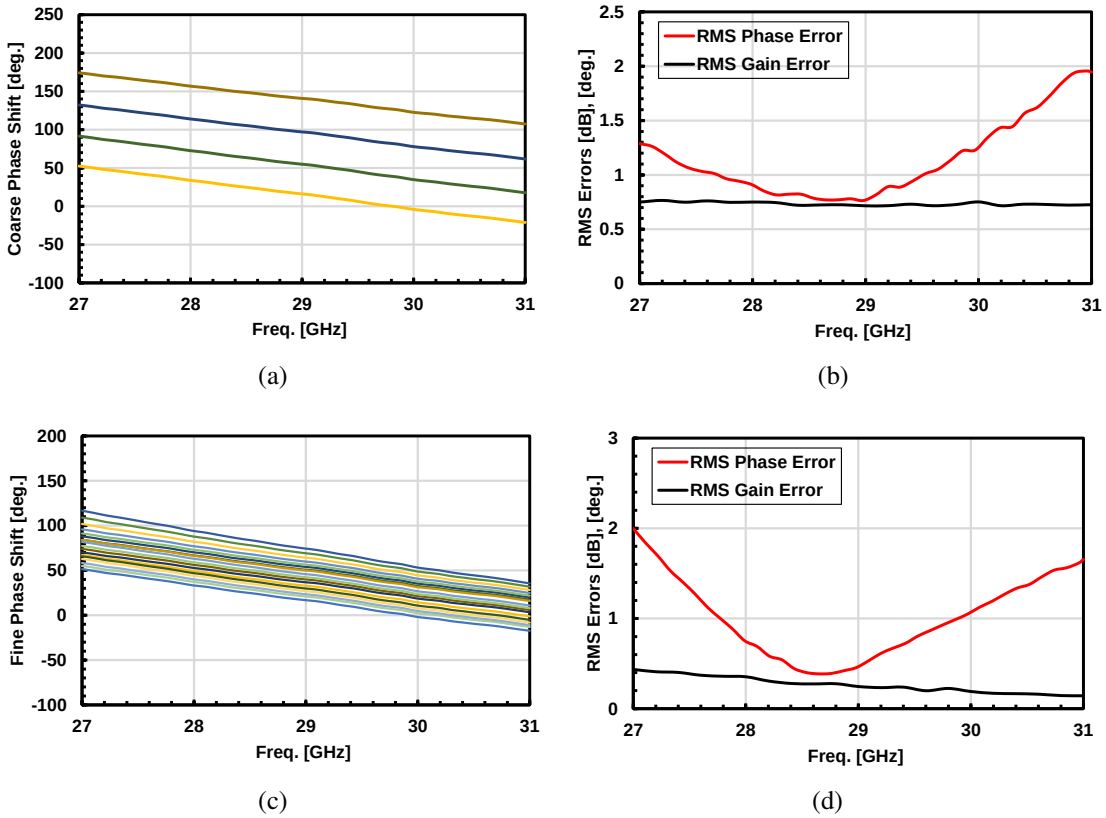
at 29 GHz, and each STPS has a phase step of 45° at 29 GHz. Figure 4.14(b) represents the measured average RMS gain and phase errors for all coarse phase states within the frequency from 27 GHz to 31 GHz. According to this figure, at 29GHz, the measured RMS gain and RMS phase errors are 0.7 dB and 0.8°, respectively. From 27.5 GHz to 30 GHz (the FCC SATCOM uplink frequency allocation), the measured RMS gain and phase errors are less than 0.8 dB and 1.3°, respectively.

To further demonstrate the fine-tuning stage performance, the phase-shifting response and the average RMS gain and phase errors for all phase states are shown in Figure 4.14(c) and Figure 4.14(d). The fine-tuning phase coverage is 55°. Compared with conventional dual-voltage control methods, the proposed fine-tuning stage reduces the control complexity with only one DAC voltage source. According to Figure 4.14(d), the measured RMS gain and phase errors are 0.3 dB and 0.4° at 29GHz. The proposed fine-tuning stage maintains RMS gain and phase errors less than 0.3 dB and 1.2° within the mentioned FCC frequency range from 27.5 GHz to 30 GHz.

As shown in Figure 4.16, the average insertion loss of all phase-shifting states is 8.5 dB. Figure 4.15(a) and Figure 4.15(b) illustrate the measured input and output return loss against the frequency. According to the figures, the S11 and S22 are less than -12 dB from 24 GHz to 34 GHz.

4.3 Magnetic Tuning Phase Shifter

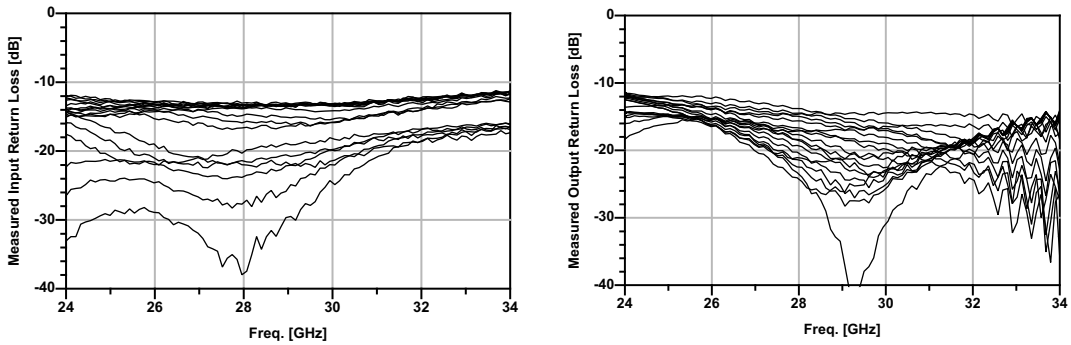
Fig.4.17 illustrates the proposed magnetic-tuning phase shifter core. One MTPS core is composed of three-coupling coils. Two coils are connected with the switch capacitor tank and input-output matching block. Another coil is connected with a CMOS resistor, which



(a) (b)

(c) (d)

Figure 4.14: Measured coarse stage phase shifting response (a), measured coarse stage RMS gain and phase errors (b), measured fine-tuning stage phase-shifting response (c), and measured fine-tuning stage RMS gain and phase errors (d).



(a) (b)

Figure 4.15: Measured S11 (a) and measured S22 (b) with sweeping the coarse sand fine-tuning stages.

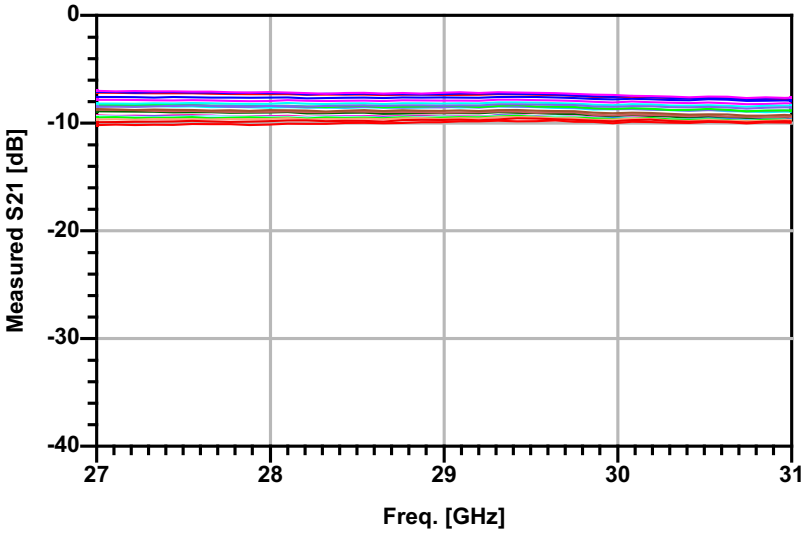


Figure 4.16: Measured S21 with sweeping the coarse and fine-tuning stages.

is implemented by NMOS transistor. By adjusting the variable voltage control of the CMOS resistor, the equivalent of the resistor will change accordingly.

Fig.4.18 shows the proposed magnetic-tuning phase shifter working principle and the simulated waveform of port IN and port ISO. In terms of the coarse-tuning core, the proposed part is served as a conventional reflective-type phase shifter, which the output phase (ISO port) is decided by the impedance of the reflective load (THR port and COU port). The switch capacitor tank can adjust the phase steps. The coarse tuning stage also helps to relieve the coverage of the fine-tuning phase shifter range.

As shown in Fig4.19, the fine tuning range is implemented by the three coil tank. The simulated waveforms of port IN, OUT, and RES are also shown in the same figure. The input signal current equals the induced current plus the tuning current. The variable resistor controls the tuning current. By adjusting the variable resistor, the tuning current will change simultaneously, and thus, the induced current will also change. From the simulated waveform, the we can easily figure out the port OUT waveform is decided by the port RES. Then the output phase will be changed owing to the different induced currents.

Fig.4.20 shows the intrinsic reason for the radiation hardness feature of the magnetic tuning phase shifter. According to this figure, the first two coils are connected by a switch capacitor tank, and there is no leak current between the MOM capacitor and the ground. Thus they are radiation hardness. In terms of the third coils with NMOS resistor for the variable resistor. The i_{ds} current after radiation is equal the leakage current plus the i_{ds} current before the radiation.

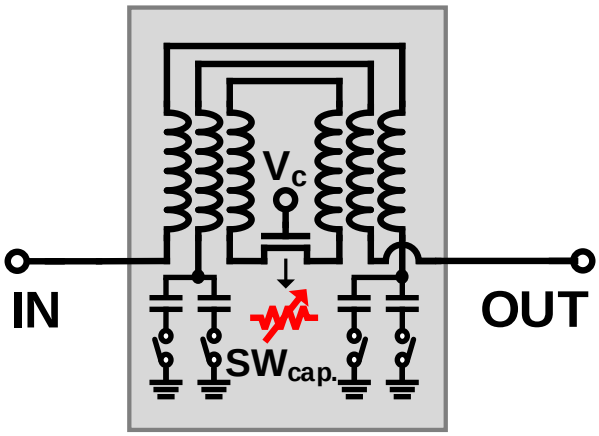


Figure 4.17: The detailed schematic of the proposed magnetic-tuning phase shifter core.

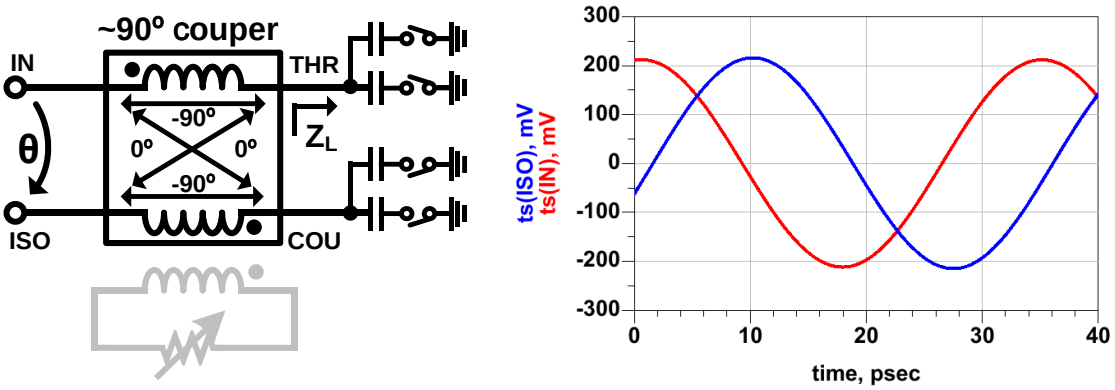


Figure 4.18: The working principle of coarse tuning core and fine tuning core.

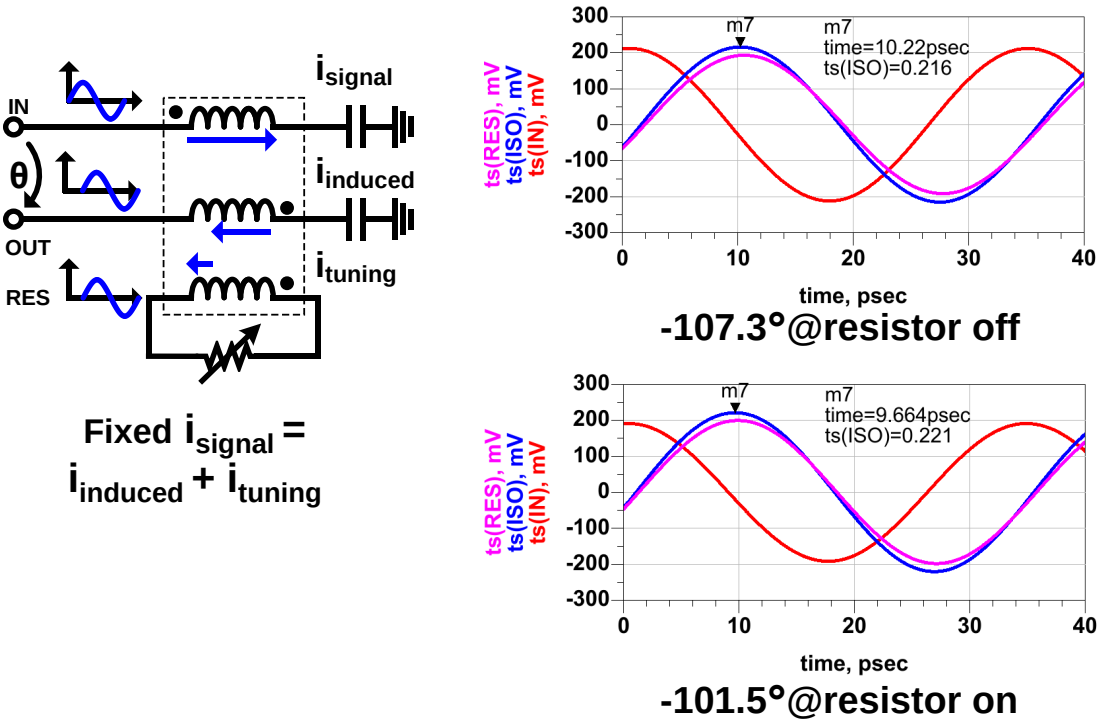


Figure 4.19: The working principle of coarse tuning core and fine tuning core.

The black and red lines in the same figures represent the i_{ds} current before the radiation and after radiation. At the variable resistor region, the current after the radiation is almost equal to the current before the radiation, and thus the proposed circuit is radiation hardness. The detailed measurement TID tolerance results of the proposed magnetic-tuning phase shifter based will be shown in the next chapter.

The measurement of single-element phase shifter phase response is shown in Fig.4.21. From this figure, the proposed phase shifter is capable of covering 360° (180° from the buffer and 214° from MTPS) when sweeping Vc and switch registers.

The measured results of RMS gain and phase errors are shown in Fig.4.22. From 27GHz to 31GHz, the RMS gain and phase errors can maintain lower than 0.2dB and 0.5degree. To be specific, at the center frequency of 29GHz, the single-element RMS gain/phase errors and resolution are 0.14dB/0.09° and 0.09°(limited by phase error), respectively.

The measurement insertion loss results of the proposed magnetic-tuning phase shifter are shown in Fig.4.23. The measured result is the standalone phase shifter TEG value with the insertion loss of input and output matching. From this figure, the average insertion loss from 27GHz to 31GHz is around -9dB.

To further evaluate the magnetic-tuning phase shifter temperature performance, the

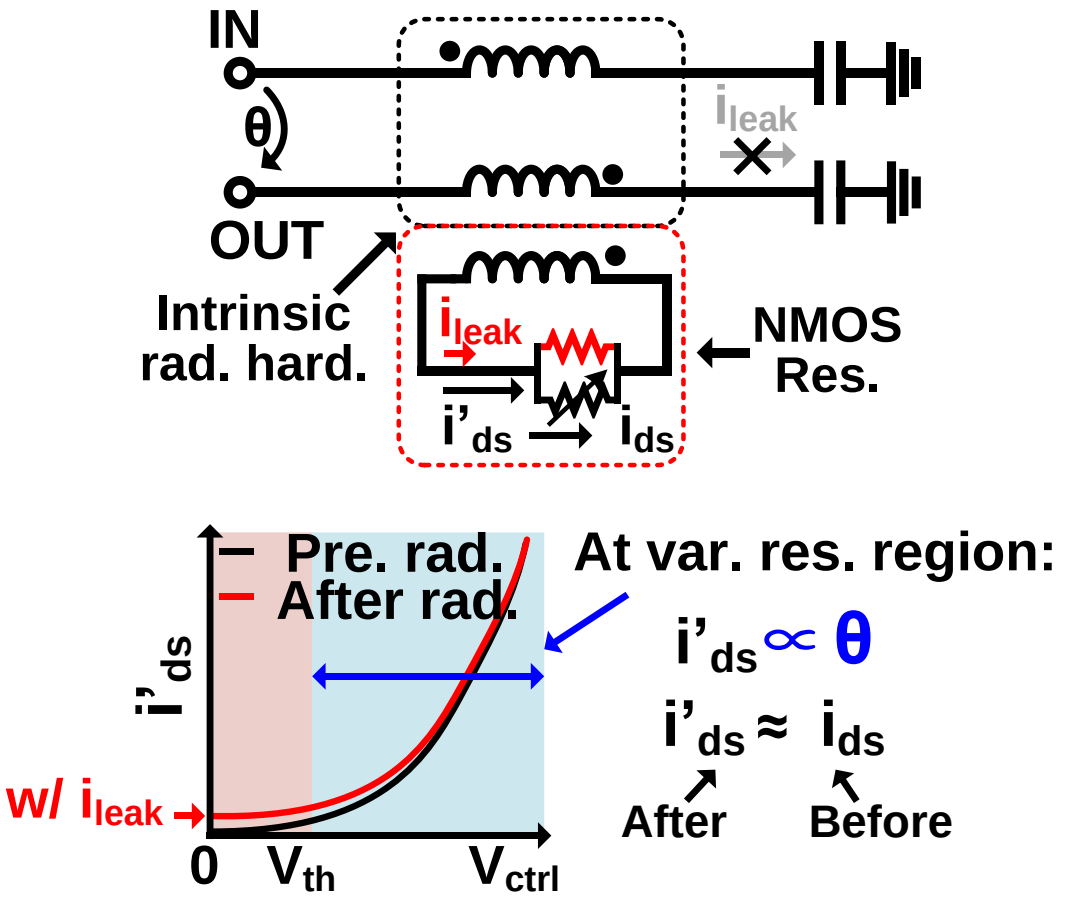


Figure 4.20: The intrinsic reason for the radiation hardness feature of the magnetic tuning phase shifter.

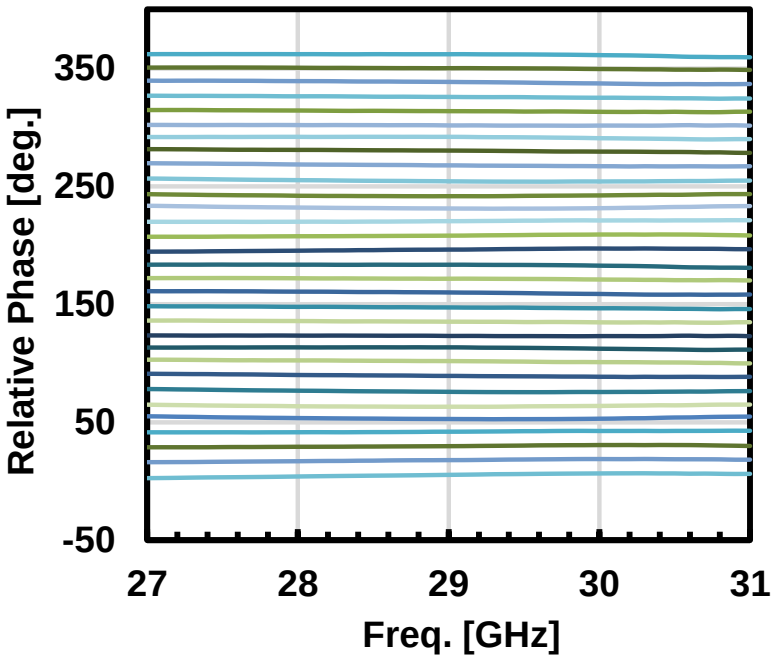


Figure 4.21: The phase response of the proposed single-element front-end.

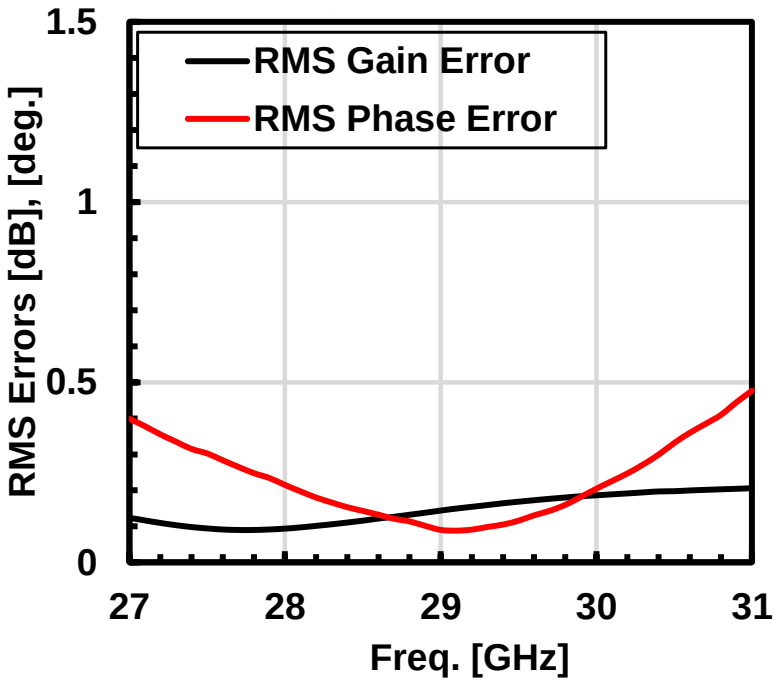


Figure 4.22: The measured results of RMS gain and phase errors.

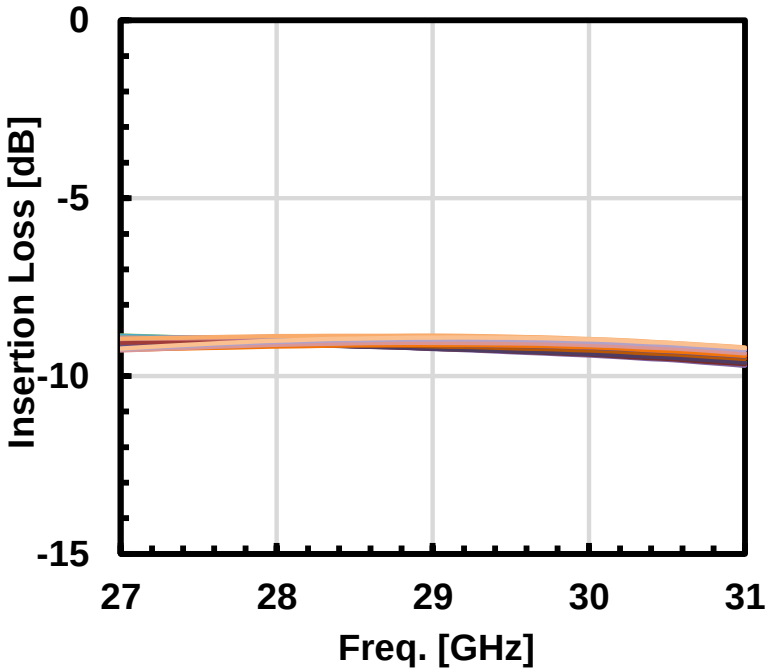


Figure 4.23: The measurement insertion loss results of the proposed magnetic-tuning phase shifter TEG.

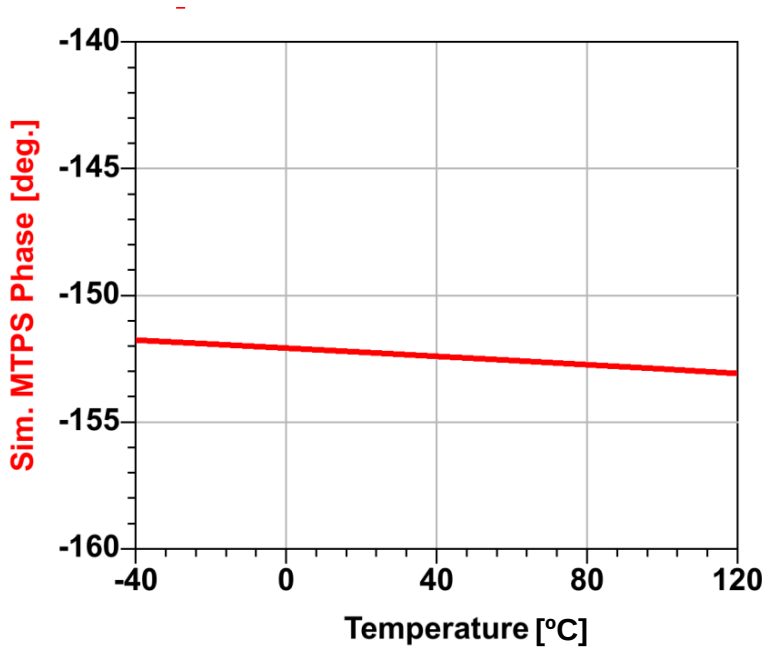


Figure 4.24: The simulated result of the proposed MTPS temperature performance.

simulated results of the proposed MTPS temperature are shown in Fig.4.24. From this figure, the phase variation is only 1.4degree from -40°C to 120°C. The process variations should also be considered (calibration) in this work for high-accuracy beam steering.

4.4 Conclusion

Conventional switch-type phase shifters cannot support high accurate beamforming owing to the limited phase resolution for phase shifters. The higher stage for higher resolution will induce many insertions too.

Conventional vector-summing phase shifters need more power to support two additional amplifier gains. The linearity performance is still not very good owing to the existence of two amplifier cores based on active CMOS transistors.

The conventional reflective-type phase shifter is suitable for power consumption. However, the temperature performance of and controlling mechanism is not very good compared with the proposed magnetic-tuning phase shifter. Thus, we use the proposed magnetic-tuning-based phase shifter for the trade-offs between linearity, power consumption, temperature performance, and controlling accuracy in this work.

Chapter 5

Phased-Array Receiver for Satellite Terminal

This chapter introduces the satellite terminal side receiver of the proposed satellite communication network. As mentioned in Chapter2, the design requirements of the satellite terminal side are more critical than requirements in the ground base station side.

Among all the requirements, the most important two are the low power consumption and high radiation hardness at the circuit design level. This chapter will show detailed information on this phased-array receiver for those two mentioned requirements.

Firstly, this chapter will present information about the two considerations. Secondly, the detailed architectures include mutually coupled inductors-based LNA, Neutralized Buffer with a 180degree build-in phase shifter. Finally, the single element measurement results and the system beam pattern will be shown in this chapter.

5.1 System Considerations of Phased-Array Receiver

Aa shown in Fig.5.1, the proposed phased-array receiver for future 6G communication network is composed by 8 path front-end with LO phase-shifting structure [100–105]. One RF front-end includes two stages of mutually coupled inductors-based LNA, one stage RF buffer with a 180-degree build-in phase shifter, magnetic-tuning based phase shifter. After one path front-end, the RF signal is processed by a lumped 8:1 Wilkinson combiner. An RF amplifier is added to this receiver's end to mitigate the insertion loss influence at the transmission lines.

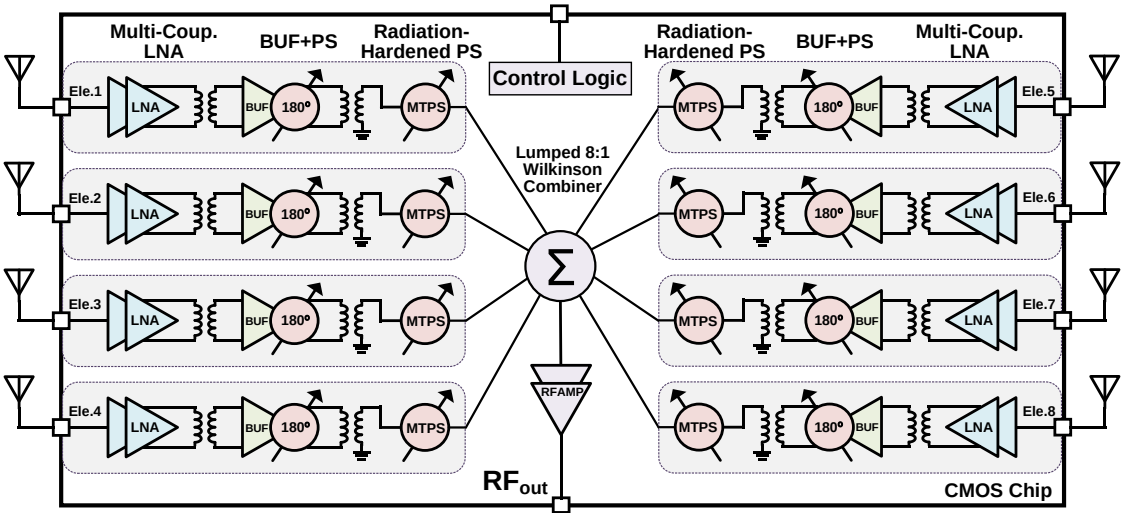


Figure 5.1: The phased-array receiver block diagram for the future 6G satellite communication network.

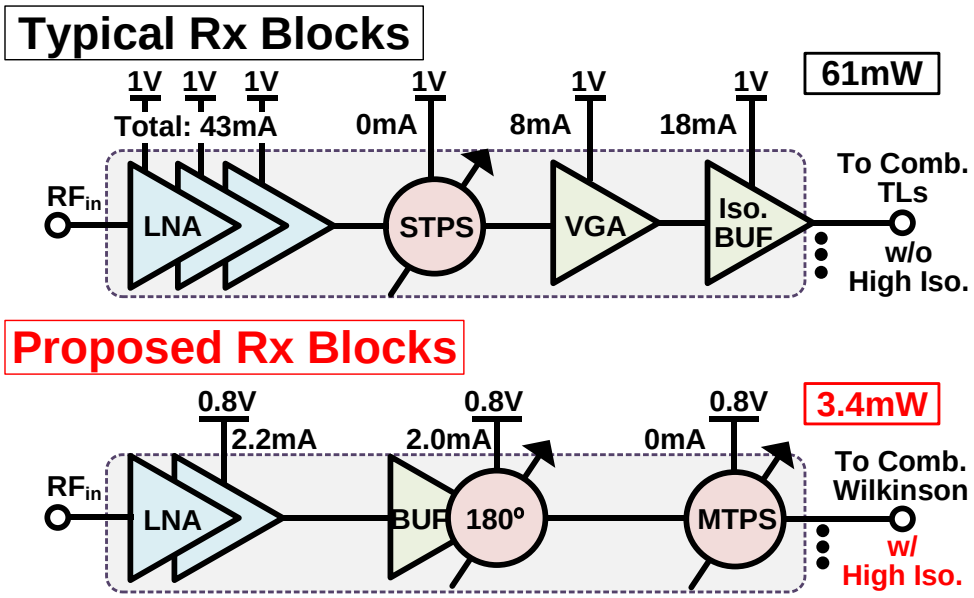


Figure 5.2: The power consumption difference between typical receiver blocks and proposed blocks.

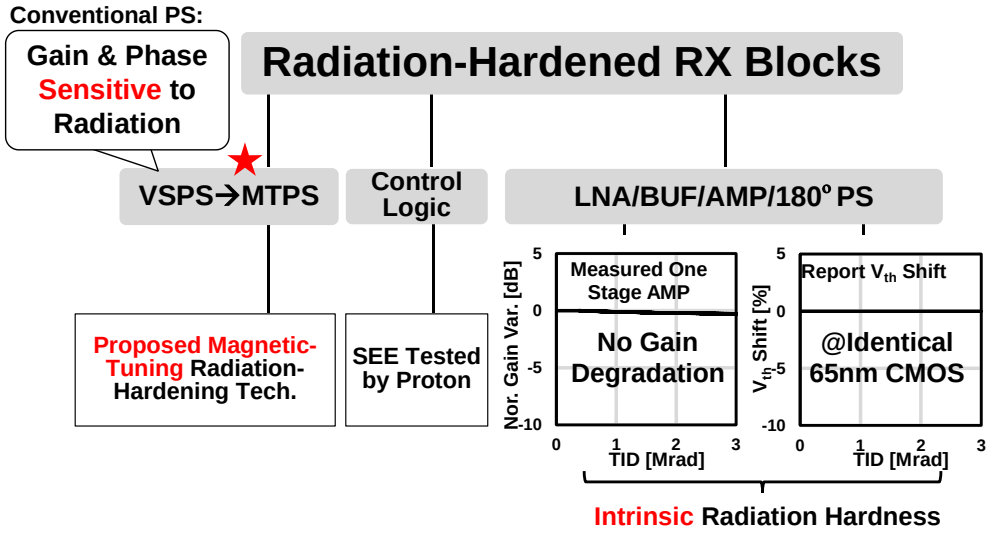


Figure 5.3: TID Tolerance analysis for different blocks in this proposed work.

5.1.1 Power Consumption Weights

Fig.5.2 represents the power consumption between typical phased-array receiver blocks and the proposed one. The main power consumption block is the LNA in terms of conventional phased-array receiver blocks. A passive phase shifter is inserted in the front-end block for phase controlling and a variable gain amplifier for system gain step controlling. After the variable gain amplifier, the isolation buffer is added to this block to mitigate the transmission-based combiner influence.

Considering the proposed phased array blocks, the power consumption of LNA is decreased to 1.8mW by the mutually coupled inductors technique. The RF signal then passes the neutralized buffer with a built-in 180-degree phase shifter. Like the conventional block, the beam angle is controlled by the passive phase shifter called the magnetic tuning phase shifter.

Noted that the existence of a lumped 8:1 Wilkinson combiner, the passive phase shifter can be directly connected through the Wilkinson combiner. The >20dB isolation between each combiner port can eliminate the phase shifter influence when controlling the beam angle.

5.1.2 TID Tolerance Weights

Another critical issue mentioned before is the radiation hardness. Considering the radiation hardness, typically, there are two main effects on the CMOS circuit: the single event

effect and the total ionizing dose. Owing to the lack of digital circuits, the primary influence of the RF circuits is the TID. In this section, we will mainly talk about the effect of the TID.

Fig.5.3 shows the detailed analysis of the system TID weight considerations. The Vth is constant (around 0.5% difference) for 3Mrad TID in terms of the LNA and buffers block. Thus, the gain and phase degradation caused by LNA and buffer is negligible in the proposed phased-array receiver.

This figure also shows the measured gain degradation results of one stage power amplifier, and the result shows the gain keeps the same for the 3Mrad TID value. However, according to the analysis in chapter 4, the conventional vector-summing phase shifter is sensitive to TID, and other types of phase shifters are not suitable for this work.

Thus, this proposed magnetic-tuning radiation hardening technique can realize high TID tolerance performance by implementing the proposed magnetic-tuning passive phase shifter. So, the total system TID tolerance feature can be increased by the proposed magnetic-tuning phase shifter.

5.2 Mutually Coupled Inductor Based LNA and Neutralized Buffer

5.2.1 Mutually Coupled Inductor Based LNA

As mentioned before, the power consumption of a phased-array receiver for the satellite terminal is a critical design requirement. Among all the blocks inside the receiver diagram, the power consumption of LNA dominates the system performance.

Fig.5.4 shows the detailed mutually coupled inductors base common gate (CG) LNA. The input transistor is designed as a conventional common gate amplifier for high bandwidth features. The proposed mutually coupled inductor based CG LNA dramatically decreases the source input impedance compared with the inductor-based CG LNA. Hence, the required transistor width is further reduced.

The mutually coupled inductor layout is also shown in this figure. From this figure, the mutually coupled inductor tank is composed of Lg, Ld, and Ls, forming mutual-inductance Msg, Mds, and Mgd.

The schematic for detailed analysis is shown in Fig.5.5. When all inductors are resonated by their capacitors, the input impedance can be written as the following equation:

$$Z_{\text{in}} = g_{\text{m}} \| (N_{\text{ds}}^2 * K_{\text{ds}}^2 * R_{\text{equ.}}) \tag{5.1}$$

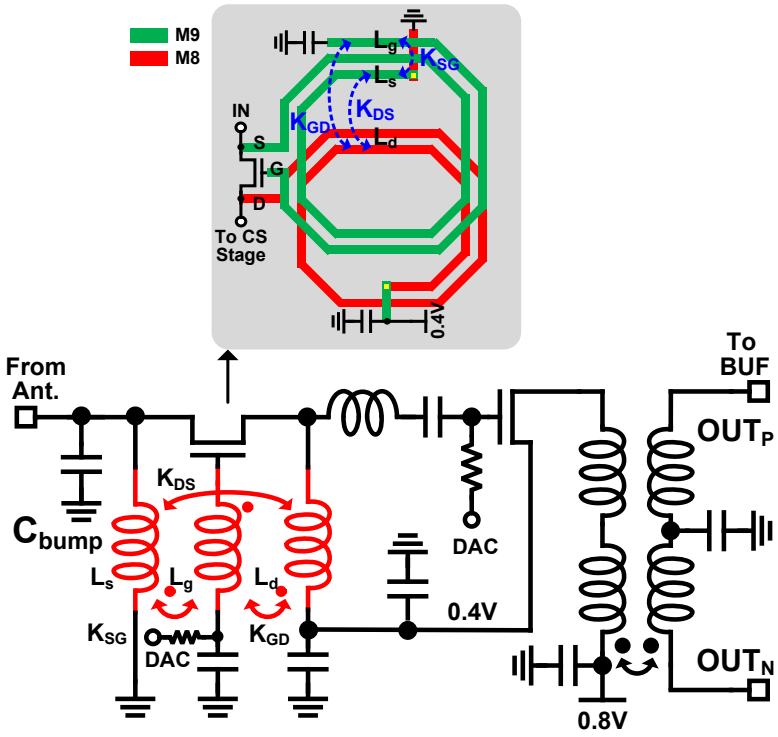


Figure 5.4: The detailed mutually coupled inductor based LNA and its input balun layout.

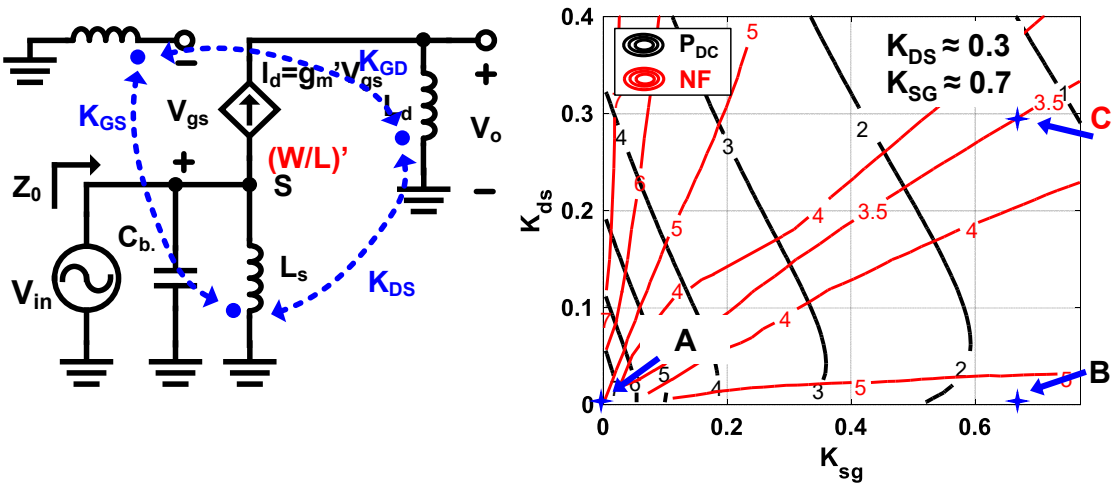


Figure 5.5: The detailed schematic for analysis and the simulated power consumption versus mutually coupled values.

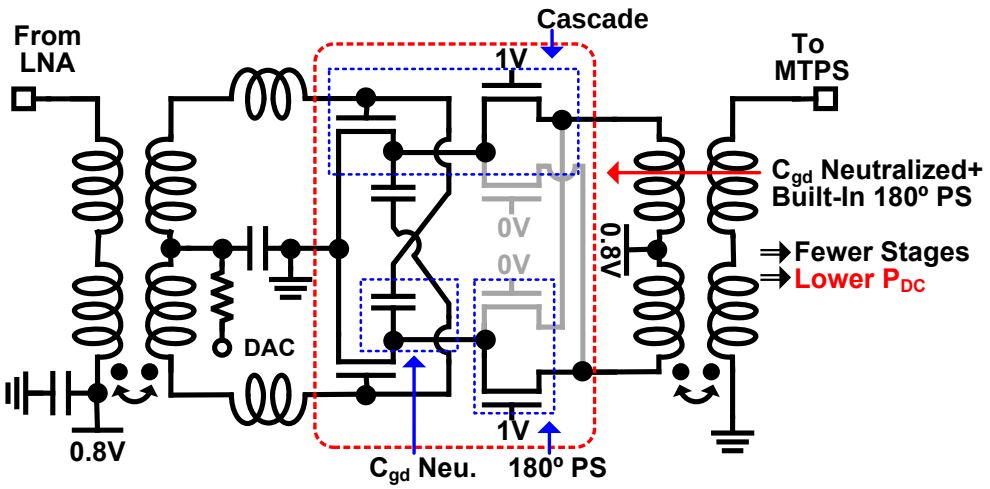


Figure 5.6: The schematic for the proposed neutralized buffer with a build-in 180° phase shifter.

The $R_{eua.}$ is the impedance value looked at from the third inductor coils. By implementing the mutually coupled inductors mentioned before, the input impedance can be reduced, and thus, the smaller transistor can be utilized for an optimized matching value. For the same operation region in the transistor, the power consumption can be represented as following:

$$P_{\mathrm{DC}} = \frac{\mathrm{V_{dd}}}{2} * \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{ox}} * \frac{W}{L} * (V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \tag{5.2}$$

Thus, the power consumption can be dramatically decreased by a smaller implemented transistor size.

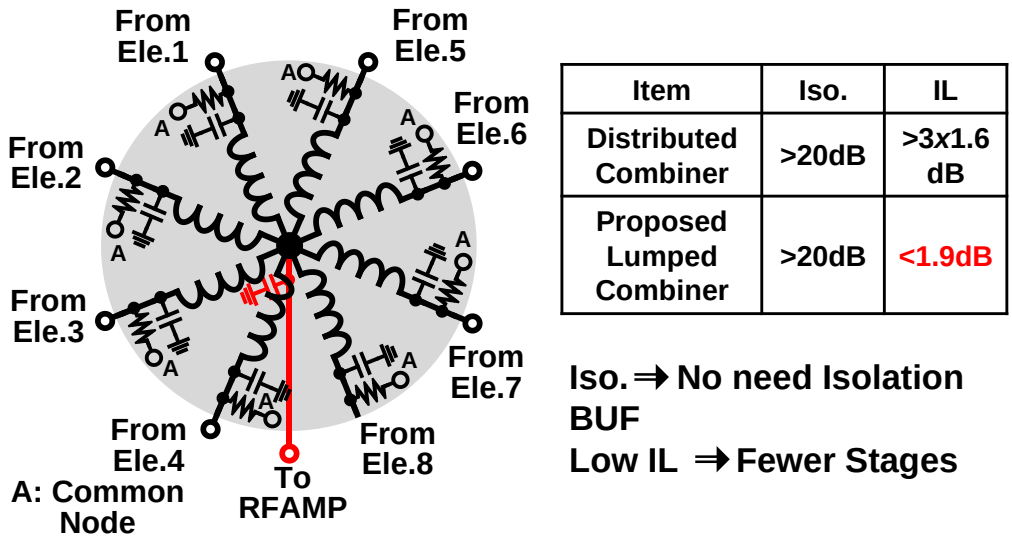
As shown in Fig.5.5, the simulated power consumption with and without a mutually coupled inductor tank is 1.8mW (Point C) and 7mW (Point A), respectively.

5.2.2 Neutralized Buffer

The Cgd neutralized cascade buffer with a built-in 180° phase shifter is also introduced to reduce the receiver power consumption further. As shown in Fig.5.6, the neutralized buffer is based on a cascade stage amplifier, and the second transistors are utilized for a 180-degree phase shifter.

Two neutralized capacitors are inserted between the first transistor input port and the second transistor input port to increase the buffer power gain. Two standalone inductors are also added at the gate of the first transistor for higher gain.

Compared with the conventional cascade buffer with an external 180° phase shifter



Item	Iso.	IL
Distributed Combiner	>20dB	>3x1.6 dB
Proposed Lumped Combiner	>20dB	<1.9dB

Figure 5.7: The lumped Wilkinson power combiner schematic and the measured insertion loss.

and without Cgd neutralized capacitor, the proposed low-power buffer is configured with a built-in full-symmetric 180° phase shifter with negligible insertion loss. Thus, the required power-consuming buffer stages can be reduced, which contributes to saving layout area and power consumption.

5.3 Lumped Wilkinson Combiner and Magnetic-Tuning Phase Shifter

5.3.1 Lumped Wilkinson Combiner

As mentioned before, to minimize the single-element insertion loss and save the power consumption, the isolation buffer between the magnetic-tuning phase shifter and combiner is deleted in the system diagram. However, the lack of isolation buffer brings the isolation issue between different paths of the phase shifter.

The proposed lumped combiner utilizes the Wilkinson structure for port-to-port isolation to keep a good insertion loss as the transmission line-based combiner. As shown in Fig.5.7, the lumped Wilkinson combiner is composed of eight identical C-L-C elements, which provide the power combiner and port-to-port isolation at the same time.

The receiver signals from beamforming elements are implemented in a single-ended configuration. By implementing the lumped Wilkinson combiner, the system can suppress

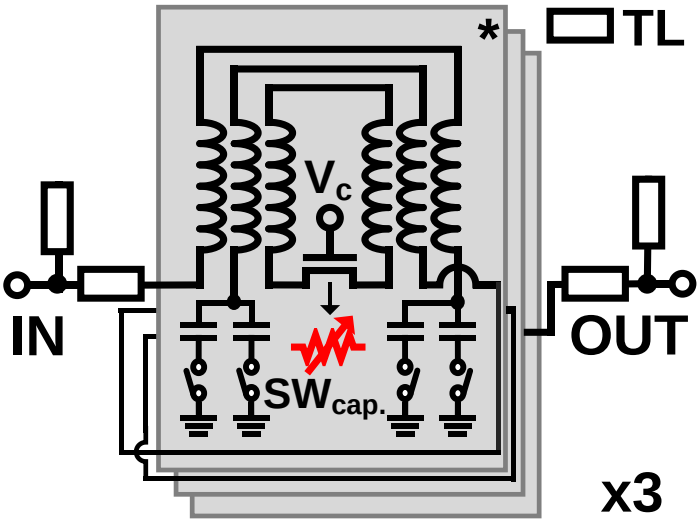


Figure 5.8: The detailed magnetic-tuning phase shifter with three identical cores and input-output matching blocks.

the influence of impedance variation caused by the phase tuning without an extra power-consuming buffer stage.

Fig.5.7 also shows the comparison between the distributed transmission line-based combiner and the proposed lumped Wilkinson power combiner. Compared with the conventional one with a transmission line-based power combiner with $3\times1.6dB$, the proposed one succeeds in 1.9dB insertion loss.

5.3.2 Magnetic-Tuning Phase Shifter

As mentioned in chapter 4, the magnetic-tuning phase shifter can help the high-resolution beam steering and high radiation hardness feature. The Fig.5.8 represents the schematic of the proposed magnetic-tuning phase shifter with three identical MTPS cores.

The detailed information on the MTPS core is already shown in Chapter 4, and the input-output matching circuits are based on the conventional transmission line for accurate circuit simulation. The measurement results of system radiation hardness are shown in the next section.

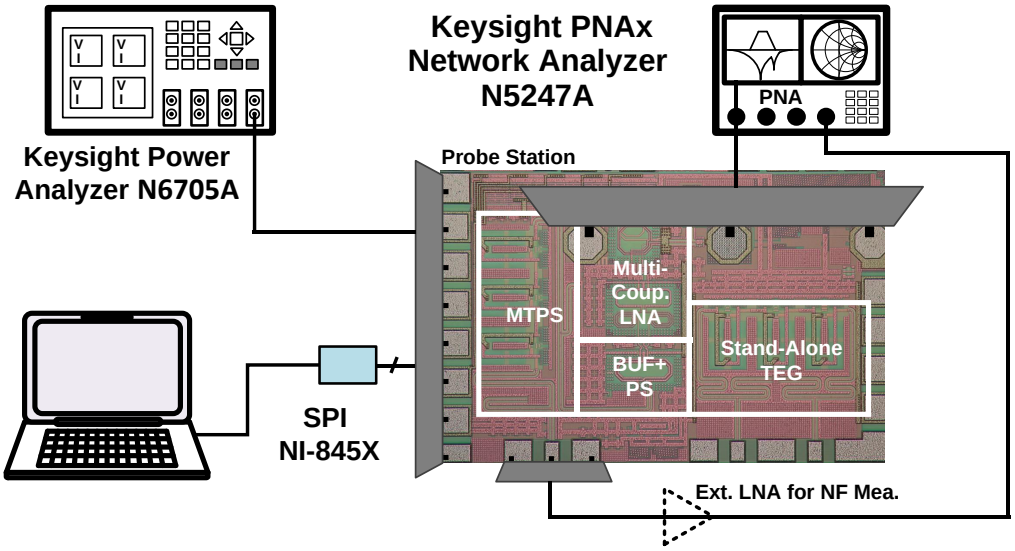


Figure 5.9: The setup for single element front-end measurement.

5.4 Measurement Results

To illustrate the system performance, two types of measurements are implemented in this work: the on-wafer single-element measurement and the phased-array system performance on PCB. This section will introduce two types of measurement with detailed implementation and results.

5.4.1 Single-Element Performance

Fig.5.9 represents the single-element setup for measurement results. The power consumption is provided by the Keysight power analyzer N6705A and the SPI DAC and switch is controlled by an external mobile computer. The input and output ports are connected with a network analyzer with a GSG 350um input probe and GSG 100um output probe.

In terms of noise figure measurement, to reduce the influence of the output GSG 100um probe, one external low noise amplifier is added at the output of the multi-coupling phase shifter for high chain gain features.

As shown in Fig.5.10, the single-element IM3 and SNDR are calculated with 400MHz signal bandwidth. At 29GHz, the peak SNDR is 40dB when the average input power is -44dB. The main tune of output power and calculated output noise floor are also shown in the same figure. The maximum SNDR can be further improved with small signal bandwidth.

Fig.5.11 shows the measured single-element S-parameter results with a network ana-

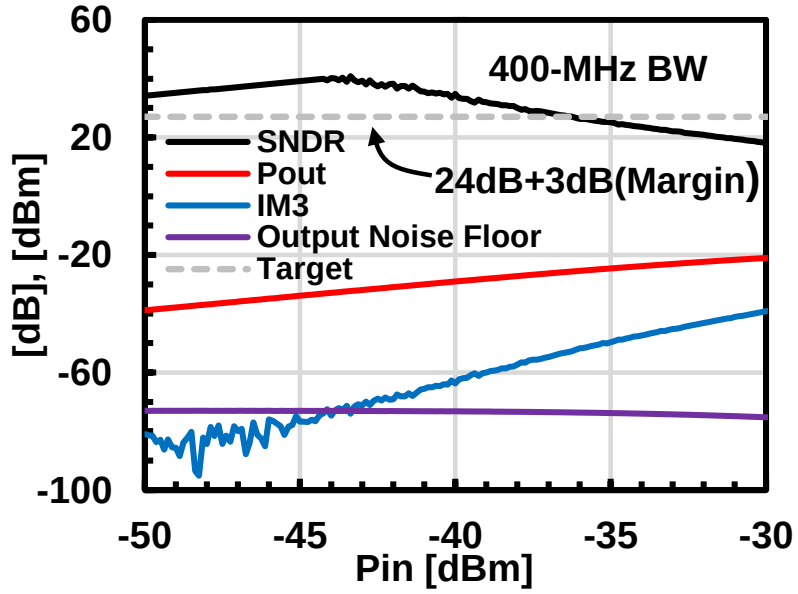


Figure 5.10: The measurement results for single-element IM3 and SNDR in 400MHz Bandwidth.

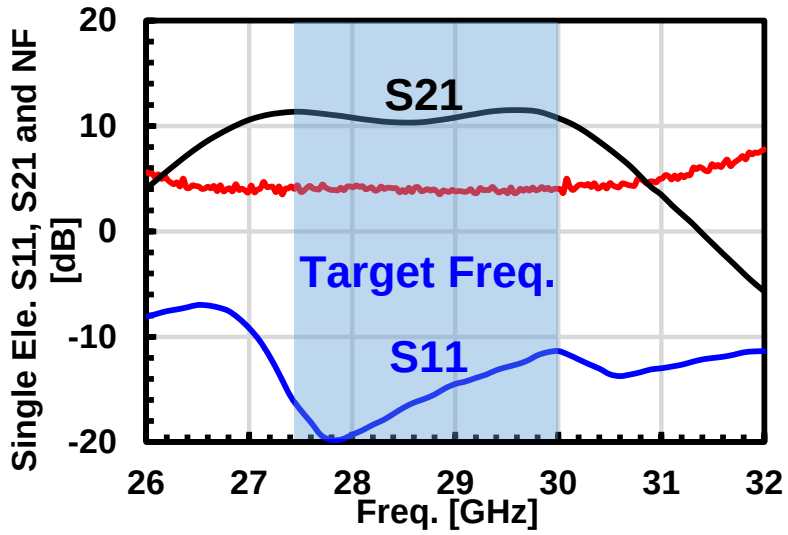


Figure 5.11: The measured S-parameter in single-element results.

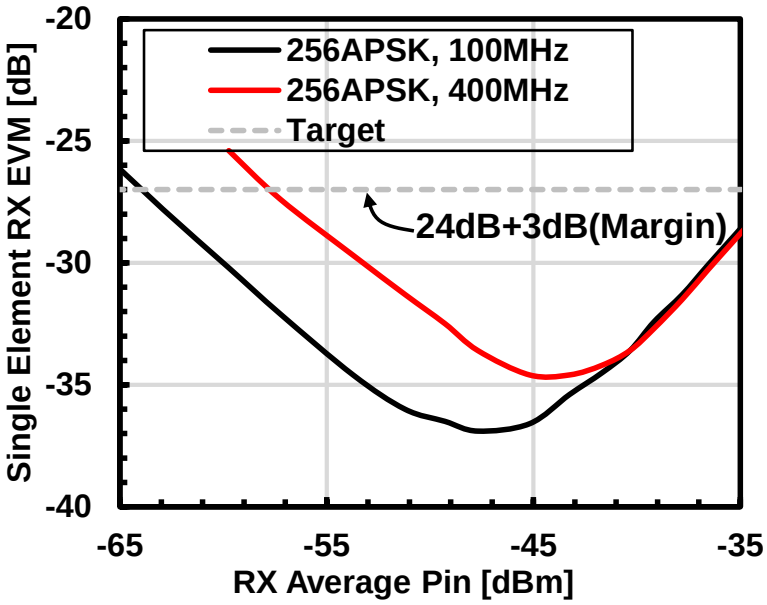


Figure 5.12: The on-wafer single-element EVM measurement results for 100MHz and 400MHz.

lyzer. According to the figure, the measured single-element S11, S21, and noise figures at 29 GHz are -14dB, 11dB, and 3.8dB, respectively. The measured 3-dB bandwidth is within 26.7GHz to 30.4GHz, which covers the 27.5GHz to 30GHz frequency band for the satellite communication uplink.

To further evaluate the single-element performance with modulated signal, the single-element input is injected with DVB-S2x APSK modulated signal, and a high bandwidth oscilloscope analyzes the output signal. Fig.5.12 shows the measured on-wafer singe-element EVM performance with DVB-S2x 256-APSK modulated signal. The single-element peak EVMs using 256APSK with 100MBaud and 400MBaud is -38dB and -35dB, respectively.

5.4.2 Phased-Array Receiver Performance

Fig.5.13 shows the proposed chip micrograph for the satellite receiver chip. One receiver chip is composed of 8-elements and one 8:1 power combiner. A RF amplifier is added at the output of 8:1 power combiner to eliminate the high insertion loss from the transmission line. The single-element area is only 0.2mm^2, which does not include the combiner and RF amplifier area.

The 256 arrays are implemented in four identical PCBs to demonstrate the phased-array performance further. As shown in Fig.5.14(a) and Fig.5.14(b), the sub-array module

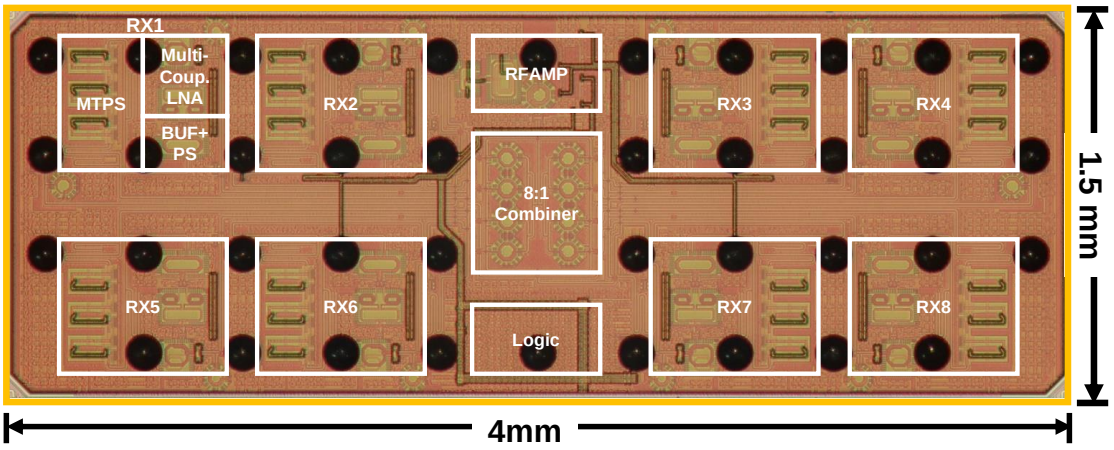
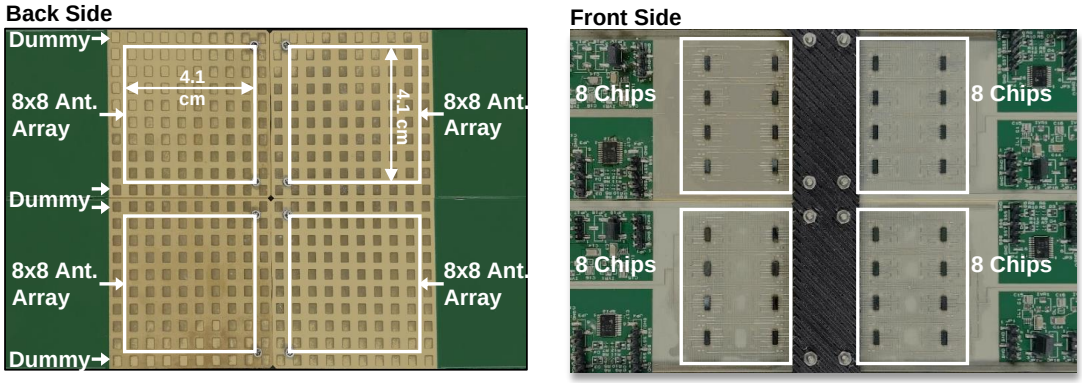
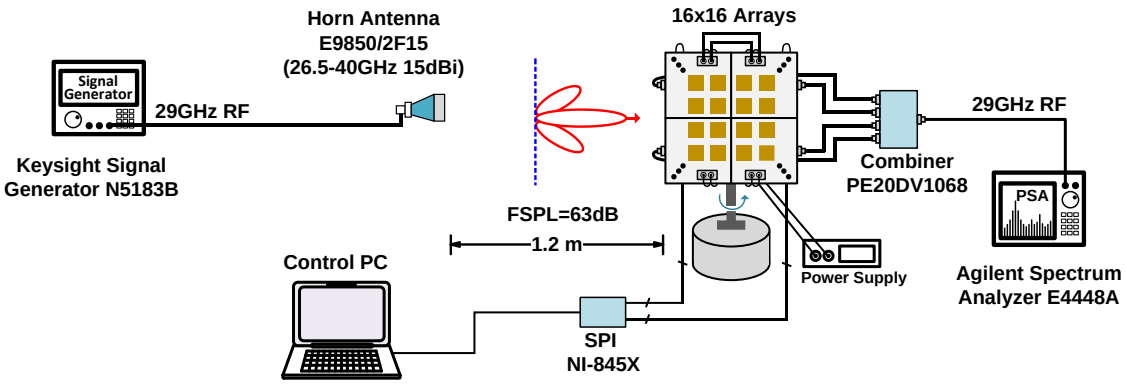


Figure 5.13: The chip micrograph for the proposed satellite receiver chip.

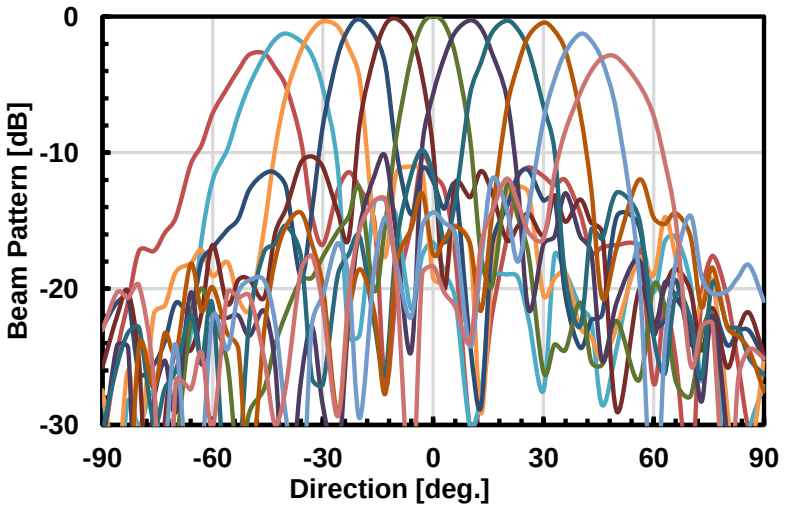


(a) (b)

Figure 5.14: The back side (a) and front side (b) of the proposed 256-array satellite receiver PCB.



(a)



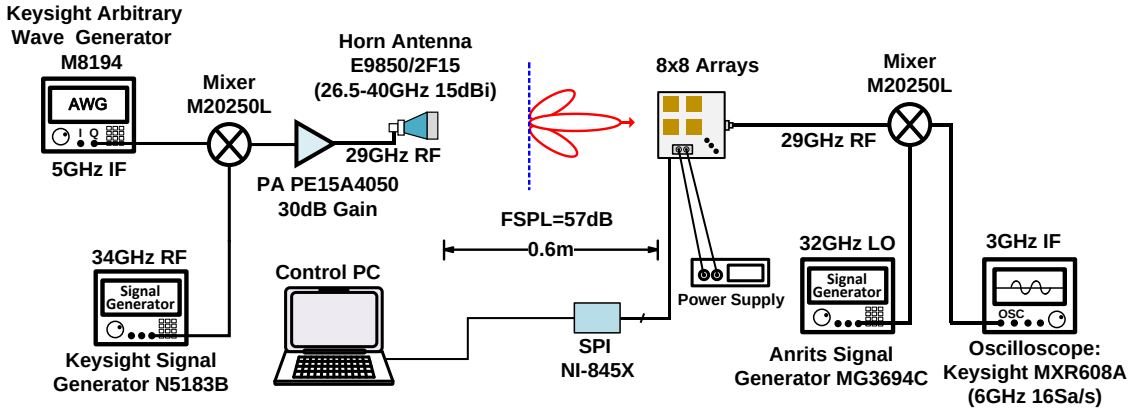
(b)

Figure 5.15: The setup (a) and measurement results (b) of 16x32 sub-array beam pattern measurement.

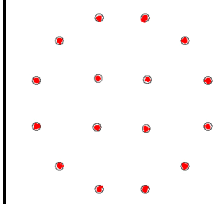
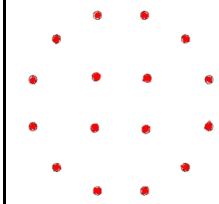
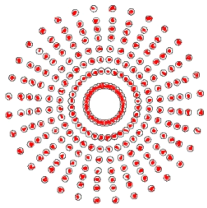
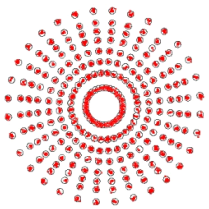
PCB has eight chips on the front with an 8x8 line-ar-polarized array antenna on the back. Each chip has 8 RF-signal ports and is connected to the 8x8 array module, which can also configure a 16x16 array.

The patch antenna also utilizes dummy antennas for increasing phased-array gain without decreasing the antenna signal bandwidth. There are also some supported chips for providing power, SPI buffer, capacitors, and even the jump connection port on the front side. The four RF signals of four PCBs can be connected outside for the 256-array configuration.

Fig.5.15(a) shows the setup for phased-array beam pattern measurement. Unlike the EVM measurement, the input signal power level is not sensitive to the final performance.



(a)

Modulation	16 APSK	16 APSK	256 APSK	256 APSK
Symbol Rate	0.8 GBaud	1.6 GBaud	0.8 GBaud	1.6 GBaud
Constellation*				
Data Rate	3.2 Gbps	6.4 Gbps	6.4 Gbps	12.8Gbps
RX EVM (RMS)	-36.4dB	-33.1dB	-35.7dB	-33.2dB

(b)

Figure 5.16: The setup (a) and measurement results (b) of 0.6-m OTA EVM measurement.

To make the setup easy, the test signal is directly generated by Keysight signal generator N5183B and a 15dBi horn antenna.

The FSPL of this measurement setup is 1.2meter, and the test module is only a 16x32 sub-array for easy measurement. Four SPI-NI-845X modules control the test module. The direction angle of the test module is changed by a tuning table controlled by the same computer.

All the signals are then combined by a combiner named PE20DV1068, and Agilent spectrum analyzer E4448A analyzes the single-carrier signal. All sub-arrays use the same power supply for simplicity.

As shown in Fig.5.16(a), the setup for 0.6-m OTA measurement is based on a 8x8 sub-array module. The IF signal is generated by Keysight arbitrary wave generator M8194. Then the IF signal is up-converted to 29GHz with a 34GHz LO RF. One power amplifier (PE15A4050) is added to the output of the mixer to satisfy the optimized input signal

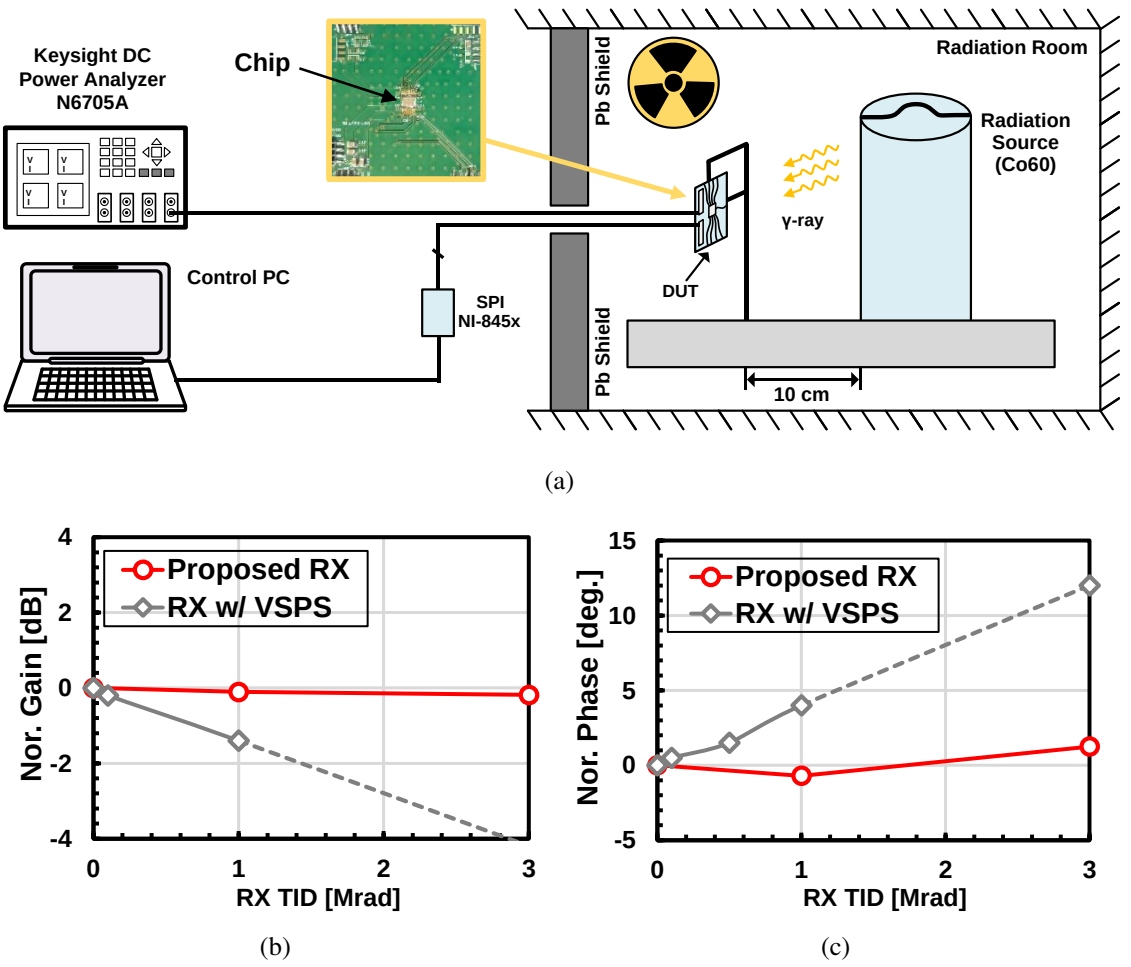


Figure 5.17: The setup (a), measured normalized gain variation (b) and measured normalized phase variation (c) for radiation hardness measurement.

power level,. Then the RF modulated signal is emitted by a horn antenna E9850/2F15.

The modulated signal is then received by our test 8x8 sub-array module. The receiver 29GHz signal is down-converted 3GHz IF by a 32 GHz LO signal. Finally, the modulated APSK signal is demodulated by a 16Sa/s Oscilloscope named Keysight MXR608A.

Fig.5.16(b) represents the measurement EVM results for 0.6-m OTA situation. At this measurement, The OTA EVMs are measured using 16APSK and 256APSK with 0.8G-Baud and 1.6GBaud symbol rates. The proposed low-power receiver realizes EVMs of -33.1dB and -33.2dB at a 1.6GBaud symbol rate using 16APSK and 256APSK, respectively.

The peak OTA EVM at 29GHz is -40dB with a 100MHz 16 APSK modulated signal. An OTA data rate of 12.8Gbps is achieved with a 1.6GHz single-carrier 256APSK modulation signal.

Fig.5.17(a) shows the setup for radiation hardness measurement. The radiation source

	This work	RFIC2021 [106]	ISSCC21 [107]	ISSCC20 [108]	TokyoTech [109, 110]
Process	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS
Operation band	26.3-31.6GHz	24-30/37-40GHz	18-19GHz	37-40GHz	27.5-30.5GHz*
Integration	8xElement Rx	2xElement Rx	8xElement Rx	16xTRx IF LO	8xElement
NF	3.8dB&	4.3-6.4dB	3.2-4.1dB	4.2-4.6dB	5.2dB@29GHz
Coherent Gain	23dB	32dB^	28dB^	16-59dB	25-27dB
IIP3	-22dBm&	-38dBm^	-17dBm*	N/A	-20dBm*
Pdc/Element	3.4mW&	17.3mW&	74mW#	39mW	61mW&
RMS Gain Error	0.14dB@29GHz$	0.9dB	0.22dB	0.33dB	0.25dB@29GHz*
RMS Phase Error	0.09°@29GHz$	6°	1.5°	3.3°	1.4°@29GHz*
TID Degradation/Mrad	0.06dB/0.4°	N/A	N/A	N/A	1.4dB/4.0°

*: estimated from figure, $: w/o cal., &: single element, ^: high gain mode, #: 2 beams

Table 5.1: The system performance comparison table with state-of-the-art works

is γ ray with radiation material cobalt 60. The distance between the test PCB and the radiation sources is 10cm.

Another measurement machine and controlling computer are protected by thick lead (Pb). To emulate the working situation in the LEO orbit, all the biases are turned on and set to the value for operation mode.

Fig.5.17(b) and Fig.5.17(c) represent the measurement TID gain and phase tolerance results. The measurement results are for the total receiver chip, including the combiner and RF amplifier. Compared with the conventional receiver, the proposed one achieves 0.06dB/Mrad gain and 0.4°/Mrad phase degradations at 29GHz. Regarding a 3-year lifespan, the receiver gain and phase reductions are only 0.18dB and 1.2°, respectively.

5.5 Conclusion

Tab.5.1 compares this work with the state-of-the-art phased-array ICs. Utilizing the magnetic-tuning phase shifter, this work achieves the smallest RMS phase and gain errors while maintaining the 0.06dB/Mrad and 0.4°/Mrad TID gain/phase degradation satisfies the satellite requirements. The lowest power consumption per element is realized by employing the mutually coupled inductor based LNA and the neutralized-cascade buffer with the built-in 180° phase shifter.

As shown in Fig.5.18, at the same value of energy/bit, the proposed work has the lowest normalized sensitivity with -55dBm.

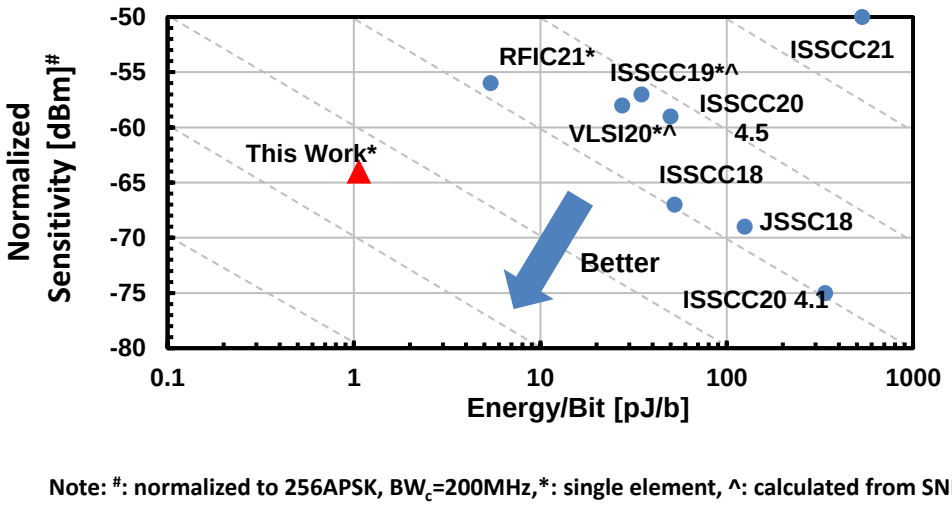


Figure 5.18: The normalized sensitivity versus energy per bit.

Chapter 6

Conclusion and Future Works

6.1 Conclusion

This thesis presented novel building block circuits and transceiver diagrams for the future 6G network with extensive coverage. The phased-array millimeter-wave transceivers can increase the link speed between the small cube satellite and the ground station terminals. The network coverage for the global network can be realized by the significant number of small cube satellites with the phased-array transceiver. Facing the design challenges brought by the small cube satellites of the future 6G network. This thesis illustrates detailed design requirements and methodology in system and block levels.

Considering the ground base station, this thesis conducted cutting-edge research on integrating a Ka-band satellite communication transceiver in a standard CMOS topology with an enhanced dual-channel low-NF wide-dynamic-range receiver and high-linearity transmitter. This work reported and demonstrated the world-first integrated CMOS satellite ground base-station transceiver, which attracted academic and industry attention. This work also reported a single-turn high-quality-factor transformer as the matching network at the output port of the power amplifier, which boosts the transmitter modulated adjacent channel power ratio by about 12dBc compared with the conventional solutions.

In terms of satellite receiver terminal, this thesis innovatively developed an ultra-low-power radiation-hardened Ka-band complementary metal-oxide-semiconductor phased-array receiver for small satellite constellation. One path of the phased-array receiver consists of a multi-coupling current-reuse low noise amplifier (LNA), a neutralized cascade buffer with a build-in 180-degree phase shifter, and a magnetic-tuning radiation-hardened phase shifter. Compared with the state-of-the-art phased-array ICs, this work achieved the smallest root mean square (RMS) phase and gain errors while maintaining the 0.06dB/Mrad and 0.4degree/Mrad total ionizing dose (TID) gain/phase degradation. This pro-

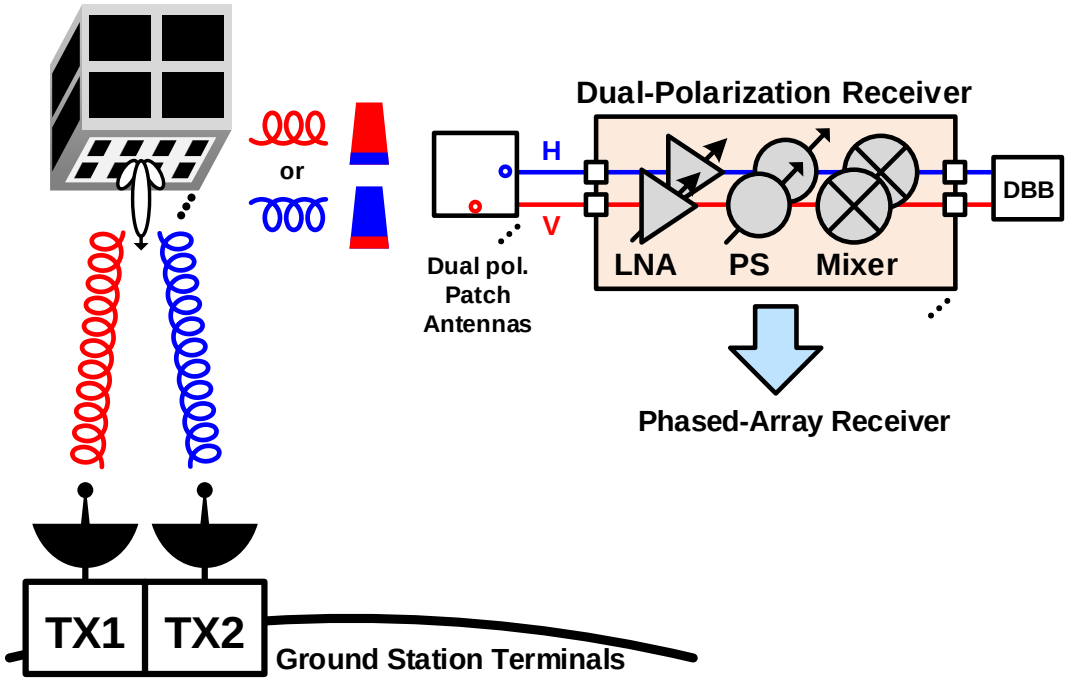


Figure 6.1: The illustration for the dual-circularly polarized phased-array receiver for LEO satellite terminal.

posed circuit realized 5.5% (the lowest in the world) of the typical power consumption compared with the conventional front-ends.

To summarize, this thesis introduces novel techniques for improving satellite transceiver system SNDR, link speed, power consumption, and TID gain/phase tolerance. The introduced ultra-low-power transceiver utilized mutually coupled inductors could be considered an early demonstration of the circuits in the future 6G network for global coverage.

6.2 Future Work

6.2.1 Dual-Circularly Polarized Phased-Array Receiver

There are two main electromagnetic wave polarization ways: linear polarization and circular polarization. As we all know, there is faraday rotation to the electromagnetic wave between the LEO satellite terminals and the ground station terminals. In terms of the linear polarization, the faraday rotation makes it difficult to receive the RF signal in a fixed angle which is a standard way for the antenna implementation for both satellite terminals

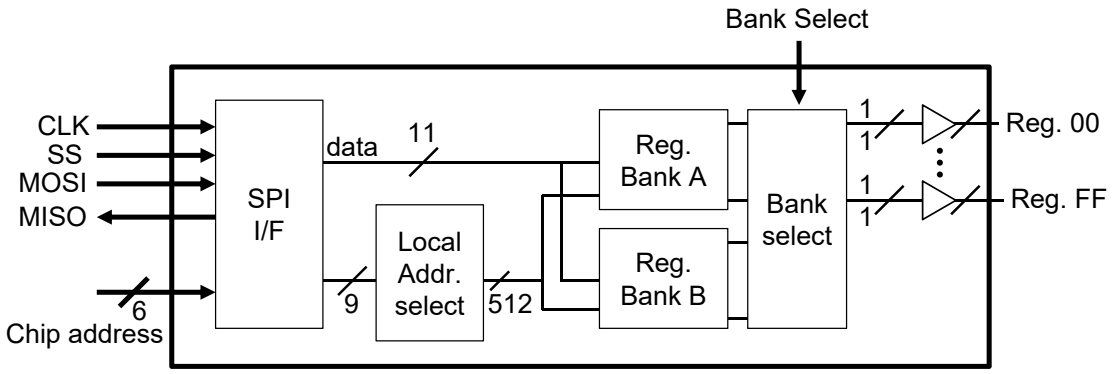


Figure 6.2: The detailed SPI schematic for the fast-beam-switching feature.

and the ground station terminals.

Circular polarization is a potential way to solve the angle problem caused by the Faraday rotation in the ionosphere. As shown in Fig.6.1, by implementing the dual-polarization path antenna with H and V paths, the phased array receiver is capable of demodulating the circular-polarized RF signal.

The future work is the implementation of the dual-circularly polarized phased-array receiver, including the single-element LNA, phase shifter, combiners, and mixer for the processing RF signal. The left-handed circularly polarized signal and the right-handed circularly polarized signal can be switched by the phase difference between the H path and V path.

6.2.2 Fast-Beam-Switching SPI

To increase the network coverage as much as possible, the satellite terminal needs to communicate with many ground base station terminals simultaneously. Thus the beam needs to be switched as quickly as possible to decrease the time gap between ground station terminals.

The beam switching time is decided by the phase shifter setting time. The phase shifter setting time is equal to the charge time of the gate capacitor by the serial resistor, which is several picoseconds. However, owing to the necessity for a hung number of phased-array elements. The SPI writing time for all phase shifters still is of enormous value.

As shown in Fig.6.2, a double-bank SPI controlling schematic can be utilized to increase the beam-switching time for supporting more ground station terminals. The phase setting codes for all elements will be previously written to the memory register bank A and bank B. Bank A and bank B save the phase setting for ground station terminal A and

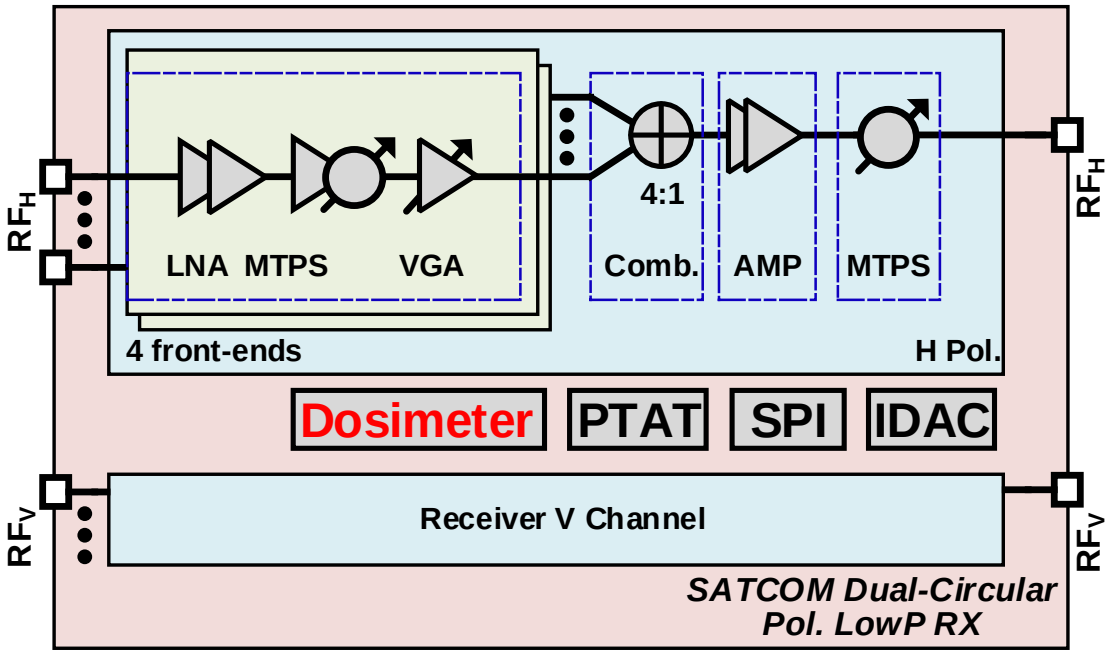


Figure 6.3: The system diagram with TID dosimeter for the monitor.

terminal B. The beam pattern can be switched by changing the bank select code in several picoseconds. Thus, the high-speed SPI schematic will be implemented in the revised version of the satellite phased-array receiver in future work.

6.2.3 Dosimeter Implementation

As we mentioned before, the TID value from the cosmic space is a critical consideration for the LEO satellite receiver terminal. The reason is that the high total ionizing dose value will degrade the RF performance of the CMOS process.

However, the value of TID is random and will be influenced by a lot of parameters such as the orbit type, the orbit altitude, the activity of the sun, and the high-energy ray from deep space. Thus, a dosimeter that can monitor the TID value is necessary for the phased-array receiver, and it is shown in Fig.6.3

The engineer can adequately operate the LEO cube satellite with the realistic TID value. For example, when the TID value of a particular satellite part increases a lot and exceeds the warning line. Then, the engineer can execute some protecting way for lifetime extension.

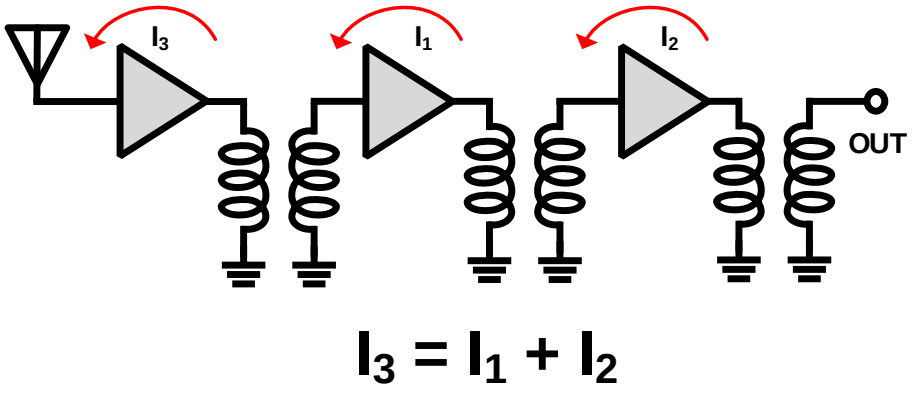


Figure 6.4: The detailed circuit for adjustable current-steering based LNA.

6.2.4 Low-Power Current-Steering Technique

In terms of satellite receiver terminal, The limitation of generated power by the limited available solar panel area is another critical issue for small cube satellites. Thus, a more specific power-saving technique should be introduced for higher system performance.

Current-reusing and current-steering techniques are possible ways to decrease the total system power consumption. The power supply voltage can be smaller for power saving for a small-amplitude RF signal received by the dual-circularly polarized antenna. Conventional current-steering techniques are implemented by connecting two operation transistors with large decoupling capacitors.

Fig.6.3 proposes an adjustable current-steering technique for power saving to reduce the system power consumption further. The current weights between the second and third transistors can be flexible for more freedom in the design dimension. In future work, the proposed adjustable current-steering technique can be implemented.

6.2.5 Advanced Process

Compared with conventional CMOS processes such as the 65nm bulk process in this work, other advanced process techniques such as SOI CMOS and compound semiconductors can also be potential candidates for the future 6G network communication system. The SOI CMOS process isolates the high-frequency transistors with the lossy P-type silicon substrate and thus can realize high performance in RF circuits.

Even though it is a little more expensive than the conventional 65nm bulk CMOS process, the penalty is valuable for the higher RF circuit performance, especially in LEO

satellite terminal applications. Other potential compound semiconductors, such as gallium arsenide (GaAs), are good candidates for their high oscillation frequency and high power efficiency feature in RF circuits.

Thus, the RF circuits with GaAs compound semiconductor process are capable of low power consumption and higher system efficiency, which is the critical requirement for a satellite terminal system (the power limitation generated by the small solar panel area). Higher costs for the GaAs process or other compound semiconductors should be carefully considered owing to the tremendous requirements of LEO small cube satellites for global network coverage.

Moreover, advanced bulk CMOS processes such as 28nm, 16nm, and 10nm are potent candidates for future RF circuits. One reason is the higher oscillation frequency with lower loss in CMOS substrate. Another reason is the high integrated level with high-speed digital circuits such as DAC, ADC, DSP, and even MCU in one chip.

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Appendix A

Publication List

A.1 Journal Papers

- **Xi Fu**, Yun Wang, Zheng Li, Atsushi Shirane, Kenichi Okada, "A CMOS SPDT RF Switch with 68 dB Isolation and 1.0 dB Loss Feathering Switched Resonance Network for MIMO Applications," *IEICE Transactions on Electronics*, Vol. E104-C, No. 7, pp. 280-288, Jun. 2021.

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- **Xi Fu**, Yun Wang, Dongwon You, Xiaolin Wang, Ashbir Aviat Fadila, Yi Zhang, Sena Kato, Chun Wang, Zheng Li, Jian Pang, Atsushi Shirane, Kenichi Okada, "A 3.4mW/element Radiation-Hardened Ka-Band CMOS Phased-Array Receiver Utilizing Magnetic-Tuning Phase Shifter for Small Satellite Constellation," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2022, pp. 90-92.

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A.3 Co-author

A.3.1 Journal Papers

- Yun Wang, Dongwon You, **Xi Fu**, Takeshi Nakamura, Ashbir Aviat Fadila, Teruki Someya, Atsuhiro Kawaguchi, Junjun Qiu, Jian Pang, Kiyoshi Yanagisawa, Bangan Liu, Yuncheng Zhang, Haosheng Zhang, Rui Wu, Shunichiro Masaki, Daisuke Yamazaki, Atsushi Shirane, and Kenichi Okada, "A Ka-Band SATCOM Transceiver in 65-nm CMOS with High-Linearity TX and Dual-Channel Wide-Dynamic-Range RX for Terrestrial Terminal," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 57, No. 2, pp. 356-370, Feb. 2022.

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