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Investigation of the Electrochemical Passivation of Porous Silicon for Tandem Solar Cells

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1.1 BACKGROUND

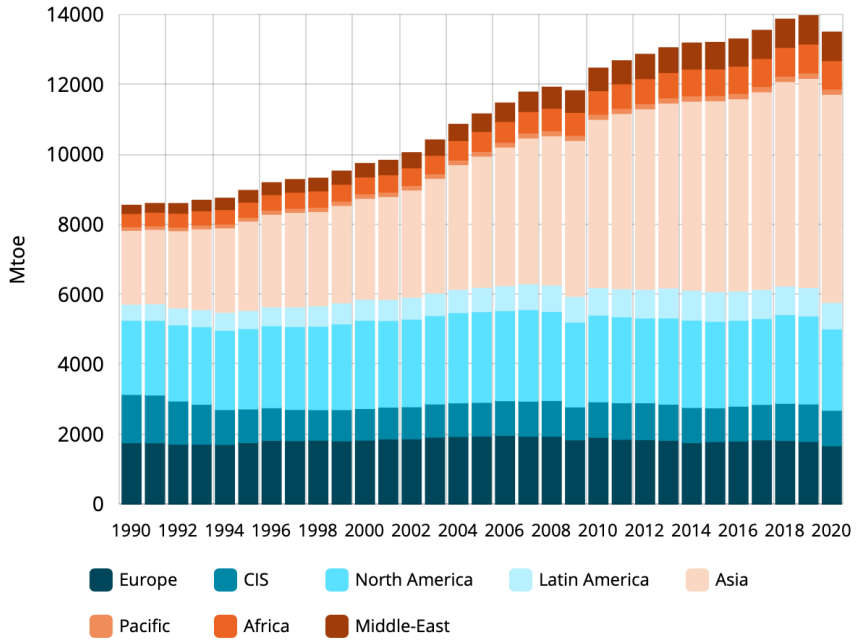


FIGURE 1: ELECTRICITY CONSUMPTION BY REGIONS BETWEEN 1990-2020 [1]

In the present time, the rising of the global energy demand is a primary issue for every country. The global energy consumption is increasing every year in respect to the world population. In order to keep the balance between the energy demand and supply, we have been heavily relied on the fossil fuel as a primary source of energy. By burning the fossil fuel, the heat generated can be utilized in many ways from directly heating up the household to generating the electricity through the steam turbine. However, despite being highly energy-concentrated, the source is not renewable, and the by-product of burning this fossil fuel is responsible for the emission of the greenhouse gases into the earth atmosphere, which is the main cause of global warming; this, as a result, causes many environmental concerns as well as the impact to the global economic. One of the most concerned greenhouse gas, CO_2, was confirmed to be the main causes that raises the average global temperature over 1°C after the industrial revolution. The power generation itself is responsible for 36.3 Gt of CO_2 emission in 2021 [2] and it seems that the trend will keep increasing if there is no meaningful law or regulations to control the emission.

To counteract those adverse consequences, power generation with less CO_2 emission by the renewable sources, e.g., solar, wind, hydrothermal, etc., has been the main research topic in the field for decades. Some countries, like Germany, China, Scandinavian countries, have been attempting to significantly replace the fossil fuel-based power generation into these CO_2-free renewable technologies within next 20 years. From Figure 2, the total amount of electricity generation in 2019 almost reached the 7 TWh level, in which the electricity by solar shares 10% of the overall generation. This trend has been increasing rapidly every year since 2010, where it reaches +22.7% in 2018-2019 [1] and it seems like the trend will not stop in the near future.

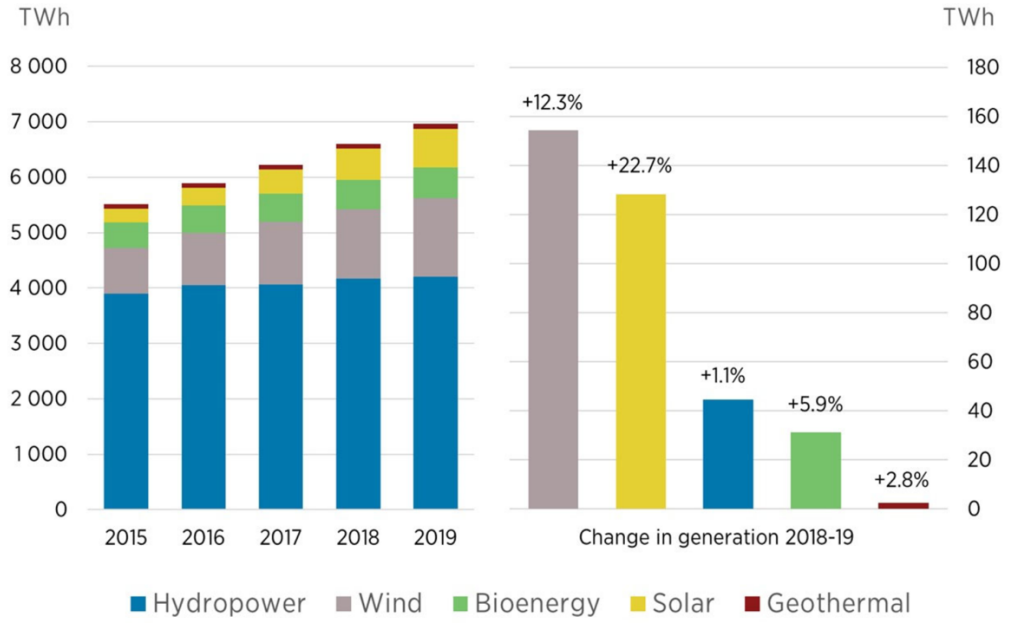


FIGURE 2: PROPORTION OF GLOBAL ELECTRICITY GENERATION BY RENEWABLE SOURCES AND ITS GROWTH IN 2018-2019 [3]

In term of the definition, the renewable energy is the energy that comes from the source that is not depleted when used, which means that it can be utilized in more sustainable way compared to the fossil fuel. One of the most abundant sources of energy is the solar radiation, and the devices that converts it into the electricity are called the photovoltaic (PV) cells or solar cells. Not only is solar power generation small and medium-sized, easily distributed, and easy to install, but it can also be used as an emergency power source. It is also suitable as an off-grid power generator for the household consumption and local community consumption of energy [4]. However, due to the high cost of electricity generation compared to those generated from the fossil fuel, the PV technologies were not much widespread and adopted by many

countries. From these facts, in order to use solar power generation as a main energy source, further improvement in efficiency and the module cost reduction are essential. It is not until the recent decade that the PV technologies have become more accessible and prevalent as a result of the significant decrease of the electricity generation cost. This is a result of the increase in the number of installations, the improved solar cell manufacturing process leading to the drop in cost, and the improvement of the efficiency of the solar cell [5].

In these recent years, technological innovation has progressed, and as shown in Figure 3, various solar cells have been developed and their efficiency has been improved. In the PV industry, silicon (Si) is a popular material because it has suitable optoelectronic properties as a semiconductor as well as its abundance on earth; it is also highly technological available as it has been studied and developed for many decades [6]. As a result, the PV market has been dominated by silicon-based solar cells up until the present time. In term of the efficiency, the best single junction Si solar cells is reported to be 26.7% [7] by Kaneka, which approaching the Shockley-Queisser limit of 32% [8]. In addition, with this theoretical efficiency in a single junction solar cell, development of a multijunction solar cell, in which two or more layers of solar cells are stacked on each other, is required to further improve the efficiency. Currently, the highest efficiency is reported to be 47.1% by NREL (Figure 3) with 6 junctions and concentrator.

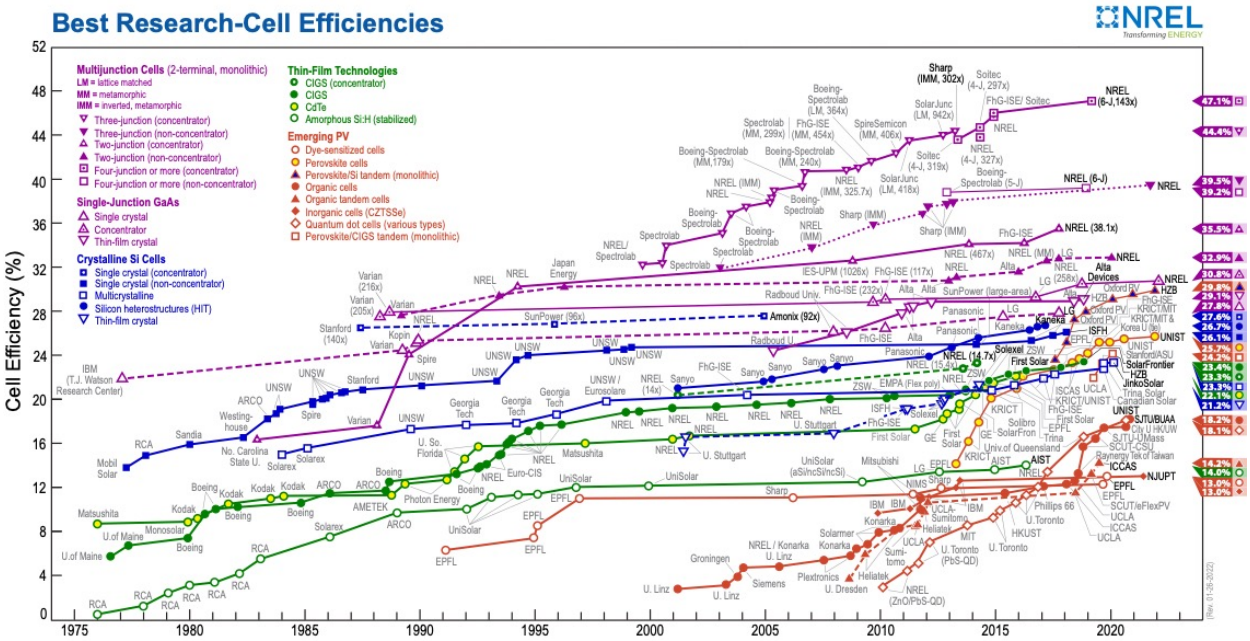


FIGURE 3: NREL BEST RESEARCH-CELL EFFICIENCY CHART [9]

However, highly efficient multijunction solar cells are not currently suitable for commercial use because they use rare metals such as indium or toxic arsenic and the fabrication process is still complicated and expensive. In this study, we aimed to develop an all-silicon multi-junction solar cell using only silicon, which is a material with abundant resources, by using the porous silicon as a top cell of the multi-junction solar cell.

1.2 Principle of Solar Cells

1.2.1 PN-Junction

The basic principle of power generation of a silicon solar cell, which is a type of semiconductor solar cell, is a P-N junction. A P-N junction is one in which a p-type semiconductor having holes as majority carriers and an n-type semiconductor having electrons as majority carriers are brought into crystallographic contact. When p-type and n-type semiconductors come in contact, holes in the p-type semiconductor diffuse into the n-type semiconductor and electrons in the n-type semiconductor diffuse into the p-type semiconductor due to the difference in carrier concentration. At this time, in the vicinity of the interface, the electron and the hole cancel each other to form a region (depletion layer) in which the carrier concentration is deficient. In the depletion layer on the p-type semiconductor side, negatively charged acceptor atoms (shown as white circle in Figure 4) are left, and in the depletion layer on the n-type semiconductor side, positively charged donor atoms (shown in red circle in Figure 4) remain. As a result, an electric field is generated from n-type to p-type. Since the electric field is opposite to the direction in which the carriers diffuse, the diffusion due to the concentration difference (diffusion current) and the drift current due to the electric field are balanced, resulting in a thermal equilibrium state. In the case of a standard silicon single crystal solar cell, the width of the depletion layer in the thermal equilibrium state spreads about 1 μm from the junction interface to the p-type side and hardly spreads to the n-type in the case of a standard silicon single crystal solar cell.

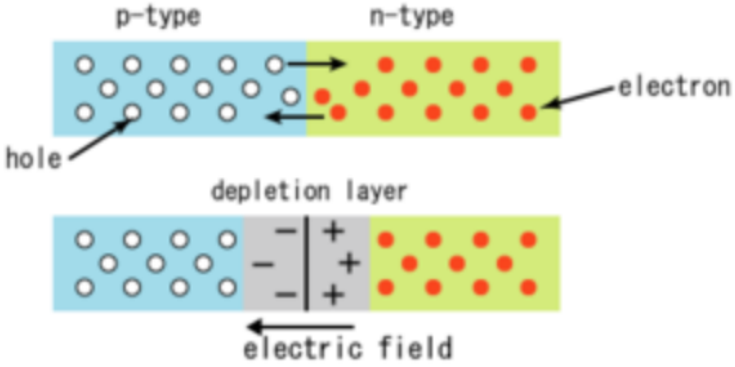


FIGURE 4: P-N JUNCTION DIAGRAM [10]

A band diagram at the time of PN junction formation is shown in Figure 5. The vertical axis is the energy of electrons. In the intrinsic semiconductor, the Fermi level locates at the center of the band gap, but due to the doping of the impurity, it shifts toward the valence band side in the p-type semiconductor and to the conduction band side in the n-type semiconductor. When these semiconductors are brought into contact, the majority carriers diffuse, the energy bands move so as to make the Fermi level coincide, and at the energy level that it matches, the P-N junction will reach a thermal equilibrium state. At this time, a built-in potential V_{bi} is generated in the depletion layer due to the difference of the initial Fermi level.

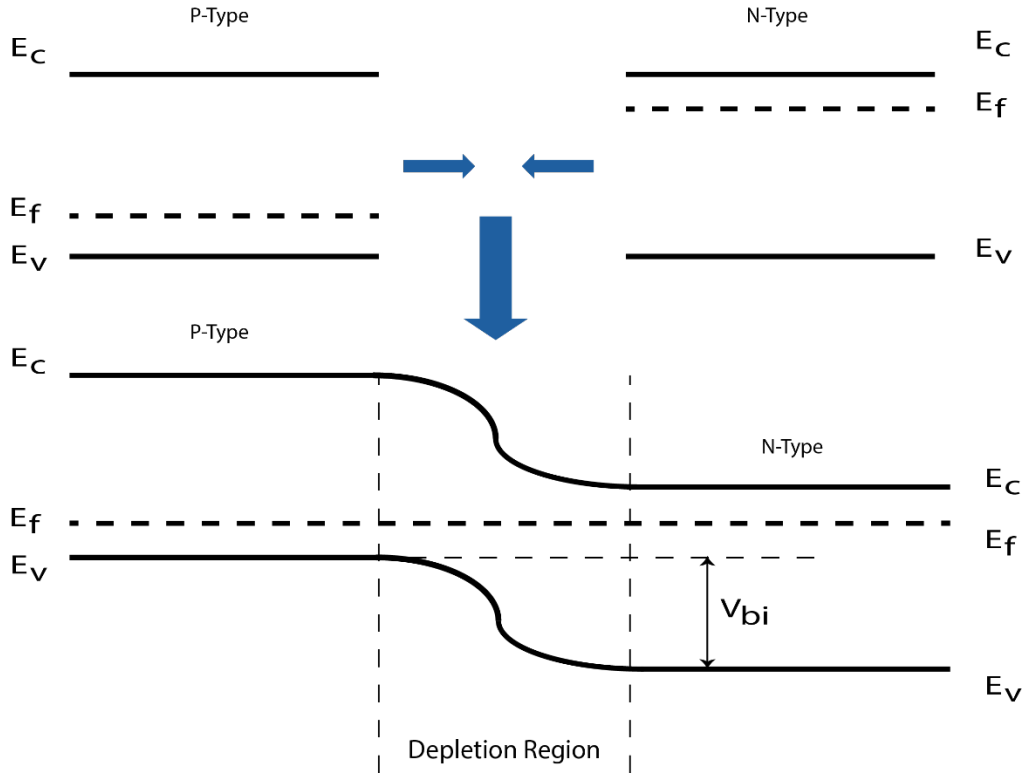


FIGURE 5: P-N JUNCTION FORMATION DIAGRAM

1.2.2 Rectification Characteristics

When a voltage is applied to the PN junction, the magnitude of the potential barrier V_{bi} changes as much as the applied voltage. When a voltage is applied in a direction to reduce the potential barrier (forward bias: connect the negative terminal of the external circuit to n-type and the positive terminal to p-type), the potential barrier decreases to cause electron diffusion from n layer to the top layer. The diffusion becomes larger as the bias is applied. Conversely, if a voltage is applied in a direction to increase the potential barrier (reverse bias: connecting the positive electrode of the external circuit to the n-type and the p-type to the negative electrode), the potential barrier becomes quite large, so the diffusion current can be ignored. On the other hand, the drift current is almost constant even in the forward bias and the reverse bias. This is because the magnitude of the current is determined by the minority carrier density generated by the thermal excitation of the drift current in the region just outside the depletion layer (about the diffusion length of minority carriers from the depletion layer). From these facts, when the PN junction is forward biased, the current increases exponentially, but in the reverse bias, only a small amount of current flows. This is called rectification characteristics of diode. The current flow over the diode is described in equation 1 and 2.

$$J = J_0(\exp(\frac{eV}{k_B T}) - 1) \quad \text{……..(1)}$$

$$J_0 = e\,(\frac{D_n p_n}{L_n} + \frac{D_p p_p}{L_p}) \quad \text{……(2)}$$

Where D_n : electron diffusion constant, D_p : hole diffusion coefficient, L_n : electron diffusion length, L_p : Diffusion length of holes

n_p : electron density in p-type semiconductor, p_n : hole concentration in n-type semiconductor

J_0 : reverse saturated current density

1.2.3 Principle of Solar Cell Power Generation

When light of energy greater than the band gap is incident on the semiconductor, part of it is absorbed, electrons are excited in the conduction band, and holes remain in the valence band. At this time, for the carriers generated in the depletion layer or generated near the depletion layer and reached the depletion layer before recombination, in case of electron, it is carried to the n-type semiconductor and carriers to the p-type semiconductor by the built-in

potential. As described above, excess minority carriers generated by light irradiation flow out from the n-type and return to the p-type, and then the power can be extracted by connecting a resistor to the external circuit. In the solar cell, the current in the reverse direction to the diode increases by the current (short-circuited current: J_{SC}) generated by the light irradiation, so the current-voltage characteristic (J-V characteristic) corresponds to the short circuit current. It is expressed by the following equation 3 by adding J_{SC}.

$$J = J_{SC} - J_0(\exp(\frac{eV}{k_B T}) - 1) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

Furthermore, it is also able to define the open-circuited voltage (V_{OC}) when the J = 0 in this equation (voltage when not connecting the resistance to both ends).

$$V_{OC} = \frac{k_B T}{q} \ln(\frac{J_{SC}}{J_0} + 1) \approx \frac{k_B T}{q} \ln(\frac{J_{SC}}{J_0}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

1.3 THEORETICAL LIMITATION OF SILICON SOLAR CELLS

1.3.1 Factors That Reducing Solar Cell Efficiency and Its Losses

The following may be mentioned as factors of the decrease in the efficiency of the solar cell [11], [12].

1) Loss due to transmission of long wavelength light

Since the light whose energy is smaller than the band gap of the semiconductor cannot be absorbed, it cannot be used for power generation. In the case of crystalline silicon, this loss is about 44% of the total solar energy.

2) Energy loss when absorbing short wavelength light

Although the light ($h\nu > E_g$) having energy greater than the band gap (E_g) is absorbed by the semiconductor, the generated electrons immediately dissipate heat and move to the lower end of the conduction band and holes move to the upper end of the valence band. From this, the energy ($h\nu - E_g$) originally possessed by the light is lost. In the case of crystalline silicon, this loss is an 11% loss of total solar energy.

3) Reflection loss

The light reflected by the solar cell surface cannot be used for carrier generation.

4) Voltage factor loss

Carriers generated by absorbing the light have energy of about band gap, but the voltage for operating the solar cell is the open circuit voltage (V_{OC}) at the maximum, and this difference is a loss.

5) Lack of light absorption

The thickness required for the semiconductor to absorb light is determined by the light absorption coefficient. A semiconductor with a low light absorption coefficient cannot perform sufficient carrier generation unless a thicker film is used.

6) Series resistance, loss due to parallel resistance

The series resistance is attributed to the resistance of the electrode, the ohmic contact resistance at the metal-semiconductor interface, and the bulk resistance. When series resistance (R_S) is taken into consideration, series resistance loss R_SI is added to the formula of the IV characteristic, and it is expressed by the following equation 5.

$$I = I_{SC} - I_0 \left(\exp\left(\frac{q(V+R_SI)}{nkT}\right) - 1\right) \quad \text{……..……..(5)}$$

Parallel resistance (shunt resistance: R_{SH}) is usually assumed to be infinite, but in the actual solar cell is a problem when the leakage current due to such cases or grain boundaries when there are many defects in the connection. J-V characteristics, including the influence of parallel resistors, are represented by the following equation 6.

$$I = I_{SC} - I_0 \left(\exp\left(\frac{q(V+R_SI)}{nkT}\right) - 1\right) - \frac{V+R_SI}{R_{SH}} \quad \text{…….(6)}$$

The series resistance has little effect on the open voltage V_{OC}, but short-circuit current density $J_{SC,}$ which may reduce the fill factor. Parallel resistors, on the other hand, have little effect on $J_{SC,}$ but reduce V_{OC} and fill factor.

7) Loss due to carrier recombination (bulk and surface recombination)

Carrier generated by light absorption disappears by partial recombination, it cannot be used for power generation. Recombination is classified into two categories: bulk recombination and surface recombination. Bulk recombination is intended to recombine before reaching the poor layer of the carrier generated outside the depletion layer.

Surface recombination defects and dangling bond (unpaired electron) of the material surface works as a recombination center, is expressed in the surface recombination rate easily occurs as compared to bulk recombination. The recombination is distinguished by the surface of the solar cell (obtaining side of light) and the back surface, it is considered divided into the surface recombination rate and the back-surface recombination rate, respectively. Since the surface has more optical carrier than the back surface, the surface recombination rate has a significant effect on the conversion efficiency.

1.3.2 Theoretical Efficiency Limit

In a single junction solar cell, assuming that all absorbed light is used for carrier generation, the short-circuited current density (J_{SC}) increases as the band gap decreases, and the open-circuited voltage (V_{OC}) increases as the band gap increases. From these relationships, the theoretical efficiency, which is known as Shockley-Queisser limit, about 30% in the single junction solar cell with energy band gap of 1.1 eV [8]. but it is known that the theoretical efficiency can be improved by increasing the number of junctions.

1.4 Solution to Surpass Theoretical Limitation

1.4.1 Tandem Solar Cell

In order to surpass the Shockley-Queisser limit for of the single junction solar cell, a tandem is one of the potential candidates. Tandem is one of a type of multi-junction solar cell, which comprises of two junctions. This type of solar cell has a stacked structure of solar cells using a material having a large band gap from the light incident side. In a solar cell of this structure, light with high energy (short wavelength) is absorbed by a material with a large band gap, and light with low energy (long wavelength side) is absorbed by a material with a small band gap. Figure 6 shows the improvement of the light absorption.

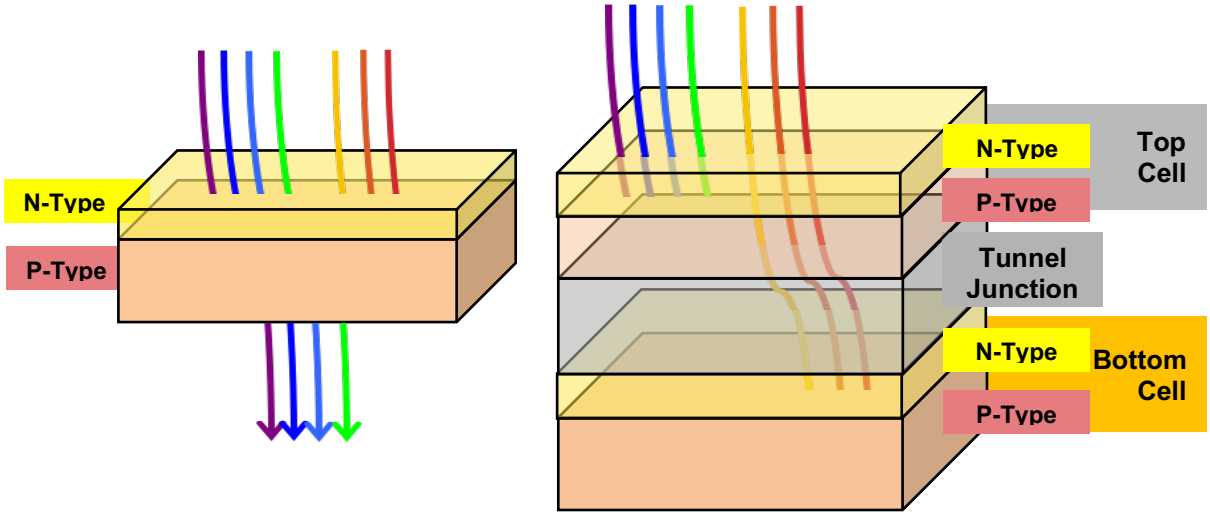


FIGURE 6: LIGHT ABSORPTION DIFFERENCE BETWEEN SINGLE -JUNCTION SOLAR CELL (LEFT) AND TANDEM SOLAR CELL (RIGHT)

In this manner, by selecting a material which absorbing sunlight in different wavelengths, light in both shorter wavelength (highlighted in blue in Figure 7) and longer wavelength (highlighted in yellow in Figure 7) can be used more effectively. The loss shown in 1.3.1 is also reduced, and high efficiency can be obtained.

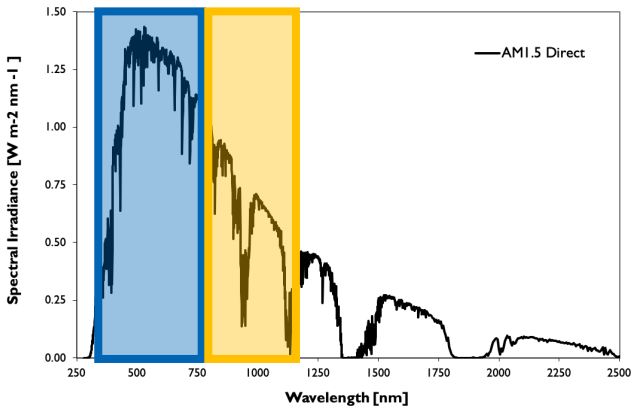


FIGURE 7: ABSORPTION OF AM1.5 DIRECT SOLAR SPECTRUM FROM DIFFERENT LAYERS OF TANDEM

At the present time, the highest efficiency of multi-junction solar cells has been reported to be 44%, which is the InGaP / GaAs / InGaAs three-junction type with light concentrator (Sharp) [9]. However, this type of multijunction solar cell is not widely used because it is expensive due to the use of the toxic substance arsenic, the use of rare metals such as gallium and indium, and the complicated manufacturing process. It is not suitable for the commercial use as a solar cell and the applications are now limited to only in lab-scale and projects that prioritizes efficiency over cost, like space missions.

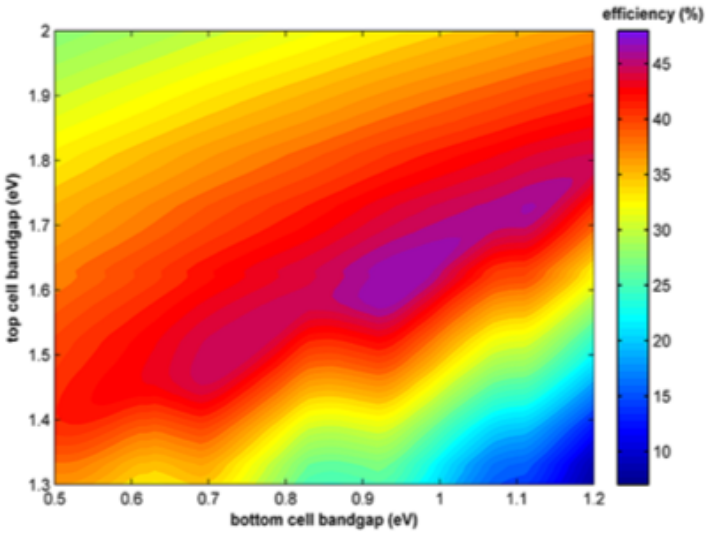


FIGURE 8: TANDEM MAXIMUM EFFICIENCY UNDER AM1.5G [13]

Figure 8 shows the maximum efficiency of tandem to be used as a guideline for material selection. The highest efficiency (~over 45%) for tandem can be achieved by matching crystalline silicon (1.1 eV) with other material with band gap of 1.7 eV.

1.4.2 All-Silicon Tandem Solar Cell and the Candidates of Top Layer

The development of all-silicon solar cells made only of silicon materials is expected as a way of solving the disadvantages of multi-junction solar cells such as cost increase by utilization of rare metals and the use of toxic materials, and also the lattice mismatch problem when using the material with different lattice constants. Silicon accounts for about 27% of the crust, and is the second most abundant element on earth, so it is a material suitable for mass production in terms of the abundance of resources and its safety. In addition, it is the most popular solar cell material at present, and the ratio of crystalline silicon type to the production of solar cells is 86.8% of the total in 2011 [14]. In the all-silicon solar cell, a single crystal silicon solar cell is used for the bottom cell (as shown in Figure 9), and a silicon material having a wider band gap is used for the top cell. In order to fabricate this solar cell, it is essential to develop a silicon material with a wider band gap.

In recent years, it has become possible to control the band gap by nano-sizing the silicon and using the quantum size effect. It has been reported that the band gap of bulk silicon can be expanded from about 1.1 eV to about 1.9 eV by reducing the size of the silicon material to several nm [14]. Among these, one of the most prominent nanosized silicon-based materials are Si nanowire [15], [16] and nanopore arrays [17], [18]. These structures are comprised of a series of vertically aligned silicon nanostructures, which not only reduce the volume of the

absorber layer, but also provide near-ideal photon absorption across the solar spectrum for improved efficiency. It has been suggested similarly that nanosizing band gap can be expanded by nano-porosity [19], and it has been suggested that, with nano-porosity, the quantum size effect is induced. Moreover, the nanoporous structures also offer another benefit, which is the enhanced light-trapping property that improves the effective light-path length in the semiconductor materials [20]–[22]. This occurs when the pore size on the surface is equivalent or greater than the wavelength of the incident light. In case of porous silicon, when its porosity is increased, the reflectance can be reduced to 3~30% while the band gap is increased [23], [24]. Because of these distinguishing features, porous silicon is a promising material for use in PV technology and an intriguing candidate for the top absorber in silicon tandem solar cells [25].

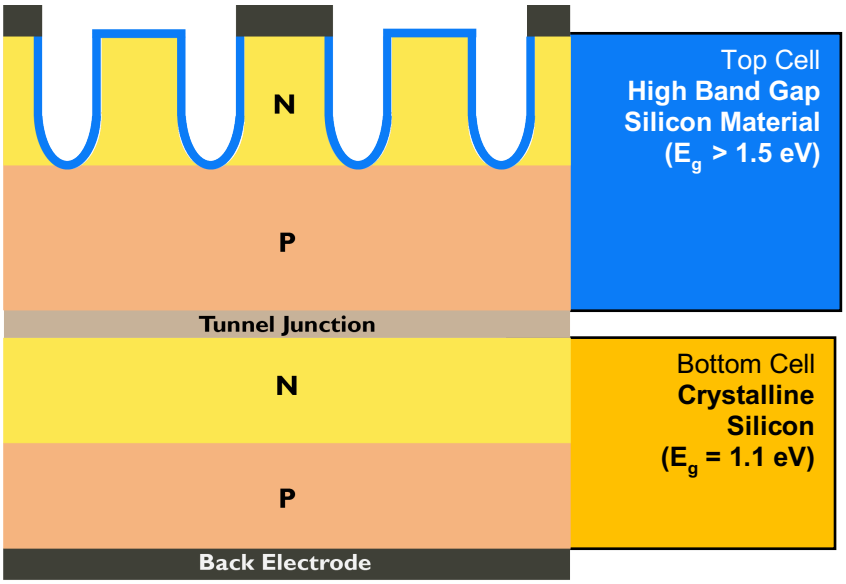


FIGURE 9: THE SELECTION OF MATERIAL AS A TOP CELL REGARDING TO ITS BAND GAP ENERGY

1.5 Porous Silicon as a Candidate of the Top Cell of Tandem

Porous silicon is a silicon material with a porous structure and is classified into microporous (<2 nm), mesoporous (2 to 50 nm), and macroporous (> 50 nm) according to the pore size. The porous silicon can be fabricated by using a wafer as an anode and a platinum as a cathode, then applying the anodic oxidation using hydrofluoric acid to etch the surface. It is known that the structure of porous silicon changes largely depending on reaction conditions (electrolyte, current density, oxidation time, temperature, presence or absence of light

irradiation) and silicon substrate (resistivity, conductivity type, plane orientation). By changing these conditions, the structure of porous silicon can be controlled to some extent [26]. The application of porous silicon to solar cells plays an important role as an antireflective film [27], [28], utilizing the increase of open voltage with increase of band gap by quantum size effect [29], and texture structure and lower refractive index compared with bulk silicon. It is expected as a top cell material for tandem solar cells. When porous silicon is used as a solar cell material, it is necessary to improve defects such as an increase in surface area per volume, an increase in oxidation and surface recombination, a high resistance value, and a low light absorption coefficient.

1.6 Surface Passivation

The surface passivation is a method to limit the recombination rate of the solar cell by using a non-conductive material to deactivate the dangling bonds on the surface, which are the unsatisfied valence electron on the immobilized atoms (shown in red dashed circle in Figure 10). This dangling bond plays an important role in semiconductor device operation as it can decrease the solar cell parameters by creating the extra trap energy state that has lower energy level than the conduction band (Figure 11), which causing the excited electron to fill in this energy level rather the conduction band where electron can be collected and used as electricity.

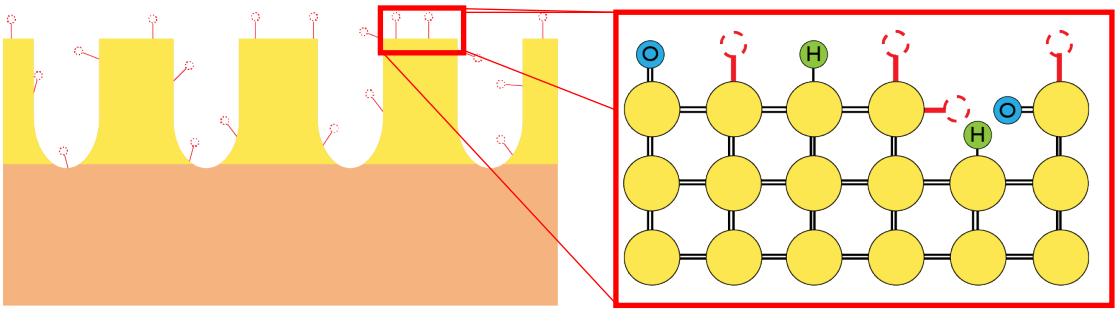


FIGURE 10: DANGLING BONDS ON THE SURFACE OF POROUS SILICON

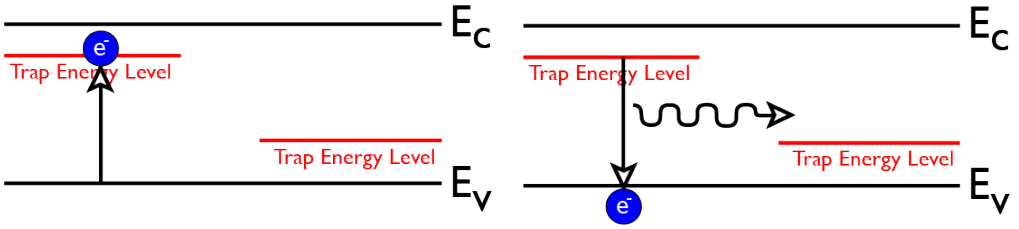


FIGURE 11: TRAPPED ENERGY LEVEL CAUSED BY DANGLING BONDS

In order to reduce the loss due to surface recombination shown in 1.3.1, passivation is one of the most critical processes for fabricating high-quality solar cell. In single crystal silicon solar cells, various materials such as alumina, amorphous silicon, silicon dioxide (SiO_2), and silicon nitride (SiN) are used extensively. There are various methods to passivate the surface. The most common method is the atomic layer deposition (ALD) that deposit the passivating atom on the surface layer by layer, in which it replaces the dangling bonds, then annealing with high temperature to form the thin film on the surface [30], [31]. In terms of the passivation of the silicon with planar surface, alumina (Al_2O_3) films deposited on silicon surfaces via ALD process provides the negative fixed charges at the Al_2O_3/Si interface, thus results in a greater passivation quality for the n-type-based solar cells with p^+ emitters [32], [33]. For p-type solar cells with phosphorus diffused n^+ emitters, SiO_2 can be deposited to provide an effective passivation film due to their excellence in passivating the Si-SiO_2 interface [34]. The recent study shows that the thin SiO_2 film with thickness of 70 nm formed by the anodic oxidation process at room temperature can demonstrate an exceptional surface passivation quality and stability on the crystalline silicon substrate with an efficiency of more than 23% [35]. However, the application of the anodic oxidation to the nanostructured silicon has not been extensively studied yet.

As porous silicon, which is a high aspect-ratio nanostructures with large surface areas, has a high tendency to be oxidized uncontrollably by the spontaneous process of native oxidation when exposed to the atmosphere [36], [37], many studies on various passivation techniques have been conducted to improve the surface stability of the porous silicon. For instance, the wet thermal oxidation [38]; the rapid thermal treatment in NH_3 [39]; and the room temperature oxidation with ozone [40]. However, as these passivation techniques are not applied to the porous silicon with p-n junction, they might not be able to use for the photovoltaics purpose and might only limit to the other applications like biosensors and microelectronics where the porous silicon is used as the photoluminescence (PL) emitting materials. For the applications in photovoltaics, at the present time, the nanostructured silicon-based solar cells without surface passivation [41]–[43] show inferior efficiencies compared to the conventional crystalline silicon cells. The major obstacles that prevent porous silicon from being used in solar cell applications are associated with the increased photocarrier trapping at the remarkably increased surface area of nano-porous silicon, resulting in reductions in both the short-circuit current and open-circuit voltage of the device, and thus decreasing the

efficiency. This suggests that the surface passivation of the porous silicon is critical for improving the performance of the nanostructured solar cell.

To effectively passivate the porous silicon, additional technological challenges must be established; these include the controllability of silicon oxide thickness in nanometer scale, the controlling of the homogeneity of the passivated films, and the preservation of the original porous structure. Oh et al. fabricated a black silicon on the p-type-based solar cell with a thermal silicon oxide passivated layer that gave a high efficiency of 18.2% and a low effective recombination velocity of 53 cm s^{-1} on the surface [44]. However, although having a little influence on the structure when applied to crystalline silicon, the thermally grown silicon oxide technique has a restriction when applied to porous silicon nanostructures with a high aspect ratio of 400:1 [45] due to its thermal sensitivity. The thermal SiO_2 deposition has an operating temperature in the range of 400–1100 °C [38], [39], which is high enough to damage the nano-porous structure [46]. As a result, the technique for depositing an oxide passivation layer on nanostructured silicon must be devised in such a manner that the thickness of the oxide can be precisely controlled to avoid the total oxidation, while the original structure must be retained by limiting the maximum processing temperature to be low enough that it is not deteriorating or causing any undesired structural changes.

One of the other possibility passivation methods is to use the supercritical fluid. The supercritical fluid method is also considered to be an effective passivation method as the supercritical fluid has advantageous properties of gas-like diffusivity and liquid-like dissolubility in the same time [47]. This is suitable for the nanostructure as the supercritical fluid can penetrate through the pore structure and deactivate the dangling bonds inside the deep pore's wall. Furthermore, some substances, like CO_2, becomes the supercritical fluid state in very mild condition (32°C, 7.39 MPa), which can be used to carry the passivating molecule to the thermo-sensitive material like porous silicon [48]–[50].

1.7 PROSPECTIVE SCALABILITY OF POROUS SILICON SOLAR CELL

With the currently available technologies for fabricating the porous silicon layer in more scalable volume or in the industrial scale [51], e.g., in microelectronics [52] and industrial microelectromechanical systems (MEMS) manufacturing [53], together with the double layer transfer process (DLPS) technology that allows the utilization of the silicon wafers in a more

efficient way, thus reduces the manufacturing cost [18], [54], [55], the fabrication of porous silicon and the silicon oxide passivation could be implemented, with some optimization of the process, in the actual photovoltaics industrial scale. Hence, as an important step toward developing a more viable passivation technique to be applied to porous silicon as the top emitter of silicon solar cell, the room temperature electrochemical passivation emphasizes the promising possibility that this fast and inexpensive method can improve the passivating quality of the porous silicon layer as well as enhance the light-trapping property in thin-film silicon solar cells and possibly be used as a wide band gap top-cell material in all-silicon tandem solar cell applications in the next generation PV cells.

CHAPTER 2: STATEMENT OF PURPOSE

The development of a clean and sustainable energy is an important issue for the future of global economics and environment. Among many renewable energy technologies, silicon solar cells have attracted an attention due to the stability and abundance of Si semiconductor material with suitable optoelectrical properties. However, the best single junction solar cells have reached the efficiency of 26.7% in laboratory that is very close to its theoretical limit of 32%, which means that there only a little room remained for improving the efficiency of the solar cell. To improve the solar cell efficiency and surpass the theoretical limitation introduced previously, the porous silicon is chosen as a promising material the top layer of all-silicon tandem solar cells. This is attributed to the improved optoelectronic properties of porous silicon which are due to its reduced surface reflectivity and its possibly wider band gap, which was previously attributed to the quantum size effect. It also eliminates the lattice mismatch issues usually found in other type of multi-junction solar cells. However, the fabrication process of porous silicon greatly increases the surface area and leaves behind dangling bonds on the top surface. These dangling bonds acts as recombination centers and directly affect the carrier extraction in a photovoltaics device. This can be mitigated by the passivation of the porous silicon layer. However, the passivation of this sensitive surface is a challenging problem as the common method that applies to crystalline silicon solar cells may not be able to achieve a uniform passivated film on the high-aspect ratio structure like porous silicon. A key purpose of this thesis is to develop a different electrochemical passivation method of porous silicon most suitable for all-Si tandem solar cells.

To achieve this purpose, we need to address specific sub-problems, which are:

- The fabrication process of porous silicon
- The process of electrochemical passivation
- The properties of passivated porous silicon
- The performance of porous silicon in a solar cell

First, the fabrication process of porous silicon is considered. In this research, the p-type crystalline silicon is used as the base layer. The wafer is cleaned, doped, and annealed to

fabricate the p-n junction with suitable junction depth. We then use a simple, fast, and low-cost method of electrochemical etching (anodization) to prepare porous silicon layers on the N+-emitter region. The current density and anodization time are selected according to the literature and previous research to obtain the desired porosity and porous layer thickness, which are key features in determining its optoelectronic properties. The purpose of this is to obtain the porous structure in the N+-emitter region with proper porosity that can reduce the surface reflectivity in ultraviolet (UV) and visible regimes (300-1100 nm), which normally are inefficiently absorbed in polished crystalline silicon wafers, as well as the proper thickness, so that the surface recombination can be controlled. Also, we would like to investigate this nano-sizing effect of the porous silicon with this structure with regard to the possibility of band gap expansion in this heterojunction structure.

For the process of passivation, the electrochemical passivation was applied to passivate the surface immediately after the porous silicon layer is fabricated. This approach was chosen over more conventional high temperature passivation processes because it enables the precise control of the thickness of the oxide layer with a quick processing time at room temperature. This lowers the risk of negatively affecting the porous silicon's original nanostructure. The passivation current density is determined according to the diffusion and reaction rate of the oxidation of porous silicon, which will be elaborated later in discussion part. The passivation times will be varied to investigate the effect of oxide thickness. The purpose of this variation is to produce the passivated porous silicon with the sufficient oxidation of the dangling bond surface states as well as the uniform silicon oxide layer to provide an adequate passivation to be used in photovoltaic application. In comparison to our original method of electrochemical passivation, the other methods are also investigated, including the conventional ALD as well as the supercritical fluid passivation. For clarification, because we would like to evaluate only the true effectiveness of the SiO_2 passivation layer, any further fabrication process (except electrode deposition) will not be conducted in this research, e.g., back surface field (BSF).

For the properties of passivated porous silicon, many characterizations are conducted to evaluate each fabrication conditions. The depth of p-n junction from the surface and the porous structure (the porous layer thickness, the thickness of the pore wall, and the pore spacing) are characterized as these are important determinants of the final optoelectrical properties of the porous silicon. The optical and vibrational spectrum are measured to evaluate

the optoelectrical properties of the fabricated porous silicon. These reflectance, transmittance, and absorbance data can be used to estimate the band edges as well as the quantum efficiency in last section. Finally, estimation of the band gap energy of porous silicon is made to verify the possibility of the expansion by the spectroscopy technique.

Furthermore, the performance of porous silicon as solar cells is investigated. The silver (Ag) electrodes are deposited on both front and rear side of all samples to fabricate the solar cell. The structure would be as follows (from top to bottom):

Ag front electrode/ SiO_2/N+ emitter porous silicon/ P-type *c*-Si/Ag back electrode.

The effect of the passivation duration is evaluated by the photovoltaic performance measured with solar simulator; these include the current density-voltage (J-V) curve, open-circuit voltage (Voc), short-circuit current density (Jsc), fill factor (FF), efficiency (η), shunt resistance (R_Sh), and series resistance (R_S). The external quantum efficiency (EQE) data were measured, while the internal quantum efficiency (IQE) was calculated based on the reflectance data from characterization from previous section, to evaluate the quantum efficiency. The bare c-Si solar cell is used as a reference cell and to evaluate the improvement of the passivated porous silicon solar cell.

Finally, we will evaluate key properties of passivated porous silicon which are important for solar cells performance, namely: the band gap and band edges. To achieve mechanistic understanding of the resulting properties, we will also perform numerical calculations with quantum chemistry and molecular dynamics methods. This computational method allows us to obtain a direct insight at the atomistic model of the structure as well as the effect of porosity and different degree of passivation onto the specific electronic properties such as band structure, trap states, and the expansion of band gap. This is necessary as some of the mechanistic underpinning of the changes of properties due to porosity and passivation cannot be understood with experimental approach alone. In particular we will test a key proposition advanced in previous literature about the band gap expansion via quantum sizing effect. Therefore, this part of the study will investigate the effects of porosity and passivation on the porous silicon model with the relatively large size (up to ~6500 atoms). The models are based on crystalline structures, where the pores are introduced according to the actual

experimental visual data following by the passivation with hydrogenation. The models are optimized with Molecular Dynamics (MD) method following by Density Functional Tight Binding (DFTB) method. For the characterization, the density of states (DOS) is calculated to investigate the band structure of the model. The results from simulation are used to compare to the actual experimental data

CHAPTER 3: METHODS AND MATERIALS

In this chapter, the methods and materials of each experiment will be explained and calculation as well as the methodology of the research. Beginning with the overview part, this includes the methodological approach towards the research problem and the scope of work as described in the previous chapter, and the evaluation of the result. Afterwards, the experimental and computational details will be explained according to the methodological approaches. The explanations will be divided mainly into two parts–experimental and simulation–for the sake of simplicity, even though the results of experiments and simulations will be discussed collectively in the next chapter.

3.1 Overview of Research

This research will focus on the investigation of the porous silicon as a candidate for the top cell of all-silicon tandem solar cell as well as the improvement of the surface passivation methods of porous silicon. For the experimental part, the explanation will follow the fabrication process, which includes the fabrication of porous silicon, the processes of passivation, and, finally, the fabrication into the solar cell device. Along with each step, the characterization methods will be listed, and its purposes will be described.

For the experimental part, firstly, the porous silicon as a material will be evaluated with following characterizations:

1) SEM image: Porous layer thickness, porous structure from top view
2) TEM image: Porous structure in detail and PN-junction depth
3) Electrochemical CV (ECV): PN-junction depth and doping profile
4) PL spectroscopy: Estimation of band gap energy
5) UV-Vis spectroscopy: Optical spectrum
6) FTIR spectroscopy: Vibrational spectrum

In this part, the scanning electron microscope (SEM) image, transmission electron microscope (TEM) image, and electrochemical capacitance-voltage (ECV) profiling is used to confirm the structure of the porous layer as well as the doping profile of N+ emitter layer, i.e., p-n junction depth. The relationship of porous layer depth in relation with p-n junction is believed to have

a significant effect on the role of porous silicon as a top layer in tandem solar cell; this will be explained in the next chapter. Next, photoluminescence (PL) measurement is used to estimate the band gap of the porous silicon compared to the crystalline sample to investigate the effect of nano-structuring: the conversion of indirect to direct band gap material, and any change/expansion of the band gap. Lastly, the UV-Vis and Fourier Transform Infrared (FTIR) spectrophotometry are used to obtain the information about the optical and vibrational responses of the samples: reflectance, transmittance, absorbance. These results will also be used to calculate the internal quantum efficiency (IQE) to characterize the light response of the sample as a solar cell.

Secondly, the passivated porous silicon will be evaluated using the following characterizations:

1) QSSPC: Carrier lifetime and implied V_{OC}
2) MWPCD: Carrier lifetime
3) SEM image Structural change
4) TEM image: Structure of passivated film (only ALD)

Quasi-steady-state photoconductance (QSSPC) measurement is used to investigate the quality of the base silicon wafer, the N+ emitter layer, and the metal-semiconductor contact in term of its carrier lifetime and the implied V_{OC}. Microwave-detected photoconductance decay (MWPCD) measurement is used to investigate the carrier lifetime of every passivation technique as well as the sample without any passivation to confirm the quality of passivation. SEM image is used to check the structural change after passivation. TEM is used only with ALD-passivated sample to investigate the post-annealed alumina film and confirm the uniformity of the passivation film and its thickness.

Lastly for the experimental part, the final passivated porous silicon solar cell will be evaluated as by solar simulator to obtain the IV-curve, EQE, and IQE data. The open-circuited voltage (V_{OC}), short-circuited current (J_{SC}), fill factor (FF), shunt and series resistance, and conversion efficiency will be extracted from IV-curve data.

For the simulation part, a porous silicon model is made to represents key features of the experimental samples. This includes the porosity and the amorphization according to the real characterization data. The effect of passivation is studied by varying the amount of passivating material on the surface of the pore. The models are then relaxed or optimized using

computational chemistry methods and codes, and the resulting electronic properties like density of states (DOS) is calculated and used as the determinants of the effect of passivation. In this research, three types of calculation method are used: Density Functional Theory (DFT), Density Functional Tight-Binding (DFTB), and Molecular Dynamics (MD). The software/code for each method are listed as following:

1) QuantumEspresso (QE): DFT calculation
2) DFTB+: DFTB calculation
3) GULP: MD calculation

The basic principle of each calculation, the software/code, and the parametrization will be explained in this latter part of the chapter. The advantages and disadvantages of each method will be discussed as it is important to choose an appropriate method to obtain the best result, while keeping the cost and time of calculation reasonable. Also, the related software will also be introduced and briefly explained its purposes.

3.2 Methods of Experiment

3.2.1 Overall Fabrication Flow

To understand the whole picture of the process, the overall process to fabricate the passivated porous silicon solar cell is shown in Figure 12. As there are many characterizations between each step of fabrication, it will be illustrated again in each section.

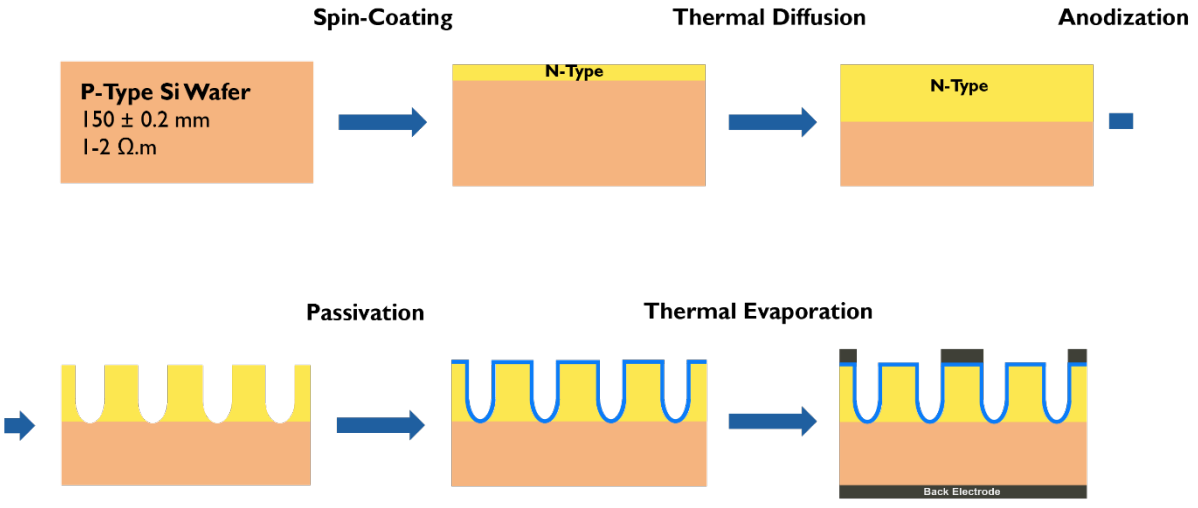


FIGURE 12: OVERALL PASSIVATED POROUS SILICON SOLAR CELL PROCESS

Totally, there are three steps of fabrication that are needed to be explained. Briefly, the process will be as following:

Porous Silicon → Passivated Porous Silicon → Passivated Porous Silicon Solar Cell

3.2.2 Porous Silicon Fabrication

Materials

Silicon wafer, P-Type, <100>, 1-2 Ω.cm, 200 μm
Hydrofluoric acid (46-48%) Wako Pure Chemical Industries, Ltd.
Ethanol (99.5%) Kanto Chemical Co., Ltd.
Phosphorus SOD (Spin-on Dopant) Standard Solution P8545PV Filmtronics

Equipment

Precision Manual Scriber IZU-SC-150 Izumi Tech Co., Ltd.
Spin Coater Opticoat MS-B100 Mikasa
Mini Lamp Annealer MILA-5000 series Advance Riko, Inc.
Circulating Chiller EYELA CCA-1111
DC Voltage Current Source/ Monitor R6240A Advantest
In-house Teflon Electrochemical Etching Equipment

Experimental Operations

For porous silicon with P-N junction

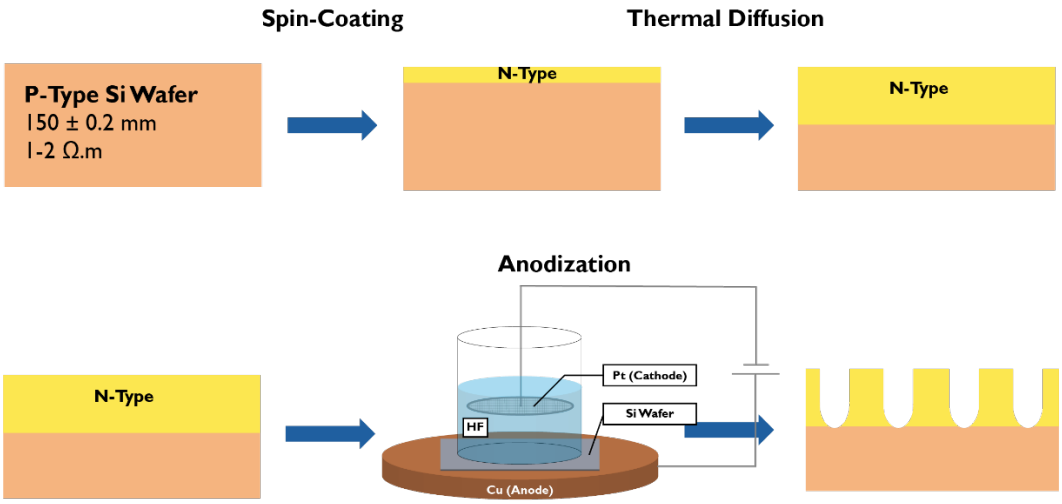


FIGURE 13: POROUS SILICON (DOPED) FABRICATION

1) Silicon wafer is cut from into 3×3 cm^2 with the precision scriber.
2) Clean the silicon wafer with ethanol and deionized (DI) water twice to clean the dust and grease on both front and rear surfaces. Then immerse the wafer into HF_{aq} 10% (w/w) for 1 minute to remove the native oxide film. Finally, immerse in the DI water for 30 seconds to wash the remaining HF.
3) To dope the wafer, the phosphorus SOD solution of 100 µL is spin-coated on the front surface. The condition of spin-coating is set according to the manufacturer's technical data to assure the uniform film thickness profile (with rpm) and enough time for the solvent to evaporate (with spinning time). These are illustrated in Figure 14 and in following detail:
    a. [0-5 second] accelerate from 0 to 1000 rpm
    b. [5-8 second] keep at 1000 rpm (SOD is dispensed at 5th second)
    c. [8-25 second] instantly increase to 1500 rpm

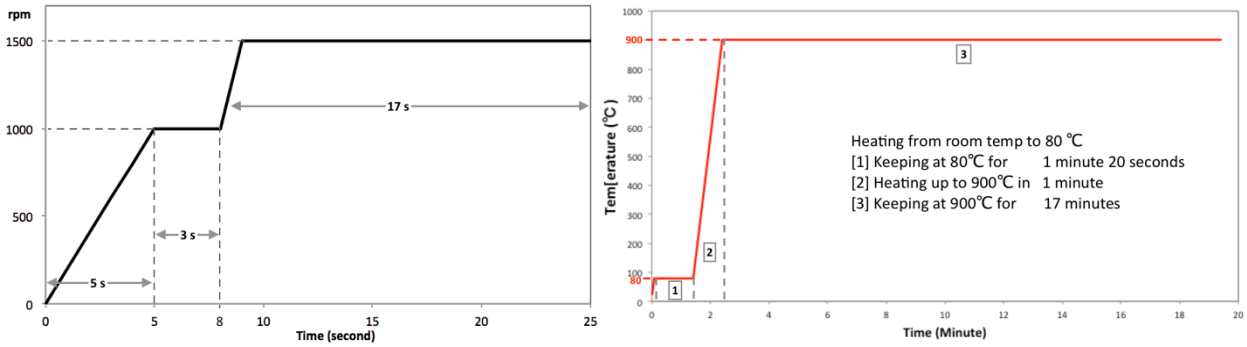


FIGURE 14: CONDITION OF SPIN-COATING AND THERMAL DIFFUSION

4) For thermal diffusion, spin-coated silicon wafer is subsequently annealed to form the N+ emitter layer at top layer. The condition of temperature is shown in Figure 14. The first

80°C step for 1 minute and 20 seconds is to ensure the evaporation of the solvent remained in the phosphorus film. The temperature is then increased with the rate of 10°C/s until reaching 900°C, which is adequate to activate the drive-in process of phosphorus into silicon material. The duration of 17 minutes is kept to obtain the desired thickness of N+ emitter layer as well as the doping profile. The chamber is continuously flowed with N_2 with constant flow rate of 20 SCCM to prevent the oxidation of phosphorus by heating.

5) To fabricate the porous silicon with P-N junction, the anodization process is performed to etch the silicon surface. As shown in Figure 13, the Si wafers are placed horizontally at the copper base of the Teflon wet-etching cell [18], [56], where the surface to be etched is faced upside. The copper base is used to provide a lower electrical contact to the wafers. The cylindrical etching chamber is then placed and tightened on the top of Si wafers with the use of 20-mm-diameter O-ring to prevent the leak of the electrolyte. The 4 mL of the electrolyte of 46% HF: 99.5% ethanol = 1:1 solution is sequentially filled. The 15-mm-diameter platinum net (cathode) is immersed in the electrolyte, and its position is adjusted to be at the center of the etching chamber. Finally, the etching process is performed under indoor irradiation conditions at room temperature. The constant current of 75 mA/cm^2 is applied through the wafer by using current source for 6 seconds.
6) The etched wafer is removed from the etching cell after washing with DI water, and dry.
7) The porous silicon wafer is cut to 1×1 cm^2 by the precision scriber (in the case of non-passivated sample).

For porous silicon <u>without P-N junction</u>

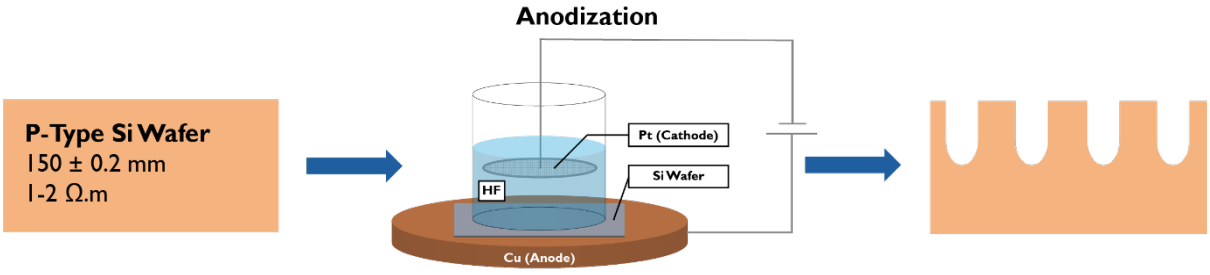


FIGURE 15: FABRICATION OF (UNDOPED) SILICON WAFER

1) Silicon wafer is cut from into 3×3 cm^2 with the precision scriber.
2) Clean the silicon wafer with ethanol and deionized (DI) water twice to clean the dust and grease on both front and rear surfaces. Then immerse the wafer into HF_{aq} 10% (w/w) for

1 minute to remove the native oxide film (SiO_2). Finally, immerse in the DI water for 30 seconds to wash the remaining HF.

3) To fabricate the porous silicon without P-N junction, the solution of [HF_{aq}: Ethanol = 1:1] of 4 mL is used as an electrolyte and etching agent. Then the constant current of 75 mA/cm^2 is applied through the wafer by using current source for 200 seconds. The reaction is carried out in the indoor irradiation. The reason the reaction time is increased is because the high resistance of undoped wafer. The voltage required to generate 75 mA/cm^2 current density is higher than the upper limitation of the current source.
4) The etched wafer is removed from the etching cell after washing with DI water, and dry.
5) The porous silicon wafer is cut to 1×1 cm^2 by a vacuum-stage cutter.

3.2.3 Passivated Porous Silicon Fabrication

Passivation Methods

Atomic Layer Deposition (ALD) Passivation

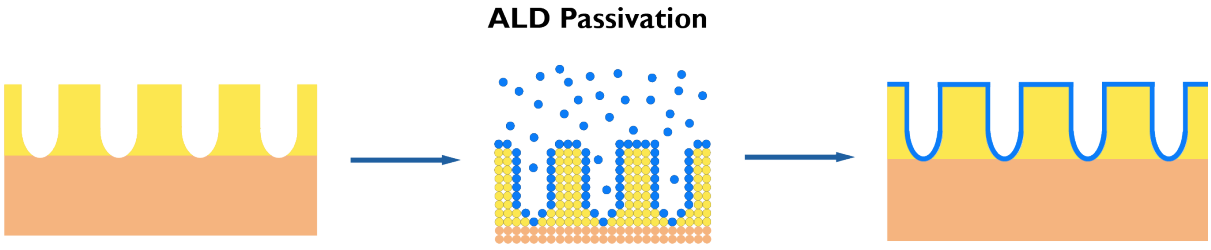


FIGURE 16: ALD PASSIVATION PROCESS SCHEME

Materials

Trimethylaluminum (TMA)

HF_{aq} 5% (w/w)

Experimental Operations

1) Porous silicon wafer is cleaned by dipping in HF_{aq} 5% solution for 7-8 seconds to remove the native oxide. It is then rinsed with DI water and dry with N_2.
2) The ALD passivation is done by using TMA as Al source in Ar atmosphere to control the deposition thickness of 5, 10, and 20 nm.

3) Then it is annealed at 400°C for 30 minutes in N_2 atmosphere to form Al_2O_3.

Electrochemical Passivation

By using the anodization process in H_2O/HCl at ambient temperature, the Si surface, including the dangling bonds (surface states) formed by the etching on the porous silicon layer, is anodically oxidized and the thin silicon oxide layer is formed. The anodic oxidation reaction is as follows:

$$Si + 2H_2O \leftrightarrow SiO_2 + 2H_2 \quad \text{.....(8)}$$

In order to confirm that the porous silicon layer is not completely oxidized, the volume ratio of SiO_2 thin film per volume of porous silicon layer in each passivation time is calculated based on the porosity and the kinetic of the anodization reaction (8) [57].

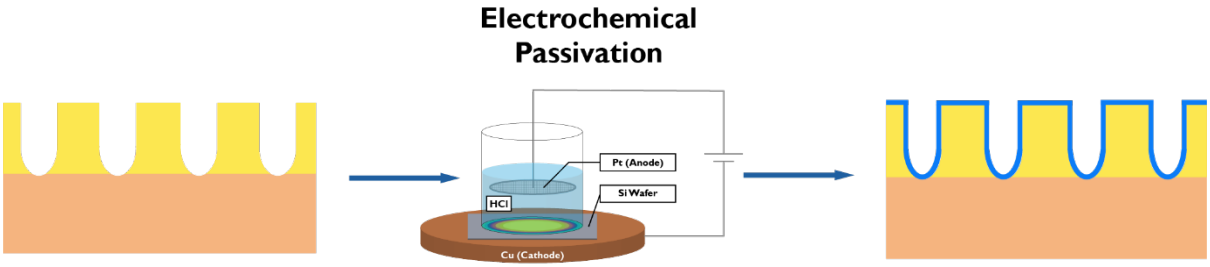


FIGURE 17: ELECTROCHEMICAL PASSIVATION PROCESS SCHEME

Materials

HCl 1M

Equipment

DC Voltage Current Source/ Monitor R6240A Advantest
Teflon Electrochemical Etching Equipment

Experimental Operations

1) From 3.2.2., the etched porous silicon wafer is continuingly processed by removing all HF solution and rinse with DI water twice.
2) 4 mL of HCL 1M is added to the Teflon etching cell. This time, the copper plate is used as a cathode, while platinum mesh is used as an anode. Then the constant current density of 0.1012 mA/cm^2 is applied through the wafer by using current source for specific amount of time. The reaction is carried out in the indoor irradiation.

Supercritical Fluid Passivation

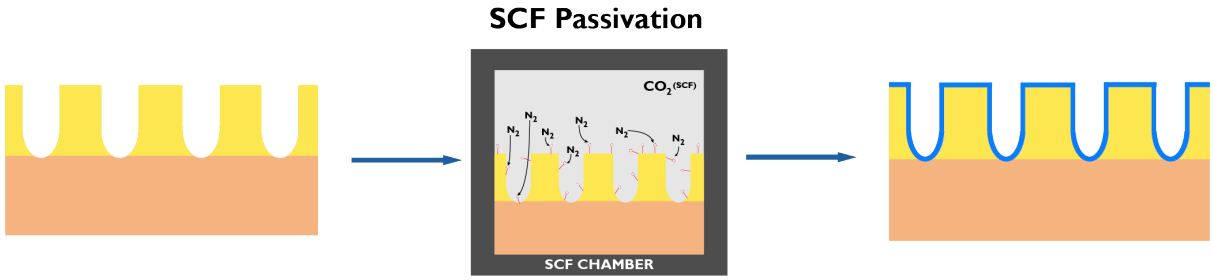


FIGURE 18: SUPERCRITICAL PASSIVATION PROCESS SCHEME

Materials

N_2 (gas)

CO_2 (liquid)

Equipment

Thermostat Oven ETTAS EO-300B As One Corporation

High Pressure Cell SUS316 25 MPa 100°C Taiatsu Japan

In collaboration with Shimoyama laboratory, Tokyo Institute of Technology

Experimental Operations

1) Porous silicon wafer is passivated by nitrogen gas with supercritical CO_2 as a carrier inside the pressurized container. N_2 is filled in the chamber until reaching 5 MPa. Then the liquid CO_2 is flowed into the container by pump until the overall pressure reaches 20 MPa.
2) The system is keeping as a batch process at 20 MPa and 100°C for 2 hours.

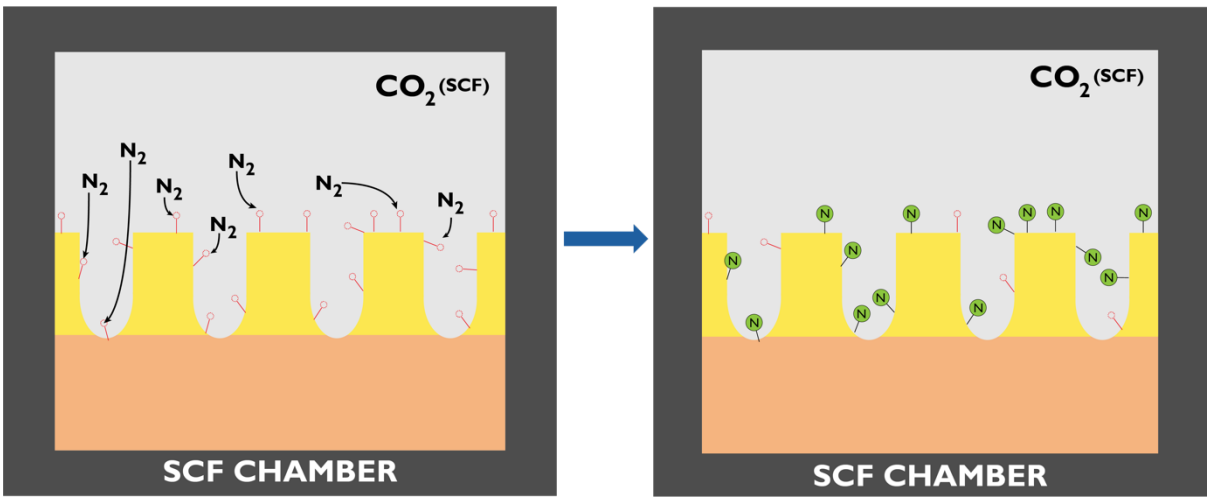


FIGURE 19: SCF PASSIVATION REACTION SCHEME

3.2.4 Solar Cell Fabrication

Materials

Tungsten Wire (W-46187, Diameter: 0.25mm), Nilako
Silver Wire (Ag-401325, Diameter: 0.30 mm), Nilako

Equipment

Volt-Slider Type V-130-3 Yamabishi
In-house Resistive Thermal Evaporator Chamber
Fishbone and Square Electrode Masks

Experimental Operations

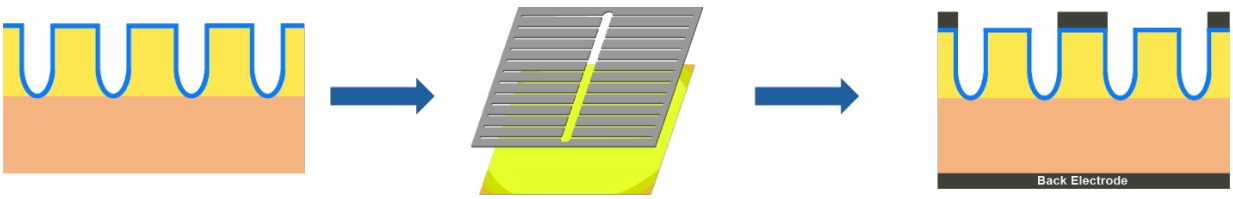


FIGURE 20: ELECTRODE DEPOSITION OF SOLAR CELL

1) Passivated silicon wafer from section 3.2.3 is cut from 3×3 cm^2 to 1×1 cm^2 by the precision scriber.
2) The cut wafer is attached firmly to the fishbone electrode mask with an area of 0.39 cm^2 by adhering to the glass substrate with tape and put in the in-house resistive thermal evaporator chamber. Then it is vacuumed for 30 minutes. Before applying the current, the N_2 gas is filled in the chamber 3 times to ensure that there is as small amount of air as possible.
3) The current is flowed through the coiled tungsten wire to heat 6 silver hooks (5 mm in length each) for 30 seconds, which evaporates the silver due to resistive heating, the voltage is adjusted by the volt-slider. The silver thin electrode thickness is 40-60 nm. Then refill the silver hook and repeat this step one more time.
4) Detach the fish bone electrode mask and continue to deposit the rear electrode with the square mask with same process.

3.2.5 Characterizations Methods and Materials

A. FESEM

Materials

Carbon tape
Carbon paste

Equipment

Field Emission Scanning Electron Microscope (FE-SEM) JSM-6301FZ JEOL
Platinum Auto Fine Coater JFC-1600 JEOL
Image Analysis Software ImageJ

Characterization Operation

1) Cleave the samples to small size to fit both flat stage and cross-sectional stage.
2) Using carbon tape and carbon paste to adhere the sample flat on the stage surface.
3) Coat with platinum to improve the conductivity for 8 seconds.

4) Observe the structure or cross-section with FE-SEM under low pressure (< 9.6×10^{-5} Pa). The voltage of 5 kV is used.

B. Electrochemical Capacitance-Voltage (ECV) Profiling

Equipment

WEP Wafer Profiler CVP21, Furtwangen, Germany (in collaboration with INSA, Lyon)

Characterization of Method and Operation

The doping profile and the depth of the PN-junction interface formed by this doping condition are characterized by the electrochemical capacitance voltage (ECV) method. This ECV measurement is performed by etching the surface of the samples and measure the capacitance voltage value at each depth, which can be interpreted concentration of the dopants.

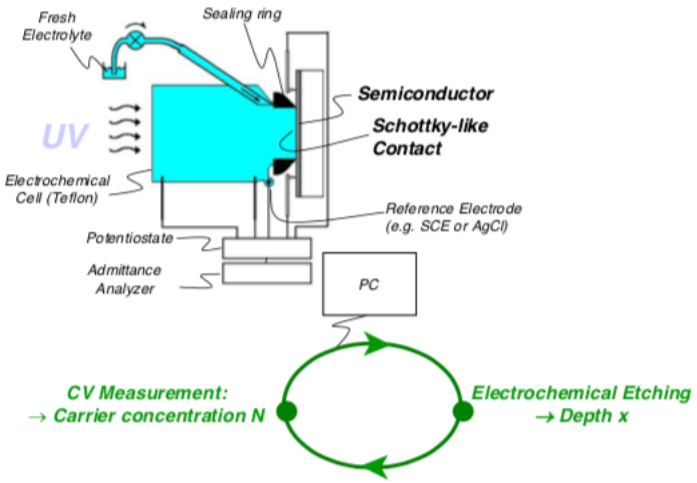


FIGURE 21: ELECTROCHEMICAL CV-PROFILING SCHEME [58]

1) Immerse the doped samples without porous structure in the HF_{aq} 10% (w/w) for 7 minutes to remove the phosphosilicate glass (PSG), which is a non-conductive layer.
2) The sample is pressed to the electrochemical cell filled with electrolyte with 5 mm in diameter sealing ring. The electrolyte also acts as an etching agent, which etch the wafer with specific depth and the capacitance in each depth is then measured. The capacitance is interpreted as the carrier concentration with Mott-Schottky equation (Equation 7).

$$N = \frac{-2}{e\varepsilon_0\varepsilon_R \bullet \frac{d(1/C^2)}{dV}} \qquad \text{…….(7)}$$

Where C: Capacitance per Area

A: Contact area

ε_R: Relative dielectricity if the semiconductor

e, ε_0: Fundamental constants

3) Repeat the measurements with three samples

*Note that the etching process referred in the "etching area" is an electrolytic etching of the doped c-Si carried out solely for the purpose of ECV profiling of the carrier concentration at various depths from the surface and is different from the etching process described in the previous section for fabricating the porous silicon layer.

C. Estimation of Band Gap using Photoluminescence (PL)

Equipment

NIR Compact Fluorescence Lifetime Spectrometer C12132 (Class B Laser) Hamamatsu Variable Temperature Liquid Nitrogen Cryostat (Optistat DN2) Oxford Instruments (in collaboration with Yamada-Miyajima laboratory, Tokyo Institute of Technology)

Characterization Operation

1) Apply the thermal grease to the rear side of sample to improve the thermal conductivity.
2) Vacuum the system and flow in the N_2 into the chamber 5 times to purge the air out. Then vacuum the system with charcoal heating (308 K) for 8 hours or until the pressure is under 2×10^{-5} hPa.
3) Pour in the liquid nitrogen to cool down the system to 77K.
4) Measure the PL between 580 – 1030 nm with spectrometer of 532-nm excitation wavelength for each temperature: 80, 130, 180, 230, and 298 K.

D. Characterization of the optical properties by UV-Vis

Equipment

SolidSpec-3700 UV-Vis-NIR spectrophotometer, Shimadzu (in collaboration with Miyajima laboratory,Tokyo Institute of Technology)

Characterization Operation

1) Prepare the samples with the desired fabrication condition.
2) Measure the background first before continuing to measure the samples the atmosphere in the range of 300-2400 nm.

E. Characterization of the vibrational spectrum by FTIR

Equipment

IRAffinity-1 FTIR spectrophotometer, Shimadzu (in collaboration with Miyajima laboratory,Tokyo Institute of Technology)

Characterization Operation

1) The samples are prepared with the desired fabrication condition, except that it is not needed to cut the sample from 3×3 cm^2 into 1×1 cm^2 in size.
2) Measure the background first before continuing to measure the samples in the N_2 atmosphere in the range of 500-4000 cm^{-1}.

F. Carrier Lifetime Measurement by MWPCD and SEMILAB

Equipment

Lifetime Measuring System LTA-1510EP Kobelco (in collaboration with Miyajima laboratory, Tokyo Institute of Technology)

SEMILAB (in collaboration with Alain Fave's laboratory, INSA, Lyon)

Characterization Operation

1) The carrier lifetime of sample with 1×1 cm^2 size is measured by MWPCD system with following parameters:
    a. Measurement Pattern: 0.5 mm
    b. Wafer Size: 25 mm^2
    c. Average time: 1024 times
2) As the actual wafer size is 1×1 cm^2, which is smaller than 25 mm^2 measuring area, the average carrier lifetime value is then calculated by counting each data and average by hand.

G. QSSPC

Materials

Quinhydrone (0.05 M in methanol)

Equipment

WCT-120 The Standard Offline Wafer-Lifetime tool, Sinton Instruments (in collaboration with Miyajima laboratory, Tokyo Institute of Technology)

Characterization Operation

1. For the evaluation of the c-Si base layer, the bare wafer with 3×3 cm^2 is immersed in the quinhydrone/methanol (0.05M quinhydrone in methanol) for 10 minutes.
2. The measurement is done in the room temperature
3. For the evaluation of the other layer of the cell, fabricate the cell in the symmetrical configuration, and measure directly.

H. Nano-structure observation by Transmission Electron Microscope (TEM)

Equipment

Transmission Electron Microscope (TEM) JEM-2010F, JEOL, 200 kV
Focus Ion Beam (FIB) FB-2100

Characterization Operation

1) A FIB method is used to prepare the TEM specimens. In prior to the measurement, the surface of the porous silicon sample is coated with a 200-nm-thick carbon as a protective layer.
2) The material is excavated from both sides to a depth of 5 m using a beam of Ga+ ions to form a foil from the porous silicon layer.
3) The foil from the porous silicon layer is extracted and deposited on the TEM membrane.

K. Solar Cell Parameter measured by Solar Simulator

Equipment

Solar Simulator CEP-25MLH Spectrometer
Tungsten Carbide Probe (K15LM Type)
Sample Stand for Back Current Collector
Xenon Lamp Power Supply Model XCS-150A Jasco
Silicon Photodiode BS-520 S/N 096 Bunkoukeiki

Characterization Operation

1) The solar cell sample is put on the stage and connect the probe to the front electrode.
2) The J-V curve (shown in Figure 22) is obtained by irradiating the pseudo-sunlight generated by xenon lamp (AM1.5 100 mW/cm^2). The solar parameters: open-circuited voltage (V_{OC}), short-circuited current density (J_{SC}), fill factor (FF), and conversion efficiency is obtained from the equation 8 and 9
3) Furthermore, the shunt resistance (R_{SH}) and series resistance (R_S) are calculated by the slope at $V_{OC} = 0$ and $J_{SC} = 0$, respectively.

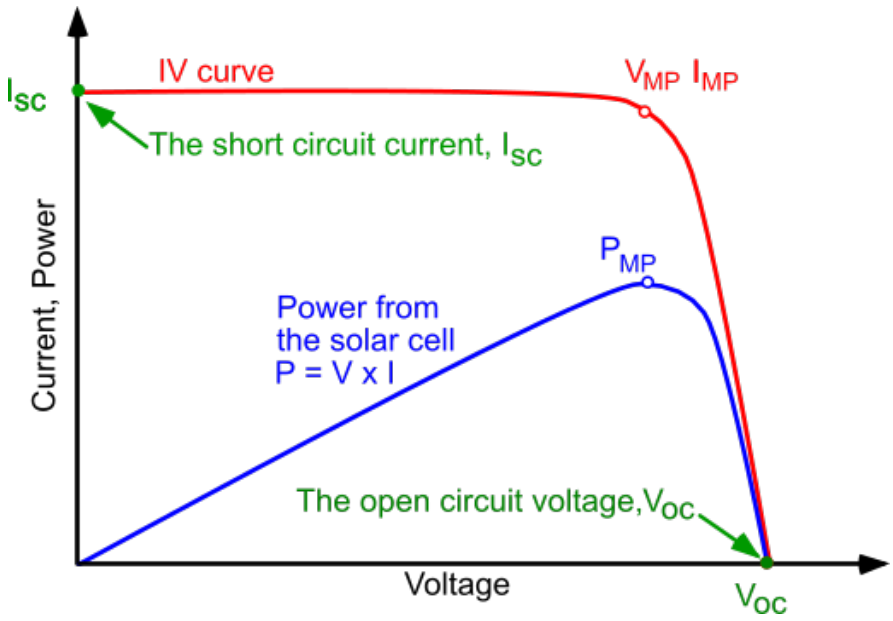


FIGURE 22: I-V CURVE OF SOLAR CELL [59]

$$\text{Conversion Efficiency } (\eta) = \frac{P_{\max}}{P_{in}} \times 100\% = \frac{J_{SC} \times V_{OC} \times FF}{Irradiance} \times 100\% \quad \text{.....(8)}$$

$$\text{Fill Factor (FF)} = \frac{P_{\max}}{J_{SC} \times V_{OC}} \quad \text{.....(9)}$$

Regarding the covered area of the Ag front electrode, the porous silicon and the c-Si cells absorb light in the region of 300–1200 nm, where the thin Ag electrode in this experiment has a low transmittance to, which means its effect to the absorbing region is negligible. As a result, the PV parameter may be determined by using the solar cell's active area.

L. External and Internal Quantum Efficiency Measurement (EQE and IQE)

Equipment

Solar Simulator CEP-25MLH Spectrometer, Bunkoukeiki
Spectral Response Measurement System (CEP-2000ML, Bunkoukeiki)
Xenon Lamp Model XCS-150A, JASCO
UV-Vis spectrophotometers V-570, JASCO
Tungsten Carbide Probe (K15LM Type)
Sample Stand for Back Current Collector

Characterization Operation

1) The solar cell sample is put on the stage and connect the probe to the front electrode.
2) EQE result (shown in Figure 23) is obtained by irradiating a light with 1-nm step increment from 300 – 1200 nm. The EQE is a proportion of the energy of generated electron to the input irradiated photon energy as shown in equation 10.
3) IQE data are calculated with the inclusion of the reflectance data obtained by UV-Vis spectrophotometers in previous section.

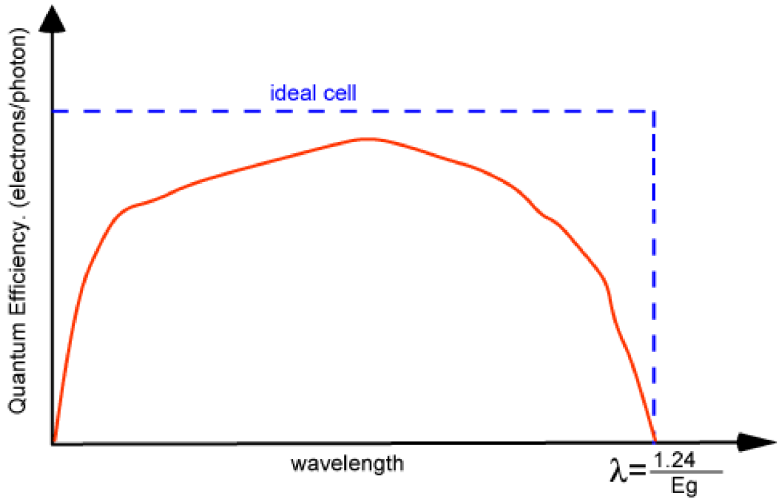


FIGURE 23: EXTERNAL QUANTUM EFFICIENCY (EQE) [60]

$$E.Q.E = \frac{\text{Electron out}}{\text{Photon in}} \qquad \text{……..…….(10)}$$

It should be noted that the J_{SC}, η, EQE and IQE values shown in the next chapter are calculated using the active area of the solar cell surface, which means that the Ag electrode area are excluded. As a reference, the fabrication process of the c-Si solar cell, except the porous silicon formation part, is the same with those for porous silicon solar cells.

3.3 METHODS OF SIMULATION

3.3.1 Overview of the Simulation

Along with the results based on various experiments and characterizations, a computational approach, is also used to investigate the properties of porous silicon model. to confirm changes in the electronic properties induced by porosity, amorphization, and passivation.

In order to be comparable to the experiment, a porous silicon model must be properly selected or generated in a way that represents the actual structure as much as possible; for instance, the porosity, the crystallinity, the element/molecule on the surface of the pore, etc. The porosity of the material is defined as the proportion of the volume of void space in the material to the total volume of the material. As the model will be calculated in a periodic mode, the final geometry of the material and pore must be properly selected so that the thickness of the wall and the pore spacing are similar to the actual sample (in nanometer scale); that is why merely using the smallest model with the target porosity will not be a good representative as the wall and spacing will be too small (in angstrom scale) in periodic mode. With all these facts, a relatively large model of porous silicon in term of number of atoms is required in order to achieve a realistic calculation. In term of the selection of crystallinity of the model, it is well-known that the etching process to fabricate the porous silicon from base crystalline silicon wafers will result in the amorphization of the top layer of the surface [61], while the crystallinity of the inner layer remains unaffected (shown in Figure 24).

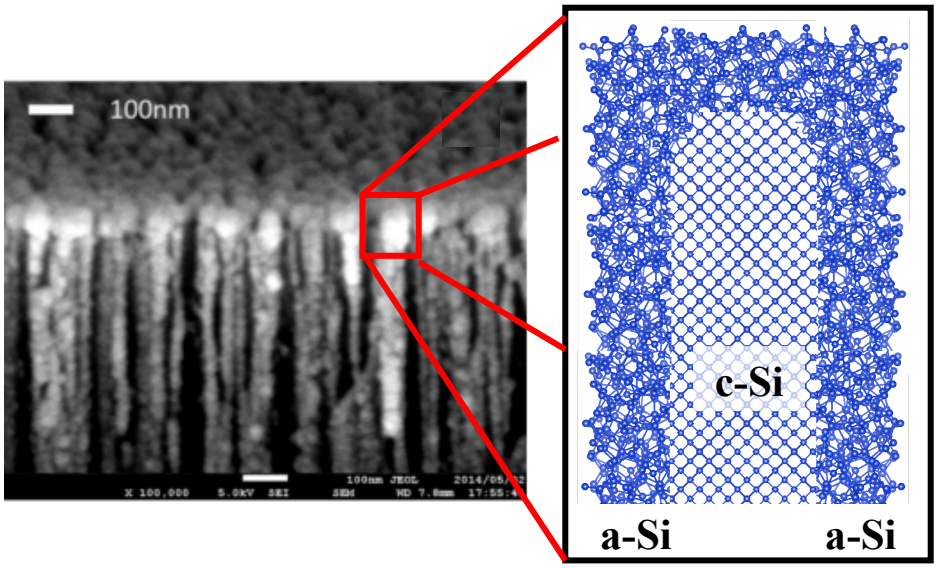


FIGURE 24: CRYSTALLINITY OF THE POROUS SILICON (LEFT) TEM IMAGE OF FABRICATED POROUS SILICON (RIGHT) SIMPLIFIED CROSS-SECTIONAL MODEL OF POROUS SILICON WITH AMORPHOUS SI ON THE SURFACE AND CORE CRYSTALLINE SILICON (NOT TO SCALE)

Together with the result from XRD measurement, the existence of the a-Si on the surface is confirmed. Therefore, in prior to simulate the realistic model which is composed of both c-Si and a-Si, the porous silicon model based only with c-Si will be calculated as a first step. Lastly,

to investigate on the effect of passivation, only the hydrogenation of the surface will be used as a first step. The method to add the hydrogen atoms to the model will be explained later in this section.

Three principles of calculation method are used in this research: Molecular Dynamics (MD), Density Functional Theory (DFT), and Density Functional Tight Binding (DFTB). For MD, the calculation is based on the classical equations of motion in which force fields are used as a method to estimate the potential energy between atoms or molecules. It is relatively fast compared to other two methods, less CPU-intensive, and able to calculate a large model. However, as it is based on the classical physics, MD cannot provide insight into electronic properties. It is also dependent on the accuracy of the force field which may not account for all relevant interactions. For the latter, electronic structure methods are needed such as the density of states (DOS). DFT, is a first principle, or *ab initio*, method which means that all of the physical properties are calculated directly from the basic physical quantities (for instance, mass, charge, coulomb force of electron and atomic nuclei, etc.) based on the quantum mechanics. This method yields a better approximation and provides electronic structure information, yet it is CPU-intensive especially for the large-scale model. For this reason, in this work, we also use DFTB, which is a semiempirical electronic structure method that is parameterized either with DFT calculations or directly to experimental data (e.g., to correctly reproduce the band structure). This allows performing calculations about 3 orders of magnitude faster than DFT while achieving DFT-like accuracy for well-parameterized systems, which is the case for Si [62]. As in solid state DFT calculations, especially in those with relatively large simulation cells (>10 Ang), one typically has to rely on GGA functionals which are known to underestimate the bandgap by about 30%, DFTB, in spite of being a more drastic approximation than DFT, due to its semi-empirical nature allows obtaining a band structure in better agreement with the experiment than GGA DFT [63]. This is true in particular for Si where the DFTB parameterization that we use was shown to correctly reproduce the band structure, which a quantitatively accurate bandgap [64]. With all these advantages and disadvantages of each method, we use all three together to capitalize on the strength and avoid the disadvantages of each method, namely:

- MD is used to pre-optimized the structures
- DFTB is used for final optimization and band gap / DOS calculations
- DFT is used to cross-check DFTB results for selected systems.

As the purposes of this calculation are to investigate the electronic structures of passivated porous silicon models, a proper structure must be obtained in order to have a good estimation. Firstly, the optimization or relaxation process of the initial structure is performed in order to obtain the structure with the lowest energy possible, i.e., the most stable structure. Without this process, the position of some adjacent atoms could be too close to each other's, causing the local potential energy to be higher than it should be, thus compromising the estimation of electronic structure. In certain positions, some could be improperly bonded with its neighboring atoms, resulting in the dangling bonds which create the trapped states in the band structure. In this study, all 3 methods are used for optimization/relaxation process. For the electronic structure calculation, the DFTB method is used as the codes itself come with a suitable parametrization for evaluating the band structure of silicon-based model. In case of DFT method, despite being *ab initio* and having a function to calculate the band structure as well, its inaccuracy in band gap estimation is well-known and the calculated values tend to be underestimated compared to the real experiment. Therefore, for the best estimation of the result, the density of states (DOS) and the band diagram of all structures, regardless of which method was used for relaxation, will be calculated by DFTB. The resulting band structure from each method of relaxation will be compared and discussed in term of its quality and its accuracy to the experiment.

The further detail of each simulation is described in the following sections:

3.3.2 Density Functional Theory (DFT)

Density functional theory (DFT) is a practical method for finding solutions to the Schrödinger equation, which is the fundamental equation that describes the underlying quantum behavior of atoms, molecules, and solids [65]. The key question it tries to answer is what the energy of a given (clamped nuclei) structure is. From there, energy as a function of structure can be computed and therefore optimal structures, transition states, energy differences between different phases, interaction energies, etc., can be found. As the mass of an electron is 1800 times less than that of the nucleus, the calculation can be divided into two distinct parts: first by solving the electron ground states where the nuclei are held fixed, and second by solving the nuclear Schrödinger equation by introducing the concepts of potential energy surfaces, equilibrium geometries, and binding energy. This method is called the Born-Oppenheimer (BO) approximation, which allows us to approximate the change of the energy of the material

when some atoms are moved around. One of the simplest forms of the Schrödinger equation is the time-independent, nonrelativistic Schrödinger equation:

$$\left[-\frac{\hbar^2}{2m}\sum_{i=0}^{N}\nabla_i^2 + \sum_{i=0}^{N}V(r_i) + \sum_{i=0}^{N}\sum_{j<1}U(r_i,r_j)\right]\varphi = E\varphi \qquad \text{.....(11)}$$

Where φ is the electron wavefunction where $\varphi = \varphi(r_1,r_2,\ldots,r_N)$, E is ground state energy of electron, m is mass of electron, and $\hbar$ is a Planck's constant, and r are coordinates of all atoms. The terms in the bracket are divided into three parts, which defines the kinetic energy, the interaction of electron-nuclei, and the interaction between electrons, in that order. These are all simple coulombic interactions.

For the electron wavefunction $\varphi = \varphi(r_1,r_2,\ldots,r_N)$, which is a function of the coordinates of all N electrons, it is more convenient to approximate this term as it will be very difficult to solve the Schrödinger equation as the number of electrons in molecule increases. This can be approximated by combining the wavefunctions of electrons as a Hatree product:

$$\varphi = \varphi_1(r)\varphi_2(r)\ldots\varphi_N(r) \qquad \text{.....(12)}$$

For electron-electron interaction part in Hamiltonian, φ(r) cannot be solved without simultaneously considering the other electron wavefunctions. Instead, the probability of finding electron in particular position in space, n(r), the electron density, is used:

$$n(r) = \varphi^*(r)\varphi(r) \qquad \text{..... (13)}$$

Where $\varphi_i(r)$ are 1-electron wavefunctions called orbitals. Hohenberg and Kohn found that the ground-state electron density uniquely determines all properties of the ground state, including its energy and wavefunction [66]. This is important because it significantly reduces the number of calculations from potentially thousands of dimensions to only 3 dimensions. The functional of 1 electron wavefunctions involved described by Hohenberg and Kohn can be written as:

$$E[\{\varphi_i\}] = E_{known}[\{\varphi_i\}] + E_{XC}[\{\varphi_i\}] \qquad \text{.....(14)}$$

Where the functional is divided into two terms: what is known so far is included in E_{known}, and everything else, E_{XC}, which includes all quantum effects not included in the known term.

$$E_{known}[\{\varphi_i\}] = \frac{-\hbar^2}{m}\sum_i \int \varphi_i^* \nabla^2 \varphi_i \, d^3r + \int V(r)n(r)\, d^3r + \frac{e^2}{2}\iint \frac{n(r)n(r')}{|r-r'|} d^3r d^3r' + E_{ion} \quad ..(15)$$

The definition of each term is similar to in Equation 11, except that there is an extra term at the end describing coulomb interaction between pair of nuclei, E_{ion}. With this theorem, they also define another property of the functional stating that: *the electron density that minimizes the energy of the overall functional is the true electron density corresponding to the full solution of the Schrödinger equation*. Later on, Kohn and Sham proved this theorem and showed a practical way to compute the orbitals. This equation is called "Kohn-Sham equation"[67]:

$$\left[-\frac{\hbar^2}{m}\nabla^2 + V(r) + V_H(r) + V_{XC}(r)\right] \varphi_i(r) = \varepsilon_i \varphi_i(r) \qquad \text{.....(16)}$$

Where the $V_H(r)$ is Hatree potential and $V_{XC}(r)$ is an exchange-correlation energy. This is with a type of Schrödinger equation for only a single electron, and the wavefunction of this electron (called orbital) depends only on three spatial variables, $\varphi_i(r)$. By using the iterative approach to Kohn-Sham equation, the ground state electron density can be solved. The iterative approach must be used as a way to break the calculation loop in solving the Kohn-Sham equation. This is originated from the dependence of the effective potential $v_{eff}(r) = V(r) + V_H(r) + V_{XC}(r)$ on the electron density as well as the dependence of the electron density on the single-electron wavefunction, which must be solved by Kohn-Sham equation.

The exchange-correlation functional, E_{XC}, is very difficult to define. Many functionals have been developed to best represent it for particular types of materials and applications. One of the most basic forms is the local electron density approximation (LDA). Combining LDA with the local gradient in electron density, the generalized gradient approximation (GGA) is obtained.

The following table lists the DFT software/code, and the related pseudopotential file used in this simulation. The pseudopotential file is an approximated and simplified description of the complex system like in the atomic all-electron potential, which allows a calculation with a significantly smaller number of nodes.

TABLE 1: SOFTWARE AND PARAMETERS USED IN DENSITY FUNCTIONAL THEORY (DFT) CALCULATION

Software/Code	Version	Application	Pseudopotential File
QuantumEspresso [68], [69]	6.3	Structure Optimization	Si.pbe-n-rrkjus_psl.1.0.0.

3.3.3 Density Functional Tight Binding (DFTB)

The derivation of the Density Functional Tight Binding (DFTB) model is performed based on a Taylor series expansion of the Kohn-Sham DFT energy equation (Equation 16) around an appropriately selected reference electron density ρ(*r*) [70]. Instead of calculating for the density ρ(*r*) that minimizes the total energy (ground-state) like in DFT approach, a reference density ρ_0 is assigned which is perturbed by some electron density fluctuation, $\rho(r) = \rho_0(r) + \delta\rho(r)$. Furthermore, the exchange–correlation energy functional (E^{XC}) is then undergone a Taylor series expansion up to the 3rd order and the total energy equation can be written as:

$$E^{DFTB\,3}[\rho_0 + \delta\rho] = E^0[\rho_0] + E^1[\rho_0 + \delta\rho] + E^2[\rho_0 + (\delta\rho)^2] + E^3[\rho_0 + (\delta\rho)^3] \quad \ldots\ldots(17)$$

Where each component of the expansion is defined as:

$$E^0[\rho_0] = \frac{1}{2}\sum_{AB}\frac{Z_A Z_B}{R_{AB}} - \frac{1}{2}\iint\frac{\rho_0(r)\rho_0(r')}{|r-r'|}drdr' - \int V^{XC}[\rho_0]\rho_0(r)dr + E^{XC}[\rho_0] \quad \ldots\ldots..(18)$$

$$E^1[\rho_0 + \delta\rho] = \sum_i n_i \langle\varphi_i|\widehat{H}[\rho_0]|\varphi_i\rangle \quad \ldots\ldots..(19)$$

$$E^2[\rho_0 + (\delta\rho)^2] = \frac{1}{2}\iint\left(\frac{1}{|r-r'|} + \frac{\delta^2 E^{XC}[\rho]}{\delta\rho(r)\delta\rho(r')}\Big|_{\rho_0}\right)\delta\rho(r)\delta\rho(r')drdr' \quad \ldots..\ldots(20)$$

$$E^3[\rho_0 + (\delta\rho)^3] = \frac{1}{6}\iiint\frac{\delta^3 E^{XC}[\rho]}{\delta\rho(r)\delta\rho(r')\delta\rho(r'\prime)}\Big|_{\rho_0}\delta\rho(r)\delta\rho(r')\delta\rho(r'')drdr'dr'' \quad \ldots\ldots.(21)$$

There are three generations of the DFTB models that have been developed over the years, where one was built successively on top of each previous model and includes more terms of the expansion. The first version is the 1st order non-self-consistent DFTB1 [71], [72] (originally DFTB or non-SCC DFTB), following with the 2nd order DFTB2 [73] (originally SCC-DFTB), and finally the most recent version of 3rd order, DFTB3 [74]–[76].

The DFTB1 model makes use of three major approximations: (1) it includes only the $E^0[\rho_0]$ and the $E^1[\rho_0+\delta\rho]$ terms from Equation 17, (2) it is based on the linear combination of atomic orbital (LCAO) ansatz of the Kohn-Sham orbitals, and (3) the two-center approximation of the $\hat{H}[\rho_0]$ is applied. Basically, this DFTB1 approximates the DFT by using a minimal basis set of nearest neighboring atoms and the Slater-Koster tables, which contain pre-calculated matrix elements. Also, as the $E^0[\rho_0]$ depends solely on the reference electron density, the

DFTB1 model further approximates the $E^0[\rho_0]$ term as a sum of the pairwise repulsive potential called a repulsive energy term (E_{rep}):

$$E^0[\rho_0] \approx E_{rep} = \frac{1}{2}\sum_{AB} V_{AB}^{rep} \quad \text{.....(22)}$$

The DFTB2 model includes the E^2 $[\rho_0+(\delta\rho)^2]$ in equation 17 on top of DFTB1. The additional features are the use of a self-consistent charge step (SCC), and the optimization of the Mulliken charges. Lastly, the DFTB3 model includes the E^3 $[\rho_0+(\delta\rho)^3]$ terms in equation 17 further, which includes the additional polarization term.

The following table lists the detail and the related Slater-Koster files used in this DFTB calculation.

TABLE 2: SOFTWARE AND PARAMETERS USED IN THE DENSITY FUNCTIONAL TIGHT BINDING (DFTB) CALCULATION

Software	Version	Application	Slater-Koster File	Ref
DFTB+ [70]	22.1	Structure relaxation	pbc	[77], [78]
		Band structure calculation	siband	[64], [79]

The pbc is used for structural relaxation as it is good and well-parametrized for the silicon clusters. The siband is preferred over pbc for the band structure calculation because it is a Slater-Koster files made specifically for accurately calculate the electronic structure of DFTB for Si, O, and H containing materials. Both of these parametrization files are based on DFTB2.

Also, for the comparison of the resulting band edge values between the different model, the DFTB built-in function to calculate the electrostatic potential is used to compared the electrostatic potential of the vacuum level and uses this reference value for offsetting all of the DOS result.

3.3.4 Molecular Dynamics (MD)

The core of the Molecular Dynamics (MD) method is based on the determination of the trajectories of the atoms or molecules by numerically solving the Newton's equation of motion. This can be done by analyzing the internal energy (U) of the system. In principle, computing the internal energy of a solid involves a many-body problem. This is highly expensive to calculate at any level of theory in the present time, which is why the approximations must be

made for the simplification of the problem. The first assumption is that the energy can be divided into an expansion in terms of interactions between different atoms in the total number of atom (N):

$$U = \sum_{i=1}^{N} U_i + \frac{1}{2}\sum_{i=1}^{N}\sum_{j=1}^{N} U_{ij} + \frac{1}{6}\sum_{i=1}^{N}\sum_{j=1}^{N}\sum_{k=1}^{N} U_{ijk} + \cdots \qquad \text{……..(23)}$$

Where the first term defines the internal energy of the atom itself (irrelevant for dynamics or for interaction energies), the second term is the interaction between the pair atoms, triples (3-body) and so on. This approximation can result in a high accuracy if the expansion order is high enough. However, it is known that the as the order of the terms becomes higher, the contribution will become progressively smaller for most of the systems. This is why the higher order terms, up to a certain point, is neglectable and will be compensated by a parametrization instead. In general, up to four-body terms is considered a reasonable approach for most systems [80], [81]. Moreover, it is intuitively evident that the greater the distance between two atoms, the weaker their interaction. As a result, the distance cut-offs can be introduced to simplify the computational task.

In the MD simulation, the forces are calculated using the Force Field (FF) model, which must be selected properly to the interested system as the nature of the forces between particles in each system (organic/inorganic/metal/etc.) are different. A typical force field includes terms that defines an electrostatic (Coulombic) interaction between atoms, spring-like terms that mimic the length of each covalent bond, and other terms expressing several types of interatomic interactions. The following section lists some of the widely used interatomic potential models:

Coulomb Interaction

$$U_{ij}^{Coulomb} = \frac{q_i q_j}{4\pi\varepsilon_0 r_{ij}} \qquad \text{……..(24)}$$

Where q is the charge on one body, r is the distance between two bodies, and ε_0 is the permittivity of free space.

Two-body Short range Interactions:

$$U_{ij}^{Buckingham} = Aexp\left(-\frac{r_{ij}}{\rho}\right) - \frac{C_6}{r_{ij}^6} \qquad \text{……(25)}$$

$$U_{ij}^{Lennard-Jones} = \frac{C_m}{r_{ij}^m} - \frac{C_6}{r_{ij}^6} \quad \text{.....(26)}$$

Where A and C are the constants.

The following table lists the software/code and the related force fields used in this simulation

TABLE 3: SOFTWARE AND PARAMETERS USED IN MOLECULAR DYNAMICS (MD) CALCULATION

Software	Version	Application	Force Field	Ref
GULP [80]	6.0	Structure Optimization	Tersoff	[82]–[84]

3.3.5 Generation of the Hydrogenated Porous Silicon Model

- Model:

The model used in this simulation is based on the crystalline silicon model. The unit cell of cubic c-Si is obtained from the database [85]. Then it is transformed in VESTA software to achieve a desired size as a base cell ready for introducing a pore.

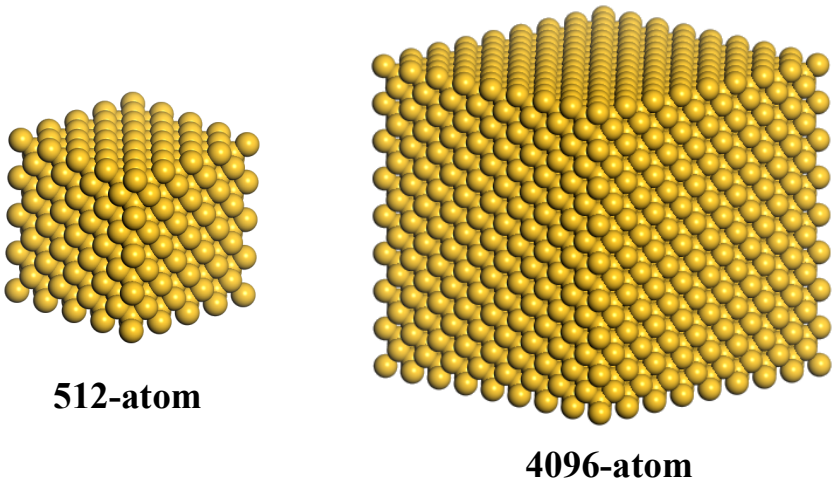


FIGURE 25: MODEL OF CRYSTALLINE SILICON (C-SI). THE UNIT CELL CAN BE TRANSFORMED INTO THE DESIRED BOX SIZES IN XYZ DIRECTION. IN THIS FIGURE, THE EXAMPLE OF 512-ATOM AND 4096-ATOM MODEL ARE PRESENTED.

- Pore Generation:

Pore is introduced to c-Si based cell manually by geometrically removing the atoms in the CIF file using python codes to generate porous silicon model with the corresponding porosity as well as the other pore dimension, such as the wall thickness and the pore spacing. 4 types of models are formulated as a representative of PSi/c-Si model in this thesis. These models are internal sphere, internal cube, pillar, and crater models. The spherical and cubic pore is carved

at the center of the cubic box base cell to generate the internal sphere and internal cube models. The surrounding atoms are removed in the cuboid base cell to some height to generate the pillar model with desired pillar diameter, height, inter-pillar spacing and base layer thickness. Finally, the hemisphere-tipped cylinder is carved out of the cuboid base cell to the desired depth and diameter in order to generate the crater model.

- Passivation

The passivation process is conducted by the hydrogenation of the surface. The hydrogenation process is done using the built-in function of Materials Studio software: Update Hydrogen. This function adds hydrogen to the atoms that are not completely bonded, i.e., possessing dangling bonds, one hydrogen per one dangling bond, thus saturating the surface.

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1 POROUS SILICON

4.1.1 Determination of PN-junction

Electrochemical Capacitance-Voltage (ECV) and Transmission Electron Microscope (TEM) images

The ECV profiling is conducted on phosphorus (P) doped bulk p-Si wafers, after removing the thermal oxide from the wafer surface by mildly etching, to obtain the activated P concentration profiles at annealing temperature of 900 °C for 17 minutes to investigate the location of the p-n junction interface. Three samples of phosphorus-doped silicon wafers (Sample 1 and 2) are measured with ECV and compared with data made from our previous researcher (Sample 3). The P-type (boron) based silicon wafer has a resistivity of 1-2 Ω.cm, which is equivalent to the doping level of 7.17×10^{15} - 1.512×10^{16} cm^{-3} [86]. The data is shown below in Figure 26.

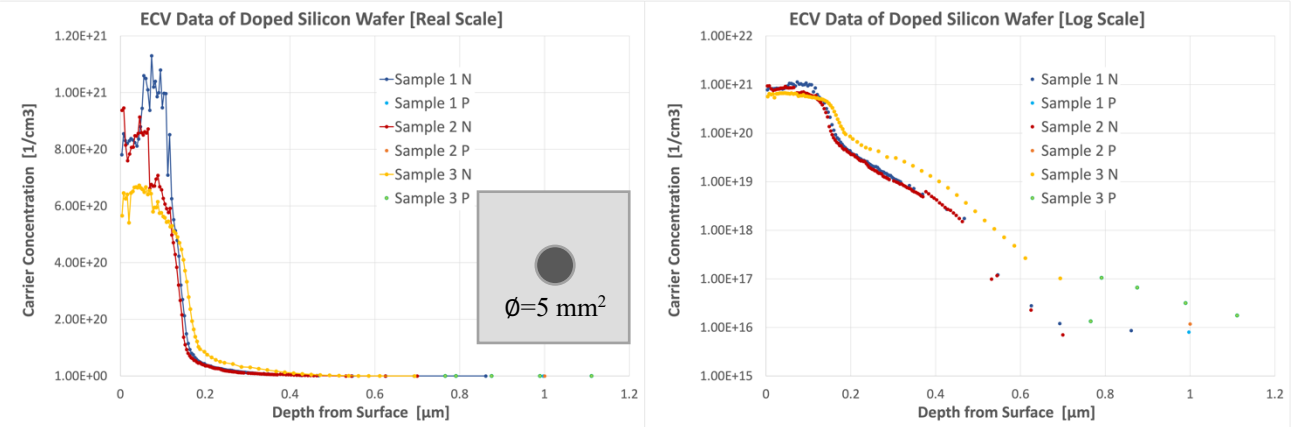


FIGURE 26: ELECTROCHEMICAL-CV DATA OF THREE DOPED SILICON WAFERS WITH ARITHMETIC SCALE (LEFT) AND LOGARITHMIC SCALE (RIGHT) AND DIAGRAM OF THE ETCHING AREA OF 5 MM^2 AT THE CENTER OF THE DOPED WAFER SAMPLES (INSET).

The carrier concentration in the n-type layer is as high as 9.46×10^{20} for Sample 1, 1.1×10^{21} cm^{-3} for Sample 2, and 6.6×10^{20} cm^{-3} for Sample 3. In Figure 26, the log scale graph on the right shows two characteristic regions. The first is the region from the surface down to 100 nm depth, where the carrier concentration is high and stable. This region is caused by slow substitutional diffusion, where the phosphorus atom replaces the silicon atoms in the crystalline

structure. The second region is the region from 100-200 nm depth, where the carrier concentration drops down to a lower concentration of 10^{15} cm^{-3}. This is caused by the fast interstitial diffusion, where the phosphorus atom diffuses in the interstices.

In order to determine the position of the p-n junction, in both the arithmetic and logarithmic scales, a sharp decline in the carrier concentration is observed to be around the wafer depth of 200 nm, indicating a high P-doping concentration of the n-layer on the top of the p-Si base wafer; this suggests that the p-n junction is located approximately around this 200 nm depth. Even though there are some differences in the carrier concentration between samples in the highly doped area from the top surface to around 150 nm depth (Figure 26 left), there is no discernible impact on the underlying location of the p-n junction. When considered in the logarithmic scale, the drop of the carrier concentration has a similar curve in every sample, as can be seen in Figure 26 (right).

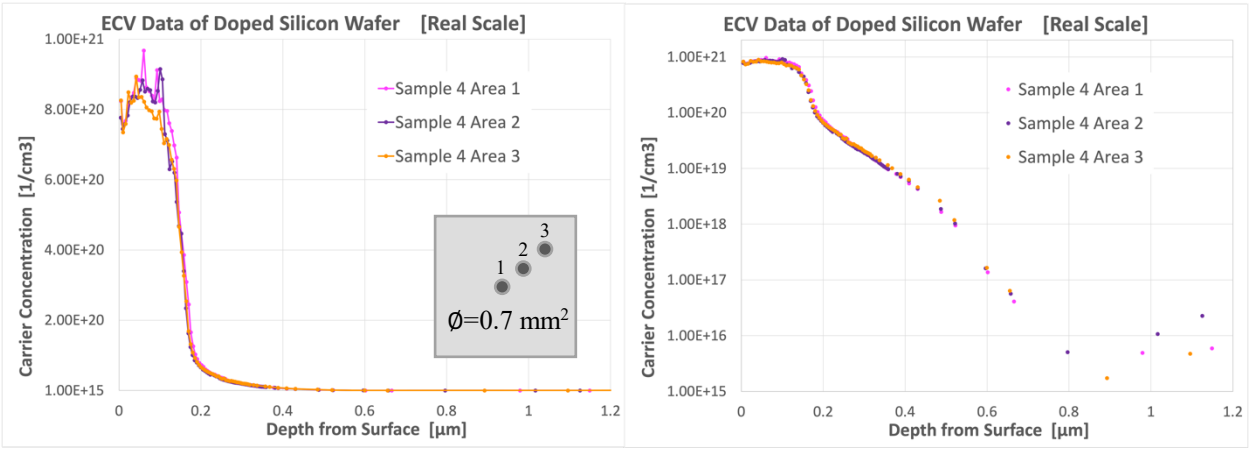


FIGURE 27: ECV DATA WITHIN SAME SAMPLE WITH ARITHMETIC SCALE (LEFT) AND LOGARITHMIC SCALE (RIGHT) AND DIAGRAM OF THE ETCHING AREA OF 0.7 MM² IN DIFFERENT AREA (1,2,3) ON DOPED WAFER SAMPLE (INSET).

To further investigate the homogeneity of the doping profile, the ECV profiling was also measured on Sample 4 in three different areas (1,2,3). The result shown in Figure 27 confirms that a uniform n-layer is formed on the top of p-Si wafer by thermal diffusion of the P-dopant as the steep drop-off is also located around 200 nm similar to Figure 26.

Moreover, the doped porous silicon is also observed visually by using TEM image to compare the result with ECV.

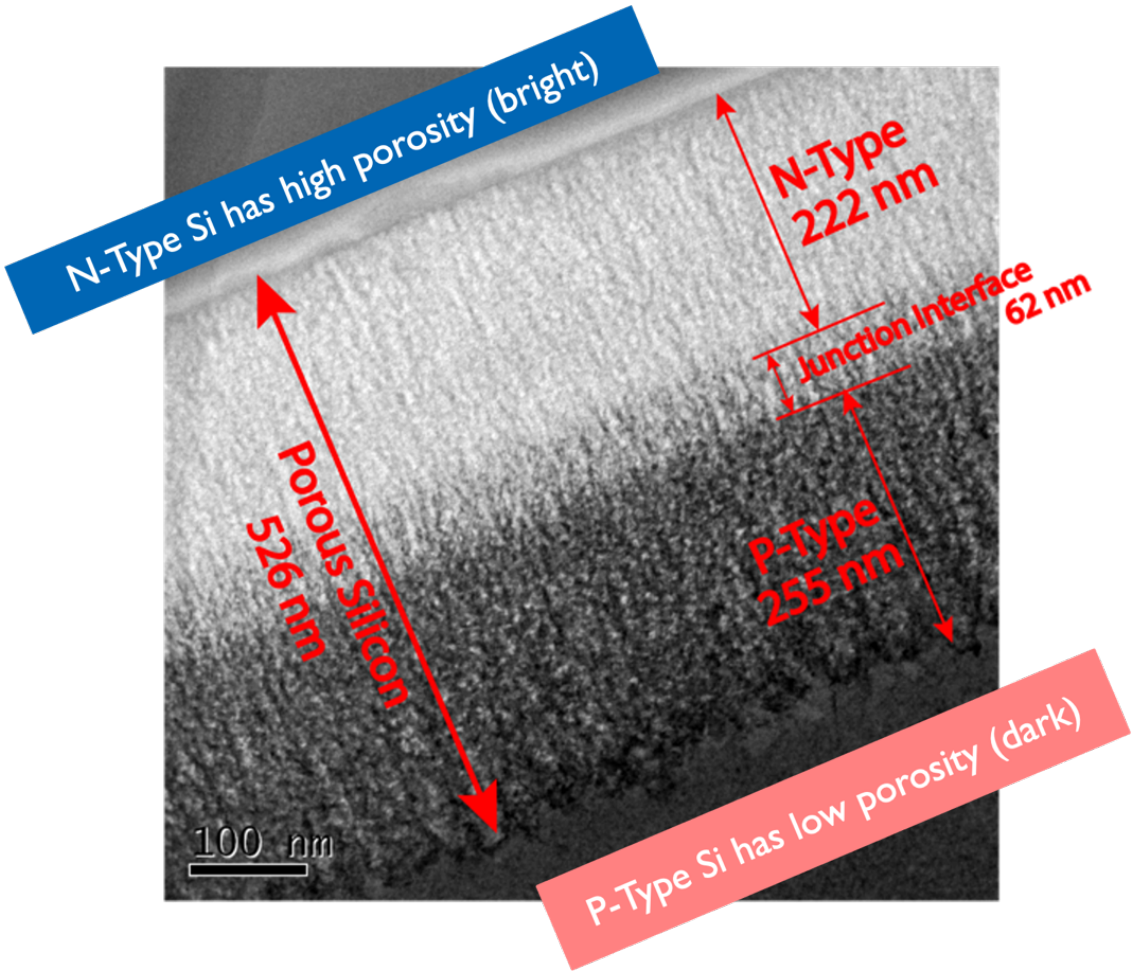


FIGURE 28: CROSS-SECTIONAL TEM IMAGE OF DOPED POROUS SILICON LAYER (526 NM) FOR OBSERVATION OF THE P-N JUNCTION BY DIFFERENCE OF POROSITY AND CONTRAST

A cross-sectional TEM image of the 526 nm thick porous silicon layer on a c-Si substrate is shown in Figure 28, displaying bright and dark contrast layers as a result of the different porosity between them. The porosity of the porous silicon layer formed on the top bright contrast layer (222-nm-thick) is different from that of the porous silicon layer on the bottom contrast dark layer (255-nm-thick), which indicates a different P-doping density of the n-type silicon region. As a result, the porosity of porous silicon could be controlled by varying the of P-doping level [87]. It is worth noting that the depth of the top bright contrast layer corresponds to the high P-doping concentration of the n-layer as shown in the ECV profile, which confirms that the p-n junction is located below 200 nm from the surface.

Discussion on the Selection of P-N Junction Depth and Porous Layer Thickness

To determine the P-N junction depth, the real scale graph is used. The tangent line drawn from the second region (the drastic drop) to intersect with the horizontal axis is an

estimated depth of P-N junction, which is located at 160 - 200 nm. These data are used to determine the condition of fabrication of the porous silicon. The Figure 29 shows the relationship between P-N junction vs porous silicon layer thickness.

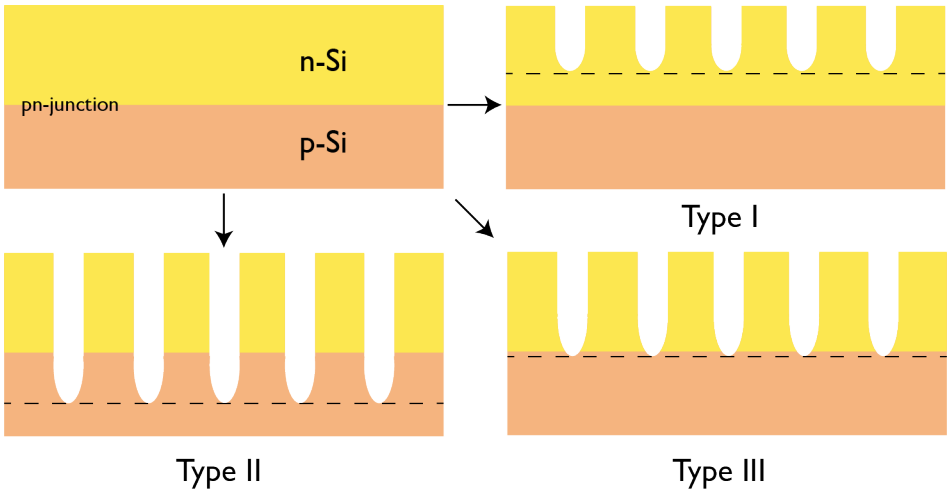


FIGURE 29: TYPES OF STRUCTURE BETWEEN POROUS LAYER AND P-N JUNCTION

There are 3 types of structure to be discussed: Type I, II, and III. Type I is where the porous silicon lies within the N-type silicon and does not reach P-N junction. In this structure, the porous silicon acts only as an anti-reflective surface. Type II structure is where the porous silicon exceeds the P-N junction depth and lies deep within the P-type silicon. In this case, the porous silicon reaches the P-N junction, which allow more probability that the higher energy photoelectrons generated by the quantum size effect reach the P-N junction, while still acting as an anti-reflective film. However, the deeper porous layer drastically increases the surface area, which means the recombination rate also likely drastically increases. Therefore, it is necessary to control the depth of porous silicon to just reach the P-N junction only, not any deeper than that. Type III is a structure type where the porous silicon reaches the P-N junction and slightly lies within P-type silicon. This is expected to be the best structure due to the least recombination, the higher collection probability of the photoelectron generated by quantum size effect to, and anti-reflective film.

Therefore, the condition to etch the porous silicon is selected by these relationships, which means we should fabricate the porous layer to be deeper than 200 nm because the P-N junction depth is at 200-250 nm.

4.1.2 Structure of Porous Silicon

Scanning Electron Microscope (SEM) images

In this experiment, the porous silicon is fabricated with the condition of 75 mA/cm^2 for 6 seconds to obtain over 200 nm thickness and exceeds the P-N junction depth. The condition was calculated by previous studies and is used in this experiment for the continuity of the study. Two SEM images are selected to show both the thickness and part of the surface.

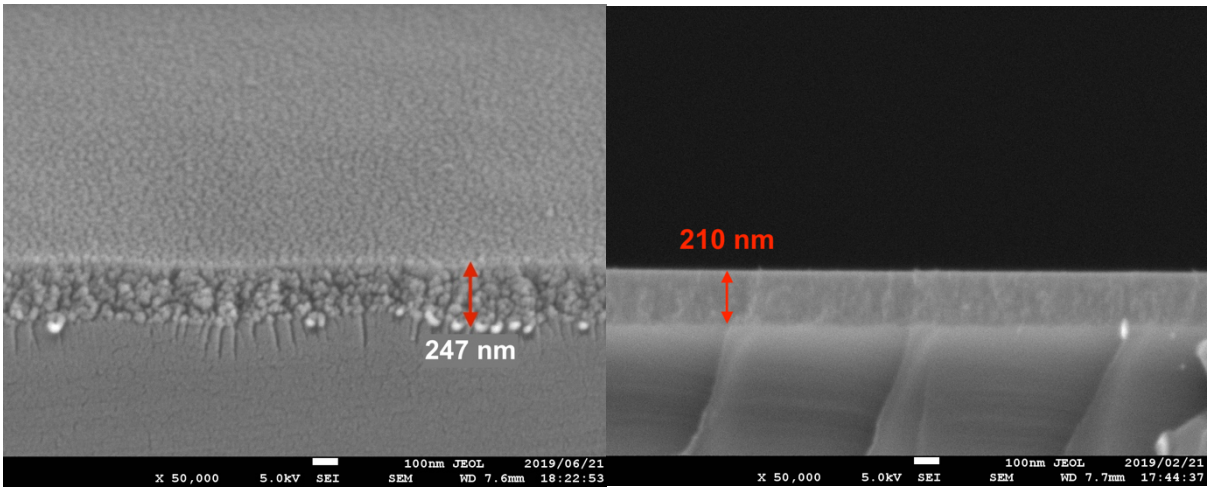


FIGURE 30: SEM IMAGES OF POROUS SILICON 40° TILTED (LEFT) AND 0° (RIGHT)

In Figure 30, it is confirmed that the porous layer thickness fabricated with this electrochemical etching condition is in the range of 200 – 250 nm. The thickness profile is found to be inhomogeneous, where the center is the thinnest (~200 nm) and becoming thicker along the radial direction (up to 250 nm), which still keeps the P-N junction inside the porous layer. The surface from the 40° tilted image shows a clear porous structure seen from the top view. However, the pore is not as well-structured as expected, it is more like an amorphous structure, of which the effects need to be clarified.

With this fabrication condition, porous silicon layers with the average porosity of 25% and thickness varied to some degrees (200-250 nm) are prepared on c-Si substrates. A porosity of 25% is calculated based on the effective medium approximation (EMA) with Bruggeman's Model [88] and is optimal to achieve a low lattice-mismatch between the porous silicon layer and c-Si substrate.

Transmission Electron Microscope (TEM) images

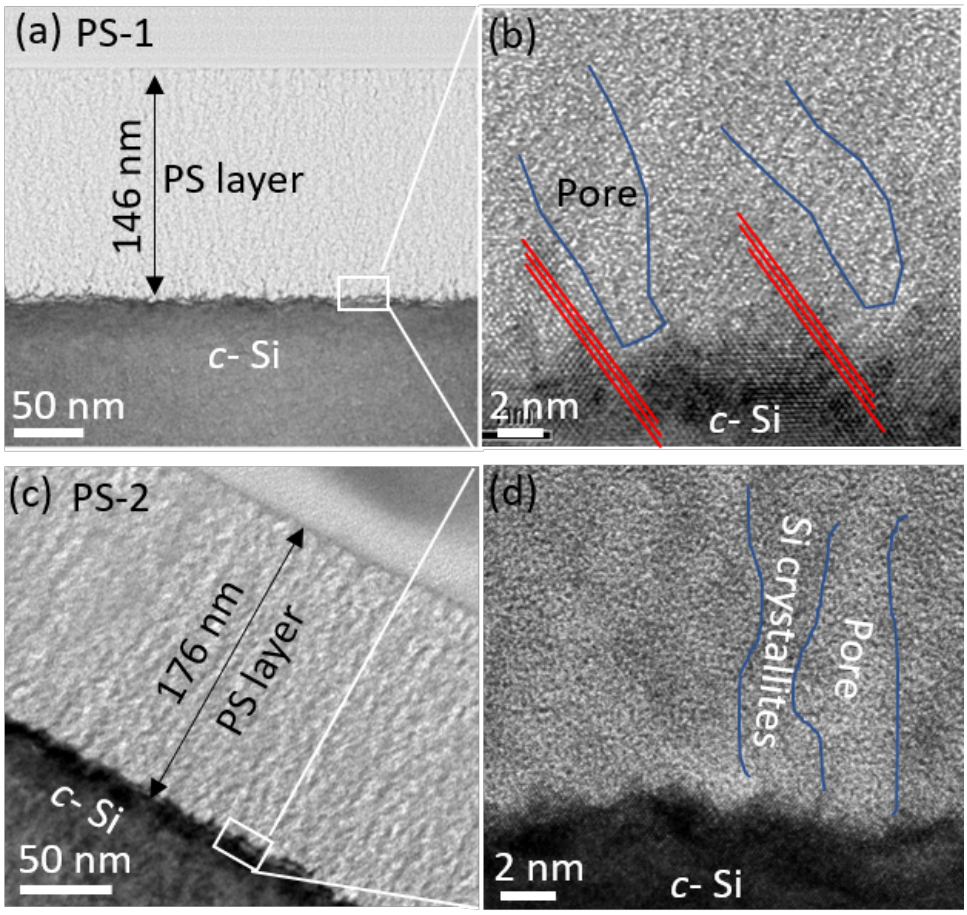


FIGURE 31: (A) TEM IMAGE OF POROUS SILICON LAYER WITH 146 NM THICKNESS (PS-1); (B) HIGH RESOLUTION TEM OF PSI/C-SI INTERFACE AT THE BOTTOM OF PS-1 LAYER; (C) TEM IMAGE OF POROUS SILICON LAYER WITH 176 NM THICKNESS (PS-2); (D) HIGH RESOLUTION TEM OF PSI/C-SI INTERFACE AT THE BOTTOM OF PS-2 LAYER

An overview of the PS-1 layer, which has a uniform thickness of 146 nm on a c-Si substrate, is shown in Figure 31a. The pore appears to be made of an amorphous substance as a result of the amorphization of the thin Si walls on the surface of pores, which is possibly caused by the FIB milling process in the TEM sample preparation. The Si skeleton's projection resembles a crystalline substance in appearance. Straight pores that have formed perpendicular to the surface are seen in the PS-1 layer. Uniform porosity, which in reflecting the uniform doping concentration of the n-layer, is shown by consistent contrast in the PS-1 layer. Figure 31b shows a high-resolution TEM (HRTEM) image of the PS-1/c-Si interface. Moreover, the n-PS-1 layer's crystalline skeleton is oriented in the same direction as the c-Si substrate, suggesting an atomic lattice matching (shown by red dotted lines in Figure 31b) at the PS-1/Si interface. The 176-nm thick PS-2 layer is shown in Figure 31c. Due to a minor top-surface

etching effects from the FIB milling pretreatment procedure for TEM imaging, the measured layer thickness (176 nm) is less than the 200 nm-thick PS-2 layer as-fabricated. A continuous PS-2/c-Si interface can be seen in the corresponding HRTEM image (Figure 31d). Si crystallites and pores are identified by the speckled contrast of dark and bright areas, respectively. Lastly, the bottom PS-2 layer has a lower hole size of 3 nm with a neighboring distance of 3.5 nm, while the top PS-2 layer exhibits a pore size of around 10 nm with a mean distance between neighboring pores of about 15 nm.

With this detailed information from TEM image, the pore size, porosity, pore spacing, wall thickness, as well as the porosity data will be used to generate the simple porous silicon model that is both suitable for the calculation capacity and representative to the actual structure.

4.1.3 Evaluation of optical band gap of porous silicon

Photoluminescence (PL) spectra

The PL spectrum is measured to investigate the luminescence of the porous silicon as it might suggest the band gap expansion. The band gap energy of crystalline silicon has a value of 1.12 eV [89] and is indirect, while the band gap of porous silicon is direct and can be ranged, according to previous reports, from 1.4 eV to 2.2 eV [90] depending on the structure. The measurement is made from 80K up to room temperature with an increment of 50K to confirm the direct transition of the porous silicon. The measured data are shown in Figure 32 below.

The result from Figure 32 shows that the PL peak of porous silicon is located around 645 nm for every temperature, which is equivalent to the energy of 1.92 eV. The fact that this peak is observed even at room temperature indicates that this is caused by the radiative relaxation of the direct band gap material, which then confirms the direct transition of the porous silicon from the indirect band gap of the c-Si base wafer. This efficient visible light emission is a well-known property of porous silicon, which attracted its attention on the research at the first place. Therefore, at first glance, we might expect that this could be a proof of the band gap expansion of the porous silicon and could possibly result in the improvement of V_{OC} when this porous silicon wafer is finally fabricated into the solar cell.

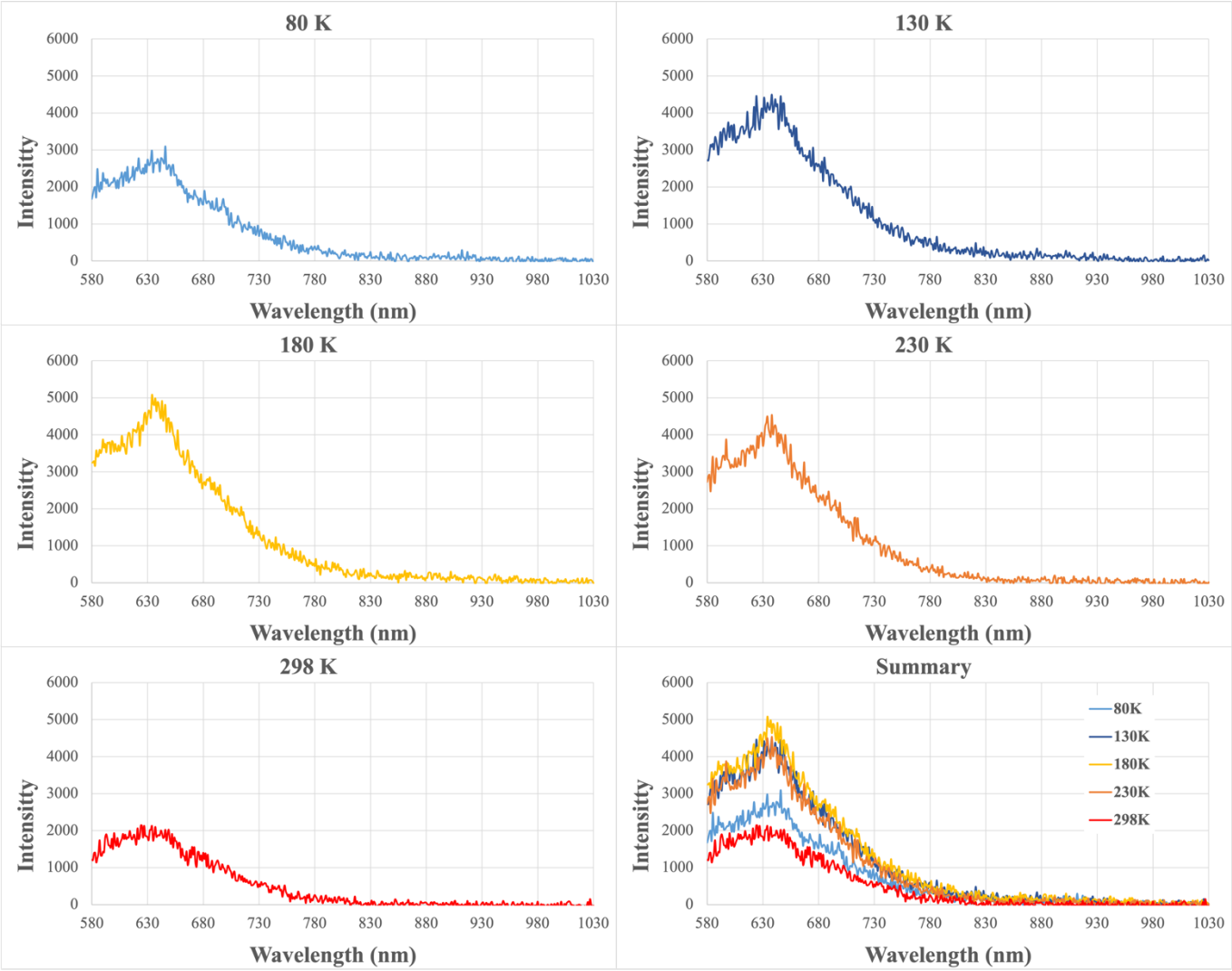


FIGURE 32: PHOTOLUMINESCENCE (PL) SPECTRA OF 200-NM-THICK POROUS SILICON WITHOUT P-N JUNCTION IN VARIOUS TEMPERATURES: 80, 130, 180, 230, 298K

However, the band gap energy calculation from PL data is subject to many limitations. For instance, PL emissions do not provide an exact band gap energy like UV-Vis absorbance (in next section). Also, the origin of the photoluminescence in visible range in porous silicon is still unclear and is subject to many debates even in the present time. Emission from defect / impurity states rather than from the band age is a possibility, The Table 4 below lists the reported photoluminescence band.

TABLE 4: POROUS SILICON LUMINESCENCE BAND [26]

Label	Spectral Range	Typical lifetime at RT	Generally Proposed Origin
IR Band	Near IR 1100 - 1500	10 ns to 10 µs	States at the silicon surface
S-Band (Oxygen-terminated)	Near IR to yellow 590 - 1300	A few ns to ~150 µs	Fast relaxation of excitation to surface states related to Si=O
S-Band (Hydrogen-terminated)	Near IR to blue 400 - 1300	µs range	Quantum confinement in Si nanocrystals; indirect band gap transitions
Hot PL Band	Yellow to blue 425 - 630	ps range	Observed only under high excitation
F-Band	Blue-green 420 - 470	~10 ns	Oxide-related defects/ Organic contamination/ Direct bandgap core luminescence
UV Band	UV 270 - 350	Ps-ns	Oxide-related defects
Long-lived Band	Blue-green 450 - 540	1-8 s	Oxide-related species

As can be seen from the PL result in Figure 32, the most possible origin of PL in the fabricated porous silicon in this thesis is in the range of the S-band. There are many possible origins of this S-band PL, which can be classified according to its proposed models: those based on quantum confinement alone [23], [91]; nanocrystal surface states [92]–[94]; specific defects or molecules [95]–[97]; and structurally disordered phases [98]. From all the proposed origins, it seems that the weight of evidence now tends toward the quantum confinement-based model, which are consistent with the experimental data as a whole [99]. In the case of the porous silicon sample in this experiment, it is possible that the obtained PL is originated by the large amount of oxygen-terminated and hydrogen-terminated surface states caused by the anodization process rather than the quantum confinement effect alone. The effect of this nano-sizing to the band structure needs a further investigation, which will be discussed in the simulation part later on.

UV-Vis spectra

UV-Vis spectra are measured to evaluate the reflectance, transmittance, and absorbance of the porous silicon which can be used to determine its optical band edges. The as-fabricated porous silicon with the same anodization condition without any passivation is used in comparison to the c-Si base wafer. The result of the measurement is shown in Figure 33.

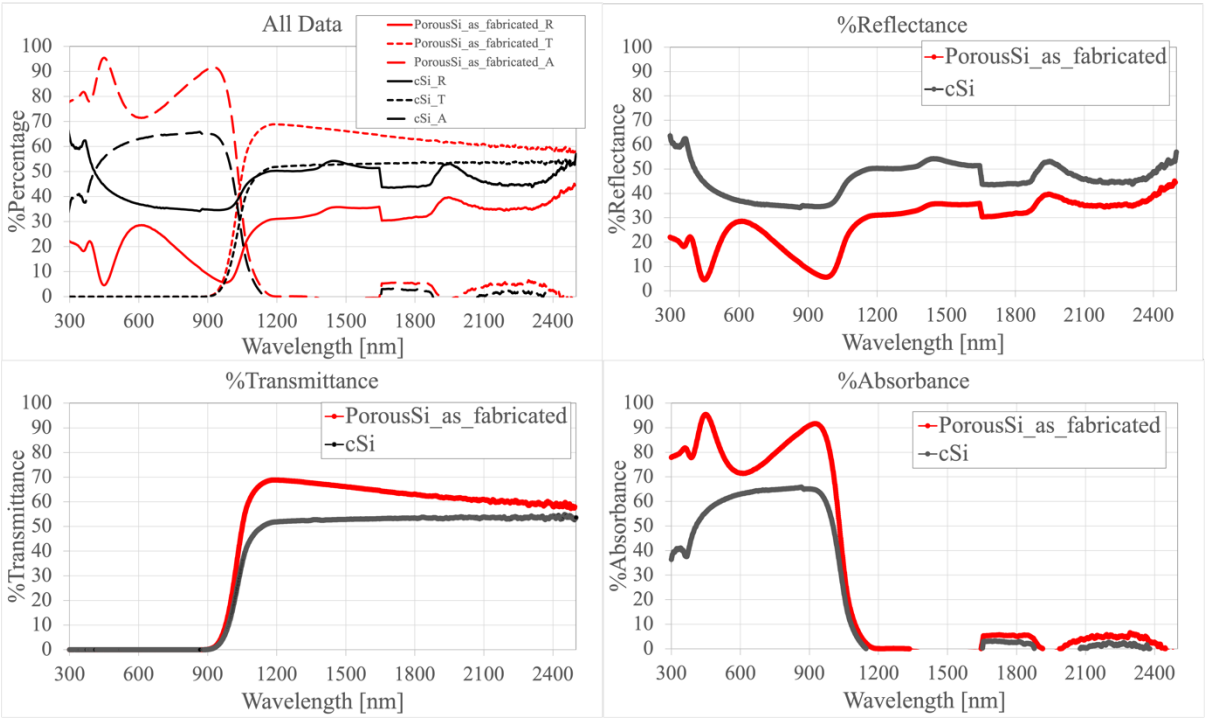


FIGURE 33: UV-VIS SPECTRUM OF AS-FABRICATED POROUS SILICON AND CRYSTALLINE SILICON (C-SI) BASE WAFER.

As can be seen from the top right figure, the porous silicon of 200 nm thickness is shown to be effective in reducing the reflectance compared to that of the bulk c-Si sample throughout the entire UV-Vis spectrum. The amount of reduction is observed to be about 40% in the UV range of 300-400 nm and 20% in the IR range of 1100-2500 nm on average. In the visible region to near IR (400-1100 nm), the reflectance sharply drops from over 20% to its at lowest of 5% at 450 nm, then increases and has a broad peak of 30% centered at 600 nm, and finally drops again to 7% at 1000 nm. This low reflectance demonstrates the potential anti-reflection property of the porous layer caused by the texturization of the surface [100]–[102].

In the bottom left graphs in Figure 33, the transmittance is shown. It is clearly seen from that the transmittances of both porous silicon and c-Si samples start to decrease at 1150 nm and sharply drop to zero around 900 nm. The absorbance is then calculated correspondingly using both reflectance and transmittance data. From the absorbance result in the bottom right graph, it suggests that the optical band edges of both porous silicon and c-Si samples are located around 1100 nm wavelength; this corresponds to the energy of 1.12 eV, which is clearly the band gap energy of c-Si. Apart from the reflectance reduction of porous silicon, the effect of the direct transition of the band gap from indirect of c-Si to direct band gap of porous silicon

is also observed as the absorbance is higher in the region above 900 nm. Also, the gap states are also found in the region of 1700-2400 nm.

As both results are similar except in the 300-1100 nm region, this suggests that the fabricated porous silicon either has the same optical band gap energy as of the c-Si base wafer or is largely influenced by the band gap of the c-Si base layer. This is because the porous silicon is fabricated on top of the c-Si, making it a heterojunction structure. This effect of the heterostructure on the V_{OC} will be seen later on when constructing to the solar cell and will be discussed more in detail in the V_{OC} issue section in the end of this chapter.

4.2 Passivated Porous Silicon

4.2.1 Mechanisms of Electrochemical Passivation and Condition Calculations

Porous silicon has a very large surface area compared to bulk silicon and is thermodynamically unstable. At present, thermal oxidation in the presence of a catalyst is mainly used as a method to reduce the surface recombination rate, but since it is a high temperature process, there is a possibility that structural change and oxidation may progress for porous silicon. In the case of passivation by formation of an oxide film, it is necessary to advance oxidation under milder conditions. Therefore, in this research, we considered forming an oxide film using an electrochemical method. By appropriately selecting the current density and the oxidation time, it is expected that the oxide film is thick enough to subdue the dangling bonds on the surface uniformly and thin enough that it does not act as a resistive oxide layer as in Figure 34.

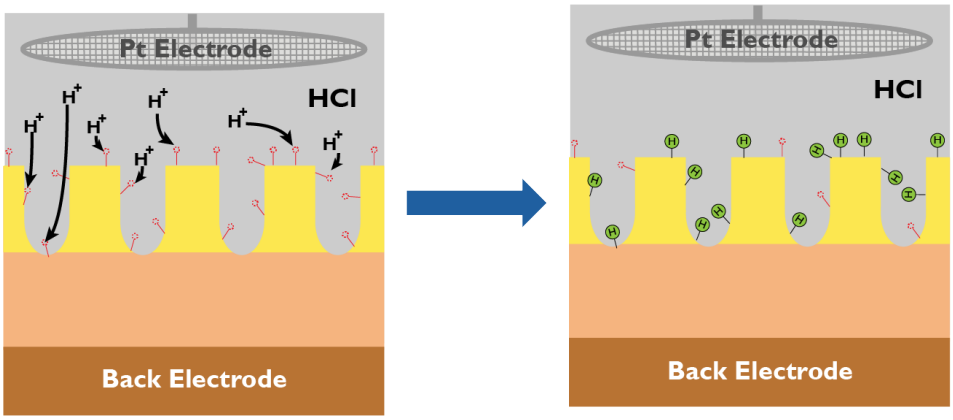


FIGURE 34: ELECTROCHEMICAL PASSIVATION REACTION SCHEME

However, when considering the reaction inside the pore, the control of the nanostructure cannot be achieved without considering which the reaction rate or mass diffusion is dominant.

The redox reaction formula of silicon when hydrochloric acid is used as the electrolyte is shown in equations 27 and 28.

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \quad \text{……...……(27)}$$

$$2H^+ + 2e^- \rightarrow H_2 \quad \text{……...… (28)}$$

As can be seen from these equations, in the oxidation reaction of silicon (equation 27), H_2O is consumed and H^+ is formed, so the diffusion of these species becomes dominant. If the resistance of the substrate is low enough, as in a silicon wafer, the reaction on the surface of the pore will selectively occur as shown in Figure 35 (Top) which means that the diffusion is slower than the reaction, so a SiO_X film is formed to cover the top of the porous structure. On the other hand, if the reaction is rate-determining, the reaction occurs uniformly over the entire wall surface of the pores, and it is considered that an oxide film is formed along the porous structure as in Figure 35 (Bottom). Therefore, it is required that the oxidation be performed in a place where the reaction is sufficiently slower than diffusion process.

Considering the rates of reaction and diffusion, the Thiele number is used as an indicator, shown in equation 29

$$h = \sqrt{\frac{k}{D / L^2}} \quad \text{……..……(29)}$$

Where k = reaction rate constant

D = diffusion coefficient

L = pore depth.

From this equation, since the k of the numerator is an indicator of reaction rate and the denominator D/L^2 is an indicator of diffusion rate, it can be understood that the Thiele number indicates the ratio of reaction rate and diffusion. As described above, in order to form an oxide film along the porous structure, conditions are required that the reaction is sufficiently slower than diffusion. Therefore, it is sufficient to set conditions that make the Thiele number smaller. However, the reaction rate constant contained in the Thiele number is generally difficult to measure. Therefore, we examined the use of the modified modulus using the average reaction rate r instead of the reaction rate constant k., the average reaction rate r is divided by the species concentration C_0 on the pore surface to achieve a dimensionless parameter, and the corrected modulus is given by the equation 30.

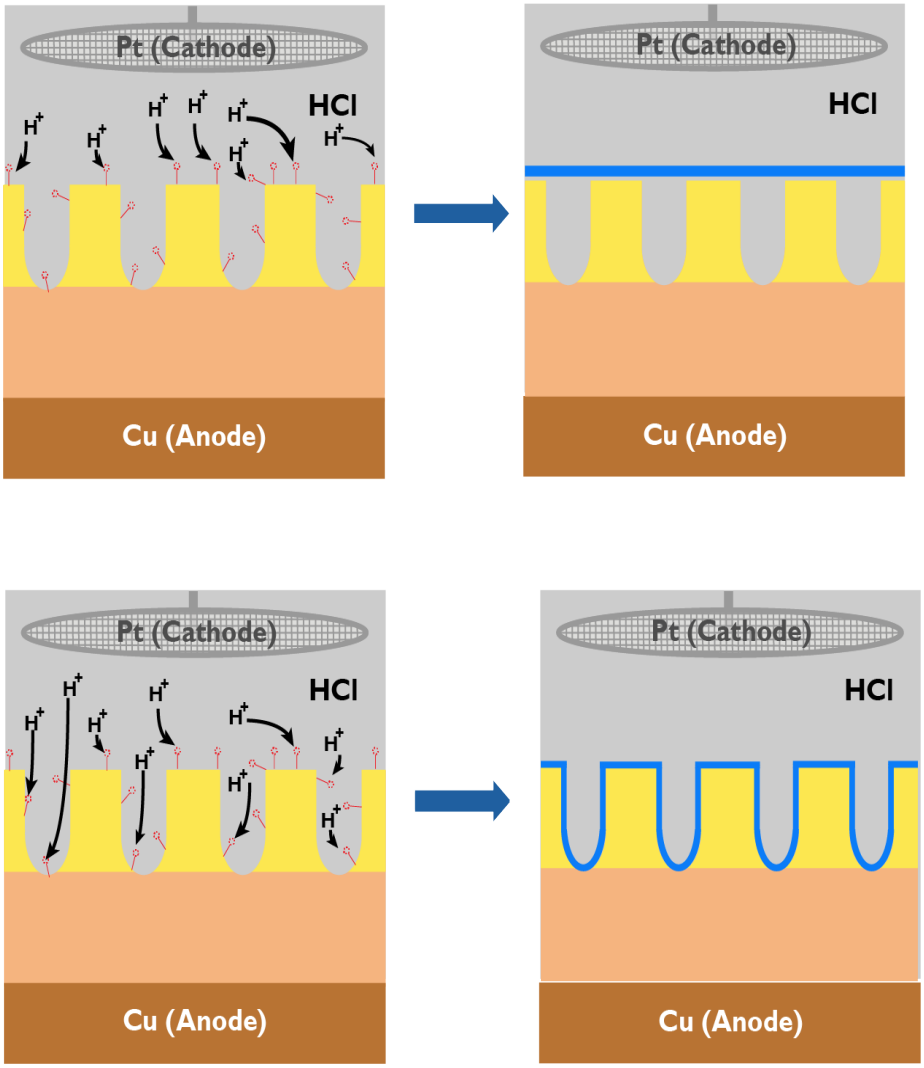


FIGURE 35: DIFFERENCE IN OXIDE FORMATION BETWEEN DIFFUSION LIMITED (TOP) AND REACTION LIMITED (BOTTOM)

$$\Phi\ [-] = \frac{r / C_0}{D / L^2} = \frac{\text{Reaction}}{\text{Diffusion}} \quad \text{.....(30)}$$

That is, if the correction modulus is a sufficiently small value, it is expected that the oxide film formation along the porous structure will be promoted. The depth dependence of the concentration of chemical species in the pores during the reaction at different Thiele number and modified modulus values is shown Figure 36. The vertical axis is based on the concentration of chemical species on the surface, and the horizontal axis is based on the bottom of the pore. In order to form an oxide film of the same thickness on the surface and bottom of the pore, the concentration of chemical species must be equal. Therefore, in this experiment,

calculation was performed with Φ = 0.15. The parameters used for other calculations are shown Table 5. Since the surface observation could not be clearly seen in the porous silicon fabricated in this experiment, the pore diameter and the pore spacing necessary for the calculation were based on the passivation conditions previously performed in this laboratory, calculation was performed by combining the porous layer thickness found by the SEM image. The SEM images of porous silicon used as a reference are shown Figure 37, and the diffusion coefficient of hydrogen ions is the literature value [103]. As a result, an anodization time of 135 seconds and a current density of 0.1012 mA/cm^2 were obtained.

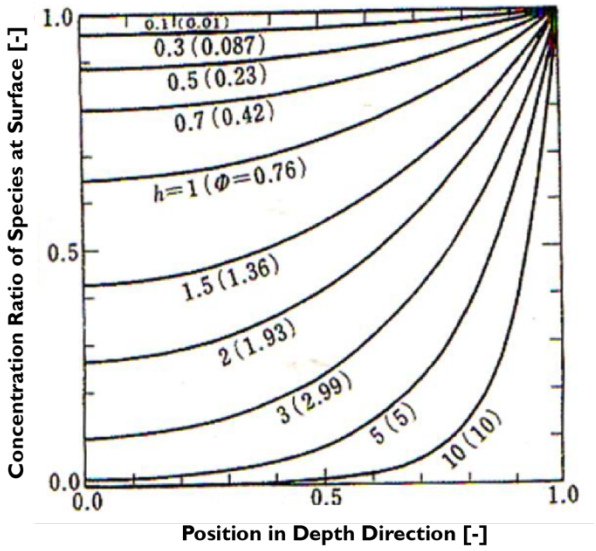


FIGURE 36: SPECIES CONCENTRATION RATIO VS. PORE DEPTH [104]

TABLE 5: PARAMETERS TO CALCULATE THE OXIDATION CONDITION

Parameter	Value
Pore Diameter [nm]	17.1
Porous Layer Depth [nm]	200
Pore Spacing [nm]	60.7
SiO_2 Film Thickness [nm]	2
HCl Concentration (C_0) [mol/L]	1
H^+ Diffusion Coefficient [m^2/s]	2.21×10^{-9}

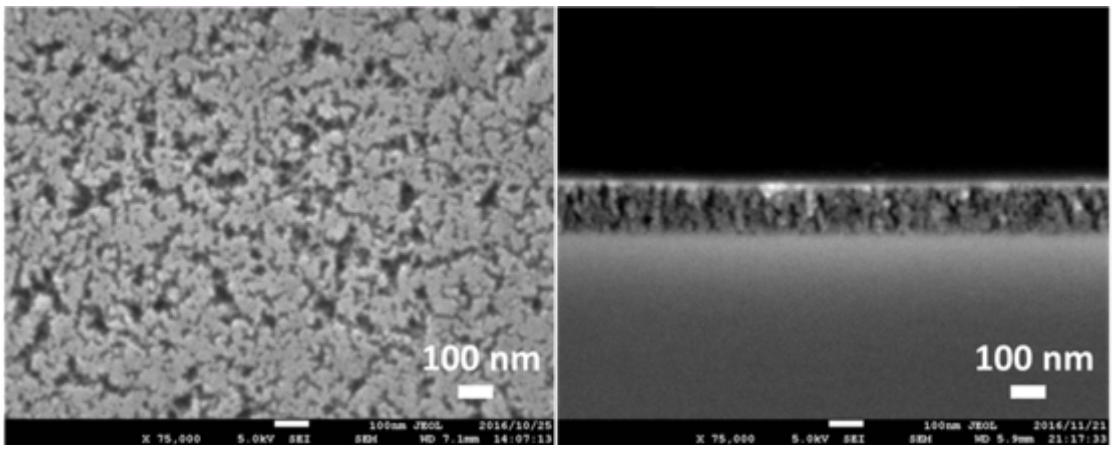


FIGURE 37: SEM IMAGES OF POROUS SILICON AS REFERENCE FOR CALCULATION [105]

From the calculation, the longer the oxidation time, the thicker the oxide film layer. When the current density of 0.1012 mA/cm^2 is kept constant and the oxidation time is varied, the relationship illustrated Figure 38 is obtained.

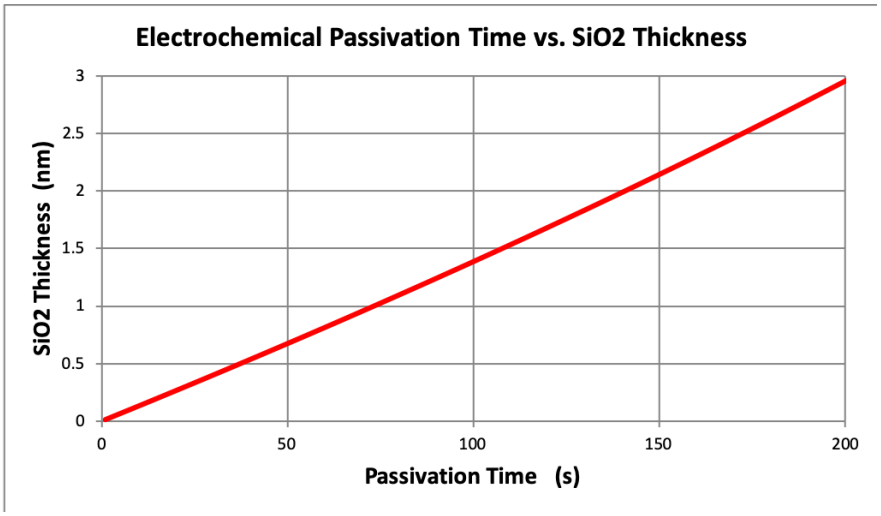


FIGURE 38: ELECTROCHEMICAL OXIDATION TIME (*T*) VS. SIO_2 FILM THICKNESS

Then electrochemical passivation time is varied to investigate the effect of SiO_2 thickness to the conversion efficiency. The oxidation time chosen to passivate the porous silicon solar cell together with its calculated thickness is listed in Table 6.

TABLE 6: OXIDATION TIME SELECTED TO POROUS SILICON SOLAR CELL FABRICATION

Oxidation Time [s]	Calculated SiO_2 Thickness [nm]
6	0.08
10	0.13
15	0.20
20	0.27
30	0.40
60	0.81
90	1.24
135	2

In this experiment, there are three passivation methods selected as a way to deactivate the dangling bonds of the nano-porous surface. The first method, ALD passivation is used as the representative method and for comparison to other passivation methods as it is a common passivation technique for crystalline silicon solar cell. Second, the electrochemical passivation is a method developed in this research to achieve a uniform passivation thin film on porous silicon with faster processing time and lower cost. Lastly, the supercritical fluid (SCF) passivation technique is experimented by using SCF unique properties of gas and liquid to penetrate through the nano-pore and dissolve the unwanted dangling bonds.

4.2.2 SEM of Passivated Porous Silicon

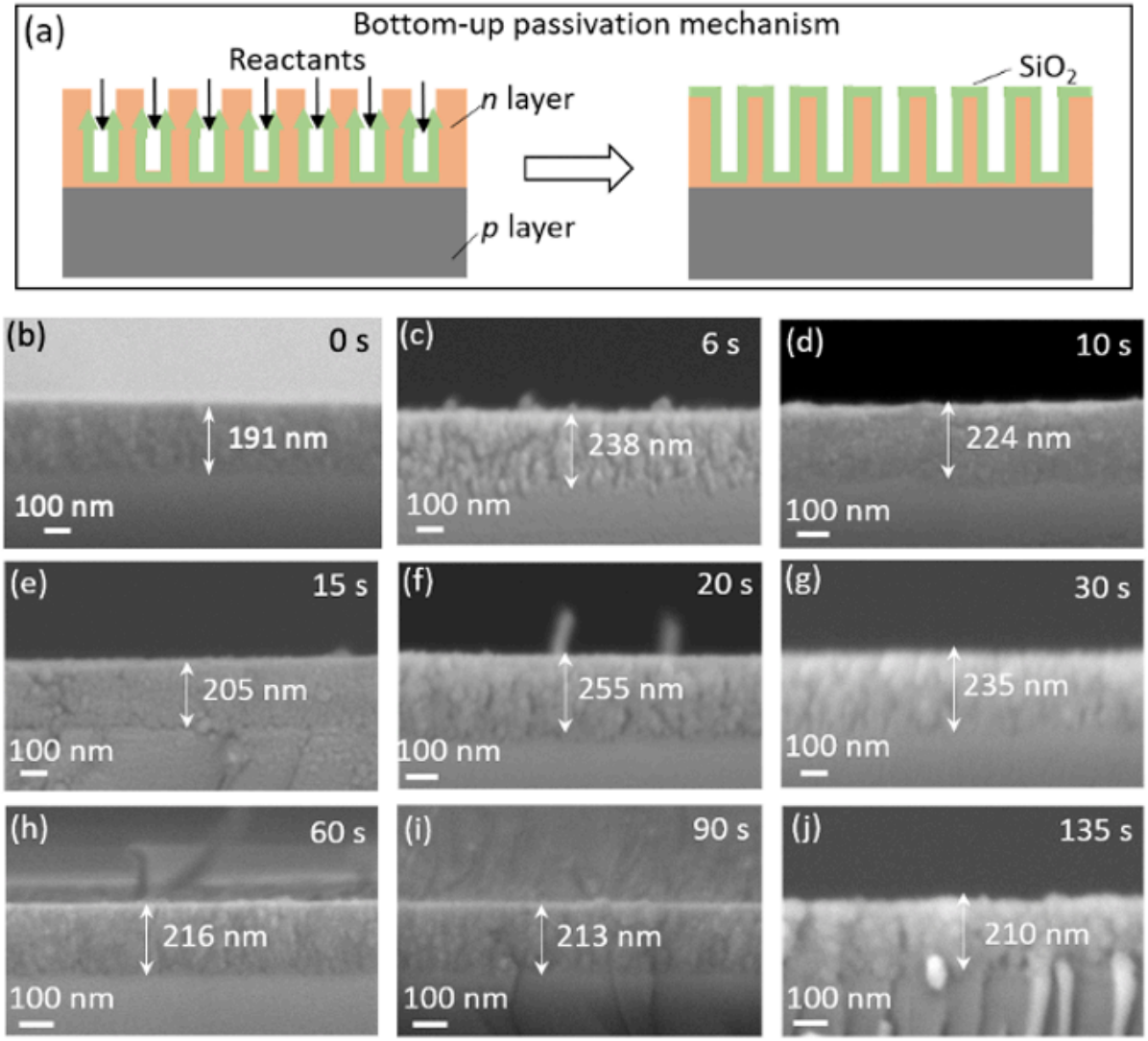


FIGURE 39: (**A**) DIAGRAM OF THE BOTTOM-UP ANODIZATION MECHANISM OF SIO_2 PASSIVATED POROUS SILICON LAYER; (**B-J**) CROSS-SECTIONAL SEM IMAGES OF FABRICATED POROUS SILICON WITH DIFFERENT POROUS LAYER THICKNESS

The anodization and electrochemical passivation process described in previous section is used to fabricate porous silicon layers with thicknesses of 191–255 nm, and which were then surface-passivated via anodic SiO_2 formation. Figure 39b–j shows cross-sectional SEM images of these porous layers with homogeneous morphology. The anodic oxidation process is carried out for passivating the porous silicon layers with different passivation time (t) of t = 6 s, 10 s, 15 s, 20 s, 30 s, 60 s, 90 s, and 135 s. This scale of SEM images shows that the original porous structures are not affected by the anodic oxidation process; the uniformity of the porous structure of these passivated samples(Figure 39b–j) is still maintained compared to that of the sample without passivation (Figure 39a).

4.2.3 Passivation Film Evaluation by Carrier Lifetime Measurement

All three passivation techniques are evaluated with the carrier lifetime measurement. The summary of the average lifetime is shown below in Table 7, and all colored mapping local lifetime is illustrated in Figure 40 for ALD-passivated porous silicon, Figure 41 for porous silicon without passivation, Figure 42 for electrochemical passivated porous silicon, and Figure 43 for SCF passivated porous silicon. All samples are undoped.

TABLE 7: SUMMARY OF AVERAGE LIFETIMES

Sample	Average Lifetime (μs)
No Passivation 1	**2.94**
No Passivation 2	**2.975**
No Passivation 3	**2.822**
ALD 20 nm (no annealing)	**3.737**
ALD 20 nm (annealing 400°C for 20 m)	**8.12**
ALD 20 nm (annealing 200°C for 15 m)	**3.007**
Electrochemical Passivation 1	**2.628**
Electrochemical Passivation 2	**1.797**
Electrochemical Passivation 3	**5.105**
SCF Passivation 1	**2.187**
SCF Passivation 2	**2.171**

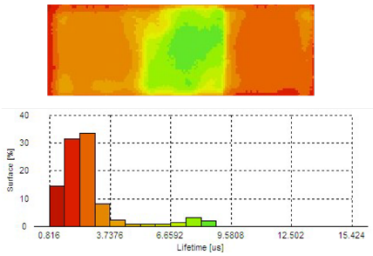


FIGURE 40: CARRIER LIFETIME OF ALD-PASSIVATED AT DIFFERENT CONDITIONS: NO ANNEALING (LEFT), ANNEALING AT 400°C FOR 20 MIN (MIDDLE), ANNEALING AT 200°C FOR 15 MIN (RIGHT) MEASURED BY SEMILAB

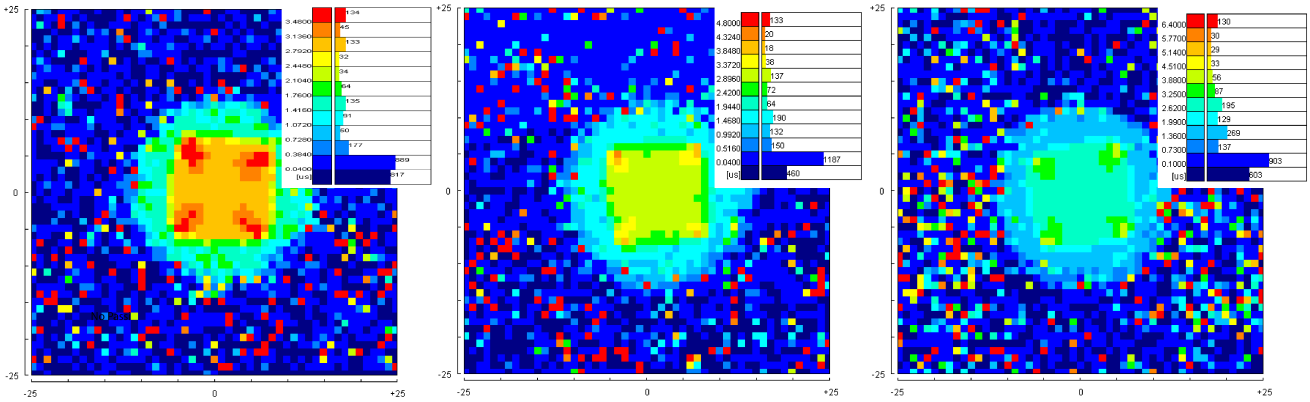


FIGURE 41: CARRIER LIFETIME OF 3 POROUS SILICON SAMPLES WITHOUT PASSIVATION (MEASURED BY MWPCD)

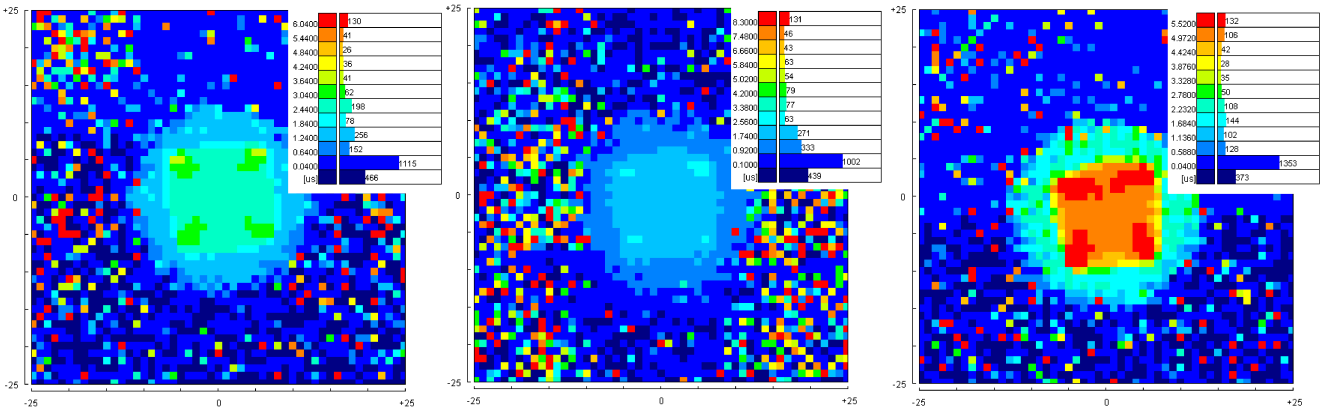


FIGURE 42: CARRIER LIFETIME OF POROUS SILICON WITH ELECTROCHEMICAL PASSIVATION (MEASURED BY MWPCD)

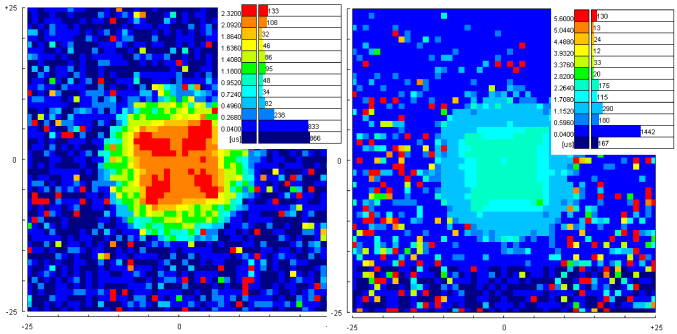


FIGURE 43: CARRIER LIFETIME OF POROUS SILICON WITH SCF PASSIVATION (MEASURED BY MWPCD)

As seen from the Table 7, all of the carrier lifetimes are very short compared to the lifetimes that can be considered suitable for c-Si cells. The longest lifetime is 8.12 µs from ALD-passivated sample 2 (annealing at 400°C for 20 minutes), and the shortest is 1.797 µs from electrochemical passivated sample 2. The samples without passivation have lifetimes ~2.9 µs, while SCF passivation sample is ~2.18 µs. For ALD passivation, the longest lifetime of 8.12 µs is believed to come from the effective annealing process when compared to ones without annealing and with an annealing temperature of 200°C for 15 minutes. After alumina forming the bond with the dangling bond, the annealing makes it an Al_2O_3 film, which suggests

that the condition of ALD sample 2 is the best so far. For the electrochemically passivated sample, the short lifetime is first believed to come from the lack of back passivation of the wafer. However, the ALD method does not passivate the back side, while SCF passivation method passivate the whole wafer. So, the effect of back passivation cannot be deduced in this experiment.

The other reason for the short lifetime is believed to be the structure of porous silicon itself. As the porous structure observed in SEM images is not a well-defined pore, more like an amorphous structure, all of the passivation methods need the access to the deep part of the pore in order to uniformly passivate the structure. As it is a 3-D porous structure, the passivating molecules are probably unable to penetrate through the complex structure despite using the SCF method, which has a high penetration property of SCF CO_2.

In conclusion, from the carrier lifetime perspective, there is no obvious improvement from each passivation process because all the obtained lifetimes are relatively short compared to the common crystalline silicon. The further optimization of the passivation condition is needed in the future work.

4.2.4 TEM Images of ALD-Passivated Samples

The TEM measurement is performed only for the ALD-passivated samples to observe the annealed Al_2O_3 structure as well as the porous silicon layer. Three ALD thicknesses are measured: 5 nm, 10 nm, and 20 nm. Figure 44 shows all the TEM images:

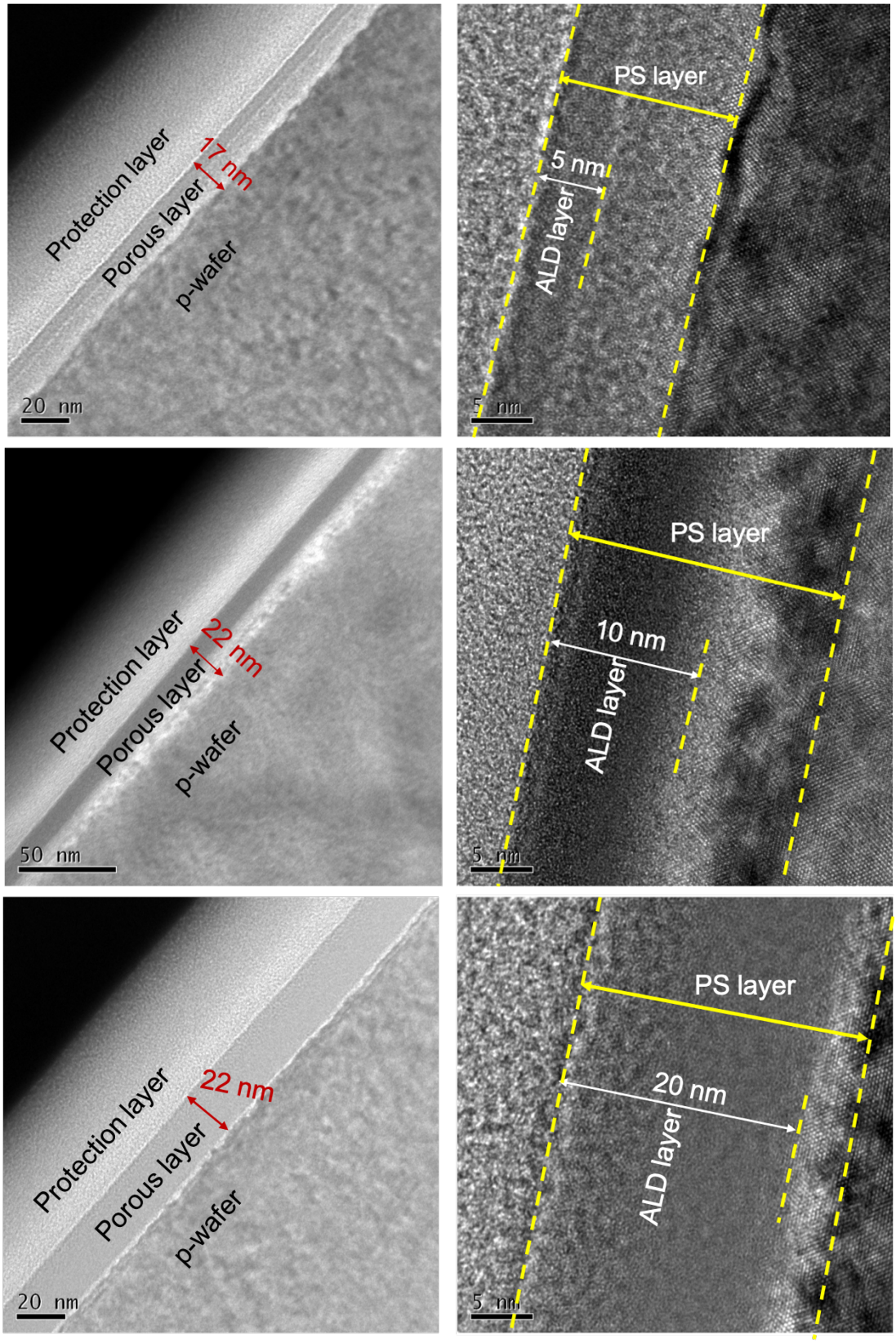


FIGURE 44: TEM IMAGES OF ALD PASSIVATION ON POROUS SILICON WITH DIFFERENT ALD THICKNESSES: 5 NM (TOP), 10 NM (MIDDLE), AND 20 NM (BOTTOM)

From the images, ALD is confirmed to lead to a formation of a film (seen in a darker color) on the surface of the porous silicon and the thickness is precisely controlled. However, the ALD film is only formed on the top part of the porous silicon; the alumina only diffuses through the pore to the set depth, not all the way through to the bottom of the pore. This results in the non-uniform passivating film over the whole structure, leaving the deep portion of the pore un-passivated, and may be the reason of the short lifetime. We will show below that after fabricating the solar cell, the performance of the ALD-passivated porous silicon solar cell is poor, as well as the diode characteristic, resulting in a very high series resistance. This is believed to result from the annealed ALD-film forming a resistive layer, which impedes the generated electron transport to the top electrode. In addition to the amorphous structure discussed in SEM section, the ALD-sample with 20 nm thickness also does not have the orientation of <100>, but a complicated structure with two- or three- dimensional orientation, which prevents the alumina to reach the bottom of the pore. Also, there is no alumina layer on the surface, which is uncommon because the alumina layer should also be deposited on the pore's top surface and be detected by TEM. Therefore, further optimization of the ALD thickness together with the annealing temperature and time is needed.

4.3 Passivated Porous Silicon Solar Cell

In this section, we will discuss about the solar cell parameter measured after completely fabricated the solar cell by depositing the electrode via the thermal evaporator on the front (fishbone) and back surface (square).

4.3.1 SEM Observation of Ag Electrode and Porous Silicon

For reference, the FE-SEM image is recorded to investigate the thickness of Ag electrode over the porous silicon. From Figure 45, the Ag electrode thickness is confirmed to be in the range of 40 – 60 nm, while the porous silicon thickness is, again, confirmed to be within 200 - 250 nm range. This inhomogeneity of the thickness results from the uncontrollable input current to the tungsten carbide wire from adjusting the volt-slider, even though the heating time is controlled.

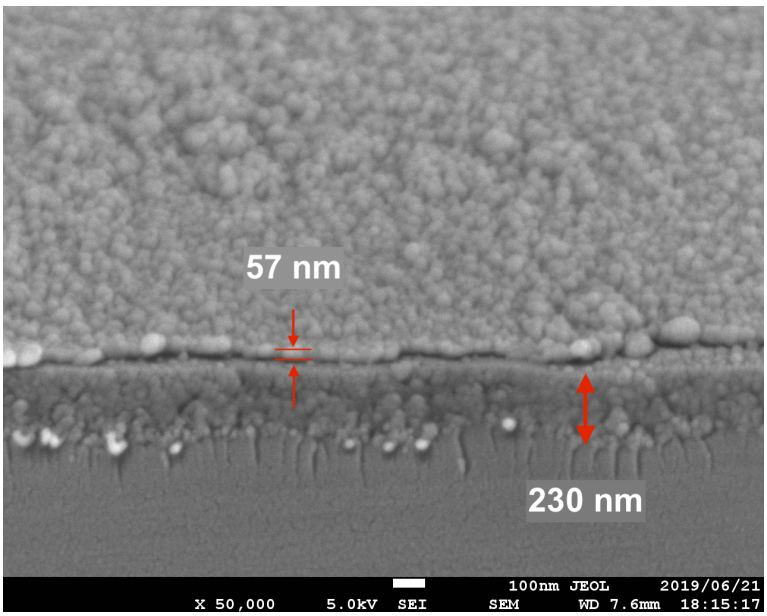


FIGURE 45: SEM IMAGE OF CROSS-SECTION POROUS SILICON WITH AG ELECTRODE

4.3.2 Solar Cell Performance of ALD-Passivated Samples

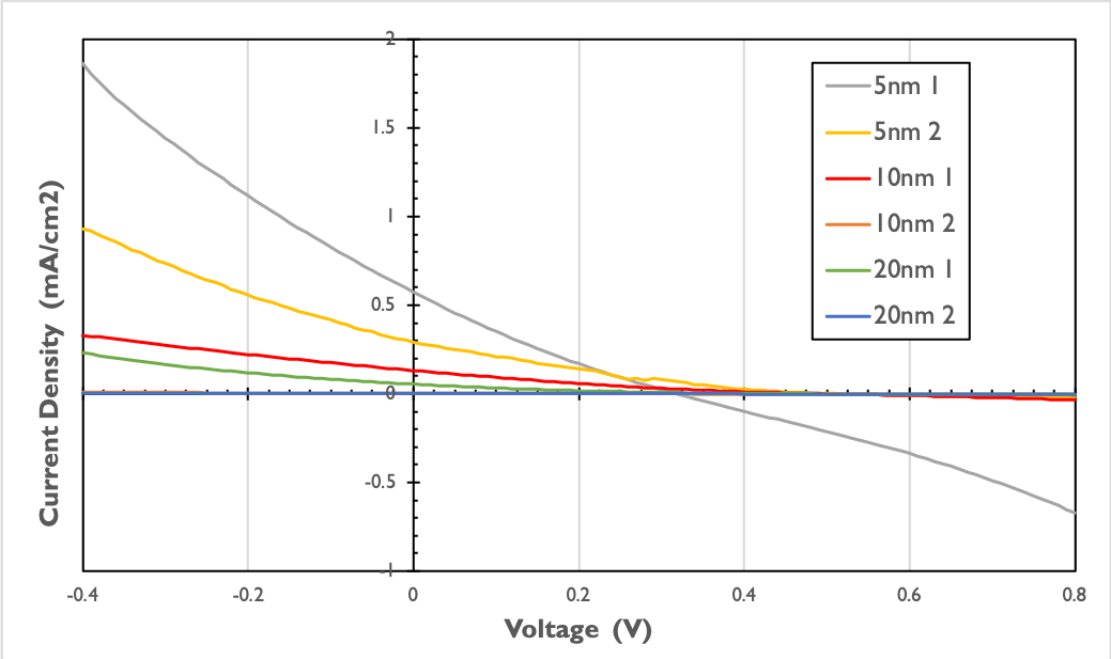


FIGURE 46: J-V CURVE OF ALD-PASSIVATED SAMPLES

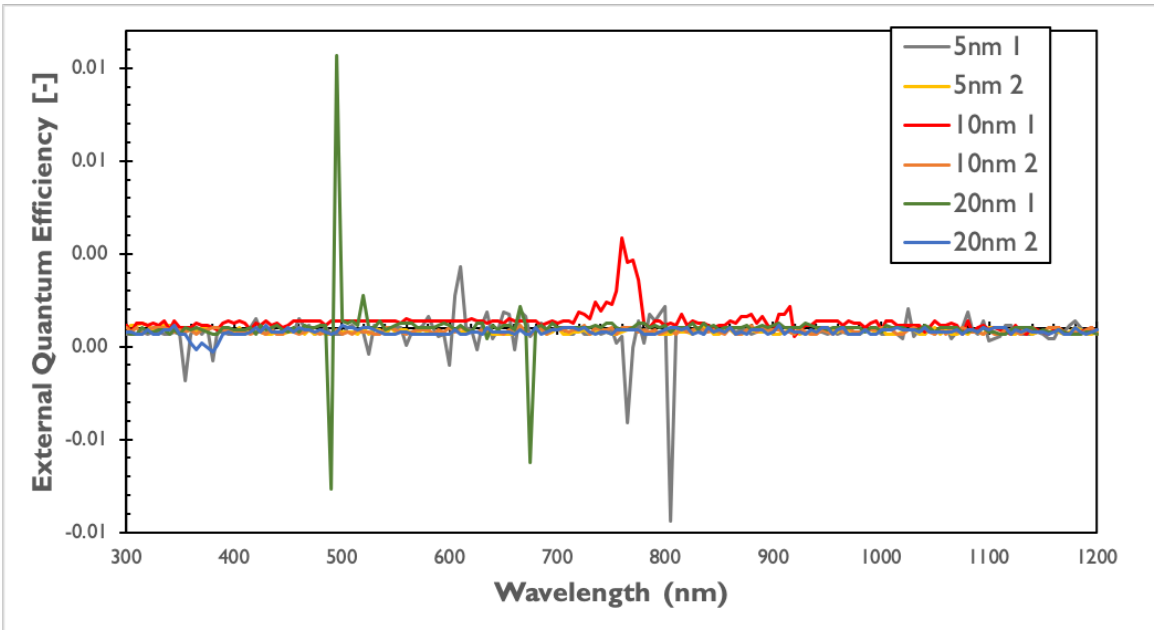


FIGURE 47: EXTERNAL QUANTUM EFFICIENCY OF ALD-PASSIVATED SAMPLES

From Figure 46, the summary of the solar cell parameters is shown in Table 8.

TABLE 8: SOLAR CELL PARAMETERS FOR ALD-PASSIVATED SAMPLES

Sample	**J_{SC}** [mA/cm^2]	**V_{OC}** [V]	**FF** [-]	**Eff.** [%]
5nm 1	**0.6585**	**0.3174**	**0.2114**	**0.044**
5nm 2	**0.3328**	**0.5203**	**0.1928**	**0.033**
10nm 1	**0.1516**	**0.4979**	**0.1788**	**0.014**
10nm 2	**0.0022**	**0.4625**	**0.1067**	**0**
20nm 1	**0.0625**	**0.491**	**0.1383**	**0.005**
20nm 2	**0.0006**	**0.4927**	**0.1359**	**0**

From Table 8, the highest J_{SC} is 0.6585 mA/cm^2 produced by the ALD-5 nm thick. The lowest J_{SC} is 0.0006, almost zero, produced by the ALD-20 nm thick. Most of the V_{OC} are in

the range of 0.49 to 0.52 V, which is the V_{OC} of this research's silicon wafer, while the best sample of 5-nm 1 has V_{OC} only 0.3174 V. All FF are poor due to the low J_{SC} and V_{OC}.

As discussed in TEM images section, after fabricating the solar cell, the performance is poor as the J_{SC} is very low. The thicker the ALD-film, the lower the J_{SC}, which confirms that the film is active as a resistive layer rather than the passivation film. Also, this layer blocks the current to flow easily, it also results in bad EQE shown in Figure 47. The contact between Ag electrode and alumina layer has a very high resistance compared to the contact with electrochemically passivated layer, which will be discussed in next section. The reason is that the ALD layer is very thick with 5, 10, and 20 nm of alumina, while the oxide layer made by electrochemical passivation has a calculated thickness of only 0.02 – 2 nm, which allowing the current to flow through more easily and allowing the tunneling to occur. This could be one of the reasons why J-V characteristics of ALD-deposited samples are not good. It is believed that removing the alumina layer before depositing the electrode by etching with HF on the resin mask, or by lithography could result in smaller contact resistance. This oxide layer removal also applies for the electrochemical passivation as it would greatly improve the electrode/emitter contact. Finally, regarding the post-annealing treatment, it is believed that there could be some structural change in the porous structure due to the high temperature and is needed to further optimized.

4.3.3 Solar Cell Performance of Porous Silicon with Electrochemical Passivation

Figure 48a shows the J–V curves for the porous silicon (PS) solar cell, PS-(a-h) cells passivated with SiO_2 formed by the anodic oxidation process, and for the reference c-Si solar cell under AM1.5 illumination. The measured PV performances and parameters for these samples are listed in Table 9. All the cells exhibit a good diode-like behavior, although the effect of the passivation time (t) is outstanding. The passivated PS-e cell (t = 30 s) demonstrates the greatest η of 10.7%, whereas the PS cell (i.e., no passivation) obtains a η of 5.15% (Figure 48b and Table 9). From Figure 48c, all the porous silicon layer cells (data marked with red symbols) exhibit a significant increase in J_{SC} when compared to the reference c-Si cell (23.4 mA/cm^2), indicating the improvement due to the porous silicon layer's anti-reflective property. However, when considering the effect of the passivation time to J_{SC}, we can see that it is not

responsible for this improvement in η, as the J_{SC} of the PS-e cell (with passivation) and the PS cell (no passivation) are similar, 29.8 mA/cm^2 and 29.9 mA/cm^2, respectively.

This significant increase in η is, instead, a result of a substantial increase in FF from 0.321 to 0.685. Figure 48d shows the t dependence of FF. The FF increases with increasing t up to 30 s in passivated cells (PS-(a-h) cells), which peaks at the value of 0.685. This coincides with an increase in J_{SC} without a significant loss in V_{OC}. The initial increase in J_{SC} up to t of around 30 s suggests that the SiO_2 layer is being passivated more adequately and has better coverage on the pore surfaces, yielding the best η. These results indicate that the porous silicon layer's microscopic pores are successfully filled by the bottom-up anodization process, and that the surface recombination is greatly reduced. However, for the longer t (t > 30 s), the J_{SC} decreases due to lower conductivity of SiO_2 caused by overoxidation. As seen in Figure 48e, all of the porous silicon solar cells have similar V_{OC}, in the range of 0.51-0.54 V, which is lower than the 0.7 V typically obtained from heterojunction with intrinsic thin layer (HIT) solar cells using a-Si as emitter. As this is the crucial issue for this thesis purpose of using the porous

silicon as a higher band gap material to improve the V_{OC} of the top cell of tandem, it deserves its own discussion part at the end of this chapter.

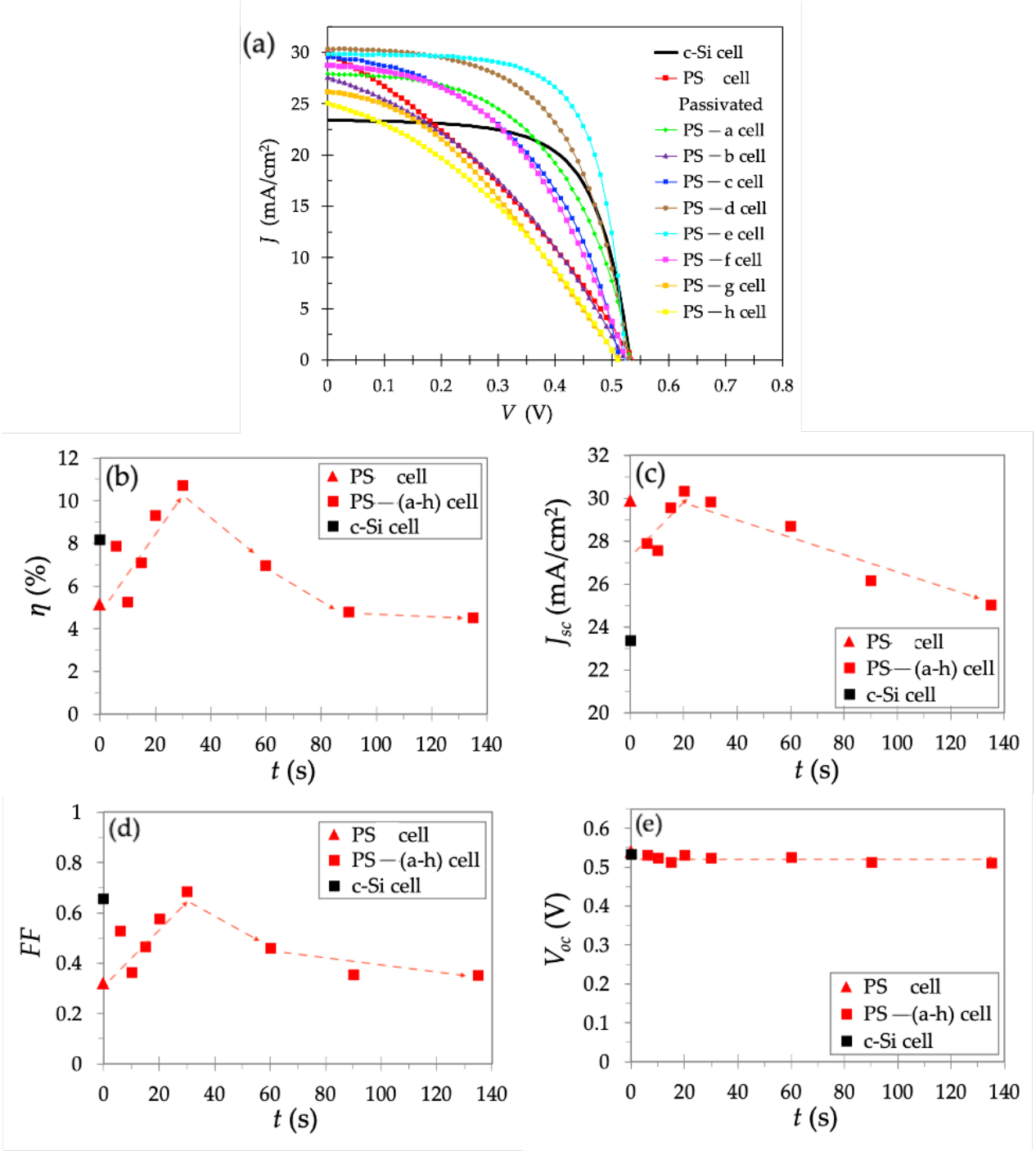


FIGURE 48: (**A**) *J-V* CURVES; (**B**) EFFICIENCY (η); (**C**) J_{SC}; (**D**) *FF*; (**E**) V_{OC} OF POROUS SILICON CELL, PASSIVATED PS-(A-H) CELLS FOR DIFFERENT PASSIVATION TIME (*T*), AND REFERENCE *C*-SI CELL.

TABLE 9: PV PARAMETERS FOR POROUS SILICON CELL, PASSIVATED POROUS SILICON CELLS FOR DIFFERENT PASSIVATION TIME (T), AND REFERENCE C-SI CELL.

Samples	*t* (s)	PS layer thickness (nm)	V_{oc} (V)	J_{sc} (mA/cm²) [1]	*FF*	η (%) [1]
c-Si cell	0	0	0.532	23.4	0.657	8.16
PS cell	0	191	0.539	29.9	0.320	5.15
Passivated PS-a cell	6	239	0.532	27.9	0.530	7.86
Passivated PS-b cell	10	224	0.524	27.6	0.364	5.25
Passivated PS-c cell	15	205	0.514	29.6	0.466	7.08
Passivated PS-d cell	20	255	0.531	30.4	0.578	9.32
Passivated PS-e cell	30	235	0.523	29.8	0.685	10.70
Passivated PS-f cell	60	216	0.526	28.7	0.462	6.97
Passivated PS-g cell	90	213	0.513	26.2	0.357	4.79
Passivated PS-h cell	135	210	0.511	25.0	0.354	4.52

[1] J_{SC} and η were calculated based on the active area.

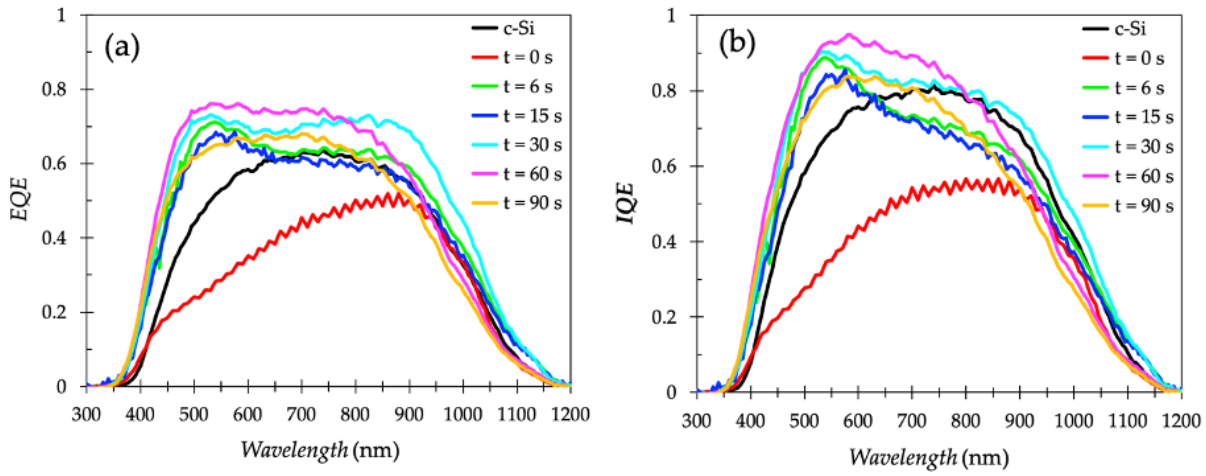


FIGURE 49: (**A**) EQE; (**B**) IQE OF POROUS SILICON CELL FOR DIFFERENT *T* COMPARED WITH AS-FABRICATED POROUS SILICON CELL (T=0), AND REFERENCE *C*-SI CELL

The passivated porous silicon solar cells show an improved EQE compared to c-Si solar cells over the whole spectra, especially at wavelengths between 300 and 1100 nm, which is attributed to the excellent anti-reflection feature of the porous silicon structure. All passivated porous silicon solar cells exhibit a remarkable enhancement compared to c-Si solar cell in the blue region of 300-600 nm. This might be the result from the enhanced light trapping properties of porous silicon. This has also been reported in the literature [17]. Among the porous silicon solar cell with passivation, when t = 30 s, a substantial improvement in the 700–1100 nm wavelength region is observed. This suggests a longer diffusion length due to adequate surface

passivation and reduced reflectivity at that wavelength range (700-1100 nm), resulting in the best FF. Because most of the light in the long wavelength region usually traverses through the semiconductor material unabsorbed, the improvement in the incident photons trapping at the 700-1100 nm wavelength range is crucial for the application in thin-film solar cells structure.

Compared to the passivated porous silicon and c-Si, the unpassivated porous silicon cell has the lowest IQE throughout the spectra, which could be attributed to its high front surface recombination at short wavelengths as well as to its rear recombination at long wavelength. The rear recombination is usually a major cause of the decrease in the absorption of the long wavelength photons and also those with low diffusion lengths. But most importantly, this poor IQE caused by the high surface recombination negates the advantage of porous silicon low surface reflectance. This can be prevented by the electrochemical passivation. As can be seen in Figure 49b, the anodic SiO_2 surface passivation greatly improves the IQE values. Especially when t = 30 s, a wider spectrum in the range of 300–1100 nm wavelength is all improved. This indicates that the surface recombination of the passivated porous silicon cells has been sufficiently reduced, and the minority carrier diffusion length has been improved.

As was mentioned in the preceding section, porous silicon solar cells are also passivated using ALD layers that are 5, 10, or 20 nm thick. However, under AM1.5 illumination, these passivated cells perform poorly in terms of PV parameters. This is because the formation of Al_2O_3 films in these high aspect-ratio porous silicon structures is diffusion-limited [106]. The reactants are blocked from penetrating deeper along the pore walls by the consequent downward trend in the saturation front process. This provides additional proof that the anodization SiO_2 technique is better than ALD method for surface passivation of the porous silicon. On the other hand, no discernible impact of the thickness of the porous silicon on the performance of such solar cells is observed (Figure 50).

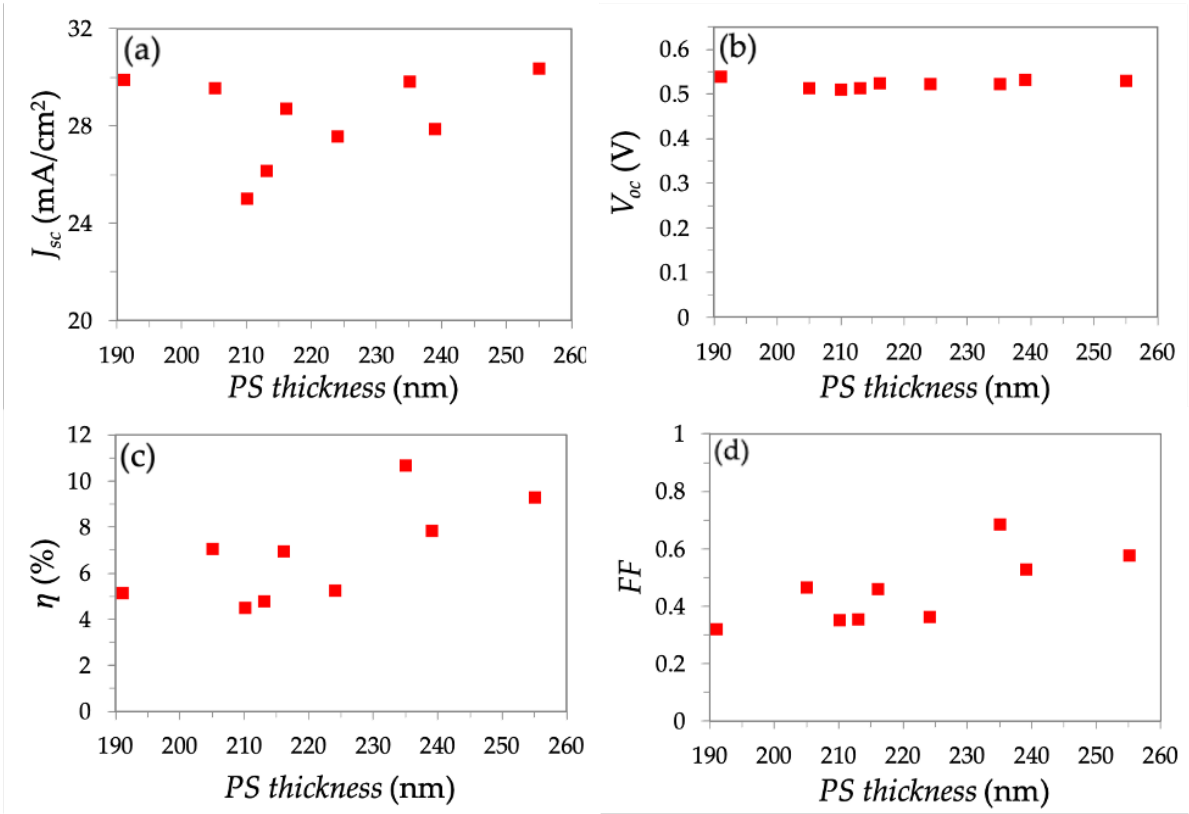


FIGURE 50: DEPENDENCE OF THE POROUS SILICON THICKNESS ON PV PARAMETERS OFPPOROUS SILICON CELLS: (A) J_{SC}; (B) V_{OC}; (C) EFFICIENCY (η); (D) FF.

Figure 51 shows the R_S (a) and R_{SH} (b) of the as-fabricated PS cell (no passivation, t = 0), passivated PS-(a-h) solar cells as a function of t, with the c-Si cell as a reference. The as-fabricated PS cell has a comparatively high value of R_S = 18 cm^{-1} when compared to the c-Si cell, indicating an inadequate passage of light-generated current through the as-fabricated PS layer and the base of the solar cell. It also corresponds to the lowest R_{SH} of 0.067 kΩ cm^{-1} as a result of the power losses induced by the alternate current route to the light-generated current in the as-fabricated PS cell. Because the as-fabricated PS cell is not passivated, a non-uniform oxide layer is formed on the porous silicon layer surface due to the uncontrollable native oxidation. This nonuniformity of the native oxide layer can behave as a crystal defect, providing an excess of trapping states and hence promoting the surface recombination process. When the recombination current is sufficiently strong, it can function as a shunt [107]. As a result, despite having a high J_{SC} of 29.9 mA/cm^2 and V_{OC} of 0.539 V, which is comparable to the passivated PS cells (Table 9), a substantial amount of light-generated current is lost in the PS cells due to the high recombination process caused by the nonuniformly passivated surface, resulting in the low R_{SH}, FF, and η.

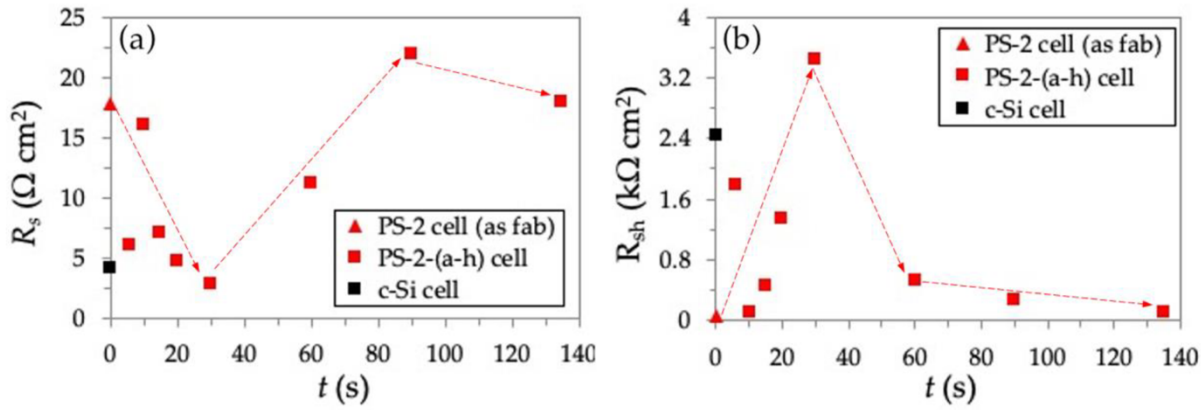


FIGURE 51: CORRELATION BETWEEN *T* AND: (**A**) R_S; (**B**) R_{SH} FOR POROUS SILICON CELL, PASSIVATED PS-(A-H) CELLS AND REFERENCE *C*-SI CELL.

As seen in Figure 51a, for the passivated PS-(a-h) solar cells, R_S declines with increasing *t* from 0 to 30 s, then gradually increases afterwards. The passivated PS-e cell achieves the lowest R_S of 2.79 cm^{-1} at t = 30 s. This lowest value is attributed to the increased light-generated current through the passivated PS-e cell, which has fewer defect-trapping states and also the reduced Ag front electrode penetration into the inadequately passivated pore, resulting in a decrease in R_S. However, the further anodic SiO_2 formation (at $t > 30$ s) could, instead, become an ineffective carrier transport medium. Since the Ag electrode is directly deposited on the passivated porous silicon surface, the contact resistance between the metal and the silicon material might increase [17].

In solar cells, the power losses due to R_{SH} indicate an undesired extra parallel high-conductivity path across the p-n junction for light-generated current. Figure 51b illustrates the variation of R_{SH} in respect to *t*. The R_{SH} increases fast initially, then peaks at 3.45 kΩ cm^{-1} at *t* = 30 s. This suggests that the lower loss of light-generated current across the p-n junction is achieved due to the reduced recombination rate caused by the surface passivation of porous silicon. The decrease in R_{SH} as *t* increases longer than 30 s also corresponds to an increasing tendency of R_S under the same *t*. At $t > 30$ s, the overoxidation of anodic SiO_2 formation increases the R_S between the metal contact and the silicon. On the other hand, the R_{SH} decreases as the recombination rate increases for an unidentified reason. The crystal defects caused on by excessive oxidation might be the possible origin to lowers R_{SH} further [107].

4.3.4 Analysis of the implied V_{OC} of the fabricated porous silicon by QSSPC

From the result of V_{OC} in previous section, we can see that the are no observed improvement even though the porous silicon is fabricated. One of the reasons of this lack of V_{OC} improvement might not originate from the absence of band gap expansion, but the limitation inside each layer of the solar cell itself. Therefore, we perform the detailed characterization by Quasi-Steady-State Photoconductance (QSSPC) bulk lifetime measurement to evaluate the implied V_{OC} of each layer. The implied V_{OC} value is measured by analyzing the photoconductance of the samples and it represents the upper limit of the V_{OC} of the measured semiconductor device without taking into account the recombination loss from metal/silicon interface.

To evaluate the effect of each layer to its implied V_{OC}, the structures are fabricated in the symmetrical configuration to eliminate the surface recombination asymmetry between front and rear surfaces, which affects the accuracy of the measured photoconductance [108]. Figure 52 shows the measured structures and the result is listed in Table 10.

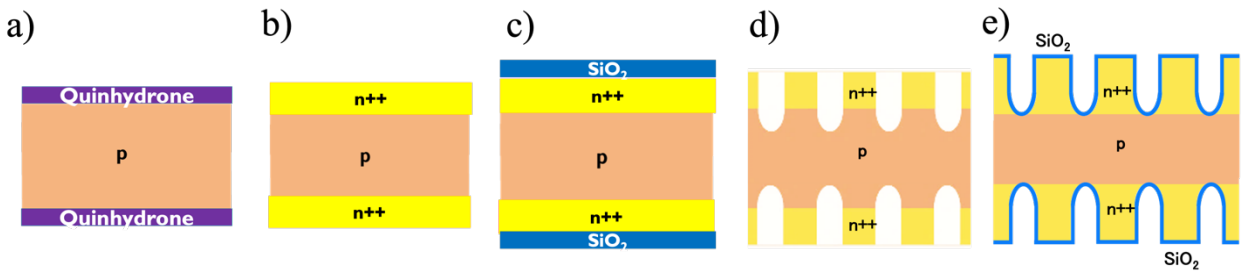


FIGURE 52: THE SYMMETRICAL STRUCTURES MEASURED BY QSSPC TO EVALUATE THE IMPLIED V_{OC} OF EACH LAYER: A) P-TYPE BASED C-SI WAFER; B) N++-EMITTER; C) N++ EMITTER WITH ELECTROCHEMICAL PASSIVATION; D) POROUS N++-EMITTER; E) POROUS N++-EMITTER WITH ELECTROCHEMICAL PASSIVATION.

TABLE 10: THE RESULT OF THE IMPLIED V_{OC} MEASURED BY QSSPC IN EACH LAYER OF THE PASSIVATED POROUS SILICON SOLAR CELL

	Structures	Evaluated layer	Implied V_{OC}
a	Quinhydrone/p-c-Si/Quinhydrone	Base c-Si wafer	0.687 V
b	n++/p-c-Si/n++	n++ emitter	0.590 V
c	SiO_2/n++/p-c-Si/n++/ SiO_2	Passivated n++ emitter	0.586 V
d	Porous-n++/p-c-Si/Porous-n++	Porous layer	0.583V
e	SiO_2/Porous-n++/p-c-Si/Porous-n++/SiO_2	Passivated porous layer	0.586 V

The first evaluation is the implied V_{OC} of the p-type base c-Si wafer. The QSSPC measurement is performed after using quinhydrone/methanol treatment to the wafer. This Quinhydrone/methanol passivation is known to have a surface recombination velocity of about 5 cm/s when applied to c-Si. This surface recombination velocity is then small enough for evaluation of the quality of the Si wafer [109], [110]. The implied V_{OC} of the base wafer is 0.687 V, which indicates that the maximum V_{OC} obtained by using this wafer is 0.687 V. In the other words, if the perfect emitter and rear side passivation are applied to the wafer, 0.687 V is a maximum. Therefore, the V_{OC} of this solar cell is not limited by the bulk lifetime of the c-Si base wafer.

Next is the emitter quality. The implied V_{OC} are measured to be 0.590 V. It is clearly seen that the n++ emitter layer is responsible for the decrease in implied V_{OC}. This is believed to be a result of two main causes. First there could be a contamination of the metal particle inside the emitter layer, which could come during the thermal diffusion process in the annealer. Secondly, this could result from the excessively high doping concentration of the n++ emitter layer. In general, as the doping concentration of the emitter increases, the reverse saturation current decreases and thus the V_{OC} of the cell increases. However, if the cell is doped beyond a certain optimum value, this will instead lead to the decrease in the minority carrier lifetime, which increase the reverse saturation current and, importantly, the band gap narrowing [111], [112]; thus, directly result in the reduction of the V_{OC} and overall efficiency. Therefore, it suggests that the doping concentration in emitter layer is too high. By optimizing the doping level of the phosphorus so that the minority carrier lifetime is high enough such that the minority carrier diffusion length is longer than the p-n junction depth, it is expected that the cell V_{OC} could be improved.

Regarding the effect of electrochemical passivation as well as the porous structure, the result from Table 10 shows that there is no significant change in implied V_{OC} compared to the structure with n++ emitter. This might suggest that the influence of excessively high doping level of emitter layer overwhelms the passivation and pore-structuring effect and becomes a main factor that determines the upper limit of minority carrier lifetime.

Finally, as can be seen from Table 9, the actual measured V_{OC} of all of samples are around 0.51-0.53 V, which indicates that there are additional factors that further reduce the V_{OC} from 0.58 of the implied V_{OC}. This could be caused by the high recombination rate at metal/silicon interface on both front and rear Ag electrode as this recombination of the minority carrier is one of the major causes to limit the V_{OC} as well as the efficiency of the cell [113]–[116]. As the porous silicon is sensitive to the thermal treatment, there is no metallization step

after depositing the Ag electrode. This could result in the poor contact as the Ag cannot diffuse through the silicon sufficiently; thus increase the recombination rate of the interface and further reduce the V_{OC} as a result [117], [118]. The front side electrode might have less effect compared to the rear side as the contact is deposited on the highly doped n++ emitter layer, which has a smaller contact resistance compared to the lightly doped p-type base wafer with the Ag back electrode. It is also smaller in size as it is deposited in the fishbone shape compared to the whole-surface deposition on the back. This could be mitigated by metallizing the electrode after fabrication at lower temperature and a very short period of time, so that the effect on porous structure is kept at minimum.

4.3.5 Discussion on the V_{OC} issue of porous silicon solar cell

As can be seen from the Figure 48e, there are no significant improvement of V_{OC} compared to the c-Si cell in every sample. This is an important issue as one of the purposes of using porous silicon is for its higher band gap energy to improve the top layer of the all-Si tandem solar cell. As the V_{OC} is defined by the splitting of the quasi-Fermi levels of electron and hole in the photoactive semiconductor material (n+ porous silicon emitter in this thesis), the maximum difference between these two levels is theoretically limited by its band gap. That is why it was expected that the use of porous silicon, which was previously proposed to have a higher band gap resulted from the quantum confinement effect, could increase the V_{OC}.

The first possible reason of this lack of V_{OC} improvement is that the fabricated porous silicon with this anodization condition has a structure that is still relatively large for the quantum size effect to occur efficiently. This small quantum size effect of the material may not be adequate for the significant improvement of V_{OC} and acts only as an anti-reflective layer.

Furthermore, the other reason is believed to be the result of the nature of the heterojunction structure of this PS/c-Si solar cell itself. As the porous silicon layer has the thickness only around 200 nm, compared to the thick bulk c-Si layer below (200 μm), which is roughly 0.1% of overall material; Other literatures of photovoltaic effect in porous silicon material fabricated on the on c-Si substrate structures also reported the same behavior of the V_{OC} being governed by the base layer. All of the reported PS/c-Si structures so far have a limited V_{OC} in the range of 0.08–0.52 V [119]–[121], which also coincides with the values observed in this thesis. It is also stated that the origin of the observed photovoltaic effect and contribution of bulk and porous silicon is difficult to analyze due to the contribution of both the metal/PS contact and the heterojunction between porous silicon and the c-Si substrate [122],

[123]. The only way to characterize the effect of porous silicon material is to fabricate the free-standing layers, which will eliminate the PS/c-Si heterojunction and the immense influence from the underlying c-Si substrate. The improvement of V_{OC} from the free-standing nanopores silicon has already been reported in [123], which yield the value of 0.87 V. However, the other PV parameters are poor in the pure structure of porous silicon; that is why the optimization of the thickness of porous silicon and the effective surface passivation was considered in this thesis.

To further explain this dominating influence on the V_{OC} of the c-Si in heterojunction structure, the absorption spectra of c-Si and porous silicon must be compared. From a comparison of the absorption spectra reported in [124], [125], it is quite obvious that for energies below 1.7-1.8 eV, which is the ideal band gap energy for PS/c-Si tandem structure, the absorption coefficient of c-Si is at least one order of magnitude larger than that of porous silicon. The absorption length of porous silicon is around 30 μm at this 1.7-1.8 eV. Thus, for the 200-nm-thick porous silicon in this research, not only that the porous layer is transparent to photon below this energy, but the absorption is also too low with this thickness. That is why most of the useful absorption takes place in the c-Si part of the sample. Therefore, the V_{OC} is determined by the underlying c-Si layer. For photon energies above 1.7-1.8 eV, since the absorption length of porous is smaller than 30 μm, the absorption in PS will become significant depending on the thickness of the porous silicon layer. However, the thicker porous layer also increases the surface area, which in turn increase the surface recombination rate. For photon in higher energy range, even though most of the electron-hole pairs are created in porous silicon, the carriers either cannot reach the built-in electric field or cannot diffuse towards the respective collecting electrode due to the thick layer of porous silicon.

4.4 SIMULATION OF THE PASSIVATED POROUS SILICON MODELS

In this part of the thesis, simulation is used to investigate the electronic structure of different PSi/c-Si model systems in order to verify the possibility for the improvement of the V_{OC}. Various models were generated in order to study the effects of each component of PSi on the band gap and band alignment. Briefly, the models were generated by cutting the desired morphology from c-Si with a home-made code, hydrogenated all the dangling bonds (passivation), relaxed by using MD method, and finally calculated the electronic properties by using DFTB method. The analysis was based on the evaluation of the density of states (DOS).

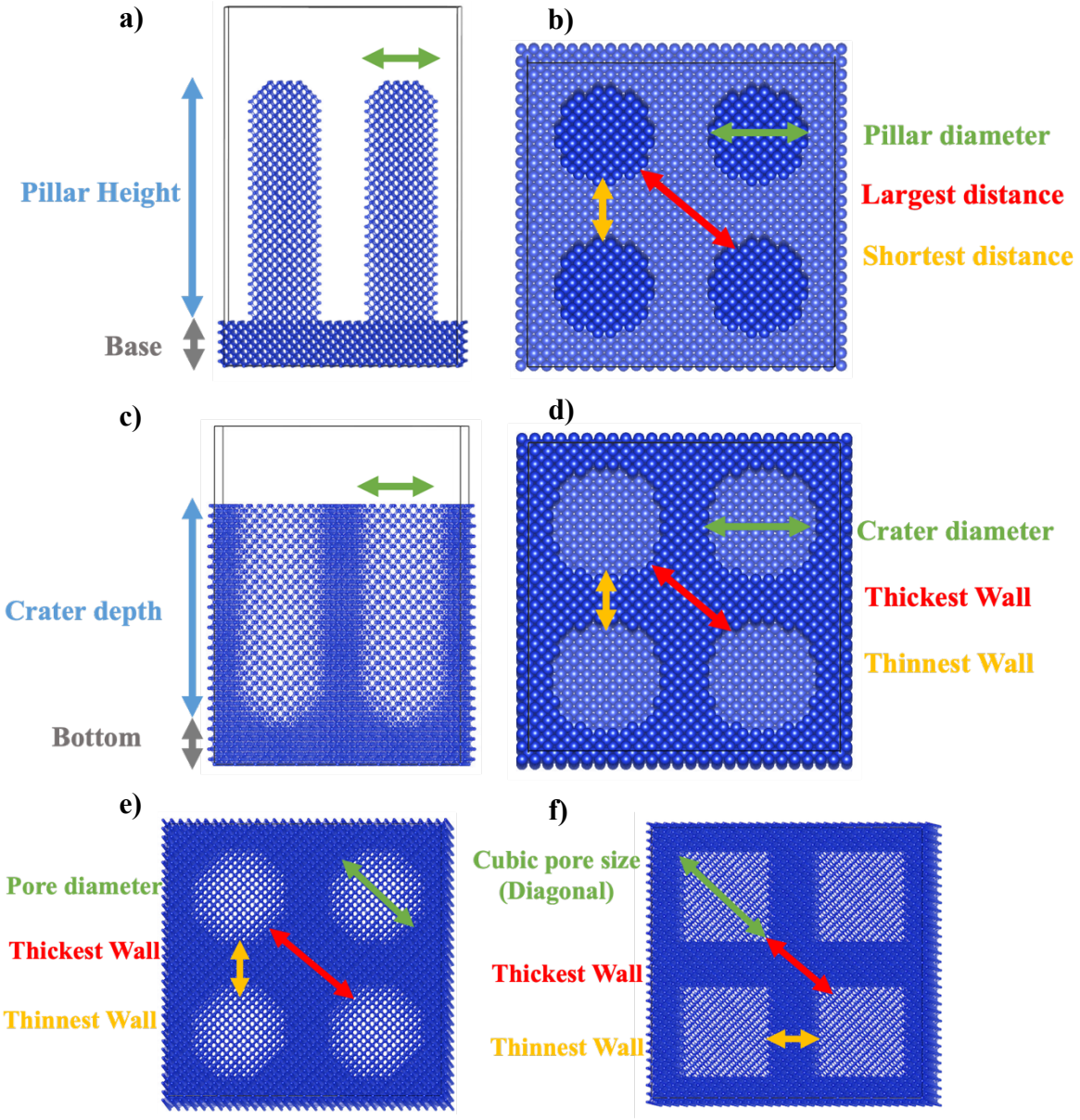


FIGURE 53: MODELS GENERATED TO SIMULATE POROUS SILICON WITH DIFFERENT KEY FEATURES. (A) INTERNAL CUBE MODELS (B) INTERNAL SPHERE MODELS (C) PILLAR MODELS (SIDE VIEW) (D) PILLAR MODELS (TOP VIEW) (E) CRATER MODELS (SIDE VIEW) (F) CRATER MODELS (TOP VIEW). 2×2 PERIODIC SIMULATIONS CELLS ARE SHOWN TO DEMONSTRATE INTER-FEATURE DISTANCES.

Four kinds of models are generated to be representative of the PSi/c-Si structure., These models are show in Figure 53, they are: a pillar model, a crater model, an internal sphere model, and an internal cube model. These models contain features typical of real PSi. The pillar model is used as a simplified model of real PSi some of which has oblong pillar-like features to investigate the effect on each components more distinctively. The crater model is the more realistic model to the porous silicon that is fabricated by using an anodization process like the one used in this thesis. The internal cube model is used to clearly illustrate the effect of the thickness of the Si framework (rather than the pore size) and any quantum confinement effect resulting from it on the electronic structure. All have a 2-nm vacuum layer on top of each model to represent the real-world situation where the top porous silicon layer is exposed to the surrounding. The vacuum layer also allows calibrating the vacuum level which is necessary to compare the PDOS of different models, as described in Methods.

As mentioned before in the V_{OC} related discussion in the experimental part, as the PSi/c-Si structure in this thesis is of heterojunction type, the measurement of the overall band gap of the whole material would give the value of the smaller band gap material (in this case, bulk c-Si). Therefore, even though the porous silicon of the top layer has a higher band gap induced by the quantum confinement effect, the effect would be masked by the smaller band gap material.

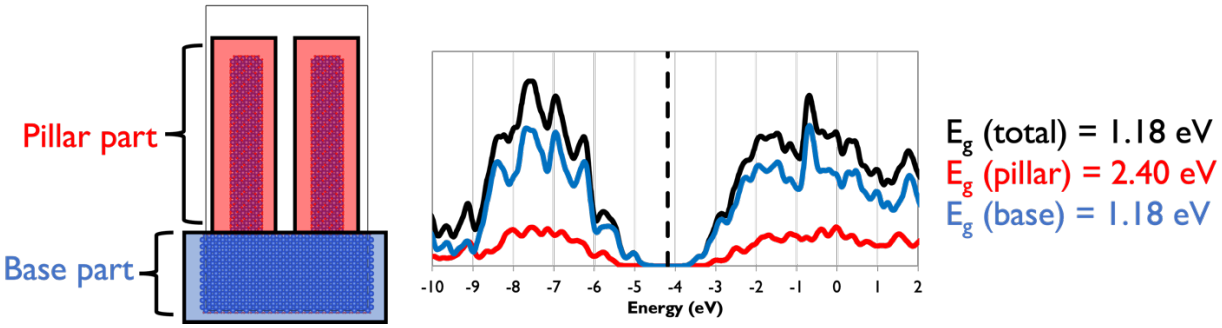


FIGURE 54: CLARIFICATION OF THE LOCAL DENSITY OF STATES (DOS) AND THE INSTRUCTION TO INTERPRET THE DATA

For example, Figure 54 shows the model with two different component: **Pillar** and **Base** parts. The **overall density of states (DOS)** is the summation of the local density of states of every component of the model. Therefore, even if the pillar part of the model has a larger band gap (e.g., from quantum confinement effect) than the base part, the overall DOS will show that overall model has a band gap of that with smallest band gap. When considered **separately**, the local band gap of each component could be observed. In this case, the pillar with 1-nm

diameter has a local DOS of 2.40 eV, which is then masked by the 1.18 eV base layer. Therefore, with such evaluation of local DOS, the true effect of the quantum confinement effect can be investigated. The DOS results of this simulation part will be discussed with this method of evaluation, where the “pillar”, “base”, ‘wall’, and “bottom” labels in the figures will indicate the local DOS of each component.

4.4.1 Internal Sphere and Cube Models

For the spherical pore models, spheres of different radii were carved in periodic cells of sizes from about 2 to 5 nm. The parameters of the models, including box sizes, numbers of Si and passivating H atoms, pore diameters *d* and resulting inter-pore distances and porosities are listed in in Table S1. The inter-pore distances are distinguished as follows: the shortest inter-pore distance *l* which is realized by crossing the cubic simulation cell laterally and the largest inter-pore distance *L* which is realized crossing the cubic simulation cell diagonally (in 3D). These distances define the thickness of the Si framework which ultimately determines the extent of any nanosizing effect. Table S1 also lists the resulting bandgaps as well as band edges. The densities of states are shown in Figure 55 (top). The band gap of crystalline Si with computational setup of this thesis, which serves as a reference for any nanosizing effects, is 1.12 eV and is in good agreement with the experimental value. One observes a trend of the band gap with the size of the model features. The XL3 model represents a case where the pore size is very small while the interpore distance is the largest, with *l* of about 2.9 nm. In this case the band gap is practically the same as in pure Si, with no gap expansion. The smallest S models show the largest gap expansion, up to 1.54 eV.

The band gap expands by simultaneously lowering the VBM and lifting the CBM, as expected for a nanosizing effect. In this case, the trend of the gap is with the thickness of silicon framework, not the size of the pore. M and L models also show a similar trend. The gap expands even as the pore size is increased, as long as the size of Si features drops.

To achieve a significant gap expansion, silicon features need to become smaller than 1 nm. This is because the electronic states of interest, which undergo nonconfining, are localized on Si and not in the pore. To put it simply it is not the hole of the doughnut that provides a useful effect. Achieving gap expansion with porosity should therefore aim at controlling the size of Si features rather than the size of the pores or the porosity as such.

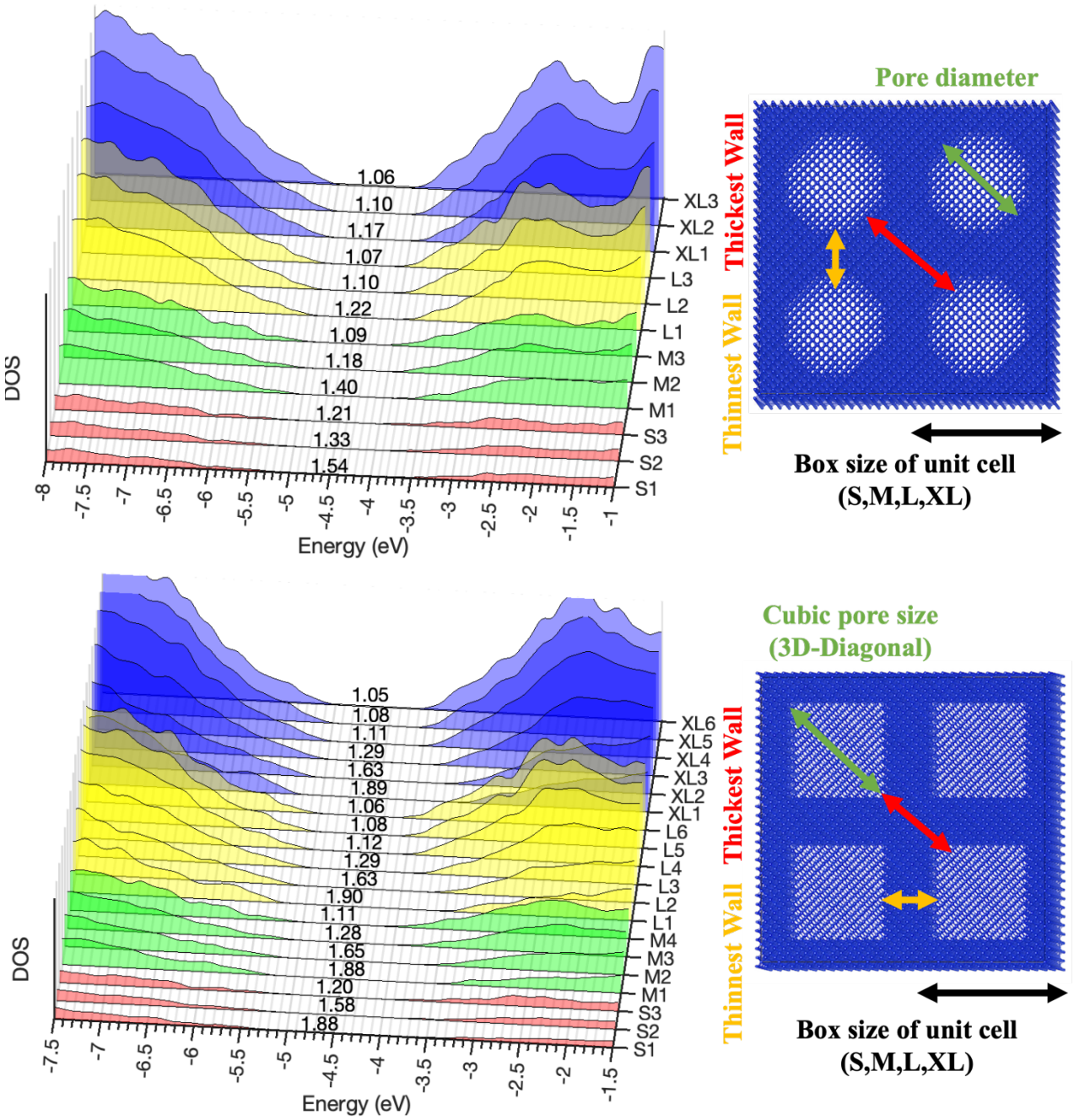


FIGURE 55: THE DENSITY OF STATES (DOS) RESULT AND THE BAND GAP VALUE INDICATED AT THE MIDDLE OF EACH DOS PLOT (TOP) INTERNAL SPHERE MODELS; (BOTTOM) INTERNAL CUBE MODEL; THE MODELS ARE SHOWN FOR 2×2×2 SIMULATION CELLS FOR BETTER VISUALIZATION.

To solidify this statement, the calculations on cubic-sized pores are performed, which have a simpler-shaped Si framework than Si with spherical pores, with a clear size parameter – wall thickness. Here, we consider the pore (cube) size, the wall thickness, and the largest Si feature thickness which is a 3D diagonal at the simulation cell vortex. The results are listed in Table S2, and the corresponding densities of states are shown in Figure 55 (bottom). We see that Si features need to approach 1 nm for a significant band expansion to occur. Sub-nm features are

needed to approach the optimal (from the perspective of a Si-Si tandem solar cell) gap of 1.7 eV. The Si feature sizes in these models required for significant gap expansion are smaller than those experimentally observed here and elsewhere. We therefore explore below other morphologies more relevant to the experimental structures.

4.4.2 Pillar Model

In this model, the pillar structure is used to study the effect of 4 silicon features (pillar height, diameter, inter-pillar distance, and base thickness) on its band gap and band alignment. Previous works reported the band gap of silicon nanowires depending on the wire (pillar) diameter [126], [127]; some having connected the pillar to a base layer, but with a relatively small number of atoms [128] and much smaller scales than the Si feature sized used in the experiment. **For the first time, this thesis investigates the band gap and band alignment of the other Si pillar features: pillar height, base layer thickness, and the interpillar distance, and at scales relevant to the experiment.** To simulate these features more realistically, the large number of atoms is required (thousands of atoms). The electronic structure of such a large-scale mode can be calculated by DFT calculation within a reasonable time even with GGA functionals (commonly used for solid state modeling) which grossly underestimate the bandgap, while hybrid functionals which allow computing more realistic bandgaps at a much higher computational cost are out of question. As explained above, using the DFTB method makes such calculations feasible, while the bandgap is more accurate than with GGA DFT due to the existence of an efficient parameterization for Si-based systems [64], [79]. The parameters of the models, including simulation cell sizes, numbers of Si and passivating H atoms, pillar height, base layer, pillar diameter, inter-pore distances and porosities are listed in in Table S3.

In Figure 56, the DOS for the pillar models with different combinations of pillar height and diameter and base layer thickness are shown. Only one parameter is varied in each graph, while others are kept constant. Here and elsewhere, the DOS of different parts are plotted in different color (pillar: red, base: blue, total: yellow), and the bandgaps computed from the DOS of different parts are also given on the graphs in their respective colors.

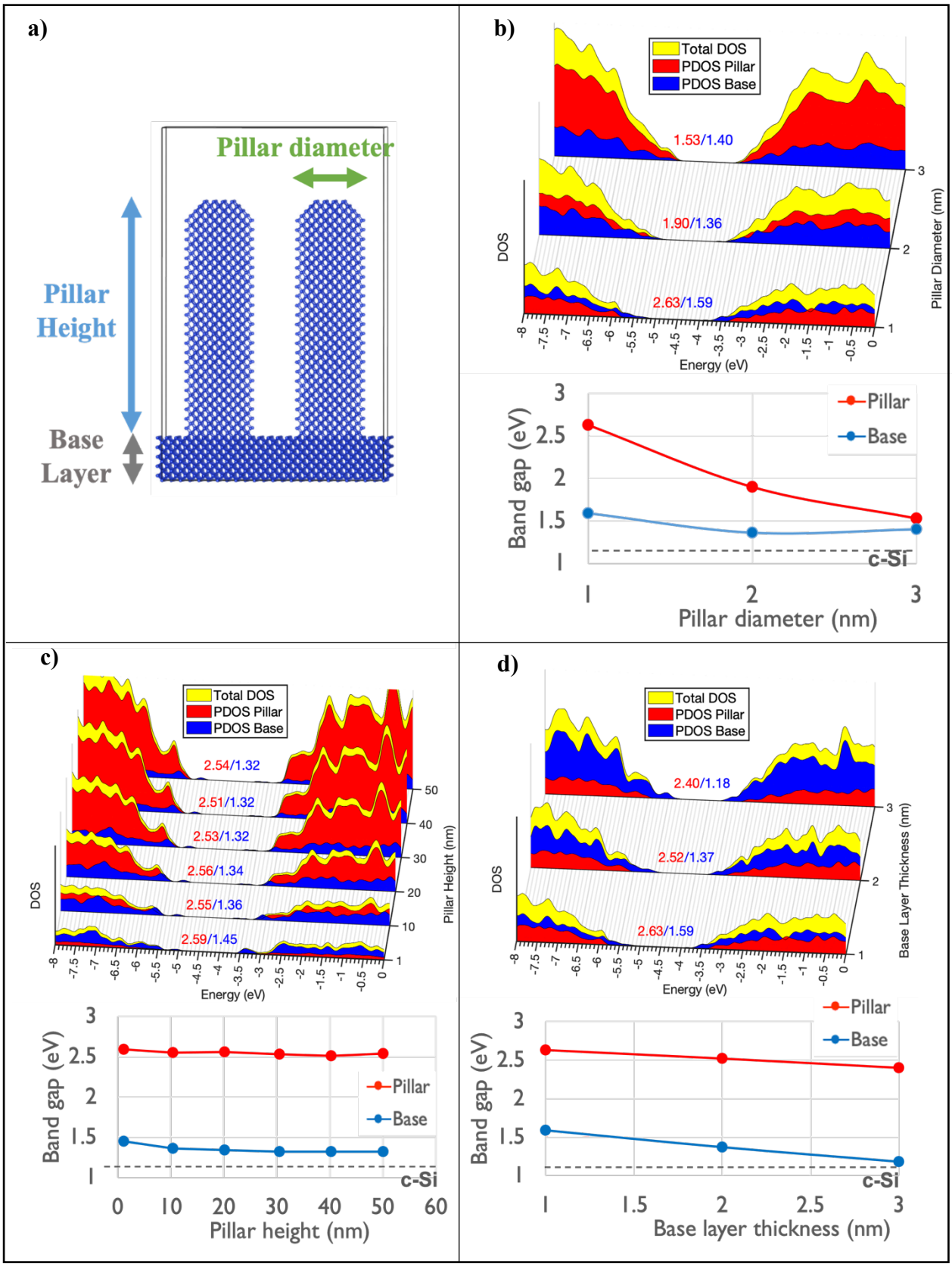


FIGURE 56: 3 EFFECTS OF THE PILLAR FEATURES ON THE BAND GAP AND BAND ALIGNMENT; (A) THE PILLAR WITH KEY FEATURES INDICATED (2×2×1 SIMULATION CELLS ARE SHOWN); (B) THE EFFECT OF THE PILLAR DIAMETERS; (C) THE EFFECT OF THE PILLAR HEIGHTS; (D) THE EFFECT OF THE BASE LAYER THICKNESS. DOS OF DIFFERENT PARTS ARE PLOTTED IN DIFFERENT COLOR (PILLAR: RED, BASE: BLUE, TOTAL: YELLOW), AND THE GAPS COMPUTED FROM THE DOS'S OF DIFFERENT PARTS ARE ALSO GIVEN IN THEIR RESPECTIVE COLORS.

For the effect of the ***pillar diameters*** shown in Figure 56a, the height and the base layer thickness are kept constant at 7 nm and 1 nm, respectively. The key findings from this result can be summarized as follows:

1. The band gap energy of the pillar part is changed significantly when the pillar diameter is varied. The **smaller** the pillar, the more confinement effect, the **larger the band gap**.
    - The pillar part undergoes a 3-Dimensional confinement resulting in larger effect of the expansion compared to a 2-D confinement observed in the base layer part (in following section)
2. 1-nm, 2-nm, and 3-nm pillar size result in band gap values of 2.64, 1.90, 1.53 eV, respectively, are obtained.
3. The pillar diameter is the **key feature that determine the value of the band gap** of the pillar part.

For the effect of the ***pillar heights*** shown in Figure 56b, the diameter and the base layer thickness are kept constant at 1 nm and 1 nm, respectively. The key findings from the result are:

1. The difference in height **does not significantly** affect the value of band gap. The pillar diameter is still the main key feature to determine the band gap.
2. For 1-nm diameter pillar, E_g is ~2.54 eV **regardless of the height**. The height in this simulation is varied up to 50 nm of pillar, which still keeps the constant value of the band gap.

For the effect of the ***base layer thickness*** shown in Figure 56d, the height and the diameter are kept constant at 7 nm and 1 nm, respectively. The key findings are:

1. The increase of the base layer thickness results **in the reduction of the band gap** of the base layer towards the band gap of crystalline silicon (1.12 eV).
    - The band gap value of each base layer is 1.59 eV, 1.36 eV, and 1.18 eV for 1 nm, 2 nm, 3 nm base layer thickness, respectively.
2. The increase of the base layer thickness also influences of the band gap of pillar.
    - The band gap of the 1-nm pillar is 2.63 eV, 2.52 eV, and 2.40 eV for 1 nm, 2 nm, 3 nm base layer thickness, respectively.

3. The quantum confinement effect of the base layer results from a 2-D confinement. Therefore, the amount of expansion is not as much as the expansion in pillar part where a 3-D confinement effect takes place.

Regarding the effect of the **distance between the pillars**, the height and the base layer thickness are kept at 10 nm and 1 nm, respectively. In this simulation, the pillar diameters are also varied in order to see its effect together with the interpillar distances. The distance is varied by changing the lateral size of the simulation cell; the larger the box size, the more distant the pillars; this also significantly increases the number of atoms as the majority of Si atoms are in the base part of the model, which limits the maximum feasible distance. On the other hand, by decreasing the unit box size of the base layer, the distance between pillar can be reduced until the pillars come in contact. The effect on the band gap energy is shown in Figure 57. The distance, indicated by red arrows in the figures, is defined so as to indicate the size of the silicon feature formed when the pillars touch, in which case the model turns into a crater model.

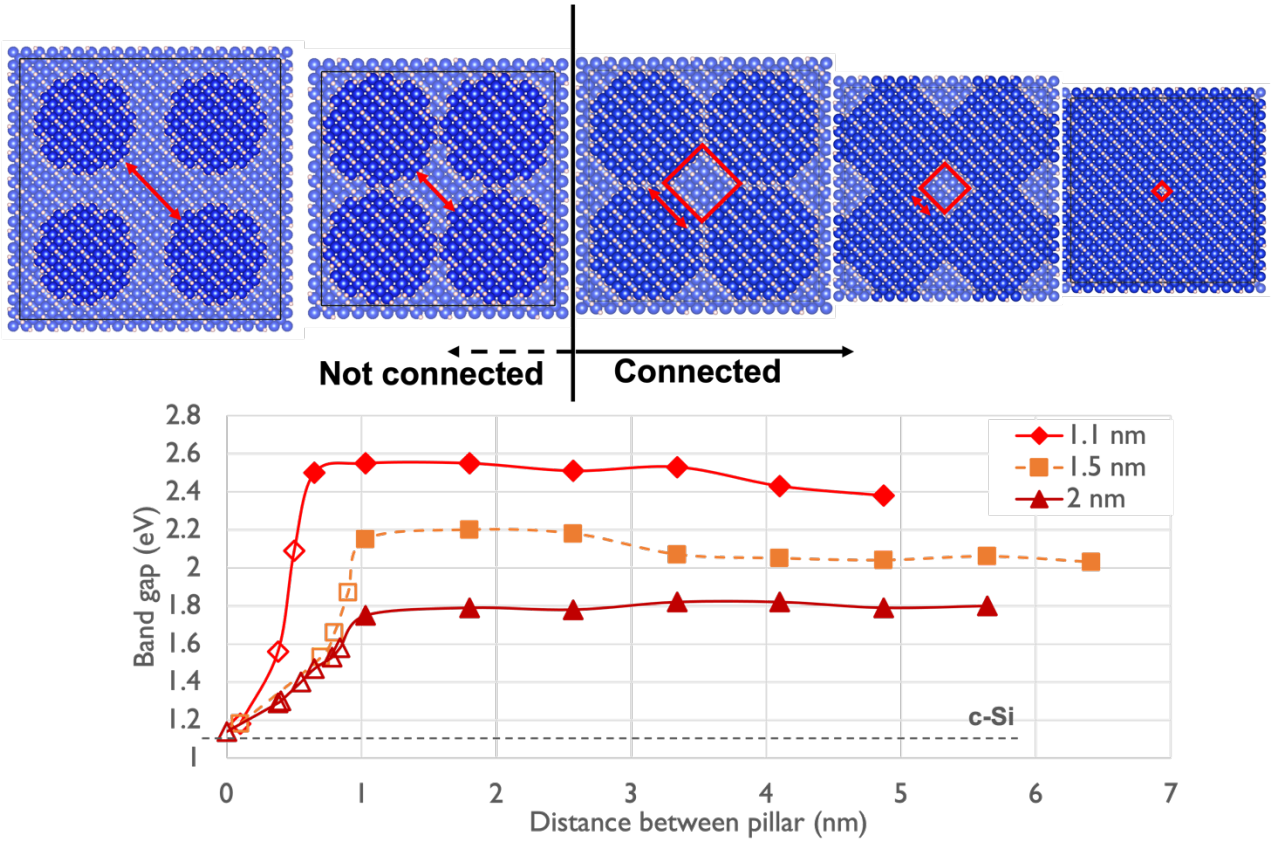


FIGURE 57: EFFECT OF THE DISTANCE BETWEEN THE PILLARS ON THE BAND GAP TOGETHER WITH THE VARIATION OF THE PILLAR DIAMETERS; (TOP) THE PILLAR MODELS SHOWING THE INTERPILLAR DISTANCE (INDICATED WITH RED ARROW). WHEN THESE ARE CONNECTED PHYSICALLY, THE PILLAR TURNS INTO A CRATER MODEL, WHERE THE CONNECTED NEIGHBORING PILLARS FORM A PORE; (BOTTOM) THE BAND GAP VALUES PLOTTED VS THE DISTANCE BETWEEN THE PILLARS, WHERE THE EMPTY SYMBOLS INDICATES THE DATA WHEN PILLARS ARE CONNECTED WHILE THE FILLED SYMBOLS ARE FOR SYSTEMS WHERE PILLARS REMAIN SEPARATED.

From Figure 57, the key findings are:

1. When the pillars are isolated, the **band gap of the pillar part** is determined by the pillar **diameter**.
2. **Only when the pillars touch**, the band gap starts to decrease towards that of the bulk c-Si (1.12 eV). The **more** the pillars merge, the **smaller** the band gap energy.
3. The reverse can be observed in the crater model that decreases its Si wall thickness until it turns into the pillar; the band gap increases significantly after the pillar becomes isolated (explained in next section).

4.4.3 Crater Model

In the previous section, the pillar model is used to study the effect of each feature on the band gap. However, it could be said that the pillar is still not the ideal model that can represent the real porous silicon. To do so, the crater model is generated in order to get closer to the real porous silicon structure, especially the one that is fabricated by anodization process. In this model, 3 crater features are varied: **crater depth**, **crater's thickest wall part, and crater pore diameter**. Figure 58 shows the DOS and the plotted values of the band gap vs. sizes of Si features. In the same manner as pillar model, the effect of each feature is computed while the other features are kept constant. The parameters of the models, including box sizes, numbers of Si and passivating H atoms, crater depth, base layer thickness, crater diameter, inter-pore distances and porosities are listed in in Table S4.

For the first two effects, a similar trend to that observed with the pillar model could be observed. Firstly, for the result of the effect of the **crater depth** is illustrated in Figure 58a, where the Si thickest wall is kept at 1.92 nm and the bottom layer thickness is kept at 1 nm. It can be seen that the depth of the crater does not affect much to the overall band gap in the same way as the height of the pillar model (Figure 56b). By varying the depth of 4, 6, and 10 nm, the band gap of the wall part is 1.60, 1.61, and 1.63 eV, respectively, while the gap of the base part is 1.39, 1.43, and 1.45 eV, respectively. This again verifies that the quantum confinement in the height/depth direction is still governed by the Si wall thickest part, which is 1.92 nm thick in this set of simulations and induces a quantum confinement effect leading to a gap expansion of ~1.6 eV. Next, the result of the effect of the **thickness of the Si "wall" between the craters** is shown in Figure 58b. The definition of the size of the Si feature formed between craters is shown by the red arrow in the figure. In this set of simulations, the bottom layer thickness and the crater depth are kept constant at 1 nm and 2.4 nm, respectively. By changing

the lateral size of the simulation cell, the thickest part of the Si wall part can be varied to 1.92, 2.69, and 3.46 nm.

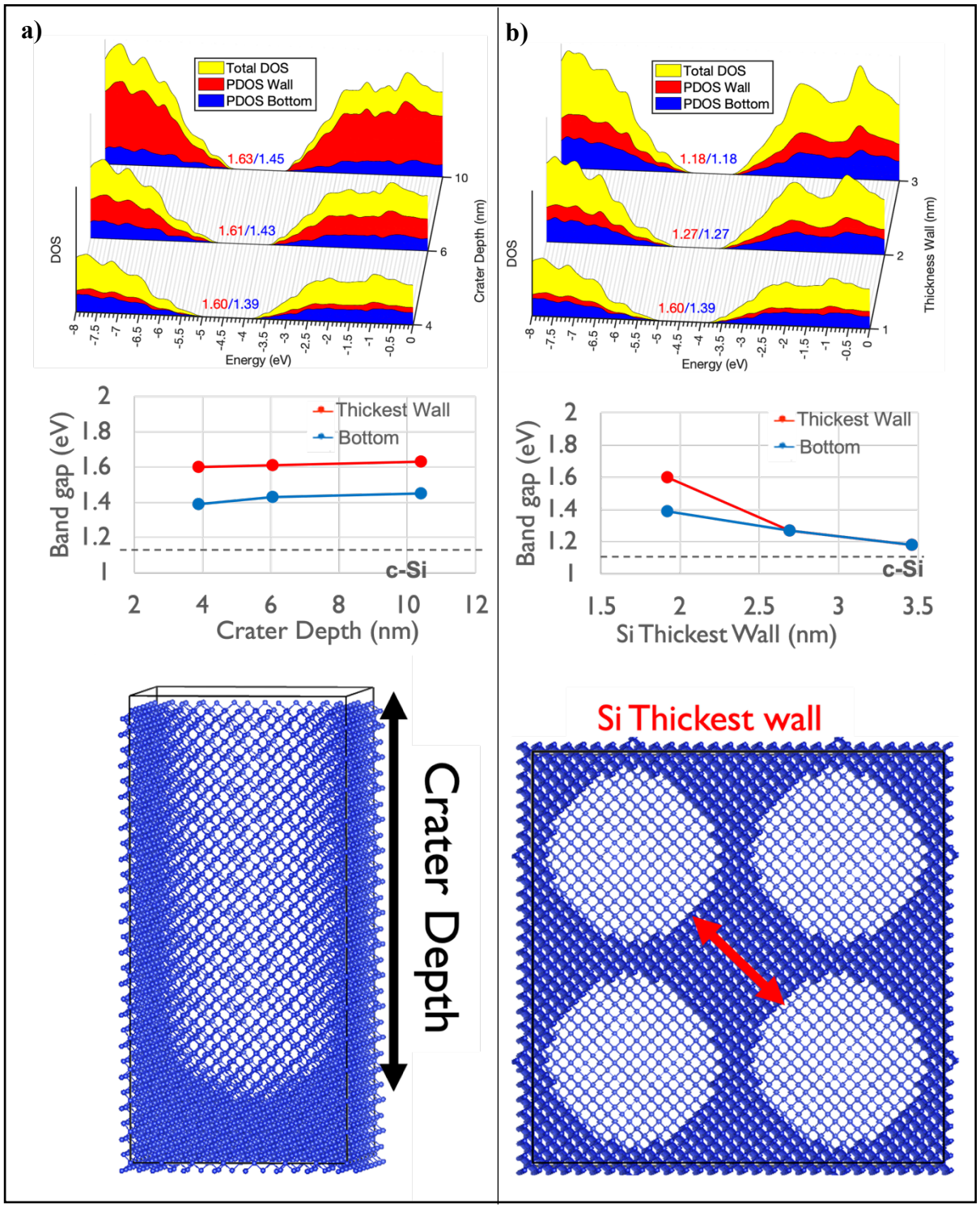


FIGURE 58: EFFECTS OF THE SILICON FEATURES OF THE CRATER MODEL ON THE BAND GAP AND BAND ALIGNMENT; (A) EFFECT OF THE CRATER DEPTH AND (B) EFFECT OF THE THICKNESS OF THE SI WALL. THE SIZE OF THE RESULTING SI FEATURE IS INDICATED BY THE RED ARROW.

From the resulting band gap, it can be clearly seen that as the size the of the Si feature increases, the band gap decreases accordingly. This verifies that it is the size of the Si feature, rather than

the size of the crater, that determines the band gap of the crater model in the same way as the diameter of the pillar is the determinant for the band gap of the pillar model. However, the extent of the band gap expansion is lower than in the pillar model because of the limitation on the geometry of the crater mode. Here, the model is generated by carving a crater into the unit bulk c-Si box with a determined crater diameter. If the crater diameter is too large, the thinnest part of the wall will become disconnected, thus the crater model cannot be called a crater anymore (this will be discussed in the following subsection.) Therefore, when the crater model is still maintained, there are a limitation to the amount of quantum confinement effect. The highest band gap energy obtained is 1.60 eV with a 1.92 nm thick wall. Thickening the crater wall part, the band gap converges to that of the bottom part, which yields the same value of the band gap.

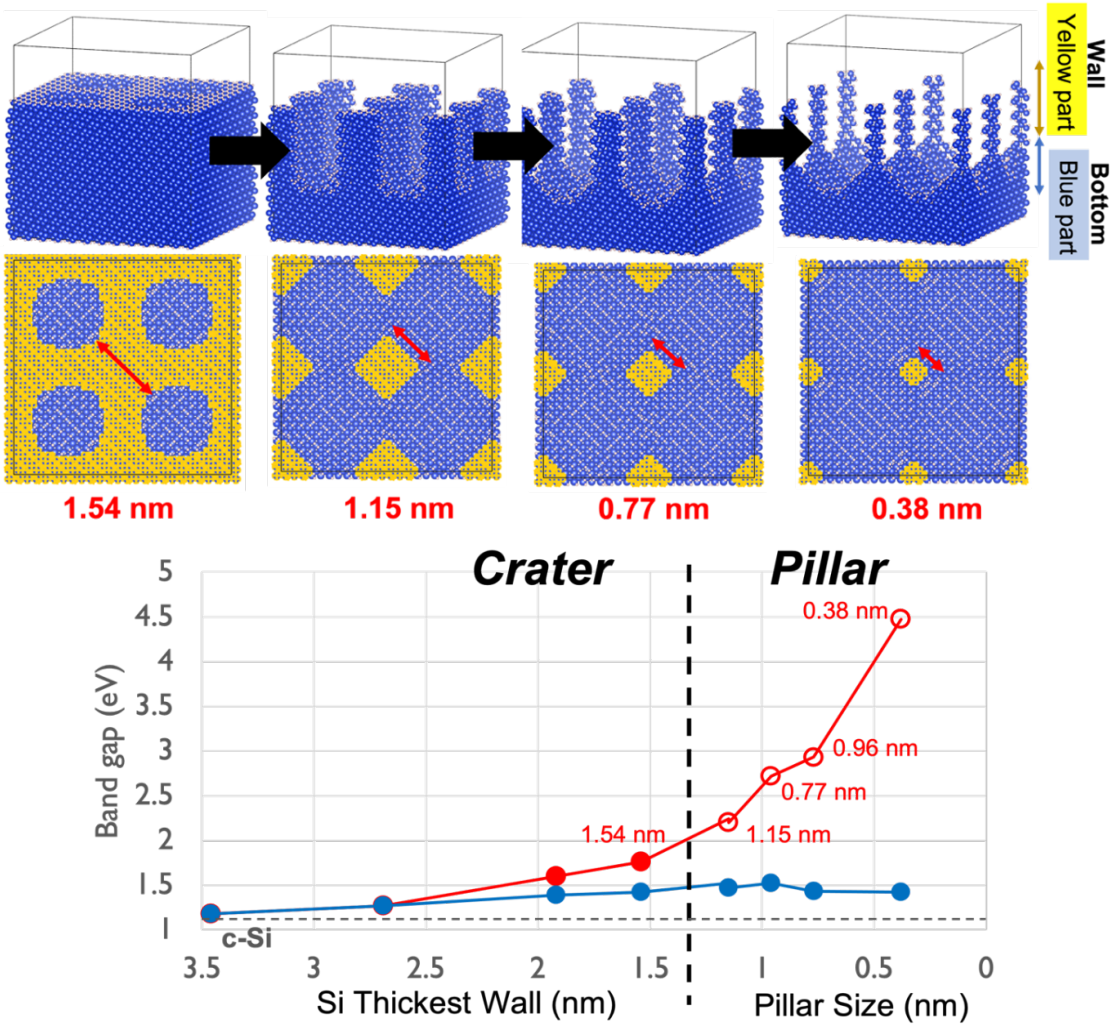


FIGURE 59: THE MODEL SHOWING THE TRANSITION BETWEEN THE CRATER MODEL AND THE PILLAR MODEL WHEN THE SIZE OF THE INTER-CRATER SI FEATURE IS DECREASED BELOW 1.54 NM SO THAT ISOLATED PILLARS ARE FORMED; (TOP) THE STRUCTURES OF THE CRATER MODEL WHERE THE ATOMS HIGHLIGHTED IN YELLOW INDICATES THE SILICON ATOMS BETWEEN THE CRATERS AND THE BLUE ATOMS ARE THE BOTTOM PART; (BOTTOM) THE BAND GAP AS A FUNCTION OF THE SIZE OF THE INTER-CRATER SI FEATURE (BEFORE PILLARS ARE FORMED) AND WITH AN AVERAGE PILLAR DIAMETER (WHEN PILLARS ARE FORMED).

This indicates that harvesting the quantum confinement effect from the crater-like morphology is more challenging than from nano-pillars, as the Si features must be made smaller than 2 nm to obtain the quantum confinement effect.

However, by increasing the crater diameter further, the crater model turns into the pillar model. This can be clearly seen in the Figure 59 where increasing the crater diameter further decreasing the size of the isolated pillar. In this case, the opposite effect of the pillar-turn-crater (Figure 57) is observed. After the pillars are isolated (occurred when the crater thickest wall is decreased below 1.54 nm), the band gap of the wall part increases dramatically, while the bottom part remains the same values of 1.4-1.5 eV. The highest band gap expansion is obtained when the isolated pillar has an average diameter size of 0.38 nm, where the band gap energy is 4.47 eV. This indicates the clear differences between two model: crater and pillar. In the crater model, the confinement effect is not much exerted as there is limit on the smallest Si features that can be obtained while preserving a crater-like morphology, which reduces the extent of the confinement. On the other hand, the pillar model has more confinement in the pillar part, thus the energy band gap can be increased by controlling the size. It is worth noting that the 0.38 nm pillar in this simulation is rather unrealistic.

As the crater model is more likely to be fabricated by anodization process more than the pillar model, this result could inform possible ways of improvement of the fabrication of porous silicon in the future; this will be discussed in the final section of the thesis.

4.4.4 Discussion on the band gap expansion of the experimental part

In order to obtain a significant impact when considering the band gap matching for the top layer of tandem structure, i.e., to have the maximum efficiency surpassing the single junction limitation, the band gap of the top layer must be at least 1.5 eV when matching with the 1.12 eV of the c-Si bottom layer; the best gap value is around 1.7 eV to obtain the 40% theoretical efficiency [13]. From the TEM data in Figure 31, the smallest size of the silicon features at the bottom of the fabricated porous silicon is 3-3.5 nm. Based on the band gaps computed above for different Si morphologies and sizes, the band gap of these Si features is estimated to be in the range of 1.18 – 1.25 eV. This slight band gap expansion is originated from the wall thickness being too thick. With this result, it suggests that the Si “wall” thickness of the fabricated porous silicon in the experimental part is not thin enough for the quantum size effect to take place efficiently which renders its electronic properties to be more like a bulk

silicon. Therefore, with the current structure of the fabricated porous silicon, it is likely that the desired fabrication condition that will result in the porous silicon that has the Si feature size that matched with the underlying bulk c-Si must be re-considered. In order to obtain the higher band gap, the wall thickness must be made smaller than 2 nm.

4.4.5 The DOS of each layer of the model

The band edges (CBM/VBM) calculated from each model are used to evaluate the band alignment, which also can be used to further estimate the other solar cell properties like the built-in voltage, maximum open-circuited voltage etc. Previously, the local DOS is used to calculate the difference between band gap of the pillar and base parts (for the pillar model) and the crater "wall" and the bottom layer parts (for the crater model). In order to further investigate how the band edges are changed at the interface of PSi/c-Si, we consider DOS in successive layers of the structures.

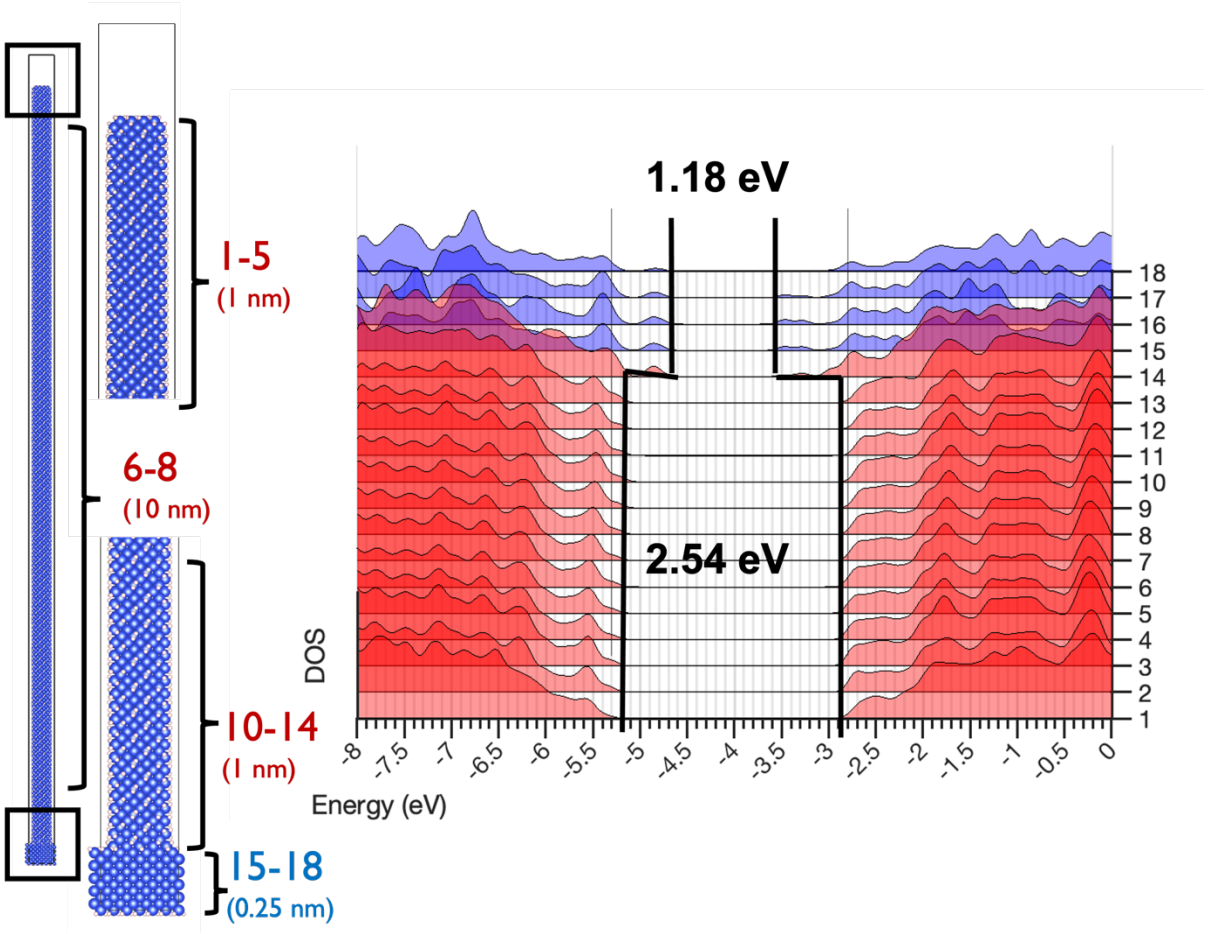


FIGURE 60: THE ANALYSIS OF THE PILLAR MODEL WITH 50-NM HEIGHT CALCULATED BY (LEFT) SEGMENTING EACH LAYER FROM THE SAME MODEL; (TOP RIGHT) THE LOCAL DOS OF EACH SEGMENT (BLUE: BASE LAYER SEGMENTS, RED: PILLAR SEGMENTS. THE THICKNESSES OF THE SEGMENTS ARE INDICATED ON THE LEFT IMAGE). THE MAGNITUDES OF THE DOS PLOTS FOR EACH LAYER ARE MADE SIMILAR FOR EASE OF READING. THE BLACK LINE AND THE NUMBER INDICATE THE BAND EDGES POSITION AND BAND GAP VALUE

Figure 60 shows the result of the band alignment of the pillar model. The features of the model are pillar height of 50 nm, pillar diameter of 1 nm, and base layer thickness of 1 nm. The 18 local DOSs are calculated in each segment of the pillar, where the size of each segments (from the top of pillar) are as follows:

Segment 1-5:	1 nm each	(pillar part)
Segment 6-8:	10 nm each	(pillar part)
Segment 10-14:	1 nm each	(pillar part)
Segment 15-18:	0.25 nm each	(base part)

The blue and red color of the resulting local DOS indicates the pillar and base part, respectively. The key finding from the DOS result are summarized as follows:

1. From the top down to almost the bottom of the pillar (segment 1-13), the difference in height **does not significantly** affect the value of band gap. The pillar diameter is still the main key feature to determine the band gap.
2. There is **no** difference in band gap energy **along the height of pillar**; in this case, ~2.54 eV for 1-nm diameter pillar.
3. Only at the interface between the pillar and the base (segment 14) that the local DOS of the pillar is influenced by the base layer and the band gap immediately drops to the value of base layer (1.18 eV). This affect appears because of the delocalized nature of the orbitals.
4. This kind of drastic change in the band gap at the interface of the adjoined materials (heterostructure) can be considered an **abrupt junction**.

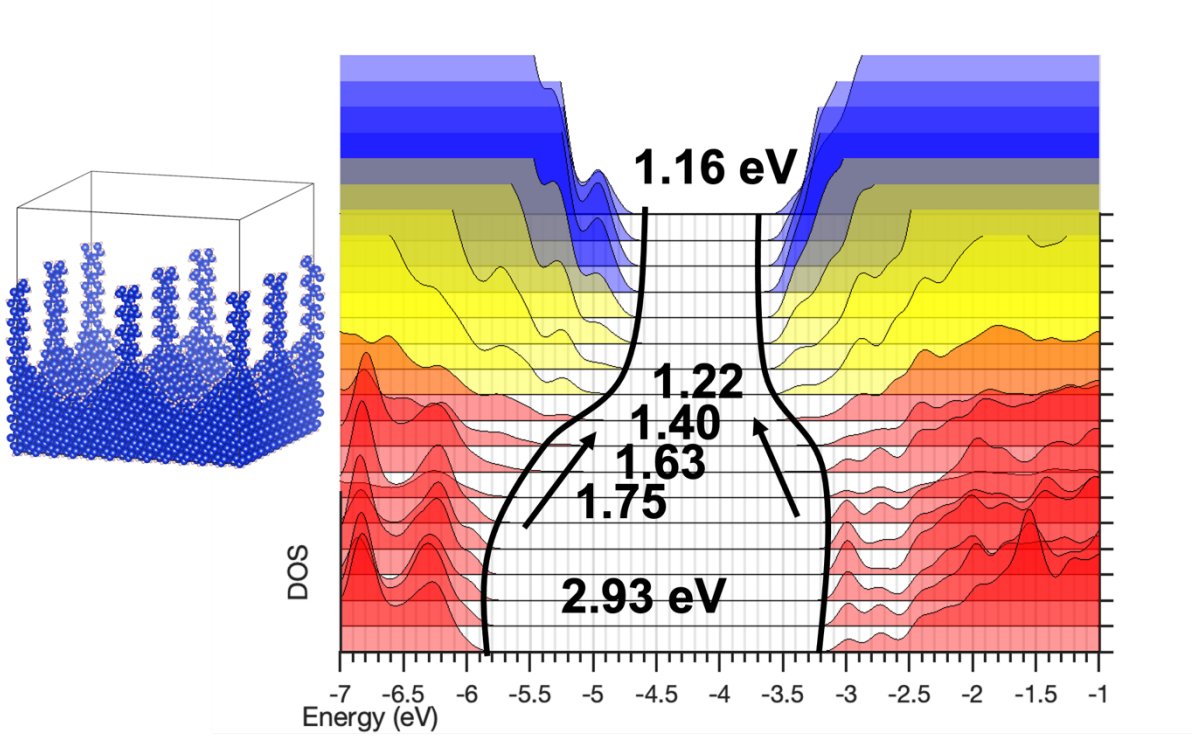


FIGURE 61: THE ANALYSIS OF THE DOS OF THE CRATER MODEL WITH SI PILLARS (SHOWN IN LEFT) CALCULATED BY SEGMENTS; THE BLACK LINE AND THE NUMBER INDICATES THE BAND EDGES POSITION AND BAND GAP VALUE.

Figure 61 shows the result of the band alignment of the crater model where the crater diameter is large enough that Si pillars form. This model is intentionally chosen so that one compares the DOS to the pillar model. In the figure, the red color DOS plots are for the Si pillar part, the yellow color DOS plots are for the bottom of the crater part where the thickness of the Si gradually increases, and the blue color DOS plots are for the base layer part. We observe that the band gap is constant at 2.93 eV along the pillars and starts to decrease in value as the Si feature thickens towards bottom of the crater. In this case, instead of an abrupt junction like in the pillar model in Figure 60, the band gap decreases gradually until it reaches the band gap value of the base layer part (1.16 eV). The band structure formed by this crater model can be considered as a "**graded semiconductors**".

4.4.6 The speculation of the band diagram of PSi/c-Si models

The previous section explains the different band gap on each segment on both pillar and crater model. In order to construct the band diagram with p-n junction for solar cell application, the doping must be assumed. Please note that as the model has a seamless structure, this band diagram is only a speculation that if this was a contact, a charge-depletion region would form.

The assumption of the doping levels are as follows:

Pillar (PSi) 10^{19} cm^{-1} (n-type)

Base (c-Si) 10^{15} cm^{-1} (p-type)

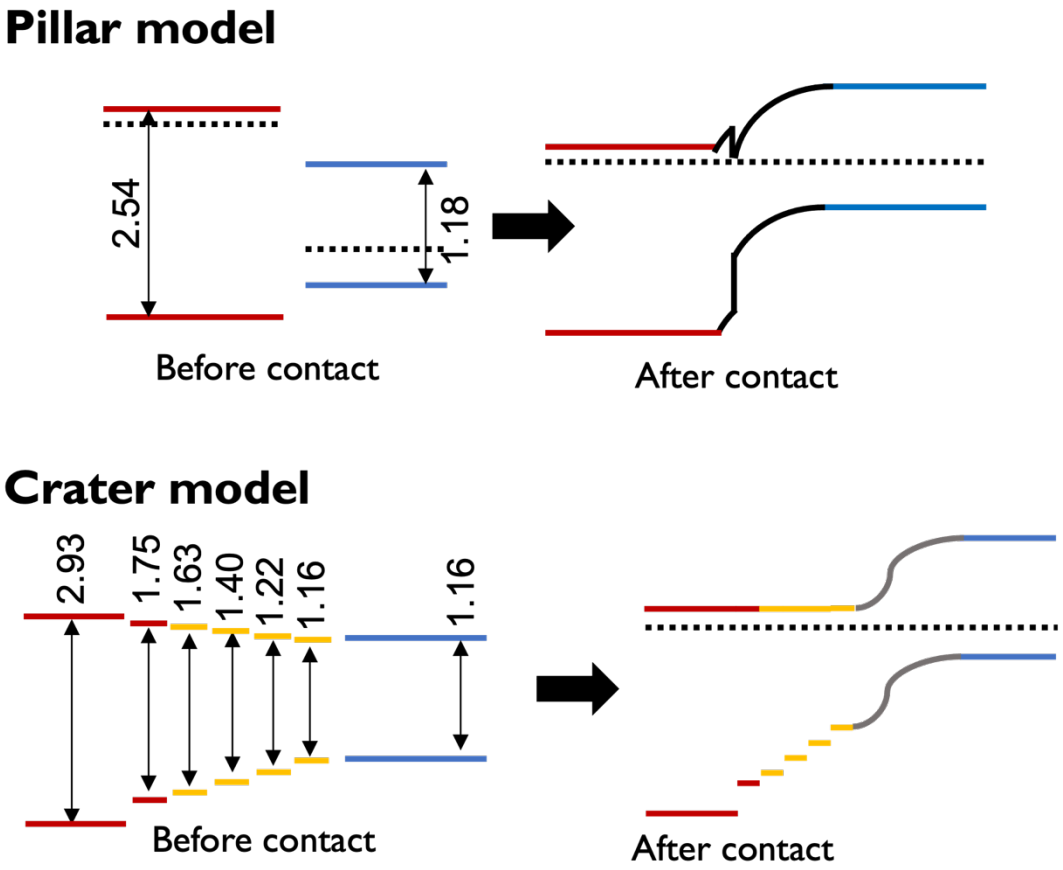


FIGURE 62: BAND DIAGRAM OF (TOP) THE PILLAR MODEL AND (BOTTOM) CRATER MODEL BOTH BEFORE AND AFTER FORMATION OF P-N JUNCTION BASED ON THE STRUCTURE IN FIGURE 60 AND FIGURE 61. THE NUMBER INDICATES THE LOCAL BAND GAP VALUE.

Figure 62 shows the estimation of the band diagram both before and after the formation of p-n junction. For the pillar model, when both doped semiconductors with different band gap are in contact forming an abrupt junction, the band spike and cliff are formed at p-n junction as a result of conduction band and valence band offsets. These spike and cliff are used in some semiconductor applications to control the charge transfer between two material; it can be used to add or reduce the potential barrier of the junction when matching the band offsets properly. In this case, the flow of the holes generated in pillars (n-type) as well as the electrons generated in base layer (p-type) can be transported normally if the charges can arrive at the depletion region. The cliff at the valence band would prevent the diffusion of the hole back to the pillar as the potential barrier in the reverse direction is increased by the cliff. On the other hand, the

diffusion of the electron back to the base layer would be easier compared to the homojunction, as the spike decreases the barrier potential for the reverse current; thus, under illumination, the diffusion current would balance out the drift current at a lower photovoltage (i.e., lower V_{OC}).

For the crater model, assuming that the thickest wall (isolated pillar) part and the bottom part is doped homogeneously with a n-type impurity and with the same amount of doping level as in the pillar model, the band diagram could be constructed as in Figure 62 (bottom), which shows an expected band diagram of n doped pSi in contact with a p-type c-Si. The band bending occurs as usual, but this time, the spike and cliff are smoothed out from the junction as the bottom-most layer before the base layer has very similar band gap as the base layer, i.e., it could be treated as homojunction. The electron transport now is not limited with the lowered potential barrier caused by spike, also the hole transport is enhanced in the area where the band gap is graded as it can transport along the valence band without any help of the PN-junction.

4.4.7 Interconnection between the experimental and simulation part

Based on the experiment and calculation results presented above, we explain the estimated effect of Psi structure on solar cell performance and suggest a fabrication process to achieve the structure with optimal performance.

V_{OC} and the efficiency estimation of the PSi/c-Si structure

As the DFTB parametrization that allows one to compute accurate band structure does not include other species of atom except Si/O/H, the addition of the impurity like boron or phosphorus is not applicable. In order to estimate the V_{OC} and other solar cell performance, many assumptions must be made.

Firstly, the position of the Fermi level of the intrinsic material is assumed to be around the center of the gap of every model. Secondly, as the parameters to calculate the drift and diffusion current are not fully known as well as the light absorption coefficient and the diffusion length of each carrier in PSi layer, the maximum V_{OC} will be calculated based on the built-in potential (V_{bi}) of the junction as is calculated by the following equations:

$$qV_{OC} = qV_{bi} = \frac{\Delta E_C - \Delta E_V}{2} + kTln\frac{N_d N_a}{n_{i,n} n_{i,p}} \quad \text{.....(27)}$$

Where q = elementary charge, ΔE_C = conduction band offset, ΔE_V = valence band offset, k = Boltzmann's constant, T = temperature, N_d = donor carrier concentration, N_a = acceptor carrier concentration, $n_{i,n}$ and $n_{i,p}$ = intrinsic carrier concentration of the n and p-type region, respectively.

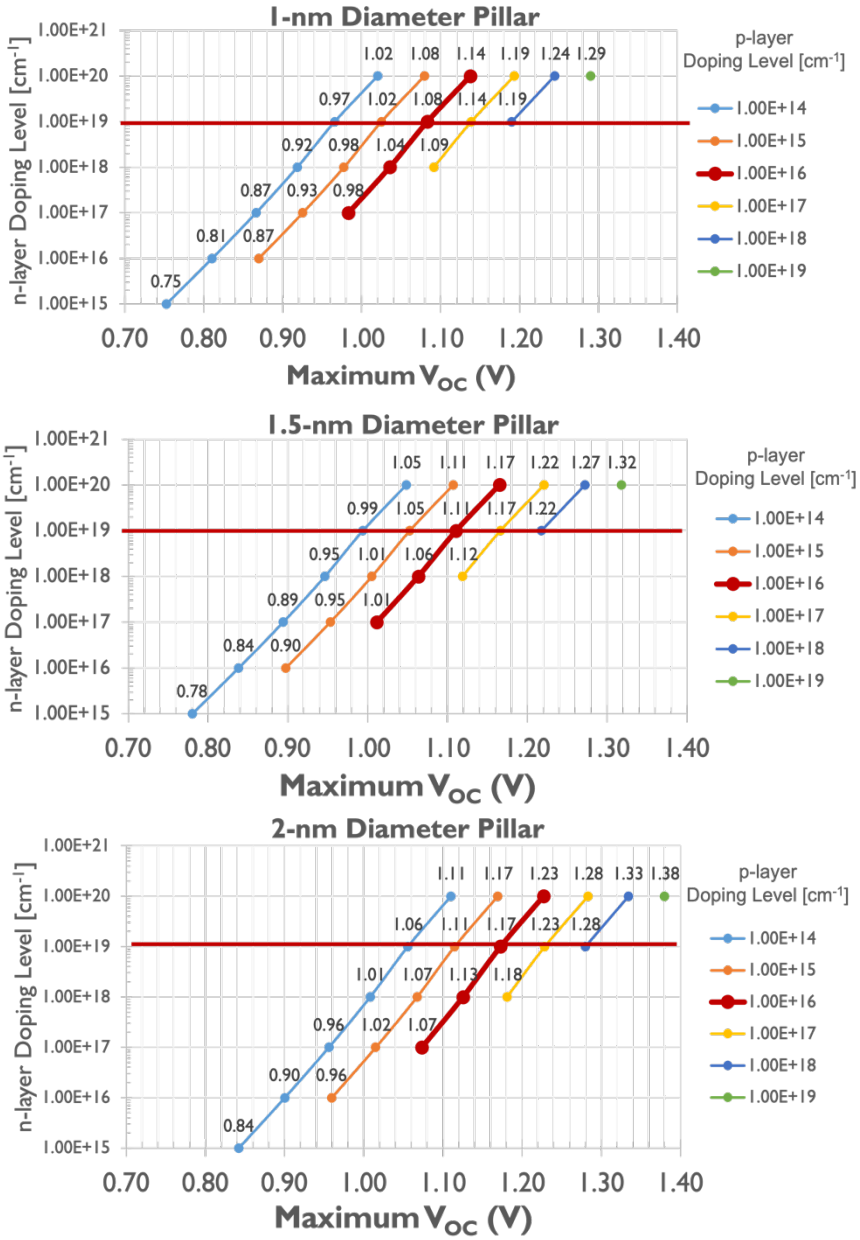


FIGURE 63: MAXIMUM V_{OC} BASED ON THE MAXIMUM BUILT-IN POTENTIAL OF THE PN-JUNCTION OF PILLAR (1, 1.5, 2 NM IN DIAMETER) AS TOP AND C-SI AS BASE PART. THE DOPING DENSITYOF P AND N-TYPE ARE VARIED.

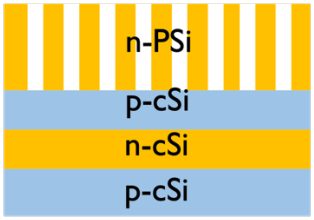
Thirdly, as the inter-model comparison is still not available, the calculated band edges and gap of pillar part of the model will be used as a representative of the top n-type PSi part of

heterostructure, and the calculated band edges and band gap of the whole c-Si model where the ΔE_V term in the equation is minimized will be used as a base p-type layer, so that the maximum V_{OC} of the structure could be obtained without the known information of the band edges between each model. Finally, the resulting V_{OC} of each model will be used to calculate the maximum efficiency of the tandem by stacking on the c-Si-based bottom cell, and assuming the AM 1.5 illumination, the J_{SC} to be maximum theoretically based on the band gap, FF is 0.85, and the efficiency is calculated with the equation 8.

Figure 63 shows the result of the calculated V_{OC} based on various doping level of both p and n-type. It is found that, in this heterostructure, the more degree of quantum confinement effects leading to larger band gap expansion does not always result in the improvement of the V_{OC}. For example, at the n-type doping level of 10^{19} cm^{-1} and p-type doping level of 10^{16} cm^{-1} (where redline intersects with the red dataset), the V_{OC} of the 1-nm diameter pillar with band gap of 2.53 eV is 1.08 V, which is improved from the c-Si homojunction at same doping condition of 0.87 V. However, the 1.5-nm and 2-nm pillar shows a slightly larger amount of V_{OC} of 1.11 V and 1.17 V, respectively, despite having the smaller band gap. This is caused by the valence band offset (ΔE_V) of the pillar and base layer of the 1.5 and 2-nm pillar models being less in value compared to the 1-nm pillar model, which increases the amount of the V_{OC} according to the equation (YY). The rest of the result of V_{OC} follows this trend; it is also the matter of doping that determine the amount of V_{OC}, intuitively. However, not all doping levels can be chosen as the effect of degenerately doping, the band gap narrowing, and the technical issue are also needed to consider (as also discussed in section 4.3.5 in experimental part). Therefore, in order to calculate the solar cell performance, the n-type doping level of 10^{19} cm^{-1} and p-type doping level of 10^{16} cm^{-1} are chosen as a basis as these two values are sensible in term of the amount of built-in potential it can create, and also it is quite common for photovoltaic industry to dope the silicon to these values to fabricate efficient solar cell.

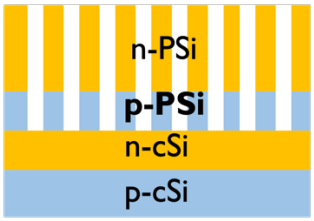
Figure 64 shows the result of the calculation based on the assumptions mentioned before. By using the heterostructure of PSi/c-Si as a top cell of the tandem, the efficiency of 34.7% could be achieved by using 2-nm diameter pillar as top layer of the heterostructure. The efficiency is improved and exceeds the theoretical limitation of the single junction solar cell by fabricating the thin porous silicon heterostructure on top of the base c-Si layer. Also, as expected for the current matching, too large band gap from ultra-small porous silicon features does not help increasing the efficiency of the tandem due to its limited J_{SC}.

Heterostructure on homo-structure



Pillar Diameter	E_g (eV)	V_{OC} (V)	J_{SC} (mA/cm²)	FF	Efficiency (%)
1-nm	2.53	**1.08**	6	0.85	**9.9**
1.5-nm	2.04	**1.11**	14	0.85	**23.5**
2-nm	1.82	**1.17**	20	0.85	**34.7**
c-Si (bottom cell)	1.12	**0.87**	44		

Double Homo-structures



Pillar Diameter	E_g (eV)	V_{OC} (V)	J_{SC} (mA/cm²)	FF	Efficiency (%)
1-nm	2.53	**2.17**	6	0.85	**15.5**
1.5-nm	2.04	**1.74**	14	0.85	**31.0**
2-nm	1.82	**1.53**	20	0.85	**40.8**
c-Si (bottom cell)	1.12	**0.87**	44		

FIGURE 64: MAXIMUM EFFICIENCY AND OTHER SOLAR CELL PARAMETERS CALCULATED FROM THE TANDEM STRUCTURE OF (TOP) THE HETEROSTRUCTURE OF PSI/C-SI AS TOP CELL AND C-SI BOTTOM CELL; (BOTTOM) THE DOUBLE HOMO-STRUCTURES OF PSI TOP CELL AND C-SI BOTTOM CELL.

As a result of the band alignment offset in PSi/c-Si explained earlier, in order to further improve this structure, the double homo-structures where top cell of the tandem is all made of PSi (Figure 64 bottom) might be a next goal of this topic as it would allow the larger value of V_{OC} by the PSi homojunction and can reach the efficiency of 40.8%. However, as explained earlier, the structure wholly made with PSi has a large resistance as well as the recombination rate. It might be interesting that if the thickness of the PSi homojunction could be made thin enough for the light absorption at higher energy light, and the electrochemical passivation can be optimized on the structure, this might create a good opportunity for realizing a full potential of all-silicon tandem solar cell in the future.

Proposal of the fabrication of the porous silicon in the future

Finally, for the last part of the thesis, it would be interesting if some fabrication guideline could be devised according to all of the knowledge gained in this thesis. In order to realize the better fabrication process, it is known from this experimental part that the previous fabrication condition still cannot produce the porous silicon with Si feature size small enough for the quantum confinement effect to take place effectively. Also, from the simulation result and the estimation on the band diagram, it is known that the exceedingly small size would not

result to the improvement of the solar cell efficiency as a result of the improper band alignment as well as the current mismatch. Therefore, there is a sweet spot to fabricate the porous silicon with proper Si feature size, and that would be around 2 nm in size. Starting from this goal, the new fabrication processes are proposed.

The proposed method to fabricate the porous silicon will be based on the anodization (electrochemical etching) for the same reason that this method was initially selected for its low cost, fast process, and the simplicity of the procedure. From the literature review from the introduction part, it is known that the pore size of the porous silicon can be controlled by the current density as well as the HF concentration. Also, as the pore size is made smaller, the silicon features will tend to have a smaller size as well.

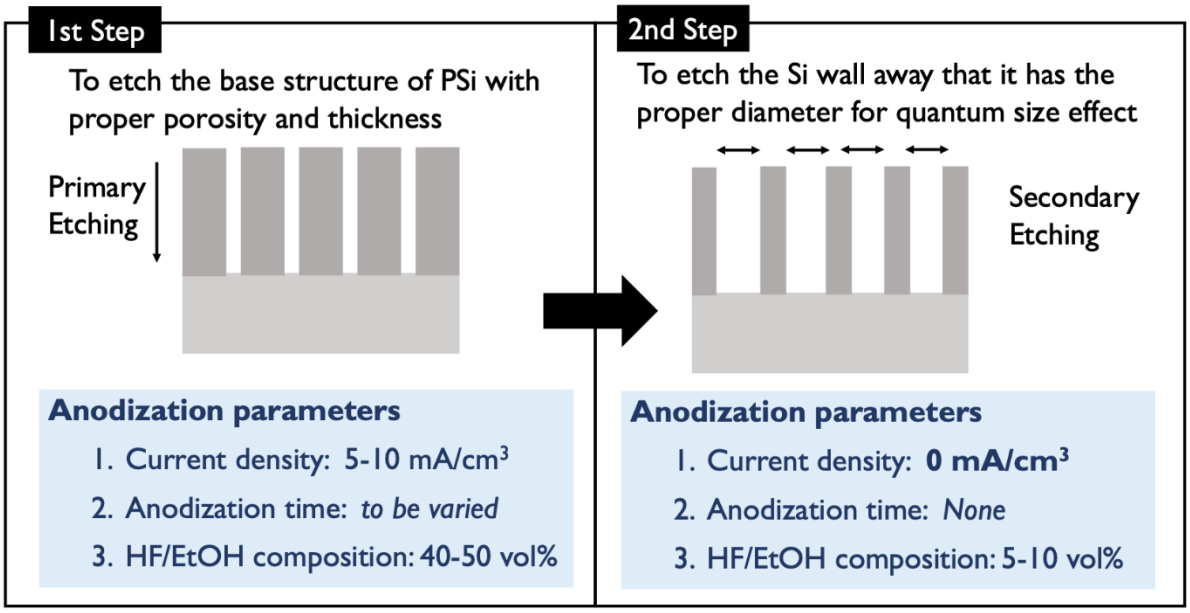


FIGURE 65: THE FIRST PROPOSAL OF THE FABRICATION PROCESS FOR IMPROVEMENT OF THE EFFICIENCY OF POROUS SILICON SOLAR CELL: TWO-STEP ETCHING PROCESS

Figure 65 is the proposal for the first, and simpler, fabrication method. It is composed with 2-step etching: primary etching and secondary etching. The primary etching is the step that etch the doped c-Si wafer to the desired porosity (i.e., pore size or porosity, and rough Si feature size) by controlling the current density to be small, ethanoic HF concentration to be between 40-50%. The microporous structure where the pore size of less than 2 nm and the Si features with size from 2-10 nm can be fabricated. Sequentially, the secondary etching process is then conducted without applying any bias; only leaving the primary-etched wafer in the lower concentration of HF/EtOH of 5-10% so that the HF can spontaneously etches the Si wall in horizontal direction, thus thinning the wall for the proper size (~2 nm).

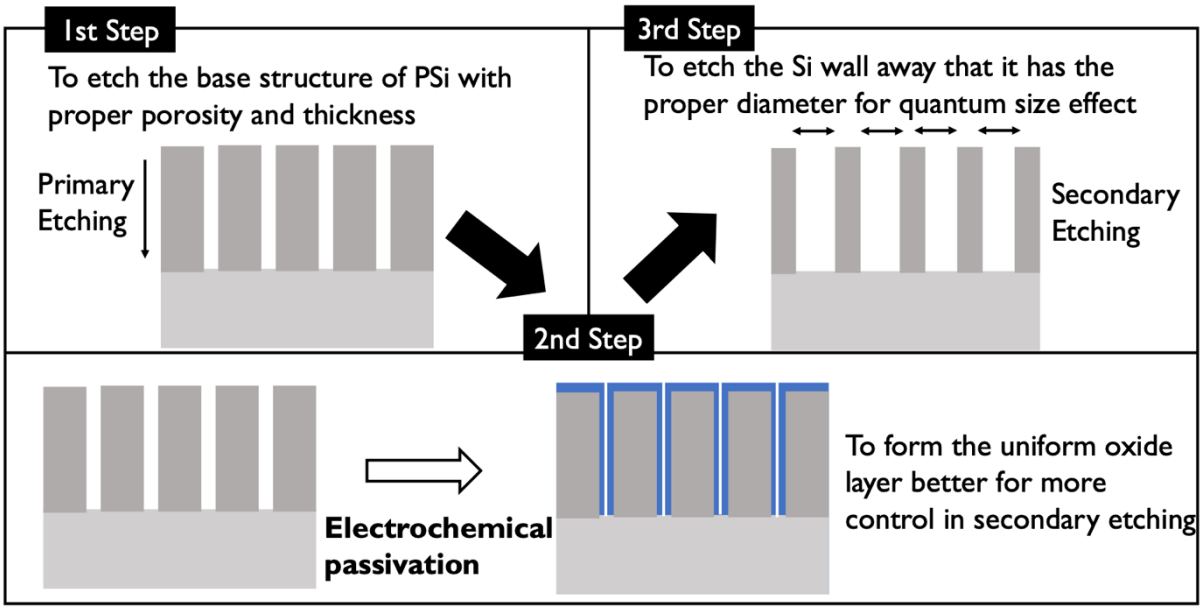


FIGURE 66: THE SECOND PROPOSAL OF THE FABRICATION PROCESS FOR IMPROVEMENT OF THE EFFICIENCY OF POROUS SILICON SOLAR CELL: TWO-STEP ETCHING WITH ELECTROCHEMICAL PASSIVATION FOR BETTER UNIFORMITY OF THE SI FEATURES

Figure 66 proposes another method with one extra step from the one described in Figure 65. In between the primary and secondary etching, this method adds one more step of electrochemical passivation (anodic oxidation) proposed in this thesis. This step is used to create a uniform silicon oxide layer on the top surface of primary-etched porous silicon, where it leaves a large amount of the dangling bonds, which is unstable and ready to react when exposed to atmosphere, thus the uncontrollable native oxide could occur randomly, making the Si feature size uneven. By introducing the electrochemical passivation, the oxide thickness could be formed controllably and uniformly, allowing the 3rd step of secondary etching to etch more uniformly. Therefore, it could lead to an economical and simpler way to fabricate the porous silicon with precise control of its size not only for the photovoltaics purpose, but any applications that needs the quantum confinement effect of this interesting material.

References:

[1] Enerdata, “World Power consumption | Electricity consumption,” *Enerdata*. https://yearbook.enerdata.net/electricity/electricity-domestic-consumption-data.html (accessed May 06, 2022).

[2] Z. Hausfather, “Analysis: Fossil-fuel emissions in 2018 increasing at fastest rate for seven years,” *Carbon Brief*, Dec. 05, 2018. https://www.carbonbrief.org/analysis-fossil-fuel-emissions-in-2018-increasing-at-fastest-rate-for-seven-years (accessed May 06, 2022).

[3] IRENA, “Solar energy,” *IRENA International Renewable Energy Agency*. https://www.irena.org/solar (accessed May 06, 2022).

[4] METI Agency for Natural Resources and Energy, *Energy Basic Plan (エネルギー基本計画) 2014*. Research Institute of Economy, Trade and Industry (Rieti), 2014.

[5] M. Taylor, P. Ralon, and A. Ilas, “The Power to Change: Solar and Wind Cost Reduction Potential to 2025,” IRENA International Renewable Energy Agency, Jun. 2016. [Online]. Available: https://www.irena.org/publications/2016/Jun/The-Power-to-Change-Solar-and-Wind-Cost-Reduction-Potential-to-2025

[6] F. Priolo, T. Gregorkiewicz, M. Galli, and T. F. Krauss, “Silicon nanostructures for photonics and photovoltaics,” *Nat. Nanotechnol.*, vol. 9, no. 1, Art. no. 1, Jan. 2014, doi: 10.1038/nnano.2013.271.

[7] K. Yoshikawa *et al.*, “Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%,” *Nat. Energy*, vol. 2, no. 5, Art. no. 5, Mar. 2017, doi: 10.1038/nenergy.2017.32.

[8] W. Shockley and H. J. Queisser, “Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells,” *J. Appl. Phys.*, vol. 32, no. 3, pp. 510–519, Mar. 1961, doi: 10.1063/1.1736034.

[9] NREL, “Best Research-Cell Efficiency Chart.” https://www.nrel.gov/pv/cell-efficiency.html (accessed May 06, 2022).

[10] Chemistry 310, “Semiconductor p-n Junctions,” in *Book: Introduction to Inorganic Chemistry (Wikibook)*, LibreTexts, 2019. Accessed: May 06, 2022. [Online]. Available: https://chem.libretexts.org/@go/page/183357

[11] K. Yamada and H. Komiyama, *Taiyoko hatsuden kogaku = Photovoltaic engineering: Taiyo denchi no kiso kara shisutemu hyoka made.* Tokyo: Nikkei BPsha ; Nikkei BP shuppan senta (Hatsubai), 2013.

[12] E. Nakazawa and N. Kamata, *Hikari bussei debaisu kogaku no kiso*. 1999.

[13] J. P. Connolly, D. Mencaraglia, C. Renard, and D. Bouchier, “Designing III-V multijunction solar cells on silicon: III-V on silicon multijunction solar cells,” *Prog. Photovolt. Res. Appl.*, vol. 22, no. 7, pp. 810–820, Jul. 2014, doi: 10.1002/pip.2463.

[14] M. Konagai and Y. Ueda, *Solar Cell Technology Handbook (太陽電池技術ハンドブック)*. Tokyo: Omusha, 2013.

[15] X.-M. Zhang, H. Akita, and M. Ihara, “Epitaxial growth of silicon nanowire arrays at wafer-scale using high-speed rotating-disk CVD for improved light-trapping,” *CrystEngComm*, vol. 18, no. 33, pp. 6153–6157, Aug. 2016, doi: 10.1039/C6CE00962J.

[16] E. C. Garnett and P. Yang, “Silicon Nanowire Radial p−n Junction Solar Cells,” *J. Am. Chem. Soc.*, vol. 130, no. 29, pp. 9224–9225, Jul. 2008, doi: 10.1021/ja8032907.

[17] L.-X. Wang, Z.-Q. Zhou, H.-C. Hao, and M. Lu, “A porous Si-emitter crystalline-Si solar cell with 18.97% efficiency,” *Nanotechnology*, vol. 27, no. 42, p. 425207, Sep. 2016, doi: 10.1088/0957-4484/27/42/425207.

[18] A. Lukianov and M. Ihara, “Free-standing epitaxial silicon thin films for solar cells grown on double porous layers of silicon and electrochemically oxidized porous silicon dioxide,” *Thin Solid Films*, vol. 648, pp. 1–7, Feb. 2018, doi: 10.1016/j.tsf.2017.12.025.
[19] X. Hou *et al.*, “Pulsed anodic etching: An effective method of preparing light-emitting porous silicon,” *Appl. Phys. Lett.*, vol. 68, no. 17, pp. 2323–2325, Apr. 1996, doi: 10.1063/1.115845.
[20] E. Garnett and P. Yang, “Light Trapping in Silicon Nanowire Solar Cells,” *Nano Lett.*, vol. 10, no. 3, pp. 1082–1087, Mar. 2010, doi: 10.1021/nl100161z.
[21] M. D. Kelzenberg *et al.*, “Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications,” *Nat. Mater.*, vol. 9, no. 3, Art. no. 3, Mar. 2010, doi: 10.1038/nmat2635.
[22] K. A. Salman, K. Omar, and Z. Hassan, “Effective conversion efficiency enhancement of solar cell using ZnO/PS antireflection coating layers,” *Sol. Energy*, vol. 86, no. 1, pp. 541–547, Jan. 2012, doi: 10.1016/j.solener.2011.10.030.
[23] L. T. Canham, “Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers,” *Appl. Phys. Lett.*, vol. 57, no. 10, pp. 1046–1048, Sep. 1990, doi: 10.1063/1.103561.
[24] T. Dzhafarov, “Silicon Solar Cells with Nanoporous Silicon Layer,” in *Solar Cells—Research and Application Perspectives*, IntechOpen, 2013. doi: 10.5772/51593.
[25] A. Martí and G. L. Araújo, “Limiting efficiencies for photovoltaic energy conversion in multigap systems,” *Sol. Energy Mater. Sol. Cells*, vol. 43, no. 2, pp. 203–222, Sep. 1996, doi: 10.1016/0927-0248(96)00015-3.
[26] L. Canham, Ed., *Handbook of Porous Silicon*. Cham: Springer International Publishing, 2014. doi: 10.1007/978-3-319-05744-6.
[27] K. Omar and K. A. Salman, “Porous Silicon Solar Cell With Anti-Reflection Coating Layer For Efficiency Improved,” *PONTE Int. Sci. Res. J.*, vol. 72, no. 5, 2016, doi: 10.21506/j.ponte.2016.5.32.
[28] A. Prasad, S. Balakrishnan, S. K. Jain, and G. C. Jain, “Porous Silicon Oxide Anti-Reflection Coating for Solar Cells,” *J. Electrochem. Soc.*, vol. 129, no. 3, pp. 596–599, Mar. 1982, doi: 10.1149/1.2123931.
[29] I. Sagnes, A. Halimaoui, G. Vincent, and P. A. Badoz, “Optical absorption evidence of a quantum size effect in porous silicon,” *Appl. Phys. Lett.*, vol. 62, no. 10, pp. 1155–1157, Mar. 1993, doi: 10.1063/1.108773.
[30] J. Bachmann, Ed., *Atomic layer deposition in energy conversion applications*. Weinheim, Germany: Wiley-VCH, 2017.
[31] W. Lu *et al.*, “Effective optimization of surface passivation on porous silicon carbide using atomic layer deposited Al_2O_3,” *RSC Adv.*, vol. 7, no. 14, pp. 8090–8097, 2017, doi: 10.1039/C6RA27281A.
[32] B. Hoex, J. J. H. Gielis, M. C. M. van de Sanden, and W. M. M. Kessels, “On the c-Si surface passivation mechanism by the negative-charge-dielectric Al2O3,” *J. Appl. Phys.*, vol. 104, no. 11, p. 113703, Dec. 2008, doi: 10.1063/1.3021091.
[33] Z. Huang *et al.*, “An effective way to simultaneous realization of excellent optical and electrical performance in large-scale Si nano/microstructures,” *Prog. Photovolt. Res. Appl.*, vol. 23, no. 8, pp. 964–972, May 2014, doi: 10.1002/pip.2506.
[34] Y. Chen, S. Zhong, M. Tan, and W. Shen, “SiO2 passivation layer grown by liquid phase deposition for silicon solar cell application,” *Front. Energy*, vol. 11, no. 1, pp. 52–59, Mar. 2017, doi: 10.1007/s11708-016-0429-3.
[35] N. E. Grant *et al.*, “Anodic oxidations: Excellent process durability and surface passivation for high efficiency silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 203, p. 110155, Dec. 2019, doi: 10.1016/j.solmat.2019.110155.

[36] R. P. Vasquez, R. W. Fathauer, T. George, A. Ksendzov, and T. L. Lin, “Electronic structure of light-emitting porous Si,” *Appl. Phys. Lett.*, vol. 60, no. 8, pp. 1004–1006, Feb. 1992, doi: 10.1063/1.106503.
[37] A. Bsiesy, F. Gaspard, R. Herino, M. Ligeon, F. Muller, and J. C. Oberlin, “Anodic Oxidation of Porous Silicon Layers Formed on Lightly p-Doped Substrates,” *J. Electrochem. Soc.*, vol. 138, no. 11, pp. 3450–3456, Nov. 1991, doi: 10.1149/1.2085432.
[38] H. Chen, X. Hou, G. Li, F. Zhang, M. Yu, and X. Wang, “Passivation of porous silicon by wet thermal oxidation,” *J. Appl. Phys.*, vol. 79, no. 6, pp. 3282–3285, Mar. 1996, doi: 10.1063/1.361226.
[39] G. Li *et al.*, “Passivation of light-emitting porous silicon by rapid thermal treatment in NH3,” *J. Appl. Phys.*, vol. 80, no. 10, pp. 5967–5970, Nov. 1996, doi: 10.1063/1.363593.
[40] S. Y. Chen, Y. H. Huang, H. K. Lai, C. Li, and J. Y. Wang, “Investigation of passivation of porous silicon at room temperature,” *Solid State Commun.*, vol. 142, no. 6, pp. 358–362, May 2007, doi: 10.1016/j.ssc.2007.02.034.
[41] H. G. Shiraz, “Effect of anodization time on photovoltaic properties of nanoporous silicon based solar cells,” *Sustain. Energy Fuels*, vol. 1, no. 3, pp. 652–657, May 2017, doi: 10.1039/C7SE00009J.
[42] L. Khezami, A. Bessadok Jemai, R. Alhathlool, and M. Ben Rabha, “Electronic quality improvement of crystalline silicon by stain etching-based PS nanostructures for solar cells application,” *Sol. Energy*, vol. 129, pp. 38–44, May 2016, doi: 10.1016/j.solener.2016.01.034.
[43] W. J. Aziz, A. Ramizy, K. Ibrahim, Z. Hassan, and K. Omar, “The effect of anti-reflection coating of porous silicon on solar cells efficiency,” *Optik*, vol. 122, no. 16, pp. 1462–1465, Aug. 2011, doi: 10.1016/j.ijleo.2010.08.025.
[44] J. Oh, H.-C. Yuan, and H. M. Branz, “An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures,” *Nat. Nanotechnol.*, vol. 7, no. 11, Art. no. 11, Nov. 2012, doi: 10.1038/nnano.2012.166.
[45] J. J. Patil, B. D. Smith, and J. C. Grossman, “Ultra-high aspect ratio functional nanoporous silicon via nucleated catalysts,” *RSC Adv.*, vol. 7, no. 19, pp. 11537–11542, Feb. 2017, doi: 10.1039/C7RA00562H.
[46] S. Ben Slama, M. Hajji, and H. Ezzaouia, “Crystallization of amorphous silicon thin films deposited by PECVD on nickel-metalized porous silicon,” *Nanoscale Res. Lett.*, vol. 7, no. 1, p. 464, Aug. 2012, doi: 10.1186/1556-276X-7-464.
[47] J. R. Dean, *Applications of Supercritical Fluids in Industrial Analysis*, 1st ed. Springer Dordrecht, 1993.
[48] M. Bouchaour, N. Diaf, A. Ould-Abbas, M. Benosman, L. Merad, and N. Chabane-Sari, “The Role of Supercritical CO2 in the Drying of Porous Silicon,” *undefined*, 2003, Accessed: May 07, 2022. [Online]. Available: https://www.semanticscholar.org/paper/The-Role-of-Supercritical-CO2-in-the-Drying-of-Bouchaour-Diaf/361ddd328417820752d762dac5f5d0c39582199c
[49] L. Jin, E. Kondoh, T. Oya, and B. Gelloz, “Supercritical fluid deposition of copper into mesoporous silicon,” *Thin Solid Films*, vol. 545, pp. 357–360, Oct. 2013, doi: 10.1016/j.tsf.2013.08.034.
[50] Y. B. Melnichenko, H. Mayama, G. Cheng, and T. Blach, “Monitoring Phase Behavior of Sub- and Supercritical CO2 Confined in Porous Fractal Silica with 85% Porosity,” *Langmuir*, vol. 26, no. 9, pp. 6374–6379, May 2010, doi: 10.1021/la904032p.
[51] “Porous Silicon - Wafer Etching on Demand,” *Porous Silicon*. https://www.poroussilicon.com/wafer-etching.html (accessed May 07, 2022).
[52] G. Gautier *et al.*, “Porous Silicon in Microelectronics: From Academic Studies to Industry,” *ECS Trans.*, vol. 69, no. 2, p. 123, Sep. 2015, doi: 10.1149/06902.0123ecst.

[53] M. Boehringer, H. Artmann, and K. Witt, “Porous Silicon in a Semiconductor Manufacturing Environment,” *J. Microelectromechanical Syst.*, vol. 21, no. 6, pp. 1375–1381, Dec. 2012, doi: 10.1109/JMEMS.2012.2205900.
[54] K. Hasegawa, C. Takazawa, M. Fujita, S. Noda, and M. Ihara, “Critical effect of nanometer-size surface roughness of a porous Si seed layer on the defect density of epitaxial Si films for solar cells by rapid vapor deposition,” *CrystEngComm*, vol. 20, no. 13, pp. 1774–1778, Mar. 2018, doi: 10.1039/C7CE02162C.
[55] R. Shibahara, K. Hasegawa, A. Fave, E. Fourmond, S. Noda, and M. Ihara, “Electrical Properties of Monocrystalline Thin Film Si for Solar Cells Fabricated By Rapid Vapor Deposition with Nano-Surface Controlling Double Layer Porous Si in H2,” *ECS Meet. Abstr.*, vol. MA2019-02, no. 39, p. 1787, Sep. 2019, doi: 10.1149/MA2019-02/39/1787.
[56] A. Lukianov, K. Murakami, C. Takazawa, and M. Ihara, “Formation of the seed layers for layer-transfer process silicon solar cells by zone-heating recrystallization of porous silicon structures,” *Appl. Phys. Lett.*, vol. 108, no. 21, p. 213904, May 2016, doi: 10.1063/1.4951671.
[57] H. R. Huff, R. R. Burgess, and E. S. E. Division, *Semiconductor Silicon*. Electrochemical Society, 1973.
[58] T. Ambridge and M. M. Faktor, “An automatic carrier concentration profile plotter using an electrochemical technique,” *J. Appl. Electrochem.*, vol. 5, no. 4, pp. 319–328, Nov. 1975, doi: 10.1007/BF00608796.
[59] C. B. Honsberg and S. G. Bowden, “IV Curve,” *Photovoltaics Education Website*, 2019. https://www.pveducation.org/pvcdrom/solar-cell-operation/iv-curve
[60] C. B. Honsberg and S. G. Bowden, “Current Losses Due to Recombination,” *Photovoltaics Education Website*, 2019. https://www.pveducation.org/pvcdrom/current-losses-due-to-recombination
[61] A. Nishida, K. Nakagawa, H. K. H. Kakibayashi, and T. S. T. Shimada, “Microstructure of Visible Light Emitting Porous Silicon,” *Jpn. J. Appl. Phys.*, vol. 31, no. 9A, p. L1219, Sep. 1992, doi: 10.1143/JJAP.31.L1219.
[62] Q. Cui and M. Elstner, “Density functional tight binding: values of semi-empirical methods in an ab initio era,” *Phys. Chem. Chem. Phys.*, vol. 16, no. 28, pp. 14368–14377, Jun. 2014, doi: 10.1039/C4CP00908H.
[63] W. Li, K. Kotsis, and S. Manzhos, “Comparative density functional theory and density functional tight binding study of arginine and arginine-rich cell penetrating peptide TAT adsorption on anatase TiO2,” *Phys. Chem. Chem. Phys.*, vol. 18, no. 29, pp. 19902–19917, Jul. 2016, doi: 10.1039/C6CP02671K.
[64] S. Markov, B. Aradi, C.-Y. Yam, H. Xie, T. Frauenheim, and G. Chen, “Atomic Level Modeling of Extremely Thin Silicon-on-Insulator MOSFETs Including the Silicon Dioxide: Electronic Structure,” *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 696–704, Mar. 2015, doi: 10.1109/TED.2014.2387288.
[65] D. S. Sholl and J. A. Steckel, *Density Functional Theory: A Practical Introduction | Wiley*. 2009. Accessed: Jun. 29, 2022. [Online]. Available: https://www.wiley.com/en-us/Density+Functional+Theory%3A+A+Practical+Introduction-p-9780470373170
[66] P. Hohenberg and W. Kohn, “Inhomogeneous Electron Gas,” *Phys. Rev.*, vol. 136, no. 3B, pp. B864–B871, Nov. 1964, doi: 10.1103/PhysRev.136.B864.
[67] W. Kohn and L. J. Sham, “Self-Consistent Equations Including Exchange and Correlation Effects,” *Phys. Rev.*, vol. 140, no. 4A, pp. A1133–A1138, Nov. 1965, doi: 10.1103/PhysRev.140.A1133.
[68] P. Giannozzi *et al.*, “QUANTUM ESPRESSO: a modular and open-source software project for quantum simulations of materials,” *J. Phys. Condens. Matter*, vol. 21, no. 39, p. 395502, Sep. 2009, doi: 10.1088/0953-8984/21/39/395502.

[69] P. Giannozzi *et al.*, “Advanced capabilities for materials modelling with Quantum ESPRESSO,” *J. Phys. Condens. Matter*, vol. 29, no. 46, p. 465901, Oct. 2017, doi: 10.1088/1361-648X/aa8f79.
[70] B. Hourahine *et al.*, “DFTB+, a software package for efficient approximate density functional theory based atomistic simulations,” *J. Chem. Phys.*, vol. 152, no. 12, p. 124101, Mar. 2020, doi: 10.1063/1.5143190.
[71] G. Seifert, D. Porezag, and Th. Frauenheim, “Calculations of molecules, clusters, and solids with a simplified LCAO-DFT-LDA scheme,” *Int. J. Quantum Chem.*, vol. 58, no. 2, pp. 185–192, 1996, doi: 10.1002/(SICI)1097-461X(1996)58:2<185::AID-QUA7>3.0.CO;2-U.
[72] D. Porezag, Th. Frauenheim, Th. Köhler, G. Seifert, and R. Kaschner, “Construction of tight-binding-like potentials on the basis of density-functional theory: Application to carbon,” *Phys. Rev. B*, vol. 51, no. 19, pp. 12947–12957, May 1995, doi: 10.1103/PhysRevB.51.12947.
[73] M. Elstner and G. Seifert, “Density functional tight binding,” *Philos. Trans. R. Soc. Math. Phys. Eng. Sci.*, vol. 372, no. 2011, p. 20120483, Mar. 2014, doi: 10.1098/rsta.2012.0483.
[74] M. Elstner, “SCC-DFTB: What Is the Proper Degree of Self-Consistency?,” *J. Phys. Chem. A*, vol. 111, no. 26, pp. 5614–5621, Jul. 2007, doi: 10.1021/jp071338j.
[75] M. Gaus, Q. Cui, and M. Elstner, “DFTB3: Extension of the Self-Consistent-Charge Density-Functional Tight-Binding Method (SCC-DFTB),” *J. Chem. Theory Comput.*, vol. 7, no. 4, pp. 931–948, Apr. 2011, doi: 10.1021/ct100684s.
[76] M. Gaus, A. Goez, and M. Elstner, “Parametrization and Benchmark of DFTB3 for Organic Molecules,” *J. Chem. Theory Comput.*, vol. 9, no. 1, pp. 338–354, Jan. 2013, doi: 10.1021/ct300849w.
[77] A. Sieck, Th. Frauenheim, and K. A. Jackson, “Shape transition of medium-sized neutral silicon clusters,” *Phys. Status Solidi B*, vol. 240, no. 3, pp. 537–548, 2003, doi: 10.1002/pssb.200301886.
[78] C. Köhler, Z. Hajnal, P. Deák, T. Frauenheim, and S. Suhai, “Theoretical investigation of carbon defects and diffusion in \ensuremath{\alpha}-quartz,” *Phys. Rev. B*, vol. 64, no. 8, p. 085333, Aug. 2001, doi: 10.1103/PhysRevB.64.085333.
[79] S. Markov *et al.*, “Permittivity of Oxidized Ultra-Thin Silicon Films From Atomistic Simulations,” *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1076–1078, Oct. 2015, doi: 10.1109/LED.2015.2465850.
[80] J. D. Gale and A. L. Rohl, “The General Utility Lattice Program (GULP),” *Mol. Simul.*, vol. 29, no. 5, pp. 291–341, May 2003, doi: 10.1080/0892702031000104887.
[81] S. Tsuneyuki, M. Tsukada, H. Aoki, and Y. Matsui, “First-Principles Interatomic Potential of Silica Applied to Molecular Dynamics,” *Phys. Rev. Lett.*, vol. 61, no. 7, pp. 869–872, Aug. 1988, doi: 10.1103/PhysRevLett.61.869.
[82] J. Tersoff, “Empirical interatomic potential for silicon with improved elastic properties,” *Phys. Rev. B*, vol. 38, no. 14, pp. 9902–9905, Nov. 1988, doi: 10.1103/PhysRevB.38.9902.
[83] F. de Brito Mota, J. F. Justo, and A. Fazzio, “Hydrogen role on the properties of amorphous silicon nitride,” *J. Appl. Phys.*, vol. 86, no. 4, pp. 1843–1847, Aug. 1999, doi: 10.1063/1.370977.
[84] A. Yasukawa, “Using An Extended Tersoff Interatomic Potential to Analyze The Static-Fatigue Strength of SiO₂ under Atmospheric Influence,” *JSME Int. J. Ser Mech. Mater. Eng.*, vol. 39, no. 3, pp. 313–320, 1996, doi: 10.1299/jsmea1993.39.3_313.

[85] J. Zemann, “Crystal structures, 2nd edition. Vol. 1 by R. W. G. Wyckoff,” *Acta Crystallogr.*, vol. 18, no. 1, pp. 139–139, 1965, doi: 10.1107/S0365110X65000361.
[86] K. McIntosh, M. Abbott, and B. Sudbury, “Resistivity calculator,” *PV Lighthouse*, Jun. 2011. https://www.pvlighthouse.com.au/resistivity (accessed May 07, 2022).
[87] M. I. J. Beale, J. D. Benjamin, M. J. Uren, N. G. Chew, and A. G. Cullis, “An experimental and theoretical study of the formation and microstructure of porous silicon,” *J. Cryst. Growth*, vol. 73, no. 3, pp. 622–636, Dec. 1985, doi: 10.1016/0022-0248(85)90029-6.
[88] D. a. G. Bruggeman, “Calculation of Various Physics Constants in Heterogeneous Substances I Dielectricity Constants and Conductivity of Mixed Bodies from Isotropic Substances,” *Ann. Phys.*, vol. 416, no. 8, pp. 665–679, 1935, doi: 10.1002/andp.19354160802.
[89] P. Würfel, *Physics of Solar Cells From Principles to New Concepts*. 2008. Accessed: May 07, 2022. [Online]. Available: https://nbn-resolving.org/urn:nbn:de:101:1-201408162007
[90] R. Brunner, E. Pinčík, M. Kučera, J. Greguš, P. Vojtek, and Z. Zábudlá, “Temperature dependence of photoluminescence peaks of porous silicon structures,” *J. Electr. Eng.*, vol. 68, no. 7, pp. 78–80, Dec. 2017, doi: 10.1515/jee-2017-0062.
[91] J. C. Vial *et al.*, “Mechanisms of visible-light emission from electro-oxidized porous silicon,” *Phys. Rev. B*, vol. 45, no. 24, pp. 14171–14176, Jun. 1992, doi: 10.1103/PhysRevB.45.14171.
[92] T. Ito, T. O. T. Ohta, and A. H. A. Hiraki, “Light Emission from Microcrystalline Si Confined in SiO2 Matrix through Partial Oxidation of Anodized Porous Silicon,” *Jpn. J. Appl. Phys.*, vol. 31, no. 1A, p. L1, Jan. 1992, doi: 10.1143/JJAP.31.L1.
[93] F. Koch, V. Petrova-Koch, T. Muschik, A. Nikolov, and V. Gavrilenko, “Some Perspectives on the Luminescence Mechanism Via Surface-Confined States of Porous Si,” *MRS Online Proc. Libr. OPL*, vol. 283, ed 1992, doi: 10.1557/PROC-283-197.
[94] A. Takazawa, T. Tamura, and M. Yamada, “Photoluminescence mechanisms of porous Si oxidized by dry oxygen,” *J. Appl. Phys.*, vol. 75, no. 5, pp. 2489–2495, Mar. 1994, doi: 10.1063/1.356247.
[95] M. S. Brandt, H. D. Fuchs, M. Stutzmann, J. Weber, and M. Cardona, “The origin of visible luminescencefrom ‘porous silicon’: A new interpretation,” *Solid State Commun.*, vol. 81, no. 4, pp. 307–312, Jan. 1992, doi: 10.1016/0038-1098(92)90815-Q.
[96] Y. Takeda, S. Hyodo, N. Suzuki, T. Motohiro, T. Hioki, and S. Noda, “An oligosilane bridge model for the origin of the intense visible photoluminescence of porous silicon,” *J. Appl. Phys.*, vol. 73, no. 4, pp. 1924–1928, Feb. 1993, doi: 10.1063/1.353182.
[97] S. M. Prokes, O. J. Glembocki, V. M. Bermudez, R. Kaplan, L. E. Friedersdorf, and P. C. Searson, “SiH2 excitation: An alternate mechanism for porous Si photoluminescence,” *Phys. Rev. B*, vol. 45, no. 23, pp. 13788–13791, Jun. 1992, doi: 10.1103/PhysRevB.45.13788.
[98] V. Petrova-Koch, T. Muschik, A. Kux, B. K. Meyer, F. Koch, and V. Lehmann, “Rapid-thermal-oxidized porous Si−The superior photoluminescent Si,” *Appl. Phys. Lett.*, vol. 61, no. 8, pp. 943–945, Aug. 1992, doi: 10.1063/1.107736.
[99] A. G. Cullis, L. T. Canham, and P. D. J. Calcott, “The structural and luminescence properties of porous silicon,” *J. Appl. Phys.*, vol. 82, no. 3, pp. 909–965, Aug. 1997, doi: 10.1063/1.366536.
[100] M. Lipiński, P. Panek, Z. Świątek, E. Bełtowska, and R. Ciach, “Double porous silicon layer on multi-crystalline Si for photovoltaic application,” *Sol. Energy Mater. Sol. Cells*, vol. 72, no. 1, pp. 271–276, Apr. 2002, doi: 10.1016/S0927-0248(01)00174-X.

[101] M. Lipinski, P. Panek, E. Bełtowska, and H. Czternastek, “Reduction of surface reflectivity by using double porous silicon layers,” *Mater. Sci. Eng. B*, vol. 101, no. 1, pp. 297–299, Aug. 2003, doi: 10.1016/S0921-5107(02)00720-1.
[102] V. Y. Yerokhov *et al.*, “Cost-effective methods of texturing for silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 72, no. 1, pp. 291–298, Apr. 2002, doi: 10.1016/S0927-0248(01)00177-5.
[103] Nihon kagakukai and yasuhiro Iwasawa, *Kagaku benran.* 2004.
[104] H. Komiyama, *Sokudoron.* Tokyo: Asakura Shoten, 1990.
[105] K. Murakami, Tokyo Institute of Technology, Tokyo, Japan, 2016.
[106] H. C. M. Knoops, S. E. Potts, A. A. Bol, and W. M. M. Kessels, “Atomic layer deposition,” in *Handbook of crystal growth : thin films and epitaxy (second edition)*, T. Kuech, Ed. Elsevier, 2015, pp. 1101–1134. doi: 10.1016/B978-0-444-63304-0.00027-5.
[107] O. Breitenstein, J. P. Rakotoniaina, M. H. Al Rifai, and M. Werner, “Shunt types in crystalline silicon solar cells,” *Prog. Photovolt. Res. Appl.*, vol. 12, no. 7, pp. 529–538, 2004, doi: 10.1002/pip.544.
[108] A. Cuevas and R. A. Sinton, “Prediction of the open-circuit voltage of solar cells from the steady-state photoconductance,” *Prog. Photovolt. Res. Appl.*, vol. 5, no. 2, pp. 79–90, 1997, doi: 10.1002/(SICI)1099-159X(199703/04)5:2<79::AID-PIP155>3.0.CO;2-J.
[109] H. Takato, I. Sakata, and R. Shimokawa, “Surface Passivation Effect of Silicon Substrates due to Quinhydrone/Ethanol Treatment,” *Jpn. J. Appl. Phys.*, vol. 40, no. 10A, p. L1003, Oct. 2001, doi: 10.1143/JJAP.40.L1003.
[110] H. Takato, I. Sakata, and R. Shimokawa, “Quinhydrone/Methanol Treatment for the Measurement of Carrier Lifetime in Silicon Substrates,” *Jpn. J. Appl. Phys.*, vol. 41, no. 8A, p. L870, Aug. 2002, doi: 10.1143/JJAP.41.L870.
[111] J. Wagner and J. A. del Alamo, “Band-gap narrowing in heavily doped silicon: A comparison of optical and electrical data,” *J. Appl. Phys.*, vol. 63, no. 2, pp. 425–429, Jan. 1988, doi: 10.1063/1.340257.
[112] S. C. Jain and D. J. Roulston, “A simple expression for band gap narrowing (BGN) in heavily doped Si, Ge, GaAs and GexSi1−x strained layers,” *Solid-State Electron.*, vol. 34, no. 5, pp. 453–465, May 1991, doi: 10.1016/0038-1101(91)90149-S.
[113] R. Hoenig, M. Glatthaar, F. Clement, J. Greulich, J. Wilde, and D. Biro, “New measurement method for the investigation of space charge region recombination losses induced by the metallization of silicon solar cells,” *Energy Procedia*, vol. 8, pp. 694–699, Jan. 2011, doi: 10.1016/j.egypro.2011.06.203.
[114] M. Jeong *et al.*, “Correlation between the open-circuit voltage and recombination loss at metal-silicon interfaces of crystalline silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 210, p. 110519, Jun. 2020, doi: 10.1016/j.solmat.2020.110519.
[115] H. Hannebauer, M. Sommerfeld, J. Müller, T. Dullweber, and R. Brendel, “Analysis of the Emitter Saturation Current Density of Industrial Type Silver Screen-Printed Front Contacts,” *Proc 27th Eur Photovolt. Sol Energy Conf Exhib*, pp. 1360–1363, Jan. 2012, doi: 10.4229/27thEUPVSEC2012-2BV.5.10.
[116] J. Müller, K. Bothe, S. Gatz, F. Haase, C. Mader, and R. Brendel, “Recombination at laser-processed local base contacts by dynamic infrared lifetime mapping,” *J. Appl. Phys.*, vol. 108, no. 12, p. 124513, Dec. 2010, doi: 10.1063/1.3517109.
[117] P. N. Vinod, “Specific contact resistance and carrier tunneling properties of the silver metal/porous silicon/p-Si ohmic contact structure,” *J. Alloys Compd.*, vol. 470, no. 1, pp. 393–396, Feb. 2009, doi: 10.1016/j.jallcom.2008.02.110.
[118] M. Hörteis, T. Gutberlet, A. Reller, and S. W. Glunz, “High-Temperature Contact Formation on n-Type Silicon: Basic Reactions and Contact Model for Seed-Layer

Contacts," *Adv. Funct. Mater.*, vol. 20, no. 3, pp. 476–484, 2010, doi: 10.1002/adfm.200901305.
[119] C. Palsule, S. Liu, S. Gangopadhyay, M. Holtz, D. Lamp, and M. Kristiansen, "Electrical and optical characterization of crystalline silicon/porous silicon heterojunctions," *Sol. Energy Mater. Sol. Cells*, vol. 46, no. 4, pp. 261–269, Jul. 1997, doi: 10.1016/S0927-0248(97)00004-4.
[120] G. Smestad, M. Kunst, and C. Vial, "Photovoltaic response in electrochemically prepared photoluminescent porous silicon," *Sol. Energy Mater. Sol. Cells*, vol. 26, no. 4, pp. 277–283, May 1992, doi: 10.1016/0927-0248(92)90047-S.
[121] M. Rajabi and R. S. Dariani, "Current improvement of porous silicon photovoltaic devices by using double layer porous silicon structure: applicable in porous silicon solar cells," *J. Porous Mater.*, vol. 5, no. 16, pp. 513–519, 2009, doi: 10.1007/s10934-008-9226-7.
[122] R. Mentek, B. Gelloz, and N. Koshida, "Photovoltaic Property of Wide-Gap Nanocrystalline Silicon Layers," *Jpn. J. Appl. Phys.*, vol. 51, no. 2S, p. 02BP05, Feb. 2012, doi: 10.1143/JJAP.51.02BP05.
[123] R. Mentek, D. Hippo, B. Gelloz, and N. Koshida, "Photovoltaic effect with high open circuit voltage observed in electrochemically prepared nanocrystalline silicon membranes," *Mater. Sci. Eng. B*, vol. 190, pp. 33–40, Dec. 2014, doi: 10.1016/j.mseb.2014.09.005.
[124] N. Koshida *et al.*, "Optical characterization of porous silicon by synchrotron radiation reflectance spectra analyses," *Appl. Phys. Lett.*, vol. 63, no. 20, pp. 2774–2776, Nov. 1993, doi: 10.1063/1.110330.
[125] D. Kovalev, G. Polisski, M. Ben-Chorin, J. Diener, and F. Koch, "The temperature dependence of the absorption coefficient of porous silicon," *J. Appl. Phys.*, vol. 80, no. 10, pp. 5978–5983, Nov. 1996, doi: 10.1063/1.363595.
[126] M. Nolan, S. O'Callaghan, G. Fagas, J. C. Greer, and T. Frauenheim, "Silicon Nanowire Band Gap Modification," *Nano Lett.*, vol. 7, no. 1, pp. 34–38, Jan. 2007, doi: 10.1021/nl061888d.
[127] F. Sacconi *et al.*, "Electronic and transport properties of silicon nanowires," *J. Comput. Electron.*, vol. 6, no. 1, pp. 329–333, Sep. 2007, doi: 10.1007/s10825-006-0138-y.
[128] X. Wu and Y. Tang, "Study on band structure of nanoporous silicon thin films," *Surf. Rev. Lett.*, vol. 25, no. 01, p. 1850045, Jan. 2018, doi: 10.1142/S0218625X18500452.

CHAPTER 5: SUMMARY OF DOCTORAL DISSERTATION

All-silicon tandem solar cell is one specific type of multi-junction solar cell, which has the potential to surpass the theoretical efficiency limit of single-junction silicon solar cell; it also eliminates the lattice mismatch issue found in hetero-junction structure, and also reduce the use of rare metal and toxic material. The porous silicon is selected as a candidate of a top cell due to its adjustable band gap, which is reported to be ranged from 1.4 – 2.2 eV depending on its porous structure. Many literatures suggests that the origin of its wider band gap comes from the quantum confinement effect. The porous silicon also has an anti-reflective property, which leads to the enhancement of light absorption. With these benefits, it provides the opportunity to use the porous silicon to improve the V_{OC}, J_{SC}, as well as the efficiency of the solar cell. However, the surface area and defects are highly increased compared to crystalline silicon, which inevitably increases the rate of recombination on the surface. Therefore, a passivation method that is suitable for the nano-structure material is necessary to reduce surface recombination. The representative and common method to passivate silicon solar cell is atomic layer deposition (ALD). However, the cost of ALD is too high to be widely used in commercial scale. In this research, a low-cost electrochemical passivation technique has been developed to achieve a uniform passivated layer on porous silicon. Together with the experimental part, we also use the simulation approach to calculate the result that is difficult to obtain experimentally. In this part, we computed and compared band structures induced by amorphization and porosity of silicon by the DFTB level.

The analysis of ECV data as well as the TEM image confirms the position of P-N junction to be around 200 nm deep from the surface, which is then used to determine the thickness of porous layer. In order to make use of the quantum size effect, the porous layer needs to exceed the P-N junction and lies within the P-type silicon, unless it would only act as an anti-reflective film. Then the porous silicon with porous layer thickness of 200-250 nm was fabricated through anodization process in HF solution with the current density is controlled at 75 mA/cm^2 for 6 seconds. Furthermore, the cross-sectional view of the microstructure confirms a lattice matching between the PS/*c*-Si interface. The lowest reflectivity of approximately 5% was achieved for this thin porous silicon at a wavelength of 450 and 1000 nm, compared to 30% at 700-1000 nm. This highlights the potential porous layer as an anti-reflection coating structure in Si solar cells. However, even though the PL data of the porous silicon shows the

peak at 645 nm, which is equivalent to the energy of 1.92 eV, the absorbance data from UV-Vis does not show the difference in optical band edge compared to the c-Si sample. This suggests that there might be a band gap expansion, but its influence is overwhelmed by the underlying thick c-Si base wafer.

Then the porous silicon is passivated by three methods of passivation: ALD (Al_2O_3), electrochemical passivation in HCl with current density of 0.1012 mA/cm^2, and supercritical passivation with N_2 with CO_2 as a carrier. The result of carrier lifetime shows that there are no obvious improvements nor differences from each passivation method; all of the lifetime is too short (in few microseconds range) compared to commercialized solar cell (in millisecond range). The longest carrier lifetime result is from ALD-passivated sample with 20 nm Al_2O_3 thickness and post-anneal at 400°C for 20 minutes, which is 8.12 μs

After the fabrication of the solar cell by electrode deposition, the PV performances of electrochemical passivated and ALD-passivated samples are measured. In ALD passivation, all of the solar cell parameters are poor, as well as diode characteristics. This is believed that the Al_2O_3 layer forms a resistive layer on the top part of the solar cell, which drastically increases the series resistance. Then the electrochemical passivation with many reaction times as a variable were measured. The result shows that bottom-up anodization process successfully produced a uniform SiO_2 passivation layer with high coverage on high aspect-ratio porous silicon layers. A maximum efficiency of 10.7% with the best *J-V* behavior yielded *FF* of 0.685 for the porous silicon solar cell at an optimized passivation time *t* of 30 s (PS-e cell). Simultaneously, this porous silicon cell had the lowest R_S (2.79 Ω cm^{-1}) and also had the highest R_{SH} (3.45 kΩ cm^{-1}). This result shows that even though the carrier lifetime is relatively short, the electrochemical passivated samples still can yield a good efficiency when operated as a solar cell and the electrochemical passivation is a better method to passivate the porous silicon structure fabricated in this experiment. Furthermore, such improved PV parameters confirm that the anodic SiO_2 provides a sufficient passivation approach, especially for nano-structured porous silicon solar cell. However, the notable enhancement in EQE in the wavelength range of 700 to 1100 nm improves the light-trapping at long wavelength, and thus provides a promising possibility for improving the light absorption in thin-film Si solar cells. In term of the practical use, the electrochemical passivation at room temperature can be performed as a surface passivation technique for other nanostructured materials because the thickness of the oxidized layer can be precisely controlled by adjusting the combination of current density and treatment period while maintaining the original nanostructure.

However, there is no improvement in the V_{OC} as all of the result remain in the range of 0.51-0.53 V. The detailed characterization by QSSPC suggests that the excessively highly doped n++ layer is a main factor to limiting the maximum V_{OC} as well as the high recombination rate from at the Ag electrode/silicon contact at the rear side. Furthermore, porous silicon layer is only 0.1% the thickness compared to its base c-Si wafer. This could lead to the inefficiency of the light absorption in the emitter layer, as the majority of the absorption occurs in the bulk c-Si below; therefore, the overall V_{OC} of this heterojunction structure is governed by the band gap of the base layer rather than the porous silicon.

In the simulation part, the band structures induced by porosity and passivation of Si were computed by the Density Functional Tight Binding (DFTB) method and compared. Four representative models of PSi were created: pillar, crater, internal sphere, and internal cube models. The results showed that the only component that determines the degree of expansion is not the pore, but the size of Si framework itself. The pillar diameter, the crater Si wall thickness, and the thickest Si skeleton part were varied including sizes which induce quantum confinement. The pillar height and crater depth have little to no effect on the band gap as long as the Si base is thicker than 1 nm. Moreover, only when two pillars are physically in contact and become crater model that the decrease of band gap is observed; the value converges to one of bulk Si (1.12 eV) as the pillars are more in contact to their neighboring pillars. On the other hand, when the crater diameters are large enough that the Si wall part is isolated, the band gap largely increases. Quantum confinement induced gap expansion was only observed when Si features approached 1 nm scale. To connect to the experiment to the simulation part, with the PSi wall thickness of more than 3.5 nm observed from TEM, the simulation result showed that the band gap expansion effect for this Si feature size is minimal (1.2-1.4 eV). Thus, the PSi framework must be fabricated with smaller sizes to utilize more quantum confinement effect.

In conclusion, this thesis investigated the possibility to use PSi as a top cell of the all-silicon tandem solar cell by both experiment and simulation approaches. With our original electrochemical passivation, the formation of the uniform and high coverage oxide layer could be achieved on PSi layer, resulting in the improvement of solar cell performance. The simulation on the electronic structure of PSi/c-Si models also shows that, in order to achieve gap expansion with porosity, it should therefore aim at controlling the size of Si features rather than the size of the pores or the porosity. These knowledge provide an insight on the more suitable PSi structure that can further improve the performance of solar cell in the future fabrication.

APPENDIX

TABLE S1: COMPUTED BAND GAP (E_G), THE VALENCE BAND MAXIMUM (VBM) AND CONDUCTION BAND MINIMUM (CBM), OF THE SPHERICAL PORE MODELS, ALONG WITH ITS CORRESPONDING FOUR INITIAL BOX SIZES (S(MALL), M(EDIUM), L(ARGE), XL (EXTRA LARGE)), NUMBER OF ATOMS, AND PORE PARAMETERS: DIAMETER (D), SHORTEST (L) AND LARGEST (L) INTER-PORE DISTANCE.

Model label	Box Size	Number of Atom			d	L	l	Porosity	VBM	CBM	E_g
	[nm]	Si	H	Total	[nm]	[nm]	[nm]	[%]	[eV]	[eV]	[eV]
S1	2.17	425	204	629	1.47	2.25	0.86	16.2	-5.48	-3.94	1.54
S2		465	188	653	1.20	2.72	0.98	8.8	-5.42	-4.09	1.33
S3		495	164	659	0.92	3.02	1.52	4.0	-5.40	-4.19	1.21
M1	3.26	1263	540	1803	2.56	3.01	0.72	25.4	-5.46	-4.06	1.40
M2		1537	436	1973	2.02	3.64	1.26	12.5	-5.40	-4.22	1.18
M3		1681	348	2029	1.20	4.58	2.07	2.6	-5.38	-4.29	1.09
L1	4.34	2997	948	3945	3.37	4.12	0.98	24.4	-5.39	-4.17	1.22
L2		3631	764	4395	2.56	4.89	1.81	10.7	-5.35	-4.25	1.10
L3		3949	612	4561	1.74	6.06	2.61	3.4	-5.37	-4.30	1.07
XL1	4.89	4264	1200	5464	3.87	4.79	0.98	26.0	-5.37	-4.20	1.17
XL2		5126	1000	6126	2.74	5.96	2.07	9.2	-5.36	-4.26	1.10
XL3		5636	792	6428	2.03	7.15	2.88	3.8	-5.37	-4.31	1.06
c-Si		**2048**	**128**	**2176**	**0**	**Bulk**	**Bulk**	**0**	**-4.83**	**-3.77**	**1.06**

TABLE S2. COMPUTED BAND GAP (E_G) OF THE INTERNAL CUBE MODELS, THEIR VALENCE BAND MAXIMUM (VBM) AND CONDUCTION BAND MINIMUM (CBM), ALONG WITH ITS CORRESPONDING FOUR INITIAL BOX SIZES (S, M, L, XL), NUMBER OF ATOMS, AND PORE PARAMETERS.

Model Name	Box Size	Number of Atom			Pore Size	Largest Si feature	Wall thickness	Porosity	VBM	CBM	E_g
	[nm]	Si	H	Total	[nm]	[nm]	[nm]	[%]	[eV]	[eV]	[eV]
S1	2.17	341	308	649	2.32	1.49	0.74	30.4	-5.63	-3.75	1.88
S2		417	252	669	1.99	1.77	1.00	16.0	-5.53	-3.95	1.58
S3		495	164	659	0.90	3.05	1.54	2.6	-5.40	-4.20	1.20
M1	3.26	863	828	1691	4.18	1.49	0.74	47.4	-5.64	-3.76	1.88
M2		1107	734	1831	3.87	1.77	1.00	33.8	-5.55	-3.90	1.65
M3		1449	540	1989	2.65	3.05	1.54	14.7	-5.43	-4.15	1.28
M4		1683	364	2047	1.39	4.27	2.36	2.4	-5.39	-4.28	1.11
L1	4.34	1625	1604	3229	6.07	1.49	0.74	58.3	-5.66	-3.76	1.90
L2		2133	1452	3585	5.75	1.77	1.00	45.8	-5.52	-3.89	1.63
L3		2931	1172	4103	4.52	3.05	1.54	27.1	-5.39	-4.10	1.29
L4		3669	852	4521	3.77	4.27	2.36	10.4	-5.37	-4.25	1.12
L5		4001	636	4637	2.01	5.52	3.15	2.1	-5.38	-4.30	1.08
L6		4091	524	4615	0.48	7.09	3.97	0.1	-5.39	-4.33	1.06
XL1	4.89	2096	2088	4184	7.01	1.49	0.74	62.6	-5.65	-3.76	1.89
XL2		2772	1912	4684	6.69	1.77	1.00	50.4	-5.50	-3.88	1.62
XL3		3870	1584	5454	5.46	3.05	1.54	32.2	-5.39	-4.10	1.29
XL4		4968	1192	6160	4.21	4.27	2.36	14.4	-5.37	-4.26	1.11
XL5		5552	904	6456	2.95	5.52	3.15	4.5	-5.38	-4.30	1.08
XL6		5786	720	6506	1.39	7.09	3.97	0.8	-5.39	-4.34	1.05
c-Si		**2048**	**128**	**2176**	**0**	**Bulk**	**Bulk**	**0**	**-4.83**	**-3.77**	**1.06**

TABLE S3. COMPUTED BAND GAP (E_G) OF THE PILLAR MODELS, CALCULATED BY ITS VALENCE BAND MAXIMUM (VBM) AND CONDUCTION BAND MINIMUM (CBM) ALONG WITH ITS CORRESPONDING NUMBER OF ATOMS, AND PORE FEATURES. THE BAND GAPS OF THE PILLAR AND BASE PART ARE CALCULATED SEPARATELY TO INVESTIGATE THE EFFECT OF THE LOCAL BAND GAP. FOUR KEY FEATURES ARE VARIED TO INVESTIGATE THE EFFECT OF EACH PART: PILLAR DIAMETER, PILLAR HEIGHT, BASE LAYER, AND INTERPILLAR DISTANCE WITH DIFFERENT PILLAR DIAMETERS. THE VARIED FEATURES IN EACH SET ARE HIGHLIGHTED IN BOLD.

Model Name		Number of Atom			Height	Base	Pillar Diameter	Distance		Porosity	VBM/CBM		E_g	
								Shortest	Largest		Wall	Base	Wall	Base
		Si	H	Total	[nm]	[nm]	[nm]	[nm]	[nm]	[%]	[eV]	[eV]	[eV]	[eV]
Pillar Diameter	1	1184	624	1808	7	1	**1**	2.17	3.46	93	-5.90 / -3.27	-5.22 / -3.63	2.63	1.37
	2	1834	824	2658	7	1	**2**	1.38	2.69	70	-5.54 / -3.64	-5.24 / -3.88	1.90	1.36
	3	3136	1016	4152	7	1	**3**	0.38	1.92	33	-5.26 / -3.73	-5.19 / -3.79	1.23	1.23
Pillar Height	1	237	100	337	**1**	1	1	0.54	1.15	70	-5.50 / -2.91	-5.02 / -3.57	2.59	1.45
	2	866	576	1442	**10**	1	1	0.54	1.15	70	-5.61 / -3.06	-5.08 / -3.72	2.55	1.36
	3	1532	1080	2612	**20**	1	1	0.54	1.15	70	-5.59 / -3.03	-5.09 / -3.75	2.56	1.34
	4	2235	1612	3847	**30**	1	1	0.54	1.15	70	-5.53 / -3.00	-5.08 / -3.76	2.53	1.32
	5	2901	2116	5017	**40**	1	1	0.54	1.15	70	-5.55 / -3.04	-5.09 / -3.77	2.51	1.32
	6	3567	2620	6187	**50**	1	1	0.54	1.15	70	-5.51 / -2.97	-5.08 / -3.76	2.54	1.32
Base Layer	1	1184	624	1808	7	**1**	1	2.17	3.46	93	-5.90 / -3.27	-5.22 / -3.63	2.63	1.59
	2	1569	652	2221	7	**2**	1	2.17	3.46	93	-5.70 / -3.18	-4.95 / -3.58	2.52	1.37
	3	2145	652	2797	7	**3**	1	2.17	3.46	93	-5.56 / -3.16	-4.80 / -3.62	2.40	1.18
Interpillar Distance Pillar diameter = 1 nm	1	468	400	868	10	1	1	**0.38**	0.77	33	-5.70 / -3.20	-5.22 / -3.94	2.50	1.28
	2	866	576	1442	10	1	1	**0.54**	1.15	70	-5.61 / -3.06	-5.08 / -3.73	2.55	1.35
	3	1006	632	1638	10	1	1	**1.09**	1.92	83	-5.68 / -3.13	-5.07 / -3.73	2.55	1.34
	4	1186	704	1890	10	1	1	**1.63**	2.69	89	-5.77 / -3.26	-5.04 / -3.72	2.51	1.32
	5	1406	792	2198	10	1	1	**2.17**	3.46	93	-5.82 / -3.29	-5.00 / -3.67	2.53	1.33
	6	1666	896	2562	10	1	1	**2.71**	4.22	95	-5.82 / -3.39	-4.97 / -3.64	2.43	1.33
	7	1966	1016	2982	10	1	1	**3.26**	4.99	96	-5.81 / -3.43	-4.94 / -3.60	2.38	1.34

Pillar diameter = 1.5 nm	1	999	604	1603	10	1	1.5	**0.38**	1.15	33	-5.43 / -3.28	-5.19 / -3.71	2.15	1.48
	2	1111	660	1771	10	1	1.5	**0.86**	1.92	63	-5.43 / -3.23	-4.99 / -3.65	2.20	1.34
	3	1255	732	1987	10	1	1.5	**1.38**	2.69	76	-5.52 / -3.34	-5.06 / -3.62	2.18	1.44
	4	1431	820	2251	10	1	1.5	**1.92**	3.46	83	-5.49 / -3.42	-5.03 / -3.59	2.07	1.44
	5	1639	924	2563	10	1	1.5	**2.46**	4.22	88	-5.53 / -3.48	-4.99 / -3.56	2.05	1.43
	6	1879	1044	2923	10	1	1.5	**2.99**	4.99	91	-5.55 / -3.51	-4.96 / -3.52	2.04	1.44
	7	2151	1180	3331	10	1	1.5	**3.54**	5.76	93	-5.60 / -3.54	-4.92 / -3.48	2.06	1.44
	8	2455	1332	3787	10	1	1.5	**4.08**	6.53	94	-5.61 / -3.58	-4.90 / -3.45	2.03	1.45
Pillar diameter = 2 nm	1	1947	956	2903	10	1	2	**0.38**	1.15	33	-5.16 / -3.44	-5.13 / -3.65	1.75	1.48
	2	2091	1028	3119	10	1	2	**0.86**	1.92	57	-5.21 / -3.42	-5.09 / -3.63	1.79	1.46
	3	2267	1116	3383	10	1	2	**1.38**	2.69	70	-5.25 / -3.47	-5.06 / -3.62	1.78	1.44
	4	2475	1220	3695	10	1	2	**1.92**	3.46	78	-5.34 / -3.52	-5.03 / -3.60	1.82	1.43
	5	2715	1340	4055	10	1	2	**2.46**	4.22	83	-5.37 / -3.55	-5.00 / -3.56	1.82	1.44
	6	2987	1476	4463	10	1	2	**2.99**	4.99	87	-5.38 / -3.59	-4.97 / -3.54	1.79	1.43
	7	3291	1628	4919	10	1	2	**3.54**	5.76	89	-5.42 / -3.62	-4.95 / -3.51	1.80	1.44

TABLE S4: COMPUTED BAND GAP (E_G) OF THE CRATERS MODELS, CALCULATED BY ITS VALENCE BAND MAXIMUM (VBM) AND CONDUCTION BAND MINIMUM (CBM) (NOT SHOWN IN THE TABLE), ALONG WITH ITS CORRESPONDING NUMBER OF ATOMS, AND PORE FEATURES. THE BAND GAPS OF THE CRATER ARE DIVIDED INTO THE WALL AND BASE PARTS, WHICH ARE CALCULATED SEPARATELY TO INVESTIGATE THE EFFECT OF THE LOCAL BAND GAP. THREE KEY FEATURES ARE VARIED TO INVESTIGATE THE EFFECT OF EACH PART: CRATER DEPTH CRATER WALL THICKNESS, AND CRATER DIAMETER.

Model Name		Number of Atom			Depth	Base	Crater Diameter	Thickest Wall	Thinnest Wall	Porosity	VBM/CBM		E_g	
											Wall	Base	Wall	Base
		Si	H	Total	[nm]	[nm]	[nm]	[nm]	[nm]	[%]	[eV]	[eV]	[eV]	[eV]
Crater Depth	1	1823	576	2399	**4**	1	2.4	1.92	0.86	34	-5.20 / -3.60	-5.08 / -3.69	1.63	1.45
	2	2491	784	3275	**6**	1	2.4	1.92	0.86	37	-5.18 / -3.57	-5.06 / -3.63	1.61	1.43
	3	3827	1200	5027	**10**	1	2.4	1.92	0.86	39	-5.18 / -3.55	-5.03 / -3.58	1.63	1.39
Crater Wall Thickness	1	1823	576	2399	4	1	2.4	**1.92**	0.86	34	-5.20 / -3.60	-5.08 / -3.69	1.60	1.39
	2	2759	680	3439	4	1	2.4	**2.69**	1.38	25	-5.04 / -3.77	-5.04 / -3.77	1.27	1.27
	3	3839	800	4639	4	1	2.4	**3.46**	1.92	19	-5.00 / -3.82	-5.00 / -3.82	1.18	1.18
Crater Diameter	1	895	348	1243	4	1	4	**0.38**	0	79	-6.85 / -2.38	-5.03 / -3.61	4.47	1.42
	2	989	392	1381	4	1	3.8	**0.77**	0	73	-6.41 / -3.21	-5.05 / -3.62	2.93	1.43
	3	1087	476	1563	4	1	3.5	**0.96**	0	64	-5.89 / -3.17	-5.07 / -3.55	2.72	1.52
	4	1137	444	1581	4	1	3.45	**1.15**	0	63	-5.69 / -3.49	-5.09 / -3.62	2.20	1.47
	5	1259	644	1903	4	1	3.2	**1.15**	0.12	56	-5.67 / -3.43	-5.10 / -3.58	2.24	1.52
	6	1525	608	2133	4	1	2.8	**1.54**	0.38	44	-5.31 / -3.55	-5.08 / -3.66	1.76	1.42
	7	1823	576	2399	4	1	2.4	**1.92**	0.86	34	-5.20 / -3.60	-5.08 / -3.69	1.60	1.39