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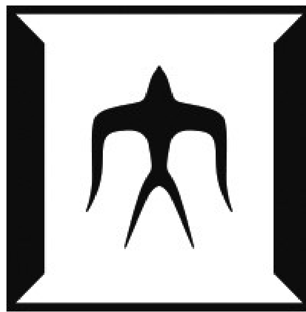
Research on semiconductor monolithic microwave integrated circuits for the advanced information and communication network infrastructure

Jun Kamioka

A dissertation submitted for the degree of Doctor of Engineering

Supervised by

Associate Professor Tetsuo Kodera



Tokyo Institute of Technology

March 2023

Abstract

Recently, there has been a need to address social issues via systems that combine communication and sensing in virtual space and reality, using artificial intelligence and big data. In addition, in an age when everything is connected to the network, cyber-attacks are a great threat, and highly reliable and secure communication technologies are becoming even more important. These requirements call for systems that combine ever more advanced wireless communication technologies with new quantum communication technologies as advanced information and communication network infrastructures. Various RF circuits are used in these systems and are keys to achieving system performance. Monolithic microwave integrated circuits (MMICs), where active microwave elements such as field-effect transistors (FETs) and diodes are integrated with passive elements on a single semiconductor chip, can allow for the optimization of RF circuits to meet the miniaturization and performance requirements in these advanced infrastructures. It is crucial to optimize the circuit constants of MMICs and improve the performance trade-off relationship by proposing new circuit configurations and device structures and combining different types of circuits. In this thesis, research is conducted on semiconductor MMICs as a viable route to high-speed, high-capacity, low-power consumption, low-cost, and high-reliability communications.

Key RF devices that would lay the foundation of advanced wireless communication systems combined with emerging quantum communication technologies include high-power and high-efficiency amplifiers and switches, low-cost transmit/receive (T/R) modules, and silicon-based quantum communication and computing chips. The base station uses high-power and high-efficiency GaN amplifiers and switches for wireless communications. GaN devices are key components that account for a large portion of wireless communication systems' power consumption and cost. Electron spin qubits based on silicon quantum dots with long coherence time and the advantage of miniaturization are great candidates for high-reliability quantum networks and computation. Improving the performance of these devices by applying MMIC technologies and optimizing circuit configurations is important, and we have researched as follows.

First, an ultra-wideband bandpass distributed GaN-MMIC power amplifier is designed and measured to realize fast and high-capacity communications. Non-uniform distributed

amplifiers (NDPAs) are used as broadband high-power-amplifiers (HPAs), but there has been a trade-off relation between output power and bandwidth. Here, we have improved the trade-off relation by proposing a bandpass distributed amplifier. We designed and evaluated a single-ended bandpass NDPA and a 2-way combined NDPA. Measurement results of the NDPAs show that the developed amplifiers achieve the highest output power and power density among the reported MMIC HPA with relative bandwidth of over 100%.

Second, the design and measurement of a GaN-MMIC high-efficiency power amplifier using the individual source via (ISV) structure is conducted to achieve low power consumption. FETs used in HPAs have a comb electrode structure with multiple source fingers, drain fingers, and gate fingers to increase the total gate width. In conventional FETs, the source fingers are each bundled and connected to the via holes through transmission lines. In this configuration, the parasitic resistance and inductance between the source fingers and the via holes degrades the amplifiers' gain and efficiency. Therefore, an ISV structure with small via holes in all source fingers was applied to improve the performance of GaN amplifiers. We also optimized an output matching circuit by considering the relationship between load impedance and circuit loss. Measurement results of the developed X-band GaN-MMIC amplifier demonstrate the highest performance in terms of the combinations of output power and power added efficiency (PAE) compared to existing state-of-the-art X-band MMIC HPAs.

Third, power amplifiers and a switch incorporating partial MMIC and GaN-on-Si technologies are developed. GaN power amplifier generally refers to GaN fabricated on a SiC substrate (GaN-on-SiC). It has high performance, but tends to be expensive because of the high cost of SiC substrates. Therefore, we developed a GaN-on-Si-MMIC using a cost-effective silicon substrate. We also proposed a partial MMIC configuration that combines a GaN-based MMIC and low-cost, low-loss GaAs matching circuits. These MMIC configurations were combined into a chipset for low-cost T/R modules: a GaN-on-Si-MMIC DA, a GaN-on-SiC MMIC HPA with a GaAs MMIC input and output matching circuits, a high-gain GaN-on-Si HPA with a GaAs output matching circuit and a GaN-on-Si high-power switch. The T/R module configuration using these components achieves a comparable performance to conventional modules at about half the cost.

Finally, research on silicon quantum dot devices for realizing quantum computers and networks is conducted. Design of compact and wideband on-chip matching circuits of quantum dot charge sensor based on RF reflectometry towards fast readout of qubit state is implemented. The matching circuit of a charge sensor has so far been comprised of a shunt capacitor and a series inductor on the printed circuit board using chip components.

To reduce the size and broaden the bandwidth of the matching circuit, we extracted the equivalent circuit parameters on the silicon chip of the quantum dots device. We also formulated circuit constants of three matching circuits, the shunt capacitor-series inductor, shunt inductor-series capacitor and shunt inductor-series inductor. We compared them in terms of sensitivity and frequency bandwidth. The newly proposed shunt inductor-series inductor type was shown to have the widest bandwidth. The design with this configuration provides the bandwidth required for high-speed readout while using smaller inductance than conventional circuit configurations, demonstrating the feasibility of on-chip compact matching circuits.

The proposal of new MMIC configurations and analysis in these researches have achieved great performance among the other reported results. We believe that these results will contribute to the realization of the advanced information and communication network infrastructure.

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Chapter 1.

Introduction

1.1 Research background

Communication is reproducing at one point either exactly or approximately a message selected at another point [1].The Morse telegraph was the first to use electric signals for ultra-high-speed communication in 1893. Since then, wireless communication, which enables communication between physically distant equipment such as mobile devices or satellites, and ultrahigh-speed, high-capacity optical communication, have been combined to realize systems that connect globally. New applications and services have been created among such systems by increasing the capacity and speed of communications. Communication is a core technology that changes the face of people's lives. There has recently been need to solve social issues through systems that combine communication and sensing in virtual space and reality, using artificial intelligence and big data. In addition, in an age when everything is connected to the network, cyber-attacks are a great threat, and highly reliable and secure communication technologies are becoming even more important.

Cyber–physical systems (CPS) have been proposed as a new generation of systems with integrated computational and physical capabilities that can interact with humans through many modals [2]. Fig. 1-1 shows the targeted cyber–physical systems. In the physical system, many devices are expected to be connected to the network and optimally controlled. Driverless cars [3] and unmanned aerial vehicles (UAVs) [4] will be moving around the city as next-generation transportation. In the industrial sector, there will be a

need for smart factories where automated guided vehicles (AGVs) and autonomous mobile robots (AMRs) work [5], smart farming [6], monitoring and control of infrastructures, telemedicine systems and so on. Components utilized in the system should not be operated individually, but rather the physical and behavioral interactions between components should be considered to achieve efficient and safe operation of the system as a whole.

To realize CPS, wireless communication infrastructure that can manage acceptable dynamic traffic load and deliver real-time data is necessary. Reliability and robustness are also very important, especially for monitoring and controlling systems because data transmission interruption will cause the unstable operation and cascade failure [8]. There are also challenges in analysis and simulation for overall system optimization in cyber systems. Multiple information must be handled for many devices, resulting in a complex system with enormous variables. Quantum computing, which utilizes quantum superposition is expected to play an active role in such combinatorial optimization with huge amounts of data and dimensions [10][11]. CPS monitor and control various physical processes in major industrial and critical infrastructure, including power grids, energy generating stations, gas pipelines, and water networks. Security risks to critical infrastructure are increasing with the realization of CPS [12]. Therefore, a highly reliable quantum network that can retain security even against attacks using quantum computers is needed.

These requirements call for systems that combine ever more advanced wireless communication technologies with new quantum communication technologies as advanced information and communication network infrastructures. Various RF circuits are crucial to achieving system performance in these systems. Monolithic microwave integrated circuits (MMICs), where active microwave elements such as field-effect transistors (FETs) and diodes are integrated with passive elements on a single

semiconductor chip, can optimize the RF circuits as a whole to meet the stringent miniaturization and performance requirements in these advanced infrastructures. The various characteristics of MMICs (frequency bandwidth, output power, efficiency, cost, etc.) have a trade-off relationship, and the method of optimizing circuit constants in a typical circuit configuration has limited performance improvement. Here, we proposed a new circuit configuration, improved the device structure, or combined multiple circuits to improve the trade-off relationship.

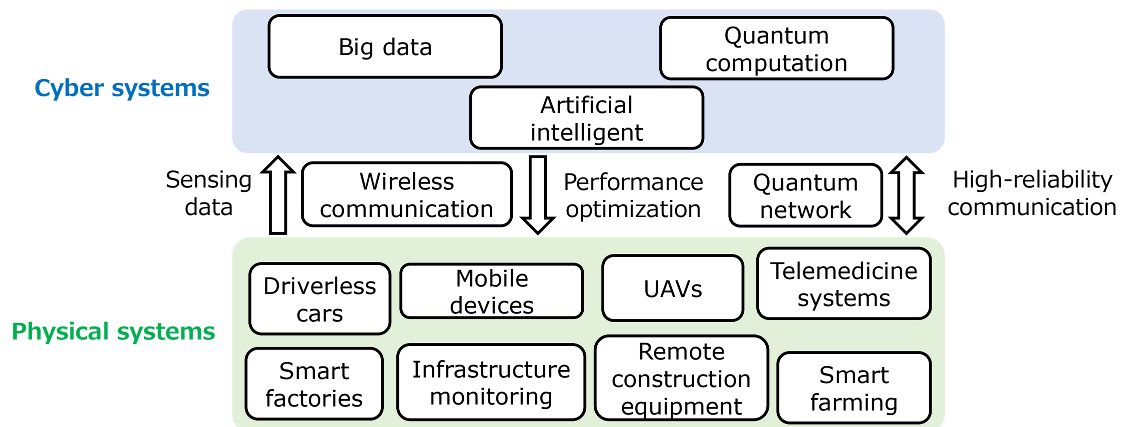


Fig. 1-1. Targeted cyber–physical systems

1.2 Key components for the advanced information and communication network infrastructure

Research on the following components was implemented to achieve the advanced information and communication network infrastructures that combine ever more advanced wireless communication technologies with new quantum communication technologies. (1) GaN-MMIC ultra-wideband bandpass distributed amplifier, (2) GaN-MMIC high-efficiency high power amplifier (HPA) using individual source via structure (ISV), (3) Power amplifiers and a switch incorporating partial MMIC and GaN-on-Si

technologies for low-cost transmit/receive module, (4) On-chip matching circuits for RF reflectometry using Si quantum dot charge sensor. Their background and requirements are discussed.

1.2.1 Wireless transmitting microwave circuits

The market for wireless communications has experienced tremendous growth recently. Transmission speeds have increased tenfold approximately every five years to accommodate mobile traffic growth. Next-generation communication systems use multi-carrier modulation, such as orthogonal frequency division multiplexing (OFDM) to achieve higher-speed communication. The number of subcarriers is increasing, and the requirement for operating frequency bandwidth is getting wider. Although it is necessary to increase the number of base stations to achieve communication with more devices, simply increasing the number of base station facilities makes installation and operating costs expensive. Therefore, co-construction and shared base station is proposed [14]. The concept of a virtual base station [15] is also important technology. Conventionally, base station facilities composed of a central unit (CU), distributed unit (DU) and radio unit (RU) have been developed for each frequency band and each telecommunications carrier. A virtualized base station is a technology to operate base station equipment suitable for each carrier by switching software on common hardware. While the virtualization of CU and DU has already been developed, RUs have not been virtualized owing to the difficulty of developing several RF components, such as a wideband amplifier. Ideally, a virtualized RU that can accomplish multiple frequency RUs with one is required. In about ten years, fully virtualized base stations will be required to further reduce installation and operation costs. Furthermore, virtualized RUs can switch operational frequencies by software to avoid interference with neighboring base stations.

There are various components to be developed for the realization of virtualized RU.

Tunable filters are needed to suppress unwanted emissions from RF-ICs, antennas, and stray signals from transmit module to receive module. Various configurations of filters have been considered [16] to improve the trade-off relationship among bandwidth, tunability and loss. Reduction of loss of the filter used for the output side of a high-power amplifier and the input side of a low-noise amplifier is particularly important because of its significant impact on output power, efficiency, and noise figure. Hence, research on the tuner filter for the virtualized RU on the filter is still challenging. Wideband high power switches for switching between 4G and 5G systems, transmit/receive mode are necessary. Although loss reduction is still challenging for broadband switches, the bandwidth required for RU virtualization has already been developed [17]. Wideband antennas that can handle various frequency bands in one are also important. Remarkable results have been achieved for wideband antenna technology [18]. Wideband low noise amplifiers (LNAs) and HPAs for received and transmitted signals are also needed. The technology for wideband LNAs is relatively mature and has already been developed for the required bandwidth [19]. For HPAs, it is challenging to obtain wideband and high power for the realization of virtualized RUs. Realizing wideband HPA is one of the most significant challenges for RU virtualization. Reducing power consumption is also important. There are several ways to reduce the base station's power consumption, such as lowering the digital components' operation voltage, digital pre-distortion [20], and PAPR reduction [21]. It is reported that cellular phone base stations consume more than 50% of the energy in a cellular network [22], and 65% of the energy consumed by base stations comes from power amplifiers [23]. Therefore, improving the efficiency of the power amplifiers is the key issue. The number of base stations has increased two to three times in the past decade. Because many T/R modules are installed in active phased allay antennas (APAAs) used for satellite communications or 5th generation mobile network (5G) base stations, reducing the cost per module is also important.

1.2.2 Power amplifiers

Many semiconductor microwave circuits are used in wireless communication systems. Among them, power amplifiers require selecting an appropriate semiconductor process depending on the required performance and application. Power amplifiers are components with high power consumption, which affects the design of the module's heat dissipation. Reliability to withstand high voltage, large RF power, and high channel temperatures is necessary. Table 1-1 shows semiconductor material parameters used in power amplifiers [24][23]. The larger the band gap, the better the chemical stability and the higher the breakdown voltage. GaN is called wide bandgap semiconductors, which allow operation at higher voltages, resulting in higher power density and superior devices for high-power applications. The higher the mobility and electron saturation velocity, the better the high-frequency properties. Fig. 1-2 shows trends in amplifier output power and frequency [25]. This graph shows the survey results from 2000 to November 2020, and the trend toward even higher frequencies and output power continues to grow. There are advantages and disadvantages of using each material in amplifiers, and the most suitable device should be used for each application based on trade-offs. For high-power applications, Si laterally diffused metal oxide semiconductor field effect transistors (LDMOS) are very competitive devices in applications such as mobile phone base stations mainly up to the S-band, due to their low cost and the benefit of highly developed process technology for LSIs. GaAs pseudomorphic high electron mobility transistors (PHEMTs) have been used in HPAs over approximately 100 GHz because of their high mobility, about five times greater than Si. PHEMTs have been used in high-power amplifiers; GaAs HEMT also have excellent noise characteristics and are often used as low-noise amplifiers. Recently, GaN HEMTs have attracted much attention owing to the demand for even higher efficiency and miniaturization of amplifier devices. GaN has a higher operating voltage than GaAs, leading to a higher power density. GaN HPA for base

stations, communication satellites, radar, etc. In recent years, amplifiers with even higher output power, efficiency, and wider bandwidth have been required for advanced communication systems. As obtaining high performance of the GaN HEMT themselves, advanced GaN-MMIC design techniques that maximize the characteristics of the devices are also important.

Table 1-1. Semiconductor material parameter

Characteristic	Unit	Semiconductor			
		Si	GaAs	InP	GaN
Band gap	eV	1.1	1.42	1.35	3.49
Electron mobility	cm^2/Vs	1500	8500	5400	2000
Saturated electron velocity	10^7 cm/s	1	1.3	1	2.5
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.3
Thermal conductivity	Wcm/K	1.5	0.5	0.7	1.5
Relative dielectric constant		11.9	12.8	12.5	9

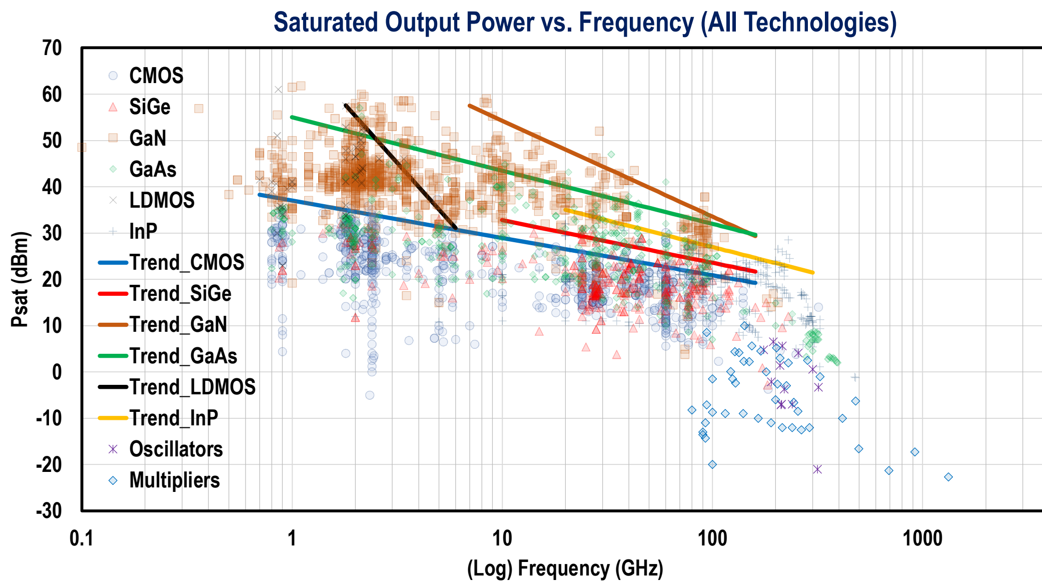


Fig. 1-2. Trends in amplifier output power and frequency [25]

1.2.3 Quantum computers and quantum network systems

In advanced information and communication network infrastructures, quantum computers that enable ultra-fast computation should be combined with highly reliable quantum communications that are not vulnerable to sophisticated cyber-attacks. A quantum computer is a computer based on a new principle that uses the properties of quantum mechanical superposition and quantum entanglement to solve problems such as prime factorization [26] and database searching [27], which cannot be solved in realistic time using classical computers. In classical computers, the binary values "0" and "1" are used as bits for computation. A superposition of quantum states $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$, called a qubit is adopted in quantum computers, where α and β represent complex constants while $|0\rangle$ and $|1\rangle$ are quantum states. Quantum computing on a small scale has been achieved so far [28]–[31]. Quantum error correction is necessary to maintain quantum coherence. However, more than 1000 logic qubits are needed to perform tasks that outperform classical computing, and 10^4 per logic qubit (with an error rate of 1%) is said to be needed to provide quantum error correction (QEC) [32]. Technical challenges remain for quantum computing, such as realizing qubits at high yields, efficient gate manipulation of many qubits, and qubit integration.

Quantum communication is one of the most important technologies for advanced network infrastructures. Various confidential information is connected to networks and shared. Based on the difficulty of the prime factorization, the RSA cipher still plays a central role in the cryptographic infrastructure. The RSA cipher can be solved in polynomial time by using a quantum computer. Quantum cryptography has been proposed as a robust cryptosystem even when large-scale quantum computers become practicable [34]. In wired optical networks, the signal is reduced by losses of cables. In classical communication, optical amplifiers or optical repeaters are used to solve the problem. However, in quantum communication, quantum states are quite fragile, and the quantum

no-cloning theorem makes it difficult to amplify or repeat the signal. For a future high-performance quantum internet, quantum error correction will be performed at each relay. As quantum error correction requires many quantum bits, the network will comprise quantum computers connected at each node [33]. By realizing the quantum network, distributed quantum computation for more complex and advanced computations will be achieved. Cloud processing to preserve privacy can also be possible, which is one solution to the problem of communication security.

1.2.4 Semiconductor quantum dot

There has been research on various types of qubits, each system has advantages and disadvantages, and the various qubit systems are expected to be incorporated into suitable fields and combined as a quantum network system.

Superconducting qubit is one of the most promising qubits, with remarkable progress in achieving 53 qubit operations [28]. Superconducting qubit has a resonant circuit structure with a capacitor and a non-linear inductor using a Josephson junction. They have long coherent times, good manufacturability, and the capability of gate manipulation of qubits. The challenge for them is integration to achieve a large-scale qubit system because the footprint of one qubit is relatively larger than other qubit systems (about 1 mm^2). The system must be operated at cryogenic temperatures of several 10 mK. It is challenging to realize millions of qubits towards quantum error correction, because of the limited size of the cryogenic space.

Trapped ion qubits are also good candidates for quantum computation. The qubits use charged ion held in an electromagnetic field. They have long coherence times and more than ten qubits have been realized [29][30]. The system also has a scalability problem because controlling many ions in a single ion trap is difficult, and techniques to connect multiple ion traps are required.

Photon qubits have a long coherence time and operation capability at room temperature. They can be transmitted over long distances and are useful for forming quantum networks. However, they are difficult to integrate, and gate operations for multiple qubits cannot be performed efficiently. Research on converting photon qubits to electron spin qubits is also conducted.

Electron spin qubits have long coherence times and compact sizes (10–100 nm). NV centers are one of the promising devices for quantum sensors and quantum repeaters, and qubits based on electron spins confined in quantum dots are also being investigated. NV centers have a long spin coherence time and can operate at room temperature, making them promising devices for quantum sensors and quantum repeaters.

Semiconductor quantum dots (QDs) are promising as quantum computers. QDs can be formed at targeted locations using semiconductor microfabrication processes, which have been developed over the years. Their size is minimal, and their potential and coupling between them can be controlled by gate manipulation. Thus, semiconductor QD can solve the problems of high integration and controllability that have been challenges for other qubits.

Semiconductor quantum dots (QDs) were first intensively studied using GaAs/AlGaAs heterostructures. However, spins in GaAs QD have short coherence time due to hyperfine interaction with nuclear spins, making high-fidelity operation difficult. Therefore, research on QDs using silicon, a material with fewer nuclear spins, has been actively conducted recently. In addition, silicon has a larger effective mass than GaAs, which requires smaller quantum dot sizes. Although the process is more challenging, long coherence times have been confirmed using silicon quantum dots [35][36].

For the readout of spin qubits, charge sensing plays an important role. Charge sensing should be performed within the spin operation time not to limit quantum computation speed. Therefore, RF reflectometry is used to achieve a fast readout of qubits [37]. This

method has the advantage of being insensitive to low-frequency noise, such as $1/f$ noise [38]. Broadband and miniaturization of impedance matching circuits for RF reflectometry is important for high-speed readout and high integration.

1.3 Organization of this thesis

Fig. 1-3 shows the organization of this thesis. Chapter 1 is the background and introduction to the research. Chapter 2 shows the challenges of advanced information and communication network infrastructure. Chapter 3 shows the GaN-MMIC ultra-wideband bandpass distributed amplifier for ultra-fast, large capacity wireless communication systems. Chapter 4 shows the GaN-MMIC high-efficiency high power amplifier using ISV structure to lower power consumption of wireless communication systems. Chapter 5 shows power amplifiers and a switch incorporating partial MMIC and GaN-on-Si technologies for low-cost T/R module. Chapter 6 shows the on-chip matching circuits for RF reflectometry using Si quantum dot charge sensor for high reliability quantum network. Chapter 7 concludes the study.

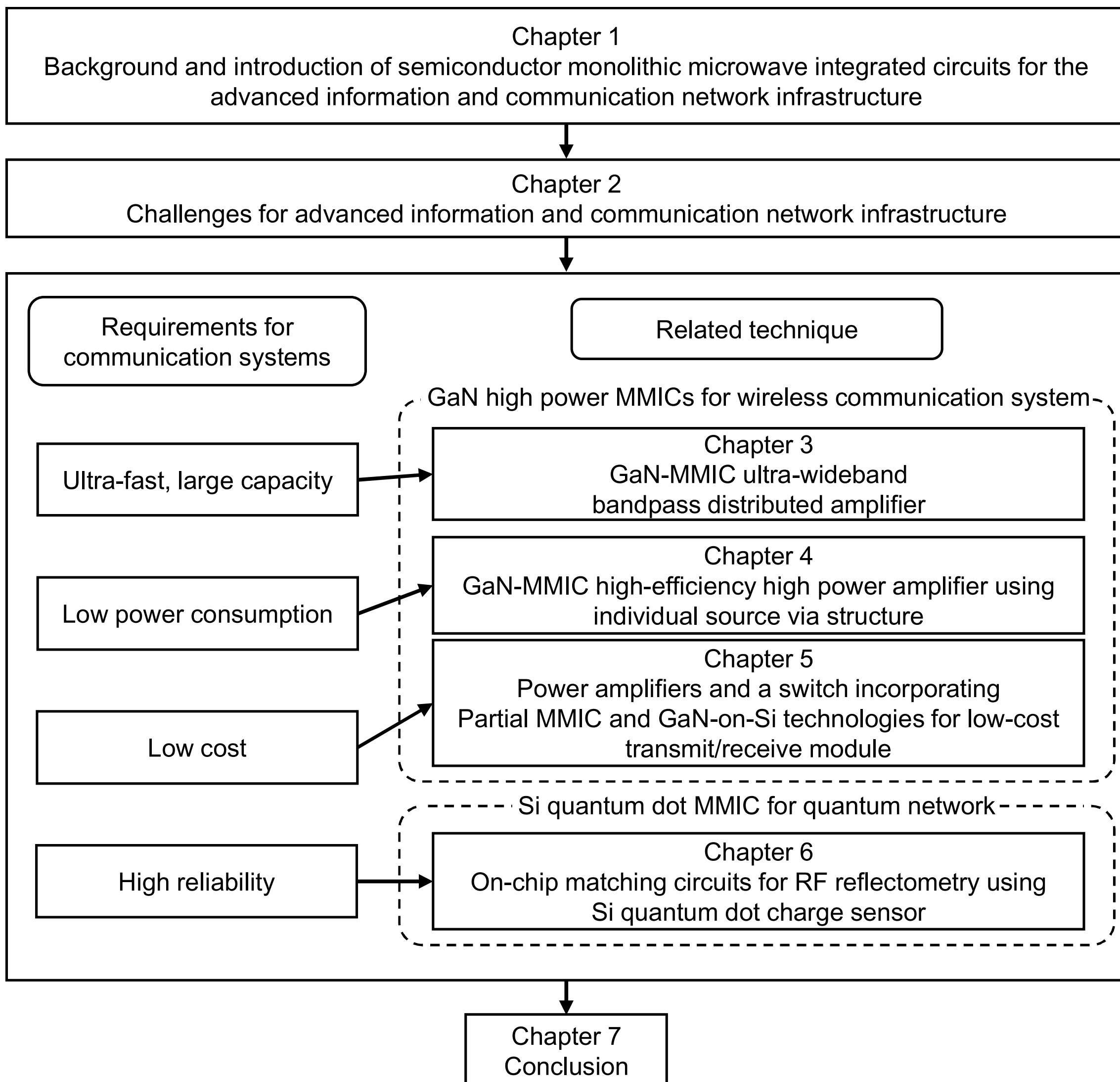


Fig. 1-3. Organization of this thesis

Chapter 2.

Challenges for advanced information and communication network infrastructure

2.1 Monolithic microwave integrated circuits

MMICs are one of the technologies that enable miniaturization and higher performance of RF circuits. MMIC integrates active microwave elements like FETs and diodes with passive elements such as matching circuits on a semiconductor chip. In contrast, the method in which only active components are formed on a chip and other passive components are formed on a separate printed circuit board (PCB) is called “discrete”. In MMIC, compact circuit components such as spiral inductors and metal-insulator-metal (MIM) capacitors can be used. This allows greater freedom in designing RF circuits and enables wider bandwidth and higher efficiency, as there is no need to consider parasitic components such as bonding wires for connection to the PCB. MMIC amplifiers were initially mainly GaAs and SiGe MMICs, but recently, GaN-MMICs have often been developed due to the demand for higher performance. Matching circuits of RF reflectometry circuits in Si quantum dot devices are currently realized in discrete form, but MMICs are expected to achieve miniaturization and higher performance. MMIC design technology is, therefore, very important.

2.2 Power amplifier

2.2.1 Basics of power amplifier

Fig. 2-1 shows a schematic of a simple amplifier. The amplifier comprises a transistor, an input matching circuit, and an output matching circuit. The RF signal is input to the gate of the FET through the input matching circuit, and the amplified signal is output from the drain of the FET through the output matching circuit. The input matching circuit transforms the source impedance (Z_0) to impedance Z_{in} to maximize the gain. The output matching circuit transforms the load impedance (Z_0) to impedance Z_{out} to maximize the output power or efficiency. Owing to the parasitic capacitance in the FET, the optimum load impedance is frequency dependent, and designing a broadband matching circuit is difficult. The optimum load impedance for the transistor is determined by load-pull measurement [39], which performs large-signal measurements while changing input and output loads using an impedance tuner. The basic properties of an amplifier include frequency bandwidth, output power P_{out}, Gain (P_{out} - P_{in}), power consumption P_{dc}, and drain efficiency which indicates how much output power is obtained relative to power consumption shown as

$$\mathrm{DE} = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}} \times 100 \tag{2-1}$$

and power-added efficiency, including input power

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} \times 100. \tag{2-2}$$

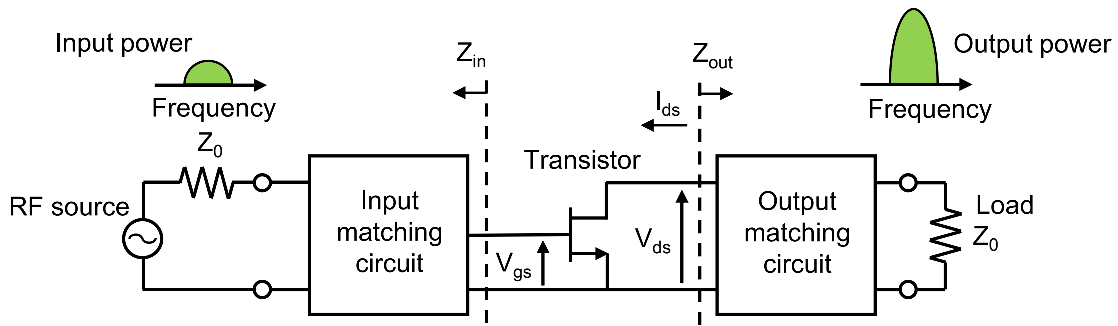


Fig. 2-1. Schematic of simplified amplifier.

2.2.2 Wideband amplifier

Sub-6 (below 6 GHz) and millimeter wave bands (28 GHz) are used for IoT communications. Millimeter wave is suitable for high-speed communication, but its high linearity makes it difficult for radio waves to penetrate. It is also difficult to achieve high output power and cover a wide area. This study attempts to achieve wideband and high amplifier power for RU virtualization at sub-6 GHz. Until now, different base stations have been used for different generation mobile networks, such as 4G and 5G, with a bandwidth of up to 200 MHz. As explained in 1.2.1, wideband RU is required for the fully virtualized base stations.

In the sub-6 band, 800–4800 MHz is used for the downlink from 4G and 5G base stations to mobile devices, which is 143% of the relative bandwidth given by the following equation

$$Relative\ bandwidth = \frac{\text{Bandwidth}}{\text{Center frequency}} \times 100. \tag{2-3}$$

Considering the replacement of conventional base stations, a 40-W class high-power amplifier is necessary, but a 40-W class amplifier that exceeds the relative bandwidth of 100% has not been realized. Therefore, wideband HPAs have become a bottleneck in system development.

Several broadband amplifier configurations are described below. Resistively matched

amplifiers use resistors for impedance matching. For example, Fig. 2-2 shows a resistively matched amplifier with shunt resistors on the input and output sides of an FET. Because resistors do not have frequency dependence, wideband flat characteristics can be achieved [40]. However, the amplifier's efficiency, output power, and noise figure are degraded because of losses caused by the resistor. Therefore, it is used as a multi-stage amplifier when only gain and frequency bandwidth are required.

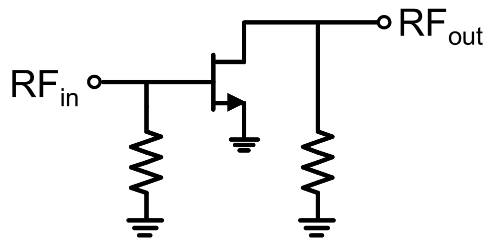


Fig. 2-2. Schematic of resistively matched amplifier

Negative feedback amplifiers are also known as broadband amplifiers. Fig. 2-3 shows a parallel feedback type negative feedback amplifier with a series RC circuit connected between the gate and drain of an FET. Flat gain and reflection characteristics can be obtained over a wide bandwidth. Particularly in LNA, achieving both low input reflection characteristic and NF matching is possible. Therefore, the structure is combined with a reactively matched amplifier configuration, which will be described later. Negative feedback amplifiers with a decade bandwidth have been realized with a few Watts of output power and tend to have low efficiency [19][41].

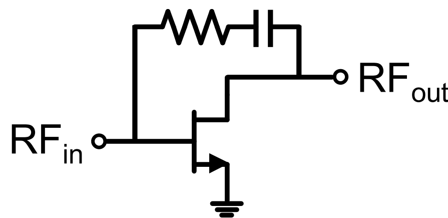


Fig. 2-3. Schematic of negative feedback amplifier

Reactively matched power amplifiers (RMPAs) are the most commonly used configuration for high-power amplifiers. Fig. 2-4 shows the schematic of RMPA. In the RMPA, reactive components such as inductors, capacitors, and transmission lines are used to obtain impedance matching between the input or output port and the optimum impedance of the transistors. Multiple FETs are arranged in parallel, and the matching circuits are designed to distribute and combine them symmetrically in a tournament-like manner such that all transistors operate in phase. RMPAs have high power and high efficiency owing to the low-loss matching circuit. Higher output power can be achieved simply by increasing the total gate width of the FETs, and output power above 50 W can be achieved with a GaN-MMIC. The output impedance of an amplifier can be expressed by a parallel circuit of resistors (R_{p}) and capacitors (C_{p}) [42]. According to Bode–Fano theory, reactive matching for parallel RC circuits has limited bandwidth [43]. The bandwidth limit of an output matching circuit is approximately expressed in inverse proportion to the supply voltage shown in the following equation [44].

$$BW < \frac{4.343 I_{\mathrm{MAX}}}{RL(dB) C_{\mathrm{p}} \beta (V_{\mathrm{D}} - V_{\mathrm{k}})} \tag{2-4}$$

where V_{D} is drain voltage; V_{K} is knee voltage (minimum drain voltage where maximum drain current is obtained); I_{MAX} is maximum drain current; RL is return loss, and β is fitting parameters which typically vary between 1 and 2. This is a theoretical limit, and the bandwidth becomes even narrower when a realizable circuit size is considered. Hence, a typical matching circuit has up to three stage impedance transformers, and the relative bandwidth of reported GaN-MMIC amplifiers with over 20-W class output power is up to 100 %.

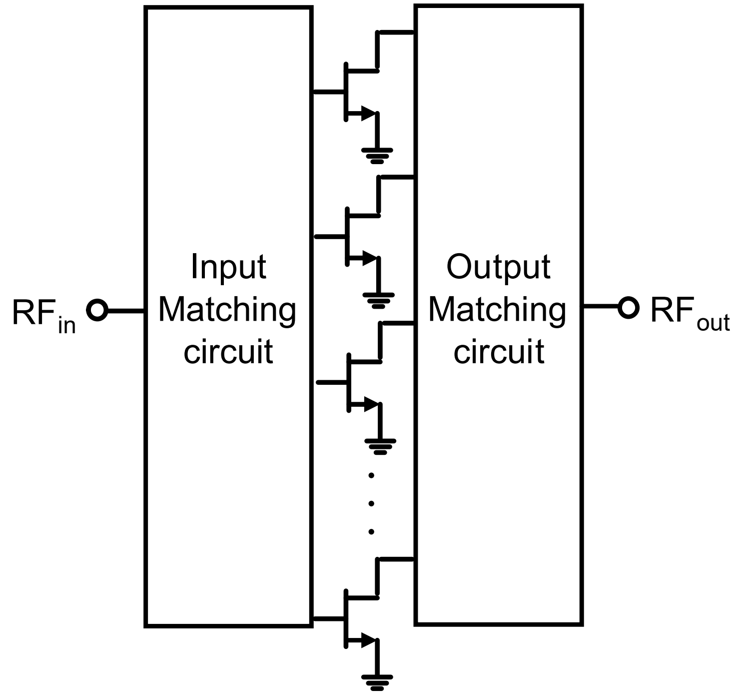


Fig. 2-4. Schematic of RMPA.

Distributed amplifiers are a configuration that can overcome the effects of the Bode–Fano limitation. Reducing C_p is effective for wider bandwidth. Fig. 2-5 shows the schematic of the uniform distributed power amplifier. The FET's output and input parasitic capacitance is absorbed in the "artificial transmission line" with impedances Z_d and Z_g [45]. Low reflection properties are obtained over a wide bandwidth by designing all artificial transmission lines to have the same impedance as the termination resistors (R_g, R_d). The disadvantages of uniform distributed power amplifiers are low output power and efficiency because the output power is consumed at the terminating resistor on the output side R_d. In addition, impedance matching between optimum load impedance and output port is not achieved.

To solve this problem, a non-uniform distributed power amplifier (NDPA) was developed [46]. Fig. 2-6 shows schematic of the non-uniform distributed power amplifier. In non-uniform distributed amplifiers, the output side termination resistor is eliminated.

The impedance of the artificial transmission line on the output side is higher on the left in the figure to obtain the optimum load impedance for each FET. High output and high efficiency for wide bandwidth can be obtained by NDPA. However, the NDPA does not allow for infinitely wide bandwidth. The parasitic capacitance of the FET and transmission lines have a cut-off frequency, which limits their wideband capability. Reducing the unit gate width of each FET and increasing the number of FETs can increase the cut-off frequency, but it increases circuit loss and size, leading to lower output power and efficiency. Therefore, even with non-uniform distributed amplifiers, bandwidth, output power, and efficiency have a trade-off relationship. Achieving both high output power and wide bandwidth is a challenge.

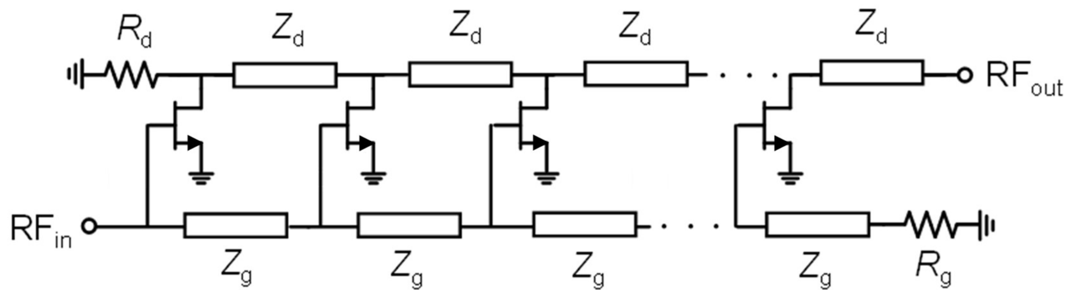


Fig. 2-5. Schematic of the uniform distributed power amplifier.

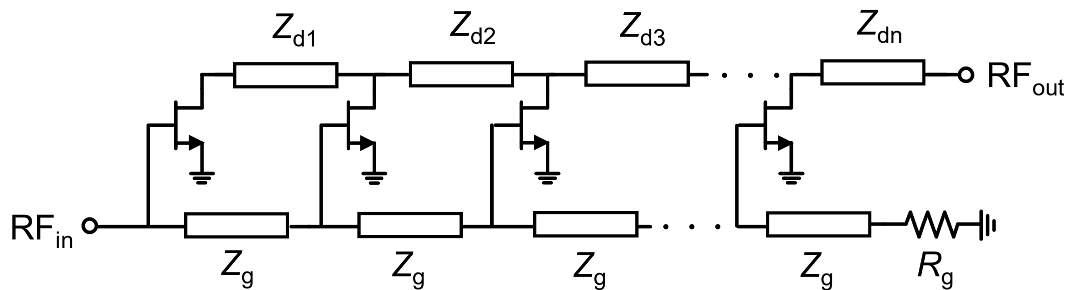


Fig. 2-6. Schematic of the NDPA.

2.2.3 High-efficiency amplifier

Communication traffic is increasing year by year. Power amplifiers are said to account for over 30% of the power consumption of a communication system [22][23]. Higher efficiency is required for the design of low-loss output matching circuits and high efficiency of the transistors. The output matching circuit is particularly important for improving efficiency in amplifier design because losses in circuits other than the output matching circuit only reduce the gain. In contrast, losses in the output matching circuit reduce the saturation output power. The key point is trade-offs of circuit configurations and optimization of the circuit parameters of the output matching circuit. Using GaN transistors with high mobility and high voltage operation effectively improves the efficiency of FET. Owing to the high output power density, the number of FETs and the circuit size can be reduced compared to FETs with other materials, leading to lower circuit loss.

Improvements in the epitaxial structure and optimization of the GaN transistor structure, including gate electrodes are also being made to increase efficiency. The source inductance of the transistor causes a negative feedback effect on the transistor, which causes reduced gain and efficiency. A transistor structure that reduces such parasitic components is desirable.

2.2.4 Low-cost amplifier

GaN transistors are generally fabricated on SiC substrates. Because SiC wafer is expensive, the cost of a GaN power amplifier is higher than GaAs or Si power amplifiers. GaN power amplifiers were initially developed primarily in discrete configurations. For discrete GaN transistors, GaN was only used as FET chips, and impedance matching circuits are designed using microstrip lines on the high-k substrate or chip LC components on PCBs by connecting with bonding wires. However, the presence of bonding wires and

parasitics in chip components made obtaining high-frequency performance and broadband characteristics difficult. To solve these problems, GaN-MMICs have been actively developed in recent years. GaN-MMIC amplifiers have been realized for millimeter-wave and beyond with great performance although the cost is higher. The choice between discrete and MMIC configurations has been based on a trade-off relationship between cost and performance. However, there has been a particularly strong demand for both low cost and high performance, and improvements in devices and circuit configurations are required.

2.3 Silicon quantum dot

2.3.1 Charge state in a quantum dot

A quantum dot (QD) is an artificial system in which electrons (or holes) are confined in zero-dimensional space. The QDs are connected to leads (electron reservoirs) through a tunnel barrier, and electrons or holes are exchanged between the leads and the dots. By connecting the source and drain leads to QD, it is possible to measure the conduction properties of the QDs. As explained in 1.2.4, silicon quantum dots have recently attracted much attention because of their long coherence time. There are gate-defined silicon QD and physically-defined Si QD. A gate-defined QD is electrically formed in 2DEG by applying a voltage to some fine gates. Gate-defined QDs allow fine adjustment of QD potential, but the large number of gates makes integration difficult. Physically-defined QD is formed by etching silicon on an insulator wafer. This structure is advantageous for integration because fewer gates are needed to adjust the quantum dots.

The electrostatic potential in the QD can be modulated relative to the leads by adjusting the voltage applied to the gate electrode electrostatically coupled to the QD. Fig. 2-7 shows the equivalent circuit of a single QD. A tunnel coupling is represented as parallel tunnel resistor and tunnel capacitor and these values vary depending on the potential of the lead and quantum dots. One of the phenomena characteristically observed in such QD systems is called Coulomb oscillation. The conductivity of quantum dots changes periodically with gate voltage and peaks at a specific gate voltage. The phenomenon in which the conductivity is significantly suppressed between current peaks is called the Coulomb blockade. In the following, we discuss the characteristic conduction properties of these quantum dots using the constant interaction model [42]. The constant interaction model is based on the following two assumptions.

1. The Coulomb interaction between one electron in the dot and all other electrons is

given by a constant capacitance C.

2. The energy levels of a single particle can be calculated in terms of discrete energy levels in the absence of interaction between electrons.

The capacitance C in the first assumption is given by $C = C_S + C_D + C_G$ where C_S, C_D, and C_G are the capacitances between the quantum dot and the source, drain, and gate electrodes, respectively. Under these assumptions, the total energy of a QD containing N electrons is

$$U(N) = \frac{(eN - C_D V_D - C_S V_S - C_G V_G)^2}{2C} + \sum_{j=1}^{N} E_n(B) \tag{2-5}$$

where e is a single electron charge, N is the number of electrons in the QD; V_i is the voltage applied to electrode i, and i = D, S, G corresponds to drain, source, and gate. ε_j is j-th eigenenergy of a single-particle Schrödinger equation for the QD confinement.

The electrochemical potential required for adding N-th electron, μ(N), is

$$\mu(N) = U(N) - U(N-1) = \left(N - \frac{1}{2}\right) E_C - \frac{E_C}{e}(C_D V_D + C_S V_S + C_G V_G) + E_N \tag{2-6}$$

where $E_C = e^2/C$, called charging energy. The energy spacing between two sequential electrochemical potentials, referred to as addition energy $E_{add}(N)$, is

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E. \tag{2-7}$$

$E_{add}(N)$ contains the charging energy and the energy spacing $\Delta E = E_{N+1} - E_N$.

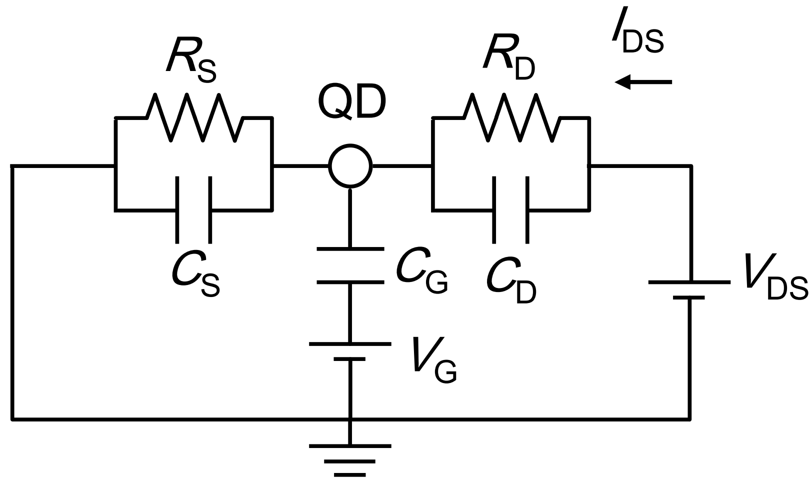


Fig. 2-7. Equivalent circuit of a single QD.

The tunneling current of a quantum dot is determined by the relationship between the dot's electrochemical potential μ(N) of the dot and the electrochemical potentials of the source and drain electrodes (μ_S and μ_D). Applying a bias voltage $V_{SD} = V_D - V_S$ between source and drain opens a bias window with a width of $|eV_{SD}|$, and tunneling current through the QD flows only when the electrochemical potential of the QD is within this window. When $e|V_{DS}| = |\mu_S - \mu_D| \ll E_C, \Delta E_N$, the QD current is only observed when the electrochemical potential μ(N) is within the bias window ($\mu_S \leq \mu(N) \leq \mu_D$). When the electrochemical potential of the QD is outside the bias window, the QD current does not flow and the number of electrons in the dot is maintained. This is called the Coulomb blockade.

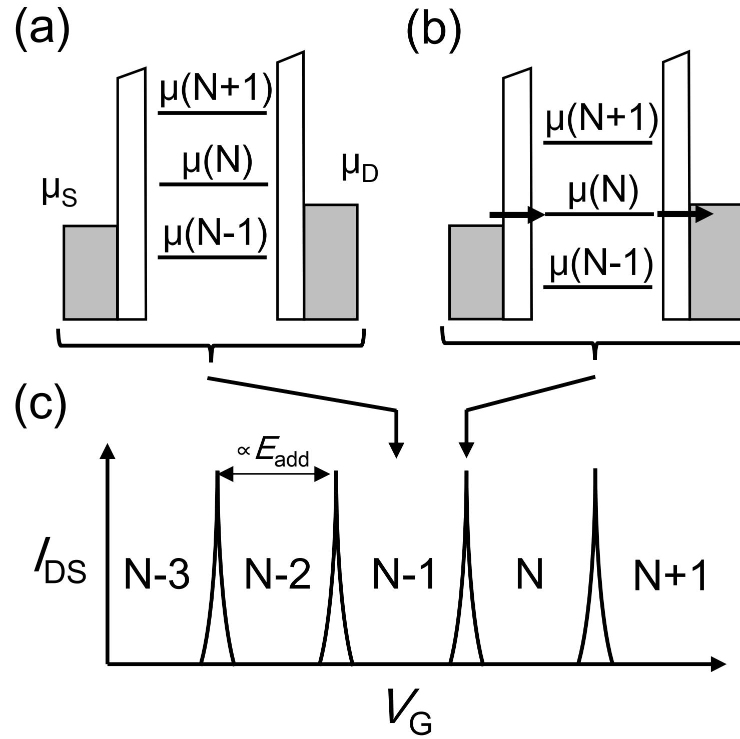


Fig. 2-8. Coulomb oscillation. (a) Electrochemical potentials of a single QD in the Coulomb blockade. (b) Electrochemical potentials of a single QD at a Coulomb peak. (c) Drain-source current (I_{ds}) through QD as a function of gate voltage (V_G)

2.3.2 Charge sensing

Manipulation and readout of electron spin qubits in a QD were performed with a few electrons. In such a state, the current flowing throw the QD is very small, making readout difficult. Therefore, the charge sensing technique was utilized. By placing a charge sensor (CS) QD near of the qubit QD, a CS's I–V characteristics change steeply with respect to the change in the number of electrons in qubit QD. Fig. 2-9 shows the schematic of charge sensing. Fig. 2-9 (a) shows the equivalent circuit of QD and CS QD. QD and CS are capacitively coupled. Fig. 2-9 (b) and (c) shows the drain-source current of QD and CS, respectively. Because the I–V characteristics of CS QD vary steeply with respect to the nearby electric field, when the number of electrons in QD changes, the I–V characteristic

of CS shows “kink”. Spin states in QD can be read out using spin-to-charge-conversion [48][49].

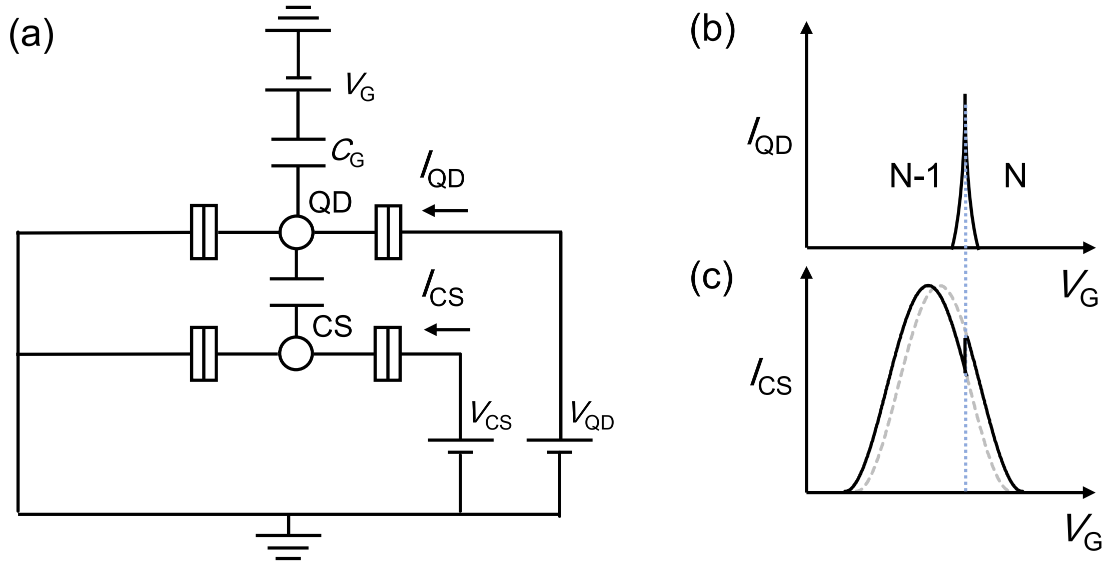


Fig. 2-9. Schematic of charge sensing. (a) Equivalent circuit of QD and CS. (b) Drain-source current of QD. (c) Drain-source current of CS.

2.3.3 RF reflectometry

A fast readout of the spin states is necessary to achieve the quantum-non-demolition spin readout for fault-tolerant quantum computing. However, charge sensing based on I–V measurement is typically slow (the order of kHz [37]), and the sensitivity is limited by $1/f$ noise [38]. Charge sensing using RF reflectometry has been widely studied in QD systems [50]–[53] to solve the problem. Fast spin readout within coherence times was realized in a gate-defined Si/SiGe QD with RF reflectometry using QD CS [50]. In physically-defined QD with fewer gates than gate-defined QD, it is more difficult to adjust tunneling resistance; hence accurate circuit design is more important.

RF reflectometry reads the change in microwave reflection characteristics of the CS QDs. As mentioned earlier, a parallel RC circuit represents the equivalent circuit of the

quantum dot charge sensor. The resistance of the quantum dots is quite high compared to 50 Ω. Therefore, quantum dot's reflection characteristic is almost open. Therefore, the quantum dot chip is connected to an external PCB and a matching circuit with chip components is used for the impedance transformation from 50 Ω to the input impedance of QD at a bias condition. Charge sensing can be achieved by reading the reflection amplitude or phase change when the resistance or capacitance changes. In conventional reflectometry, impedance matching is performed using a chip series inductance and a shunt capacitor (mainly parasitic capacitance of the PCB). In this configuration, the PCB's parasitic shunt capacitance determines the operation frequency and value of inductance. For a QD impedance of several MΩ, the operation frequency is around 100 MHz, and the size of the inductor used in the matching circuit is the order of μH, requiring a large chip inductor. For future frequency multiplexing, it is desirable to have a circuit configuration that enables matching at various frequencies. In addition, for fast readout, it is necessary to have a wideband impedance matching. Changes in the reflectance characteristics of quantum dots are read out as pulsed signals. The required bandwidth is proportional to the inverse of the readout time. Considering QEC, a state fidelity of 99% [32] or more is required. The state fidelity of data qubits is expressed by the following equation

$$e^{-\frac{t}{T_2^H}} \cong 1 - \frac{t}{T_2^H} \tag{2-8}$$

By assuming the dephasing time T_2^H of 130 μs [54], readout time of less than 1.3 μs is required. To achieve that, a bandwidth of 0.77 MHz or more is required for the matching circuit of the RF reflectometry. Considering QEC, the number of matching circuits for the charge sensor also increases; hence it is necessary to downsize the circuit. The application of MMIC technology, which can be made at a higher frequency will be a good solution.

Chapter 3.

GaN-MMIC ultra-wideband bandpass distributed amplifier

There is a need for high-capacity, high-speed communications and base stations that can be shared across frequency bands for multiple generations of communication systems. To meet these demands, microwave amplifiers with a wide bandwidth and high output power are required. As described in Section 2.2.2, there is a trade-off between bandwidth and output power in microwave amplifiers. In this chapter, we propose a bandpass distributed amplifier that improves the tradeoff relationship. We also design and evaluate a wide-bandwidth, high-power bandpass-distributed amplifier with a specific bandwidth of 120% or more in the S-X band, and confirm the effectiveness of the proposed circuit.

3.1 Introduction

HPAs with high efficiency and wide operation bandwidth are in increasing demand for radar or communication systems. GaN high electron mobility transistors (HEMTs) have been utilized in HPAs because of its high power capability. To date, wideband GaN-MMIC HPAs with various circuit configuration have been developed [55]–[71]. NDPAs were proposed to enhance output power and efficiency. Optimum load impedance for each FET is obtained by properly tapered characteristic impedance of “artificial transmission lines” [71]. Utilizing FET cells with large gate width is effective to increase output power of NDPA but cut-off frequency decrease due to large parasitic capacitor of

FETs. In this chapter, bandpass distributed amplifier configuration is applied to NDPAs in order to increase cut-off frequency without reducing gate width of FETs. Two MMIC HPAs are designed and measured. One is a single-ended HPA which achieves output power of 17 to 26 W, PAE of 24 to 44% across 2.5 to 11.0 GHz. The other is a two-way combined HPA which achieves output power of 27 to 61 W, PAE of 24 to 43% across 2.5 to 10.0 GHz. These results demonstrate the highest output power among wideband amplifiers ever reported.

3.2 Theoretical analysis of the artificial line of the distributed amplifier

The advantage and design method of a bandpass NDPA are described here. Fig. 3-1 shows a schematic of a conventional NDPA. Input and output matching circuits of the NDPA have artificial transmission lines composed of inductance of transmission lines and parasitic capacitance of FETs. For simplicity, design method is explained focused on the input circuit. Impedance of each artificial transmission line in the input circuit is the same impedance as the termination resistance. This realizes broadband characteristic overcoming Bode-Fano criterion [72], [73] which restricts the bandwidth of reactively-matched power amplifiers (RMPAs). Although, the bandwidth of a NDPA is limited by cut-off frequency of the transmission lines due to parasitic capacitance of FETs. To discuss bandwidth, cut-off frequency of the artificial transmission lines are calculated. Fig. 3-2 shows the LC circuit which is simplified equivalent circuit of artificial transmission line of the conventional distributed amplifier.

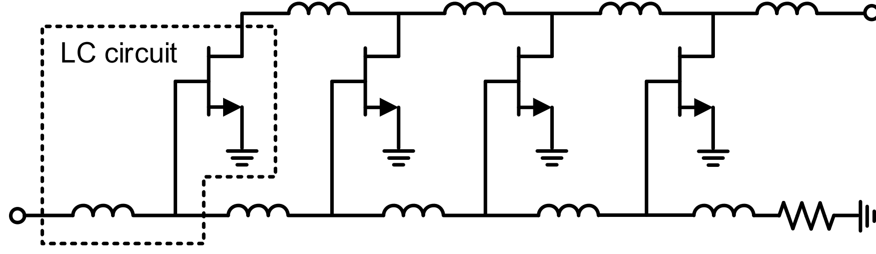


Fig. 3-1. Schematic of a conventional NDPA.

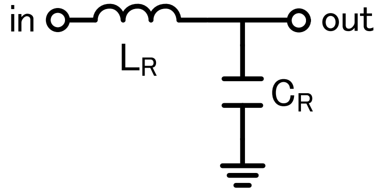


Fig. 3-2. Simple equivalent circuit of unit artificial transmission line (LC circuit)

F-matrix of the LC circuit is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Unit} \equiv \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1 & j\omega L_{\mathrm{R}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{\mathrm{R}} & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1-\omega^2 C_{\mathrm{R}} L_{\mathrm{R}} & j\omega L_{\mathrm{R}} \\ j\omega C_{\mathrm{R}} & 1 \end{bmatrix}. \tag{3-1}$$

When the impedance of input and output ports are Z_0, S_{21} of the LC circuit is

$$S_{21Unit} = \frac{2}{2-\omega^2 C_{\mathrm{R}} L_{\mathrm{R}} + j\omega L_{\mathrm{R}}/Z_0 + j\omega C_{\mathrm{R}} Z_0}. \tag{3-2}$$

By assuming the input port and output port and the characteristic impedance are the same, their relation is given by

$$\mathrm{Z_{in}} = \mathrm{Z_{out}} = \sqrt{\frac{\mathrm{L_R}}{\mathrm{C_R}}}. \tag{3-3}$$

By defining

$$\omega_{se} \equiv \frac{1}{\sqrt{C_R L_R}}, \tag{3-4}$$

Equation (3-2) is derived to

$$S_{21Unit} = \frac{1}{1 - \frac{1}{2}\left(\frac{\omega}{\omega_{se}}\right)^2 + j\frac{\omega}{\omega_{se}}} \tag{3-5}$$

and transmission amplitude is calculated to be

$$|S_{21Unit}| = \frac{1}{\sqrt{\left[1 - \frac{1}{2}\left(\frac{\omega}{\omega_{se}}\right)^2\right]^2 + \left(\frac{\omega}{\omega_{se}}\right)^2}}$$

$$= \frac{1}{\sqrt{1 + \frac{1}{4}\left(\frac{\omega}{\omega_{se}}\right)^4}}. \tag{3-6}$$

Then, 3 dB cut-off frequency of the LC circuit (ω_{LC}) is calculated as follows.

$$\frac{1}{4}\left(\frac{\omega_{LC}}{\omega_{se}}\right)^4 = 1$$

$$\Rightarrow \omega_{LC} = \sqrt{2}\omega_{se} = \sqrt{\frac{2}{C_R L_R}} \tag{3-7}$$

It is shown that cut-off frequency of input circuit is determined by gate-source capacitance of FET (C_R) since L_R is fixed by (1). Therefore, reducing the gate width of the FET and increasing the number of FETs are effective to increase cut-off frequency but this also increases loss and then the efficiency decrease. To avoid this, additional capacitor C_{add} is inserted in series with C_R in conventional NDPA[55] as shown in Fig. 3-3. In this case, 3 dB cut-off frequency is derived to

$$\omega_{LC-} = \sqrt{\frac{2}{\frac{C_R C_{add}}{C_R + C_{add}} L_R}} = \sqrt{\frac{C_R + C_{add}}{C_{add}}}\ \omega_{LC}. \tag{3-8}$$

Equation (3-8) indicates that cut-off frequency can be increased by additional capacitance. Although, gain of FETs decrease because voltage applied to gate-source capacitance is divided. In other words, conventional NDPAs have trade-off relation between gain and cut-off frequency.

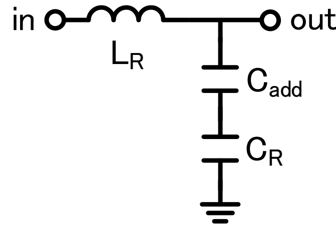


Fig. 3-3. Simple equivalent circuit of unit artificial transmission line (LC circuit with additional capacitor)

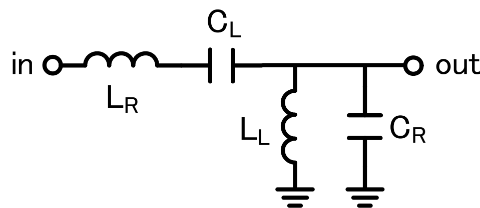


Fig. 3-4 Simple equivalent circuit of unit artificial transmission line of bandpass distributed amplifier

To improve the trade-off relation in the conventional NDPA, bandpass NDPA configuration is proposed. Fig. 3-4 shows a simple equivalent circuit of artificial transmission lines of the bandpass NDPA. In this configuration, gain is not reduced since gate-source voltage is not divided. Cut-off frequency of the bandpass NDPA is also calculated. Coefficient α (>0) is defined as relation between the LC circuit parameters (L_R, C_R) and additional parameters in the bandpass circuit (L_L, C_L).

$$L_L = \alpha L_R, C_L = \alpha C_R. \tag{3-9}$$

By defining

$$\omega_\Gamma = \frac{1}{\sqrt{C_R L_L}} = \frac{1}{\sqrt{\alpha L_R C_R}} = \frac{\omega_{LC}}{\sqrt{2\alpha}}, \tag{3-10}$$

F-matrix of the bandpass circuit is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Unit} \equiv \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1 - \frac{1}{\alpha}\left(\frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}\right)^2 & j\left[\left(\frac{\omega}{\omega_\Gamma}\right)^2 - 1\right]\left(\frac{\omega_\Gamma^2 L_R}{\omega}\right) \\ j\frac{(\omega/\omega_\Gamma)^2 - 1}{\alpha\omega L_R} & 1 \end{bmatrix}. \tag{3-11}$$

By assuming that the input port, the output port and characteristic impedance Z_0, S_{21} of the bandpass circuit is calculated as

$$S_{21Unit} = \frac{1}{1 - \frac{1}{2\alpha}\left(\frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}\right)^2 + \frac{j}{2}\left(\frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}\right)\left(\frac{\omega_\Gamma L_R}{Z_0} + \frac{Z_0}{\alpha\omega_\Gamma L_R}\right)}. \tag{3-12}$$

By assuming the characteristic impedance of bandpass circuit is also Z_0,

$$Z_0 = Z_{in} = Z_{out} = \sqrt{\frac{L_R}{C_R}} = \sqrt{\frac{L_L}{C_L}}. \tag{3-13}$$

From (2-10) and (2-13),

$$\frac{\omega_\Gamma L_R}{Z_0} = \frac{1}{\sqrt{L_R C_L}}\sqrt{\frac{C_R}{L_R}}L_R = \sqrt{\frac{C_R}{C_L}} = \frac{1}{\sqrt{\alpha}} \tag{3-14}$$

By substituting (2-14) to (2-12),

$$\frac{1}{1 - \frac{1}{2\alpha}\left(\frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}\right)^2 + j\frac{1}{\sqrt{\alpha}}\left(\frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}\right)}$$

$$= \frac{1}{1 - \frac{\chi^2}{2\alpha} + j\frac{\chi}{\sqrt{\alpha}}} \tag{3-15}$$

where

$$\chi \equiv \frac{\omega}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega}. \tag{3-16}$$

Then transmission amplitude is calculated to be

$$|S_{21Unit}| = \frac{1}{\sqrt{\left(1-\frac{\chi^2}{2\alpha}\right)^2 + \left(\frac{\chi}{\sqrt{\alpha}}\right)^2}} = \frac{1}{\sqrt{1+\frac{\chi^4}{4\alpha^2}}} \tag{3-17}$$

Then, 3 dB cut-off frequency ω_c is calculated as follows.

$$\frac{\chi|_{\omega=\omega_C}^4}{4\alpha^2} = 1 \Leftrightarrow \left(\frac{\omega_c}{\omega_\Gamma} - \frac{\omega_\Gamma}{\omega_c}\right)^2 = 2\alpha \tag{3-18}$$

From (2-10) and (2-17), when $\omega_c > \omega_\Gamma$,

$$\omega_c^2 - \sqrt{2\alpha}\omega_\Gamma\omega_c - \omega_\Gamma = 0$$

$$\Rightarrow \omega_c = \frac{\sqrt{2\alpha+4}+\sqrt{2\alpha}}{2}\omega_\Gamma = \frac{1}{2}\left(\sqrt{1+\frac{2}{\alpha}}+1\right)\omega_{LC} \equiv \omega_{c+} \tag{3-19}$$

When $\omega_c < \omega_\Gamma$,

$$\omega_c^2 - \sqrt{2\alpha}\omega_\Gamma\omega_c - \omega_\Gamma = 0$$

$$\Rightarrow \omega_c = \frac{\sqrt{2\alpha+4}-\sqrt{2\alpha}}{2}\omega_\Gamma = \frac{1}{2}\left(\sqrt{1+\frac{2}{\alpha}}-1\right)\omega_{LC} \equiv \omega_{c-}. \tag{3-20}$$

(19) indicates that the bandpass circuit has lower cut-off frequency (ω_{c-}) and higher cut-off frequency (ω_{c+}). It is shown that the higher cut-off frequency is higher than that of LC circuit since $\alpha > 0$. From (3-19) and (3-20),

$$\omega_{c+} - \omega_{c-} = \omega_{LC}. \tag{3-21}$$

(3-21) indicates that a total bandwidth of the bandpass circuit and the conventional LC circuit are the same. It is apparent that higher cut-off frequency of the bandpass circuit is higher than that of LC circuit by the bandwidth of the lower-cut off frequency. Fig. 4 shows transmission characteristics of LC circuit and bandpass circuit. In actual design, conventional NDPAs with LC circuit configuration has lower cut-off frequency due to the

limitation of realizable on-chip DC-cuts and choke inductors on MMIC. In addition, lower frequency region is usually stabilized to avoid unwanted oscillation. By applying the bandpass amplifier configuration, the bandwidth of wasted lower frequency region can be shifted to increase higher cut-off frequency.

How to determine parameters of bandpass NDPA by modifying already designed conventional LC circuit is described. By solving (3-20) for α, α is given by

$$\alpha = \frac{2}{\left(\frac{2\omega_{c-}}{\omega_{LC}} + 1\right)^2 - 1} = \frac{1}{2A(A+1)}, A \equiv \frac{\omega_{c-}}{\omega_{LC}} \tag{3-22}$$

By determining lower cut-off frequency, A and then the design parameter α is obtained from (3-22). When $\omega_{c-} \rightarrow 0$ ($A \rightarrow 0$), it is apparent that $\alpha \rightarrow \infty$ where the circuit is equivalent to the conventional LC circuit. This means that (3-22) is applicable to the design of conventional LC circuits. Fig. 3-5 shows the relation between α and A.

This design method can be also applied to the output matching circuit by considering C_R as drain-source capacitance.

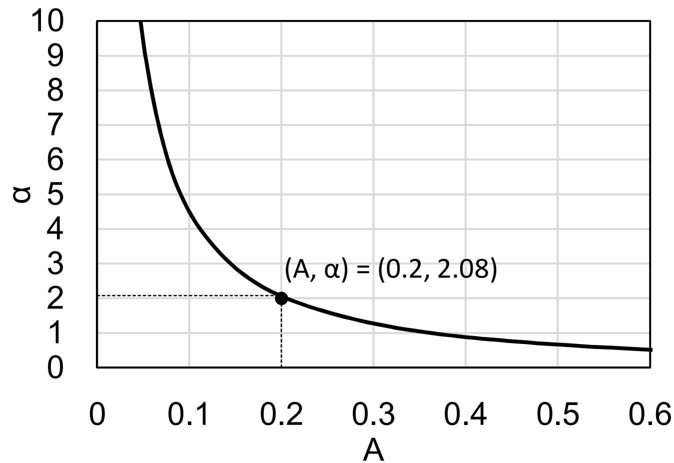


Fig. 3-5. Relation between α and A.

3.3 Design and measurement results of single-ended GaN-MMIC HPA

Two MMIC HPAs are designed utilizing 0.25 μm GaN HEMT technology on 100 μm thick silicon carbide (SiC) substrate based on proposed design method. One is a single-ended bandpass NDPA. Fig. 3-6 shows a schematic diagram of the single-ended bandpass NDPA. 4 FET cells are utilized. Gate peripheries of the FET1–4 are 1.0 mm, 0.7 mm, 0.6 mm, 0.5 mm respectively. Bandpass artificial transmission lines are applied to the FET1 and the FET4 to make the chip size compact. Another advantage of the bandpass NDPA is that each shunt-inductor can be used as a bias circuit. In case of the conventional NDPA, unnecessary inductance of bias circuit degrades the performance.

The other is a HPA realized by combining two single-ended HPAs in parallel. Fig. 3-7 shows the schematic of the two-way combined NDPA. Combiner is composed of 70.7- Ω transmission line transformers with the electrical length of λ/4 at the frequency of slightly higher than the center frequency to compensate lower gain at high frequency.

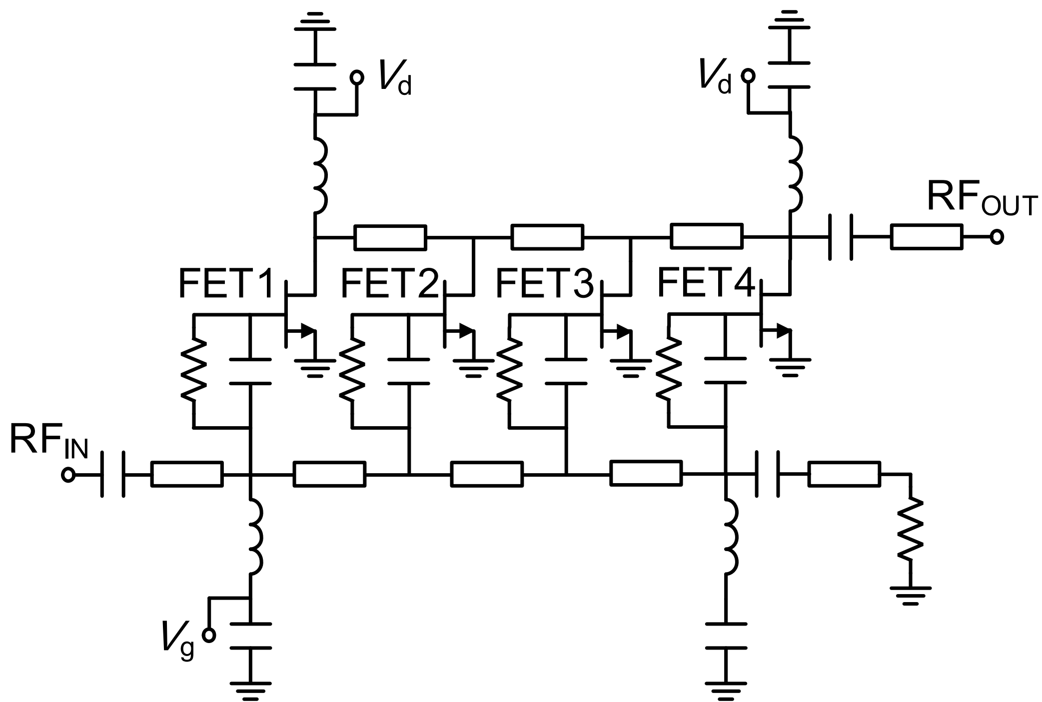


Fig. 3-6. Schematic diagram of a bandpass NDPA.

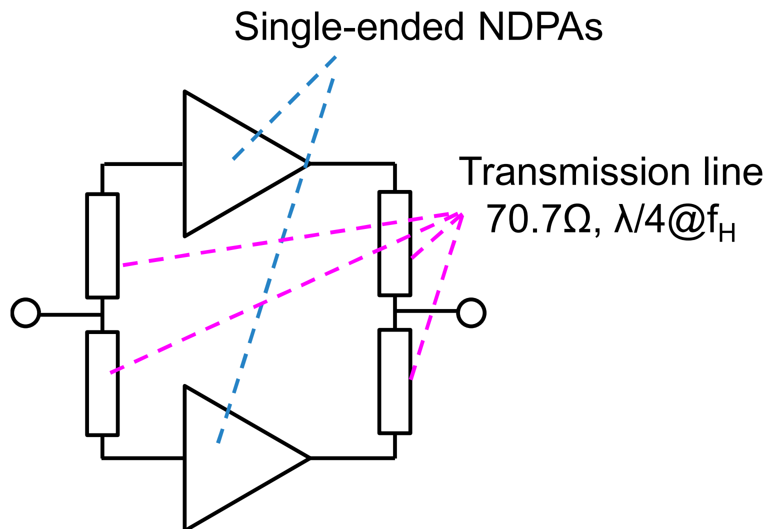


Fig. 3-7 Schematic of the two-way combined NDPA

Fig. 3-8 shows the fabricated single-ended GaN-MMIC HPA. The chip size is 2.8 × 1.5 mm^2. The developed single-ended GaN-MMIC HPA is measured in small-signal and large-signal conditions. Fig. 3-9 shows measured S-parameters of the single-ended GaN-

MMIC HPA. Measurements are performed at a DC drain voltage of 50 V and quiescent drain current of 50 mA. The small-signal gain is greater than 12 dB over 2.5 to 11.0 GHz. Input and output return loss is greater than 6.4 dB and 9.6 dB, respectively.

Large-signal measurement of the single-ended GaN-MMIC HPA is performed under pulsed gate bias conditions with pulse duty-cycle of 10%. Fig. 3-10 shows measured saturated output power (P_{out}) and PAE of the developed single-ended GaN-MMIC HPA as a function of frequency. The output power of 42.2 to 44.1 dBm (17 to 26 W, 20 W on average), the PAE of 24 to 44% (35% on average) at input power of 35.5 dBm over 2.5 to 11.0 GHz are achieved.

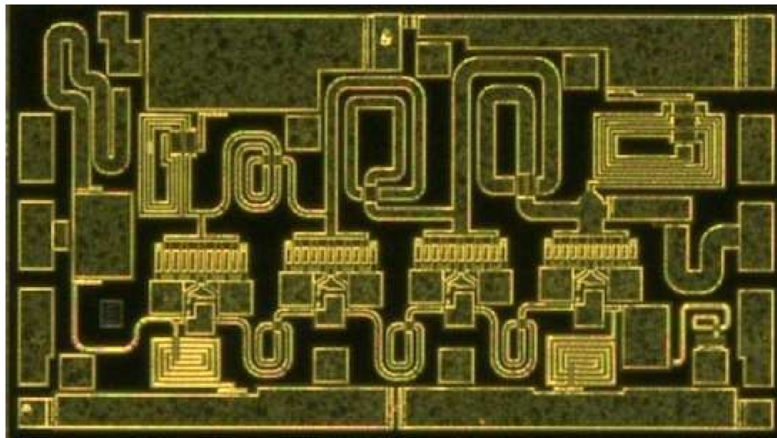


Fig. 3-8. Photograph of the developed GaN-MMIC NDPA

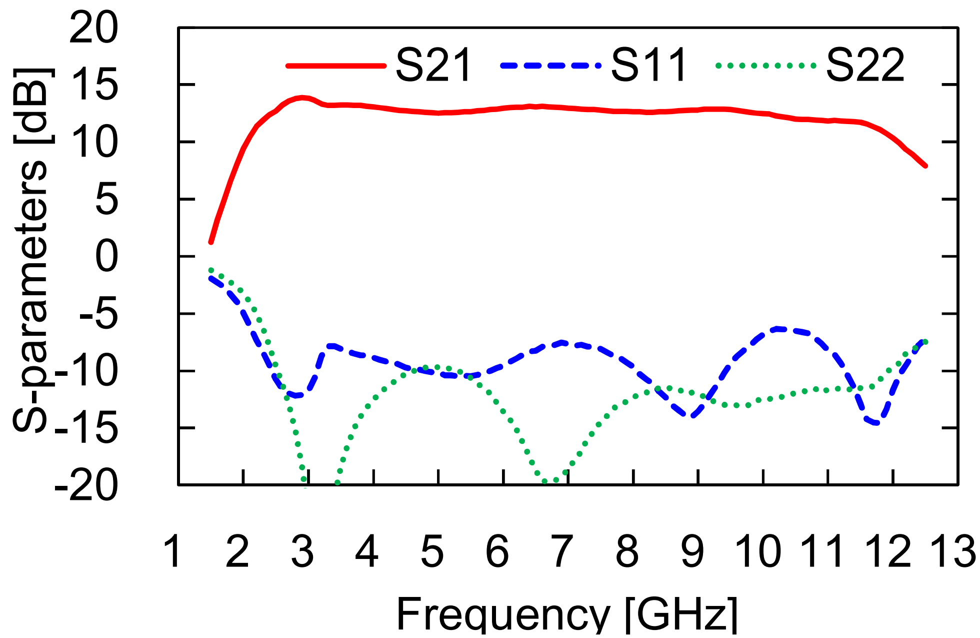


Fig. 3-9. Measured S-parameters of the single-ended GaN-MMIC NDPA

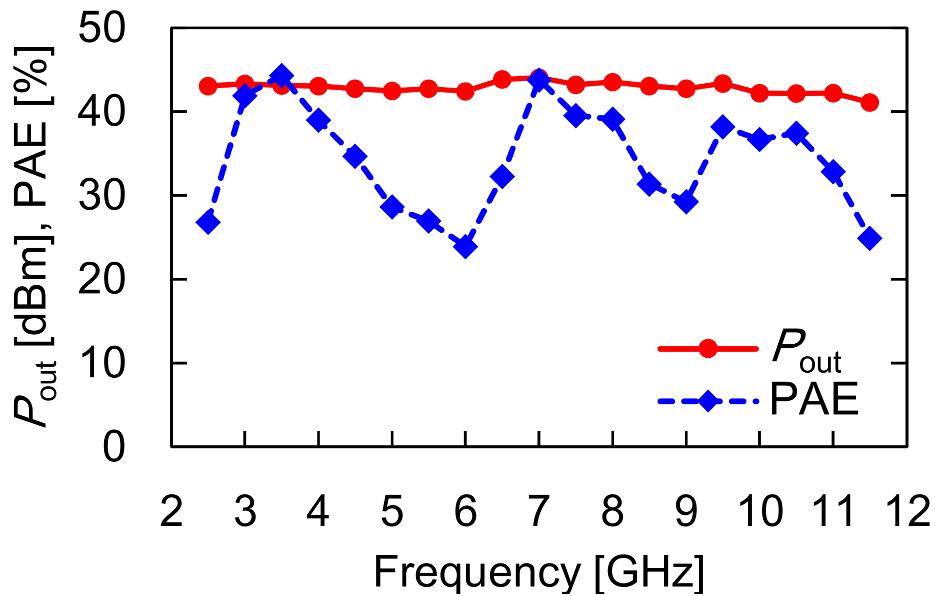


Fig. 3-10. Measured output power and PAE of the single-ended GaN-MMIC HPA

The developed two-way combined GaN-MMIC HPA is measured in small-signal and large-signal conditions. Fig. 3-11 shows the fabricated two-way combined GaN-MMIC HPA. The chip size is 3.2 × 3.0 mm^2. Fig. 3-12 shows measured S-parameters.

Measurements are performed at a DC drain voltage of 50 V and quiescent drain current of 50 mA. The small-signal gain is greater than 11 dB over 2.5 to 10 GHz. Input and output return loss is greater than 4.7 dB and 6.6 dB, respectively.

Large-signal measurement of the two-way combined GaN-MMIC HPA is performed under pulsed gate bias conditions with pulse duty-cycle of 10%. Fig. 3-12 shows measured saturated output power and PAE of the developed two-way combined GaN-MMIC HPA as a function of frequency. Output power of 44.3 to 47.9 dBm (27 to 61 W, 40 W on average), PAE of 24 to 43% (31% on average) at input power of 38 dBm over 2.5 to 10.0 GHz are achieved. Table 3-1 summarizes the performance comparison to other broadband MMIC power amplifiers. It shows that the developed amplifier demonstrates the largest output power and power density. Great performance considering combination of output power and PAE compared to broadband MMIC amplifier ever reported is obtained.

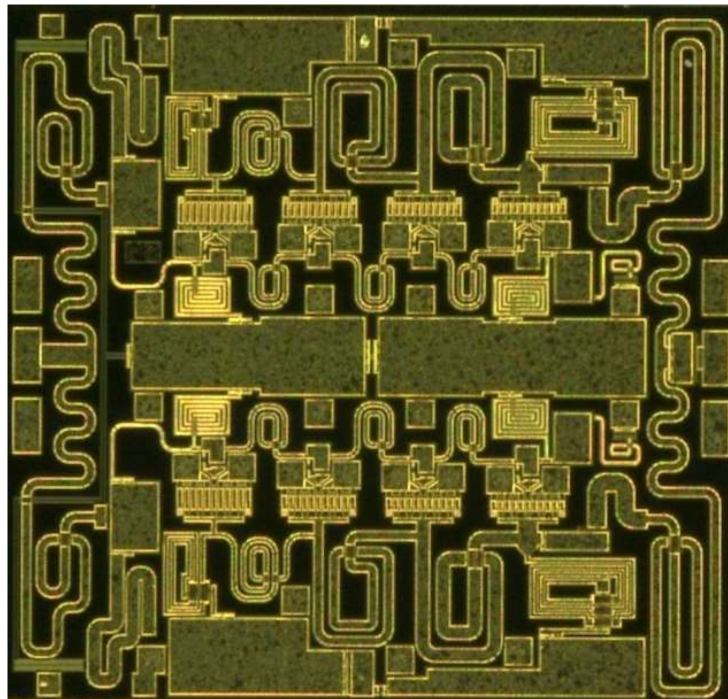


Fig. 3-11. Photograph of the two-way combined GaN-MMIC NDPA

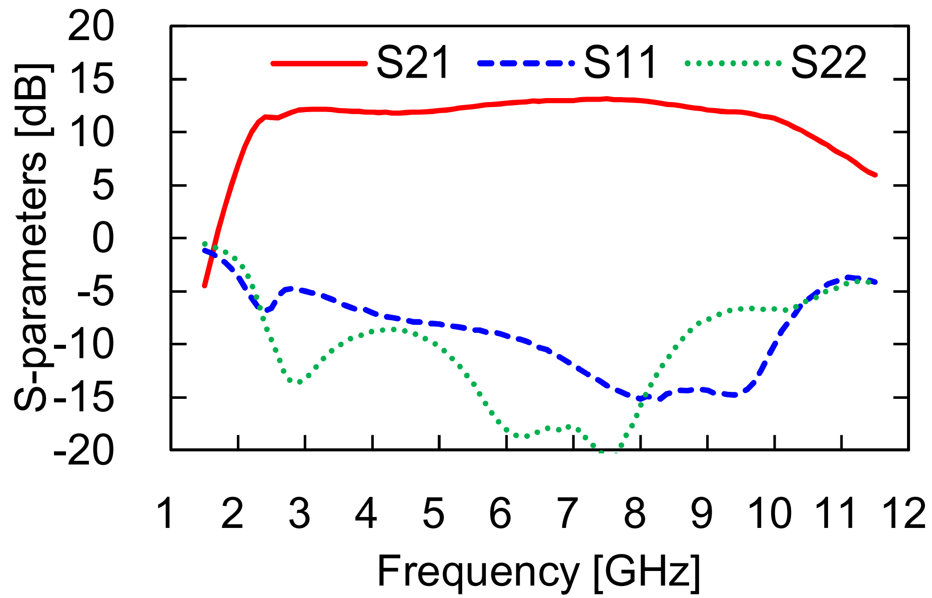


Fig. 3-12. Measured S-parameters of the two-way combined GaN-MMIC HPA.

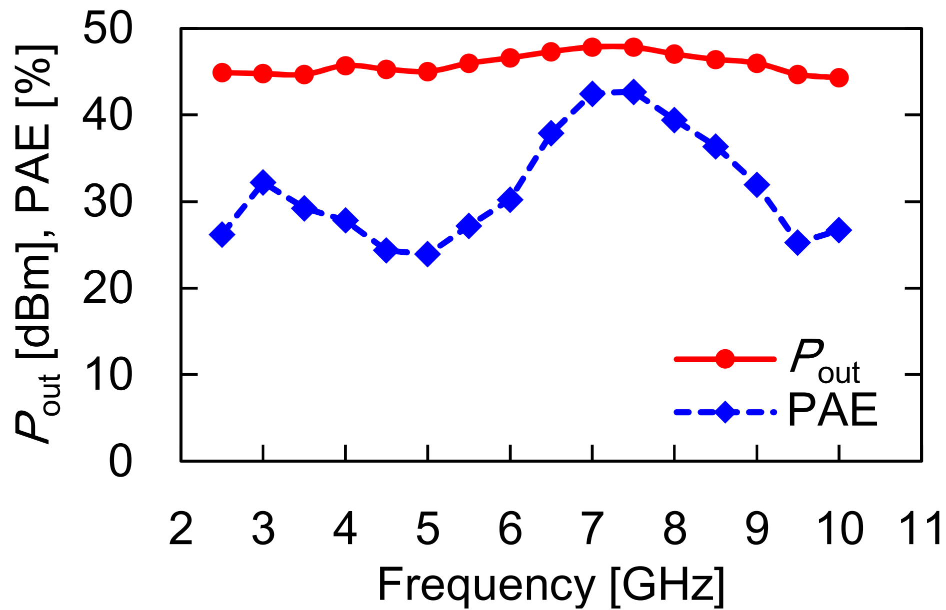


Fig. 3-13. Measured output power and PAE of the two-way combined GaN-MMIC HPA.

Table 3-1. Performance comparison to other state-of-the-art broadband MMIC high power amplifiers

Refs.	Frequency [GHz]	Output power [W]	PAE [%]	Area [mm^2]	Power density [W/mm^2]	Circuits
[55]	1.5 – 17	9 – 15	20 – 38	15.3	0.58 – 0.98	NDPA
[56]	2 – 20	10 – 21	15 – 36	38	0.26 – 0.56	2-way NDPA
[57]	2 – 20	18 – 20	18 – 40	N/A	–	RMPA
[58]	2 – 18	9.1 – 15.8	18 – 38	7	1.3 – 2.3	NDPA
[59]	1 – 8	9 – 13	29 – 48	11.4	0.81 – 1.15	NDPA
[60]	1 – 7	14 – 27	26 – 44	47.4	0.29 – 0.57	2-way NDPA
[61]	2.5 – 10.5	18 – 37	19 – 40	20	0.89 – 1.86	RMPA
[62]	2.0 – 18.0	9.1 – 15.8	18.3 – 38.1	7.0	1.3 – 2.26	NDPA
[63]	2.0 – 20.0	18.0 – 30.8	18.0 – 29.7	25.8	0.70 –1.19	2-way NDPA
This work	2.5 – 11.0	17 – 26	24 – 44	4.2	3.9 – 6.1	Bandpass NDPA
	2.5 – 10.0	27 – 61	24 – 43	9.6	2.8 – 6.4	Bandpass 2-way NDPA

3.4 Conclusion

Bandpass NDPA to achieve high power and wide bandwidth is proposed. Two bandpass NDPAs are developed and measured. One is a single-ended HPA which demonstrates output power of 17 to 26 W, PAE of 24 to 44% across 2.5 to 11.0 GHz (relative bandwidth of 126%) with chip size of 4.2 mm^2. The other is a two-way combined HPA which demonstrates output power of 27 to 61 W, PAE of 24 to 43% across 2.5 to 10.0 GHz

(relative bandwidth of 120%) with chip size of 9.6 mm^2. These results demonstrate highest output power and power density among wideband amplifiers ever reported. We have realized design technology for wideband, high-power amplifiers with relative bandwidths exceeding 120% which enable base station for high-capacity, high-speed communication, or multipurpose radars. Although the developed amplifier is out of the sub-6 frequency, this technology can be scaled to lower frequencies. The target specific bandwidth of 143% mentioned in section 2.2.2 has not been achieved, and further bandwidth expansion is needed. The maximum PAE of the developed amplifier is 43%. In conventional narrowband amplifiers, the backoff PAE is about 40% [65]. Although the developed amplifier has a lower backoff PAE than 43%, the envelope tracking technique allows the amplifier to maintain its efficiency during backoff. When the efficiency of the power modulator used for envelope tracking is 78% [66], the backoff PAE is estimated to be about 33%. It is basically difficult to achieve the same efficiency in a wideband as a narrowband amplifier, but efforts must be made to get close enough to enable simple replacement. Improving the efficiency is important and will be discussed in Chapter 4. This circuit configuration allows the cutoff frequency to be changed as described in 3.2, and expansion to various frequencies can be realized within the frequency range in which the FET can be operated.

Chapter 4.

GaN-MMIC high-efficiency high power amplifier using individual source via structure

It is said that more than 30% of the power consumption of communication systems is due to power amplifiers [22][23], and high efficiency HPAs is strongly required. GaN transistors are widely used as high-efficiency HPAs in communication base stations, communication satellites, radars and so on. Comb electrode structure with gate fingers between multiple source and drain fingers is typically used for high-power amplifiers. In the conventional FET structure, the gain and efficiency characteristics deteriorate at higher frequencies due to parasitic resistance and inductance in the transmission line from the source finger to the via hole. In this chapter, high efficiency GaN-MMIC HPA using the FET with ISV structures [85] is used to solve this problem. The ISV structure has fine via holes in each source finger section, which has low source resistance and inductance to improve gain and efficiency characteristics.

4.1 Introduction

T/R modules have been widely used in radar, satellite communications, base stations for mobile communication systems, and other applications. To lower the cost and increase versatility, the size of these systems must be reduced. Accordingly, the heat problem is getting more serious. As HPAs are one of the most power-consuming components in T/R modules, there is a high demand for an HPA of a compact size and with a lower power

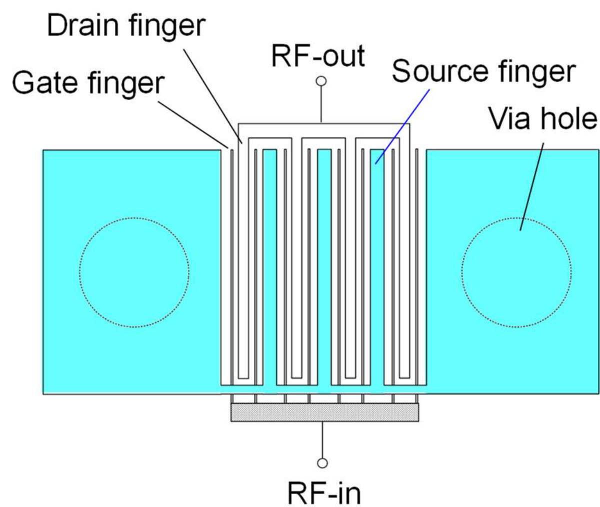
consumption. GaN HEMTs on SiC substrates are promising candidates for solving these issues of HPA because of their high-power capabilities and high-efficiency characteristics. To obtain a compact size and high performance, monolithic microwave integrated circuits (MMICs) are becoming more common recently. To date, many X-band GaN-MMIC HPAs with a high output power and efficiency have been reported [75]–[85].

In this study, a high-efficiency X-band GaN-MMIC HPA has been designed and measured. A design technique for an output-matching circuit to obtain high power and efficiency characteristics considering the relation between the optimum load impedance and loss is described. Measured performance shows an output power of 46.1–47.4 dBm (41–56 W), a power added efficiency (PAE) of 49–55% and a gain of 10.1–11.0 dB at 8.5–10.5 GHz, which are obtained with a drain voltage of 30 V. Output power of 47.2–48.4 dBm (53–70 W), PAE of 52–54%, and gain of 11.2–12.1 dB are obtained at the frequency 8.5–10.5 GHz with a drain voltage of 35 V. The developed GaN-MMIC HPA achieves the highest performance in terms of combination of saturated output power and efficiency compared to existing state-of-the-art X-band GaN-MMIC HPAs.

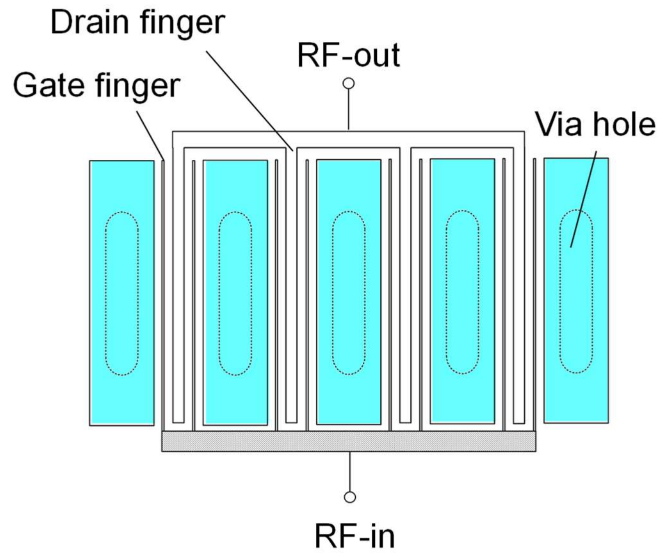
4.2 Individual source via structure

Improvement of transistor structure and optimization of circuit design are important to achieve high efficiency. The ISV structure [86] has been applied to improve the transistor structure, which is described below. Fig. 4-1 shows the schematic of FET structures. Fig. 4-1(a) shows the conventional FET structure. Comb electrode structure with gate fingers between multiple source and drain fingers is typically used for high-power amplifiers. RF signals are distributed from the RF input port to the multiple gate fingers, each of which amplifies the RF signal and outputs it through the drain fingers to the RF output port. Source fingers are bundled and connected to via holes on both sides of the FET. In this

conventional structure, the gain and efficiency characteristics deteriorate at higher frequencies due to parasitic resistance and inductance in the transmission line from the source finger to the via hole. The ISV structure is used to solve this problem. Fig. 4-1(b) shows the FET with ISV structure. The ISV structure has fine via holes in each source finger section, which has the effect of reducing parasitic resistance and inductance of the source and improving gain and efficiency characteristics. Although the structure with smaller vias holes on both sides is effective in reducing inductance, the effect of the ISV structure is dominant because the inductance of the source fingers and drawer lines is more significant. Such structures had been studied earlier in silicon with a structure called TSV structure, but it was difficult to form via holes in small source fingers because of the difficulty of micro-etching in SiC, the substrate of GaN. Fabrication proves of the ISV was made possible by a process using metal masks. In this study, FETs with ISV structure could be fabricated by improving the process, an amplifier design was conducted using them.



(a) Conventional FET structure



(b) FET with ISV structure

Fig. 4-1. Schematic of FET structures

4.3 GaN HEMT characteristics

Mitsubishi's 0.15-μm GaN-MMIC is fabricated. The process technology has an AlGaN/GaN HEMT epitaxial layer with an AlN spacer, which improve the electron mobility, grown on a 50-μm-thick SiC substrate. Typical DC characteristics of the FET are I_{max} = 1.37 A/mm, gate-drain breakdown voltage exceeding 160 V at I_{gd} = 1 mA/mm and three terminal breakdown voltage at pinch-off exceeding 160 V. An individual source via (ISV) structure [86] is employed to reduce source inductance. Fig. 4-2 shows measured load-pull contour of a 10 × 100 μm GaN FET. The measurement is implemented at 10 GHz, a drain voltage of 30 V, a quiescent drain current density of 50 mA/mm, a pulse width of 100 μs and a pulse duty-cycle of 10%. Fig. 4-3 shows measured output power, PAE and gain of the GaN FET. The source and the load impedances are tuned to the PAE maximum impedance in the power sweep measurement and a saturated output power of 37.3 dBm, a PAE of 73%, and an associated gain of 14 dB are obtained. The

improvement due to the ISV structure is estimated to be about 2 dB gain and 2% PAE from the large signal model.

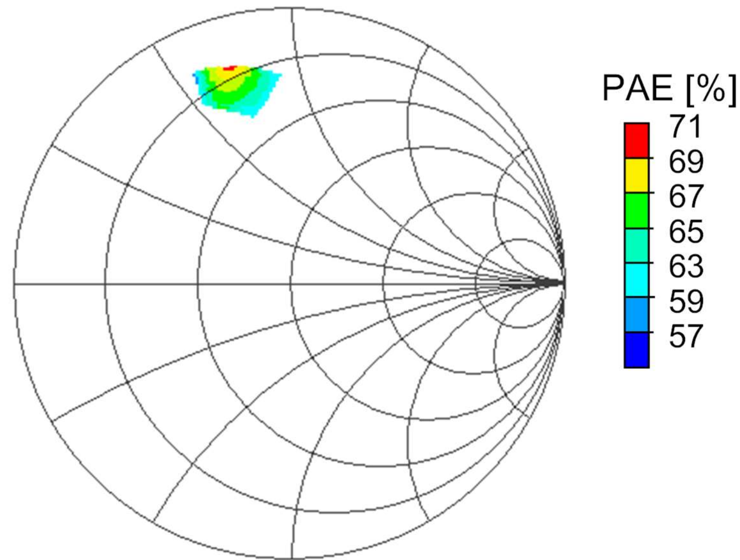


Fig. 4-2. Measured load-pull contour of the GaN FET.

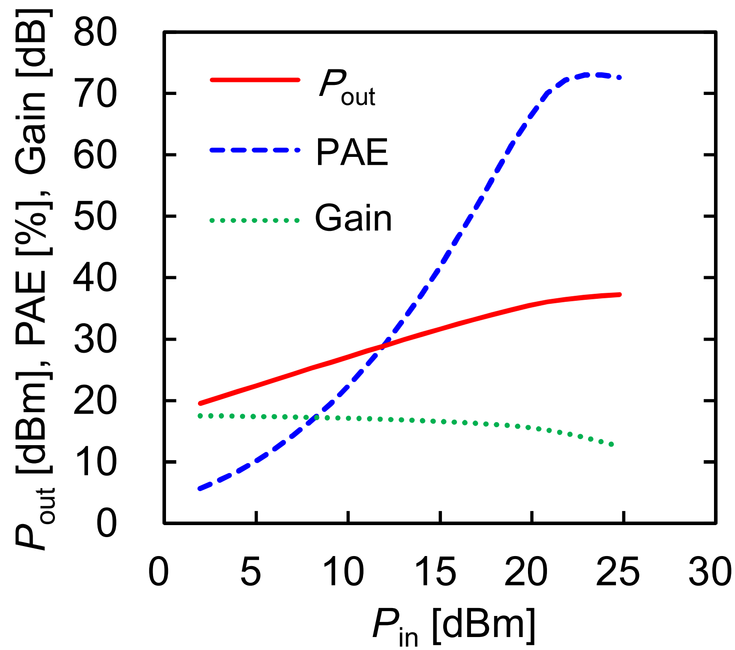


Fig. 4-3. Measured output power, PAE and gain of the GaN FET.

4.4 Design of GaN-MMIC HPA

The design targets of a GaN-MMIC HPA are an output power of 40 W, a gain of over 10 dB, and a PAE of higher than 50% over 8.5–10.5 GHz. To achieve these targets, single-stage amplifiers with eight-unit-cell FETs with a gate width of 10 × 100 μm are utilized. The total gate periphery is 8 mm. The design of GaN-MMIC HPA to obtain this wideband high-output-power and high-efficiency characteristics is shown in detail. Fig. 4-4 illustrates a schematic of the GaN-MMIC HPA. Half of the circuit is shown, and the other half is symmetric to the part shown. Fig. 4-5 shows the impedances seen from the part of the output matching circuit of GaN-MMIC HPA indicated in Fig. 4-4 and the optimum load impedances for PAE and the output power for 8.5–10.5 GHz. Each impedance, Z_0, Z_1, Z_2, Z_3 and Z_4, shown as red line in Fig. 4-5 corresponds to the impedance seen from the part of the circuits indicated in Fig. 4-4 for 1-cell FET. The optimum load impedance, PAE maximum impedance, and output power maximum impedance are shown as a blue dashed line and a green dashed line. They are conjugate to an equivalent parallel RC network derived from the load-pull measurement results. The arrows indicate the direction from low frequency to high frequency. The impedance transformation is explained using Fig. 4-4 and Fig. 4-5. Since eight FETs are symmetrically combined, 50 Ω termination (Z_0) seen from 1-cell FET is 400 Ω. Therefore, impedance transformation from 400 Ω to the optimum load impedance is required. From the output port, a DC cut capacitor, a shunt capacitor, transmission lines, shunt inductors, which are also utilized as drain bias circuits and transmission line combiners, are placed, as shown in Fig. 4-4. First, the shunt capacitor and the transmission line transform 400 Ω (Z_0) to a lower real impedance (Z_2) at the center frequency, as shown in Fig. 4-5. This impedance transformation can also be done by a λ/4 wavelength transmission line but the

combination of a shunt capacitor and a transmission line realizes a comparable transformation in a more compact area. The shunt inductors and series transmission line combiners transform the impedance from Z_2 to Z_4. By carefully choosing the lengths of the shunt inductors and the series transmission lines, either PAE maximum impedance or output power (P_{out}) maximum impedance can be achieved. Two circuits are designed to obtain either PAE maximum impedance or P_{out} maximum impedance and their losses are compared. Fig. 4-6 shows the losses of the output matching circuits used to obtain PAE maximum impedance or P_{out} maximum impedance. The loss of the output matching circuit used to obtain PAE maximum is larger by 0.1 dB than that of the circuit used to obtain Pout maximum. As this increase in loss reduces the merit of the maximum PAE impedance, the circuit with the maximum Pout impedance is chosen as the design target. To compensate for the higher loss at the edge of the operation frequency, the circuit is designed to provide better matching at the edge of the operation frequency. Harmonic impedance is not considered in the design because the dependence of the harmonic impedance was confirmed to be negligibly small in the operation frequency by simulation. The input matching circuit is composed of shunt R-L with DC cut capacitors, which are utilized as gate bias circuits and stabilization circuits, three high-pass and two low-pass impedance transformers. Resistors are placed between each FET to avoid odd-mode oscillation and to realize gate biasing to all FETs. The simulated gate current at saturation is confirmed to be small enough not to affect the RF characteristics. DC-decoupling capacitor is necessary at the input port of the HPA if the output port of the previous device is not DC-decoupled.

Fig. 4-7 shows a photograph of the fabricated X-band GaN-MMIC HPA. The chip area is 3.75 mm × 3.25 mm. A compact design is achieved compared with reported HPAs with a similar output power.

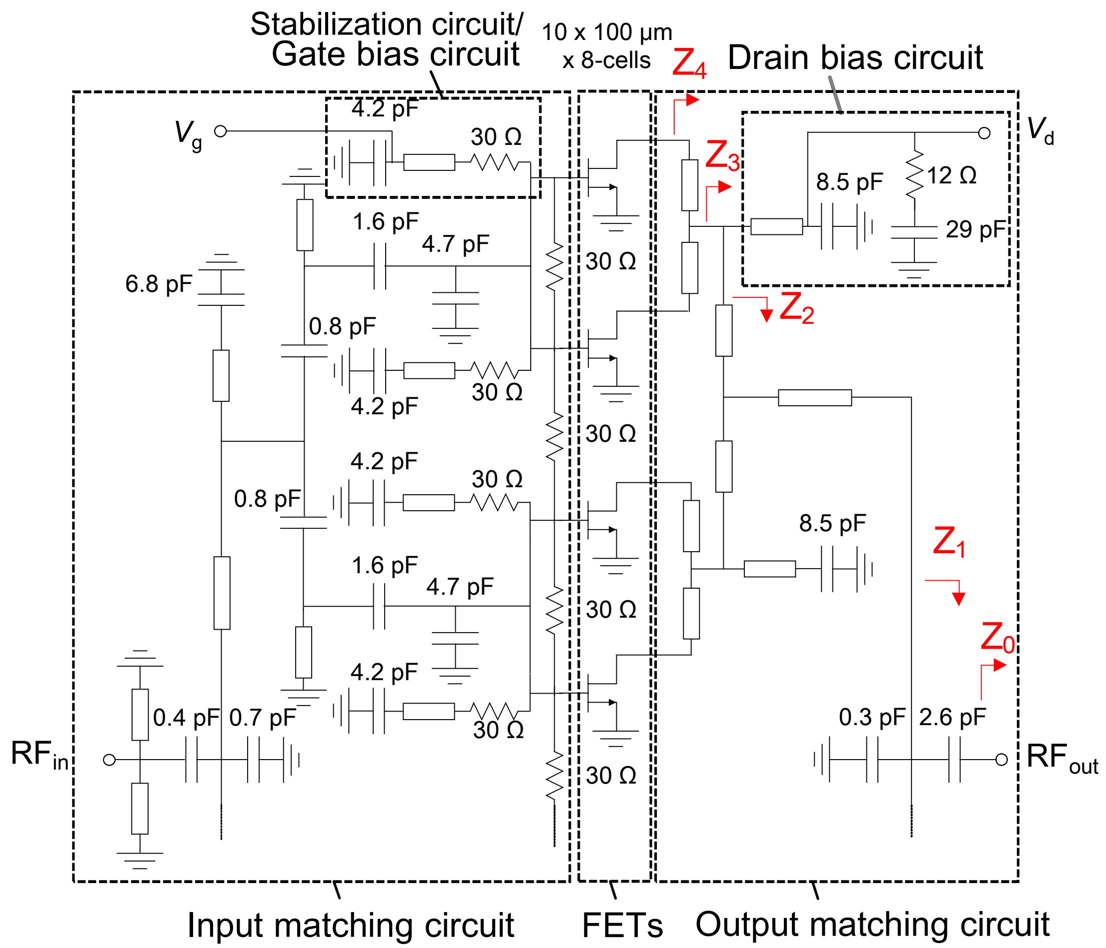


Fig. 4-4. Schematic of the GaN-MMIC HPA. Half of the circuit is shown, and the other half is symmetric to this part.

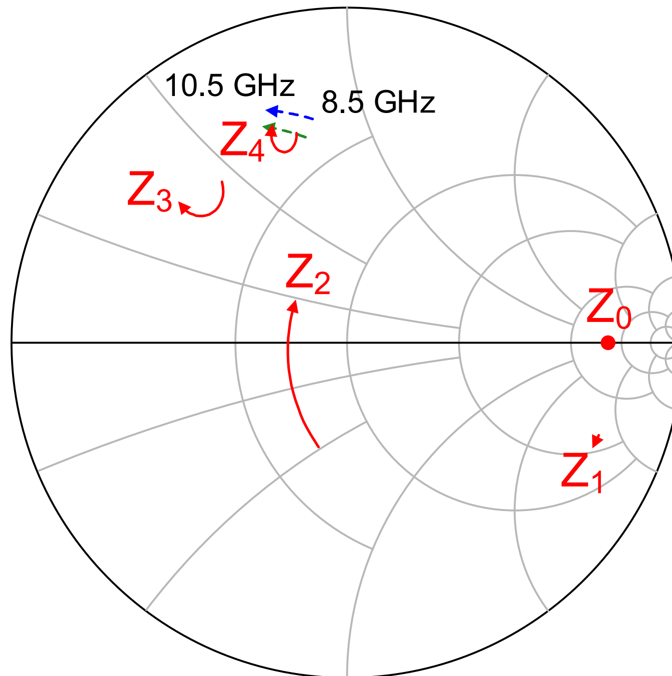


Fig. 4-5. Impedance of the output matching circuit for 1-cell FET and simulated optimum load impedance of 1- cell FET for 8.5–10.5 GHz.

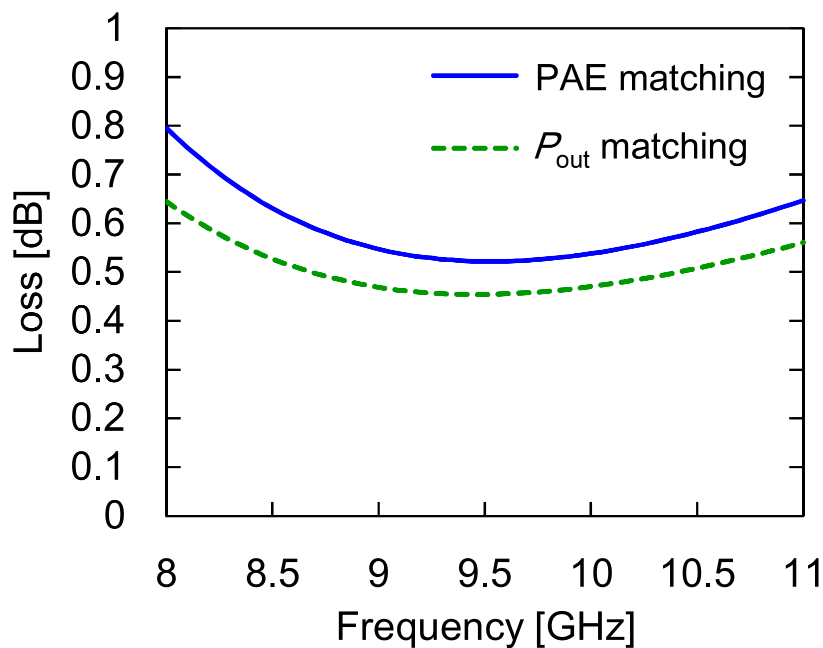


Fig. 4-6. Losses of the output matching circuits used to obtain maximum PAE and maximum output power.

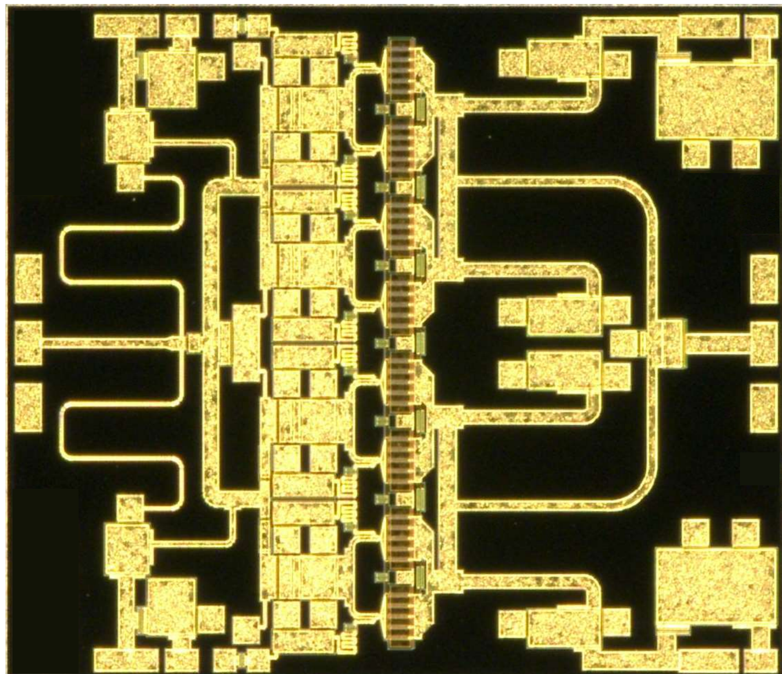


Fig. 4-7. Photograph of developed GaN-MMIC HPA.

4.5 Measurement results

Small- and large-signal measurements of the fabricated GaN-MMIC HPA are performed. The measurement conditions are a quiescent drain current density of 50 mA/mm, a pulse width of 100 μs, and a pulse duty-cycle of 10% at the ambient temperature of 25℃. Fig. 4-8 shows the measured s-parameters of the GaN-MMIC HPA with a drain voltage of 30 V. A linear gain of 12.9–13.8 dB and an input return loss of larger than 5.2 dB over 8.5–10.5 GHz is obtained. Fig. 4-9 shows the measured output power, PAE and gain of the developed GaN-MMIC HPA as a function of input power with a drain voltage of 30 V. The maximum output power of 47.4 dBm and PAE of 55% are obtained at 8.5 GHz. Frequency dependence is measured with a drain voltage of 35 V in addition to 30 V to confirm power capability. Fig. 4-10 shows the measured saturated

output power, PAE, and associated gain as a function of frequency. Output power of 46.1–47.4 dBm (41–56 W), PAE of 49–55%, and gain of 10.1–11.0 dB are obtained at 8.5–10.5 GHz with a drain voltage of 30 V. Output power of 47.2–48.4 dBm (53–70 W), PAE of 52–54%, and gain of 11.2–12.1 dB are obtained at 8.5–10.5 GHz with a drain voltage of 35 V. Broadband high-power and high-efficiency characteristics are obtained. Output power density of 3.3–4.5 W/mm^2 for a drain voltage of 30 V and 4.3–5.7 W/mm^2 for 35 V are obtained. Power density over gate periphery is 5.1–7.0 W/mm for a drain voltage of 30 V and 6.6–8.9 W/mm for 35 V. Measured results are compared to other published X-band MMIC HPAs. Table 4-1 shows a comparison of state-of-the-art X-band MMIC HPAs. The measured performances demonstrate the highest performance in terms of the combinations of output power and PAE compared to existing state-of-the-art X-band MMIC HPAs.

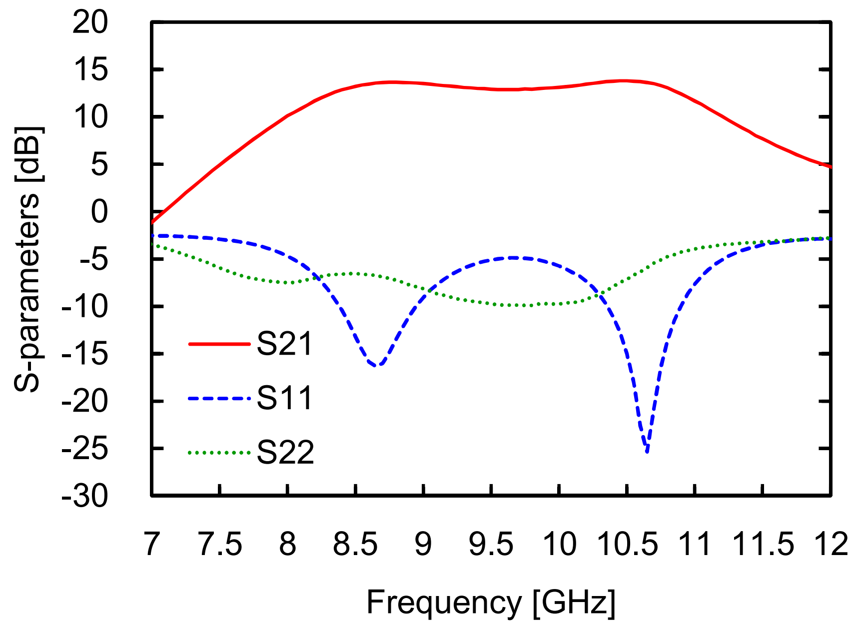


Fig. 4-8. Measured s-parameters of GaN-MMIC HPA.

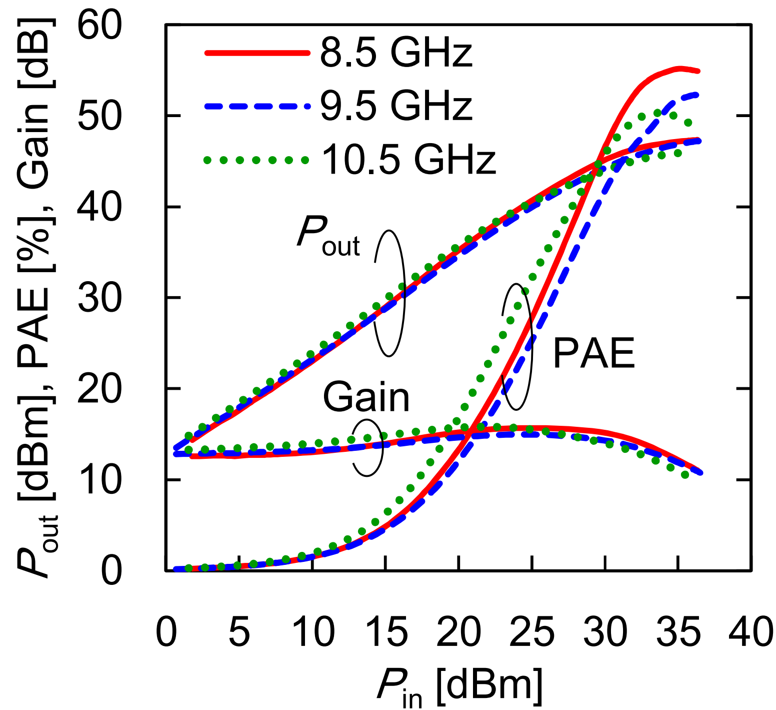


Fig. 4-9. Measured output power, PAE and gain of the developed GaN-MMIC HPA as a function of input power with drain voltage of 30 V.

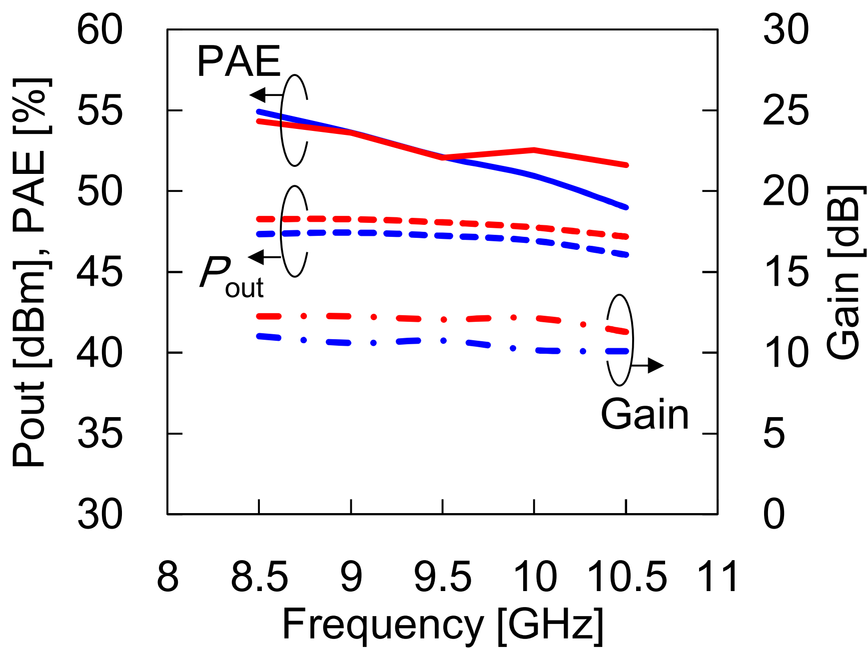


Fig. 4-10. Measured output power, PAE and gain of the developed GaN-MMIC HPA as a function of frequency. Blue lines are for drain voltage of 30 V and red lines are for drain voltage of 35 V.

Table 4-1. Comparison of state-of-the-art X-band MMIC HPAs

Ref	Frequency [GHz]	Output power [W]	PAE [%]	Gain [dB]	Drain Voltage [V]	Area [mm^2]	Output power/Area [W/mm^2]
This work	8.5–10.5	41–56	49–55	10.1–11.0	30	12.2	4.5
	8.5–10.5	53–70	52–54	11.2–12.1	35	12.2	5.7
[75]	10.2	9.2	61.1	10.8	44	NA	NA
[76]	10.0–10.5	10–14	48–61	19	25	9.2	1.52
[77]	9–11	35–45	40–52	16.3	25	18	2.5
[78]	8–12	56–74	40–45	21.5–22.7	28	13.3	5.57

4.6 Conclusion

An X-band MMIC HPA utilizing the 0.15-μm GaN FET process with an ISV structure is designed and studied. The developed HPA demonstrates an output power of 46.1–47.4 dBm, PAE of 49–55%, and a gain of 10.1–11.0 dB at 8.5–10.5 GHz with a drain voltage of 30 V. Output power of 47.2–48.4 dBm, PAE of 52–54%, and gain of 11.2–12.1 dB are obtained at 8.5–10.5 GHz with a drain voltage of 35 V. The developed GaN-MMIC HPA demonstrates the highest performance in terms of the combination of output power and PAE compared to other reported state-of-the-art X-band MMIC HPAs.

The ISV structure and low-loss output matching circuit technology are more effective at high frequencies where parasitic inductance and dielectric loss are large, and can be expected to be applied to millimeter-wave HPAs. The effect of improvement in efficiency at Ka-band will be between 2-7% [86].

Chapter 5.

Power amplifiers and a switch incorporating partial MMIC and GaN-on-Si technologies for low-cost transmit/receive module

It was shown in Chapters 3 and 4 that GaN-MMICs are compact and offer a high performance thanks to its high degree of freedom in circuit design. However, the cost of GaN-on-SiC substrates tends to be high. Since MMIC chipsets such as power amplifiers and switches account for a high cost ratio of the T/R module, it is important to lower the cost of the chipset. In this chapter, we propose two cost reduction strategies for the T/R modules. One is to use GaN-on-Si devices [88][89]. The other is to use a partial MMIC configuration. Since GaN-on-SiC is expensive, a low-cost and low-loss GaAs MMIC is used as a matching circuit to reduce the cost. Based on these concepts, GaN-on-Si-MMIC DA and HPA, GaN-on-SiC HPA and GaN-on-Si-MMIC SW have been developed as chip sets for low-cost T/R modules.

5.1 Introduction

Transmit-receive (T/R) modules have been widely utilized in applications such as radar technology and communication systems. Active phased array antennas (APAAs), which enable electrical beam formation, have been applied to radar systems [90] and recently also introduced to communication systems such as fifth-generation mobile communications (5G) [91]. As APAAs require thousands of T/R modules, the cost of T/R

modules accounts for a large portion of the system cost [92]. There is an increasing demand for cost-effective transmit modules with high-performance characteristics. A major contributing factor to the cost of T/R modules is the cost of the monolithic microwave integrated circuits (MMICs) component. As the cost of MMIC is mainly driven by the choice of substrate materials and chip size, cost-effective substrate materials and compact design configurations ought to be considered. To realize high power density outputs and PAE, GaN-on-SiC HPAs [93]–[99] and switches (SWs) [100][101] are often utilized. To achieve low-cost chip set, GaN-on-Si-MMIC DA and HPA, GaN-on-SiC HPA and GaN-on-Si-MMIC SW are developed. The concepts of X-band GaN chipsets are proposed, and the design methods and measurement results are shown in Section 5.2, with their performance and cost-effectiveness evaluated against advanced MMIC based chipset devices in Section 5.3.

5.2 Concepts of GaN Chipsets

A schematic of a targeted T/R module is illustrated in Fig. 5-1. The chipsets include amplifier stage and SW. The target performance of amplifier stage is an output power of 20 W and gain of 30 dB to configure proper amplifier chain with a typical Si core-chip with the saturate output power of about 15 dBm. The target performances of SW are isolation of 15 dB with high power input up to 20 W considering isolation of a circulator. Transmit modules with such performances are conventionally composed of a GaAs or GaN-on-SiC MMIC DA, a GaN-on-SiC HPA, and a GaN-on-SiC SW [103]–[109]. Another option for an amplifier stage is utilizing a high-gain GaN-on-SiC MMIC HPA [109] instead of the combination of a DA and an HPA. These configurations demonstrate good performance due to high power capability and high-efficiency characteristic of GaN FETs. However, the configuration tends to be relatively costly due to the high-cost of

GaN-on-SiC substrates. GaAs realizes lower cost to area ratios, but the doubling of sizes is necessary to obtain such a high power of 20 W amplifier because of its lower power density. Two types of T/R modules are proposed to configure low-cost and high performance. Fig. 5-1 illustrates schematics of proposed amplifier stages wherein one of the proposed amplifier stage is a combination of GaN-on-Si-MMIC DA and GaN-on-SiC HPA with GaAs output matching circuit (Case-1) as illustrated in Fig. 5-2. The power density of GaN-on-Si is as high as that of GaN-on-SiC while the cost to size ratio is comparable with that of GaAs. GaN-on-SiC HPA with GaAs output matching circuit retains the high performance of GaN-on-SiC FETs while matching circuits are realized by GaAs to reduce cost. The other module is composed of a high-gain GaN-on-Si HPA (Case-2) as illustrated in Fig. 5-3, a DA and an HPA is integrated in a GaN-on-Si chip, and a GaAs output matching circuit is applied. However, the cost of case-2 is lower than that of case-1, whereas, efficiency of case-2 is slightly lower than that of case-1 due to the difference in FET performance. The GaAs output matching circuit is applied to reduce circuit losses compared to those with GaN-on-Si substrate. GaN-on-Si-MMIC SW is proposed to reduce the cost and realizes that while retaining high power capability. Circuit design and measurement results of these four devices are shown in detail as follows.

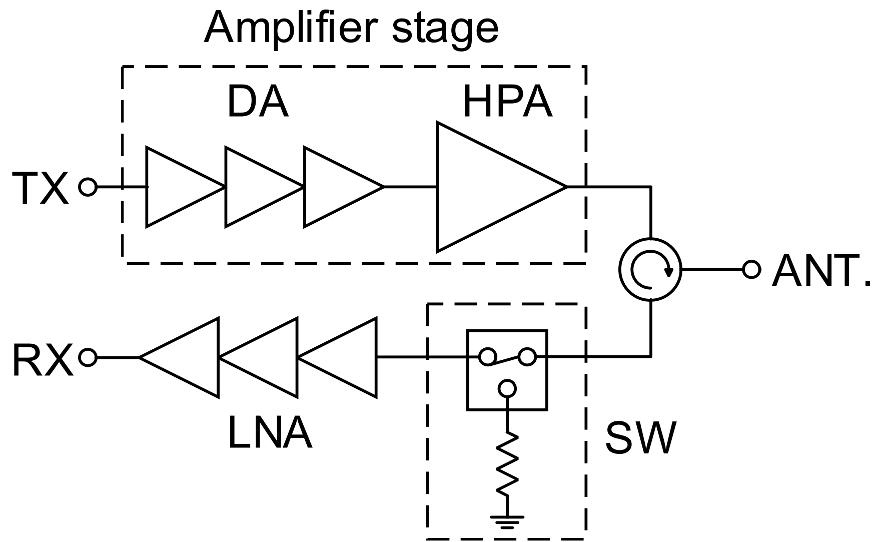


Fig. 5-1. Schematic of target GaN T/R module with the chipset

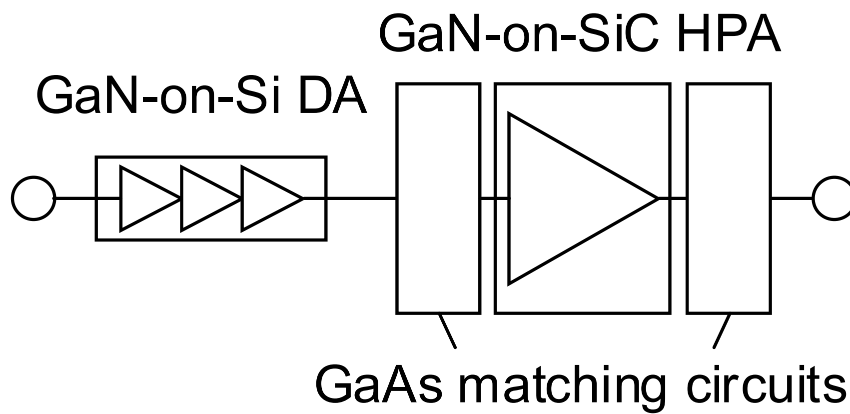


Fig. 5-2. Schematic of the proposed amplifier stage case-1.

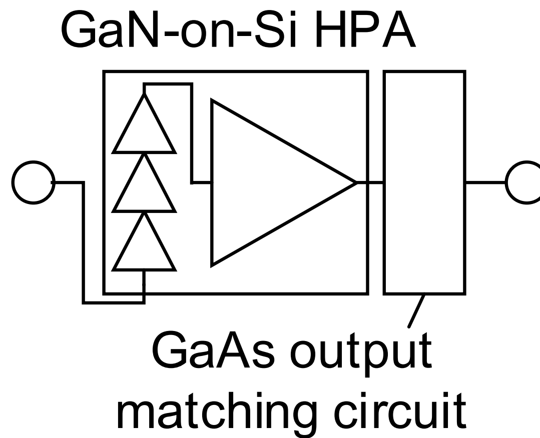


Fig. 5-3. Schematic of the proposed amplifier stage case-2.

5.3 GaN-on-Si-MMIC DA

5.3.1 Circuit Design

A GaN-on-Si-MMIC DA is designed and fabricated utilizing a 0.25 μm GaN-on-Si process. Fig. 5-5 illustrates a schematic of GaN-on-Si-MMIC DA. The DA has three FET stages, with gate peripheries of 0.5 mm for the first stage, 0.7 mm for the second stage, and 1.0 mm × 2 cells for the third stage respectively. R//C stabilization circuits with reduced losses at higher frequencies are utilized to compensate for the gain slope of FETs, which results in the DA with broadband flat gain. As illustrated in Fig. 5-4 from the dense integration of matching circuits in limited spaces, the DA is carefully designed considering electromagnetic coupling between each matching circuit. Fig. 5-5 illustrates a photograph of GaN-on-Si-MMIC DA with a chip size of 3.5 mm × 1.1 mm.

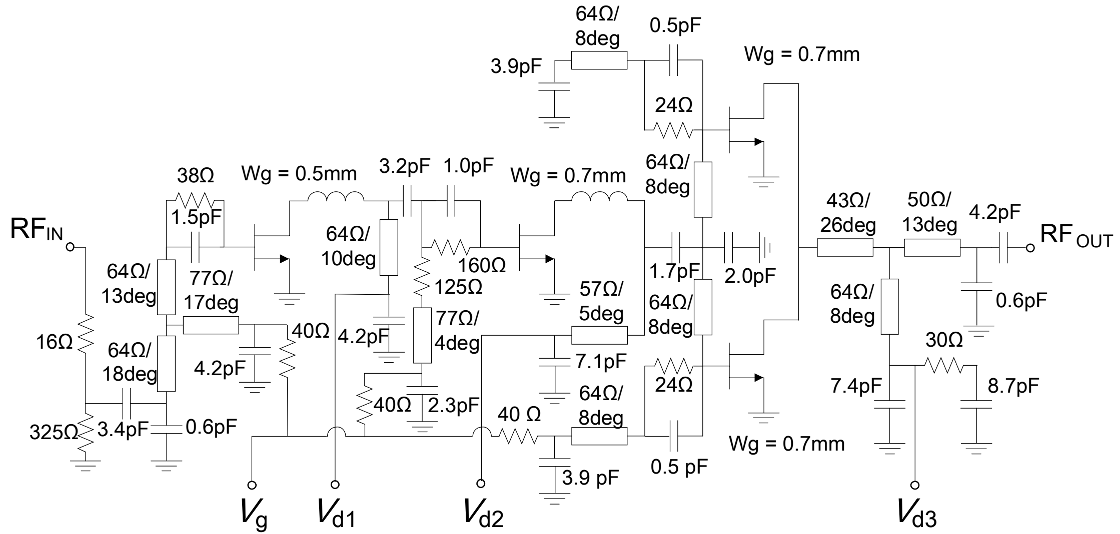


Fig. 5-4. Schematic of the GaN-on-Si-MMIC DA

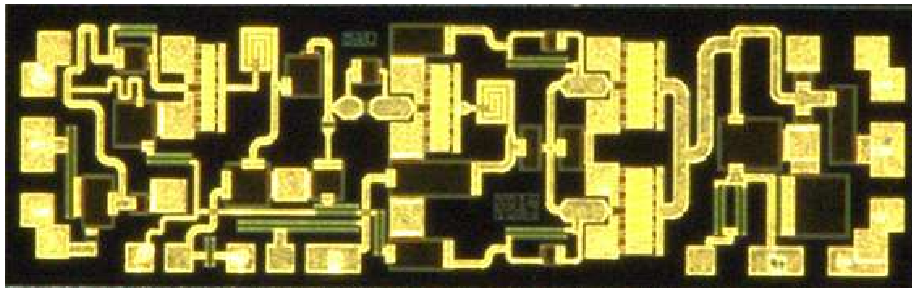


Fig. 5-5. Photograph of the GaN-on-Si-MMIC DA

5.3.2 Measurement

Small and large-signal measurements of the enhanced GaN-on-Si-MMIC DA are performed with a drain voltage of 32 V and a quiescent drain current density of 50 mA/mm. Fig. 5-6 illustrates measured S-parameters of the developed GaN-on-Si-MMIC DA. A linear gain greater than 28 dB is obtained for frequencies conditions of between 8.5–11.0 GHz. Fig. 5-7 illustrates the DA's measured output power, PAE, and gain as a function of frequency. The measurement is performed under pulsed operation with a pulse duty-cycle of 10%, and a saturated output power of 38.1–38.7 dBm, associate gain of

22.3–24.6 dB, and PAE of 32–36% over 9.0–11.0 GHz are obtained. The GaN-on-Si-MMIC DA achieves high power and high gain with an extremely compact size that is less than half the size of typical GaAs MMIC HPA with similar output power[110].

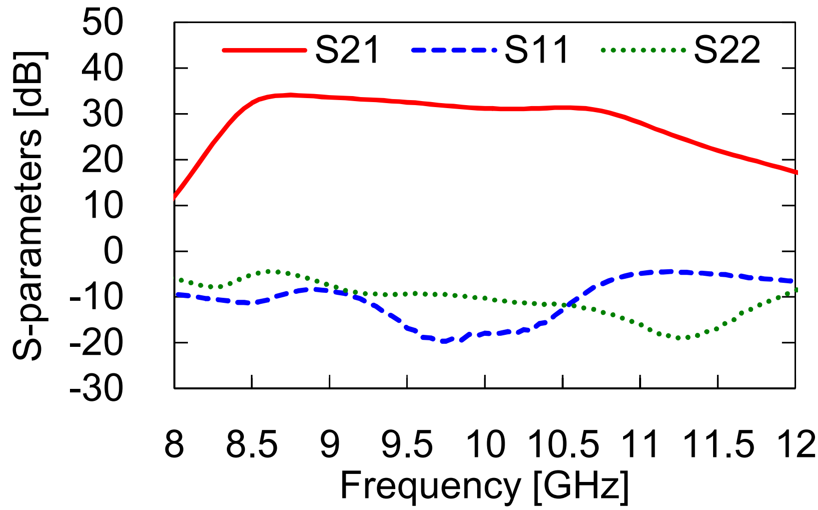


Fig. 5-6. Measured S-parameters of the developed GaN-on-Si-MMIC DA

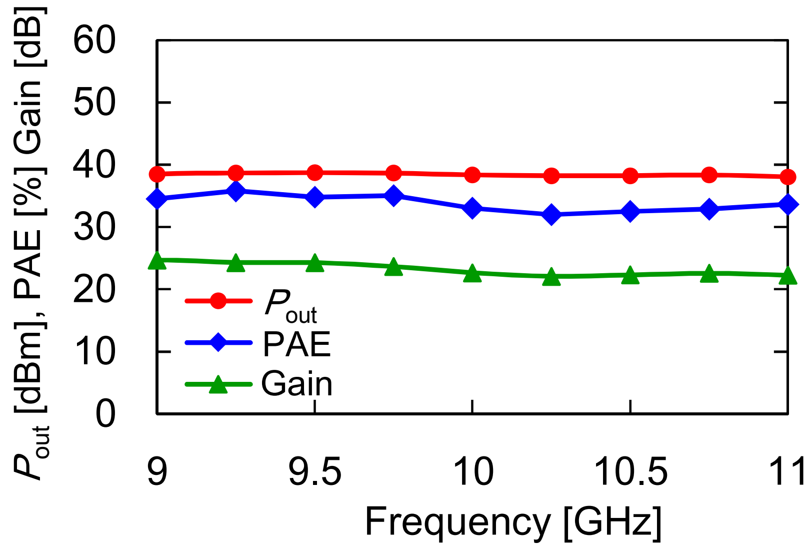


Fig. 5-7. Measured output power, PAE, and gain of the improved GaN-on-Si-MMIC DA.

5.4 GaN-on-SiC HPA with GaAs input and output matching circuits

5.4.1 Circuit Design

GaN-on-SiC HPA with GaAs input and output matching circuits are designed and fabricated utilizing the 0.25 μm GaN-on-SiC MMIC and GaAs passive MMIC process. A schematic of the GaN-on-SiC HPA with GaAs matching circuits is illustrated in Fig. 5-8. GaAs input and output matching circuits and a GaN-on-SiC FET chip are connected via bonding wires. With HPAs being one of the most power-consuming components in T/R modules, design of the output matching circuit is important to realize high efficiency utilizing harmonic impedance tuning technique [111]–[117]. Impedance matching at the fundamental frequency is mainly based on a quarter-wavelength transmission line and a shunt inductance. In addition, open stubs with an electrical length of λ/4 at the second harmonic are used to obtain PAE matching at the second harmonic frequency. Fig. 5-9 illustrates the simulated target impedance and impedance of matching circuits seen from the FETs for the fundamental (solid lines) and the second harmonic (dotted lines) frequency. Fig. 5-9(a) illustrates the source-pull contour and the designed impedance of the input matching circuit seen from the FETs for the second harmonic. The impedance for the maximum PAE and the impedance for the minimum PAE are almost equal. Therefore, the designed impedance is slightly mismatched from the maximum PAE impedance so that the impedance is far from the minimum PAE impedance. Fig. 5-9(b) illustrates impedances of the output matching circuit seen from the FETs. PAE contours are plotted by 2 pt. step. Designed impedance of the output matching circuit seen from the FETs for the fundamental (9–11 GHz) and the second harmonic (18–22 GHz) frequencies are shown, and the direction of the arrows indicate the low frequency to the

high frequency. The HPA behaves like inverse class-F amplifier since only the second harmonic impedance is designed to realize open impedance. It is shown that the fundamental and the second harmonic impedances are well matched to the target impedances. On the input side, impedance matching at the fundamental frequency is achieved by one bandpass and one low-pass configuration. Pre-match small shunt capacitors are incorporated into the GaN-on-SiC FET chip to tune the second harmonic impedance. Fig. 5-10 shows a photograph of the developed GaN-on-SiC HPA. The input matching circuit chip sizes, the FET chip, and the output matching circuit are 1.8 mm × 3.8 mm, 0.8 mm × 3.8 mm and 2.0 mm × 3.8 mm, respectively.

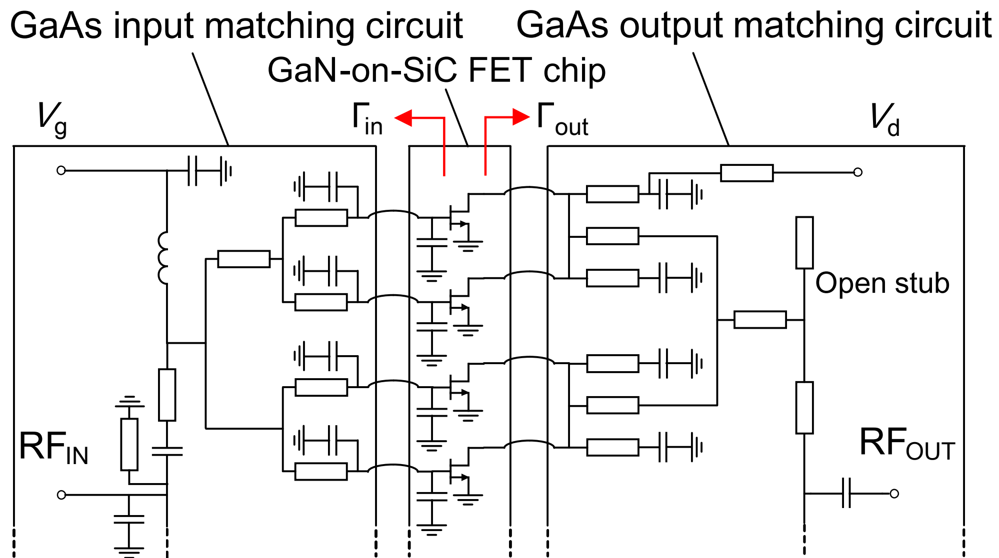


Fig. 5-8. Schematic of GaN-on-SiC HPA with GaAs matching circuits. Half of the circuit is shown, and the other half is symmetric.

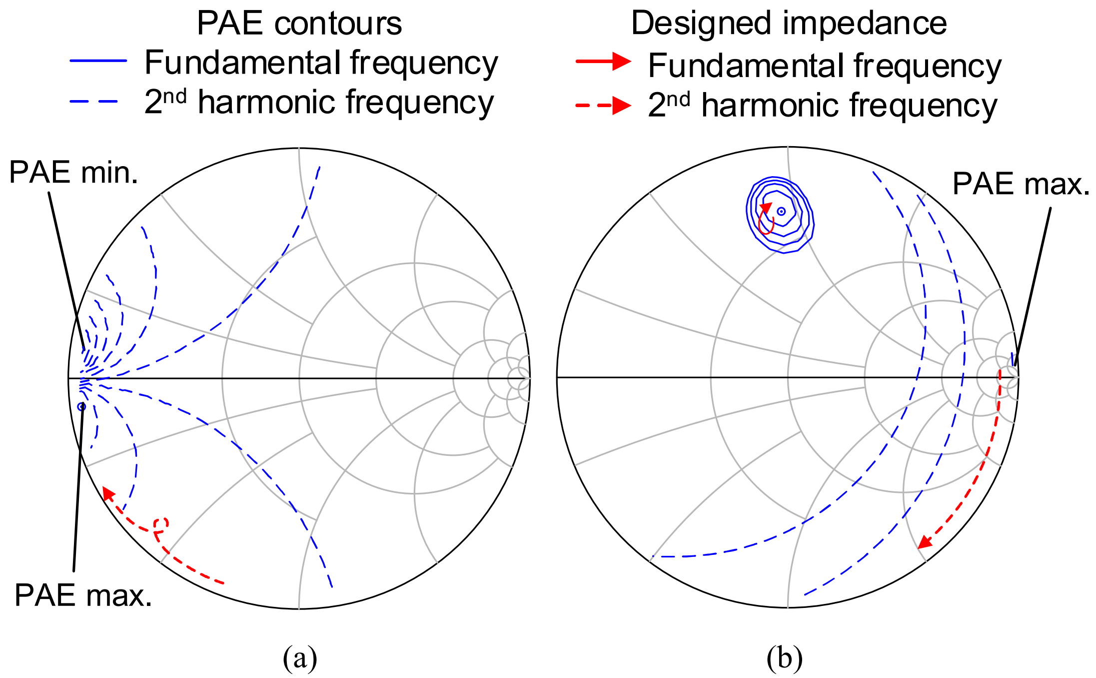


Fig. 5-9. Simulated targeted and designed impedances of the matching circuits. (a) Impedance of the input matching circuit. (b) Impedance of the output matching circuit.

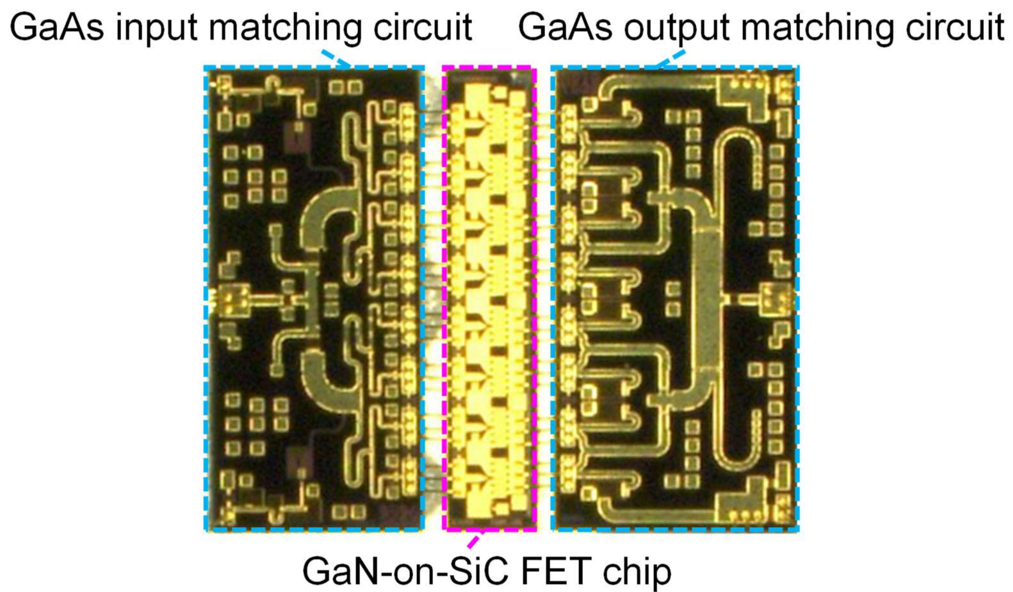


Fig. 5-10. Photograph of GaN-on-SiC HPA with GaAs matching circuits.

5.4.2 Measurement

Small and large-signal measurements of the developed GaN-on-SiC HPA are performed with a drain voltage of 30 V and the quiescent drain current density of 50 mA/mm. Fig. 5-11 illustrates the measured S-parameters of the developed GaN-on-SiC HPA. The linear gain of 8.1–11.5 dB is obtained at frequencies of over 9.0–11.0 GHz. The large-signal measurement is performed under the pulsed condition with a pulse duty-cycle of 10%. Fig. 5-12 illustrates the measured output power, PAE, and gain of the developed GaN-on-SiC HPA as a function of frequency. The drain voltage is 30 V and the quiescent drain current density is 50 mA/mm. A saturated output power of 42.0–44.5 dBm, associate gain of 7.8–10.7 dB, and PAE of 40–56% for 9.0–11.0 GHz is obtained. These measured results show that the lower cost amplifier exhibits comparable characteristics with all reported advanced amplifiers.

By combining GaN-on-Si-MMIC DA and GaN-on-SiC HPA, an output power in excess of 20 W, gain of higher than 30.8 dB, and PAE greater than 37% is estimated for frequencies of over 9.0–11.0 GHz.

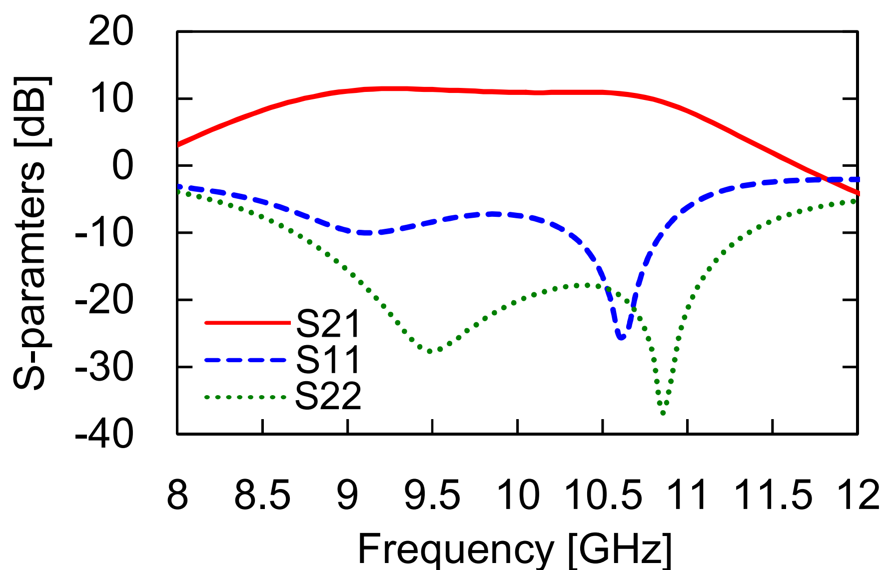


Fig. 5-11. Measured S-parameters of GaN-on-SiC HPA

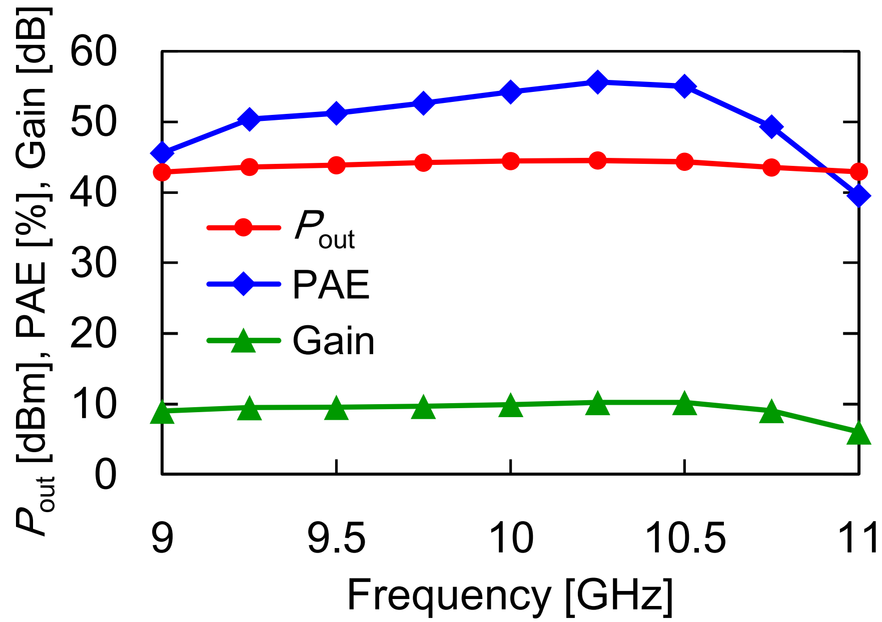


Fig. 5-12. Measured output power, PAE and gain of the developed GaN-on-SiC HPA

5.5 GaN-on-Si HPA with GaAs output matching circuits

5.5.1 Circuit design

The circuit design and measurements of a high-gain GaN-on-Si HPA are shown. A GaAs matching circuit is employed as the output matching circuit of the final stage amplifier to realize lower losses. As illustrated in Fig. 5-3, the high gain four-stage GaN-on-Si HPA amplifier is composed of the GaN-on-Si amplifier chip and GaAs output matching circuit, which are connected via bonding wires. The aforementioned three-stage GaN-on-Si-MMIC DA, an input matching circuit as well as FETs for the final-stage are incorporated into the GaN-on-Si chip. The final stage-gate periphery of the FETs is 1 mm × 8 cells. The DA is placed vertically with respect to the final-stage amplifier to reduce the chip size and connected with HPA via a 50 Ω transmission line. The output matching circuit is the same as the GaN-on-SiC HPA described in Section 2.3 as the target impedances are quite similar. Although the cost to area ratio of the GaAs and GaN-on-Si is comparable, GaAs exhibits lower dielectric losses, which enables high power and high-

efficiency HPA. Fig. 5-13 illustrates a schematic of the input matching circuit of the final-stage GaN-on-Si HPA, which is newly designed for the HPA. Two high-pass and one low-pass section are utilized. Fig. 5-14 illustrates simulated target and designed second harmonic impedances of the input matching circuits of the GaN-on-Si HPA seen from the final-stage FETs. PAE contours of the second harmonic frequency for 10 GHz are plotted by 2 pt. step. The designed impedance for the second harmonic (18–22 GHz) frequencies are also shown and the direction of the arrows indicates the low frequency to the high frequency. The impedance for the maximum PAE and the impedance for the minimum PAE are close each other. Therefore, the designed impedance is mismatched from the maximum PAE impedance so that the impedance is far from the minimum PAE impedance as in case of the GaN-on-SiC HPA. Fig. 5-15 illustrates a photograph of the GaN-on-Si HPA with a GaAs output matching circuit. The total chip size of the GaN-on-Si chip and the GaAs chip are 3.5 mm × 3.8 mm and 2.0 mm × 3.8 mm, respectively.

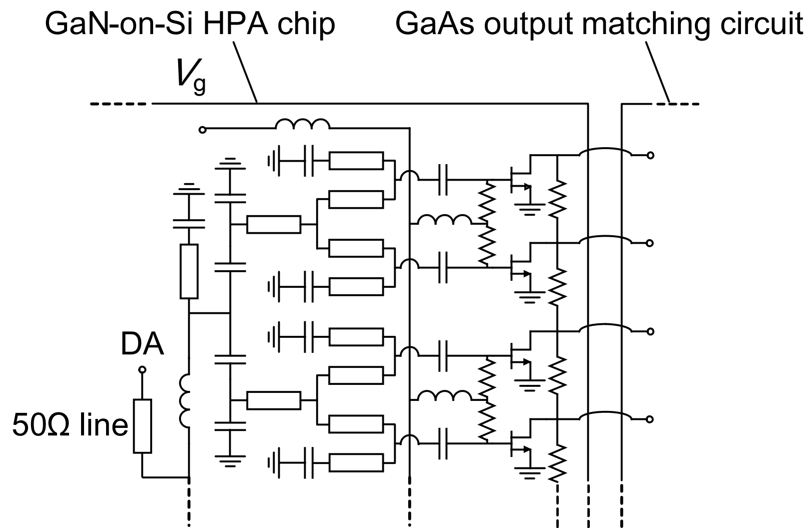


Fig. 5-13. Schematic of the input matching circuit of GaN-on-Si HPA. Half of the circuit is shown, and the other half is symmetric.

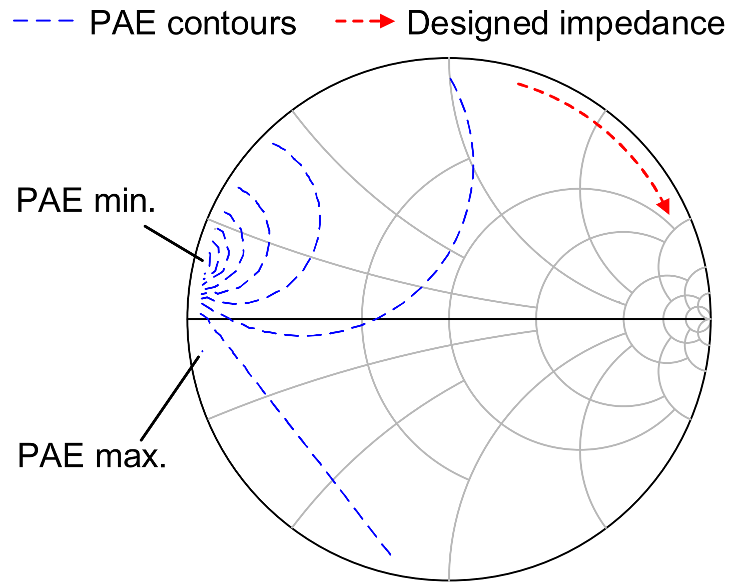


Fig. 5-14. Simulated target and designed second harmonic impedances of the input matching circuits of the GaN-on-Si HPA.

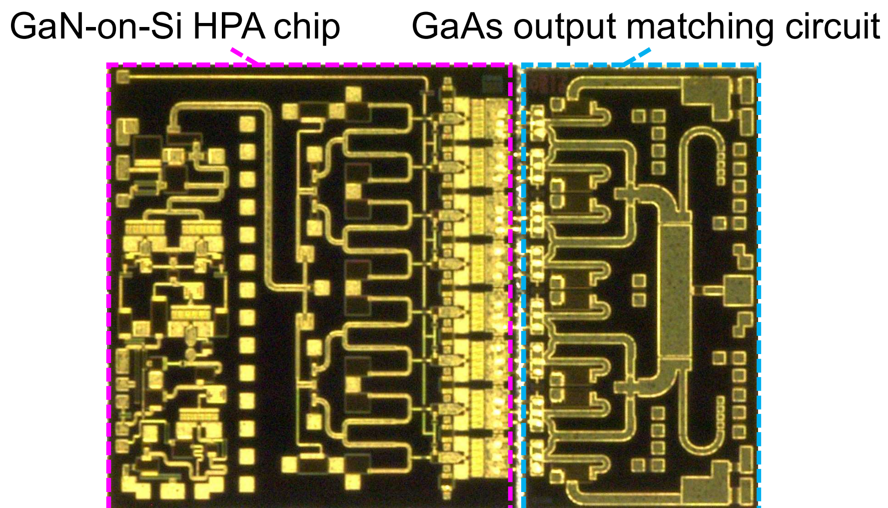


Fig. 5-15. Photograph of the developed GaN-on-Si HPA

5.5.2 Measurement

Small and large-signal measurements are performed, with a drain voltage is 32 V and the quiescent drain current density of 50 mA/mm being recorded. Fig. 5-16 illustrates the measured S-parameters of the developed GaN-on-Si-MMIC HPA. A linear gain of 38.7–

41.2 dB is obtained over frequencies of 9.0–11.0 GHz. Fig. 5-17 illustrates measured output power, gain, and PAE for the improved GaN-on-Si HPA as a function of frequency. The large-signal measurement is operated under a pulse duty-cycle of 10%. And reports a saturated output power in the 41.8–44.8 dBm range, associated gain of 26.9–29.5 dB and PAE of 26–33% for frequencies of 9.0–11.0 GHz. While the efficiency is not as high as that of GaN-on-SiC HPA, these configurations indicate compact and high output power and gain characteristics. The effect of the machining accuracy on the performances is comparable for the two configurations because the deviation of bonding wire length connected to the output matching circuit is dominant on the performance. The configuration of amplifier stage is in a trade-off between the efficiency and the cost.

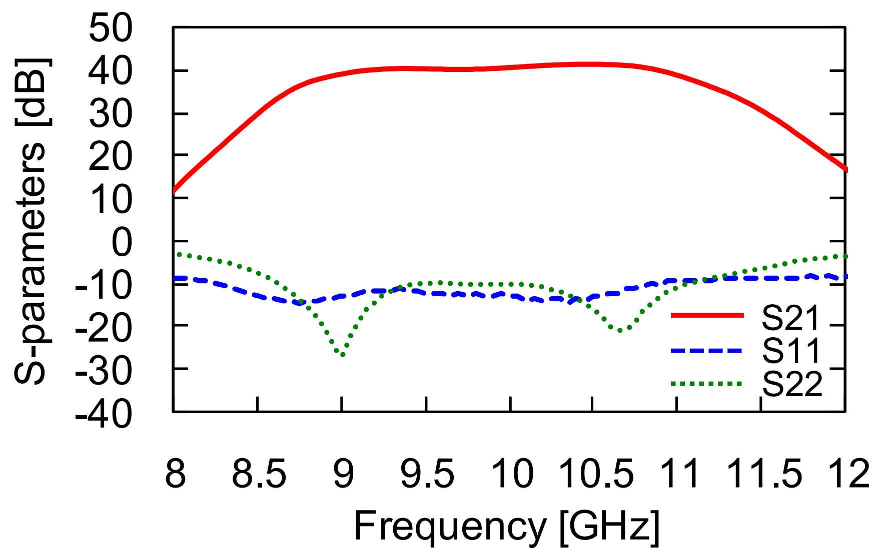


Fig. 5-16. Measured S-parameters of the GaN-on-Si HPA

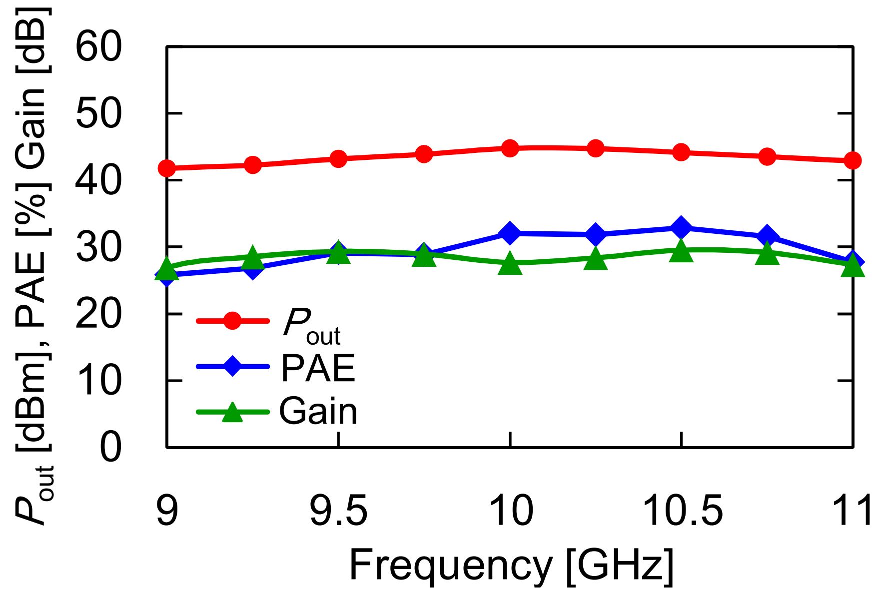


Fig. 5-17. Measured output power, PAE and gain of the GaN-on-Si HPA.

5.6 GaN-on-Si-MMIC High Power SW

5.6.1 Circuit design

A cost-effective GaN-on-Si-MMIC SW is designed to protect the receiving devices such as low noise amplifier (LNA) from transmission or reception of unwanted large signals. Fig. 5-18 illustrates schematics of the developed GaN-on-Si-MMIC SW. Fig. 5-18 (a) illustrates the equivalent circuit of the developed GaN-on-Si-MMIC SW. The SW has an input port and a terminal port which is terminated to 50 Ω. The SW has two FETs, namely FET1 and FET2. FET1 is connected in series between the input and the output ports. A transmission line with the length of λ/4 at the center frequency followed by shunted FET2 is placed between the input and the terminal ports. A spiral inductor is connected in parallel with each FET. Gate electrodes of the FETs are connected to a common DC voltage supply with high resistance. The operation modes of the SW are controlled by a DC voltage applied to the gates of the FETs, wherein the FET shows off-capacitance when biased at -40 V and on-resistance when biased 0 V. The FETs are biased

at 0 V in receive-mode and -40 V in transmit-mode, respectively. Fig. 5-18(b) and (c) illustrate equivalent circuits of the SW in receive-mode and transmit-mode, respectively. In receive-mode, FETs are biased at 0 V so that they behave as low on-resistance. The equivalent circuit of the receive-mode is illustrated in Fig. 5-18(b). FET1 exhibits limited losses and the impedance of the shunt-connected λ/4 and FET2 exhibits open impedance looking from the input port at the center frequency. Therefore, it has low loss characteristic from the input to the output port. In transmit-mode, isolation between input and output ports must be high to protect receiving devices from high power transmit signal or noise. FETs are biased at -40 V so that they behave as off-capacitance. The equivalent circuit of the transmit-mode is illustrated in Fig. 5-18(c). Each FET and inductance behave like an open circuit, with external signals from input port going to the terminal port. Then, it demonstrates high isolation characteristics between the input and output ports. Design of gate-width of the FETs is explained. Parallel inductors are neglected for simplification. F-matrix between the RF input and output port of the receive-mode is calculated to be

$$F_{\mathrm{RX}} = \begin{pmatrix} 1 & 0 \\ \frac{1}{Z}\frac{Z + jZ_{\mathrm{L}}\tan\theta}{Z_{\mathrm{L}} + jZ\tan\theta} & 1 \end{pmatrix} \begin{pmatrix} 1 & R_{\mathrm{on1}} \\ 0 & 1 \end{pmatrix}, Z_L = Z_0 // R_{\mathrm{on2}} \tag{5-1}$$

where Z_0 is the port impedance, Z and θ are the characteristic impedance and the electrical length of the λ/4 line, R_{on1} and R_{on2} are the on-resistance of FET1 and FET2, respectively. By assuming that θ = 90 deg., $R_{\mathrm{on}} \cong R_{\mathrm{on1}}, R_{\mathrm{on2}}$, $Z_{\mathrm{L}} \cong R_{\mathrm{on}}$, $Z \cong Z_0$ and $(R_{\mathrm{on}}/Z_0)^2 \cong 0$, Eq. 5-1 is transformed to

$$F_{\mathrm{RX}} \cong \begin{pmatrix} 1 & R_{on} \\ R_{on}/Z_0^2 & 1 \end{pmatrix}. \tag{5-2}$$

Then the insertion loss in receive-mode ($\mathrm{IL_{RX}}$) is derived by calculating $|S_{21}|$ using Equation (5-2) as

$$\mathrm{IL_{RX}} \cong \frac{1}{1 + R_{on}/Z_0} = \frac{1}{1 + R_{on}\ /W_g Z_0} \tag{5-3}$$

where R_{on0} (Ωmm) is the on-resistance of the 1 mm-gate-width FET and W_g (mm) is the gate width of the FET. Similarly, F-matrix between the RF input and output port of the transmit-mode is calculated to be

$$F_{\text{TX}} = \begin{pmatrix} 1 & 0 \\ \frac{1}{Z}\frac{Z + jZ_{\text{L}}tan\theta}{Z_{\text{L}} + jZtan\theta} & 1 \end{pmatrix} \begin{pmatrix} 1 & 1/j\omega C_{\text{off1}} \\ 0 & 1 \end{pmatrix}, Z_L = Z_0 // j\omega C_{\text{off2}} \qquad (5\text{-}4)$$

Where C_{off1} is the off-capacitance of the FET1. By assuming that $Z_{\text{L}} \cong Z \cong Z_0$, Equation (5-4) is transformed to

$$F_{\text{TX}} \cong \begin{pmatrix} 1 & 1/j\omega C_{\text{off1}} \\ 1/Z_0 & 1 + 1/j\omega C_{\text{off1}} Z_0 \end{pmatrix}. \qquad (5\text{-}5)$$

Then the isolation in transmit-mode (ISO_{TX}) is derived by calculating $|S_{21}|$ using Equation (5-5) as

$$\text{ISO}_{\text{TX}} \cong \frac{1}{\sqrt{2.25 + (1/\omega C_{\text{off1}} Z_0)^2}} = \frac{1}{\sqrt{2.25 + \left(1/\omega C_{\text{off0}} W_{\text{g}} Z_0\right)^2}} \qquad (5\text{-}6)$$

Where C_{off0} (F/mm) is the off-capacitance of the 1 mm-gate-width FET. Insertion loss and isolation are in a trade-off relation according to W_{g}. Fig. 5-19 shows the dependence of insertion loss and isolation on the gate width of FET according to Equation 5-3 and Equation (5-6) (Z_0 = 50 Ω, R_{on0} = 3.7 Ωmm, C_{off0} = 0.186 pF/mm and f = 10 GHz). Large W_{g} of 1 mm is employed for loss reduction and the value of the inductors is set so that the resonation frequency of C_{off} and the inductance is equal to the center frequency to improve isolation.

A photograph of the GaN-on-Si-MMIC SW, with a chip size of 1.05 mm × 1.95 mm is illustrated in Fig. 5-20. Transmission lines between the input port and the output port are designed to be as short as possible to reduce losses.

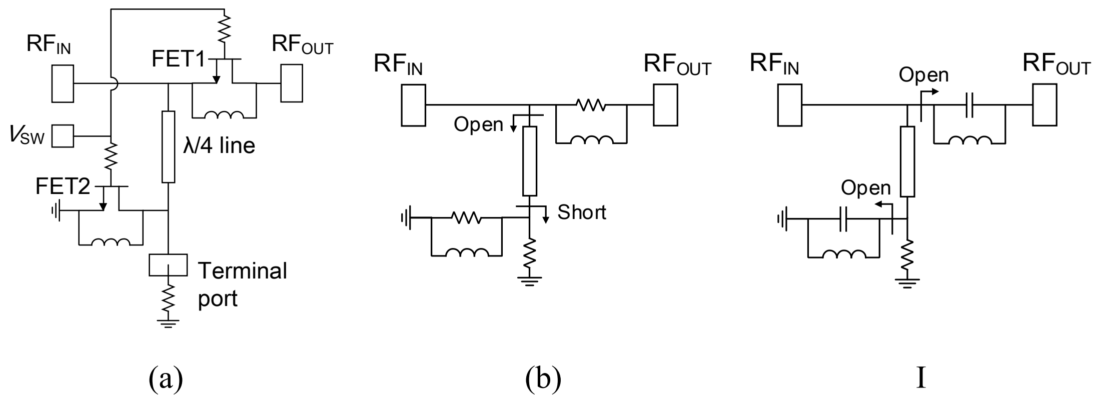


Fig. 5-18. Schematic of GaN-on-Si-MMIC SW. (a) Equivalent circuit of developed GaN-on-Si-MMIC SW. (b) Simplified equivalent circuit of SW in receive-mode. (c) Simplified equivalent circuit of SW in transmit-mode.

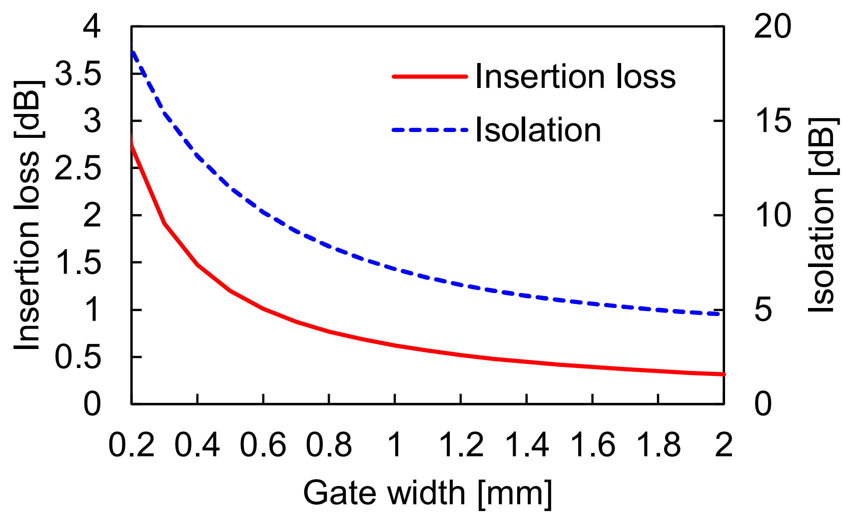


Fig. 5-19. Dependence of insertion loss and isolation on the total gate width.

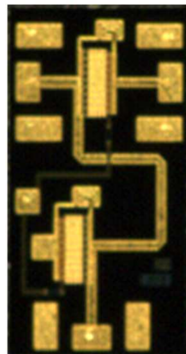


Fig. 5-20. Photograph of the developed GaN-on-Si-MMIC SW

5.6.2 Measurements

Fig. 5-21 shows a measurement insertion loss and isolation of the developed GaN-on-Si-MMIC SW. Insertion losses of 1.1–1.3 dB and isolation of 10.1–14.7 dB are obtained at frequencies of 8.0–11.5 GHz. The measured loss is larger than the calculated loss due to the loss of transmission lines is neglected in the calculation. The measured isolation is larger than the calculated isolation since the parallel inductor is neglected in the calculation. Fig. 5-22 illustrates the measured large-signal characteristic of GaN-on-Si-MMIC SW. Deviation of isolation is less than 0.5 dB, and up to 43.1 dBm input power.

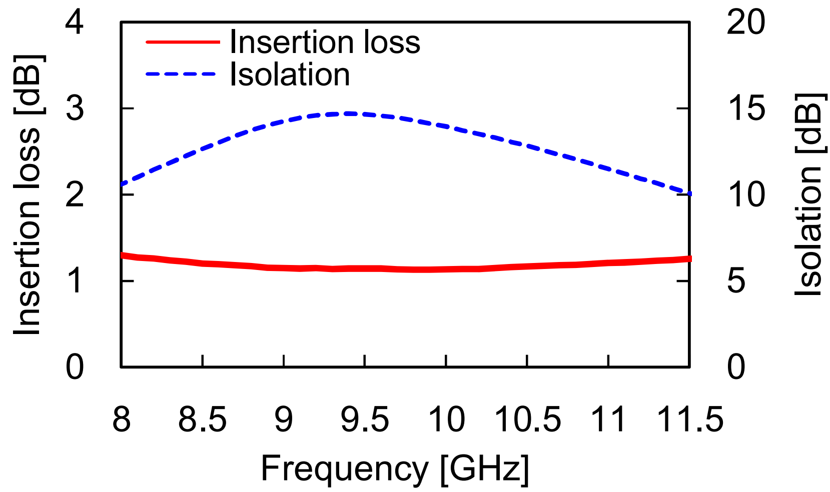


Fig. 5-21. Measured small-signal characteristics of the developed GaN-on-Si SW

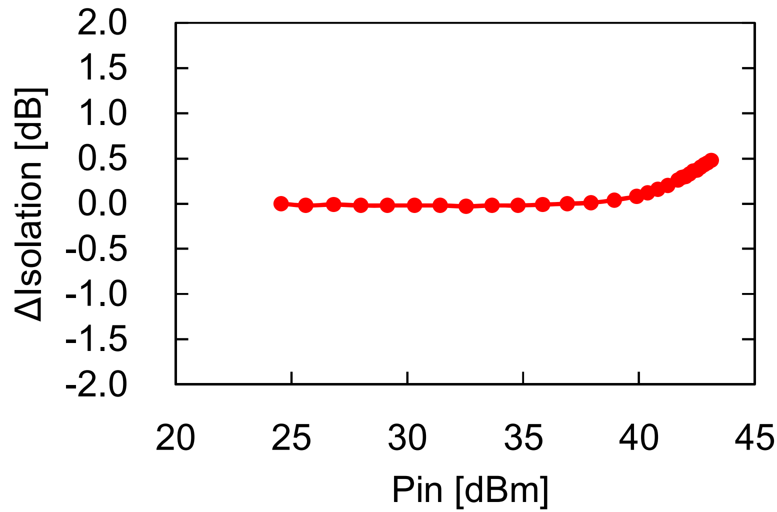


Fig. 5-22. Measured large-signal characteristic of GaN-on-Si-MMIC SW

5.7 Evaluation of cost-effectiveness

The cost-efficiency of the developed chipsets is evaluated. Table 5-1 summarizes comparisons of size and the estimated relative cost with other published power amplifiers and switches for X-band T/R modules. Applying a partial MMIC configuration increases bonding wire mounting, but in general the cost of wire mounting is negligibly low (<1%) relative to the chip cost. In case-1, the developed GaN-on-Si-MMIC DA, the GaN-on-SiC HPA with the GaAs output matching circuit, and the GaN-on-Si-MMIC SW are utilized. In case-2, the developed GaN-on-Si high-gain HPA and the GaN-on-Si-MMIC SW are utilized. In case-3, conventional T/R modules composed of the GaAs DA[110], the GaN-on-SiC HPA [93] and the GaN-on-SiC SW [100] ever-reported. The cost ratio of GaAs:GaN-on-SiC is typically said to be 1:2 [106][107]. 50% cost reduction of GaN device fabrication is achieved by using larger wafer. Because large Si wafer is commonly available, cost of GaN-on-Si can be half the cost of GaN-on-SiC. The normalized cost is calculated using a chip size and assumed cost ratio of GaN-on-Si:GaAs:GaN-on-SiC = 1:1:2. By employing the chipset shown in case-1, 46% cost reduction from case-3 is

estimated. The cost of case-2 is estimated to be less than half as expensive as case-3. As the output power is comparable between case-1 and case-2, only the efficiency is a trade-off factor with the cost. If power consumption of system specification was not as tight, for example, the system only required short pulse mode operation, case-2 can be the best candidate for the T/R module.

Table 5-1. Comparisons of size and estimated relative cost with other published power amplifiers and a switch for X-band modules.

		DA		HPA		SW		*Cost ratio (a.u)
		Substrate	Size (mm^2)	Substrate	Size (mm^2)	Substrate	Size (mm^2)	
This work	Case 1	GaN-on-Si	3.9	GaN-on-SiC/GaAs	3.0/14.4	GaN-on-Si	2	0.54
	Case 2	-	-	GaN-on-Si/GaAs	13.3/7.6	GaN-on-Si	2	0.47
Case 3		GaAs [110]	8.8	GaN-on-SiC [93]	18	GaN-on-SiC [100]	1.9	1

(*) Assuming cost ratio of GaN-on-Si:GaAs:GaN-on-SiC = 1:1:2

5.8 Conclusion

GaN chipsets for cost-effective X-band 20 W T/R modules are fabricated and measured. The chipsets include four devices, a GaN-on-Si-MMIC DA, a GaN-on-SiC MMIC HPA with a GaAs MMIC input and output matching circuits, a high-gain GaN-on-Si HPA with a GaAs output matching circuit, and a GaN-on-Si high power SW. The developed chipsets are estimated to be about half the cost of a conventional chipset while maintaining performances. Utilizing partial MMIC and GaN-on-Si technologies are more advantageous at sub-6 band frequencies because the effects of transistor performance differences, bonding wires will be lower because of low frequency. On the other hand, application to high frequencies, such as millimeter wave, is expected to be affected by transistor performance degradation and narrowing of bandwidth due to the presence of bonding wires.

Chapter 6.

On-chip matching circuits for RF reflectometry using Si quantum dot charge sensor

This chapter reports on extracting the equivalent circuit model parameters of a physically-defined silicon QD at a cryogenic temperature and designing impedance matching circuits to improve the performance of a charge sensor for RF reflectometry. The I–V characteristics and the S-parameters of the quantum dot device are measured around a Coulomb peak at 4.2 K. The measured results are modeled by an RC parallel circuit, and the model parameters for the quantum dot device were obtained. We considered three impedance matching circuits for RF reflectometry of a quantum dot: shunt C-series L-type, shunt L-series C-type, and shunt L-series L-type. We formulated and compared the sensitivity and bandwidth of RF reflectometry for the three types of circuits. The analysis should be useful for selecting the optimal matching circuit and the circuit parameters for given equivalent circuit parameters and working frequency. This procedure is demonstrated for a quantum dot with the characterized model circuit and simulated performance. These results will facilitate fast semiconductor qubit readout in various quantum dot platforms.

6.1 RF reflectometry

Radio-frequency (RF) reflectometry is highly sensitive and useful for spin qubit readout. RF reflectometry using RF-QPC (quantum point contact) [120]–[122], gate

sensor [123]–[127] and RF-QD [128]–[134] have been studied. RF-QPC was first proposed and was replaced by highly sensitive RF-QD as process technology matured. Gate sensor reads changes in capacitance, and while it is compact, it is less sensitive than RF-QD. RF-QD is roughly 100 times more sensitive than RF-QPC and roughly ten times more sensitive than gate sensing, making it a promising method for qubit readout [123]. In the case of physically-defined QDs, the number of gate electrodes for a single quantum dot can be reduced compared to gate-defined quantum dots, allowing for integration even using RF-QDs. Multi-functional cryo-CMOS technology is also being developed for future integration [135]–[138]. Cryo-CMOS reduces the number of external interfaces and is used to achieve gate operation and sensing of the quantum dot spin qubit.

A typical QD charge sensor becomes most sensitive at a resistance of ~1 MΩ. Realizing a good impedance matching of this sensor resistance to the 50 Ω is crucial to achieving high reflectometry sensitivity. Therefore, it is important to design the impedance matching circuit based on the effective circuit model of the QD charge sensor. However, the QD charge sensor is located in a cryogenic environment where precise calibration of the high-frequency transmission properties is challenging, making detailed evaluations of the QD to extract the equivalent circuit parameters elusive. Furthermore, several types of circuits are proposed or utilized for RF reflectometry measurements of a QD charge sensor, which necessitates design methodology and trade-off analysis between the sensitivity and bandwidth for different circuits.

Here, a physically-defined silicon QD [139]–[141] is fabricated and characterized as a testbed to establish the design scheme of a matching circuit for RF reflectometry. The I–V characteristics and S-parameters of the QD are measured to extract the equivalent circuit parameters at the measurement plane located on the bonding pads of the QD chip. The expected sensitivity and bandwidth are analytically obtained for three simple, typical kinds of matching circuits. The result can be used to obtain the optimal circuit parameters

given the model parameters for the QD sensor and the target performance. The circuit design formulations are derived to obtain impedance matching between the 50 Ω input port and the QD equivalent circuit represented by an RC parallel circuit. The sensitivity to changes in the resistance or capacitance and the frequency bandwidth is analyzed and compared among the circuits. A selection criterion for the appropriate circuit in terms of sensitivity and bandwidth is given, and its simulated performance for the quantum dot measured in the experiment is presented.

6.2 Device

The device used here is an n-type physically-defined silicon QD fabricated as previously reported [140][141]. Fig. 6-1 shows a scanning electron microscope image of the physically-defined silicon QD device. The device has an n+- polysilicon top gate on top of an insulating layer which induces electrons in the SOI layer. The sensor QD is connected to the source and drain electrodes, and one side gate located nearby is biased to adjust the potential of the sensor QD. The drain and source contacts of the charge sensor QD are connected to ports 1 and 2 of the vector network analyzer (VNA) via RF-through of bias tees, respectively, and to DC measurement systems via DC-through of bias tees. Fig. 6-2 shows a photograph of the silicon QD chip mounted on a PCB. Each pad on the silicon chip is connected to the external circuitry by bonding wires and transmission lines. SMA connectors are mounted on the back side of the PCB and connected to the measurement system via RF cables. The calibration planes of the S-parameter measurement are at the SMA connectors on the PCB, and the S-parameters between the source and drain bond pads are obtained by a deembedding technique from the measurement results of calibrated S-parameters and the simulated S-parameters between the pads and the SMA connectors on the PCB.

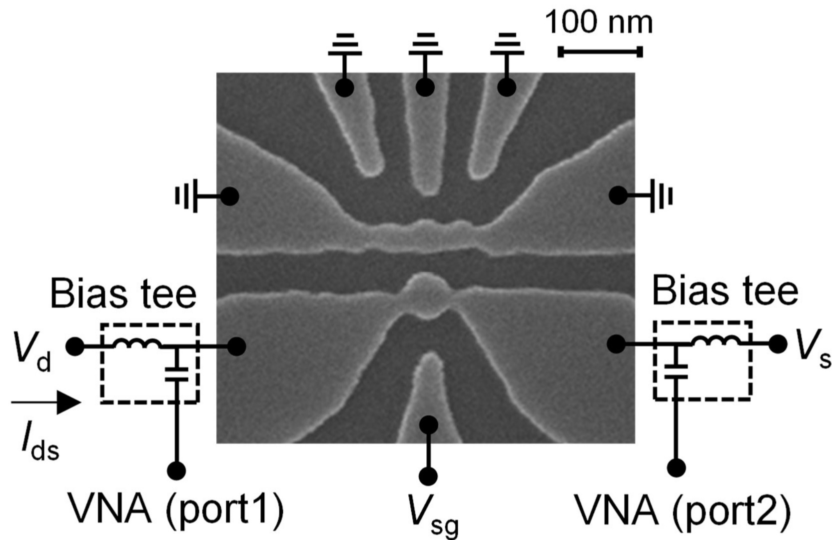


Fig. 6-1. Scanning electron micrograph of QD device.

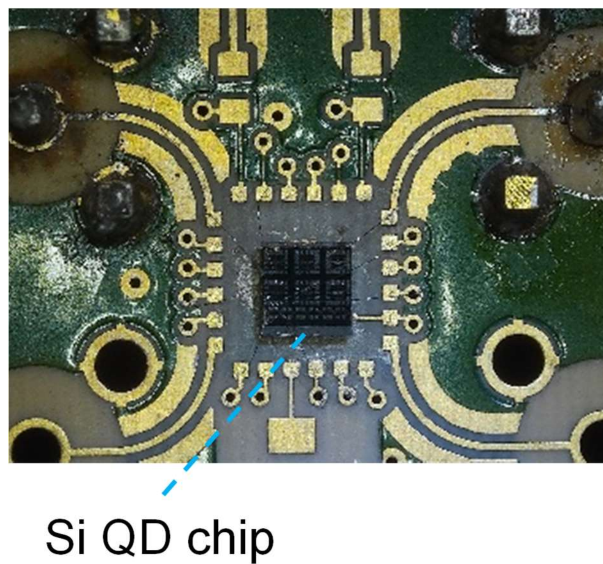


Fig. 6-2. Picture of the Si QD chip mounted on a PCB.

6.3 Measurements

A detailed equivalent circuit of a QD can be given by using a parasitic capacitance, a tunnel junction (comprising a parallel circuit of tunnel resistance and tunnel capacitance), and a gate-voltage-dependent current source [144]. While this can reproduce various

electrical properties (including I–V characteristics), for RF reflectometry, it can be simplified to a good approximation as a parallel circuit with only a resistor and a capacitor4. Theoretically, both parameters can be evaluated only by measuring the S-parameters. The reflection coefficient should ideally yield both the resistance (R_{QD}) and the capacitance (C_{QD}) of the QD. R_{QD} can be calculated from the reflection coefficient at a low frequency. When the absolute value of the reflection coefficient at low frequencies, such as near DC, is Γ_0 and the port impedance is Z_0, R_{QD} is calculated as

$$R_{QD} = \frac{1+\Gamma_0}{1-\Gamma_0} Z_0. \tag{6-1}$$

The capacitance of the QD (C_{QD}) is calculated as

$$C_{QD} = -\frac{R_{QD}(\Gamma^2 - 2\Gamma\cos\theta + 1) + \sqrt{R_{QD}^2(\Gamma^2 - 2\Gamma\cos\theta + 1)^2 - 16 Z_0^2 \Gamma^2 \sin^2\theta}}{4\Gamma\omega R_{QD} Z_0 sin\theta}. \tag{6-2}$$

where Γ is the absolute value of the reflection coefficient, θ is the reflection phase, and ω is the angular frequency. However, R_{QD} is difficult to extract accurately only from the reflection amplitude because it is very high compared to Z_0 = 50 Ω. Therefore, here, we calculate the resistance from the I–V characteristic.

All measurements were performed at a temperature of 4.2 K for a top-gate voltage of 10 V and a drain voltage of 300 μV. The I–V characteristic is measured using a lock-in amplifier technique at 71 Hz. I–V amplifier and AC voltmeter are used, and the current values are calculated from their conversion factors. Fig. 6-3 shows drain current's side-gate voltage (V_{sg}) dependence (I_{ds}). The current peaks when the side-gate voltage is swept between -2.5 and -4.0 V: a so-called Coulomb peak of the QD. Fig. 6-4 shows the V_{sg} dependence of the resistance of the charge sensor QD (R_{QD}). Fig. 6-5 compares the phase of S_{11} for V_{sg} = -3.5 and -4.0 V, for which the change in conductance is large. RF reflectometry can read out the change in the resistance and/or the capacitance of a QD due to the variation in the QD potential or the energy dispersion. However, the V_{sg}

dependence of the reflection phase of the QD is small enough to be neglected in this device, meaning that the reflection phase in the present circuit is insensitive to the resistance change. Its frequency dependence can be well fit by the RC model circuit with R_{QD} = 1.4 MΩ and C_{QD} = 65 fF using Equation (6-2), suggesting the model's validity in this frequency range. We note that this value of C_{QD} is smaller than the typical parasitic capacitance (on the order of several hundreds of fF) seen in the conventional reflectometry measurements with bond wires or transmission lines of PCBs included.

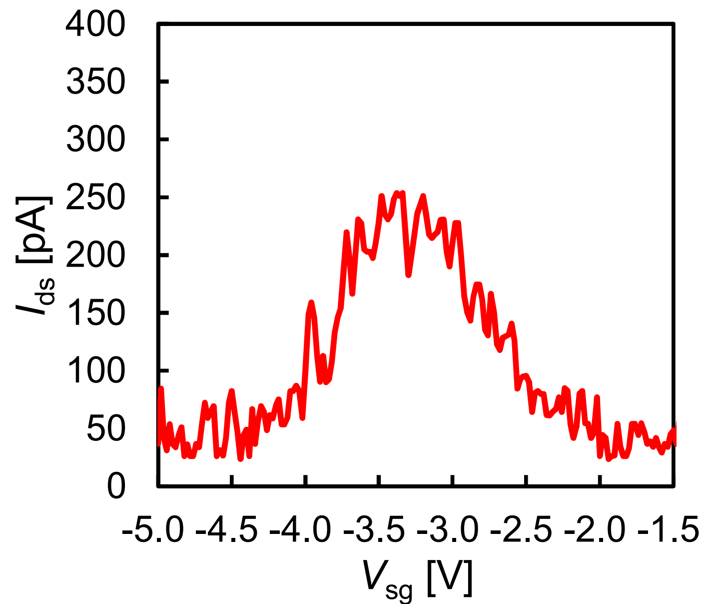


Fig. 6-3. Drain current dependence on the side-gate voltage.

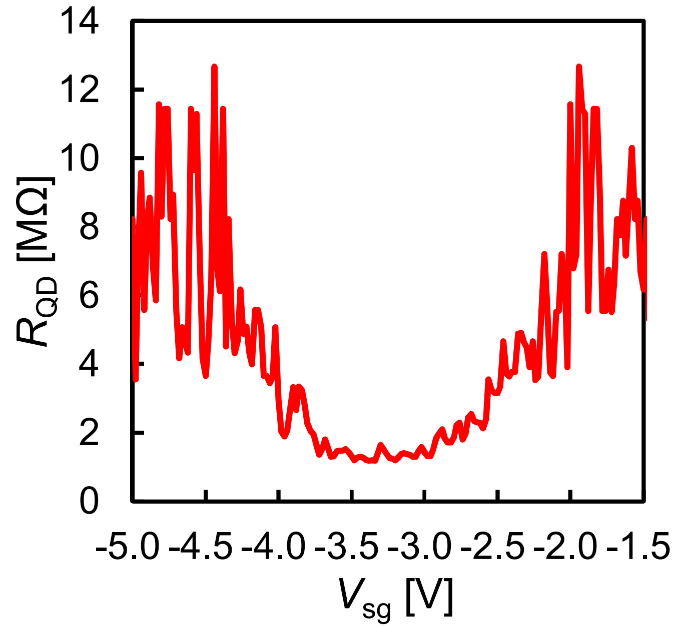


Fig. 6-4. Resistance of the charge sensor QD as a function of the side-gate voltage.

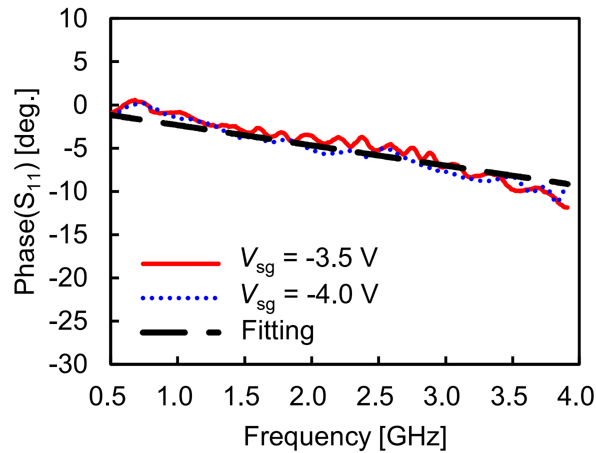


Fig. 6-5. Measured reflection phase of the S_{11}. The solid red (dotted blue) line shows the result for V_{sg} = -3.5 V, (-4.0 V) with smoothing applied. The dashed black line shows the fit result to the parallel RC circuit model for V_{sg} = -3.5 V, with the best values (R_{QD} = 1.4 MΩ and C_{QD} = 65 fF). The fitting of the result for V_{sg} = -4.0 V yields a very similar C_{QD} value.

6.4 Circuit design and analysis

The circuit model obtained above should help to devise the matching circuit towards improved sensing performance. In the following, three simple impedance matching circuits were considered, as schematically shown in Fig. 6-6, and a comparison is given in terms of sensitivity and impedance matching bandwidth. In all types (a, b, and c), the matching circuit has two elements, one series and one shunt. The charge sensor QD is modeled by an RC parallel circuit, parameterized by R_{QD} and C_{QD} which take the values of R_0 and C_0, respectively, under the default bias condition. The values of the components in the matching circuit for a given working (angular) frequency $\omega = \omega_0$ are then determined to match the input impedance of the overall circuits (Z_{x} with x = a, b, c) to the port impedance (Z_0). The sensitivity indexes to a change in R_{QD} (S_{R}) and a change in C_{QD} (S_{C}) for circuit x are defined as

$$S_{\mathrm{R}x} = \left.\frac{\partial |Z_x|}{\partial R_{\mathrm{QD}}}\right|_{R_{\mathrm{QD}}=R_0,\, C_{\mathrm{QD}}=C_0, \omega=\omega_0} \tag{6-3}$$

$$S_{\mathrm{C}x} = \left.\frac{\partial |Z_x|}{\partial C_{\mathrm{QD}}}\right|_{R_{\mathrm{QD}}=R_0,\, C_{\mathrm{QD}}=C_0, \omega=\omega_0} \tag{6-4}$$

respectively. The larger the absolute value of the index, the higher the sensitivity to the corresponding change. In addition, the frequency derivative of the impedance

$$D_{\omega x} = \left.\frac{\partial |Z_x|}{\partial \omega}\right|_{R_{\mathrm{QD}}=R_0,\, C_{\mathrm{QD}}=C_0, \omega=\omega_0} \tag{6-5}$$

can be used to evaluate the impedance matching bandwidth at the default bias. The smaller the absolute value of this value, the wider the impedance matching bandwidth. Calculation results for Circuit (a) are shown as

$$C_a = \frac{1}{\omega_0 R_0}\sqrt{\frac{R_0 - Z_0}{Z_0}} - C_0, \tag{6-6}$$

$$L_a = \frac{\sqrt{(R_0 - Z_0)Z_0}}{\omega_0}, \tag{6-7}$$

$$|S_{\mathrm{Ra}}| = \frac{\mathrm{Z}_0}{\mathrm{R}_0} - 2\left(\frac{\mathrm{Z}_0}{\mathrm{R}_0}\right)^2, \tag{6-8}$$

$$|S_{\mathrm{Ca}}| = 2\omega_0 Z_0 \sqrt{(R_0 - Z_0)Z_0}, \tag{6-9}$$

$$|D_{\omega\mathrm{a}}| = \frac{2(R_0 - Z_0)Z_0}{\omega_0 R_0}, \tag{6-10}$$

with restrictions of

$$\omega_0 < \frac{1}{C_0 R_0}\sqrt{\frac{R_0 - Z_0}{Z_0}}. \tag{6-11}$$

Calculation results for Circuit (b) are shown as

$$C_b = \frac{1}{\omega_0 \sqrt{(R_0 - Z_0)Z_0}}, \tag{6-12}$$

$$L_b = \frac{R_0 Z_0}{\omega_0\left(\omega_0 C_0 R_0 Z_0 + \sqrt{(R_0 - Z_0)Z_0}\right)}, \tag{6-13}$$

$$|S_{\mathrm{Rb}}| = \frac{\mathrm{Z}_0}{\mathrm{R}_0} - 2\left(\frac{\mathrm{Z}_0}{\mathrm{R}_0}\right)^2, \tag{6-14}$$

$$|S_{\mathrm{Cb}}| = 2\omega_0 Z_0 \sqrt{(R_0 - Z_0)Z_0}, \tag{6-15}$$

$$|D_{\omega b}| = \frac{2(R_0 - Z_0)Z_0}{\omega_0 R_0} + 4C_0 Z_0 \sqrt{(R_0 - Z_0)Z_0}, \tag{6-16}$$

without any restrictions. Calculation results for Circuit (c) are shown as

$$L_{c1} = \frac{R_0 Z_0}{\omega_0\left(\omega_0 C_0 R_0 Z_0 - \sqrt{(R_0 - Z_0)Z_0}\right)} - C_0, \tag{6-17}$$

$$L_{c2} = \frac{\sqrt{(R_0 - Z_0)Z_0}}{\omega_0}, \tag{6-18}$$

$$|S_{\mathrm{Rc}}| = \frac{\mathrm{Z}_0}{\mathrm{R}_0} - 2\left(\frac{\mathrm{Z}_0}{\mathrm{R}_0}\right)^2, \tag{6-19}$$

$$|S_{\mathrm{Cc}}| = 2\omega_0 Z_0 \sqrt{(R_0 - Z_0)Z_0}, \tag{6-20}$$

$$|D_{\omega\mathrm{c}}| = \frac{2(R_0 - Z_0)Z_0}{\omega_0 R_0} - 4C_0 Z_0 \sqrt{(R_0 - Z_0)Z_0}, \tag{6-21}$$

with restrictions of

$$\omega_0 > \frac{1}{C_0 R_0} \sqrt{\frac{R_0 - Z_0}{Z_0}}. \quad (6\text{-}22)$$

The calculated values of the circuit parameters for Circuits (a), (b), (c) are shown by Equations (6-6) and (6-7), (6-12) and (6-13), and (6-17) and (6-18), respectively. Interestingly, the resistance sensitivity indexes, $|S_{Ra}|$, $|S_{Rb}|$, and $|S_{Rc}|$, are the same values for the three circuit types, as given by Equations (6-8), (6-14), and (6-19). These expressions show that higher sensitivity to change in resistance of QD is obtained by lowering R_0 (closer to Z_0). The capacitance sensitivity indexes, $|S_{Ca}|$, $|S_{Cb}|$, and $|S_{Cc}|$, are also the same for the three circuits, as shown by Equations (6-9), (6-15), and (6-20). Based on the calculation, the capacitance sensitivity will be enhanced by increasing R_0 and ω_0. We noted that the sensitivity was improved for a smaller value of R_0 for resistance readout. In contrast, the opposite is the case for capacitance readout, meaning that the optimal condition depends on the readout mode. The bandwidth indexes, $|D_{\omega a}|$, $|D_{\omega b}|$, and $|D_{\omega c}|$, are shown by Equations (6-10), (6-16), and (6-21). The frequency bandwidths are wider in the order of Circuits (c), (a), (b). Based on the discussion up to this point, it may seem that Circuit (c) is the best among the three, with the widest bandwidth $|D_{\omega x}|$ and identical sensitivities ($|S_{Rx}|$, $|S_{Cx}|$). However, this circuit cannot always be used, because, for a particular combination of the values of R_0 and C_0, the shunt inductance value given by Equation (6-17) becomes negative (see also expression (6-22)). Circuit (a) becomes realizable in this parameter regime and will be the best choice among the three. The diagram of the best circuit as a function of R_0 and C_0 is given in Fig. 6-7 for several different values of the operation frequency, $\omega_0/(2\pi)$. In the lower left region of the line, Circuit (a) can be realized, and in the upper right region, Circuit (c) can be realized. A matching circuit with only one series inductor can be realized on the lines. The boundary is at 293 MHz for the extracted RC parameters. Once the equivalent circuit parameters are known, the optimal circuit configuration can be determined accordingly.

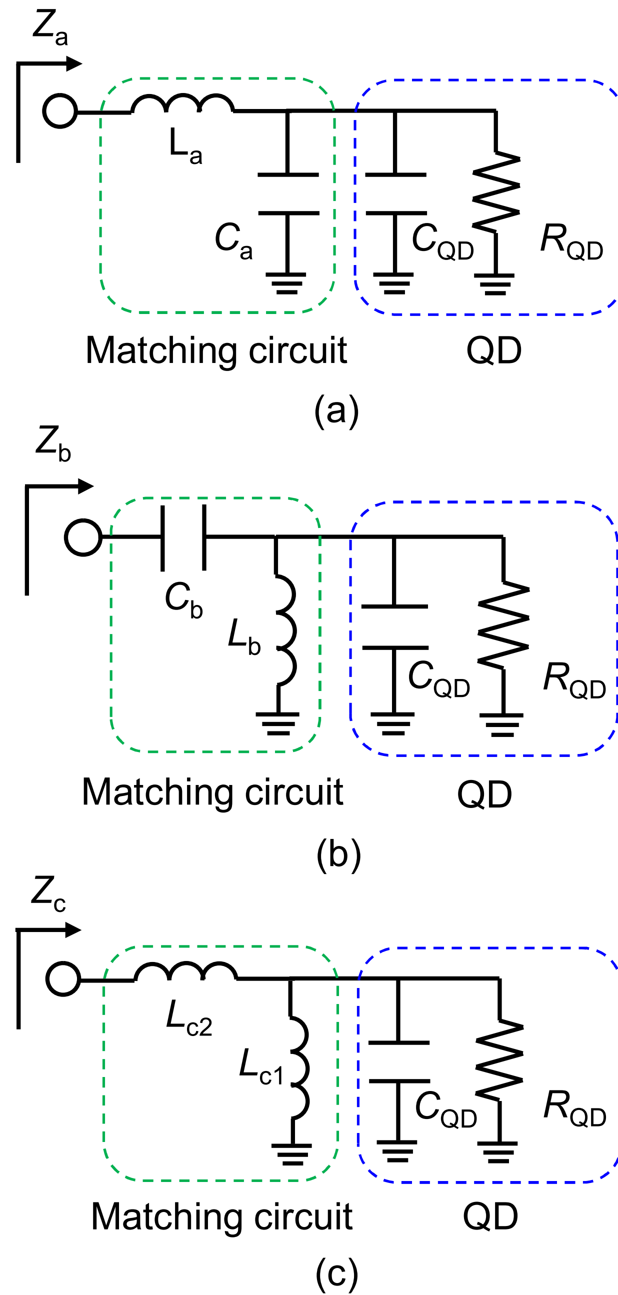


Fig. 6-6. Schematics of a matching circuit and a QD charge sensor. QD charge sensors are represented as resistance (R_{QD}) and capacitance (C_{QD}) in parallel. (a) Matching circuit with a shunt capacitor (C_a) and a series inductor (L_a). (b) Matching circuit with a shunt inductor (L_b) and a series capacitor (C_b). (c) Matching circuit with a shunt inductor (L_{c1}) and a series inductor (L_{c2})

Based on the analysis above, an optimal impedance matching circuit can be designed for our QD using the extracted equivalent circuit parameters (R_0 = 1.4 MΩ and C_0 = 65 fF. The default bias is V_{sg} = -3.5 V). The port impedance of the reflection measurement is assumed to be 50 Ω, the standard for normal measurement systems. The working frequency is assumed to be 2 GHz. We observed that a higher frequency leads to wider matching bandwidth (see (6-10), (6-16) and (6-21)) and compact circuit parameters, but it comes at the cost of the increased effects of parasitic components. Fig. 6-7 indicates that for the given parameters, Circuit (c) should be optimal in terms of the bandwidth with the resistance sensitivity equivalent to that from Circuit (b) while Circuit (a) cannot realize impedance matching. Using Equations (6-17) and (6-18), the circuit parameters are calculated as L_{c1} = 114 nH and L_{c2} = 666 nH. These values are about 1/10 times smaller than conventional shunt C-shunt L configuration operated at around 100 MHz. The performance of the designed circuit is checked by small-signal simulation. The reflection is calculated for different values of V_{sg} or R_{QD}, which emulates the effect of the electric field change at the sensor QD. Fig. 6-8 shows the frequency dependence of the reflection amplitude of the designed QD charge sensor for two conditions: R_{QD} = 1.4 MΩ and C_{QD} = 65 fF corresponding to V_{sg} = -3.5 V (the red solid trace) and R_{QD} = 5.1 MΩ and C_{QD} = 65 fF corresponding to V_{sg} = -4.0 V (the blue dashed trace). When V_{sg} is changed from V_{sg} = -3.5 V to -4.0 V, the reflection amplitude at 2 GHz changes from less than -40 dB to about -4.9 dB (owing to design accuracy and measurement accuracy, there is no predominant difference below -40 dB). The bandwidth of less than -10 dB at V_{sg} = -3.5 V is over 0.8 MHz, which is enough for the readout in 1.3 μs to obtain fidelity of 99% considering the dephasing time of 130 μs [28]. The bandwidth in the previous physically-defined QD sensor with a shunt capacitor-series inductor on PCB was 0.5 MHz (estimated readout fidelity of 98.5%). However, it is improved to 0.8 MHz by applying the on-chip shunt inductor-series inductor [145]. The obtained bandwidth is comparable

to the typical reported results with gate-defined QDs [132]. Controlling the tunneling resistance of physically-defined QDs is difficult and tends to be higher than that of gate-defined QDs, resulting in a narrow bandwidth. This problem is solved by proposing a new circuit configuration. Fig. 6-9 shows the R_{QD} dependence of the reflection amplitude at 2 GHz. The reflection amplitude is changed significantly when the value of R_{QD} is varied from R_{QD} = 1.4 MΩ, where the circuit is impedance matched to the 50 Ω system.

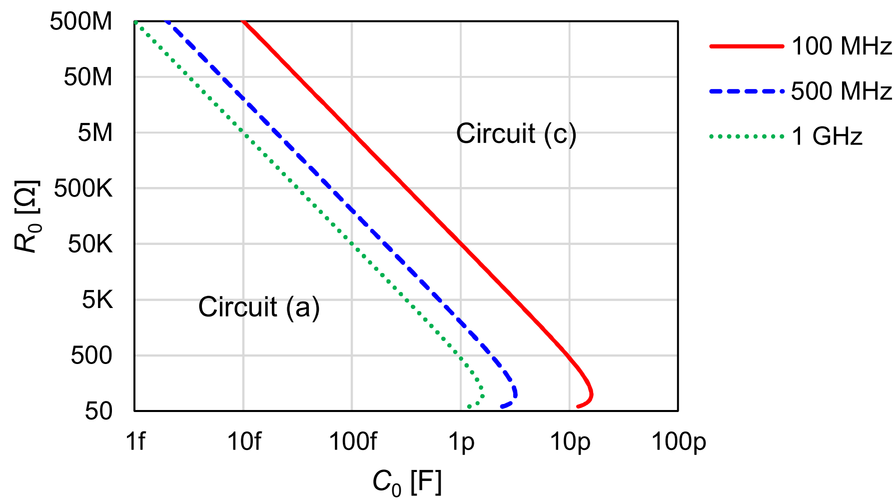


Fig. 6-7. Optimal circuit configuration when the resistance and the capacitance of the equivalent circuit of a QD are given. The red solid curve, the blue dashed curve, and the green dotted curve show the boundary between the optimal circuit configurations for the frequency of 100 MHz, 500 MHz, and 1 GHz, respectively.

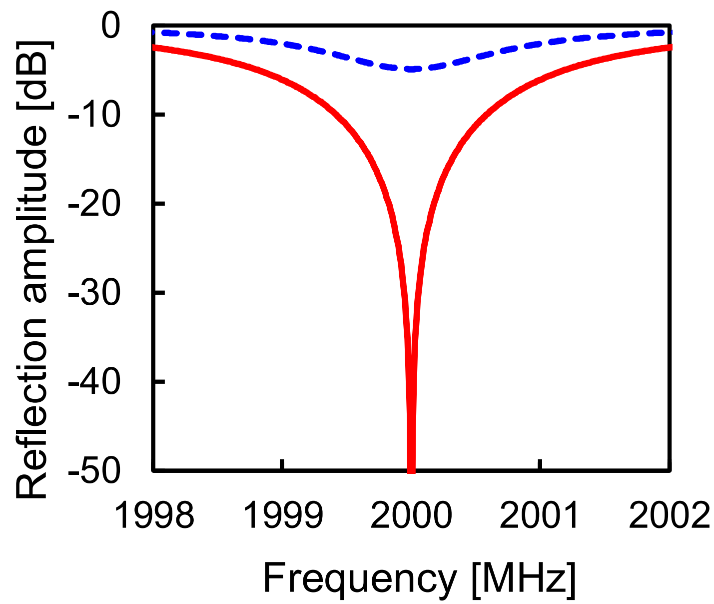


Fig. 6-8. Dependence of the reflection amplitude on the carrier frequency. The red solid line shows the reflection amplitude when R_{QD} = 1.4 MΩ and C_{QD} = 65 fF and the blue dashed line shows when R_{QD} = 5.1 MΩ and C_{QD} = 65 fF.

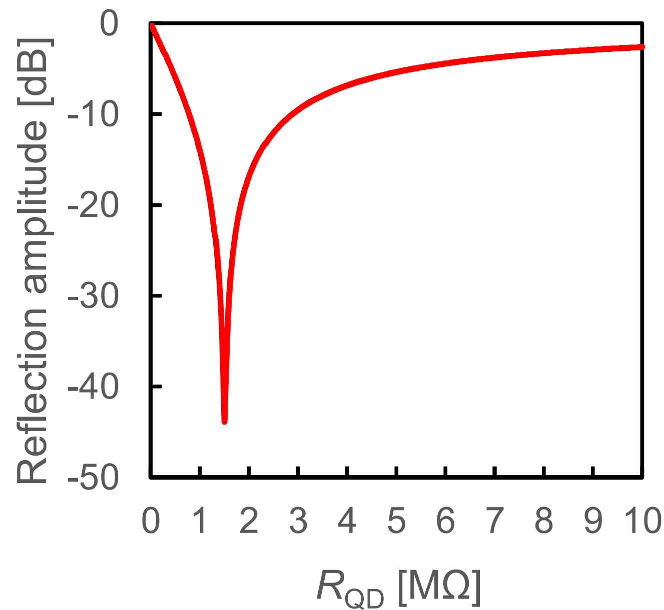


Fig. 6-9. Dependence of the reflection amplitude of the designed QD charge sensor on R_{QD} at 2 GHz with C_{QD} = 65 fF.

6.5 Conclusion

In conclusion, a physically-defined silicon QD device was measured. The equivalent circuit parameters of the QD chip at a cryogenic temperature were extracted from the S-parameter measurements in combination with a deembedding technique. Conventionally, shunt capacitor-series inductor circuits have been formed on PCBs in the matching circuit. We have proposed shunt inductor-series capacitor type and shunt inductor-series inductor type circuits. Design methodologies for the three matching circuits were established, with comparisons made regarding the sensing sensitivity and bandwidth. The design and the simulation of the impedance matching circuit with a series inductor and a shunt inductor were performed. The circuit design with smaller inductance than conventional configuration, which enables on-chip matching circuit and the wide bandwidth required for high-speed readout were realized. These results should facilitate the realization of RF reflectometry of semiconductor qubits on various QD platforms. Further miniaturization is possible by increasing the operation frequency using this analysis. However, because the effect of parasitic inductance is large at high frequency, the accuracy of the circuit design using the approximation of the equivalent circuit of QDs as an RC circuit is reduced. The measurement results here indicate that fitting RC circuits up to at least 4 GHz is feasible. For higher frequencies, extracting the equivalent circuit parameters with the closer measurement plane to the drain and the source of the quantum dots is desirable. The size of the developed matching circuit is compact enough for a noisy intermediate-scale quantum device (NISQ) with around 10^3 quantum bits but still large for the realization of fault-tolerant quantum computers with around 10^7 qubits. Reducing the number of matching circuits by time division readout using cryo-CMOS [135] or miniaturizing circuits using active inductors is necessary for further integration.

Chapter 7.

Conclusion

This Ph.D. thesis presents research on semiconductor MMICs for the advanced information and communication network. Chapter 1 explains the necessity of further development of wireless communication technology and quantum network technology in solving social issues. GaN high-power devices and silicon quantum dots devices for qubit are described as key components. It is also mentioned that research on MMIC technologies to improve their performance and make the size compact is important. Chapter 2 describes the importance of broadband, high efficiency, and low-cost GaN-MMIC HPAs, miniaturization, and broadband of silicon quantum dot charge sensors. The current status of these devices and the required performance were discussed in detail. In Chapter 3, we proposed a bandpass NDPA that achieves broadband and high output power. Two GaN-MMICs, single-end GaN-MMIC bandpass NDPA, and two-way combined GaN-MMIC bandpass NDPA were designed and evaluated. Measurement results of the two-way combined GaN bandpass distributed amplifier show output power of 44.3 to 47.9 dBm (27 to 61 W, 40 W on average), PAE of 24 to 43% (31% on average) at an input power of 38 dBm over 2.5 to 10.0 GHz (relative bandwidth of 120%). The measurement results demonstrated the effectiveness of the bandpass distributed amplifier by achieving the world's highest output power and power density among the other reported wideband MMIC HPAs. In Chapter 4, ISV structure with small via holes in all source fingers was applied to improve the performance of GaN amplifiers. We also optimized an output matching circuit by considering the trade-off relationship between load impedance and circuit loss. Measurement results of the developed X-band GaN-MMIC amplifier s 46.1–

47.4 dBm, PAE of 49–55%, and a gain of 10.1–11.0 dB at 8.5–10.5 GHz with a drain voltage of 30 V. Output power of 47.2–48.4 dBm, PAE of 52–54%, and gain of 11.2–12.1 dB were obtained at 8.5–10.5 GHz with a drain voltage of 35 V. The highest performance in terms of The highest performance in terms of output power and PAE combinations was demonstrated compared to existing state-of-the-art X-band MMIC HPAs. In Chapter 5, we studied the configuration of power amplifiers and a switch T/R module that achieves both low cost and high output power. We demonstrated a GaN-on-Si DA, a high gain GaN-on-Si HPA with a GaAs output matching circuit, GaN-on-SiC HPA with a GaAs matching circuit, GaN-on-Si HPA with GaAs output matching circuit and GaN-on-Si SW. Each device achieved comparable performance at about half the cost of conventional amplifiers.

Based on the findings in Chapters 3 to 5, we estimated the performance of a wideband amplifier for the virtualization of RUs. Fig. 7-1 shows the proposed amplifier configuration for the virtualized RU. The bandpass distributed amplifier shown in Chapter 3 shows a 40-W class amplifier with 120% relative bandwidth. Scaling to the lower frequency side with the same relative bandwidth will be possible because of the lower dielectric loss. It is estimated that a 40-W class amplifier can be realized in the 1200-4800 MHz range. Although it does not cover the entire 800–4800 MHz base station frequency in Sub-6, it provides broadband and high-power characteristics. To further broaden the bandwidth, applying stack amplifiers is one possible approach [62]. If the same output power can be achieved with half the gate width, ideally the parasitic capacitance would be halved, and a doubled relative bandwidth of half the 600–4800 MHz could be achieved in a rough estimate. Because there is a trade-off relationship between frequency bandwidth and the amount of mismatch, it may be possible to achieve a bandwidth of 800–4800 MHz with even flatter output power and PAE characteristics. Additional considerations would be necessary to reduce the effect of performance

degradation due to impedance mismatch between common-source FET and common-gate FET. Applying a dual-gate structure [146]–[149] would be one solution to the problem. The backoff PAE also needs to be improved for communication systems. Envelope tracking technique effectively improves efficiency by varying the drain voltage supplied to the amplifier according to the envelope of the transmitted signal, such that the amplifier always operates near the saturation point. Envelope tracking requires a wider bandwidth envelope amplifier as the communication bandwidth becomes wider, and the efficiency of envelope amplifiers becomes lower in the case of wideband communication such as 5G. The wideband amplifier in Chapter 3 has the maximum saturated PAE (43%) in the band, estimated to be improved to 45% by applying the ISV structure described in Chapter 4. Assuming that the envelope tracking amplifier can achieve the same PAE as at saturation output power, the backoff PAE will be about 35% when the efficiency of the envelope tracking power supply of 78% with a switching frequency of 400 MHz is considered [66]. While this value of PAE may be an acceptable range for a communication system, it is still low compared to narrowband amplifiers [65]. In combination with several other technologies, there is potential for improvement to increase efficiency. One approach is to improve the field plate structure of the FET. FET utilizing source field plate structure with reduced parasitic capacitance [150] and drain-connected field plate [151] shows a 3–5% improvement in PAE. The harmonic tuning technique will also be applicable [79], [111]–[117]. This technique can be applied only to the high-frequency side, not to affect the operation frequency. Utilizing a parallel LC circuit, which is low loss at operation frequency and open impedance at the second harmonic at the high-frequency side of the operation frequency will be effective [79]. The technique may improve PAE by 2–6% according to the result of the second harmonic load-pull simulation given in 5.5.1. By utilizing these technologies, achieving PAE of over 50% at saturated output power and 40% backoff PAE will be realizable. For lower cost, a partial

MMIC configuration combining GaN-on-SiC FETs and GaAs matching circuits can be used to reduce cost without sacrificing performance as shown in Chapter 5. Although there are still issues related to frequency bandwidth, efficiency improvement, and linearity, we showed a path toward full virtualization of the base station. Bandwidth, output power, efficiency, and cost (circuit size) are in a trade-off relationship, and there were limitations in adjusting circuit constants based on existing circuit configurations. We have shown that these trade-off relationships can be improved and performance can be enhanced by proposing new circuit configurations, applying new device structures, and appropriately combining different MMICs. These technologies are expected to be applied not only to amplifiers for telecommunications, but also to various applications such as radar and wireless power transmission.

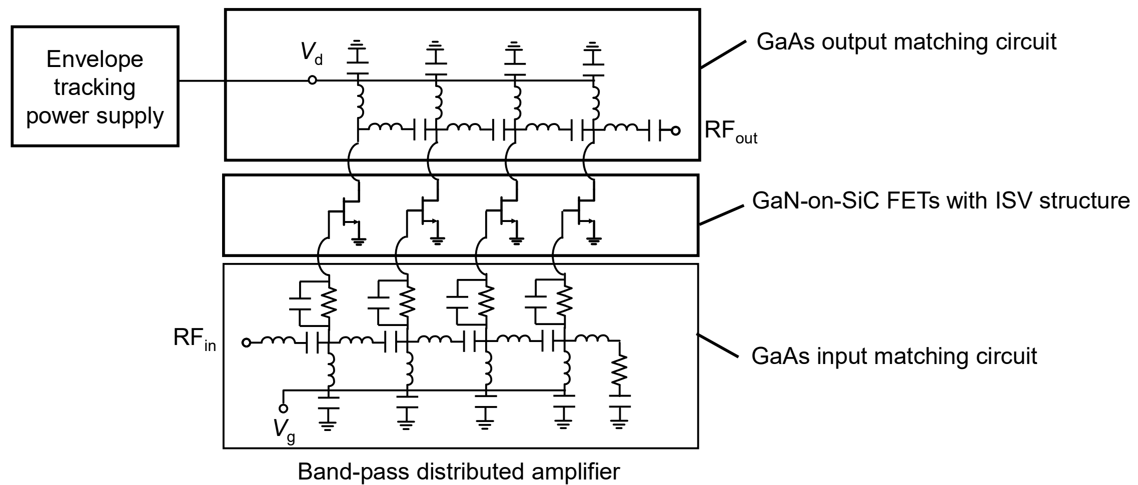


Fig. 7-1. Proposed amplifier configuration for the virtualized RU

In Chapter 6, the design of compact and wideband on-chip matching circuits of quantum dot charge sensors based on RF reflection measurement toward fast readout of a qubit state is implemented. To reduce the size and broaden the bandwidth of the matching circuit, we extracted the equivalent circuit parameters at the silicon chip of the

quantum dots device. We also formulated circuit constants of three matching circuits, the shunt capacitor-series inductor, shunt inductor-series capacitor, and shunt inductor-series inductor. We compared them in terms of sensitivity and frequency bandwidth. By designing a matching circuit with a newly proposed shunt inductor-series inductor type, wide bandwidth enough for fast readout of qubit states within the dephasing time is obtained. In addition, a design with circuit constants that can be on-chip has been realized, showing the prospects for integrating multi-qubits. The size is compact enough for NISQ with around 10^3 quantum bits but still large for realizing of fault-tolerant quantum computers with around 10^7 qubits. For further integration, reducing the number of matching circuits by time division readout using cryo-CMOS [135], miniaturizing the circuit components using active inductors [138], or 3D packaging technology is necessary. For high-fidelity spin manipulation and readout, not only circuit improvement but also process improvement is necessary. Charge noise is said to be the limiting factor for phase relaxation time. Charge noise is generated by charge entering and leaving defects and impurities in the device, and it is important to reduce these effects. For silicon quantum dots, dangling bonds at the Si/SiO_2 interface [152] and defects at the interface between the insulating layer under the top gate and Si must be reduced. Optimization of process conditions such as cleaning, surface passivation, deposition, and annealing conditions is necessary. In addition, the balance between the top gate and side gate voltages may also reduce the charge noise [153]. Improving the circuits, the device and the operation are important to increase spin manipulation and readout fidelity. Future research on these topics will bring us closer to the realization of quantum computers by reducing the number of qubits required for quantum error correction.

We proposed new circuit configurations and optimized circuits that were impossible with discrete configurations for the requirements of next-generation communication systems and achieved state-of-the-art results. The requirements for RF components are

expected to become more stringent, and MMIC technology will continue to play an increasingly important role in meeting these requirements. Designing MMICs with higher functionality and integration will become increasingly important. Chiplet and heterogeneous integration have also been studied extensively for yield improvement, cost reduction, and performance optimization [154]. Applying these technologies with interconnects smaller than bonding wire to partial MMICs technologies described in Chapter 5 makes it possible to support even higher frequencies and smaller modules. In the future, it will be more important to consider the appropriate partitioning of chips considering function, cost, and yield. It will also be necessary to consider the performance of MMICs and their cooperative operation to optimize their performance when connected to other chips.

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