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1T1C FeRAM memory array with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film

Jun Okuno

Thesis

Submitted in Partial Fulfillment of the Requirements for the Degree of

Doctor of Engineering

Thesis Advisor: Professor Hitoshi Wakabayashi

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ABSTRACT

1T1C FeRAM memory array with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film

Jun Okuno

Since the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-based material was reported in 2011, there has been much discussion about its application to 1T1C FeRAM. However, the feasibility of practical memory array operation using practical 1T1C memory cell structures has never been discussed. In this thesis, a novel 64 kbits of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array with dedicated CMOS logic circuit was integrated into 130 nm CMOS technology node and demonstrated the memory array operation for the first time. As a result, perfect functionalities in 64 kbits arrays and array operation at 2.0 V with sub 10 ns were demonstrated using 8 nm thick $Hf_{0.5}Zr_{0.5}O_2$. The memory window dependence on the ferroelectric capacitance area revealed that this technology has the potential for future scaling to capacitor areas of 0.1 μm^2 toward 40 nm CMOS technology node. Cycling tolerance of hard breakdown of the 1T1C FeRAM memory array was investigated, revealing the 1 ppm Raw-Bit-Error-Rate at 2.0 V, 100 ns, and 85°C operation was predicted to be > 10^{15} cycles, based on the dependence of time to breakdown on the stress voltage. Considering a degradation of the remanent polarization due to a fatigue, the memory window was decreased post 10^8 cycles. This degradation can be recovered by applying higher stress cycling on the MFM with keeping the distribution of memory window. These results should encourage the mass production of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM, which has been at the research level until now.

1 Introduction

1.1 Background

An edge computing architecture has been gaining attention in recent years due to its low latency, low data transaction, and high security communications compared to a cloud computing architecture[18–20]. In the edge computing, huge amount of calculation for inference of image, speech and language is required at distributed internet-of-things (IoT) edge devices illustrated in Figure 1.1. For applications where it is difficult to secure a power supply or replace batteries, low-power consumption and small-footprint edge IoT devices are desired (Figure 1.2). Such edge IoT devices use various types of memory, such as static random access memory (SRAM), dynamic random access memory (DRAM), and NAND FLASH memory, which serve as a storage or working memory. Therefore ultra-low-power and small-footprint memories are strongly desired.

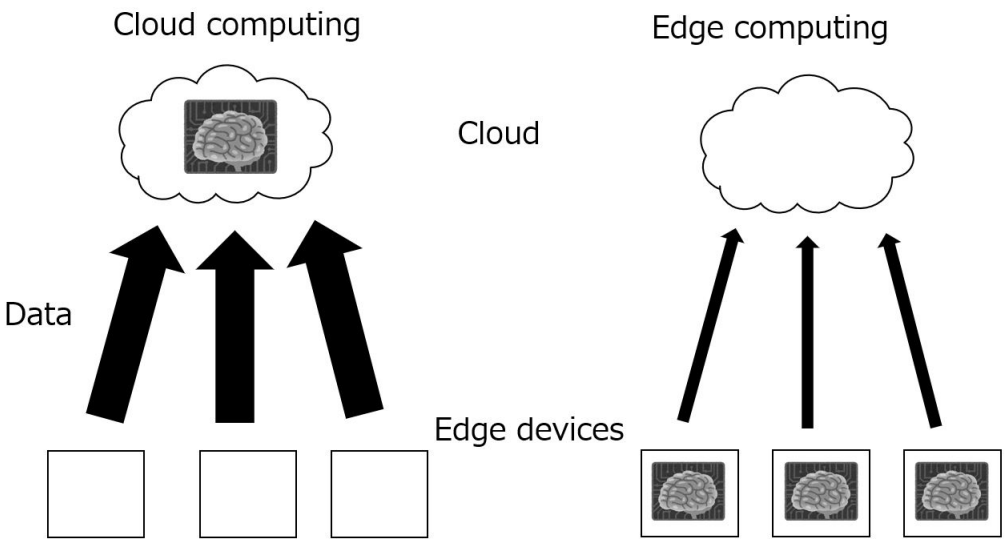


Figure 1.1. Illustration of cloud computing and edge computing architectures.

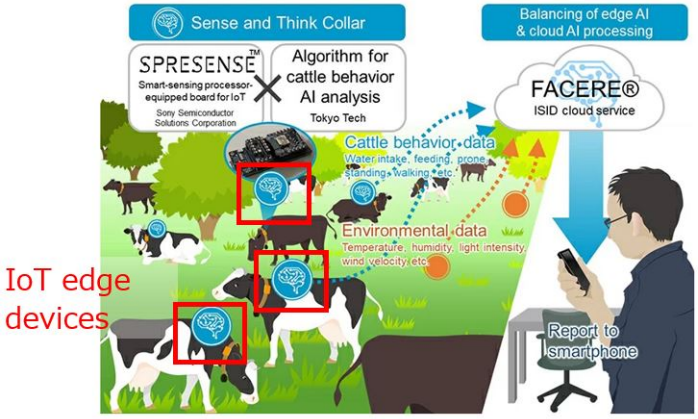


Figure 1.2. Use case of the edge IoT device application[4].

Figure 1.3 is illustrating a hierarchical structure of memory showing trade-off between capacity and latency. Because of the trade-off between capacity and latency, memory system needs to be divided according to the application. SRAM is commonly used for the highest speed application near Central Processing Unit (CPU) such as register, layer 1 cache (L1) to last level cache (LL). It has an advantage of high speed operation, but requires large footprint because a memory cell consists of more than 5 transistors. Since SRAM is a volatile memory, it has the problem that standby leakage increases power consumption. NAND flash memory is widely used as a storage memory because of its high density and non-volatility, although it operates at low speed. It requires high voltage (> 10 V) to store the data, resulting in large energy consumption during write operation. DRAM is used as primary working memory to bridge the performance gap between SRAM and NAND FLASH. Since it is volatile memory, it requires refresh operations at regular intervals (once every 64 ms), which increases power consumption. Since different memories are used for different purposes, the problem is that a lot of power consumption is generated during data transfer between memories. Therefore, embedded memory that replaces all or part of the memory system is desired to reduce power consumption.

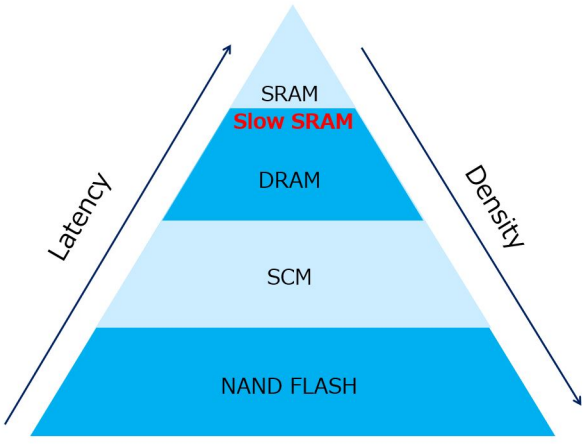


Figure 1.3. Hierarchical structure of memory showing trade-off between capacity and latency.

Table 1.1 is a comparison table of performance in embedded memories. Although several emerging or emerged memories such as embeded flash memory (eFlash), resistive Random Access Memory (RRAM) , spin torque transfer magnetic RAM (STT-MRAM) and perovskite-based ferroelectric RAM (barium titanate ($BaTiO_3$)[21] and later in lead zirconate titanate (PZT)[22], have been suggested to achieve the replacement, but no one accomplish it due to limitation of write energy, endurance and scaling resulting from high process cost caused by complex structures.

Table 1.1. Comparison table of performance in embedded memories.

	SRAM	eDRAM	eFlash	eRRAM	STT MRAM	Perovskite-FeRAM
Non-volatile	No	No	Yes	Yes	Yes	Yes
Write voltage	$>$ 0.5V	$>$ 1.0 V	$\sim$ 10 V	2 $\sim$ 3 V	2 V	$>$ 1.5 V
Write speed	$<$ 1 ns	20 $\sim$ 100 ns	$\sim$ 10 µs	1 $\sim$ 100 µs	10 ns	10 $\sim$ 100 ns
Endurance	10^{16}	10^{16}	10^5	10^6	10^9	10^{15}
Energy	Standby leak	Dynamic refresh	High	High	High	Low
Scaling	5/7 nm	28 nm	28 nm discontinued	40 nm discontinued	$<$ 22 nm	180 nm discontinued

1.2 Ferroelectricity of hafnium-oxide-based material

The ferroelectricity of hafnium silicon oxides ($HfSiO_2$) was first reported in 2011[23], showing the presence of a polar orthorhombic phase in $HfSiO_2$ thin films that contributes to their ferroelectricity. Compared to conventional perovskite ferroelectric materials, HfO_2-based ferroelectric materials have the advantages that they can be deposited by an atomic layer deposition (ALD) method and have better compatibility with CMOS processes since HfO_2 is widely used in front-end processes. This advantages indicates that HfO_2-based ferroelectric materials have potential for application in state-of-the-art CMOS technology nodes.

HfO_2 exhibits ferroelectricity due to an appearance of the polar orthorhombic $Pca2_1$ phase group, which didn't exist in the conventional classical phase diagram as described in Figure 1.4. In this lattice configuration, the oxygen atoms can take two equilibrium positions corresponding to the two opposite directions of polarization. When an external electric field is applied, oxygen atoms move from one equilibrium position to another by polarization switching.

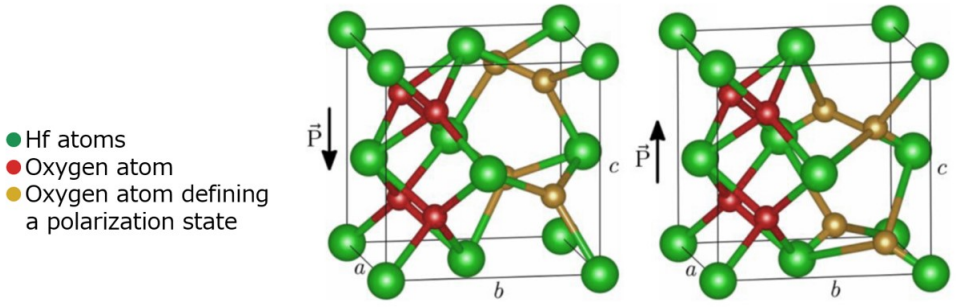


Figure 1.4. Schematic diagram of a $Pca2_1$ unit cell corresponding to polar-orthorhombic phase with two opposite polarization directions in hafnium oxide. Picture was taken with permission[5].

Figure 1.5 shows a polarization (P) vs. electric field (E) for the typical ferroelectric behavior. The electric dipole on the surface of a ferroelectric material is called "spontaneous polarization" because the centers of gravity changes to positive or negative spontaneously. The direction of spontaneous polarization is reversed when an external electric field is applied. The value of the polarization remaining on the surface at the absences of external electric field is called "remanent polarization (Pr)" and the value of the electric field when the polarization reverses is called the "coercive field (Ec)". When a sufficiently strong electric field is applied, all mobile charge is transferred to the surface. This is called the saturated state, and the value of polarization at this time is called the "saturation polarization value (Ps)". All of these parameters have a polarity of positive or negative.

Table 1.2 shows ferroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ comparing with another ferroelectric materials. The Pr and Ec of $Hf_{0.5}Zr_{0.5}O_2$ have been reported to be competitive with other materials.

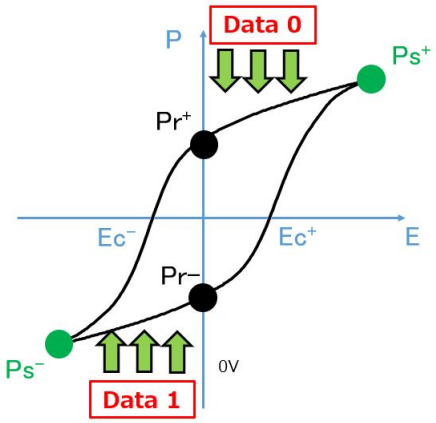


Figure 1.5. Polarization vs. electric field for ferroelectric behavior.

Table 1.2. Comparison table of ferroelectric properties[1,2].

	PZT	SBT	AlScN	$Hf_{0.5}Zr_{0.5}O_2$
Pr [μC/cm²]	40 ∼ 90	10 ∼ 20	80 ∼ 140	30 ∼ 60
Ec [MV/cm]	0.05	∼ 0.05	2 ∼ 5	0.8 ∼ 2
k	1300	150 ∼ 250	∼ 25	∼ 30

1.3 Application of hafnium-oxide-based ferroelectric material

In past two decades, ferroelectric memory application based on $Hf_{0.5}Zr_{0.5}O_2$ have been extensively discussed for their low switching current due to the polarization switching, their compatibility with the CMOS process, and their scaling potential as described in Figure 1.6. Table 1.3 shows a performance comparison table between three typical $Hf_{0.5}Zr_{0.5}O_2$-based memory application such as ferroelectric field effect transistors (FeFETs)[24], ferroelectric tunnel junctions (FTJs)[25,26], and one-transistor and one-capacitor ferroelectric random access memories (1T1C FeRAMs)[27].

FeFETs are capable of non-destructive read schme and multi-bit write operations and are suitable for higher density devices. However, the dielectric film formed between the ferroelectric gate oxide film and the Si interface can cause charge trapping and degradation of reliability and variability of the characteristics. Several studies have been conducted to address these issues. The choice of a back-gate FeFET structure with a channel-last process flow can achieve the higher endurance behavior[28].

FTJs have been proposed as two-terminal resistance-change devices with a ferroelectric layer and an interface layer between two metal electrodes. The device has advantages of nondestructive readout with high density, and proposed as potential applications in neuromorphic computing devices. The retention properties due to depolarizing magnetic fields are controversial. To overcome this challenge, optimization of the film stack and operating voltage has been proposed[25].

1T1C FeRAM has an excellent interface layer between the metal electrode and the ferroelectric layer, which enables high endurance, low operating voltage, and disordered operation despite destructive readout operation. However, from the discovery of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$, FeFETs attracted much attention owing to single transistor structure. On the other hand, the development of 1T1C FeRAM

has been delayed from FeFETs due to the complexity of the process to form integrated capacitors and the need for a dedicated circuit to identify minute capacitance changes and read them out destructively. Therefore, research has been limited to basic evaluation using the MFM structure.

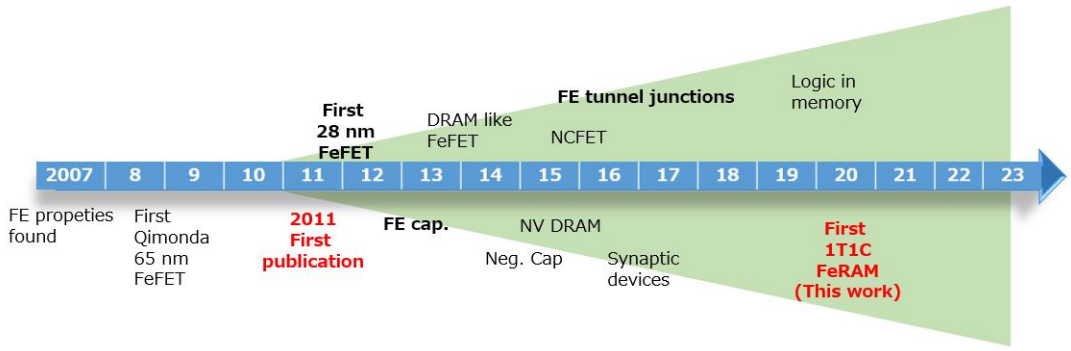


Figure 1.6. Chronology of semiconductor ferroelectric science and industry discoveries and advances since first reported. Picture is adapted from work[6].

Table 1.3. Comparison table of performance in $Hf_{0.5}Zr_{0.5}O_2$-based memory devices[1].

	FeFET[28]	FTJ[25]	1T1C-FeRAM[29]
Non-destructive read	Yes	Yes	No
2-terminal stucture	No	Yes	No
Write Voltage (< 2 V)	No	No	Yes
Endurance ($> 10^6$)	No	No	Yes
Memory array operation	Yes	No	This thesis

1.4 Challenges of conventional methods

There have been many reports on fundamental properties of $Hf_{0.5}Zr_{0.5}O_2$-based materials toward 1T1C FeRAM application. In a conventional method, a large area (larger than 100 μm^2) of metal/ferroelectric/metal(MFM) capacitor has been commonly used to amplify small displacement currents as shown in Figure 1.7. However, following matters remains controversial.

(1) CMOS process compatibility
(2) Ferroelectric properties under practical use case ($<$ 100 kHz)
(3) Uniformity of ferroelectric properties at realistic MFM size.
(4) Reliability of small MFM capacitors

First, integration process of MFM is needed to be optimized according to the CMOS process. In particular, the thermal budget is limited depending on the CMOS process, so material optimization is necessary. Second, large capacitor causes large RC delays during measurement and cannot apply ideal pulses shape, which limits their operating speed. It has been reported that this issue can be solved by extrapolating from the frequency dependence of lower than 100 kHz[30], but for a more realistic study, direct measurements around 100 MHz are desired. Third, it is essential for 1T1C FeRAM to be able to separate high and low states even at several megabits, so it is important to investigate the capacitance variation of both states in a realistic MFM structure. Finally, reliability of ferroelectricity of realistic MFM capacitors using memory array under practical use case is inevitable for the feasibility study of 1T1C FeRAM application. Recently, process integration of memory arrays with realistic MFM structures with 110 nm CMOS technology node has been reported[29]. However, memory array operation using dedicated circuits such as address decoders and sense amplifiers (SA) in $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM under actual use conditions has never been reported.

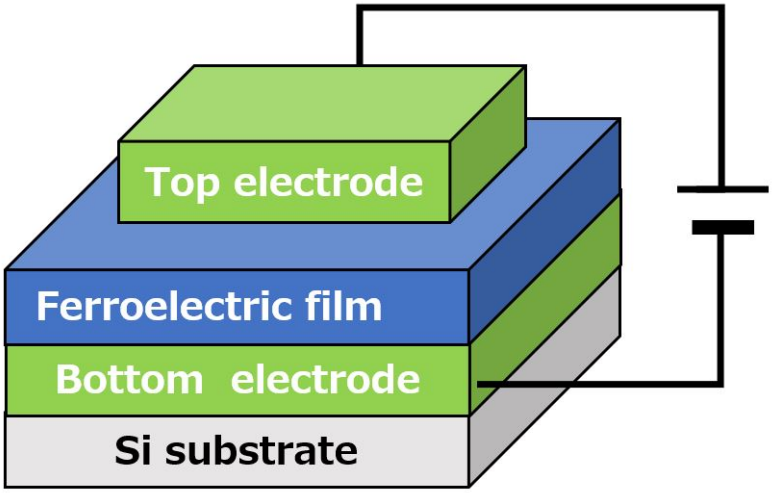


Figure 1.7. Illustration of a conventional test structure for MFM with larger than 100 μm^2.

1.5 Motivation of this thesis

In this thesis, a feasibility study of 1T1C FeRAM with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film was experimentally performed to address challenges as mentioned in Section 1.4. First, $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film was developed for integrating it into 130 nm CMOS technology node considering the thermal budget in Chapter 2. Second, a novel 64 kbits 1T1C FeRAM memory array with small MFM capacitors (0.4 μm^2) based on $Hf_{0.5}Zr_{0.5}O_2$ film using a dedicated CMOS logic circuit was integrated into 130 nm CMOS technology in Chapter 3, and memory array performance was investigated to verify the ferroelectric properties under practical use case (100 kHz) in Chapter 4. Third, memory window analysis using the 1T1C FeRAM memory array was studied to reveal a variability of ferroelectricity of small MFM capacitors and predict the scalability toward more advanced CMOS technology in Chapter 5. Finally, film thickness scaling to reduce operating voltage and improve cycling tolerance for hard breakdown was studied and a recovery effect from the fatigue was comprehensively investigated by applying various operating condition to verify the reliability of small MFM capacitors.

The target performance was defined as shown in Table 1.4, taking other technologies into account. This thesis focuses on $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM as a slow SRAM replacement for ultra-low power and small area embedded memory as shown in Figure 1.3. The target of write voltage was defined to be around 2.0 V, assuming a 40nm CMOS technology node as the first stage of scaling. Aiming for a speed between SRAM and DRAM, the target of write speed was set at about 20 ns. Since high endurance was required for low-speed SRAM replacement, the target of write endurance was set to more than 10^{15} cycles. No any other technologies, such as conventional FeRAM and $Hf_{0.5}Zr_{0.5}O_2$-based FeFET have never achieved these targets. $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM is included for reference, but as mentioned in Section 1.3, it is not the result based on memory array operation. To accomplish this targets, a 64 kbits of 1T1C FeRAM with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film was fabricated with dedicated CMOS logic circuits to demonstrate its memory array operation for the first time.

Table 1.4. Target performance comparing with another technology.

	SRAM	eDRAM	perovskite-based FeRAM	$Hf_{0.5}Zr_{0.5}O_2$-based FeFET[24]	$Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM[29]	Target
Non-volatile	No	No	Yes	Yes	Yes	Yes
Write voltage	>0.5 V	>1.0 V	1.0 V	4.2 V	4.0 V	~ 2.0 V
Write speed	<1 ns	~ 20 ns	20 ns	20 ns	100 ns	~ 10 ns
Endurance	10^{16}	10^{16}	10^{15}	$\sim 10^5$	10^{11}	$\sim 10^{15}$
Retention	Volatile	Volatile	125°C 10 years	no data	125°C 10^4sec	85°C 100 min
Scalability	5/7 nm	28 nm	180 nm	28 nm	No data	=< 40 nm

1.6 Structure of this thesis

In this thesis, feasibility study of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM was experimentally performed for the first time. Figure 1.8 explains the structure of this thesis. In Chapter 1, a target characteristics is defined comparing other emerging technologies. In Chapter 2, materials used in the 1T1C FeRAM are mentioned. In Chapter 3, experimental of the process integration and design of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAMs are mentioned. In Chapter 4, a memory array operation of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM are discussed . In Chapter 5, an improvement to reduce the operation voltage is conducted by film thickness scaling of the ferroelectric layer using 1T1C FeRAM. In Chapter 6, the fatigue characteristics of the HZO based 1T1C FeRAM memory array, which has never been addressed before is discussed. In Chapter 7, all results on this thesis are summarized and matters which are not covered in this thesis are mentioned.

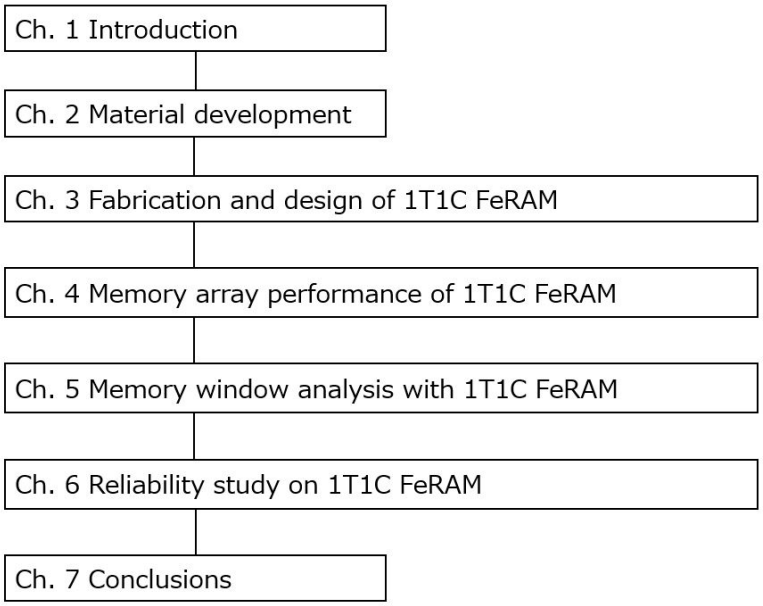


Figure 1.8. Structure of this thesis.

2 Material development

2.1 Introduction

This chapter mentions about ferroelectric materials which was used for 1T1C FeRAM. To obtain ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$-based materials, appropriate thermal budget is required to crystallize the film. Since process conditions depend on dopants, thickness, and materials for the bottom and top electrodes, it is important to select dopants and check their thermal stability when incorporating them into conventional CMOS process flows. In this thesis, an intrinsic material properties were developed using a single large MFM capacitors prior to install them into a 1T1C FeRAMs. In Section 2.2, a selection of the dopant and optimization method for the $Hf_{0.5}Zr_{0.5}O_2$-based materials are described. In Section 2.3, the thermal stability emulating the thermal budget in CMOS process are mentioned including the intrinsic reliability.

2.2 Material selection for ferroelectric films

In the past decade, ferroelectricity has been reported in HfO_2 thin films doped with many different elements[31] and ZrO_2 [14,32]. Even un-doped HfO_2 is known to emerge ferroelectricity[33] . Unlike other dopant species, Zr substitutes Hf atoms in large amounts. In this case, the term "solid solution" is more appropriate than "doping". Since both Zr and Hf are IV-valent elements with identical atomic radius, they are often classified as "sister substances". One of the major advantages

of using Zr as a dopant of Hf is that it has wider concentration window to obtain ferroelectric properties with more flexible process[7,34]. Furthermore, its low thermal budget process allows to fabricate the ferroelectric material by compatible process with well developed knowledge from DRAM[35]. Therefore, HZO layers are widely studied in ferroelectric device applications.

Various factors contributes to the stabilization of the metastable polar orthorhombic phase such as surface and volume effects[7], dopant atom incorporation, the presence of oxygen vacancies[8,9], and mechanical stress[10–12], and rapid cooling[13] as described in Figure 2.1. The layers appear to transition from the monoclinic phase to the polar orthorhombic phase and then to the tetragonal phase with increasing content. Previous studies have obtained the dependence of the remanent polarization values as a function of concentration, finding a peak around a Hf:Zr ratio of 1:1, indicating that the orthorhombic phase is most sufficiently detected[14,34,36]. Therefore, this work focuses on the characterization of $Hf_{0.5}Zr_{0.5}O_2$ films.

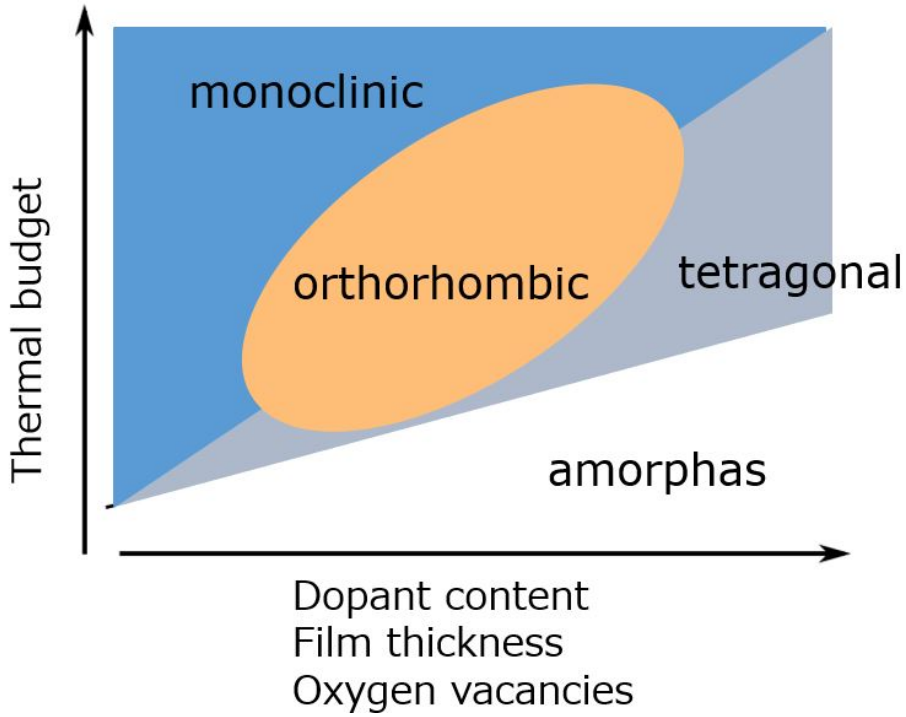


Figure 2.1. Schematic illustration of crystal phase of ferroelectric HZO.[7–13]

There is a lot of methods to fabricate the ferroelectric layer such as atomic layer deposition (ALD), physical vapor deposition (PVD)[37],chemical vapor deposition (CVD)[38], pulsed layer deposition (PLD)[39]. chemical solution deposition (CSD)[40]. However ALD is the most widely used for the ferroelectric layers since its mono-atomic-layer deposition is suitable to deposit thin films with good uniformity and excellent step coverage. The ALD cycle consists of two self-limiting processes in Figure 2.2. First, when metal precursors are pulsed into the surface, then they are absorbed on the available sites of the substrate with a mono-atomic-layer. Next, the oxidizer such as H_2O, O_2 and O_3 are then also introduced into the chamber reacting with the absorbed metal precursor molecules and creates mono-atomic-layer. It reacts with the absorbed metal precursor molecules to form a sub-mono-atomic-layer of metal oxide. In between these two steps, purging is performed to remove un-reacted molecules and byproducts. If theses precursor reaction and purging process are not optimized correctly, residual reactants can affect the quality and homogeneity of the layer.

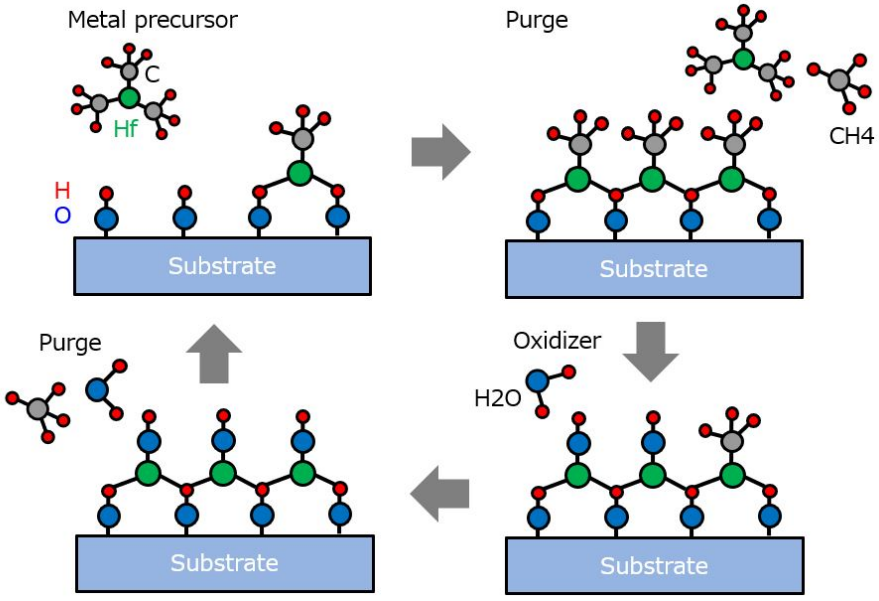


Figure 2.2. Schematic illustration of an ALD cycle.

Since impurities, thermal stability, and dense layers depend on molecules in precursors, the choice of precursor is important to obtain high residual polarization. Figure 2.3 shows a remanent polarization as a function of Zr content in HZO for a different metal precursors, TEMA-Hf (Zr) (Hf[N(CH_2)(C_2H_5)], Zr[N(CH_3)(C_2H_5)]), TDMA-Hf (Zr) (Hf[N(CH_3)$_2$]$_4$), Zr[N(CH_3)$_2$]$_4$)), cyclopentane (Cp)-based precursors (Zr-yALD, Hf-yALD). As a result, the largest remanent polarization is obtained by TEMAHf + ZyALD combination. The reason for this could be that ZyALD has high thermal stability because it belongs to the Cp group. Therefore, the precursor molecules are transported to the active surface of the substrate surface without dissociation even at film deposition temperatures, resulting in homogeneous Cp desorption and oxidation reactions. In addition, the residue of carbon-based reaction products generated by other organic precursors is less likely to be generated, which is said to reduce leakage paths in the film and provide good film quality.[41,42]

Process condition of the oxidizer is an important parameter that fluctuates the amount of oxygen deficiency in the film as described in Figure 2.1. Figure 2.4 shows a Contour plots report which is depicting the amount of each crystalline phase (m-phase, polar o-phase, and t-phase) as a function of ozone exposure time (x-axis) and Zr content (y-axis). The amount of the crystalline phase is calculated from the de-convolution of the measured grazing incidence X-ray diffraction (GIXRD) signals using TEMAHf + ZyALD precursors.

Therefore, TEMAHf + ZyALD precursors were chosen as precursors to deposit $Hf_{0.5}Zr_{0.5}O_2$ layers films and the condition of oxidizer were optimized.

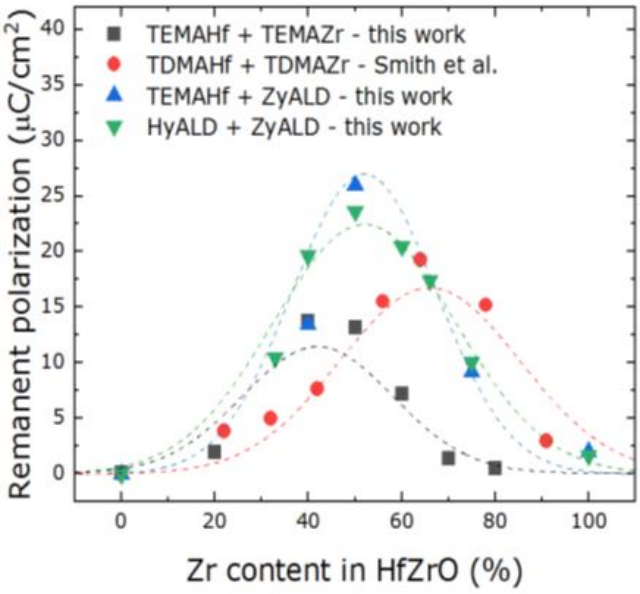


Figure 2.3. Remanent polarization as a function of the Zr content in the film for different Hf- and Zr-based precursor combinations[14–16]. Picture was taken with permission[14].

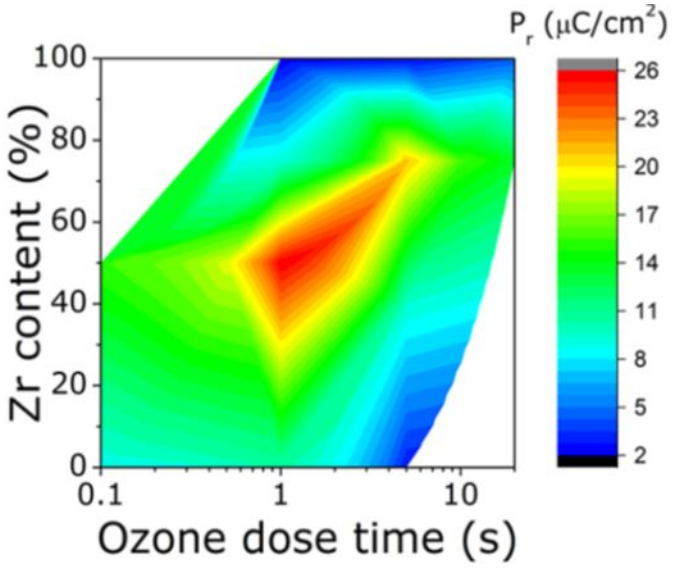


Figure 2.4. Contour plots for a remanent polarization as a function of Zr content and ozone dose time[14–16]. Picture was taken with permission[14].

2.3 Thermal stability of the ferroelectric material

Large round MFM capacitors with a diameter of 100 μm were fabricated to investigate the ferroelectric characteristics dependence on the Rapid Thermal Anneal (RTA) temperature. Both 10 nm thick TiN electrodes were sputtered using PVD method. Different RTA temperatures of 450°C and 500°C were used to crystallize the MFM capacitors. 450°C for 30 s and 500°C for 30 s were performed, and control samples without RTA treatment were also processed. The existence of polar-orthorhombic ferroelectric phase in large MFM capacitors of 100 μm diameter was investigated by grazing incidence X-ray diffraction (GIXRD). Figure 2.5 shows the GIXRD data for all three variations; the highest intensity was observed when annealing was performed at 500°C for 30 seconds, but no significant intensity was detected when no RTA was performed. This indicates that the films can be crystallized by annealing at a temperature of at least 450°C in this experiment. The remanent polarization of these capacitors with RTA at 450 and 500°C was characterized by polarization versus voltage measurements, as shown in Figure 2.6. Ferroelectric hysteresis behavior due to the ferroelectric polar-orthorhombic phase was obtained for both samples, with the sample annealed at 450°C showing lower remanent polarization than the sample annealed at 500°C (2Pr, 40 $\mu C/cm^2$). This indicates a greater proportion of ferroelectric orthorhombic crystals in the sample annealed at 500°C, as shown in the GIXRD results in Figure 2.5.

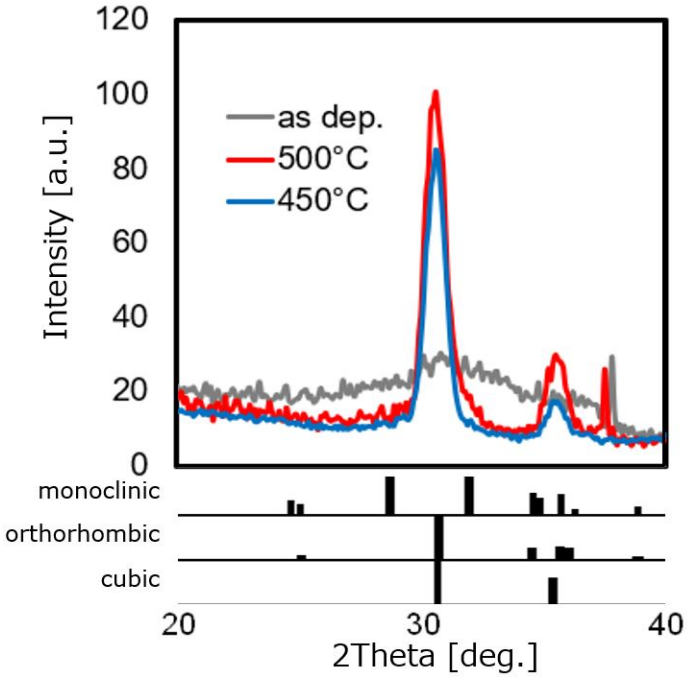


Figure 2.5. GIXRD spectrum of the TiN/HZO/TiN stack annealed at 450°C, 500°C and without annealing.

As shown in Figure 2.7, the cycling endurance performance was investigated up to 10^9 cycles with a cycle frequency of 100 kHz and a rectangular pulse shape. For the sample RTA at 500°C, stable residual polarization is observed up to 10^9 cycles, after which the capacitor begins to fatigue. Considering the difference from the frequency in actual use conditions (10 MHz), the cycle durability of 10^9 measured at 100 kHz is expected to be equivalent to 10^{11} cycles at 10 MHz if the durability characteristics correspond to the accumulated stress energy. Figure 2.8 shows retention tests of the same state (SS) and opposite state (OS) measured on samples subjected to RTA at 500°C[32]. A smaller change in polarization was observed at 500°C than at 450°C during 1000 min at 85°C . The retention result at 500°C can be projected to result in a slight degradation, even after 10 years applying a fitting model of power-law for the result above 10 min, considering charge trapping and the migration[17,43].

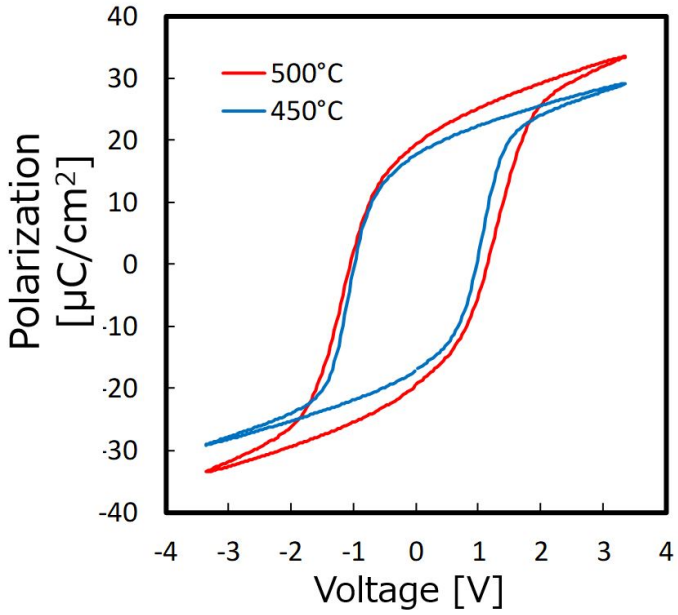


Figure 2.6. Polarization vs voltage hysteresis of the MFM capacitors after RTA at 450 and 500°C and for 30 s after 100 cycles at 1 kHz. The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept.

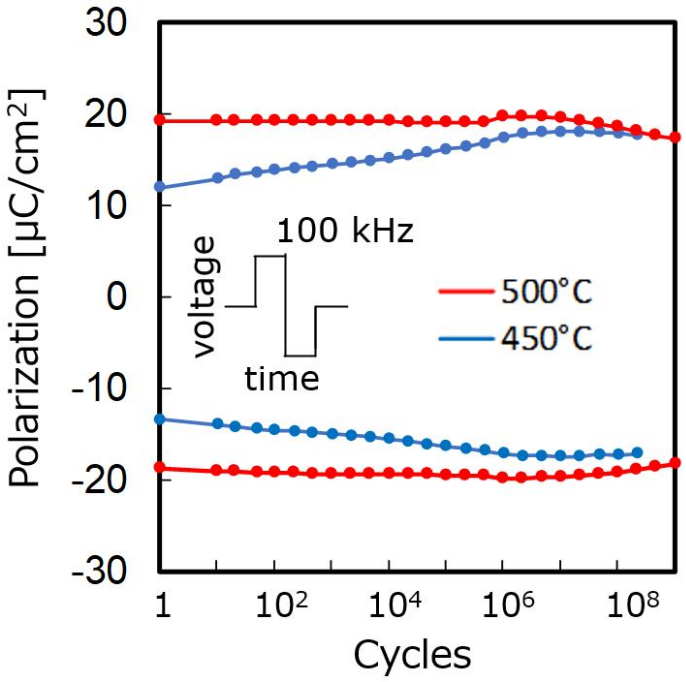


Figure 2.7. Cycling tolerance of the MFM capacitors after RTA at 450 and 500°C for 30 s. Cycling tolerance for 3 V amplitude at 100 kHz up to 10^9 cycles. Inset Figure shows the pulse shape.

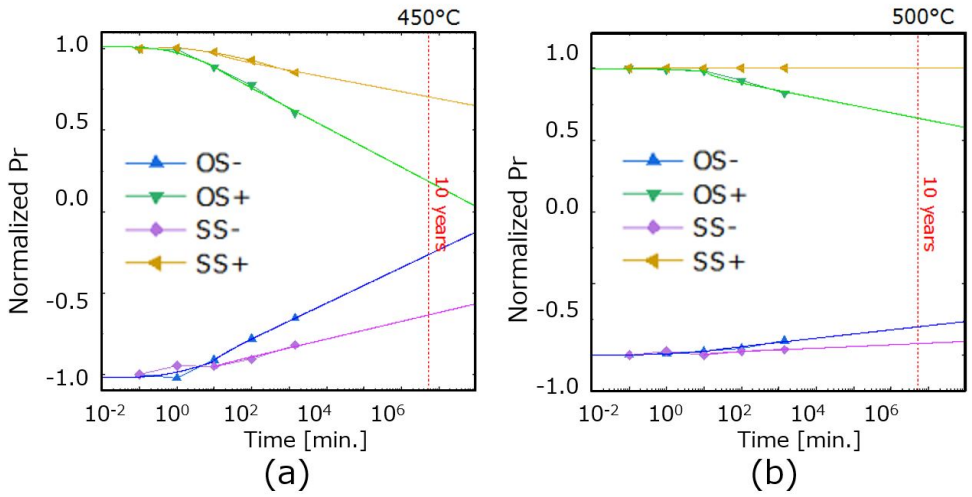


Figure 2.8. Data retention up to 1000 min baking time at 85°C for the same state (SS) and the opposite state (OS) after RTA at (a) 450°C for 30 s and (b) 500°C for 30 s. The lines are prediction to 10 years using fitting model of previous report[17].

2.4 Summary

$Hf_{0.5}Zr_{0.5}O_2$ was chosen as a ferroelectric material from large concentration window and CMOS compatibility point of view. TEMAHf + ZyALD precursors materials as precursors to deposit $Hf_{0.5}Zr_{0.5}O_2$ films and the condition of oxidizer were optimized to obtain higher remanent polarization.The reason for this could be that ZyALD has high thermal stability because it belongs to the Cp group. Therefore, the precursor molecules are transported to the active surface of the substrate surface without dissociation even at film deposition temperatures, resulting in homogeneous Cp desorption and oxidation reactions. In addition, the residue of carbon-based reaction products generated by other organic precursors is less likely to be generated, which is said to reduce leakage paths in the film and provide good film quality.

The impact of the RTA temperature on the ferroelectricity was investigated using single large capacitors. Higher remanent polarization and better endurance for RTA at temperatures up to 500°C were demonstrated. This thermal budget is applicable for 1T1C FeRAM process with a capacitor under bit line structure. Cycling endurance on the single capacitor was projected to be more than 10^{11} cycles considering accumulative energy. Retention characteristics on the single capacitor was projected to be more than 10 years at 85°C.

3 Fabrication and design of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM

3.1 Introduction

This chapter mentions about experimental and design of 1T1C FeRAM with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film. A 64 kbits of 1T1C FeRAM with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film was fabricated with dedicated CMOS logic circuits to demonstrate its memory array operation for the first time. As described in Chapter 1, the conventional characterization method using a large capacitance MFM capacitor (larger than 100 μm^2) is difficult to read and write the state of the ferroelectric capacitor in the order of 100 ns due to the RC delay. To address the issue, practical size of MFM capacitors (smaller than 1 μm^2) was fabricated to avoid the RC delay, and dedicated sense amplifier (SA) was design to detect the small capacitance change derived from the small capacitor.

As mentioned in Chapter 2, since ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ requires appropriate thermal budget to obtain ferroelectricity, capacitor under bitline structures are selected to avoid a degradation of back-end-of-line process. In Section 3.2, the concept was described followed by the process flow in Section 3.3. In Section 3.4, design for the 1T1C FeRAM is described which is mainly focus on the read scheme to overcome a destructive read operation of the 1T1C FeRAM. In Section 3.5, the thermal stability of the characteristics of the CMOS transistor suffering from the RTA temperature was confirmed by electrical measurements.

3.2 Capacitor under bitline structure

There are mainly two MFM structures, capacitor under bit line (CUB) and capacitor over bitline (COB) described in Figure 3.1. In the case of CUB structure the MFM capacitors are fabricated prior to the back-end-of-line (BEOL) process as a middle-of-line (MOL), while MFM are located on top of the wiring layer of BEOL process for COB structure. The advantage of the COB structure is that the MFM is on the top layer, which allows for greater flexibility when creating a three-dimensional MFM structure. While, CUB structure allows 1T1C FeRAM to avoid a degradation of BEOL wiring layers from thermal budget during crystallization anneal on metal/ferroelectric/metal (MFM).

Large area (> 1000 μm^2) MFM of ferroelectric materials. Most studies on doped $Hf_{0.5}Zr_{0.5}O_2$ films employ high rapid thermal annealing (RTA) above 500°C to obtain large remanent polarization ($2Pr > 40\ \mu C/cm^2$) [31,44,45].However, high thermal budgets affect transistor performance and back-end-of-line (BEOL) reliability when incorporated into state-of-the-art CMOS manufacturing processes[46], while high crystallization annealing temperatures contribute to higher density memory applications with capacitors with thinner ferroelectric layer, resulting in high remanent polarization.

To date, MFM capacitors made of TiN/HZO/TiN have been incorporated into the BEOL process with COB structure by applying temperatures below 450°C to avoid metal layer degradation, demonstrating the functionality of 1T1C FeRAM arrays without degrading CMOS characteristics[29]. In this work, we have applied the CUB structure to acquire larger remanent polarization by applying higher thermal budget over 450°C to the ferroelectric capacitors.

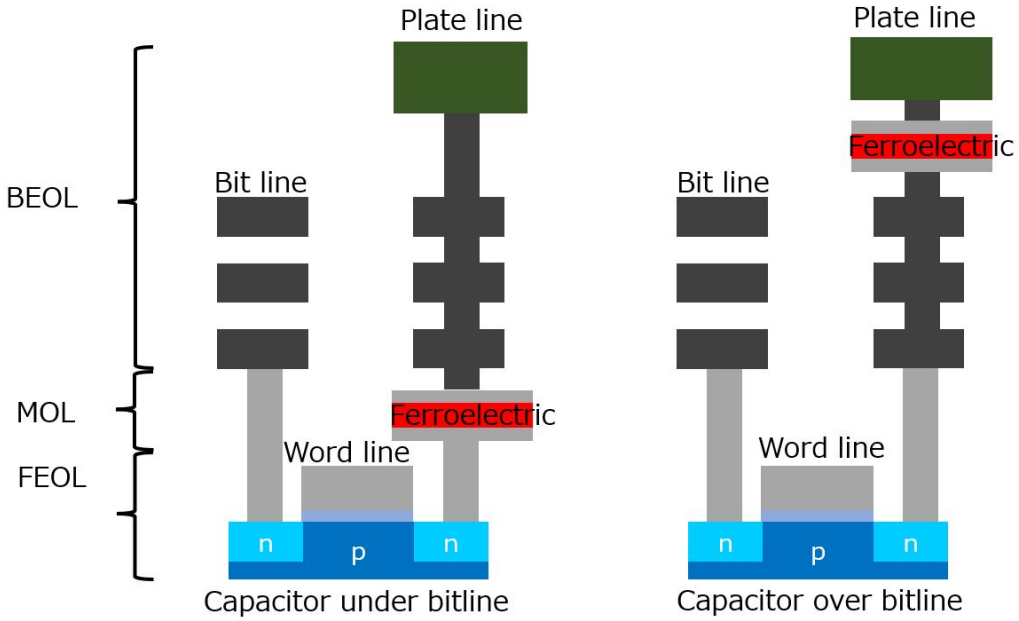


Figure 3.1. Schematic illustration of capacitor under bitline structure (left) and capacitor over bitline structure (right).

3.3 Process flow

The ferroelectric material as described in Figure 2.2 was implemented in a 64 kbits one-transistor and one-capacitor (1T1C) FeRAM array fabricated in 130 nm CMOS technology. Figure 3.2 shows an optical micrograph of the test chip, showing the presence of four mats on the chip with MFM capacitor areas of 0.4, 0.6, 0.8 and 1.0 μm^2 in the 1T1C memory cells, respectively. Figure 3.3 shows a scanning electron microscope cross section of a 1T1C cell containing an MFM capacitor.The MFM capacitor, consisting of a TiN/HZO/TiN stack, is integrated directly on top of the transistor in the CUB structure and crystallized before the BEOL metal interconnect process at a maximum temperature of 500°C and a holding time of 30 s annealing was possible. A two-step etching process is used to protect the sides of the HZO film from processing damage (ion, electron, UV, etc.). Direct patterning process could allow to reduce a MFM capacitance area, but it is necessary to consider increased leakage current and mechanical stress fluctuations due to the etching damage.

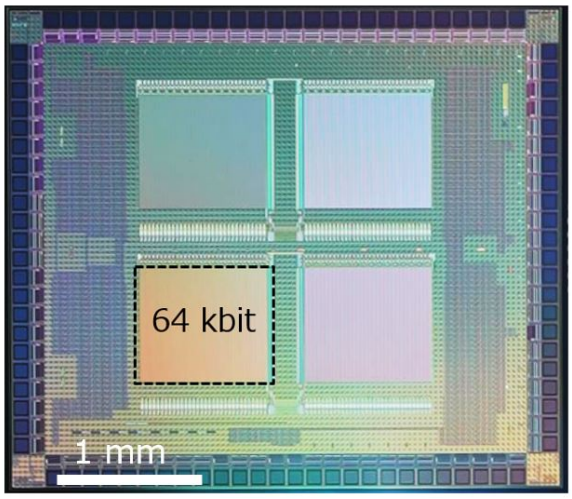


Figure 3.2. Optical microscope image of the 64 kbits 1T1C FeRAM test chip.

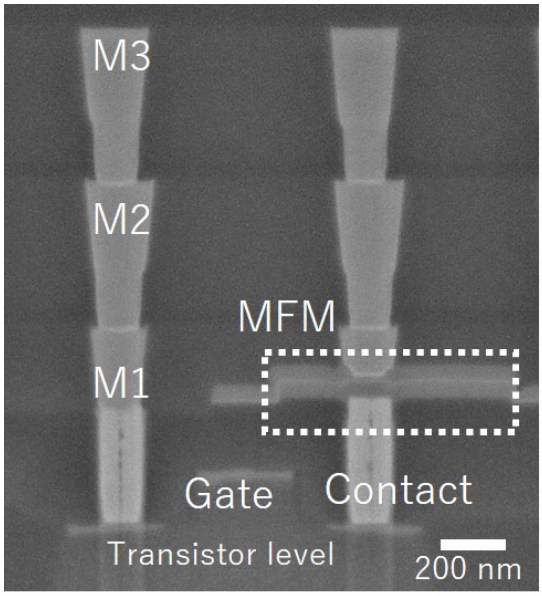


Figure 3.3. Scanning Electron Microscope cross section of one 1T1C cell.

The process flow of the fabricated CUB-structured 1T1C FeRAM is schematically shown in Figure 3.4. After the traditional CMOS front end of line (FEOL) fabrication process, a 50 nm thick of PVD-TiN bottom electode was deposited and patterned, as illustrated in Figure 3.4 (a). Next, $Hf_{0.5}Zr_{0.5}O_2$ and CVD-TiN top electrode were deposited with thicknesses of 10 and 50 nm, respectively, as shown in Figure 3.4 (b). Subsequently, RTA at 500°C was applied for 30 s using a rapid thermal process, as shown in Figure 3.4 (c), and the MFM was patterned using a reactive ion etching process (Figure 3.4 (d)). Finally, a passivation film was deposited by CVD method and, the contacts between the first metal layers (M1) to both the substrate and top electrode TiN were fabricated simultaneously, as shown in Figure 3.4 (e) and Figure 3.4 (f). Therefore, this CUB-structured 1T1C FeRAM facilitated flexible RTA engineering at a low process cost.

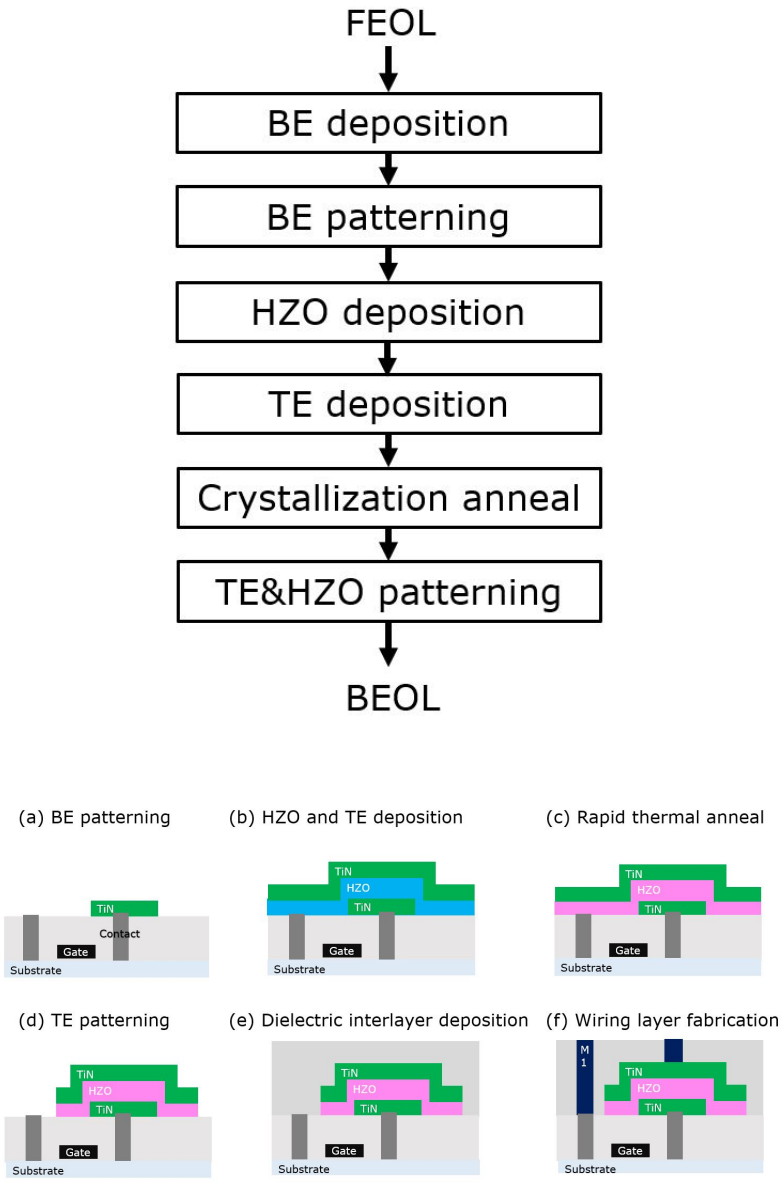


Figure 3.4. Process flow for the fabrication of the capacitor under bitline structure.

3.4 Design of 1T1C FeRAM memory array

Ferroelectric switching in a 1T1C FeRAM array with CUB structure was verified by integrating a dedicated sense amplifier (SA) in a CMOS integration process. Figure 3.5 shows the schematic design of the SA. 1T1C cells are connected to bit lines (BL), word lines (WL), and plate lines (PL). In this figure, 1T1C cell for read is connected to bit lines true (BLT), while that for reference is connected to bit lines bar (BLB). A transient switching or non-switching of the MFM (C_{FE}) depending on the state of the MFM capacitor, generates voltage changes in the bit line voltage (ΔV_{BL}) when the PL voltage is applied to the MFM capacitor. Furthermore, two states of the capacitor are defined as data0 and data1 in Figure 3.6. Data0 is corresponding to the downward polarity when a positive PL voltage is applied to the capacitor. On the other hand, data1 is corresponding upward polarity when the positive BL voltage is applied. The change in bit line voltage ΔV_{BL} that occurs during read is compared to a reference voltage (V_{REF}) generated from a reference capacitor (C_{REF}) or an externally applied voltage.

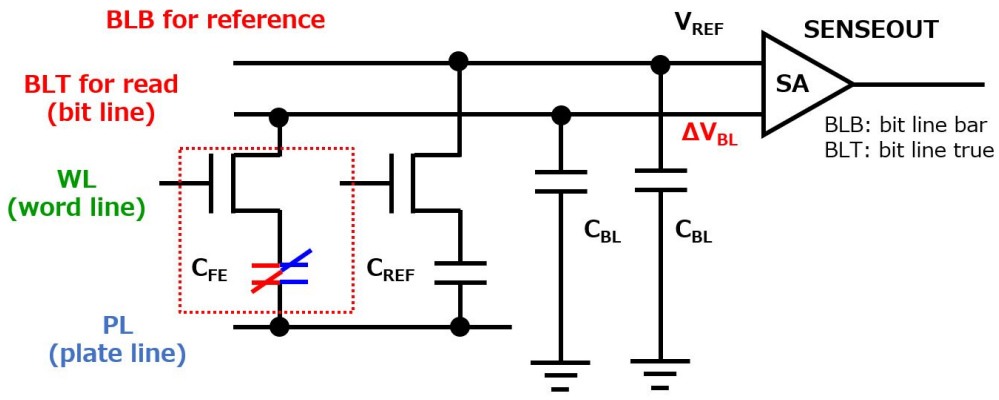


Figure 3.5. Schematic design of SA for read-out operation.

1T1C FeRAM is a destructive read method, and once data1 is read, it is converted to data0. Therefore, a step-pulse detection method is used to write the state back to the initial state[47]. Figure 3.7 shows a timing diagram of the proposed method simulated using Spectre, which is commercially available from Cadence. The ferroelectric capacitor is modeled using the following equation:

$$\Delta V_{\mathrm{BL}} = V_{\mathrm{PL}} \frac{C_{\mathrm{FE}}}{(C_{\mathrm{FE}} + C_{\mathrm{BL}})} \tag{3.1}$$

In this scheme, the read operation is divided into four periods from Δt0 to Δt3. In the Δt0 period, ΔV_{BL} is pre-charged to ground. In the Δt1 period, PL is activated, and ΔV_{BL} is generated. The amount of the ΔV_{BL} is determined resulting from the voltage divider between the C_{BL} and C_{FE}. The C_{FE} is defined as C_{FE}low and C_{FE} high as described in Figure 3.6. C_{FE}low is the linear dielectric capacitance of the ferroelectric capacitor, while in C_{FE}high, the effect of the switched polarization Psw = 2 Pr in charging the bitline needs to be added. In the period Δt2, the SA is activated by a sense enable (SE) pulse that turns on the power supply of the cross-coupled SA. If ΔV_{BL} is larger than V_{REF} , the SA destructively amplifies V_{BL} to VDD, turning the state of the ferroelectric capacitor from C_{FE}high to C_{FE}low. In this case, the original state is written back to data1 during Δt3 by the PL voltage V_{PL}. In contrast, if ΔV_{BL} is smaller than V_{REF}, V_{BL} is discharged to the ground, keeping C_{FE}low during periods Δt2 and Δt3

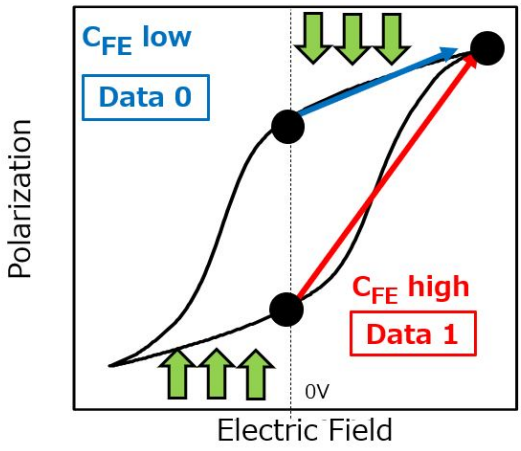


Figure 3.6. Definition of two different polarity states, data0 and data1. Data0 is defined as the polarization up state, whereas data1 is defined as the polarization down state.

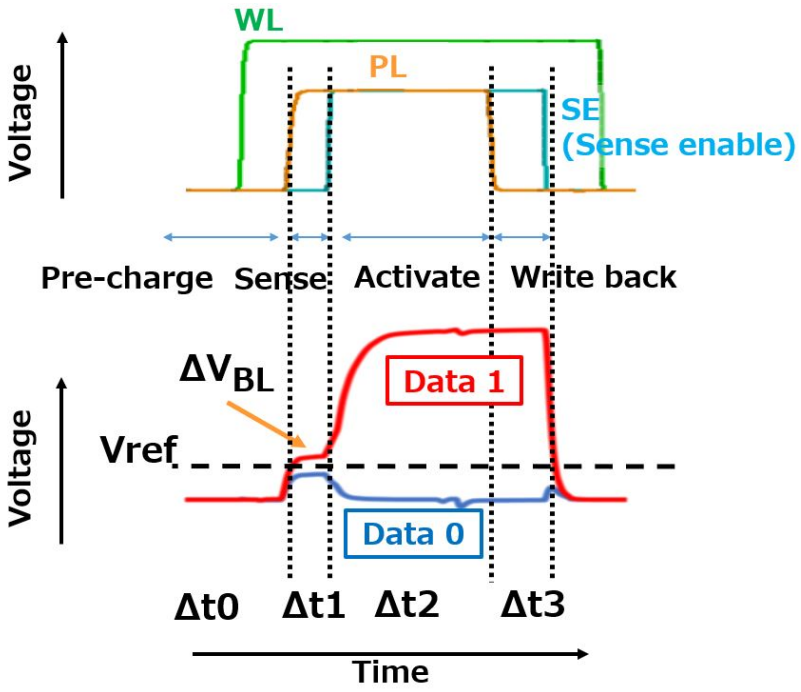


Figure 3.7. Schematic illustration of a step pulse sensing scheme using SA.

3.5 CMOS characteristics

The thermal stability of the characteristics of the CMOS transistor by the RTA temperature was confirmed by electrical measurements. Figure 3.8 shows the drain current versus gate voltage (Id-Vg) characteristics of both P-channel metal oxide semiconductor (PMOS) and N-channel metal oxide semiconductor (NMOS) transistors with or without RTA at 500°C for 30 s. Neither threshold voltage shift nor current reduction caused by the RTA was observed, indicating that the capacitor under bitline (CUB) structure endures thermal stress without degradation of the transistor characteristics. This occurs as the thermal budget, which is significantly higher than 500°C, was already processed at FEOL in 130 nm CMOS technology. Even if the PMOS and NMOS transistors were fabricated by cutting edge technology, the RTA of 500°C would not significantly affect the CMOS characteristics[46].

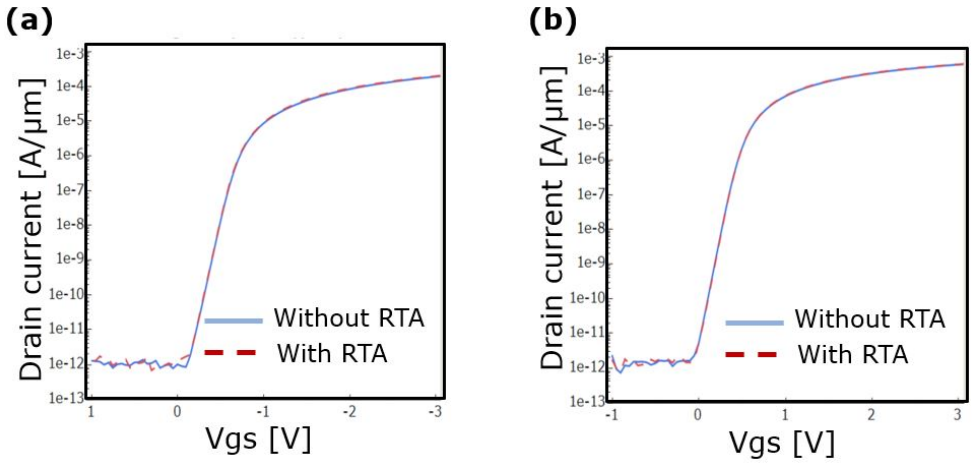


Figure 3.8. Id-Vg transfer characteristics of CMOS transistors for (a) PMOS and (b) NMOS with and without 500°C RTA.

3.6 Summary

The 64 kbits of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array was experimentally implemented into a 130 nm CMOS technology with capacitor under bit line structure for the first time. It allows 1T1C FeRAM to apply higher thermal budget to obtain higher remanent polarization of $Hf_{0.5}Zr_{0.5}O_2$-based materials than a capacitor over bit line structure. Four mats on the chip with MFM capacitor areas of 0.4, 0.6, 0.8 and 1.0 μm^2 in the 1T1C memory cells were prepared to investigate a scalability. Dedicated sense amplifier for destructive read scheme was designed in a circuit. The change in bit line voltage ΔV_{BL} that occurs during read is compared to a reference voltage (V_{REF}) generated from a reference capacitor (C_{REF}) or an externally applied voltage. Finally, the thermal stability of the characteristics of the CMOS transistor suffering from the RTA temperature was confirmed by electrical measurements, and neither threshold voltage shift nor current reduction caused by the RTA was observed.

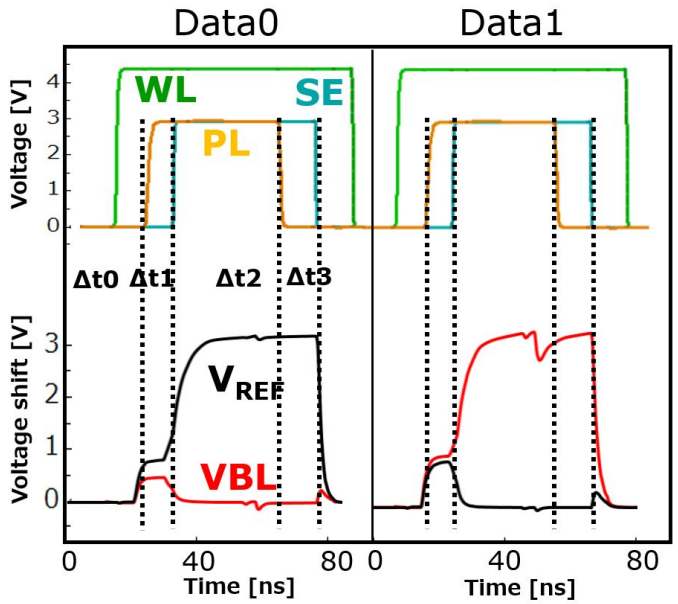
4 Memory array performance of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM

4.1 Introduction

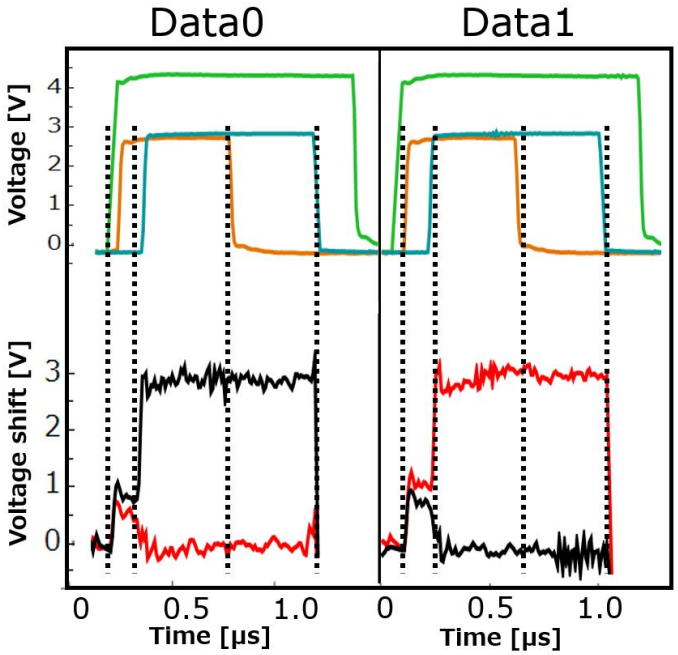
This chapter describes the results of memory array operation of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM. A memory array operation of the 1T1C FeRAM fabricated as described in Chapter 3 is revealed for the first time. The practical size of MFM capacitors (smaller than 1 μm^2) with the dedicated sense amplifier (SA) was expected to allow 1T1C FeRAM memory array to be operated under the practical operating speed in the order of 10 ns. First, the waveforms during read operation by the SA circuit were simulated by extracting resistance and capacitance from designed circuit to verify whether operation speeds in the order of ns are possible. And then, the behavior of bitline voltage shift (ΔV_{BL}) for reading data0 and data1 were experimentally confirmed in Section 4.2. Second, a practical operating performance of 64 kbits 1T1C FeRAM with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film was comprehensively investigated by obtain a shmoo plot by changing operating voltage and operating speed in Section 4.3. Finally, a switching kinetics were discussed by comparing the result of shmoo plot and switching model in Section 4.4.

4.2 Validation of read operation

The waveforms during read operation by the sense amplifier (SA) circuit were simulated by Spectre commercialized by Cadence. Characteristics of CMOS transistor, resistance and capacitance (RC) of designed circuit were extracted using process design kit of 130 nm CMOS technology. A behavior of metal/ferroelectric/metal (MFM) capacitor was prepared based on the polarization vs. voltage characteristics of MFM with 500°C rapid thermal anneal (RTA) in Figure 2.6.In this simulation, transient response of switching current was not take into account and only RC extraction from circuit components was simulated. Figure 4.1 (a) shows a simulation result at the sensing speed of 10 ns for both reading data0 and data1. Ideal read out behaviour as designed was observed. In the case of reading data0, ΔV_{BL} which is smaller than ΔV_{REF} was observed, and the ΔV_{BL} was discharged to ground, while in the case of reading data1, ΔV_{BL} which is larger than V_{REF} was observed, and the ΔV_{BL} was activated to VDD. Figure 4.2 is an enlarged image of the simulated waveform during the sense period during 10ns in Figure 4.1(a). The waveform rounded off at the beginning of 5ns, but ΔV_{BL} could be detected between whole 10 ns. Figure 4.1 (b) shows an experimental waveforms obtained on the 1T1C FeRAM array with a MFM size of 1.0 μm^2 by CX1000D on CM300 (FormFactor Inc.). It should be noted the time scale of the experimental result is limited to 1 MHz due to the test environmental restriction. Comparing with simulation result, ideal waveforms were detected for reading data0 and data1 described in Figure 3.6, indicating that the SA and step sensing approach for the FeRAM successfully separated both memory states as described in Section 3.4. Therefore these result indicates that the 1T1C FeRAM memory array allows to be operated under the practical operating speed in the order of 10 ns.



(a)



(b)

Figure 4.1. Timing diagrams for the read operation scheme of the 1T1C FeRAM cell for data0 and data1: (a) simulation results and (b) experimental waveforms. The time scale of the experimental result was limited to 1 MHz due to the test environmental restriction.

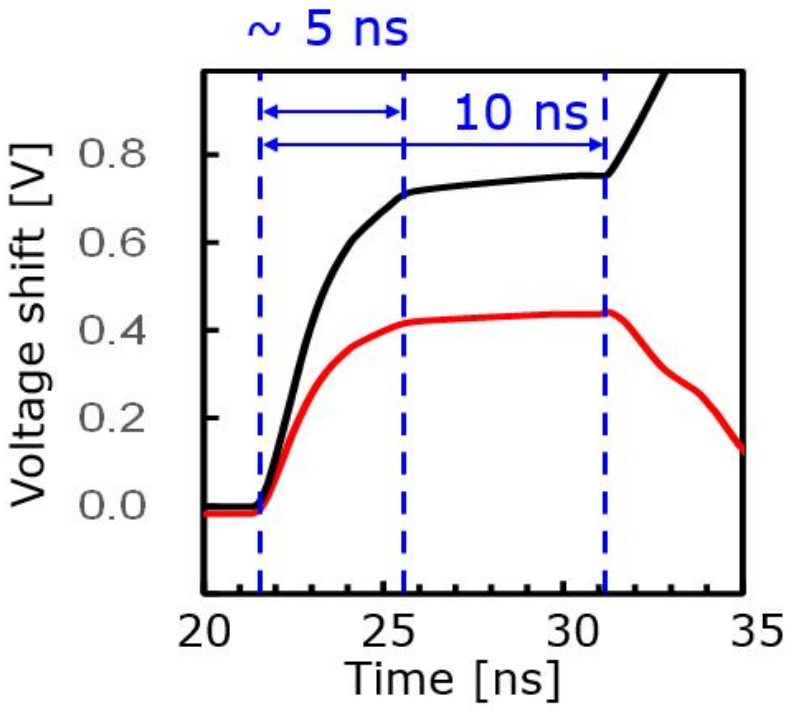
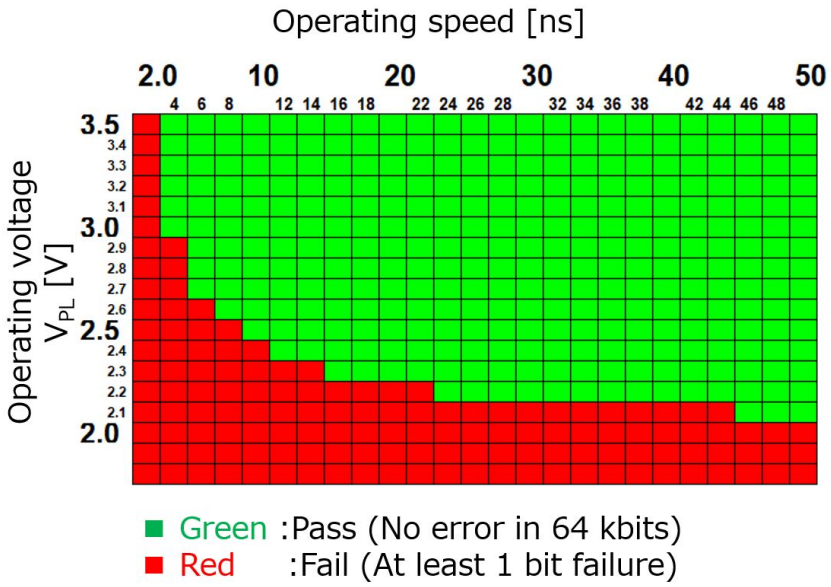


Figure 4.2. Enlarged image of the simulated waveform during the sense period in the Figure 4.1(a).

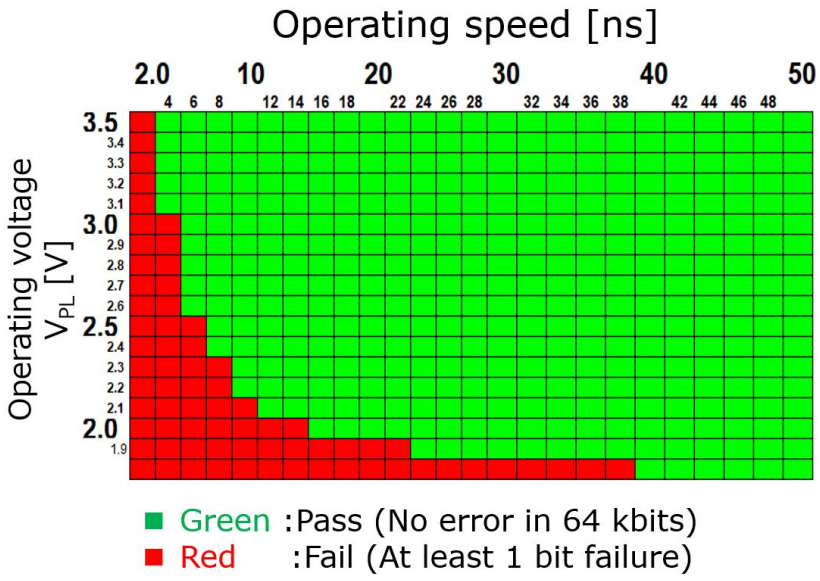
4.3 Shmoo plots

In this section, a practical operating performance of 1T1C FeRAM memory array were investigated for the first time. Furthermore, switching kinetics of ferroelectricity was discussed from a dependence of operating voltage and operating speed.

Operating performance of the 1T1C FeRAM were investigated using shmoo plots for write operation and sense operation described in Section 3.4. Figure 4.3 (a) shows a shmoo plot for the write operation in the CUB-structured test chip with a capacitor size of 0.4 μm^2 for an operating time ranging from 1 to 50 ns and an plate line (PL) operation voltage from 2.0 to 3.5 V. No fail bits were observed for 10 ns write operation at 2.5 V. A lower operating voltage can be allowed by relaxing the operating speed, demonstrating 2.1 V operation at 46 ns speed. Figure 4.3 (b) shows a shmoo plot for the sense operation. It is not certain that the operating performance of write was worse than that of sense, one possible reason is that, remanent polarization could be slightly reduced right after write operation, and need more time to detect by sense operation. Therefore, the worse one should be defined as the true performance of 1T1C FeRAM memory array, resulting in 10 ns operation speed and 2.5 V operation voltage.



(a)



(b)

Figure 4.3. Shmoo plot of time ranging from 1 to 50 ns and operation voltage ranging from 2.0 to 3.5 V obtained on the 64 kbits CUB-structured 1T1C FeRAM memory array with the capacitor size of 0.4 μm^2 for (a) write and (b) sense (green: pass, red: fail).

4.4 Switching kinetic analysis

The trade-off between the operation speed and operating voltage was investigated with reference to the switching model. Switching kinetics model of the $Hf_{0.5}Zr_{0.5}O_2$-based material have been widely discussed[13]. The polarization reversal is widely discussed based on the following three mechanisms as described in Figure 4.4:

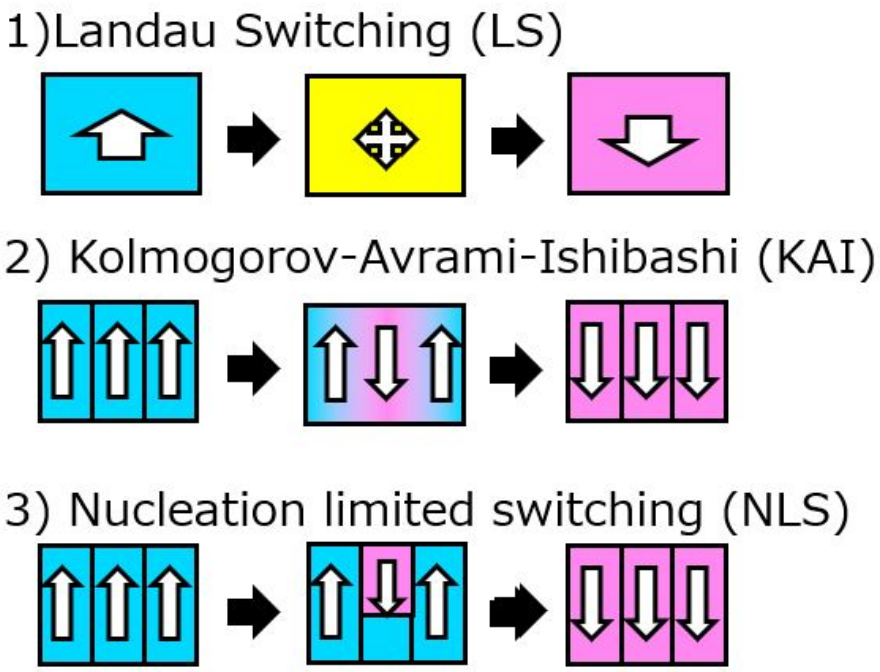


Figure 4.4. Switching models.

(1) Landau Switching (LS) model
(2) Domain Growth (KAI) model
(3) Nucleation Limited Switching (NLS) model

LS model is a thermodynamic model[48]. A coercive field (Ec) of the ferroelectrc material is discussed from the Landau expansion of the free energy. Although it illustrates the general theory that materials with smaller dielectric constants have larger Ec, it didn't explain the film thickness dependence on Ec. The KAI model explains that the domain wall coalescence process due to domain sidewall growth

defines the switching speed[49,50]. In this case, switching speed is limited by growth time. It is comparable with thick perovskite-based materials films but not for thin $Hf_{0.5}Zr_{0.5}O_2$-based materials. NLS model is commonly used for thin $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric materials,[30,51,52]. In this case, domain nucleation is taken to be account as the rate-limiting process for polarization reversal and introduces a latency period before nucleation. The Du-Chen model[53] has introduced the delay time t and the required voltage to switching using following equation:

$$\tau = \tau_0 \cdot \exp(\frac{\alpha}{k_B T} \cdot \frac{1}{V^2}) \tag{4.1}$$

where τ is the constant parameter corresponding to the delay time for the domain nucleation, and α corresponds to the thermodynamic contribution associated with the domain wall energy in the layer. kb is the Boltzmann constant. T is the temperature. Although there were initial concerns that the switching speed would be slow due to domain pinning caused by oxygen vacancy defects in $Hf_{0.5}Zr_{0.5}O_2$, switching speeds of 10 to 100 ns have been demonstrated using ferroelectric field effect transistors (FeFET)[54]. In the case of 1T1C FeRAM, it is difficult for a single large capacitor to confirm sub-ns switching speed directly due to larger RC delay resulting from large capacitance area than FeFET.

Figure 4.5 shows the switching analysis as a function of operating voltage and speed for CUB-structured FeRAM extracted from the Shmoo plot in the Figure 4.3 (a) using the Equation 4.4.Good compatibility with the NLS model was confirmed up to operating speeds of 10 ns or less.On the other hand, the operating speed is limited at speeds exceeding 10 ns. A possible reason for this limitation is not material related switching but RC delay from circuit components described in Figure 4.2. This RC delay is assumed to be about 5 ns based on the simulation results, which is in good agreement with the hypothesis.

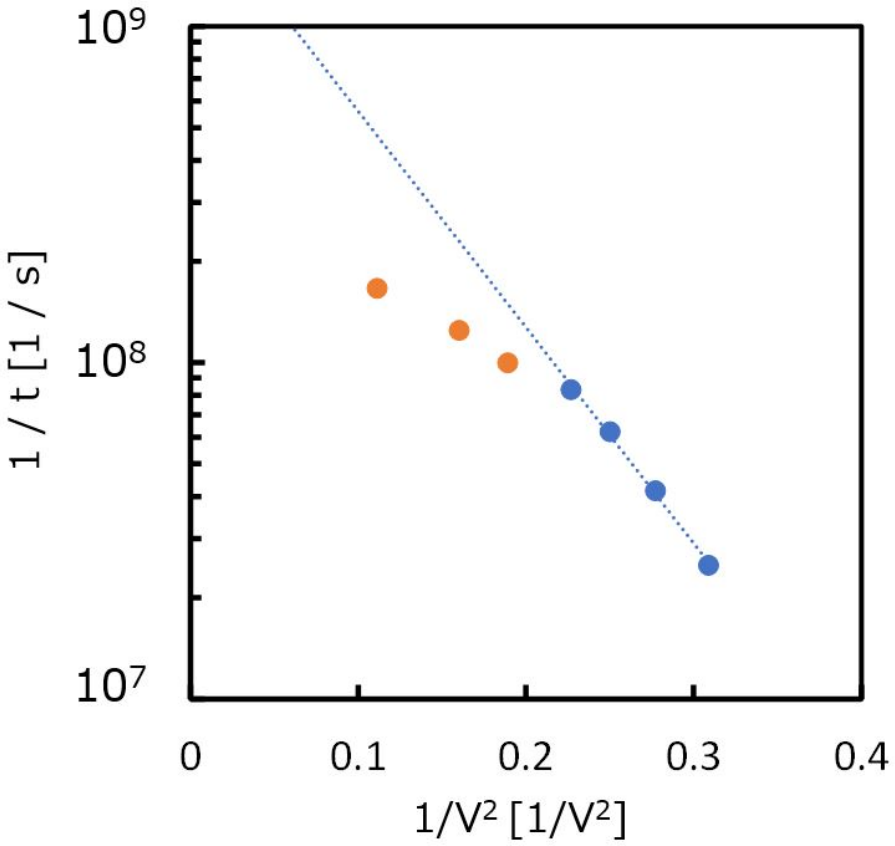


Figure 4.5. Reciprocal switching time versus $1/V^2$ for the CUB-structured FeRAM. Switching time and voltage are extracted from the shmoo plot. The line in the Figure is a least-squares fitting using data over 10 ns.

4.5 Summary

The performance of 64 kbits 1T1C FeRAM memory array with ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film with CUB structure implemented in 130 nm CMOS technology was experimentally demonstrated for the first time. The practical size of MFM capacitors (smaller than 1 μm^2) with the dedicated SA was demonstrated to allow 1T1C FeRAM memory array to be operated under the practical operating speed in the order of 10 ns. First, we extracted the RC from the designed circuit and simulated the waveform during readout by the SA circuit, and confirmed that it can be driven at an operating speed of 10 ns but with a rounded waveform

of 5 ns at the beginning. And then, the behavior of ΔV_{BL} during reading data0 and data1 were experimentally confirmed. Finally, Operation performance for a write and sense voltages of 2.5 V and operating speed of sub-10 ns were obtained by investigating a shmoo plots. Furthermore, switching kinetics of ferroelectricity was discussed from a dependence of operating voltage and operating speed, and the trad-off was in good agreement with NLS model considering the RC delay around 5 ns. A possible reason for this limitation is not material related switching but RC delay from circuit components described in Figure 4.2. This RC delay is assumed to be about 5 ns based on the simulation results, which is in good agreement with the hypothesis. From these results, it can be said that 1T1C FeRAM memory arrays with $Hf_{0.5}Zr_{0.5}O_2$ was proved to operate at 2.5 V with an operation speed of less than 10 ns.

5 Memory window analysis of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM

5.1 Introduction

This chapter describes the results of memory window analys with $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array to reveal the uniformity of $Hf_{0.5}Zr_{0.5}O_2$ film by obtaining distribution of bitline voltage shift (ΔV_{BL}) in 64 kbits 1T1C FeRAM under a practical measurement condition in Chapter 4 for the first time.

First, distribution of ΔV_{BL} on the 64 kbits 1T1C FeRAM memory array for both data0 and data1 were investigated with different MFM capacitor sizes to verify the uniformity of ferroelectricity for small MFM capacitor (smaller than 1 μm^2) in Section 5.2. Second, memory window at median value in the 64 kbits 1T1C FeRAM memory array was discussed by the size dependence of metal/ferroelectric/metal (MFM) capacitors in Section 5.3. Finally, in Section 5.4, feasibility study of memory window considering distribution of MFM capacitance was discussed. Variability of capacitance of MFM for both data0 and data1 was extracted from the variability of ΔV_{BL} by combining the experimental result with Monte Carlo simulation to estimate a memory window of 1M bits for advanced CMOS technology node such as 40 nm.

5.2 Distribution of bitline voltage difference

For the practical application of 1T1C FeRAM, it is important to evaluate the variation of bitline voltage (ΔV_{BL}) of each memory cell. Major root cause of the variability in MFM capacitors are;

(1) Number of switchable domains (edge dead domain)
(2) Size of capacitors (area, thickness)
(3) Randomly induced defects
(4) Variation of parasitic capacitance of bitlines (BL)

It is said that domains located in the edge region of ferroelectric layer cause degradation due to process damage of nucleation or inhibition of nucleation and growth of polar-ortholombic phase during rapid thermal annealing[55,56], resulting in reduction of switchable domains. In the scaled device, the impact is expected to be significant and increase the variability of remanent polarization, since the edge region occupies a larger percentage of the total area. With reference to the area of capacitors, variability of MFM area and its thickness caused by process variability directly affects on the capacitance[57]. If there is a fatal or systematic defect in the ferroelectric layer, the variation will not follow a normal distribution. HZO is poly-crystalline, and its grain size is known to be distributed in the range of 5 to 40 nm, with the distribution converging to about 15 nm after wake-up[58]. In FeFETs, it is known that when the device size is scaled down to the 28 nm technology node, the number of grains in the device drops below 10, resulting in a quantization of Vth[59]. On the other hand, in 1T1C-type FeRAM, the area of the element can be obtained by 3D structure even as miniaturization progresses. For example, assuming that the MFM area can be within 0.1 μm^2 regardless of the technology nodes, about 400-500 grains can exist in a capacitor, resulting in no quantization could occur.

As described in Equation 5.4, in 1T1C FeRAM memory array operation, not only material-induced variations but also circuit-induced variations must be considered.

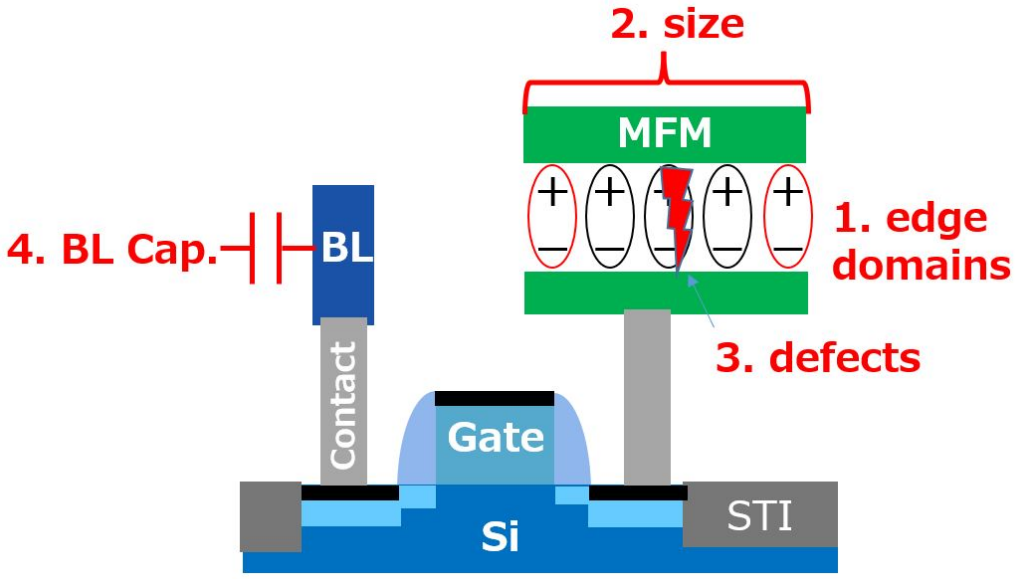


Figure 5.1. Root causes of variation in ferroelectric materials.

The distribution of ΔV_{BL} for each MFM capacitor area in the 1T1C FeRAM was further investigated. ΔV_{BL} was extracted by sweeping an externally applied V_{REF} (see Figure 3.5). Normal probability plots of ΔV_{BL} for data0 and data1 were obtained at an operating voltage of 2.5 V with an operation time of 100 ns, as shown for each MFM capacitor area in Figure 5.2. During the measurement, a fixed delay time was applied to the devices, ignoring the influence of a fluid imprint[60]. A perfect bit functionality in the 64 kbits was confirmed in every capacitor area. The memory window at median value was extracted to be above 0.41 V for a capacitor with an area as small as 0.4 μm^2.

It is important to verify that the value of ΔV_{BL}, which is extracted from a single capacitor measurement. Figure 5.3 shows the results of ΔV_{BL} comparison between a single capacitor and 1T1C FeRAM for data1 and data0. The ΔV_{BL} of the single capacitor was calculated using the capacitance using C_{BL} with 250 fF and capacitance extracted from Figure 2.6 at 500°C. Howeever, similar ΔV_{BL} for data0 was obtained, while smaller ΔV_{BL} for data1. Furthermore, the difference is decreased with smaller capacitance area. This suggests that 1T1C FeRAM does not fully reproduce the ferroelectric properties obtained in a single capacitor. The cause of this

difference is that the amount of oxygen vacancy in the film due to the quality of interfacial layer of the bottom electrode[61,62], the presence of a passivisation film[56], the thermal history of the BEOL process[7], and mechanical stress caused by MFM device structure[55] and orientation of domain[26], etc, require further analysis in the future.

Figure 5.4 shows a variability of ΔV_{BL} extracted from slopes of Figure 5.2 for data0 and data1 on each MFM capacitor area. Larger variability number of ΔV_{BL} around 15 mV/sigma for data1 ($\sigma V_{\text{BL of data1}}$) than that of data0 ($\sigma V_{\text{BL of data0}}$) around 10 mV/sigma was obtained. It is assumed that the variation in data0 is due to the dielectric component (DE) and the variation in data1 is due to both the dielectric and ferroelectric components (DE + FE). Assuming that the variability of DE and FE are independent components each other, the variability of FE ($\sigma V_{\text{BL of FE}}$) was extracted using the following equation. Figure 5.5 shows that the variation due to the FE is almost equivalent to the variation due to DE. This result indicates that there are large amount of grains in the HZO film and variability of switching of domains is not dominant factor.

$$\sigma V^2_{\text{BLof data1}} = \sigma V^2_{\text{BL of FE}} + \sigma V^2_{\text{BL of data0}} \tag{5.1}$$

Furthermore, the variability increased with smaller capacitance area due to the variation described in Figure 5.1. The impact of this dependency on future miniaturization will be investigated in the next section.

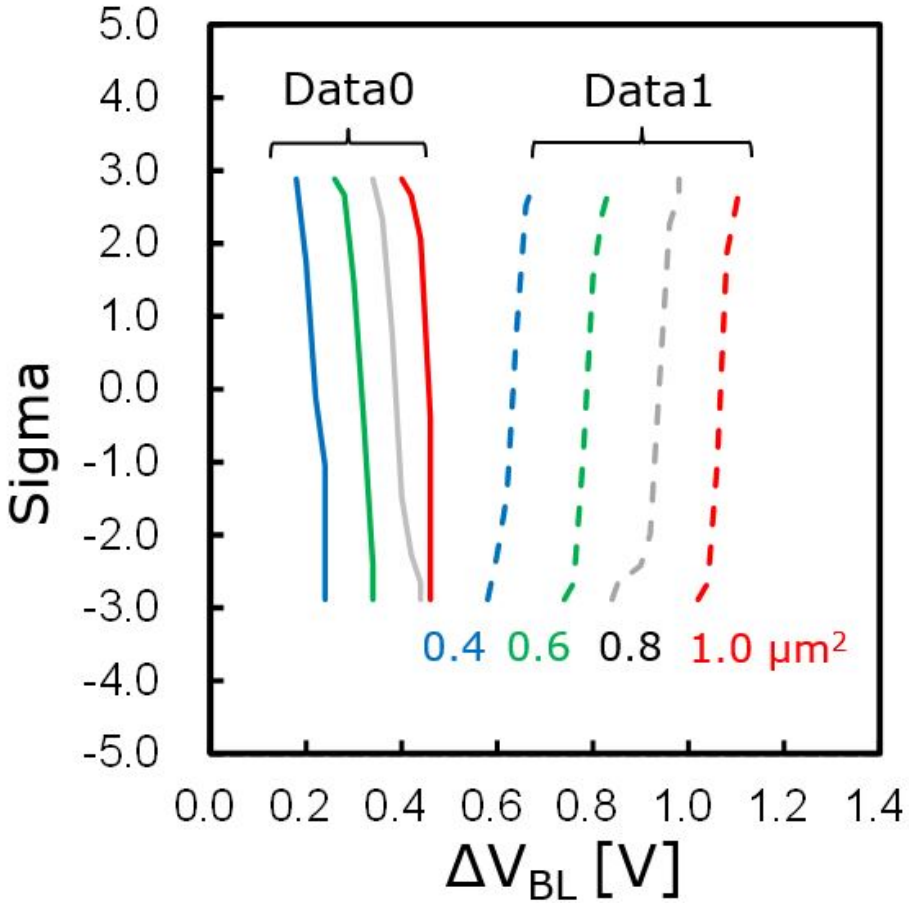
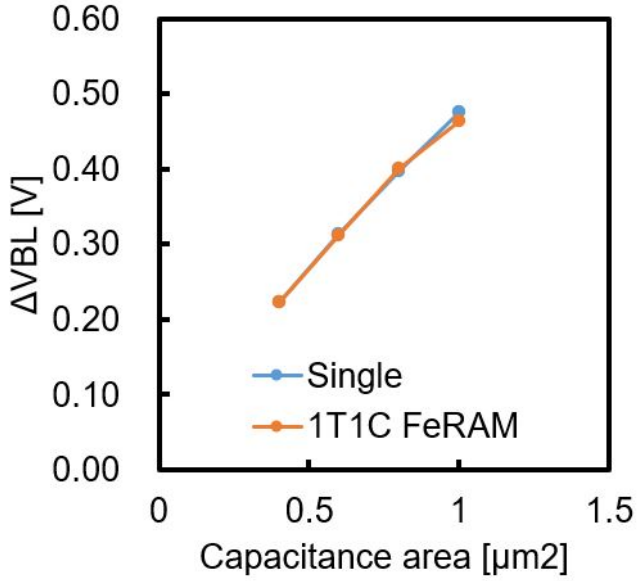
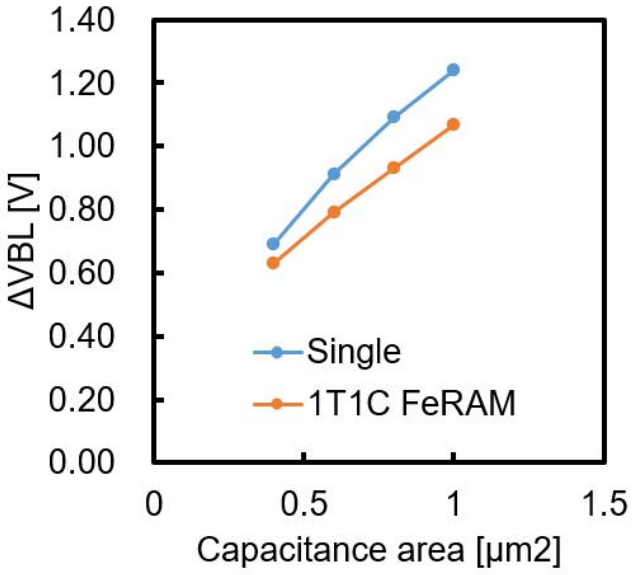


Figure 5.2. Normal distribution plot of ΔV_{BL} for the CUB-structured 64 kbits 1T1C FeRAM operated at 2.5 V, 100 ns for capacitors having 0.4, 0.6, 0.8 and 1.0 μm^2 capacitor area.



(a)



(b)

Figure 5.3. Comparison of ΔV_{BL} between single large capacitor and 1T1C FeRAM at 0.4, 0.6, 0.8 and 1.0 μm^2 capacitor area for (a) data0 and (b) data1. The ΔV_{BL} of the single capacitor was calculated using the capacitance using C_{BL} with 250 fF and capacitance extracted from Figure 2.6 at 500°C.

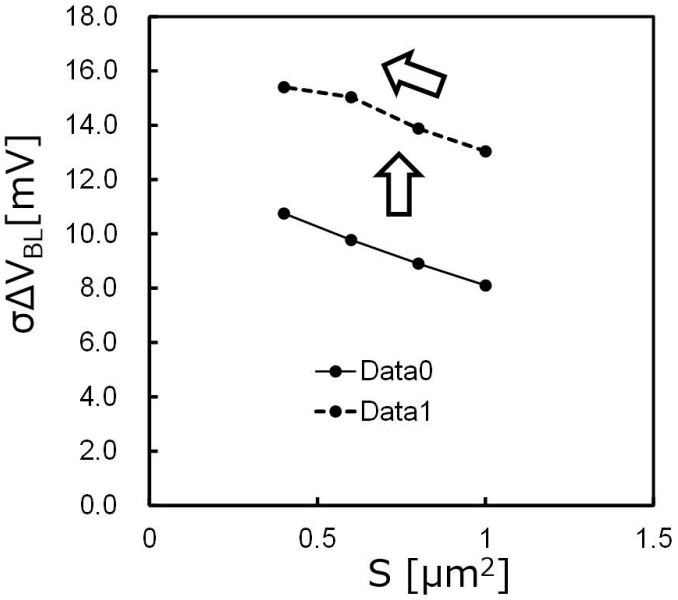


Figure 5.4. Variability of ΔV_{BL} for the CUB-structured 64 kbits 1T1C FeRAM operated at 2.5 V, 100 ns for capacitors having 0.4, 0.6, 0.8 and 1.0 μm^2 capacitor area.

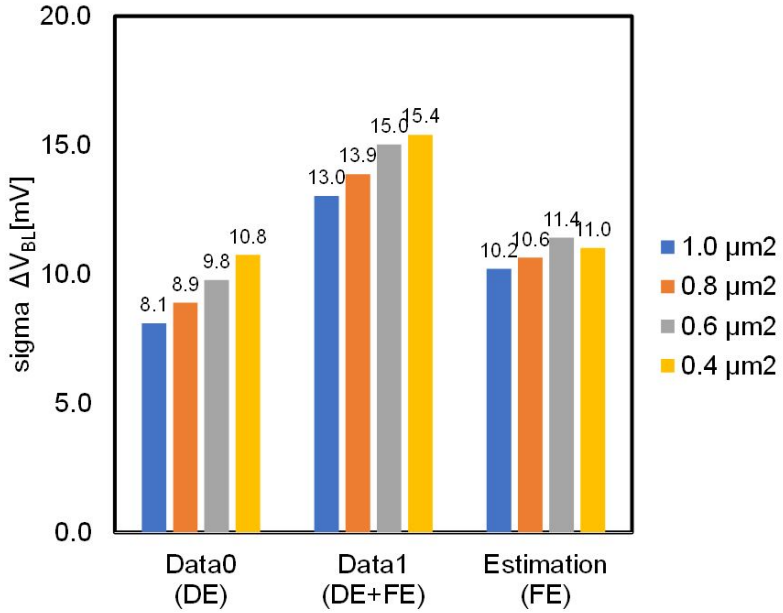


Figure 5.5. Variability of ΔV_{BL} comparison between DE and FE components having 0.4, 0.6, 0.8 and 1.0 μm^2 capacitor area.

5.3 MFM memory window capacitance area dependency

Scalability of memory window of $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array was investigated. Required MFM capacitance area at 40 nm technology node was estimated by referring to the Front End Process (FEP) of the 2013 International Technology Roadmap for Semiconductors (ITRS) roadmap[3]. In 2013, FeRAM was already being manufactured using older materials (perevskite-based), but ITRS surveyed FeRAM manufacturers to determine their requirements for future FeRAM performance. The roadmap is shown in Table 5.1. According to the Table 5.1, it is expected that;

(1) Since 2013, processing dimensions will be scaled by 0.8 every 4 years.
(2) Parasitic capacitance of BL will be scaled by $F^{2/3}$ starting from 320 fF in the 180 nm generation[63].
(3) ΔV_{BL} must be 140 mV (ITRS assumes no change (improvement))

Conventional materials (perevskite-based) will face manufacturing technology challenges (yellow) and limitations (red - Redbrick Wall) in the roadmap because of scaling limitations due to ferroelectric size effects and difficulties in creating 3D capacitors (cylinder and pillar structures) due to limitations in deposition methods.

Table 5.2 shows the characteristics and capacitance area of MFM required for the 40nm technology node, assumed from the Table 5.1.Two cases of remanent polarization (2Pr) were calculated as 30 $\mu C/cm^2$ as case1 and 40 $\mu C/cm^2$ as case2 according to a realistic 2Pr of $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric material. Parasitic capacitance of BL (C_{BL}) was estimated to be 120 fF/BL based on the[63]. As a result, the required MFM capacitance area were 0.055 and 0.041 in the case1 and case2 accordingly.

Table 5.1. FeRAM technology roadmap from ITRS road map 2013[3].

Table FEPS FeRAM Technology Requirements

Year of Production	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*
FeRAM technology node	130	130	130	90	90	90	90	90	65	65	65
MET1 1/2 Pitch - F(nm)[A]	175	175	175	135	135	135	135	135	105	105	105
FeRAM cell size – area factor a in multiples of F2 [B]	23.2	23.2	23.2	21.9	21.9	21.9	21.9	21.9	20.0	20.0	20.0
FeRAM cell size (μm^2) [C]	0.710	0.710	0.710	0.400	0.400	0.400	0.400	0.400	0.220	0.220	0.220
FeRAM cell structure [D]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [E]	stack	stack	stack	stack	stack	stack	stack	stack	stack	stack	stack
FeRAM capacitor footprint (μm^2) [F]	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234	0.125	0.125	0.125
FeRAM capacitor active area (μm^2) [G]	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234	0.125	0.125	0.125
FeRAM cap active area/footprint ratio	1	1	1	1	1	1	1	1	1	1	1
Ferro capacitor voltage (V) [I]	1.5	1.5	1.5	1.2	1.2	1.2	1.2	1.2	1.0	1.0	1.0
FeRAM minimum switching charge density ($\mu C/cm^2$) [J]	8.5	8.5	8.5	12.0	12.0	12.0	12.0	12.0	18.1	18.1	18.1
FeRAM endurance (read/write cycles) [K]	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	1.00E+15	>1.0E16	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years) [L]	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years

Year of Production	*2024*	*2025*	*2026*	*2027*	*2028*
FeRAM technology node	65	45	45	45	45
MET1 1/2 Pitch - F(nm)[A]	105	80	80	80	80
FeRAM cell size – area factor a in multiples of F2 [B]	20.0	18.8	18.8	18.8	18.8
FeRAM cell size (μm^2) [C]	0.220	0.120	0.120	0.120	0.120
FeRAM cell structure [D]	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [E]	stack	stack	stack	stack	stack
FeRAM capacitor footprint (μm^2) [F]	0.125	0.067	0.067	0.067	0.067
FeRAM capacitor active area (μm^2) [G]	0.125	0.067	0.067	0.067	0.067
FeRAM cap active area/footprint ratio	1	1	1	1	1
Ferro capacitor voltage (V) [I]	1.0	1.0	1.0	1.0	1.0
FeRAM minimum switching charge density ($\mu C/cm^2$) [J]	18.1	26.5	26.5	26.5	26.5
FeRAM endurance (read/write cycles) [K]	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years) [L]	10 Years	10 Years	10 Years	10 Years	10 Years

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 5.2. Estimated MFM specification for 40 nm technology node.

Parameter	Unit	Perevskite-based FeRAM ITRS2013	$Hf_{0.5}Zr_{0.5}O_2$ -based FeRAM Case 1	$Hf_{0.5}Zr_{0.5}O_2$ -based FeRAM Case 2
Node	µm	0.13	0.04	0.04
Memory cell area	μm^2	0.71	0.12	0.12
Capacitance of BL	fF	0.26	0.12	0.12
Sensing voltage	V	0.14	0.14	0.14
Q	pC	0.036	0.016	0.016
2Pr	$\mu C/cm^2$	8.7	30	40
Capacitance area	μm^2	0.42	0.055	0.041

Figure 5.6 shows a comparison of the capacitance area dependence on the memory window for simulation and experimental result.The capacitor area dependence on the memory window of experimental result were obtained by the difference in the median value of ΔV_{BL} for both data0 and data1 on the CUB-structured 1T1C FeRAM memory array. Black line was calculated by Equation 5.4 considering the capacitance area. The memory window obtained from the experimental results agreed with the simulation results, demonstrating that a significant memory window above 100 mV is expected at a capacitor size of 0.10 μm^2. Figure 5.7 shows a simulation result ranging from 0 to 0.1 μm^2 capacitance area, assuming 40 nm technology node. More than 140 mV will be obtained over 0.065 μm^2 capacitor area, which is good agreement with the estimation in Table 5.2. However, distribution of the ΔV_{BL} must be considered for practical memory array operation, and will be discussed in Section 5.4.

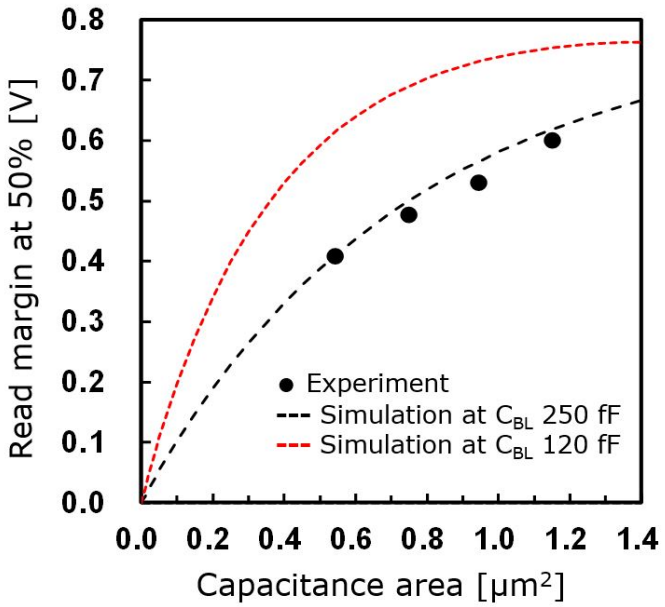


Figure 5.6. Read margin of the test chip for 2.5 V, 100 ns operation as a function of the capacitor area. The values of C_{BL} were determined as 250 fF for the 130 nm technology.

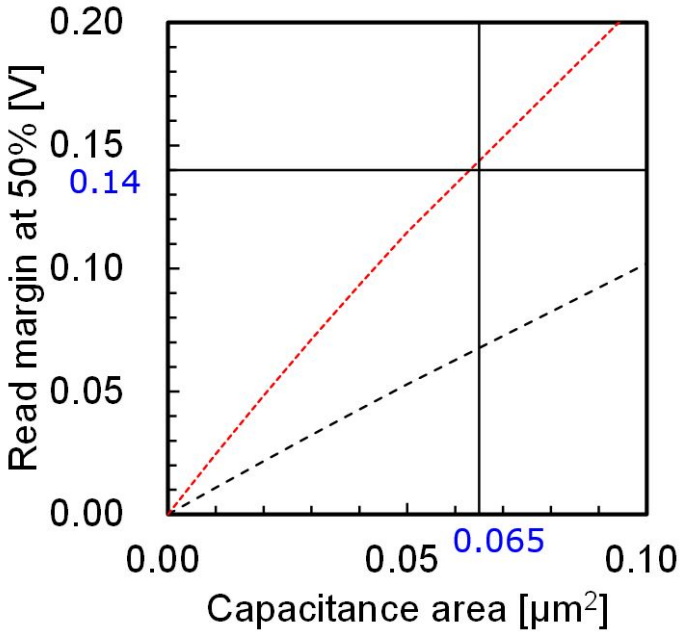


Figure 5.7. Read margin of the test chip for 2.5 V, 100 ns operation as a function of the capacitor area. The values of C_{BL} were determined as 250 fF for the 130 nm technology and 120 fF for 40 nm technology.

5.4 Memory window prediction for future technology node

Feasibility study of memory window considering distribution of MFM capacitance for 40 nm technology node was investigated by using variability result in Section 5.2. As discussed in Chapter 3, ferroelectric capacitor is modeled using the following equation:

$$\Delta V_{\mathrm{BL}} = V_{\mathrm{PL}} \frac{C_{\mathrm{FE}}}{(C_{\mathrm{FE}} + C_{\mathrm{BL}})} \tag{5.2}$$

Since the smaller the area of the MFM, the larger variability of C_{FE} (σC_{FE}) is expected, it is required to estimate the σC_{FE} in 40 nm CMOS technology node. Furthermore, scaling of C_{BL} is needed to be considered as well. Since the 1T1C FeRAM results only provide the variation of ΔV_{FE} ($\sigma \Delta V_{\mathrm{BL}}$), it is necessary to consider area dependence separately for σC_{FE} and σC_{BL} when estimating memory windows at 40 nm technology.

The method is schematically illustrated in Figure 5.8. First, $\sigma \Delta V_{\mathrm{BL}}$ with different variability of σC_{FE} was simulated by Monte Carlo Simulation. Then σC_{FE} of each MFM area were extracted comparing the simulation data and experimental data from Figure 5.4. Second, size effect of the variability was calculated using extracted σC_{FE} to predict a σC_{FE} in for 40 nm technology node. Target MFM area was defined as 0.1 $\mu\mathrm{m}^2$ considering the ITRS road map in Section 5.2. Finally, a $\sigma \Delta V_{\mathrm{BL}}$ at 40 nm CMOS technology node was simulated again by Monte Carlo Simulation using extracted σC_{FE}.

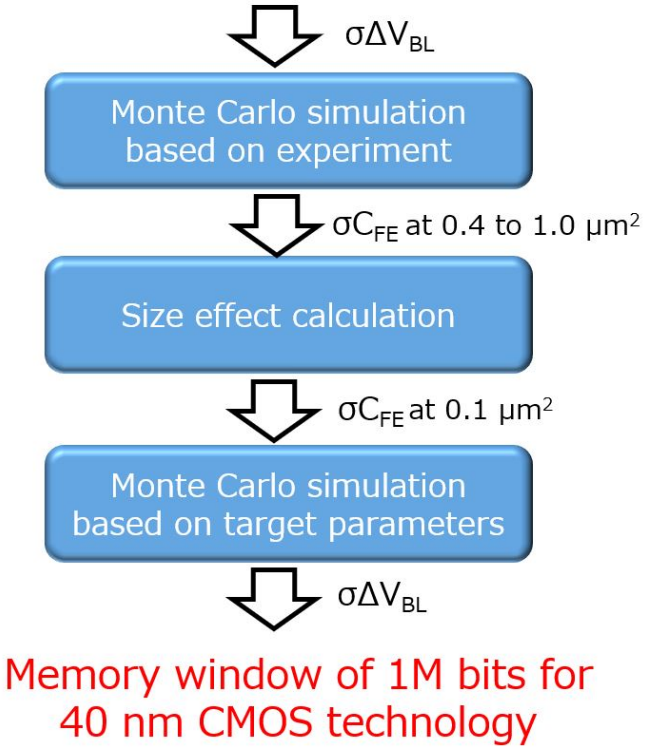


Figure 5.8. Schematic illustration of method for predicting memory window combining Monte Carlo simulation.

Figure 5.9 shows a Monte Carlo Simulation result for $\sigma\Delta V_{\mathrm{BL}}$ with different variability of σC_{FE} for MFM area of 1.0, 0.8, 0.6 and 0.4 μm^2. Table 5.3 shows the input parameters for the simulation and 1000 times trial were conducted by using VBA script. In this simulation, fixed $\sigma\Delta V_{\mathrm{BL}}$ at 2%sigma was used referring to well known experimental data (not shown in this thesis). The smaller variability was obtained with smaller σC_{FE} for every capacitance area. Furthermore, a MFM area dependence on the $\sigma\Delta V_{\mathrm{BL}}$ became smaller with smaller σC_{FE}, indicating that σC_{BL} becomes dominant comparing with σC_{FE}. Then, σC_{FE} of each MFM area were extracted comparing the simulation data and experimental data from Figure 5.4.

Table 5.3. Input parameters for Monte Carlo simulation.

Parameter	Median value[fF]	Variability [%sigma]
C_{BL}	250	2
C_{FL} for data1	120, 96, 72, 48	0, 1, 2, 4, 8
C_{FL} for data0	40, 32, 23, 16	0, 1, 2, 4, 8

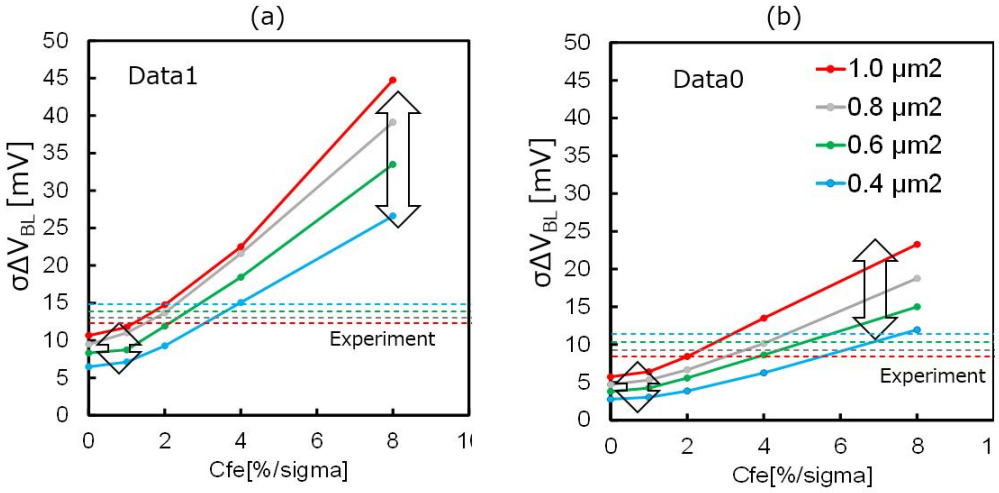


Figure 5.9. Monte Carlo simulation result for $\sigma\Delta V_{\mathrm{BL}}$ with different variability of σC_{FE} for MFM area of 1.0, 0.8, 0.6 and 0.4 μm^2 for data1 (left) and data0 (right).

Figure 5.10 shows size effect of the variability was calculated using extracted σC_{FE} to predict σC_{FE} at 0.1 μm^2. There are no model for size effect of the variability for the ferroelectric capacitance and two different trends were plotted as linear plot and Pelgrom plots[57]. In both case, σC_{FE} increases with smaller memory area and worse variation was predicted at Pelgrom than Linear fitting. Table 5.4 shows output parameters when extrapolating to 0.1 μm^2 using Figure 5.10.

In the case of dealing with Vth variation of Tr, it is known that the Pelgrom plot passes through the origin. On the other hand, there are cases where it does not pass through the origin when applied to a paraelectric capacitor, and it has been reported that the model is followed by considering the dependence of the fringe capacitance of the capacitor[64,65]. In this study, the Pelgrom plot does not pass through the origin in the right Figure of Figure 5.10 (b). This suggests that the variation component of the fringe capacitance component may have to be taken into account, which is an issue for future work.

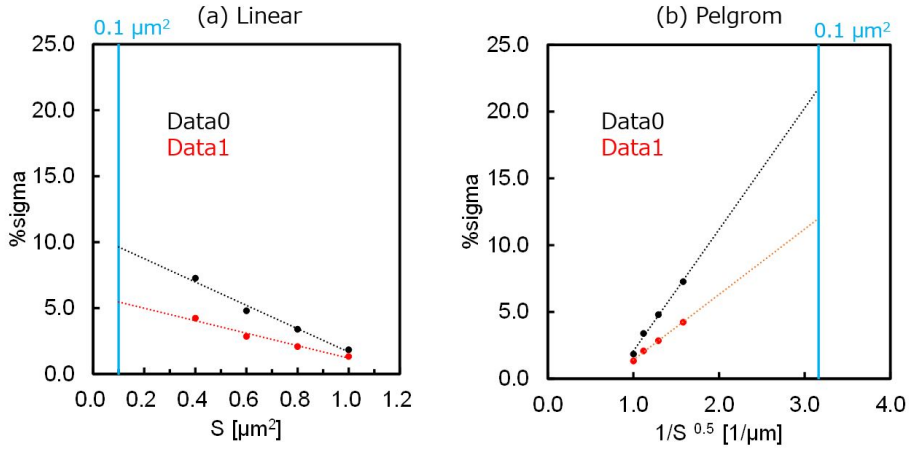


Figure 5.10. σC_{FE} as a function of MFM area for (a) Linear fitting plot and (b) Pelgrom plot.

Table 5.4. Output parameters for MFM area of 0.1 μm^2.

Parameter	Linear plot[%sigma]	Pelgrom plot [%sigma]
C_{FL} for data1	5.8	12
C_{FL} for data0	13	21

Distributions of $\sigma\Delta V_{BL}$ for both data1 and data0 were simulated by Monte Carlo Simulation using parameters in Table 5.5 to predict a memory window of 1 Mbits distribution at MFM area of 1.0 μm^2. Figure 5.11 shows distributions of ΔV_{BL} for both data1 and data0 with two types of area dependence, Linear plot and Pelgrom plot. In the case of Linear plot, a memory window of l00 mV was achieved at -5 σ (around 1 Mbits), while no window for Pelgrom plot. As aresult, a 10% increase in remanent polarization is required for Linear plot case and 40% for Pelgrom plot case. Since sense amplifier circuits capable of detecting potential fluctuations of a few mV have been put to practical use, the value would be acceptable for planer type MFM capacitors in 40 nm technology nodes.

Table 5.5. Input parameters for Monte Carlo Simulation for 40 nm CMOS technology.

Parameter	Median value[fF]	Linear[%sigma]	Pelgrom [%sigma]
C_{BL}	120	2	2
C_{FL} for data1	14	5.8	12
C_{FL} for data0	4	13	21

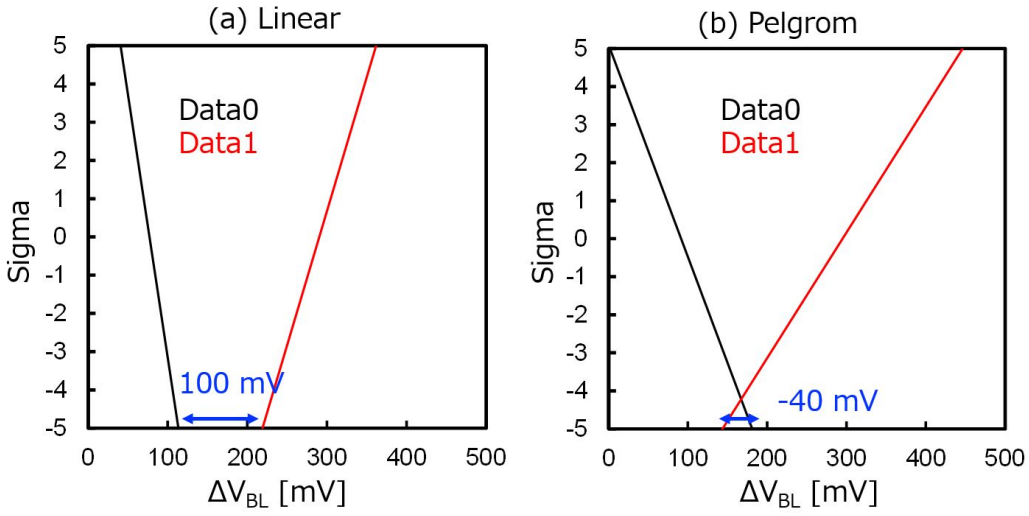


Figure 5.11. Memory window of 1 Mbits distribution at MFM area of 1.0 μm^2 for (a) Linear fitting plot and (b) Pelgrom plot.

5.5 Summary

The practical memory window analysis of the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-based 64 kbits 1T1C FeRAM memory array with CUB structure implemented in 130 nm CMOS technology was experimentally demonstrated for the first time. A perfect yield and a large memory window above 400 mV were obtained for a capacitor area of 0.4 μm^2, revealing good uniformity or the film. Comparing the ΔV_{BL} with what predicted from single capacitor results in Chapter 2, similar ΔV_{BL} for data0 was obtained while smaller ΔV_{BL} for data1. the difference is decreased with smaller capacitance area.This suggests that 1T1C FeRAM does not fully reproduce the ferroelectric properties obtained in a single capacitor described in Chapter 2. The cause of this difference is that the amount of oxygen vacancy in the film due to the quality of interfacial layer of the bottom electrode, the presence of a passivisation film, the thermal history of the BEOL process, and mechanical stress caused by MFM device structure and orientation of domain, etc, require further analysis in the future. The variability of ΔV_{BL} due to ferroelectric and dielectric components were calculated, resulting in the variation due to the ferroelectric is almost equivalent to that of dielectric. This result indicates that there are large amount of grains in the HZO film and variability of switching of domains is not dominant factor.

Memory window at median value in the 64 kbits 1T1C FeRAM memory array was discussed by the size dependence of MFM, and more than 140 mV will be obtained over 0.10 μm^2 capacitor area, which is good agreement with the estimation.Finally, to investigate the feasibility of a memory window that accounts for the capacitance distribution of the MFM, Monte Carlo simulation was applied for the experimental results to estimate a 1 Mbit memory window in the 40 nm CMOS technology node. As a result, memory window can be achieved by MFM area between 0.11 to 0.14 μm^2 to achieve the memory window.

Table 5.6 shows a comparison table with a target properties toward 1T1C FeRAM under 40 nm CMOS technology node. In summary, the target for write speed was achieved, but that for write voltage was not reached, and further study is required to achieve the target value.Furthermore, the endurance and retention results are

predicted from the single-capacitor results, and further research is needed to clarify them.

Table 5.6. Comparison table with target.

	SRAM	eDRAM	$Hf_{0.5}Zr_{0.5}O_2$-based FeRAM Target	$Hf_{0.5}Zr_{0.5}O_2$-based FeRAM This work
Write voltage	$\sim$ 0.5 V	$\sim$ 1.0 V	2.0 V	2.5 V
Write speed	$<$ 1 ns	20 $\sim$ 100 ns	$\sim$ 10 ns	$\sim$ 20 ns
Endurance	10^{16}	10^{16}	$\sim 10^{15}$	$\sim 10^{11}$ [(b)]
Retention	No	No	85°C, 10 min	85°C, 100 min[(a)]
Scalability	5/7nm	28 nm	40 nm	40 nm[(b)]

(a) Result using a single capacitor
(b) prediction

6 Reliability study on $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM

6.1 Introduction

This chapter discusses a reliability of the $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array, which has never been addressed before. In $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM, the polarization vs. electric field characteristics change gradually with cycling stress as described in Figure 6.1 (a) and Figure 6.1 (b). There are following major stages during the cycling.

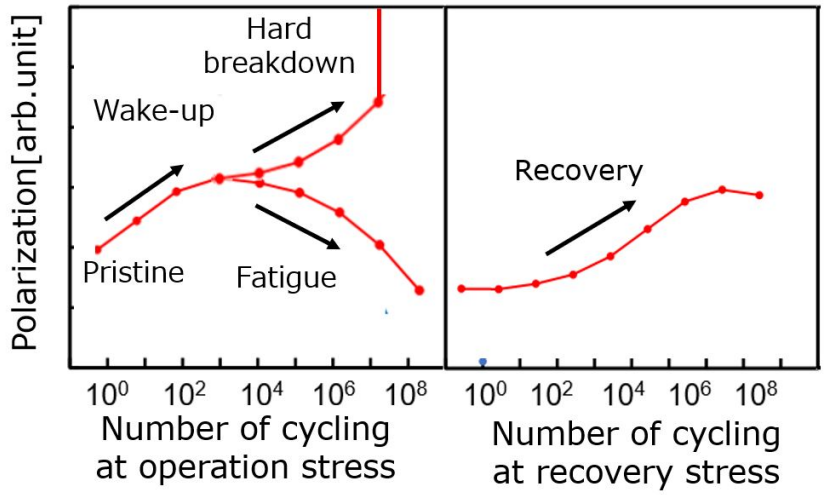
- Pristine : In this stage, a remanent polarization is smaller than wake-up state (see below). Uneven charge distribution at bottom and top electrodes or the presence of an interface dead layer due to oxidation of the electrode surface can cause non-polar dipoles, resulting in lower 2Pr. In addition, charges in the layer could cause domain pinning and inhibit its switching, reducing the switchable polarization as well[61,66].
- Wake-up : In this stage, 2Pr is increased with applying external electric field. In generally, by applying bipolar external electric field, the internal bias electric field can be decreased due to charge of oxygen vacancy redistribution, resulting phase transition from tetragonal phase to ortholombic phase. Furthermore, reorientation from in-plane to out-of-plane domains also contributes to increased involvement in the switching domain[67].
- Fatigue :During the fatigue phase, new charging defects are generated that pin the switching domain, often reducing the observed polarization again.

The charged defects are trapped at the interfacial layer between ferroelectric layer and electrode, and the increase in the trap density near the electrodes results in the domain pinning of dipoles[68]. This fatigue occurs with hard breakdown (HBD) of the film at the same time.

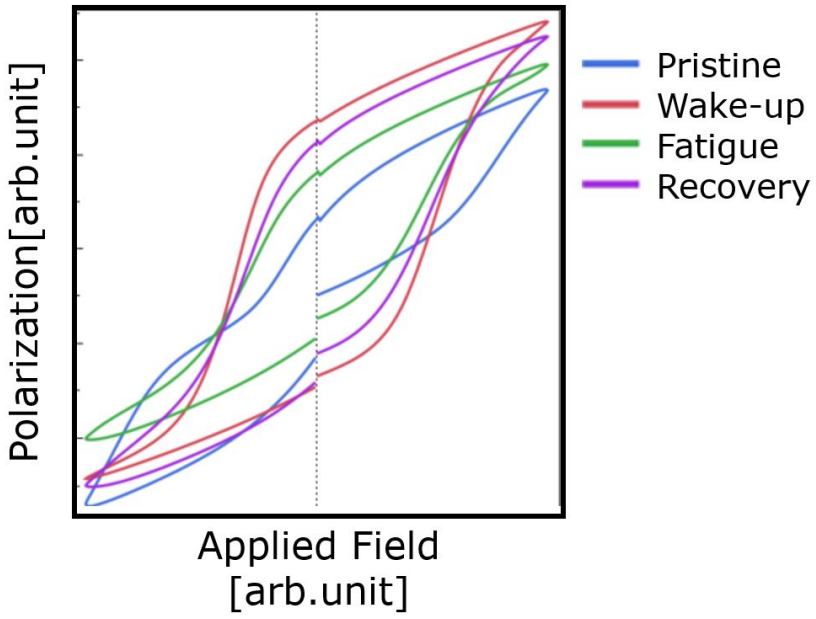
- Hard breakdown : As mentioned in fatigue phenomena, if charge defects are accumulated in the film, it creates leakage paths are created resulting in a short between top electrodes and bottom electrodes. Whether hard breakdown or fatigue occurs first is determined by the intensity of the applied stress voltage, and in the case of high voltage stress, hard breakdown occurs before fatigue[69].
- Recovery : When a higher cycling stress was applied to the fatigued capacitor, the pinned domain started to flip via neutralization of the positively charged oxygen vacancy accompanied by electron de-trapping at the interfacial layer[69].

When discussing the cycling endurance of 1T1C FeRAM under realistic operation, it is necessary to consider cycling tolerance for hard breakdown but also the impact of the fatigue and its recovery.

In this chapter, the dependence of reliability on the $Hf_{0.5}Zr_{0.5}O_2$ thickness was investigated to improve the cycling tolerance for hard breakdown and reduce an operating voltage. First, the experimental method is described in Section 6.2 for the thinner 1T1C FeRAM memory array. Second, the fundamental ferroelectric properties with thinner $Hf_{0.5}Zr_{0.5}O_2$ is verified with single capacitor and 1T1C FeRAM memory array in Section 6.3.1. Third, cycling tolerance for hard breakdown was investigated to verify the impact of film thickness scaling in Section 6.4. Finally, fatigue and its recovery was investigated in these stage to confirm the characteristic under realistic operating condition and reveal the uniformity for the first time in Section 6.5.



(a)



(b)

Figure 6.1. Schematic illustration of ferroelectricity in 4 stages; pristine, Wake-up, fatigue and recovery (a) Polarization during cycling stress for operation stress and recovery stress. The recovery stress should higher stress than operation stress. (b) Example of ferroelectric behaviour of polarization vs. electric field plots for the 4 stages.

6.2 Experiments

To improve a cycling tolerance for hard breakdown and reduce a write voltage of 1T1C FeRAM memory array, film thickness scaling of the HZO was conducted. Film thickness scaling has been a widely used technique in scaling of CMOS transistors, and also be used in ferroelectric memory development to obtain lower write voltages. The voltage can be controlled, resulting from film thickness dependency of the effective electric field between both conductive layers such as metal or Si by the following equation.

$$V = E \cdot d \tag{6.1}$$

where V is the applied voltage, E is the electric field between the electrodes, and d is the thickness of the ferroelectric film. Furthermore, by applying the film thickness scaling, cycling endurance tolerance is also expected as well. This effect can be explained by the same theory for metal/oxide/silicon (MOS) structures, with lower electron energy for a given field on thinner SiO_2, indicating better breakdown resistance[70] as described in the Figure 6.2.

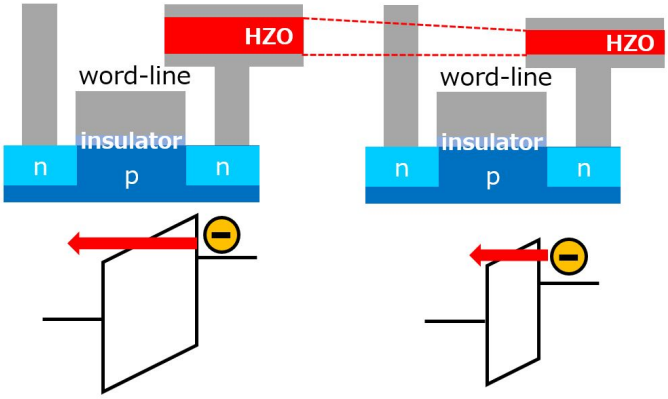


Figure 6.2. Schematic illustration of a motivation of film thickness scaling of HZO and band diagram in the HZO in this thesis.

Taking for example the three devices mentioned in the Chapter 1; FeFET, FTJ and 1T1C FeRAM, 1T1C FeRAM has an advantage of using this technology due to

the better interfacial layer.In terms of FeFET, the ferroelectric film thickness need to be optimized considering the ferroelectricity of the ferroelectric layer and dielectric breakdown of the insulator caused by divided voltage[71]. In the case of FTJ, the thickness of the ferroelectric film must be optimized to control the modulation of the barrier height through the ferroelectric material and the intermediate interface layer while taking into account the tunneling current. On the other hand, 1T1C FeRAM does not require the intentional deposition of an insulator layer, allowing for more flexibility in lowering the voltage compared to FeFETs and FTJs. The strategy for low-voltage operation with thickness scaling was comprehensively reported, revealing that 1.2 V operation is possible with a large single capacitor in 4 nm thick $Hf_{0.5}Zr_{0.5}O_2$ (HZO)[72].

In this thesis, dependence of reliability on film thickness was investigated using single large MFM capacitor of 1,000 μm^2 area with 1,000 capacitors (1 μm^2 each) connected in parallel were integrated for an intrinsic study of ferroelectricity and dielectric behavior of MFM capacitor with $Hf_{0.5}Zr_{0.5}O_2$. This capacitor was fabricated at the same time of the 64 kbits 1T1C FeRAM. For the study using 1T1C FeRAM array, 64 kbits $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM was integrated in 130 nm CMOS technology as described in Section 3.3. A capacitor under bitline (CUB) structure was used for the memory array. Planar MFM capacitors made of PVD-TiN/ALD-$Hf_{0.5}Zr_{0.5}O_2$/CVD-TiN were stacked on the planar transistor contact plug. To investigate array-level thickness scaling, tree types of HZO samples with thickness values of 5 nm, 8 nm and 10 nm were prepared by similar process in Section 2.2.The HZO film thickness was confirmed by ellipsometer measurements. Rapid thermal annealing (RTA) at 600°C was performed on both HZO samples to obtain significant ferroelectric properties with high remanent polarization in terms of memory window. If insufficient thermal budget is applied to the capacitors, the film would contain more anti-ferroelectric or amorphous domains, resulting in lower remanent polarization. The RTA did not degrade the characteristics of the CMOS transistors post back-end-of-line (BEOL) process.

6.3 Validation of ferroelectric performance on thinner HZO

6.3.1 Fundamental analysis with single capacitor

The impact of film thickness scaling effect from 10 nm thick to 5 nm thick on the ferroelectric performance was verified using a single large capacitor.The ferroelectricity and its reliability were investigated. Figure 6.3 shows the presence of ferroelectric orthorhombic phase for 5, 8 and 10 nm samples by grazing incidence X-ray diffraction (GIXRD). The intensity associated with the tetragonal or orthorhombic phase at around 30 deg was almost same between 8 nm and 10 nm samples but slightly increased at 5 nm sample. Furthermore, the intensity around 35 deg was decreased with thinner film, indicating that less monoclinic phase should be contained in thinner film.

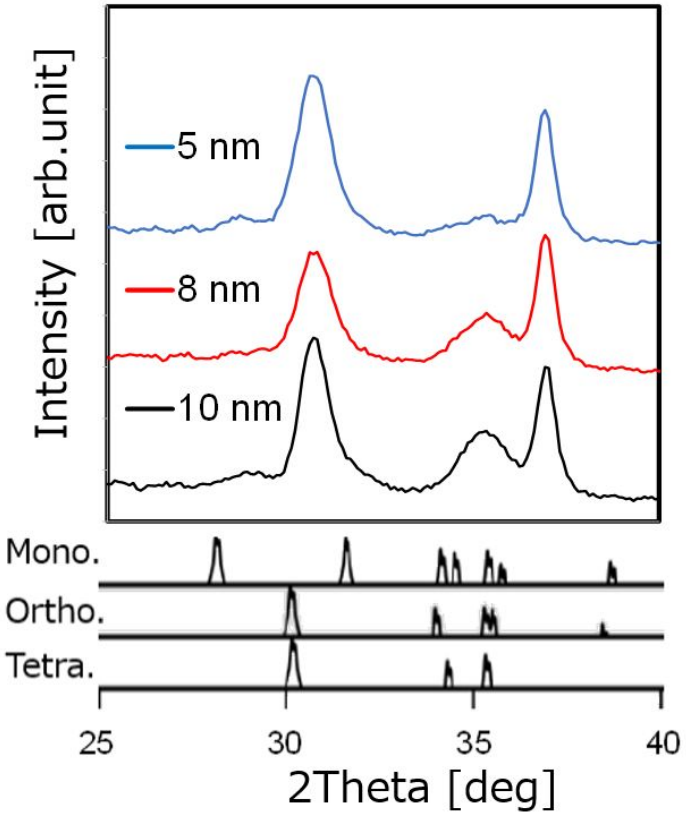


Figure 6.3. GIXRD spectra on 5, 8 and 10 nm thick HZO MFM capacitors.

Figure 6.4 shows the polarization vs electric filed for MFM capacitors with 5, 8 and 10 nm thick HZO at maximum applied electric field of 3 MV/cm at 1 kHz. Almost similar remanent polarization (2Pr) was observed between 8 nm and 10 nm thick HZO samples, while smaller 2Pr for 5 nm sample. Taking into account the GIXRD result in Figure 6.3, more tetragonal phase could exist at 5 nm thick HZO than polar-orthorhombic phase. The more difficult it is to obtain ferroelectric properties derived from polar-ortholombic phase, and more higher crystallization anneal would be required[72].

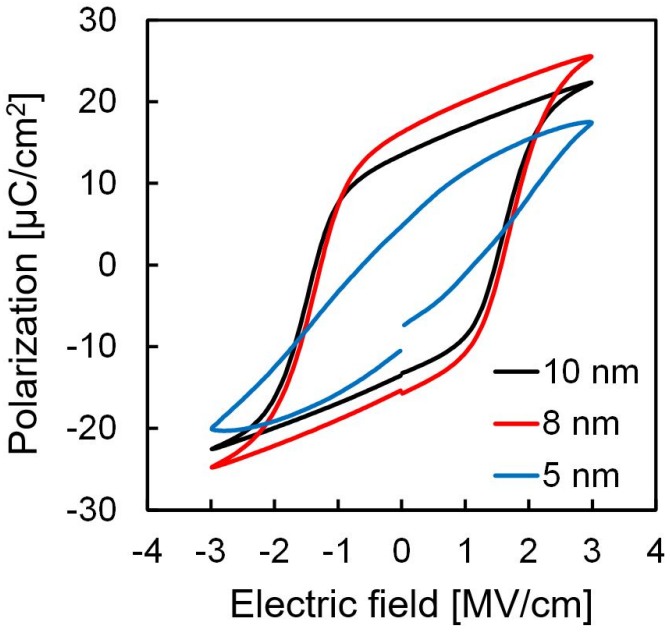


Figure 6.4. Polarization vs electric filed for MFM capacitors with 5, 8 and 10 nm thick HZO at maximum applied electric field of 3 MV/cm at 1 kHz.The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept.

Figure 6.5 shows the remanent polarization of the MFM for 8 and 10 nm thick HZO samples characterized by polarization vs. voltage measurements at a maximum applied voltage of 3 V. 5 nm thick HZO sample has been broken during measurement and not shown in the figure. Ferroelectric hysteresis indicates the presence of a ferroelectric polar-orthorhombic phase in both cases. A slightly higher remanent polarization ($2Pr \sim 32\ \mu C/cm^2$) was observed for the 8 nm sample than

for the 10 nm sample (2Pr $\sim$ 27 μC/cm^2), which was consistent with GIXRD results.Figure 6.6 shows the polarization vs. voltage hysteresis when a low applied voltage is applied to an 8 nm thick sample. The hysteresis maintains the main loop at 1.8 V, indicating that this capacitor may operate at an operating voltage of 2.0 V, which is lower than 10 nm sample. Figure 6.7 shows applied voltage dependence of capacitance and remanent polarization (2Pr) for data0 and data1. The capacitance were extracted by the definition in Figure 3.6. The capacitance was gradually increased with small applied voltage owing to sub-loop like behavior. The impact of this capacitance shift will be further investigated in next Chapter.

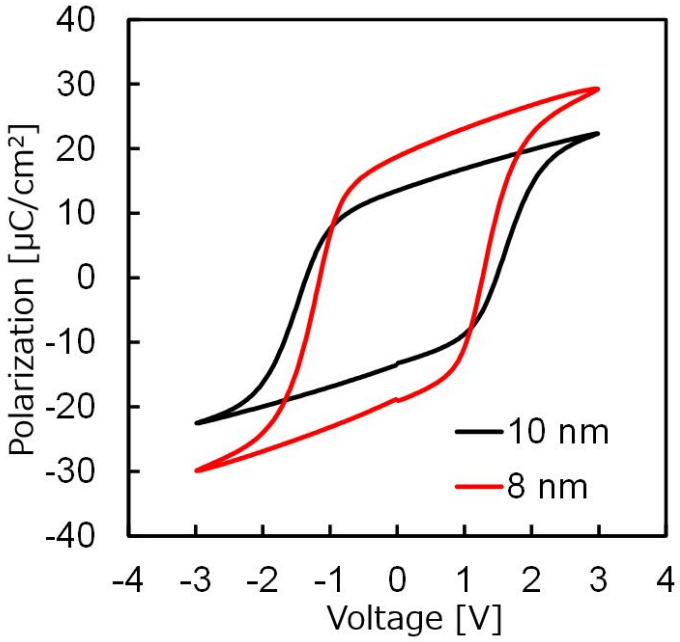


Figure 6.5. Polarization vs voltage hysteresis of a MFM capacitor for 8 and 10 nm thick HZO samples with applied voltage of 3 V at 1 kHz. 5 nm thick HZO sample has been broken during measurement and not shown in this figure.The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept.

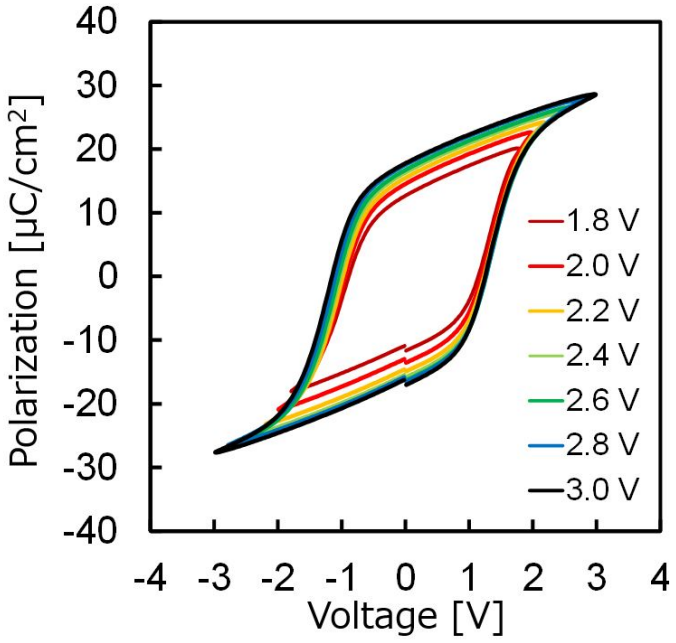


Figure 6.6. Dependence on applied voltage ranging from 1.8 to 3.0 V for the 8 nm sample. The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept.

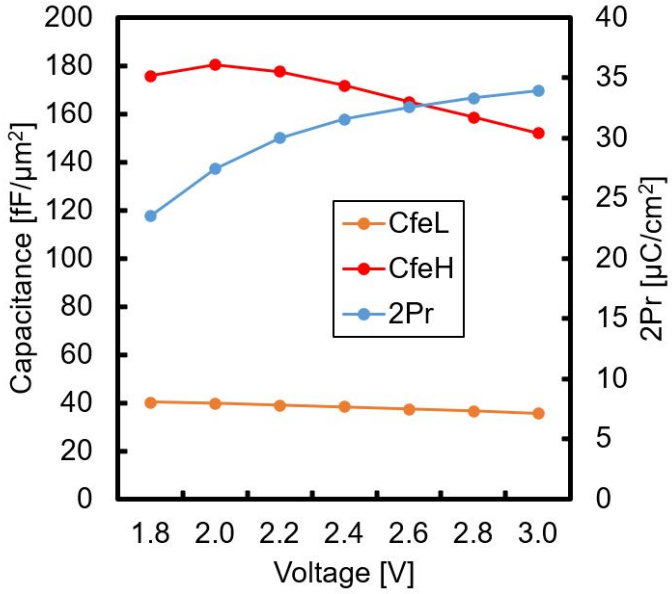


Figure 6.7. Applied voltage dependence of capacitance and remanent polarization (2Pr) for data0 and data1 extracted by definition in Figure 3.6.

The endurance property of HZO with a thickness of 8 nm was examined up to 10^9 cycles at a stress voltage of 2.0 V, as shown in Figure 6.8. The remanent polarization decreased by 30% from 10^5 cycles to 10^9 cycles owing to the fatigue phenomenon of the MFM structure, and hard breakdown was not observed. Considering the cycling frequency of the practical use case at 10 MHz, the cycling endurance was projected to be higher than 10^{11}cycles. The impact of this fatigue will be further investigated in next Chapter.

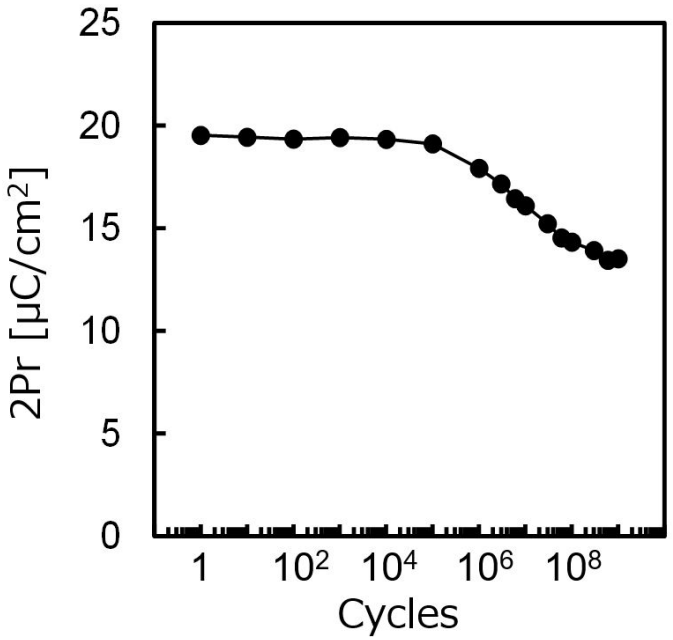


Figure 6.8. Reliability result for endurance at 2.0 V stress voltage and at 100 kHz Dynamic Hysteresis Measurement post wake-up cycling for the 8 nm thick sample. Measurement was stopped at 10^9 cycles.

The data retention test at 85°C for 60 min was measured, revealing that the change in the polarization value of the sample at 500°C was negligible, and a slight degradation up to 10 years was expected as shown in Figure 6.9. These results indicate that this MFM structure is suitable for fabricating integrated 1T1C FeRAM with high reliability and excellent performance.

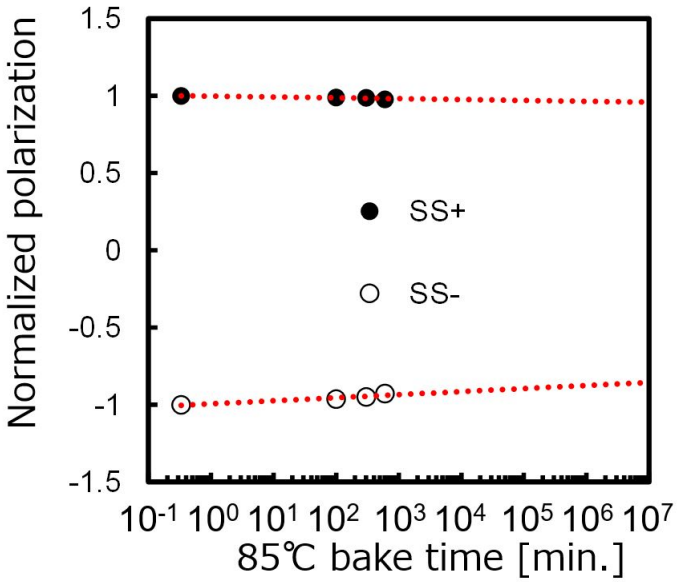
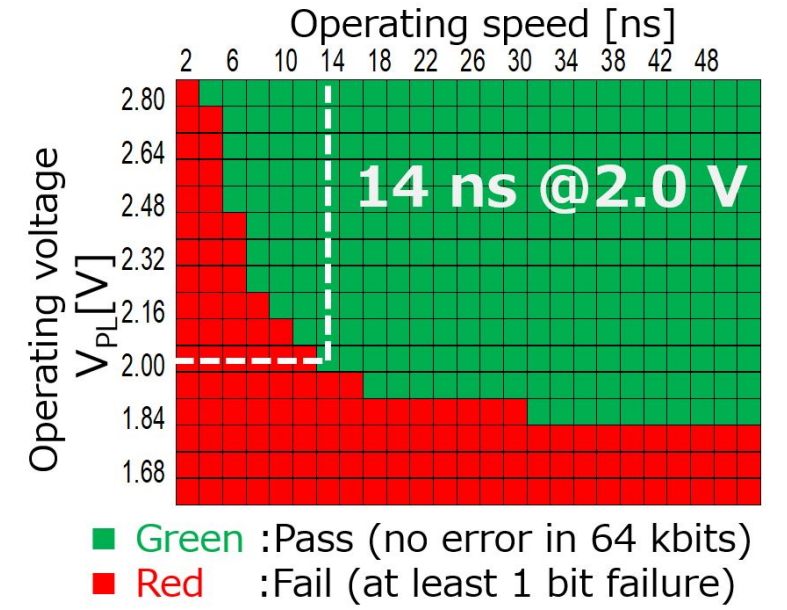


Figure 6.9. Retention tests have been performed on HZO with a thickness of 8 nm for firing times up to 60 min at 85°C and prediction up to 10 years under the same conditions. The line in the Figure is a least-squares fitting using data.

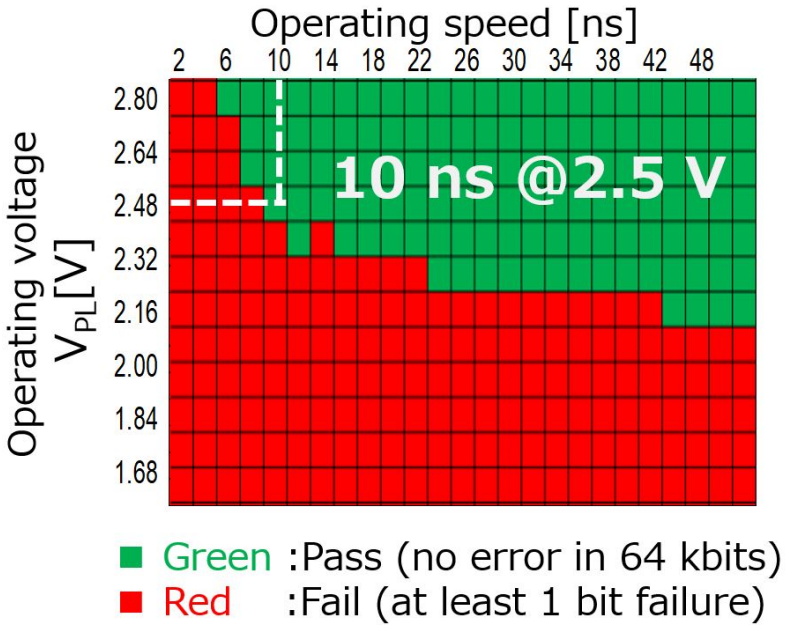
6.3.2 Memory array performance of thinner HZO

Figure 6.10 shows a comparison of shmoo plots about array performance between 10 nm thick HZO and 8 nm thick HZO samples. Shmoo plot for the write operation and sense operation were merged as described. 8 nm sample enables lower voltage operation at 2.0 V with 14 ns operating speed, which is in good agreement with a single capacitor result in Figure 6.5.

The distributions of ΔV_{BL} for the 8 nm thick HZO for both C0 and C1, described in Figure 3.6, were detected by the SA. Figure 6.11 shows the normal probability plot of ΔV_{BL} for each capacitor area of 0.06, 0.20, 0.40 and 1.00 μm^2 at an operation voltage 2.0 V for both polarization states of data0 (up state) and data1 (down state). A Perfect bit functionality in the 64 kbits array was observed for each capacitor area, demonstrating no degradation of the variability even if the smallest capacitor area was 0.06 μm^2. The dependence of the memory window at the median value ofΔV_{BL} on each capacitor area was compared with the simulation result, as shown in Figure 6.12. The obtained memory window margins corresponded with the estimation for the 130 nm technology.



(a)



(b)

Figure 6.10. Shmoo plot of time ranging from 1 to 50 ns and operation voltage ranging from 1.6 to 2.8 V obtained (green: pass, red: fail) on the 64 kbits 1T1C FeRAM memory array for (a) 8 nm thick HZO at 0.2 μm^2 and (b) 10 nm thick HZO at 0.4 μm^2.

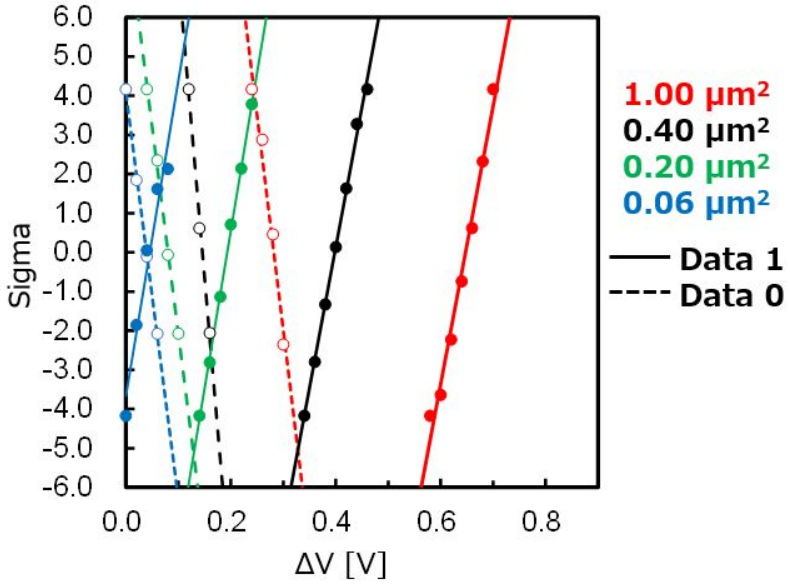


Figure 6.11. ΔV_{BL} distribution of the 1T1C FeRAM for 64 kbits at 2.0 V with 100 ns operation at 0.06, 0.20, 0.40 and 1.0 μm^2 capacitor areas using the 8 nm sample.

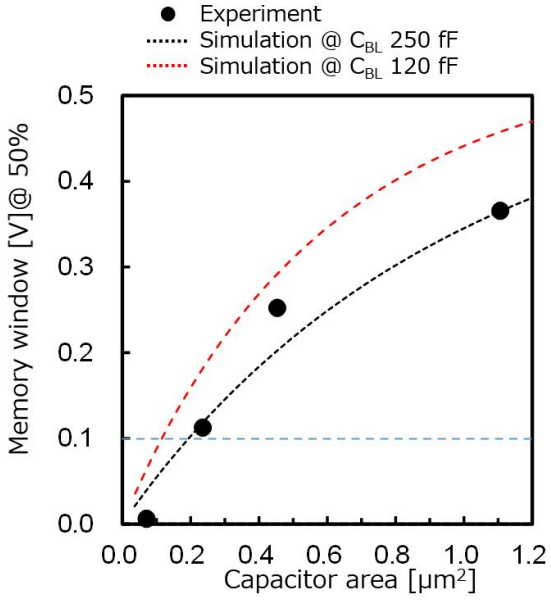


Figure 6.12. Read margin of test chip 2.0 V, 100 ns operation as a function of capacitor area. Values of C_{BL} were determined as 250 fF for the 130 nm technology and 120 fF for the 40 nm technology.

The capacitance change during low-voltage operation, which was confirmed in the single capacitor evaluation in Figure 6.7, was investigated using 1T1C FeRAM. The rate of capacitance change due to lower voltage operation from 2.8 to 2.0 V for single capacitor and 1T1C FeRAM were compared. The parameter of single capacitor was calculated using Figure 6.7. The capacitance of 2.0 V for 1T1C FeRAM was calculated by Figure 6.11 and 2.8 V by Figure 6.31, respectively using the Equation 5.4. The capacitance of both data0 and data1 increased more than 10% in single capacitor, while the capacity change estimated from 1T1C FeRAM were below 3%. This indicates that the capacitance definition based on the Equation 5.4 is not realistic for near-sub-loop operation, and correct capacitance estimation requires estimation by further transient analysis, such as measuring the frequency and duty dependence of capacitance.

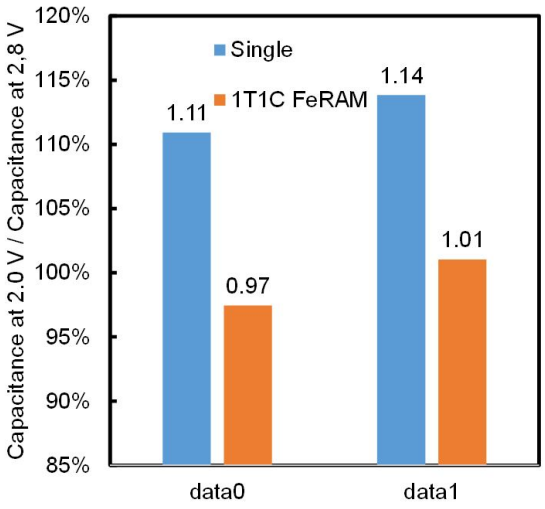


Figure 6.13. The rate of capacitance change due to lower voltage operation from 2.8 to 2.0 V for single capacitor and 1T1C FeRAM. The parameter of single capacitor was calculated using Figure 6.7. The capacitance of 2.0 V for 1T1C FeRAM was calculated by Figure 6.11 and 2.8 V by Figure 6.31 using Equation 5.4.

These results indicates that lower voltage operation of 2.0 V was achieved by thinner 8 nm sample without degradation of uniformity of HZO material and scaling capability, comparing 10 nm sample described in Section 4.

6.4 Cycling tolerance for hard breakdown

In this section, cycling tolerance for hard breakdown was investigated using 5, 8 and 10 nm thick HZO films. First, fundamental analysis on cycling tolerance for hard breakdown was evaluated using the samples in Subsection 6.4.1. Then, cycling tolerance for hard breakdown for memory array was discussed in Subsection 6.4.2 .

6.4.1 Fundamental analysis with single capacitor

Fundamental analysis on cycling tolerance for hard breakdown was evaluated using the single capacitor with 5, 8 and 10 nm thick HZO films at a total area of 1,000 μm^2 MFM capacitor.

Figure 6.14 shows the current density as a function of electric field on the samples. The higher breakdown electric field (EBD) was observed with thinner HZO at 5.5 MV/cm for 5 nm, 4.8 MV/cm for 8 nm, and 4.2 MV/cm for 10 nm thick HZO. It is consistent result with a similar theory according to the metal/oxide/silicon (MOS) described in Section 6.1. However current density of 5 nm thick HZO shows dramatically larger than others. There are two possible causes for the sudden increase in leakage current at 5 nm. One is due to the direct tunnel current flowing between the electrodes[73], and the other is the increase in leakage due to the dispersion of oxygen defects[68]. As mentioned in Figure 6.4, the crystal phase of 5 nm thick HZO is clearly different from others, suggesting that the significantly larger number of oxygen vacancy (Vo) or charge defects in the film may have increased the leakage path formation. In that case, this leakage current can be suppressed by increasing the thermal history or optimizing the HZO deposition process to improve the crystallization phase.

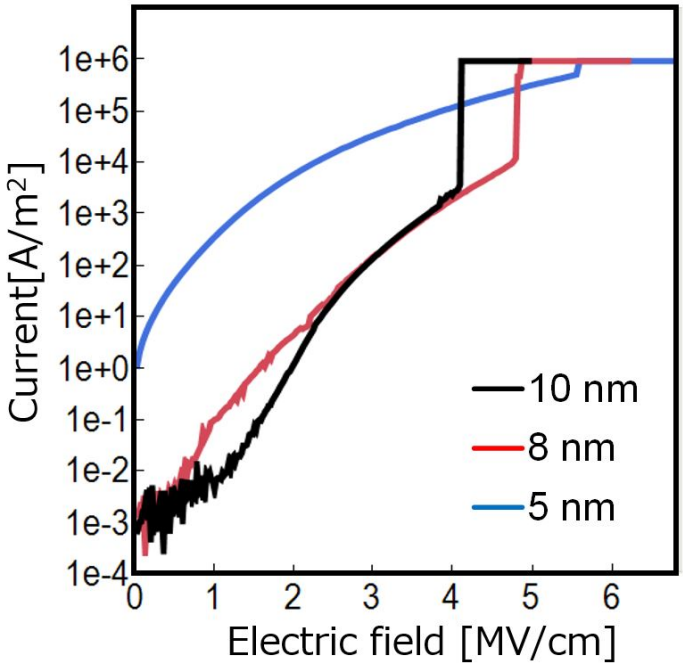
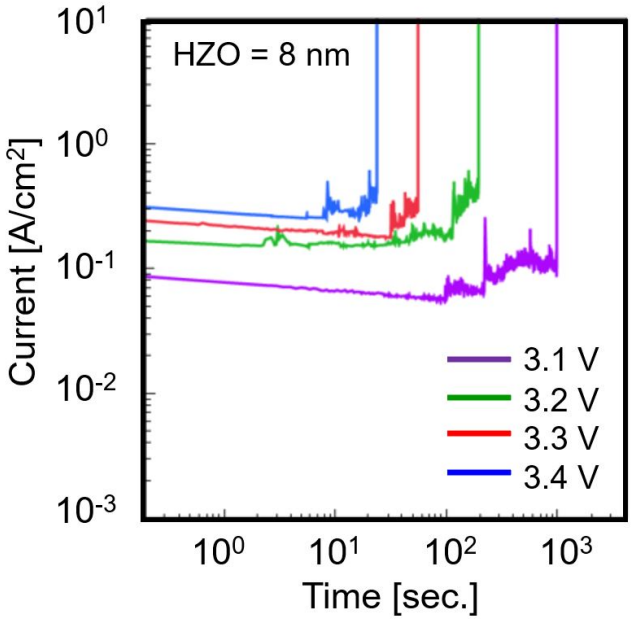
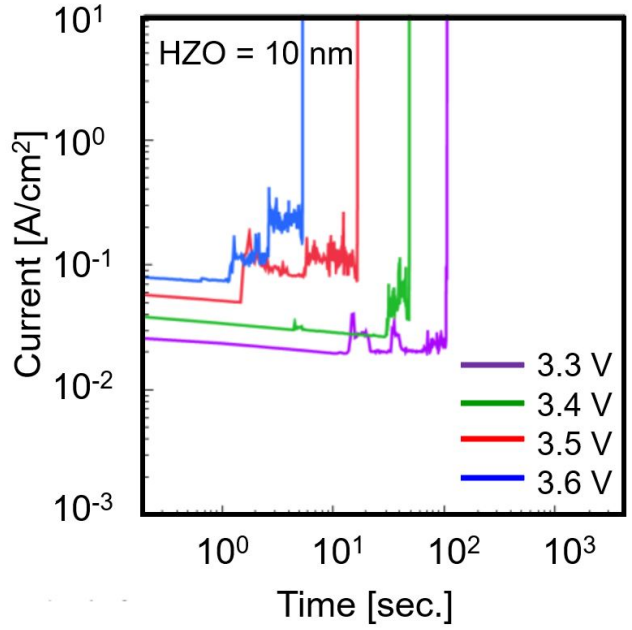


Figure 6.14. J-E characteristics of 5 (blue), 8 (red) and 10 nm (black) samples consisting of one large MFM capacitor at 1,000 μm^2 with 1,000 capacitors connected in parallel (1 μm^2 each). The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept at 2 V/s.

The TDDB characteristics of the MFM capacitors were obtained by current-time trace tests, where constant voltage stresses of 3.3, 3.4, 3.5 and 3.6 MV/cm were applied to the 10-nm samples (Figure 6.15 (b)). While, stress voltage of 3.9, 4.0, 4.1 and 4.3 MV/cm were applied to the 8 nm sample (Figure 6.15 (a)). The 5 nm thick HZO was excluded from the TDDB measurement because of its large leakage current and inability to detect clear breakdowns. In both 8 nm thick and 10 nm thick case, the current through MFM capacitors gradually decreased with time, and soft breakdown was observed before hard breakdown. This phenomenon can be explained by the formation of trap sites in the film and the generated defects forming percolation paths along the trap sites[74]. The P–V characteristics during soft breakdown at 8 nm thick HZO sample were confirmed, resulting in clear remanent polarization was obtained described in Figure 6.16. Therefore, the hard breakdown time (tBD) of the film was extracted as the lifetime at which the current flow exceeds 10 A/cm^2, resulting in lower tBD at higher applied voltages. The tBD at 63% (T63) versus electric field for samples of both thicknesses were plotted in a log–log graph (Figure 6.17).



(a)



(b)

Figure 6.15. Results of current trace measurements for (a) 8 nm and (b) 10 nm thick samples with one large MFM capacitor of 1,000 μm^2 area and 1,000 capacitors (1 μm^2 each) connected in parallel. The 5 nm thick HZO was excluded from the TDDB measurement because of its large leakage current and inability to detect clear breakdowns.

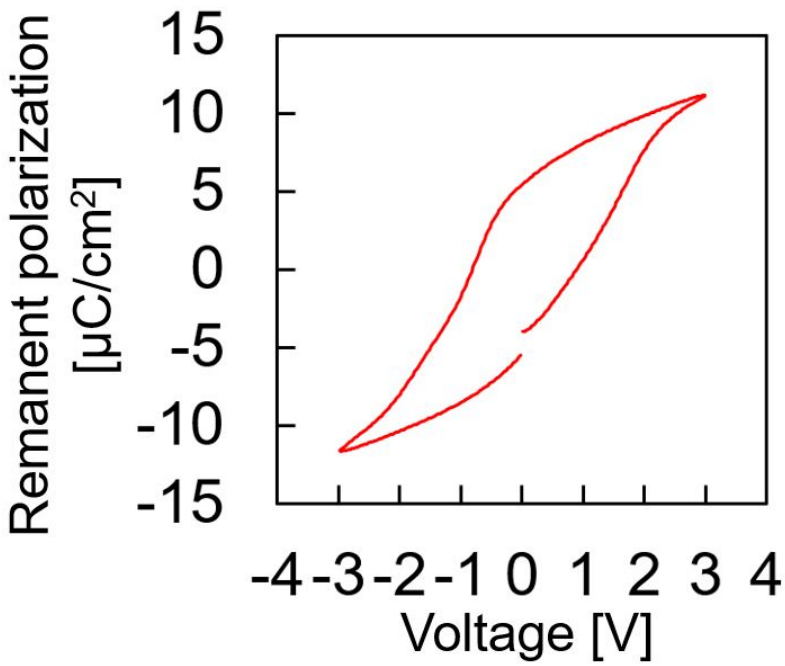


Figure 6.16. P–E characteristics post soft breakdown during the current–time trace measurement on another device under the same test conditions. The bottom electrode was fixed to ground and the applied voltage of the top electrode was swept.

The tBD follows a power-law fit (tBD $\propto V^{-n}$) for both samples, as commonly accepted[75]. The tBD of the 8 nm thick HZO sample was longer than that of the 10 nm sample, which is in good agreement with the value of EBD in Figure 6.14 while maintaining parallelism. The accelerated factor of the tBD from 4.4 MV/cm to 2.5 MV/cm for the 8 nm sample was extracted at approximately 10^{12} cycles, as shown in Figure 6.17. Considering these effects, film thickness scaling should result in a reliable hard breakdown when operating at 2.0 V using a 1T1C FeRAM array.

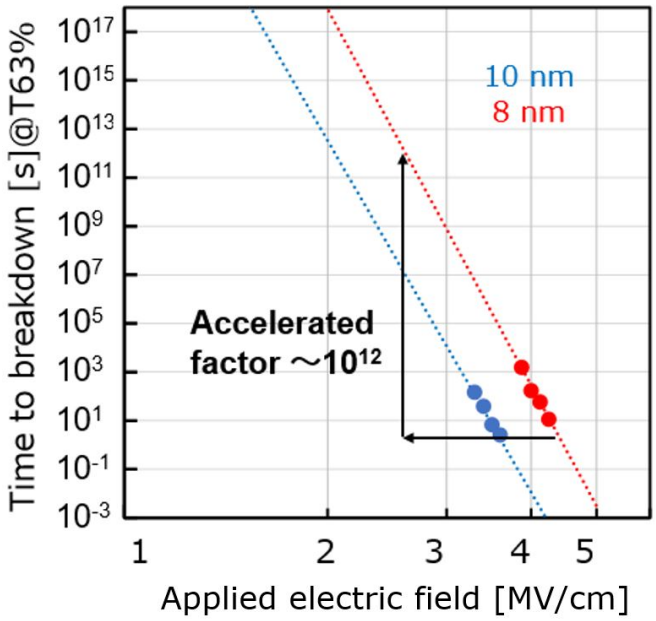


Figure 6.17. The tBD at 63% (T63) versus electric field in a log–log graph for both 8 nm (red) and 10 nm (blue) samples. A total of 22 devices were tested for stress for each sample. Weibull slopes of 1.01 and 1.00 were used for the 8 nm and 10 nm samples plots, respectively.

6.4.2 Cycling tolerance for hard breakdown with 1T1C FeRAM

The cycling tolerance for hard breakdown using 1T1C FeRAM memory array under realistic operating condition was firstly measured. Figure 6.18 shows a Raw-Bit-Error-Rates (RBERs) due to hard breakdown investigated on both 8 nm and 10 nm samples with 4 kbits for MFM capacitors in 1T1C FeRAM memory array with capacitance areas of 0.20, 0.40 and 1.00 μm^2. The measurement for 5 nm thick HZO has not been performed due to extremely high leakage.

Bipolar pulse cycling stress with 4.4 MV/cm, 100 ns was applied at 85°C as an accelerated condition. The cycle to failure of the earliest bit on the 8 nm sample was longer than that of the 10-nm sample in any capacitor size, which is in good agreement with the TDDB results in Figure 6.17. Five readouts were performed within a digit, and the fail bits were counted at that time. The area dependence on the cycle to failure was clearly observed following the Poisson distribution[76]. The area dependence converged as the number of cycles increased, implying that the failure mechanism changed with increased cycling. One possible explanation for this phenomenon is that as the number of cycles increased, too many trap sites were generated in the film, obscuring the dependence on the area.

The cycling tolerance for hard breakdown at an RBER of 1 ppm on the 8 nm sample was predicted under the operating conditions of 2.0 V and 100 ns at 85°C at a capacitor area of 0.20 μm^2 in the memory cell, as shown in Figure 6.19. Considering the accelerated factor extracted from the TDDB results in Figure 6.19, the value was projected to be 3.2×10^{18} cycles. Lower cycling tolerance for hard breakdown was obviously predicted for the 10 nm sample using the data on Figure 6.17 and Figure 6.18 with a same method. (Not shown)

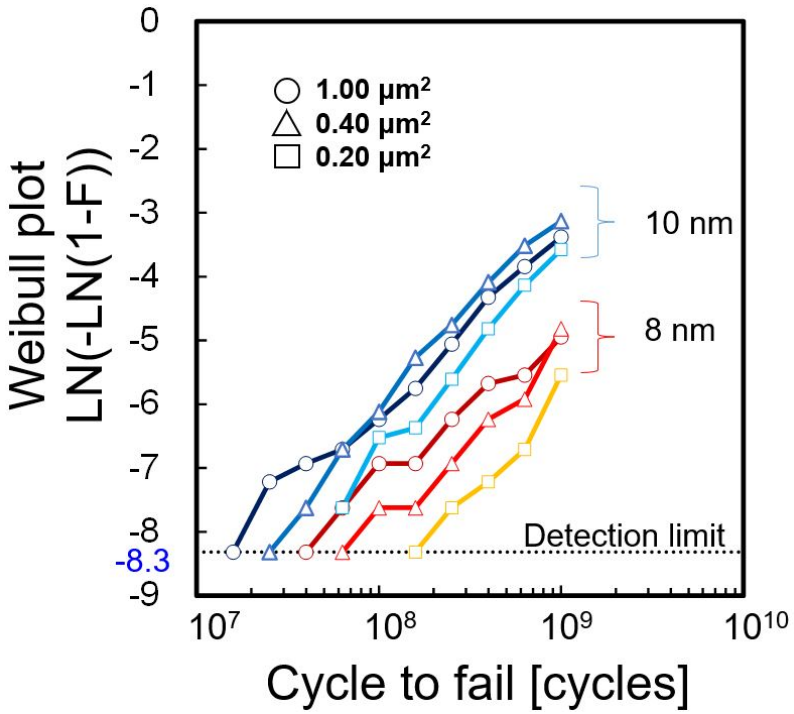


Figure 6.18. Weibull plot as a function of the number of cycles to failure for 4 kbits of the 8 nm and 10 nm samples at a capacitance area in a memory cell of 0.20, 0.40 and 1.00 μm^2 with a same bipolar stress electric field of 4.4 MV/cm on both samples. The detection limit was obtained by substituting 1/4000 for the probability of failure F in the Weibull formula. The measurement for 5 nm thick HZO has not been performed due to extremely high leakage.

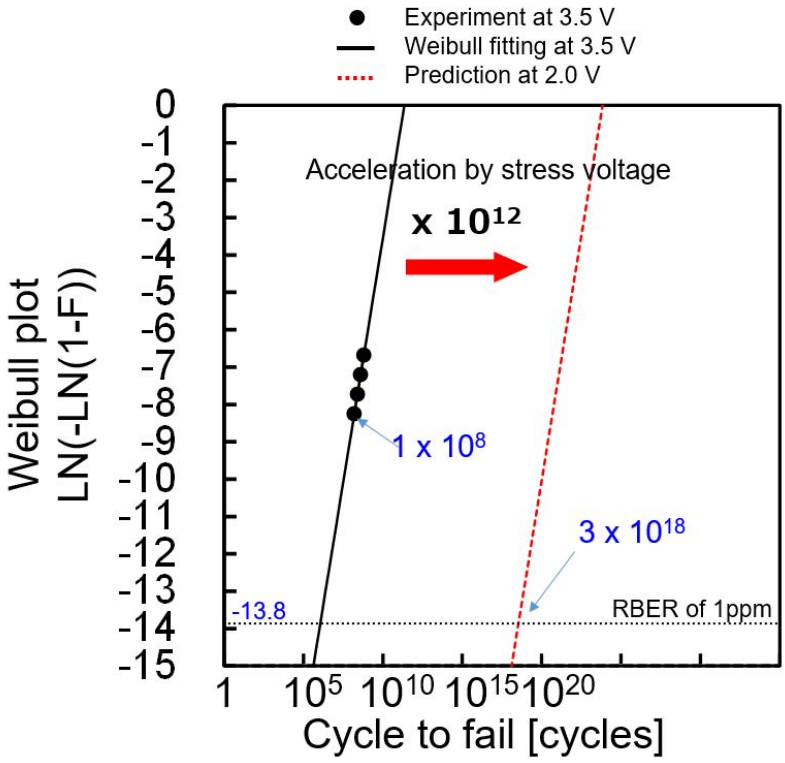


Figure 6.19. Weibull fitting plot as a function of the number of cycles to failure for the 8 nm sample at a capacitance area in a memory cell of 0.20 μm^2. The black line shows a fitting curve based on the experimental results at an operating voltage of 3.5 V. The red line shows a prediction at 2.0 V using accelerated factor extracted from Figure 6.17. The detection limit was obtained by substituting 1 ppm for the probability of failure F in the Weibull formula.

6.5 Fatigue and its recovery

This section discusses the fatigue and recovery characteristics of 1T1C FeRAM memory array with 8 nm thick HZO sample, which has never been addressed before. In Subsection 6.5.1, mechanism study of the recovery effect was investigated using single capacitor from switching current peak split point of view. And then, in Subsection 6.5.2, recovery effect was firstly qualified by applying various recovery condition using single capacitor. Finally, the fatigue and its recovery effect was confirmed and investigated the uniformity using the 1T1C FeRAM memory array for the first time in Subsection 6.5.3.

6.5.1 Fundamental analysis with single capacitor

Figure 6.20 demonstrates the measurement sequences during the fatigue, recovery and re-fatigue phases with 8 nm sample at 1,000 μm^2 area with 1,000 capacitors (1 μm^2 each) connected in parallel. To investigate current peak and its intensity, Positive-Up-Negative-Down (PUND) pulses were applied as a read sequence using voltages ranging from -2.8 to 2.8 V, which were higher than the cycling stress during the fatigue phase to investigate a current peak split clearly. A PUND measurment ranging from -2.4 to 2.4 V was applied to exclude the remanent polarization without current peak split. Figure 6.21 shows the P-V and I-V curves during the fatigue, recovery and re-fatigue phases. The current peak split at a cycling stress voltage of 2.0 V was observed during the fatigue and re-fatigue phases. During the recovery phase, the split current peak first merged, and then the current peak intensity increased. A remanent polarization (2Pr) as a function of cycling stress during each phase in Figure 6.20 was described in Figure 6.22 using red lines. An internal field (E_{int}) was derived by following equation.

$$E_{\text{int}} = 1/2(|Ep| - |En|) \tag{6.2}$$

where Ecp and Ecn represent positive and negative coercive fields described in Figure 3.6, respectively.The coercive fields were extracted from the voltage with peak current in Figure 6.20 bottom I-V curves. It is known that TiO_xN_y or TiO_x could

be formed by N diffusing out the oxygen in HZO and top electrode during deposition, respectively. These interfacal layer should cause work function differences between the top and bottom electrodes and charge trapping at the interface, resulting in an internal electric field[68,77,78]. The E_{int} is represented by the blue lines shown in Figure 6.22. The E_{int} increased with cycling stress in the fatigue phase, whereas in the recovery phase it decreased. This result implies that that a positively charged oxygen vacancy generated by electron detrapping at bottom electrodes could cause domain pinning during the fatigue phase and can be neutralized in the recovery phase[69], represented by Figure 6.23.

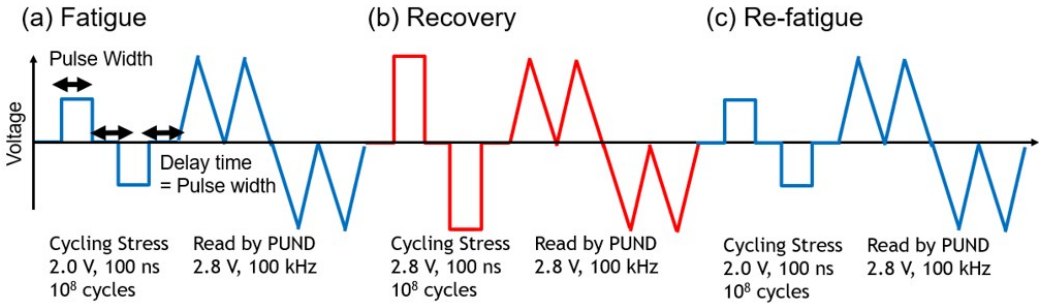


Figure 6.20. Measurement sequence during (a) Fatigue up to 10^8 cycles with a cycling stress voltage of 2.0 V and the pulse width of 100 ns (b) Recovery up to 10^8 cycles with a cycling stress voltage of 2.8 V and the pulse width of 100 ns, and (c) Re-fatigue up to 10^8 cycles with a cycling stress voltage of 2.0 V and the pulse width of 100 ns. PUND ranging from -2.4 to 2.4 V was applied to exclude the 2Pr without current peak split.

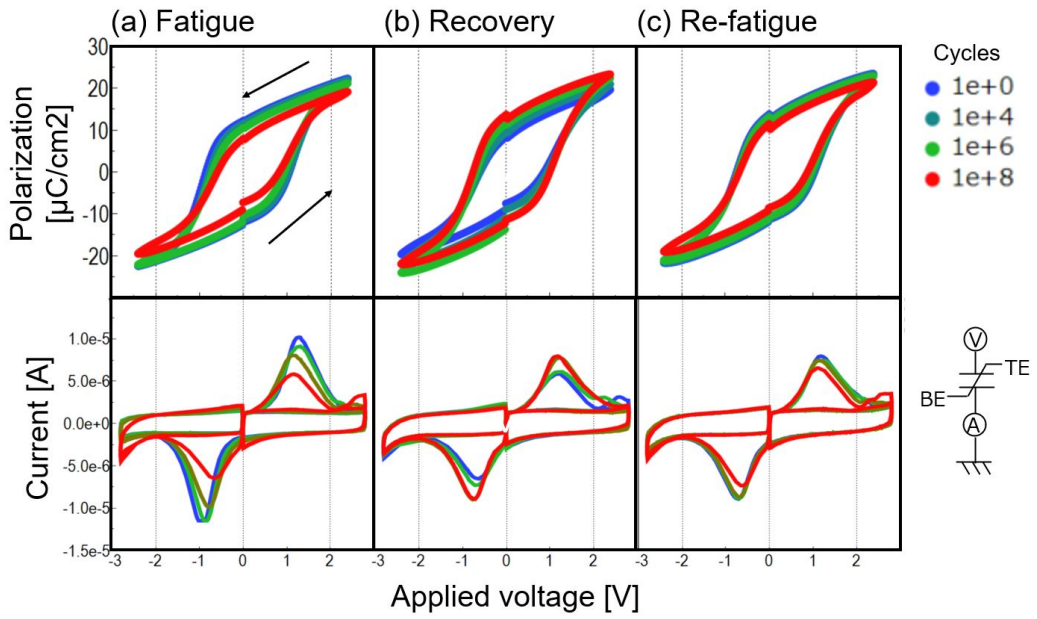


Figure 6.21. P-V curve and I-V curve obtained from PUND results during (a) Fatigue, (b) Recovery, and (c) Re-fatigue phases with 8 nm thick HZO at 1,000 μm^2 area with 1,000 capacitors (1 μm^2 each) connected in parallel. Positive bias was applied from top electrodes. PUND ranging from -2.4 to 2.4 V was applied to exclude the 2Pr without current peak split.

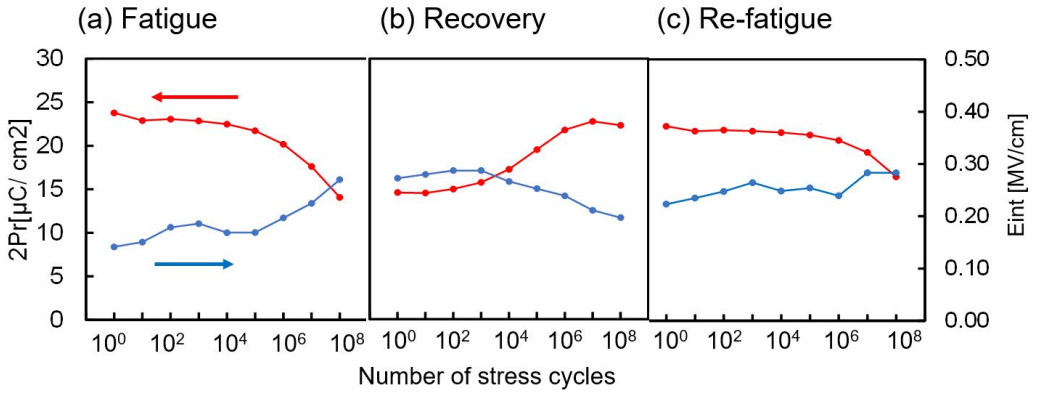


Figure 6.22. Remanent polarization and E_{int} as a function of cycling stress during (a) Fatigue, (b) Recovery, and (c) Re-fatigue phases. 2Pr was extracted by PUND pulse subscribing dielectric contribution in the left vertical axis. E_{int} was extracted by a formula of ½(|Ecp|-|Ecn|) in the right vertical axis.The coercive fields were extracted from the voltage with peak current in Figure 6.21 bottom I-V curves.

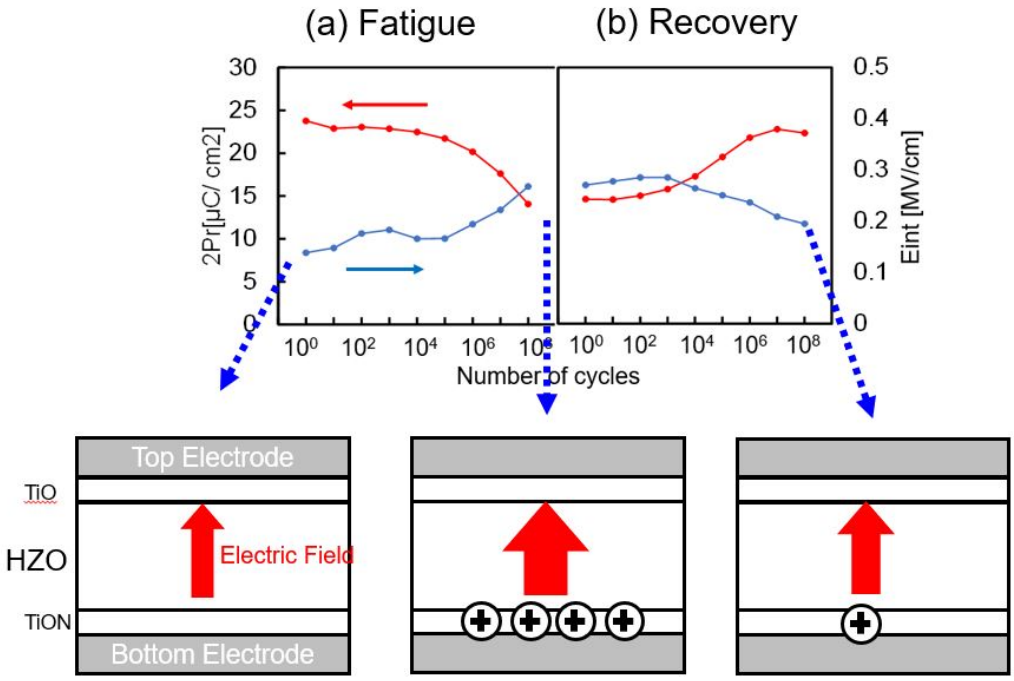


Figure 6.23. Schematic illustrations for E_{int} shift during (a) fatigue and (b) recovery.

From the result of current peak splitting behavior and decrement of E_{int}, the recovery mechanism can be explained as shown in Figure 6.24. In the initial state, there could be pinned domains that were not flipped by a stress voltage during the fatigued phase (Figure 6.24(a)). When a higher cycling stress was applied to the fatigued capacitor, the pinned domain started to flip via neutralization of the positively charged oxygen vacancy accompanied by electron de-trapping at the interfacial layer (Figure 6.24(b)) resulting in merged current peak splits. Applying further recovery stressed cycling, redistribution or generation of oxygen vacancy occurs resulting in more switching domains that can participate in remanent polarization owing to similar factors during wake-up behavior such as, phase change[79] or reorientation of domains[26] (Figure 6.24(c)).

In summary, a recovery mechanism was studied by in this section.First, a peak splitting behavior and its intensity were monitored during the fatigue, recovery, and re-fatigue phases. The E_{int} decreased with cycling stress during the fatigue phase and increased during the recovery phase. During the recovery phase, the current peak splits first merged, and then the current peak intensity increased. These results suggest a recovery mechanism in which positively charged oxygen vacancies are neutralized, resulting in domain pinning, followed by redistributed oxygen vacancies forming new switching domains.

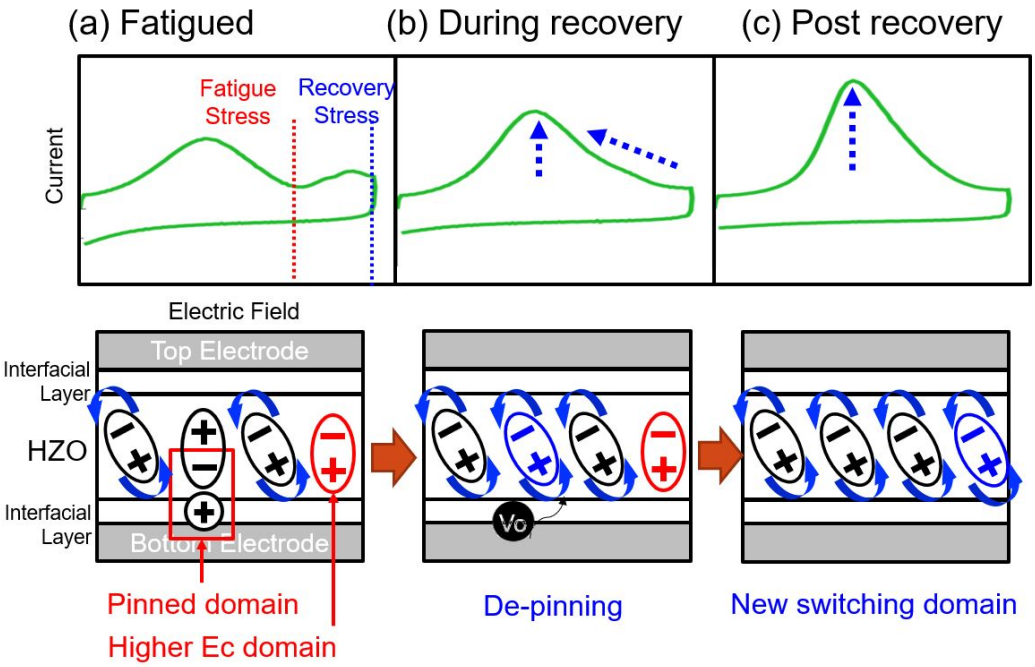


Figure 6.24. Recovery model during (a) fatigue, (b) recovery, and (c) further-recovery phases. I-V image extracted from Positive pulse in PUND sequence at upper row. Image of switching behavior of domains at bottom row.

6.5.2 Stress condition dependence of the recovery effect

A recovery effect was qualified by investigating various recovery stress pulses. Different recovery voltages and pulse widths shown in Figure 6.20 (b) were applied post fatigue stress shown in Figure 6.20 (a). Figure 6.1 (a) shows a qualification of the recovery effect obtained from the recovery voltage and pulse width dependence. The recovery ratio was determined by following equation.

$$Recoveryratio = Pr_{\text{recover}}/Pr_{\text{loss}} \tag{6.3}$$

where Pr_{loss} is the remanent polarization degradation post 10^8 cycles with a cycling stress voltage of 2.0 V, and $Pr_{recover}$ is the amount of Pr recovered from the fatigue post 10^5 recovery cycles. Higher recovery ratio was obtained with higher cycling voltage and longer pulse width as described in Figure 6.1 (b). There was no recovery effect observed at 2.0 V, and this was similar to that observed for fatigued stress voltage including when the pulse width was longer. Moreover, a large recovery ratio was obtained at recovery stresses higher than 2.4 V, indicating that a higher recovery voltage was required for the recovery phase, contrary to a higher fatigue stress voltage. Furthermore, the recovery ratio increased above 100 % when the recovery stresses and pulse widths where 2.8 V with 100 µs and 3.2 V with 10 µs, respectively. An impact of newly wake-up domains due to the recovery stress was investigated in Figure 6.27. The 2Pr of recovery stage under the condition of 3.2 V with 100 µs was saturated to the value of fatigue stage under the same condition of fatigue phase. This indicates that domains, which was not involved in switching during fatigue (Pr_{new}), contribute to enhance the recovery rate above 100% as shown in Figure 6.24 (c).

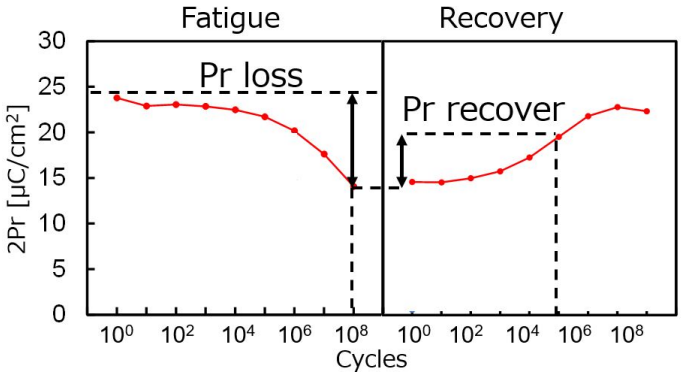


Figure 6.25. Definition of the recovery ratio.

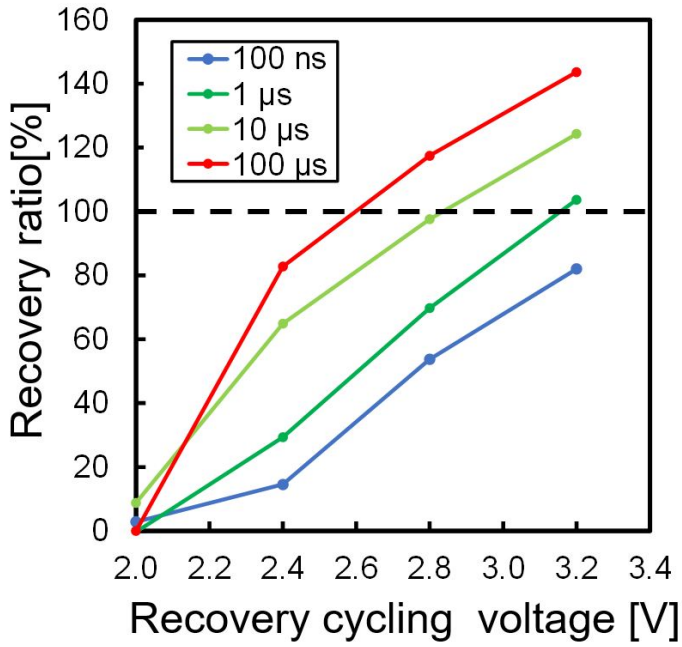


Figure 6.26. Recovery ratio calculation as a function of recovery cycling voltage ranging from 2.0 to 3.4 V (step 0.4 V) with different pulse width of 100 ns, 1 μs, 10 μs and 100 μs.

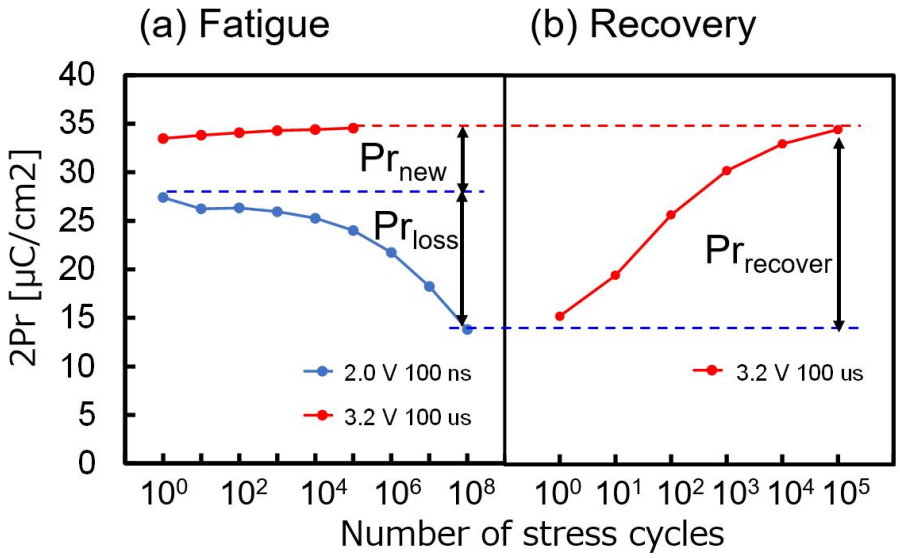


Figure 6.27. Remanent polarization as a function of cycling number during (a) fatigue with different conditions as 3.2 V with 100 μs in red and 2.0 V with 100 ns in blue and (b) recovery at 3.2 V with 100 μs.

The recovery cycling voltage dependence on the switching current with a fixed pulse width of 1 μs is shown in Figure 6.28. It can be observed that when the recovery stress voltage was 2.4 V, the current peak split was emerged, and the current peak intensity was saturated, indicating that the current peak split should be suppressed first by applying a higher recovery stress voltage. Figure 6.29 shows the recovery cycling pulse width dependence on the switching current with a fixed stress voltage of 3.2 V. The current peak split was merged including when the pulse width was 100 ns, and a higher current peak was obtained post 10^5 cycles with a longer recovery pulse width. These results summarized that the domain de-pinning and generation of polar domains can occur simultaneously under higher recovery voltage or longer recovery pulse conditions. These results is in good agreement with the assumed mechanism described in Figure 6.24.

In this section, the recovery effect was qualified by investigating the recovery voltage and pulse width dependence on the recovery ratio. A recovery ratio above 100% was obtained at a higher recovery voltage and longer recovery pulse width, which is in good agreement with the mechanism that domain de-pinning and new domains contribute to remanent polarization increment. A higher recovery ratio was obtained at a higher recovery voltage or longer pulse width in contrast to the stress condition of the fatigue phase, and the recovery voltage can be reduced by applying longer recovery pulse widths.

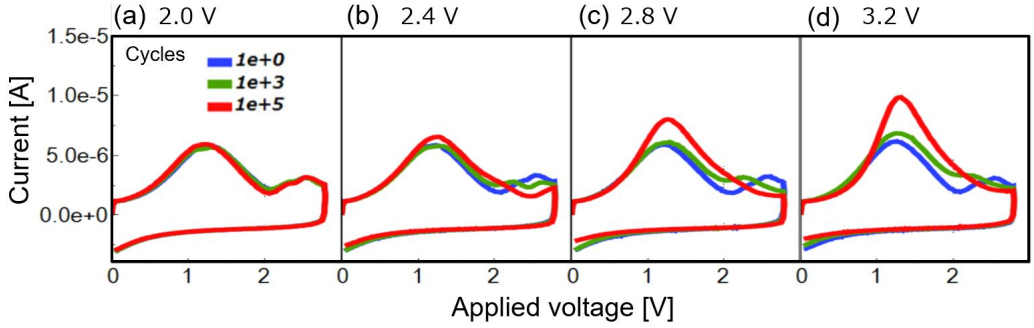


Figure 6.28. I-V curve during recovery cycling post fatigue stress with a different voltage condition of (a) 2.0 V, (b) 2.4 V, (c) 2.8 V and (d) 3.2 V, respectively. Only positive pulse during PUND pulse subscribing was described for simplicity.

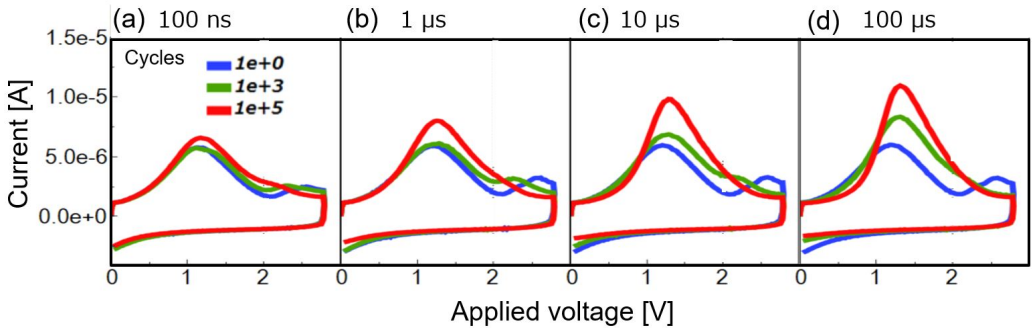


Figure 6.29. I-V curve during recovery cycling post fatigue stress with a pulse width condition of (a) 100 ns, (b) 1 µs, (c) 10 µs and (d) 100 µs, respectively. Voltage of the pulses were fixed as 3.2 V among these conditions. Only positive pulse during PUND pulse subscribing was described for simplicity.

6.5.3 Validation of fatigue and its recovery with 1T1C FeRAM

Figure 6.30 (a) shows the fatigue test result on the 1T1C FeRAM memory array post wake-up cycling under a stress voltage of 2.0 V at 10 MHz for up to 10^{10} cycles. ΔV_{BL} of data1 gradually decreases post 10^8 because of polarization fatigue, resulting in memory window degradation. Figure 6.30 (b) illustrates the recovery performance from fatigued bits under a stress voltage of 2.8 V at 10 MHz for up to 10^{10} cycles. The ΔV_{BL} of data1 increases with cycling and fully recovers to its initial value. The suggested fatigue and subsequent recovery mechanisms are charge trapping and de-pinning of domains in ferroelectric HZO, respectively. Trapped charges could pin domains, hindering their polarization reversal. Applying a higher electric field could result in charge de-trapping and subsequent domain de-pinning, allowing pinned domains to take part in the switching again. Figure 6.30 (c) shows the re-fatigue test result under a stress voltage of 2.0 V at 10 MHz for up to 10^{10} cycles. Degradation of ΔV_{BL} is only observed after 10^8 cycles, indicating that the recovery procedure prolongs the endurance performance. In contrast, minor changes were observed in ΔV_{BL} for data0 during fatigue, recovery, and re-fatigue, supporting the idea that a phase change in HZO could not cause this phenomenon.

Figure 6.32 depicts the normal probability distribution sigma plots of data0 and data1 for the initial, fatigued, and recovered samples described in Figure 6.30(a) and (b). Although memory window at -3 sigma was diminished at fatigued state, but clearly recovered at recovery state. Figure 6.33 shows variability of ΔV_{BL} in 4 kbits of 1.0 μm^2 capacitor area during initial, fatigue and recovery phase extracted from Figure 6.32 The distribution of data 0 is not deteriorated by the fatigue and recovery stress, supposedly indicating uniform charge trapping and domain de-pinning within the deployed HZO.

The distribution of data 1 was slightly improved from initial to fatigue and not changed from fatigue to recovery phase. It indicats that at initial stage charges were distributed in whole film resulting in higher variability of coercive field. In the fatigue and recovery stage, the distributed charges were collected to localized

locations such as grain boundaries, and would cause uniform charge trapping and detrapping.

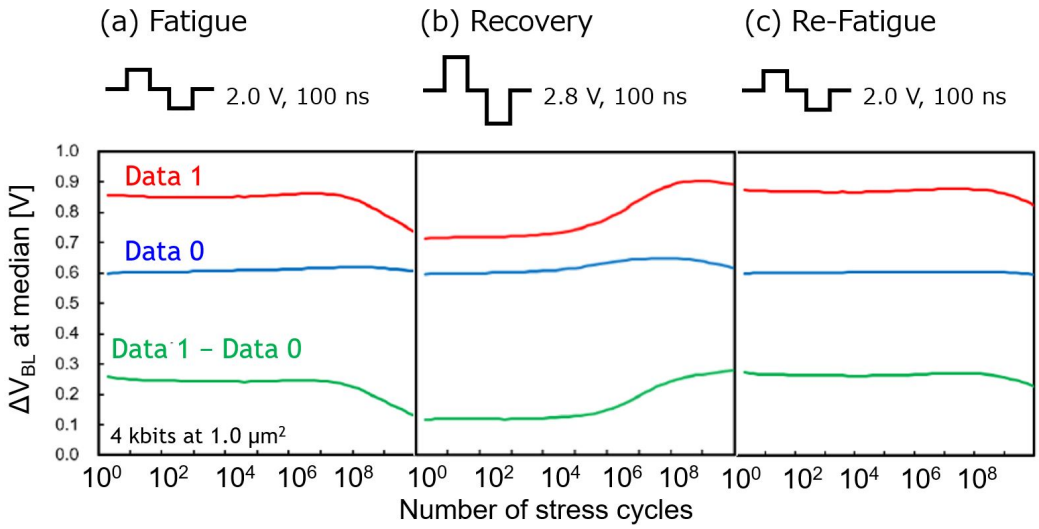


Figure 6.30. (a) Fatigue test result for 10^{10} cycles under a stress voltage of 2.0 V at 10 MHz, (b) Recovery test result of 10^{10} cycles under a stress voltage of 2.8 V at 10 MHz, (c) Re-fatigue test results for 10^{10} cycles post recovery under the same stress condition as (a). Median value of ΔV_{BL} in 4 kbits 1T1C memory cells with 1.0 μm^2 capacitor areas are extracted at each cycling phase.

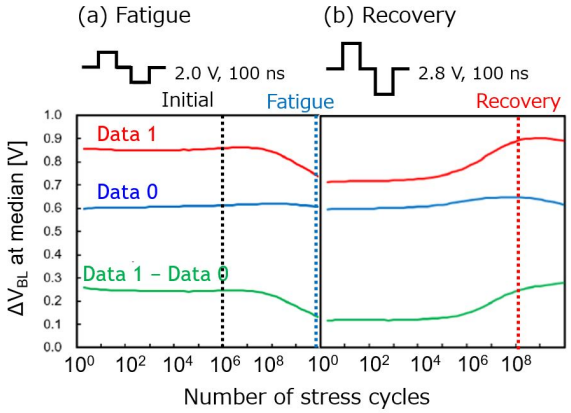


Figure 6.31. Definition of a data which was extracted in Figure 6.32. post 10^6 cycles and blue lines for 10^{10} cycles are extracted from Figure 6.30 (a). Red line shows a distribution post recovery stress at 10^8 cycles extracted from Figure 6.30 (b).

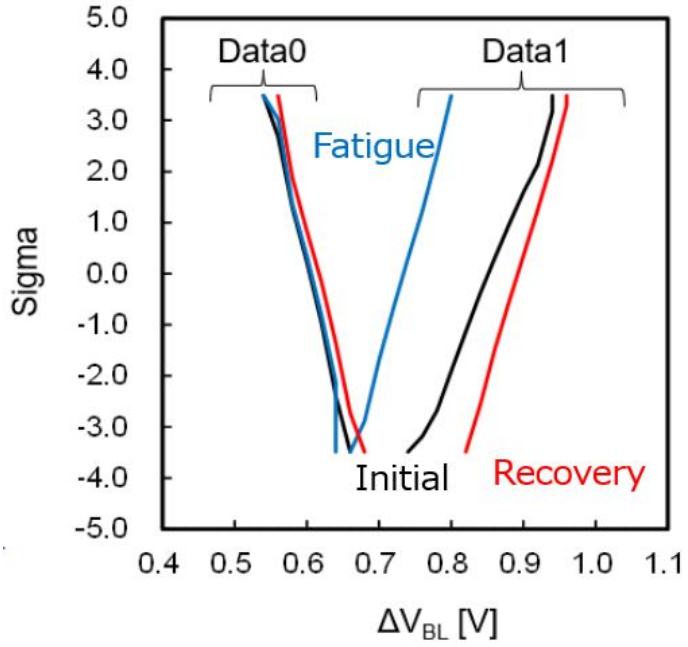


Figure 6.32. ΔV_{BL} distribution of data0 and data1 during endurance test. Black lines show an initial distribution, blue lines for 10^{10} cycles and red line shows a distribution post recovery stress.

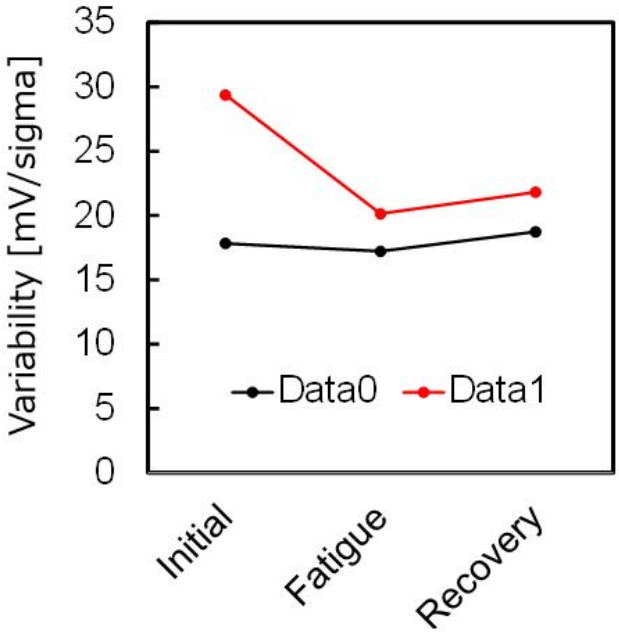


Figure 6.33. Variability of ΔV_{BL} in 4 kbits of 1.0 μm^2 capacitor area during initial, fatigue and recovery phase.

6.6 Summary

This chapter discusses a reliability of the $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM memory array by applying film thickness scaling of HZO from 10 to 8 nm, which has never been addressed before. First, ferroelectric performance of the thinner HZO material was verified in Subsection 6.3.1, demonstrating perfect functionalities in 64 kbits array with 2.0 V and 16 ns operating performance. The capacitance change during low-voltage operation was investigated comparing single capacitor evaluation and 1T1C FeRAM, resulting in larger capacitance change was obtained by single capacitor.This indicates that the capacitance definition based on the Equation 5.4 is not realistic for near-subloop operation, and correct capacitance estimation requires estimation by further transient analysis, such as measuring the frequency and duty dependence of capacitance.

Second, cycling tolerance for hard breakdown of the 1T1C FeRAM memory array with 8 nm thick HZO was investigated in Section 6.4, revealing no bit error count during 10^8 cycles at an accelerated operating voltage of 3.5 V and an operating speed of 100 ns, which was better than that of 10 nm thick HZO. This is because higher electric field was able to applied by thinner HZO. The 1 ppm RBER at 2.0 V, 100 ns, and 85°C operation was predicted to be > 10^{15} cycles, based on the dependence of time to breakdown on the stress voltage. This effect can be explained by the same theory for metal/oxide/silicon (MOS) structures, with lower electron energy for a given field on thinner SiO_2.The operating voltage is predicted to be reduced by further film thickness scaling. Under 1.2 V operation was reported by using 4 nm thick HZO[72]. However, it requires much higher crystallization anneal temperature (more than 600°C) to obtain a significant remanent polarization and the leakage current through the film becomes not negligible. Therefore, another approach is also required to achieve under 1.2 V operation voltage for cutting-edge-technology node.

Finally, fatigue and its recovery were investigated in Section 6.5. The ΔV_{BL} of data1 and data0 were extracted during fatigue and recovery cycling up to 10^{10} cycles, under a stress voltage of 2.0 V at 10 MHz and 2.8 V at 10 MHz, respectively. The

ΔV_{BL} for data1 was decreased post 10^8 cycles owing to a fatigue effect. However, the ΔV_{BL} for data1 significantly was recovered under stress, whereas slight changes were observed for data0. Furthermore, no degradation of the The ΔV_{BL} distributions was noted during fatigue and recovery measurements, indicating that charge trapping and domain de-pinning in HZO was uniform within the test chip. These results suggest that the HZO-based 1T1C FeRAM array is a good high-density and high-reliability replacement candidate for existing embedded memories.

Table 6.1 shows a comparison table with a target properties toward 1T1C FeRAM under 40 nm CMOS technology node. Perfect functionalities in 64 kbits array and array operation at 2.0 V and 16 ns were demonstrated experimentally. Cycling tolerance of hard breakdown was predicted to be > 10^{15} cycles under practical operating condition of 2.0 V and 100 ns. Although the ΔV_{BL} for data1 was decreased post 10^8 cycles owing to a fatigue effect, the ΔV_{BL} for data1 significantly was recovered under stress, whereas slight changes were observed for data0. Furthermore, no degradation of the The ΔV_{BL} distributions was noted during fatigue and recovery measurements, indicating that charge trapping and domain de-pinning in HZO was uniform within the test chip.

Table 6.1. Comparison table with target.

	SRAM	eDRAM	Target	$Hf_{0.5}Zr_{0.5}O_2$-based FeRAM HZO 8 nm
Write voltage	$\sim$ 0.5 V	$\sim$ 1.0 V	2.0 V	2.0 V
Write speed	$<$ 1 ns	20 $\sim$ 100 ns	$\sim$ 20 ns	$\sim$ 16 ns
Endurance	10^{16}	10^{16}	$\sim 10^{15}$	$\sim 10^{15}$ [(b)] for Hard Breakdown $\sim 10^8$ for Fatigue
Retention	No	No	85°C, 10 min	85°C, 100 min[(a)]
Scalability	5/7 nm	28 nm	40 nm	40 nm[(b)]

(a) Result using a single capacitor
(b) prediction

7 Conclusions

7.1 Summary of this thesis

Since ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-based material was reported in 2011, there has been much discussion about its application to 1T1C FeRAM. However, the feasibility with practical memory array operation using 1T1C memory cell structures has never been discussed. In the conventional method, a large area (larger than 100 μm^2) of metal/ferroelectric/metal (MFM) capacitor has been commonly used to amplify small displacement currents, resulting in unrealistic memory cell structure with limitation of operating condition due to RC delay. In this thesis, a novel 1T1C FeRAM memory array with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film using dedicated CMOS logic circuits was integrated into 130 nm CMOS technology node and demonstrated the memory array operation for the first time.

In Chapter 2, materials used in the 1T1C FeRAM were mentioned. $Hf_{0.5}Zr_{0.5}O_2$ was chosen as a ferroelectric material from large concentration window and CMOS process compatibility point of view. The atomic layer deposition process using TEMAHf + ZyALD as metal precursors and oxidizer were optimized to obtain higher remanent polarization considering limitation of thermal budget. The reason for this could be that ZyALD has high thermal stability and the residue of carbon-based reaction products generated by other organic precursors is less likely to be generated, which is said to reduce leakage paths in the film and provide good film quality.

In Chapter 3, experimental of the process integration and design of 1T1C FeRAM memory array with $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric film were mentioned. 64 kbits

of MFM capacitors with $Hf_{0.5}Zr_{0.5}O_2$-based material were implemented to 130 nm CMOS technology with capacitor under bitline structure. A dedicated sense amplifier for destructive read scheme was designed in the circuit. The change in bitline voltage (ΔV_{BL}) that occurs during read operation can be compared to a reference voltage (V_{REF}) generated from a reference capacitor (C_{REF}) or an externally applied voltage.

In Chapter 4, the memory array operation of 64 kbits $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM were investigated. First, the simulation result of the designed circuit revealed that it allows the 1T1C FeRAM to apply pulse width with less than 10 ns and the behavior of ΔV_{BL} during read operation for data0 and data1 were experimentally confirmed. A possible reason for this limitation is not material related switching but RC delay from circuit and it is assumed to be about 5 ns based on the simulation results. The memory array performance with write and sense voltages of 2.5 V and operation speed of 10 ns or less were verified by investigating a shmoo plot, and found to be in good agreement with the ferroelectric switching kinetics of the Nucleation Limited Switching model.

In Chapter 5, memory window analysis of the 64 kbits $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM were performed. A perfect yield and a large memory window were obtained at the capacitor area of 0.4 μm^2, revealing good uniformity of the film. Comparing the ΔV_{BL} with what predicted from single capacitor results in Chapter 2, similar ΔV_{BL} for data0 was obtained while smaller ΔV_{BL} for data1. This suggests that 1T1C FeRAM does not fully reproduce the ferroelectric properties obtained in a single capacitor described in Chapter 2. The cause of this difference is considered to be the amount of oxygen vacancy in the film due to the quality of interfacial layer of the bottom electrode, the presence of a passivisation film, the thermal history of the BEOL process, and mechanical stress caused by MFM device structure and orientation of domain, etc, and further analysis is required in the future study. The variability of ΔV_{BL} due to ferroelectric and dielectric components were calculated, resulting in the variation due to the ferroelectric is almost equivalent to that of dielectric. This result indicates that there are large amount of grains in the HZO film and variability of switching of domains is not dominant factor. To investigate

the feasibility of a memory window that accounts for the capacitance distribution of the MFM, Monte Carlo simulations was applied for the experimental results to estimate a memory window in Mbits at the 40 nm CMOS technology node. As a result, more than 140 mV of memory window can be achieved by MFM area between 0.11 to 0.14 μm^2.

In Chapter 6, the dependence of reliability on the $Hf_{0.5}Zr_{0.5}O_2$ thickness was investigated to improve the cycling tolerance of hard breakdown and reduce an operating voltage using 1T1C FeRAM for the first time. Furthermore, fatigue and its recovery of the 1T1C FeRAM memory were investigated to confirm the uniformity under practical memory array operation. Fundamental study for ferroelectric and dielectric properties between 5, 8 and 10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ were investigated using large single capacitor, indicating that 8 nm thick sample had the largest remanent polarization and higher break down voltage with low leakage in the samples. Memory array performance of the 64 kbits 1T1C FeRAM with 8 nm thick $Hf_{0.5}Zr_{0.5}O_2$ was confirmed that array operation at 2.0 V and 16 ns were demonstrated experimentally, which was lower than 10 nm thick HZO. The capacitance change during low-voltage operation was investigated comparing single capacitor evaluation and 1T1C FeRAM, resulting in larger capacitance change was obtained by single capacitor.This indicates that the capacitance definition based on the Equation 5.4 is not realistic for near-subloop operation, and correct capacitance estimation requires estimation by further transient analysis, such as measuring the frequency and duty dependence of capacitance.

Cycling tolerance of hard breakdown of the 1T1C FeRAM memory array revealed no bit error count during 10^8 cycles at an accelerated operating voltage of 3.5 V and an operating speed of 100 ns. The 1 ppm raw bit error rate at 2.0 V with 100 ns, and 85°C operation was predicted to be $>10^{15}$ cycles, based on the dependence of time to breakdown on the applied voltage.

Fatigue and recovery operations of the 1T1C FeRAM memory array were investigated for the first time. The memory window of median value was decreased post 2.0 V with 100 ns for 10^8 cycles, but recovered by applying higher stress at 2.8 V with 100 ns for 10^8 cycles. During fatigue and recovery phases, no degradation of the

ΔV_{BL} distributions was obtained, indicating that charge trapping and domain depinning in HZO was uniformly occurred. The mechanism of the recovery effect was investigated by polarization vs voltage measurement on single large MFM capacitor. As a result, in the recovery period, positively charged oxygen vacancies were neutralized by applying higher stress voltage, resulting in domain depinning followed by redistributed oxygen vacancies forming new switching domains, phase change or reorientation of domains (in-plane to out-of-plane) which are similar to wake-up mechanism. A higher recovery ratio was obtained at a higher recovery voltage or longer pulse width in contrast to the stress condition of the fatigue phase, and the recovery voltage can be reduced by applying longer recovery pulse widths.

Table 7.1 shows a table comparing this technology with target which was defined at Chapter 1. The target of writing voltage was achieved by the film thickness scaling technology without degradation of the write speed. Furthermore, cycling tolerance due to hard breakdown (HBD) was predicted to be more than $>10^{15}$ cycles by precise prediction using memory array operation. However, considering fatigue, the cycling endurance is only 10^8 cycles, which needs to be improved. Recovery schemes are a possible solution to this problem, but they require extra circuit and complicated sequences of operation, which may limit applications. Considering the 2Pr degradation due to fatigue, a more realistic solution would be to increase the 2Pr in advance by increasing capacitance area or improving the MFM fabrication process, such as initial thermal quenching[80] or stacking laminated ferroelectric layers[81] and so on. In terms of a retention, this thesis didn't cover a retention result using 1T1C FeRAM array, and further investigation is required to discover the performance. Finally, based on a capacitor area dependence on the memory window, it can be said that 40 nm is barely practical, considering a reduction of parasitic capacitance of bitlines.

In conclusion, this technology with planer-type capacitor under bitline structured 1T1C FeRAM can be a candidates for edge IoT application for advance technology node. and should encourage the mass production of $Hf_{0.5}Zr_{0.5}O_2$-based

1T1C FeRAM, which has been at the research level until now. For further miniaturization, a different approach is needed and will be discussed in the next chapter.

Table 7.1. Comparison table with this technology.

	SRAM	eDRAM	perovskite-based FeRAM	$Hf_{0.5}Zr_{0.5}O_2$-based FeFET [24]	$Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM [29]	Target	This thesis
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes
Write voltage	> 0.5 V	> 1.0 V	1.0 V	4.2 V	4.0 V	~ 2.0 V	2.0 V
Write speed	< 1 ns	~ 20 ns	20 ns	20 ns	100 ns	~ 10 ns	~ 10 ns
Endurance	10^{16}	10^{16}	10^{15}	$\sim 10^5$	10^{11} (b)	$\sim 10^{15}$	$\sim 10^{15}$ (b) for HBD $\sim 10^8$ for Fatigue
Retention	Volatile	Volatile	125°C 10 years	no data	125°C 10^4 sec	85°C 100 min	85°C > 100 min (a)
Scalability	5/7 nm	28 nm	180 nm	28 nm	no data	$=<$ 40 nm	40 nm (b)

(a) Result using a single capacitor
(b) prediction

7.2 Future technologies and directions

This thesis has revealed that a planer-type capacitor under bitline structured 1T1C FeRAM can be a candidates for edge IoT application as long as 40 nm technology node. To achieve 1T1C FeRAM with more advanced technology node, a different approach is needed to obtain a large memory window and low-voltage operation. In this section, feasibility study for more advanced technology node are conducted.

7.2.1 Three dimensional cylinder capacitor

Figure 7.1 describes a relationship between technology node and cell size. Blue line is corresponding to a proximal line of SRAM which was extracted from literature. The memory cell area is decreasing with an advances of the technology nodes. To show that FeRAM has an advantage over SRAM in terms of cell size, it is necessary to achieve smaller memory cells. Red lines shows describes a proximal line of 1T1C FeRAM with planer type metal/ferroelectric/metal(MFM) structure. The memory cell area was estimated based on a layout described in Figure 7.2, which refers to the layout of DRAM. As discussed in Section 5.3, an MFM area larger than 0.1 μm^2 is required to obtain sufficient read voltage for a sense amplifier. In the case of planer type MFM, even if the technology node advances and transistors become smaller, memory cell size is not able to be reduced due to the limitation of the size of MFM capacitor. According to this estimation, it is difficult to maintain an advantage over SRAM at technology nodes below 28 nm technology node. Green lines shows a proximal line of 1T1C FeRAM with three dimension (3D) cylinder, indicating that it is possible to break through the barrier of scaling limit.

To address the limitation of memory cell area, 3D cylinder MFM is required for enlarge a effective capacitance area without increasing memory cell area owing to the capability of atomic layer deposition for MFM materials[82,83]. In embedded memory, it is desirable to fabricate the 3D capacitor without changing the CMOS process or CMOS structure from the viewpoint of the fabrication cost. Figure 7.3 shows an schematic illustration of the 3D cylinder MFM for capacitor under bitline

(CUB) stricture and capacitor over bitline (COB) stricture. The advantage of the CUB allows 1T1C FeRAM to apply higher crystallization anneal for HZO as shown in Section 3.2 without degradation of a reliability of BEOL, but the effective area contributed from side area of the capacitor is limited by a height of front-end-of-line process when it is integrated to 3D cylinder MFM. On the other hand, COB structure has an advantage of earning the height of inter mediate layers in back-end-of-line (BEOL) process. The concern about the thermal budget on the BEOL lines could be overcome by reducing the crystallization anneal temperature using material engineering[84,85] or applying extremely fast (nano second order) annealing using laser anneal method to the capacitors[76].

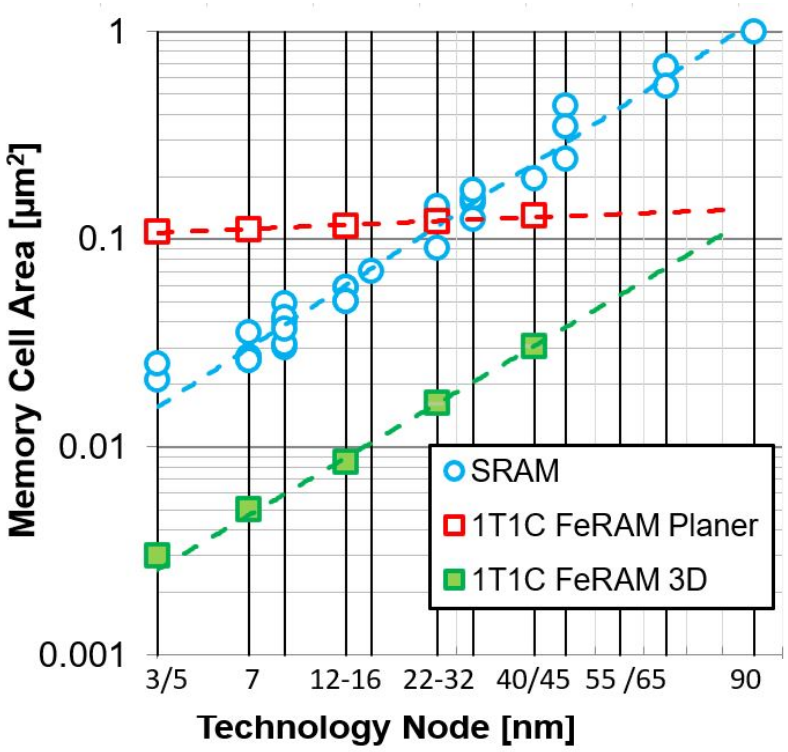


Figure 7.1. Relationship between technology node and cell size. Blue line describes a trend of SRAM. Red line describes a that of 1T1C FeRAM with planer type MFM structure and green line for 3D MFM structure.

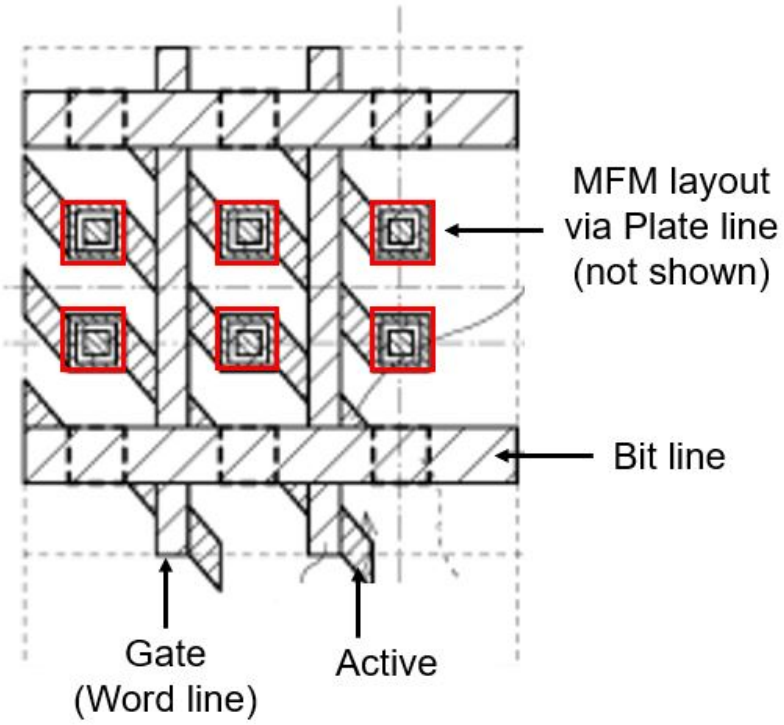


Figure 7.2. Concept of memory cell layout design of 1T1C FeRAM for a planer-type MFM structure.

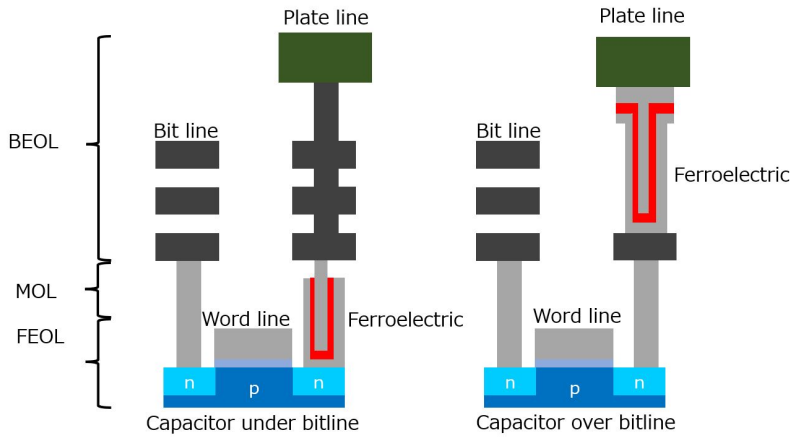


Figure 7.3. Schematic illustration of capacitor under bitline structure (left) and capacitor over bitline structure (right) for 3D cylinder MFM.

The memory cell size using COB structured 3D cylinder MFM was estimated for each technology node. Ideally, the memory cell size is independent on the the site area of the MFM cylinder, since the effective capacitance area is determined by the sidewall of the capacitor. However, it could be difficult to achieve the structure because the aspect ratio is too high or the capacitor diameter is too small to allow the MFM layers to be filled in. Therefore, the aspect ratio and the diameter of the 3D cylinder was estimated to ensure a total area of 1 μm^2 at each technology node and verified its feasibility.

The sidewall area was calculated by using schematic illustration in Figure 7.4. The Bottom electrode film thickness was assumed to be 3 nm, referring to the DRAM and FeRAM capacitor structures that have been commercialized and presented at academic conferences[86]. Same HZO thickness of 8 nm as this thesis was used for it. The capacitance area was calculated by following equation.

$$S = 2\pi hd \ln \frac{a}{b} + \pi a^2 \tag{7.1}$$

where S is an equivalent total area of the cylindrical capacitor including bottom area. Parameters of "a" and "b" in Equation 7.2.1 are defined as Figure 7.4 and calculated by using a parameter in Table 7.2. The diameter of the cylinder for the each technology node was assumed with reference to the design rule and contact diameter at each technology node. A parameter of "h" in Equation 7.2.1 is corresponding to the height of a cylinder and extracted by using Table 7.3. The height depends on how many intermediate layers in BEOL was contributed.

Figure 7.5 (a) shows a capacitor area dependence on cylinder diameter which was calculated using the Equation 7.2.1. The number of intermediate layers required to achieve a capacitance area of over 0.1 μm^2 depends on the technology node. One layer is sufficient for technology nodes later than 22 nm, but 14 nm requires two or more layers, tree layers for 7 nm technologies and more than 4 layers are required for more advanced than 5 nm technology node. Figure 7.5 (b) shows an aspect ratio dependence on the cylinder diameter. As the cylinder diameter decreases, the aspect ratio increases.

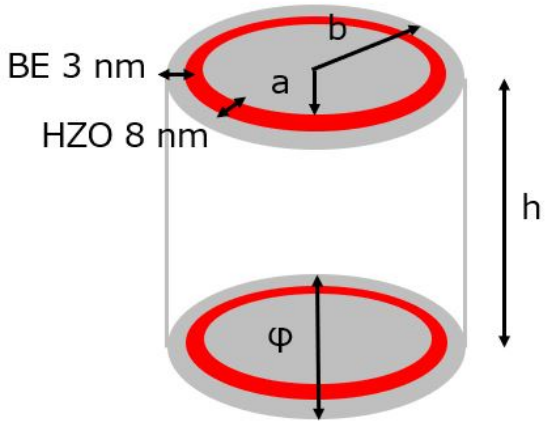


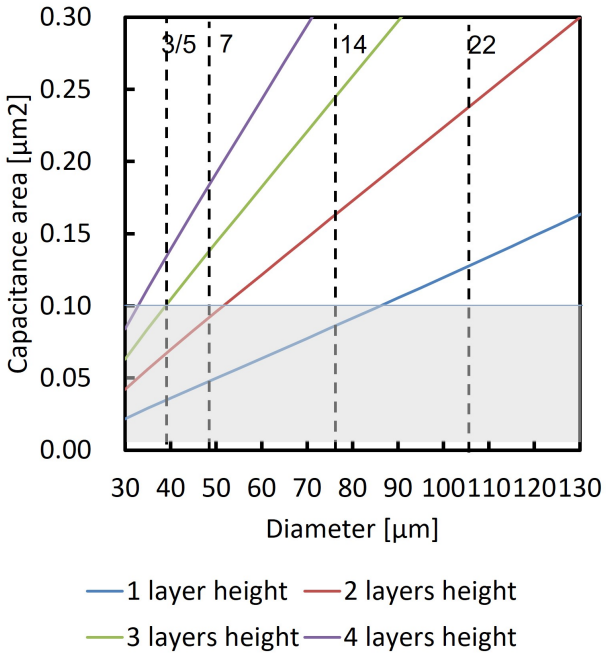
Figure 7.4. Schematic illustration of 3D cylinder MFM for the capacitance area calculation.

Table 7.2. Diameter of the cylinder for each technology nodes.

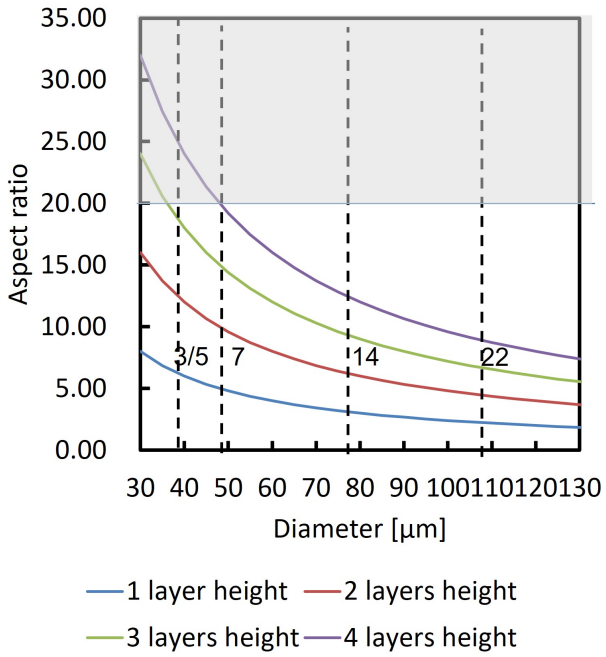
Technology node [nm]	40/45	28/22	16/14/12	7	5/3
Diameter [nm]	150	107	77	47	38

Table 7.3. Height of the cylinder for the numbers of metal layer.

Number of metal layer	1	2	3	4
Height [nm]	240	480	720	960



(a)



(b)

Figure 7.5. Capacitor area dependence on the cylinder diameter (a) and aspect ratio dependence on cylinder diameter (b).

As a result, Table 7.4 describes a summary of memory cell area and aspect ratio for each technology node. The memory cell cylinder can be integrated without impact on the memory cell, and the memory cell size can be calculated by only gate pitch and metal pitch. Therefore this result was plotted on Figure 7.4.

Table 7.4. Summary of memory cell area and aspect ratio for each technology node.

Technology node [nm]	Gate pitch [nm]	Metal [nm]	Cell area [μm^2]	Diameter [nm]	Inter mediate layers	Height [nm]	Capacitance area [μm^2]	Aspect ratio
40/45	162	126	0.0306	150	1	240	0.193	1.6
22/28	120	90	0.0162	107	2	480	0.250	4.5
12/14/16	90	70	0.0095	77	2	480	0.170	6.2
7	66	46	0.0046	47	3	720	0.134	15.3
3/5	56	40	0.0034	38	4	960	0.130	25.3

7.2.2 Anti-ferroelectric material

As discussed in Chapter 6, the operating voltage is predicted to be reduced by further film thickness scaling and 1.2 V operation was reported by using 4 nm thick HZO[72]. However, another approach is also required to achieve under 1.2 V operation voltage for cutting-edge-technology node. Some studies have demonstrated that anti-ferroelectric-typed (AFE) 1T1C FeRAMs have lower voltage operation than ferroelectric-typed (FE) 1T1C FeRAM[87,88]. Anti-ferroelectricity can be obtained by controlling the oxygen vacancies in the HZO film and including tetragonal phase in the $Hf_xZr_{1-x}O_2$ film[77]. If the top and bottom electrodes have the same material, the anti-ferroelectric does not show remanent polarization in the absence of an electric field as described in Figure 7.6 in blue. By applying built in bias through the capacitor with different work function between top and bottom electrodes, the P-E curve can be shifted and emerge an remanent polarization in red. The Operating voltage can be reduces in the amount of the voltage shift and better endurance can be obtained than FE-type 1T1C FeRAM. Compared to FE type 1T1C FeRAM, AFE type 1T1C FeRAM has half the remanent polarization and worse retention characteristics, but can be used for applications that do not require retention characteristics since its capability of low voltage operation.

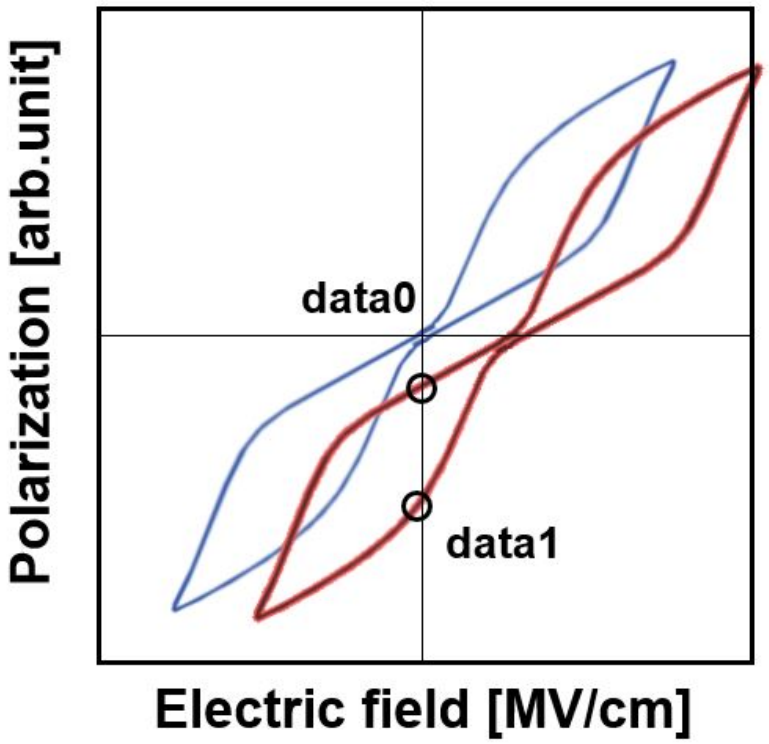


Figure 7.6. Schematic illustration of polarization vs. electrical field for anti-ferroelectric material with same work function electrodes among top and bottom electrodes in blue and different work function in red.

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Publications and Presentations

International Journals

(1) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Monica Materano, Tarek Ali, Kati Kuehnel, Konrad Seidel, Thomas Mikolajick, Uwe Schroeder, Masanori Tsukamoto and Taku Umebayashi, "1T1C FeRAM Memory Array Based on Ferroelectric HZO with Capacitor Under Bitline", *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 29–34, 2022.

(2) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Maximilian Lederer, Kati Kuehnel, Konrad Seidel, Thomas Mikolajick, Uwe Schroeder, Masanori Tsukamoto, and Taku Umebayashi, "Reliability Study of 1T1C FeRAM Arrays with $Hf_{0.5}Zr_{0.5}O_2$ Thickness Scaling", *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 778–783, 2022.

(3) Jun Okuno, Tsubasa Yonai, Takafumi Kunihiro, Kenta Konishi, Monica Materano, Tarek Ali, Maximilian Lederer, Konrad Seidel, Thomas Mikolajick, Uwe Schroeder, Masanori Tsukamoto and Taku Umebayashi, "Investigation of Recovery Phenomena in $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM", *IEEE Journal of the Electron Devices Society*, vol. 11, pp. 43–46, 2023.

Presentations

(1) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Hideki Maemura, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Kati Kuehnel, Konrad Seidel, Uwe Schroeder, Thomas Mikolajick, Masanori Tsukamoto and Taku Umebayashi, "SoC compatible 1T1C FeRAM memory array based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$", in *2020 IEEE Symposium on VLSI Technology*, IEEE, TF2-1, 2020.

(2) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Hideki Maemura, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Kati Kuehnel, Konrad Seidel, Uwe Schroeder, Thomas Mikolajick, Masanori Tsukamoto and Taku Umebayashi, "Demonstration of Fatigue and Recovery Phenomena in $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM Memory Arrays", in *25th Workshop on Electron Device Interface Technology*, JSAP, pp. 11 - 14, 2020, in Japanese, invited.

(3) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Hideki Maemura, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Kati Kuehnel, Konrad Seidel, Uwe Schroeder, Thomas Mikolajick, Masanori Tsukamoto and Taku Umebayashi, "SoC compatible 1T1C FeRAM memory array based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ report on 2020 IEEE VLSI symposia", in *The Institute of Electronics, Information and Communication Engineers*, vol. 120, no. 126, SDM2020-1, pp. 1-1, 2021, in Japanese, invited.

(4) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Hideki Maemura, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Maximilian Lederer, Kati Kuehnel, Konrad Seidel, Uwe Schroeder, Thomas Mikolajick, Masanori Tsukamoto and Taku Umebayashi, "High-endurance and low-voltage opera- tion of 1T1C FeRAM arrays for nonvolatile memory application", in *2021 IEEE International Memory Workshop (IMW)*, IEEE, pp. 29–31, 2021, invited.

(5) Jun Okuno, Takafumi Kunihiro, Kenta Konishi, Hideki Maemura, Yusuke Shuto, Fumitaka Sugaya, Monica Materano, Tarek Ali, Maximilian Lederer, Kati Kuehnel, Konrad Seidel, Uwe Schroeder, Thomas Mikolajick, Masanori Tsukamoto and Taku Umebayashi, "Demonstration of 1T1C FeRAM arrays for nonvolatile memory applications", in *2021 20th International Workshop on Junction Technology (IWJT)*, IEEE, S1-1, 2021, Honorable Invited Speaker Award.

(6) Jun Okuno, Tsubasa Yonai, Takafumi Kunihiro, Kenta Konishi, Monica Materano, Tarek Ali, Maximilian Lederer, Konrad Seidel, Thomas Mikolajick, Uwe Schroeder, Masanori Tsukamoto and Taku Umebayashi, "Demonstration of Fatigue and Recovery Phenomena in $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C

FeRAM memory arrays", in *2022 6th IEEE Electron Devices Technology and Manufacturing Conference (EDTM)*, IEEE, 2B-ME1-1, 2022, invited.