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Doctoral dissertation

Study on 0.18 μm SiGe BiCMOS having compatibility with standard CMOS process and SiGe HBT with high frequency characteristics over 250 GHz

(標準 CMOS プロセスとの整合性と高周波特性 250GHz 越の SiGe HBT を有する 0.18μm SiGe BiCMOS の研究)

March 2023

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1. Background and Purpose of This Study

1.1 Applications and Technical Challenges of BiCMOS and Bipolar Transistor Technologies

1.1.1 Application of Bipolar Transistor / BiCMOS Technology to Mainframe Computers

ENIAC, developed in 1946 at the University of Pennsylvania, was the first computer to support today's information society. The utilization of the large equipment using 17,468 vacuum tubes (floor area=100 m^2, weight= 30 tons, power consumption=150 kW) was limited to ballistic calculations for military applications [1]. On the other hand, the transistor was invented to replace the vacuum tube at about the same time. The amplification effect of the point contact bipolar transistor was confirmed in December 1947 by William Bradford Shockley, John Barden, Walter House Brattain, etc., of Bell Laboratory. Robert Noyce of Fairchild and Jack St. Clair Kilby of Texas Instruments conceived the idea of integrated circuits using transistors in 1958-1959, and Intel started to manufacture 4-bit i-4004 processors for electronic desktop calculators using the 10 μm PMOS process in March 1971 [2]. Intel, Motorola, and Zilog subsequently developed 8-bit microprocessors and began full-fledged development of computers using semiconductor technologies. Initially, the scale of integrated circuits was limited, and the application was also limited to desktop calculators. However, as the scale of integrated circuits grew, the development of large-scale general-purpose computers (mainframes) became famous for batch processing like

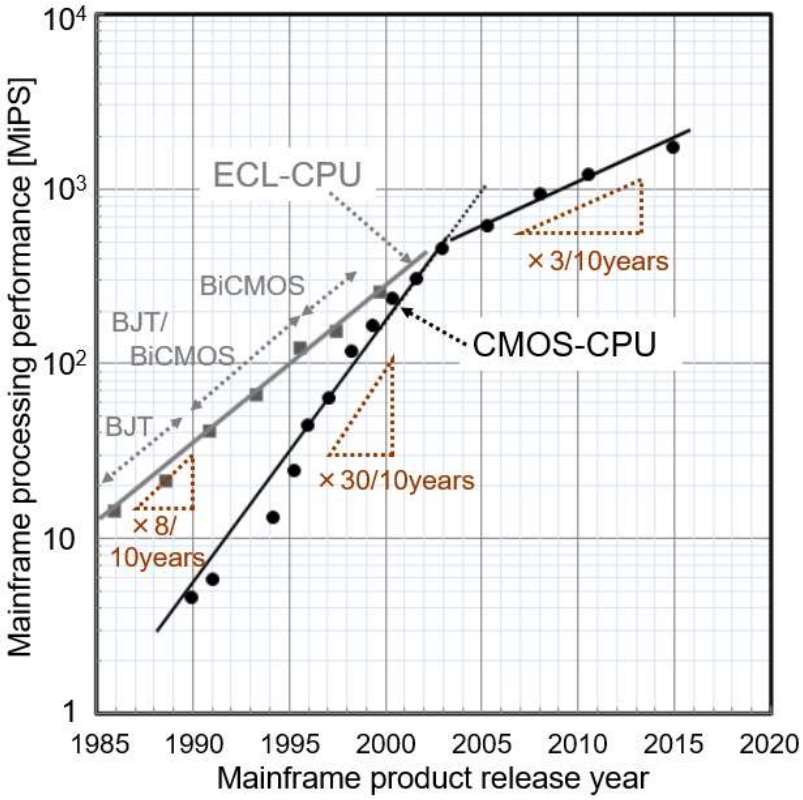


Fig. 1.1. Comparison of trends in the processing speed of mainframe computers by devices that made the CPU up.

accounting and inventory calculations and large-scale online processing systems like banks and train seat reservations. The technologies developed for these mainframe applications were applied to servers and personal computers. In 1985, the CPU consisting mainly of Si-based bipolar junction transistors (hereafter referred to as bipolar transistors) performed only about 20 MIPS alone. However, the performance of the CPU for the IBM mainframe (zEnterprise 196) that was developed in 2010 using the latest CMOS process at that time was 1,200 MIPS alone, and 52,000 MIPS (floor area=3 m^2, weight=1.5 tons, power consumption=27.5 kW) in parallel with 80 units. The supercomputer "Fugaku" that was in whole operation in 2021 at RIKEN (Institute of Physical and Chemical Research) has a CPU of 52 cores per node and parallelized 158,976 nodes. Its weight is about 1.6 t × 432 chassis, and its power consumption is 28.3 MW; it makes it a vast system in performance and scale.

In the case of an ECL circuit (Emitter Coupled Logic) using bipolar transistors, the through current flows in both the ON and OFF states. In the case of a CMOS circuit, the through current flows only when switching between ON and OFF states, resulting in a power consumption difference of more than two orders of magnitude. For this reason, CMOS was initially used in electronic desktop calculators that pursued portability because low power consumption was more critical than circuit performance. On the other hand, the mainframe capable of thoroughly preventing heat generation continued to improve the performance of bipolar transistors for adopting an ECL circuit faster than CMOS [4]. In addition, to control the increase in power consumption per chip as the scale of ECL circuits become more extensive and more integrated, the BiCMOS (Bipolar CMOS) technology was developed in the 1980s to enable the equipping of ECL circuits and CMOS circuits on the same chip. Using this technology, the ECL-CPU that appeared in 1991 was fitted with a chip that combined the secondary cache of CMOS memory and the logic of the ECL circuit. The processing capacity of ECL-CPU was improved 10-fold in 10 years by increasing the speed of ECL circuits and increasing the integration with BiCMOS technology (Fig. 1.1). However, the power consumption of the ECL-CPU chip introduced in 1999 reached 600 W even though more than half of the logic was made up of CMOS circuits. The power consumption of the ECL-CPU in the next generation was estimated to be around 2 kW, and it was judged that further high integration should reach the limitation of the cooling function. ECL-CPU was an aggregate of multiple chips due to the degree of gate integration and power consumption limitations. On the other hand, the CMOS-CPU has multiplied cores on a single chip to reduce processing delays due to transactions between chips to improve system performance. Although there was an 8-fold difference in processing performance in 1990, the performance of the CMOS-CPU was enhanced by 30-fold in 10 years, enabling it to catch up with the performance of the ECL-CPU in 2001. Since then, only the CMOS CPU has been used in the mainframes.

1.1.2 Challenges Relating to BiCMOS Technology Applied to the Communications Fields

On the other hand, with the widespread use of the Internet and smartphones in corporate work and daily life, there have been demands for constructing communication infrastructure systems for higher-speed and large-capacity data transmission. Because communication infrastructure systems must operate at high speeds and over a wide range of areas, LSIs must be compatible with performance, cost, and reliability [5]. In addition, digital processing circuits for converting analog and digital signals have become large-scale for supporting communication systems, and low power consumption is also required for LSIs for communications. For this reason,

BiCMOS technologies have continued to be used in the communication fields. For example, at the 40 Gbps optical transceiver, the ECL was responsible for the 43 Gbps high-speed signal processing, and the CMOS was accountable for the 2.7 Gbps middle-speed processing, reducing power consumption (Fig. 1.2, [6]). The scale of the CMOS circuit was 250 times that of the ECL circuit, but the power consumption was half. The advantage of the BiCMOS technology against compound semiconductors is that high integrated circuits can be achieved by equipping the CMOS circuits with low power consumption on the same chip.

Even if a BiCMOS process with bipolar transistors and CMOS on the same chip was developed, product design could not begin without a series of PDKs (Process Design Kits) for design. PDK consists of device parameters extracted from device characteristics, CMOS cell libraries, and various tools for automatically arranging CMOS

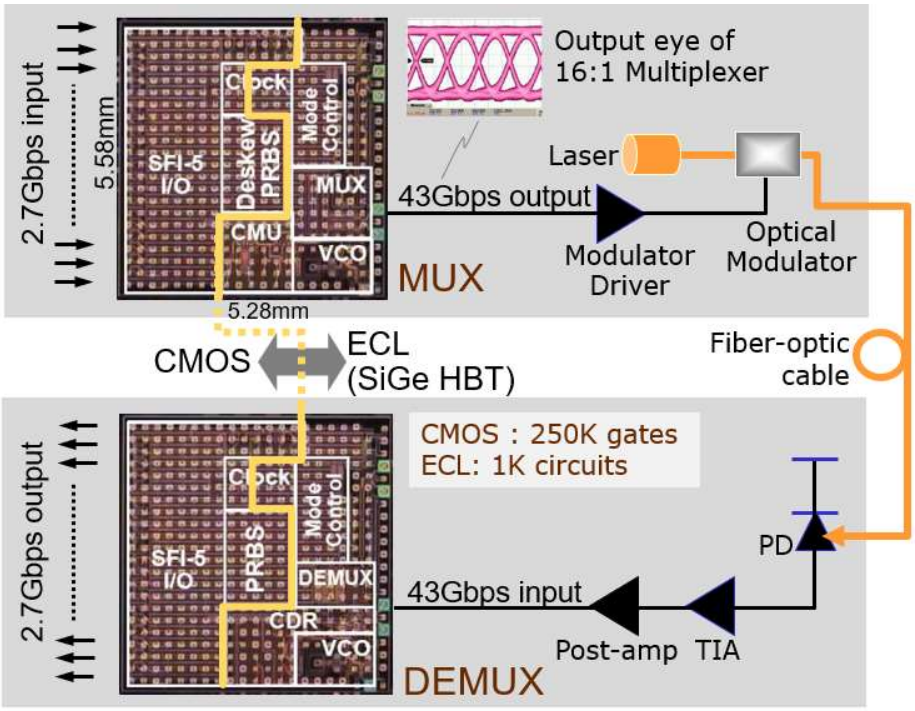
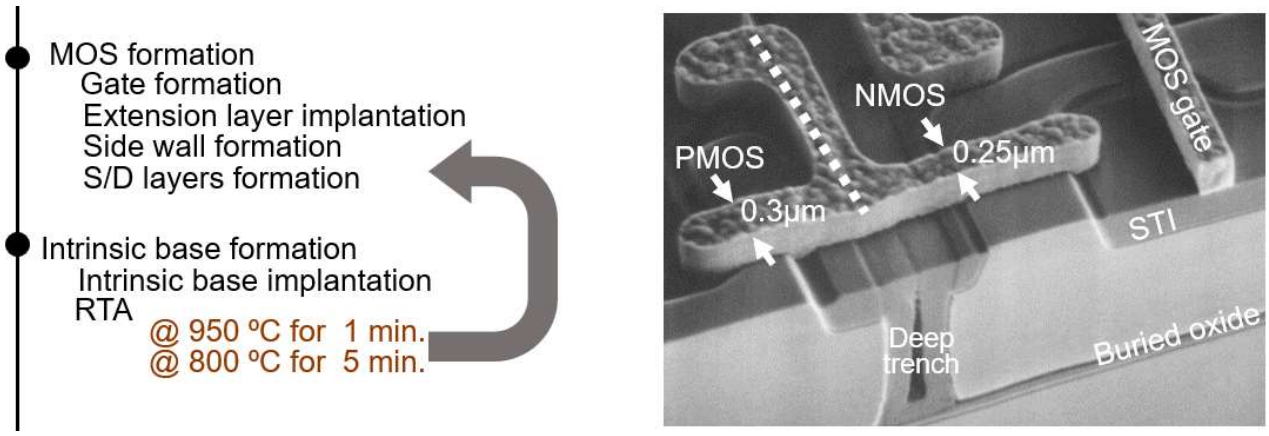


Fig. 1.2. Conceptual diagram of role-sharing between CMOS and SiGe HBT in LSI for optical communication [6].



(a) 0.25 μm Si BiCMOS process flow (b) Bird's-eye SEM photo-view of CMOS part in BiCMOS

Fig. 1.3. NMOS and PMOS equipped on the 0.25 μm Si BiCMOS [7].

cells. Since PDK requires confirmation of the cell operation, the development cost and effort shall be high. However, because LSIs for communications are small in volume and large in variety, it isn't easy to individually develop the PDKs that are expensive to produce, even if new devices are created exclusively for products. On the other hand, it was necessary to maintain a thin base layer to increase the frequency of the bipolar transistor, so the MOS formed up to the S/D (Source/Drain) region before forming the bipolar transistor in conventional BiCMOS processes (Fig. 1.3(a)). The short channel characteristics were maintained by making the PMOS gate length longer than the NMOS gate length due to the expansion of the MOS diffusion layer due to the thermal budget during the fabrication of the bipolar transistor (Fig. 1.3(b)) [7]. For this reason, conventional BiCMOS technologies could not achieve compatibility with standard CMOS and had to develop their PDK. Still, it was necessary to maintain compatibility with existing CMOS in the BiCMOS process to utilize the abundant design assets of standard CMOS.

1.1.3 Challenges Relating to Bipolar Transistors Applied to the Communications Fields

The three main applications for bipolar transistors/BiCMOS that were reported in academic conferences or technical papers have been optical communication [8]-[19], wireless communication [20]-[25], and in-vehicle radar [26]-[37]. There is a rough correlation between the operating frequency of each application and the cutoff frequency (f_T) of bipolar transistors, and the operating frequency has increased by about 2.6 times in five years (Fig. 1.4).

SONET (Synchronous Optical NETWORK), one of the global standards for optical transmission, has a transmission speed of 9.952 Gbit/s (OC-192), 39.8 Gb/s (OC-768), and 159.252 Gbps (OC3072). In addition, Ethernet, one of the global standards of LAN (Local Area Network), includes IEEE802.3ae (10GE: 10G Ethernet) and IEEE802.3z with a transmission speed of 1 Gbit/. In optical communications, the bipolar transistors with f_T

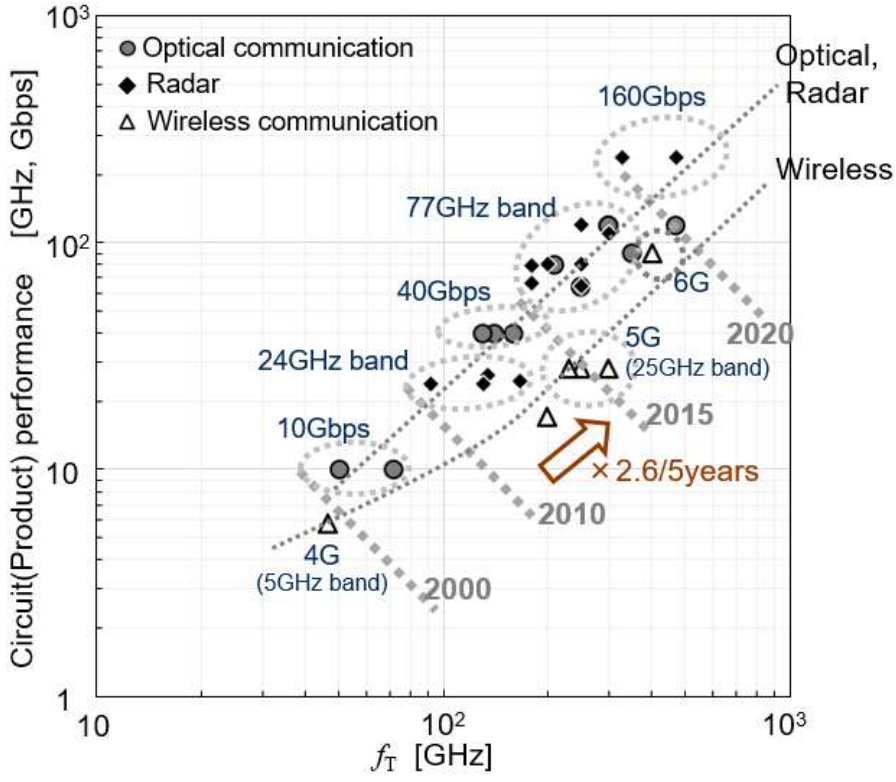


Fig. 1.4. Correlation between f_T of bipolar devices and circuit performance in applied products [5],[8]-[37].

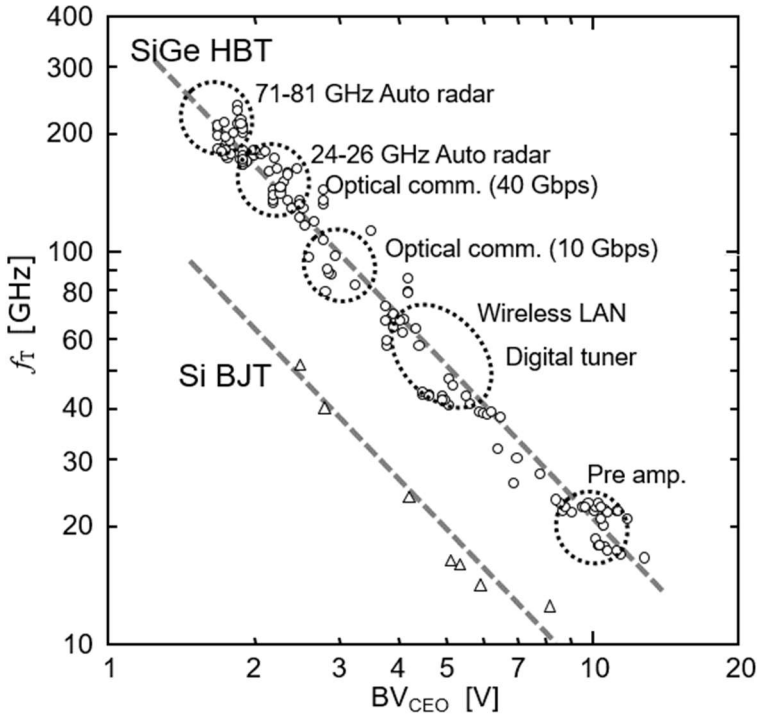


Fig. 1.5. Tradeoff relation between f_T and BV_{CEO} among SiGe HBTs and Si BJTs; both types were fabricated on Hitachi's 8-inch line. SiGe HBTs were manufactured in the 0.15-0.25 μm process, and Si BJTs were manufactured in the 0.25-0.35 μm process.

and f_{MAX} (Maximum oscillation frequency) of about 70 GHz were used to support communication speeds of 10 Gbps around the year 2000, and the bipolar transistors of about 140 GHz were used to support communication speeds of 40 Gbps. In 2015, communication technology exceeding 100 Gbps was announced with the advent of higher-frequency bipolar transistors. The bipolar transistor with f_T =300 GHz and f_{MAX} =350 GHz was used to research a communication rate of 120 Gbps, and it was estimated that the next generation OC-3072 with 160 Gbps requires f_T =500 GHz. In the wireless field, a product of 4G (5 GHz band) was reported for bipolar transistors with f_T and f_{MAX} of around 70 GHz around the year 2000, and the use of bipolar transistors with f_T of about 300 GHz resulted in 5G (25 GHz band) and 77 GHz band radar. In addition, around 2020, adopting bipolar transistors with f_T of 500 GHz or higher reported the possibility of 6G wireless communication and 120 Gbps optical communication [5]. In recent years, there has been an increasing need for the development of onboard radar that matches market prices in line with the trend toward commercializing automotive automated driving functions. Previously, announcements were centered on 24-26 GHz radars using bipolar transistors with f_T =130 GHz-160 GHz, but the emphasis has shifted to those of 77-79 GHz radars employing bipolar transistors with f_T =180 GHz-220 GHz.

The high frequencies of the bipolar transistors have increased following the high-speed operation of the application. However, the conventional Si BJT (Bipolar Junction Transistor) has a limit of f_T of 100 GHz. In the SiGe HBT (Heterojunction Bipolar Transistor) incorporated with Ge in the intrinsic base layer, the f_T of SiGe HBT has been approximately 2.5 times that of Si BJT compared with the same Collector-Emitter (CE) breakdown voltage (BV_{CEO}) (Fig. 1.5). With f_T and f_{MAX} exceeding 250 GHz, the SiGe HBT has been extended to the high-

frequency range of optical communication and radar that were previously realized with compound semiconductors. Furthermore, with BV_{CEO} higher at the same frequency, SiGe HBT has been applied to wireless communication and preamplifiers in HDD (Hard Disc Drive). However, because the production volume of semiconductor devices used in these markets has been limited, technology standardization has been an issue. In addition, the challenge was not the level of feasibility study described in the technical papers but the realization of bipolar transistors with f_T and f_{MAX} exceeding 250 GHz with the reliability of using them in the market.

1.1.4 Positioning of Bipolar Transistors in the Trend Toward Higher CMOS Speeds

On the other hand, the applications of CMOS, including SOI-CMOS, have been studied for high-frequency products, and the device performance of f_T=300 GHz and f_{MAX}=450 GHz at the 22 nm node was reported (Fig. 1.6). This performance is comparable to that of SiGe HBT using a 0.13 μm process. Studies on the combination of fine CMOS and high resistance SOI substrate have been presented, and fundamental studies [41] for the application of the 40 nm CMOS to 5G chips and the results of prototype and evaluation of 2.8 GHz PA (Power Amplifier) using the 45 nm CMOS [42] have been reported. By utilizing a high-resistance SOI having a resistivity of 1 to 10 kΩ•cm on the base substrate, the crosstalk noise propagation could be suppressed, and the Q value of the inductor equipped on the chip could be improved. Prototype and evaluation of 80-100 GHz bandpass filter using the 65 nm node [43], LNA (Low Noise Amplifier) using 0.13 μm node [44], and 5.8 GHz bandpass filter using 0.18 μm node [45] have been announced. Millimeter-wave circuits are expected to develop due to fine CMOS, such as the 22 nm node.

However, ArF liquid immersion scanner has been a prerequisite for fine CMOS of the 45 nm node or later, so the process cost shall be high. The 0.13 μm node CMOS that has used a KrF scanner has a relatively low process cost, but its device performance is limited to f_T=70 GHz and f_{MAX}=140 GHz. On the other hand, SiGe BiCMOS technology can achieve high-frequency characteristics comparable to advanced CMOS even with a 200-mmφ 0.18-μm process that is not the most advanced.

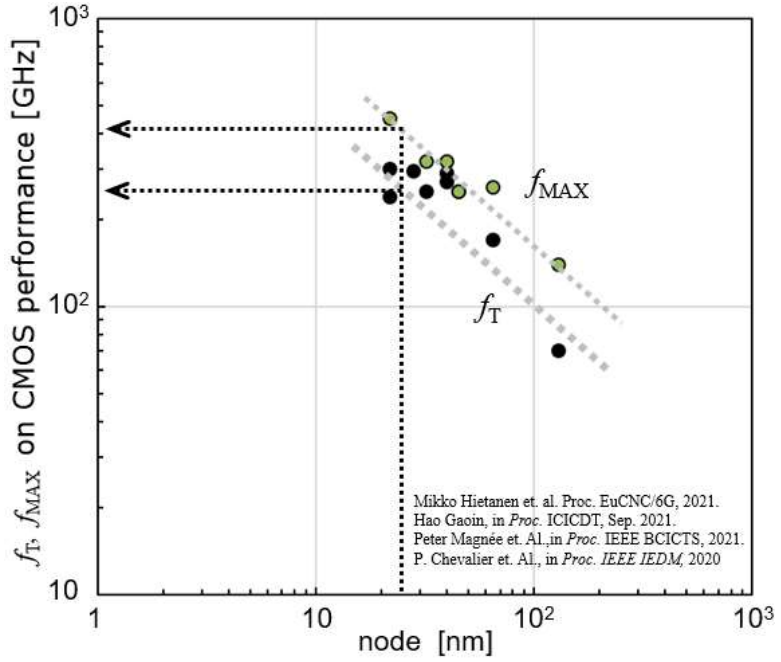


Fig. 1.6. Node dependence of high-frequency characteristics of CMOS devices [5],[38]-[40].

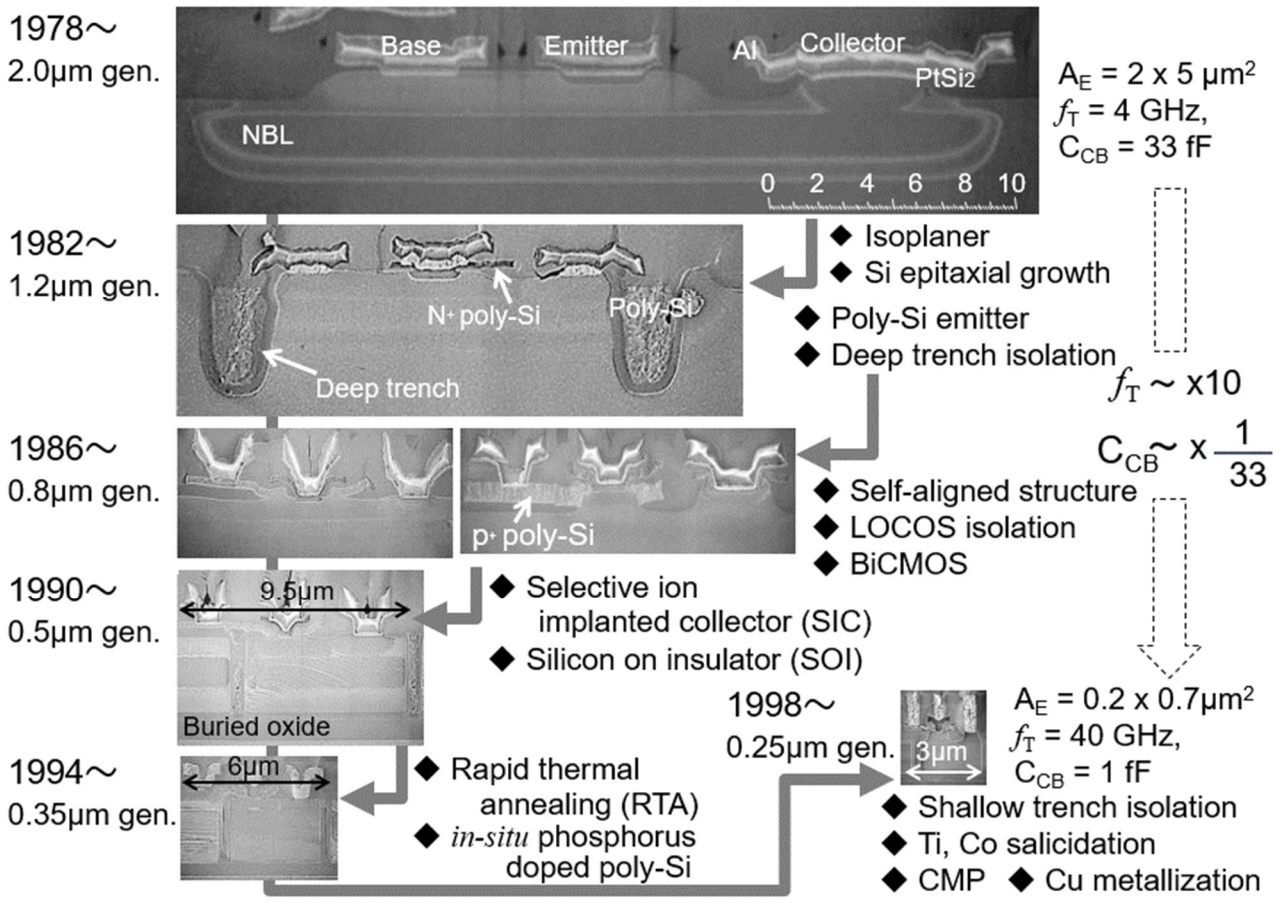


Fig. 1.7. SEM cross-sections of Si BJTs from 2.0 μm to 0.25 μm generation. Describe the main technology innovations of each generation [46].

1.2 Overview of Conventional Techniques for Increasing the Frequency of Bipolar Transistors

The following techniques realized the performance improvement of Si BJTs developed in the past for large general-purpose computers (Fig. 1.7).

(i) Improvement of f_T by thinner intrinsic base layers
... Low-acceleration ion implantation, RTA (Rapid Thermal Annealing), poly-Si emitter structure

(ii) Improvement of f_T by thinner and higher-impurity-concentration collector layers
... Profile optimization in the SIC (Selective ion Implanted Collector) region

(iii) Improvement of f_{MAX} by new device structure and narrow emitter width
... Double-polysilicon self-aligned structure, Fine lithography technology

(iv) Improvement of f_{MAX} by using the same fine technology as CMOS
... Fine lithography technology, STI(Shallow Trench Isolation), Silicide process, etc.

From 2.0 μm generation to 0.25 μm generation, the adoption of (i)-(iv) increased f_T tenfold and reduced collector-base parasitic capacitance (C_{CB}) to 1/33. The inverse of f_T can be indicated as Eq. (1.1), which is the sum of the emitter time constant (τ_E), the charge and discharge time in the collector-base parasitic capacity (τ_C), the transit time in the intrinsic base region (τ_B), and the transit time in the collector layer (τ_{CSCL}).

$$\frac{1}{2\pi f_{\mathrm{T}}} = \tau_{\mathrm{EC}} = \tau_E + \tau_C + \tau_B + \tau_{\mathrm{CSCL}} = \frac{kT}{qI_c} C_{EB} + \left(\frac{kT}{qI_c} + R_C + R_E\right) C_{CB} + \gamma \frac{{W_B}^2}{D_n} + \frac{W_{CSCL}}{2v_{SAT}} \quad (1.1)$$

I_C: Collector current

W_B: Intrinsic base thickness Dn: Electron diffusion coefficient

γ : Constant that depends on accelerating built-in field

W_{CSCL}: Collector depletion thickness v_{SAT}: Electron saturation speed

Thinning the intrinsic base layer could reduce the third term, τ_B. The fourth term, τ_{CSCL}, is the transit time of the collector layer of the low-impurity-concentration layer between the intrinsic base layer and the NBL (: N-type Buried Layer). τ_{CSCL} could be reduced by suppressing the Kirk effect (: push-out of the base layer in the high current region). The Kirk effect could be stopped by thinning the collector layer or increasing the concentration of impurities in the collector layer. τ_E in the first term and τ_C in the second term are the charge/discharge time of the emitter-to-base parasitic capacitance (C_{EB}) and the collector-to-base parasitic capacitance (C_{CB}). Significantly, the CR time constant of the second term is the product of C_{CB} and the sum of the collector resistance (R_C) and the emitter resistance (R_E). Therefore, reducing parasitic capacitance and parasitic resistance by a self-aligned structure and device shrink has been effective. Here, making the junction shallower and narrowing the depletion layer width increases the junction capacitance, so τ_C and τ_{CSCL} are in a conflicting relationship. As one solution, the SIC region has been formed by implanting impurities only right under the intrinsic base layer. The increase in C_{CB} due to increased impurity concentration was somewhat suppressed.

Conventional higher frequency techniques familiar to the SiGe HBT device design are summarized below.

(i) Thinner the intrinsic base layer

Thinning the intrinsic base layer effectively improves f_T because τ_B varies with the square of the intrinsic base layer width. To make the intrinsic base layer thinner, there has been a poly-Si emitter structure or combination of low-acceleration ion implantation (BF_2, single-digit keV) and RTA.

(i)-1. Thinning the intrinsic base layer by low-acceleration ion implantation

BF_2, rather than boron, has been used as ion species to implant impurities into the intrinsic base layer because boron is too light in weight and has a deeper boron profile due to channeling effects even at the low-acceleration energy implantation. In 0.35 μm generation, annealing after impurity implantation was switched from batch-type furnace annealing (FA) to single-wafer RTA. The RTA facilitated shallow junction by instantaneously recovering damage to the substrate during ion implantation and suppressing enhanced boron diffusion through defects. Furthermore, emitter diffusion into the substrate switched from the arsenic diffusion after ions were implanted into the non-doped poly-Si layer to the phosphorus diffusion from the *in-situ* phosphorus-doped poly-Si layer. This technique suppressed the thermal budget for annealing from 900 ℃ for 10 minutes to 875 ℃ for 10 seconds, and both the emitter layer and the intrinsic base layer became shallow.

Based on the above, the intrinsic base layer formed by boron ion implantation in the 0.5 μm generation was 100 nm thick and had a boron peak concentration of 4×10^{18} cm^{-3}, whereas that in the 0.25 μm generation was 50 nm thick and had a boron peak concentration of 3×10^{18} cm^{-3} (Fig. 1.8). Including the contribution of changing the collector conditions, f_T was improved from 18 GHz for the 0.5 μm BJT to 40 GHz for the 0.25 μm BJT. In addition, in the 0.25 μm BJT, f_T was increased from 47 GHz to 52 GHz by further reducing the acceleration of BF_2 ion

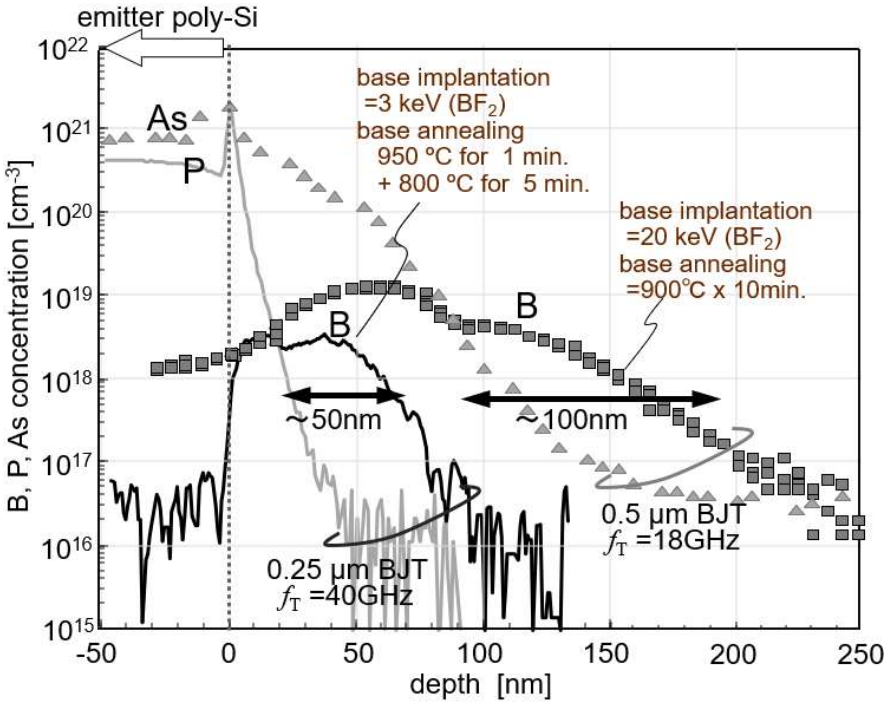


Fig. 1.8. Comparison of the emitter and base impurity profile on Si BJTs between generations.

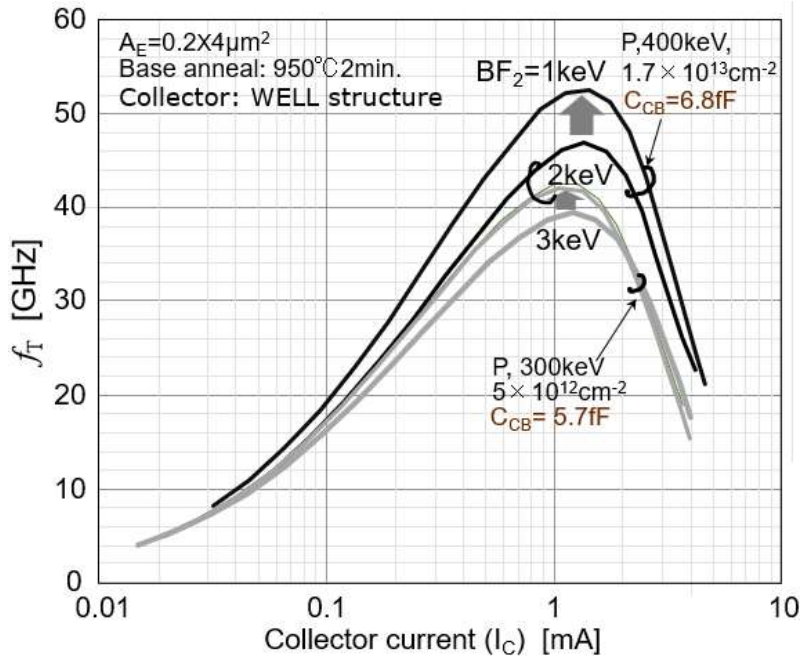


Fig. 1.9. Dependence of high-frequency characteristics of Si-BJTs on base layer formation conditions.

implantation under the same collector formation conditions (Fig. 1.9). However, because of thinning of the impurity diffusion layer by the combination of ion implantation and RTA was limited to 50 nm, it was aimed in this study to form a box-shaped boron profile by selective SiGe epitaxial (SEG: Selective Epitaxial Growth) technology to make the layer thinner.

(i)-2. Thinning the intrinsic base layer by the poly-Si structure

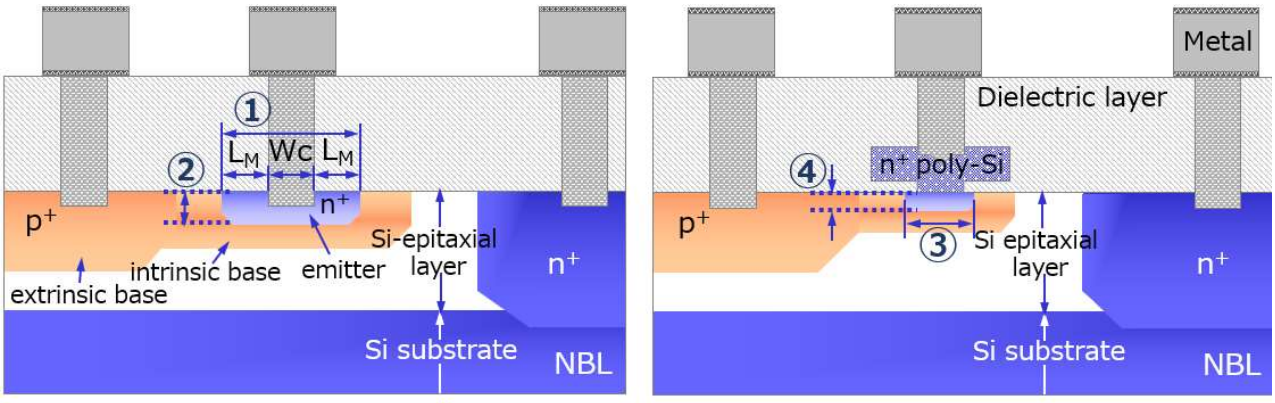
In the 2 μm generation, emitter and base diffusion layers were formed by implanting impurities directly into the

Si epitaxial growth layer formed on the NBL [46]-[50]. In this method, the emitter and base diffusion layers needed to be deep because the emitter diffusion layer was etched to some extent during contact hole formation (Fig. 1.10(a)). On the other hand, thinning the base layer was required to improve the performance of the bipolar transistor, as shown in equation (1.1), so the emitter layer also needed to be shallow. When the impurity ions were implanted deep in the Si substrate, considering that the surface of the substrate was etched during contact hole processing, the impurity profile became deeper, making it difficult to thin the base layer. Therefore, the poly-Si emitter structure that forms the emitter region by diffusion of impurities from the poly-Si layer doped with arsenic or phosphorus was adopted in the 1.3 μm generation (Fig. 1.10(b)). The emitter poly-Si layer functioned as an etching stopper during contact hole formation, so the emitter and base diffusion layers were shallow. In addition, the emitter width, determined by the sum of the minimum dimensions and matching accuracy for lithography, could be shrunk to the minimum dimensions for lithography.

Up to the 0.5 μm generation, the non-doped poly-Si layer was ion-implanted with arsenic to form the emitter electrode (Fig.1.8). However, the crowding effect where the impurity diffusion becomes uneven due to the influence of the embedded shape of the poly-Si layer in the emitter hole was an issue. *In-situ* phosphorus-doped poly-Si that does not require ion implantation has been applied to the emitter electrode since the 0.35μm generation. Furthermore, because the process temperature was lowered in the 0.25 μm generation, an *in-situ* boron-doped poly-Si was also applied to the base electrode.

(ii) Thinning the collector layer and increasing impurity concentration in the collector layer

When the collector current increases during the forward operation of the bipolar transistor, the Kirk effect becomes apparent so that intrinsic base thickness effectively thickens and f_T decreases. Concerning the collector layer between the NBL and the intrinsic base layer, increasing the concentration of impurities and thin layers can increase the electric field to suppress the Kirk effect and improve the f_T. However, the side effect remains as increasing the C_{CB}. Unlike the WELL type (Fig. 1.11(a) that increases the concentration of impurities on the entire area of the collector layer, the SIC type (Fig. 1.11(b) that only increases the concentration under the intrinsic base

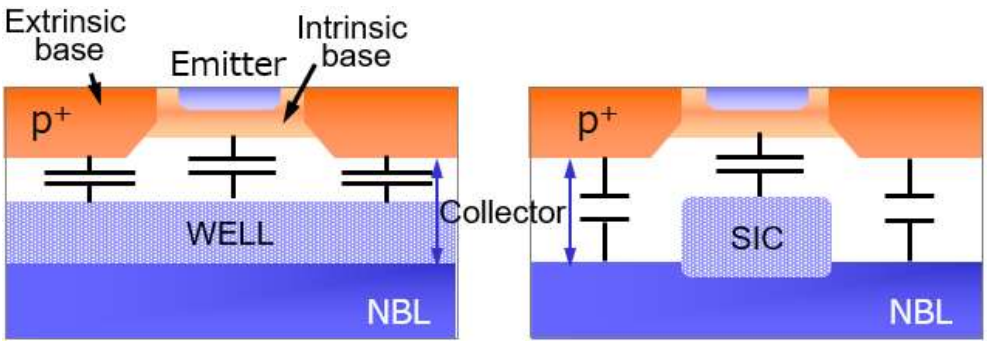


① Emitter width(We)=Metal contact width(Wc) + alignment margin (L_M)×2
② Deep diffusion layer formed by direct impurity implantation into a substrate

③ Emitter width(We)=Emitter contact width +impurities lateral diffusion distance ×2
④ Shallow diffusion layer formed by impurity diffusion from emitter poly-Si layer

(a) Conventional Transistor (2.0 μm generation) (b) Poly-Si Emitter Transistor (1.2 μm generation)

Fig. 1.10. Comparison of bipolar device structures with and without the emitter poly-Si layer.



(a) WELL-type collector doping (b) SIC-type colllector doping

Fig. 1.11. Differences in techniques for implanting impurities into the collector layer.

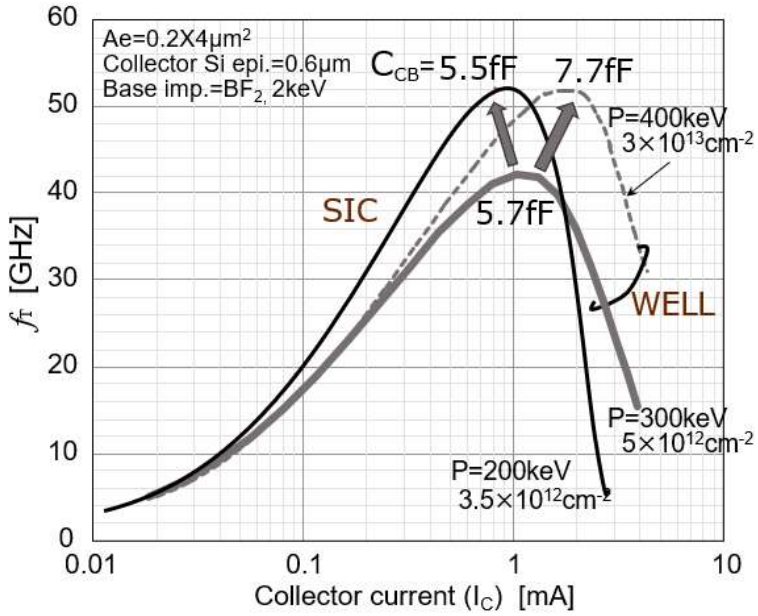


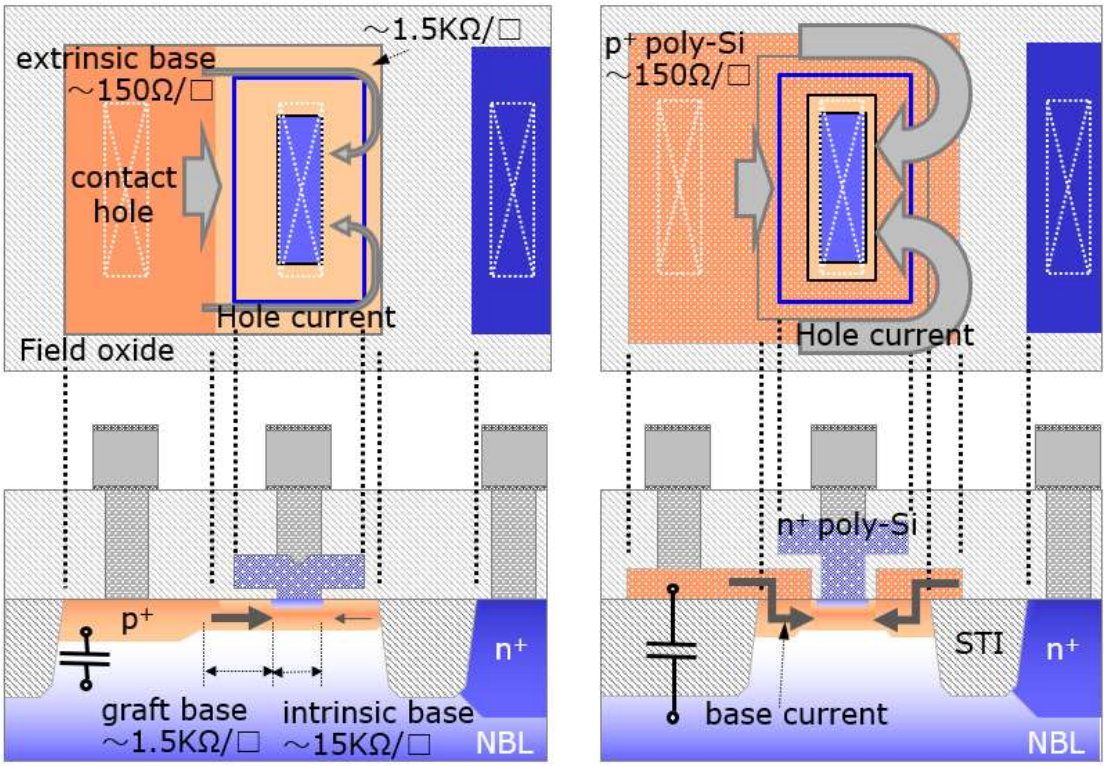
Fig. 1.12. Collector structure dependence of Si-BJT characteristics (intrinsic base layers formed by ion implantation and RTA).

layer is one of the measures to prevent the increase in C_{CB}. After the emitter hole is opened, the SIC region is formed by phosphorus ion implantation at an accelerating energy of 200-300 KeV. In the SIC type, C_{CB} increase could be suppressed by limiting the high impurity concentration region to just under the intrinsic base layer. For example, f_T was increased from 42 GHz to 52 GHz by changing the acceleration energy and dose of phosphorus ion implantation into the entire collector region from 300 keV, 5×10^{12} cm^{-2} to 400 keV, 3×10^{13} cm^{-2} (Fig. 1.12), C_{CB} increased 1.4 times. On the other hand, in the SIC type, the C_{CB} was reduced by 29 % from 7.7 fF to 5.5 fF while realizing the same f_T of 52 GHz under the conditions of 200 keV and 3.5×10^{12} cm^{-2}.

(iii) A double-polysilicon self-aligned structure

As an advanced one of the poly-Si emitter structure, a double-polysilicon structure in which the extrinsic base diffusion layer was switched to the poly-Si electrode in addition to the emitter layer appeared in the 0.8 μm generation (Fig. 1.7). Although the same p^+ diffusion layer as the PMOS S/D layer is used for the extrinsic base

region in the poly-Si emitter structure (Fig. 1.13(a)), the emitter is surrounded by the intrinsic base layer of a high sheet resistance of 1.5 kΩ/□. Therefore, the base current to the opposite side of the base contact hole is suppressed. On the other hand, at the double poly-Si emitter structure, the base resistance was lower than in the poly-Si emitter structure because the intrinsic base layer was surrounded by a poly-Si electrode of 150 Ω/□ (Fig. 1.13(b)). Also,



(a) Poly-Si emitter structure (b) Double poly-Si emitter structure

Fig. 1.13. Comparison of layout and cross-section of bipolar devices with poly-Si emitter electrode.

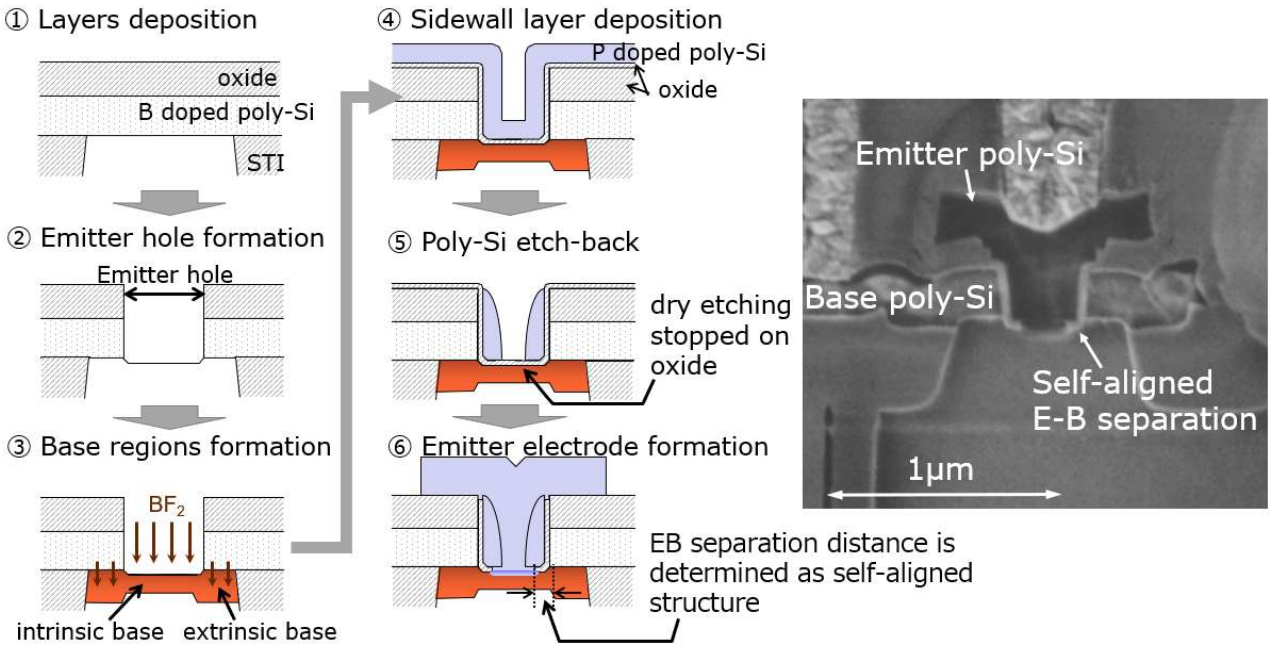
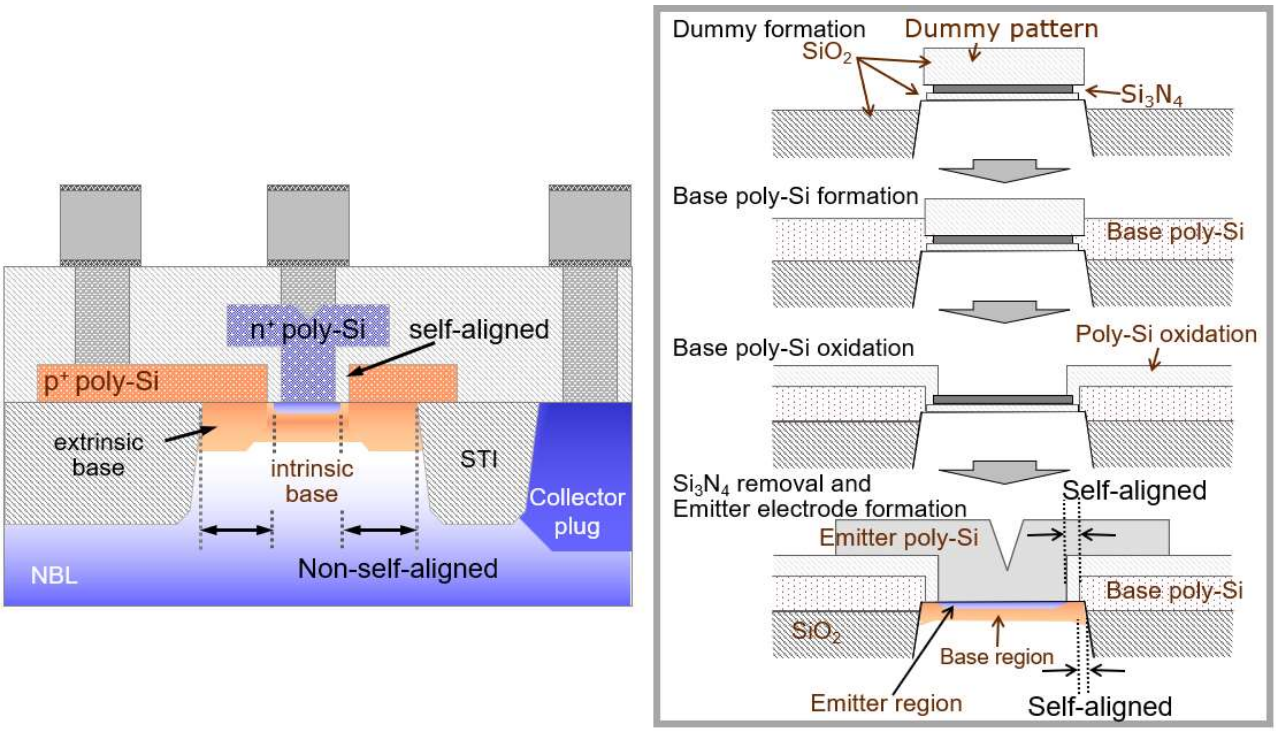


Fig. 1.14. The formation process of sidewall structure for the E-B (Emitter electrode – Base electrode) isolation in a typical self-aligned structure.

the base poly-Si layer was formed on the field oxide, thus reducing parasitic capacitance.

The self-aligned structure is a technique that determines the distance between patterns without relying on the alignment accuracy of lithography. For bipolar transistors, the self-aligned structure is employed for the emitter-base (E-B) electrode separation distance, thereby further reducing the base resistance (rbb') and C_{CB} [51]-[56]. Various structures other than those shown in Fig. 1.7 were developed. Still, the most utilized structure was the one in which a side wall layer consisting of a poly-Si layer and an oxide layer was formed in the emitter hole to separate the emitter and base (E-B) electrode layers (Fig. 1.14). Since the thickness of the sidewall layer determined the E-B electrode separation distance in a self-aligned manner, rbb' was reduced because the width of the connecting base region was reduced. In addition, the area around the emitter becomes narrower by decreasing the width of the connecting base, and the C_{CB} could be reduced. The initial structure was a side wall structure with only an oxide layer. Still, a certain amount of the intrinsic base diffusion layer was also etched by the dry etching process for forming the oxide layer sidewalls, which caused variations in the thickness of the intrinsic base layer. Therefore, a stacked structure of poly-Si and oxide layers was obtained.

Most of the self-aligned structures were only between the emitter region and base region and not up to the extrinsic base region (region of connection between the base poly-Si electrode and the Si substrate layer) were self-aligned (Fig. 1.15(a)). The SICOS structure studied at the Central Research Laboratory of Hitachi, Ltd. was self-aligned both between the emitter and base poly-Si electrode and between the base poly-Si electrode and filed oxide layer (Fig. 1.15(b)). First, a dummy pattern of the emitter layer was formed on the mask up to the field oxide layer and the base poly-Si electrode layer. The Si substrate connection of the extrinsic base electrode was determined by self-alignment. In addition, the E-B electrode separation region was also formed as a self-aligned structure by



(a) Most common self-aligned structure (b) SICOS (Side Wall Contact Structure) process flow

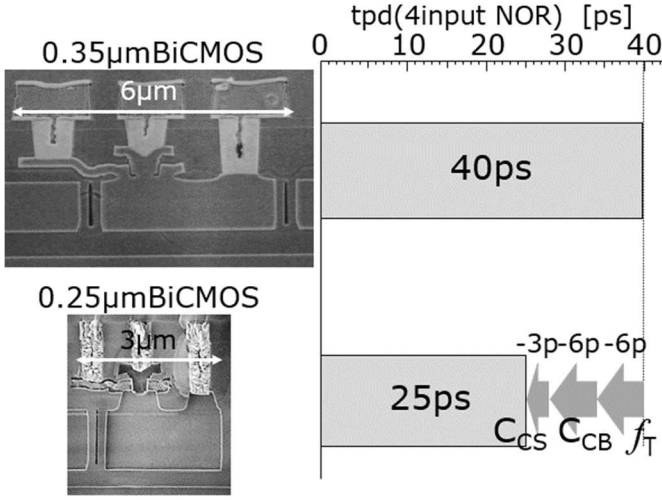
Fig.1.15. Comparison between widely adopted self-aligned and SICOS structures, including process flow [57].

thermally oxidizing the upper layer and sidewalls of the extrinsic base electrode. There were many process steps in a complex structure, and there was no continuous application of this structure.

(iv) Fine process technology

Up to the 2.0 μm generations, the separation between devices was achieved by a combination of LOCOS: LOCal Oxidation of Silicon) and channel stoppers by impurity ion implantation. However, the reduction of the separation width was limited due to the lateral spread of the diffusion layer. After the 1.2 μm generation, the device-to-device distance was shortened by forming trenches deeper than the N^+ buried layer. Furthermore, in the 0.25 μm generation, technologies such as STI (Shallow Trench Isolation) and silicide newly developed by CMOS technologies were also incorporated in BiCMOS, thereby facilitating the reduction of the parasitic capacitance and resistance of bipolar transistors [58]. The isolation region was shrunk by applying the STI because there was no lateral broadening of the oxidation region by the bird's beak at the LOCOS structure. The device shrinkage in the fine process may cause an increase in parasitic resistance because of the decrease in the width of the current path. However, the increase in parasitic resistance was suppressed by the Ti salicide technology in the 0.25μm generation and by the Co salicide technology in the 0.18μm generation. As the fine process technologies progressed from the 2.0 μm generation to the 0.25 μm generation for Si BJTs (Fig. 1.7), the substrate parasitic capacitance (C_{CS}) was reduced to 1/50, and the collector-base parasitic capacitance (C_{CB}) was reduced from 33 fF to 1 fF. In addition, the f_T was increased from 4 GHz to 40 GHz with increasing the collector current density, and the emitter area was reduced from 2×5 μm^2 to 0.2×1 μm^2 to suppress various parasitic parameters. As a result, the ECL gate delay time (tpd) was reduced from 250 ps/gate for the 2.0 μm generation to 25 ps/gate for the 0.25 μm generation [55][58]. In addition, the delay time of the 4-input NOR circuit was shortened from 40 ps/gate for the 0.3 μm generation to 25 ps/gate for the 0.25 μm generation (Fig. 1.16)[58]. According to the sensitivity analysis of various device parameters by circuit simulation, the f_T improvement (from 25 to 40 GHz) contributed 6 ps of the 15 ps reduction. On the other hand, the total contribution of parasitic capacitance due to the fine process was 9 ps.

Other research and development institutes like IBM stopped applying BJTs to mainframe computers at the 0.5



Comparison of device characteristics

BiC [μm]	Ae [μm²]	f_T [GHz]	rbb' [Ω]	C_{CB} [fF]	C_{EB} [fF]	C_{CS} [fF]
0.35	0.3 x 1.0	25	310	2.2	3.2	3.5
0.25	0.2 x 0.7	40	360	1.0	2.1	1.5
ratio	0.47	0.63*	1.16	0.46	0.65	0.43

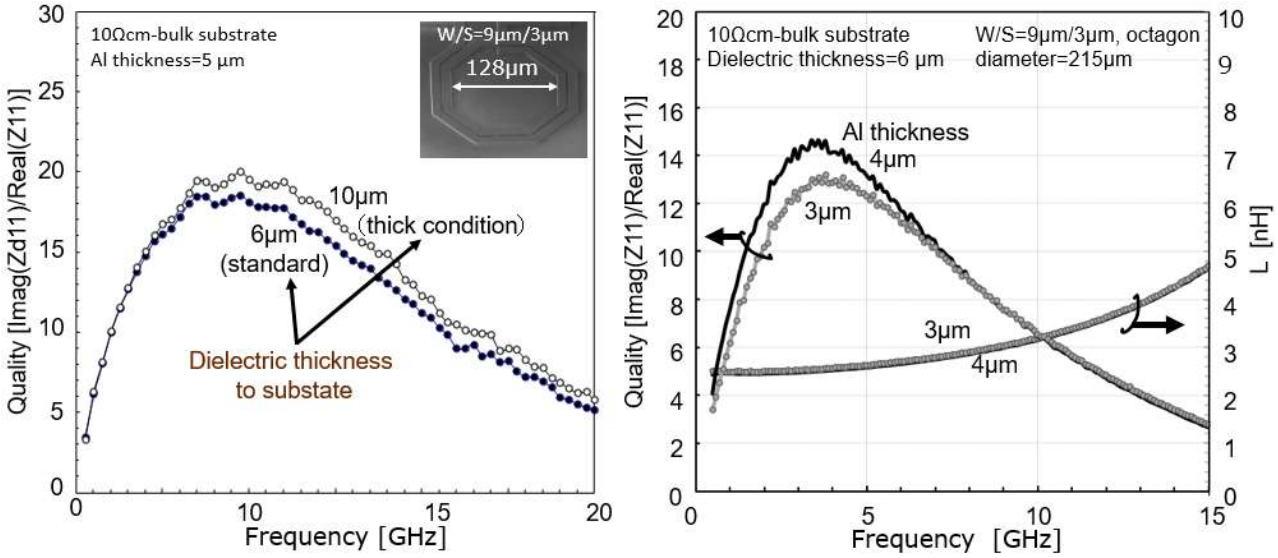
* Ratio after time conversion ($t=1/2\pi f_T$)
A_E : Emitter area size
C_{EB}: Parasitic capacitance between Emitter and Base
C_{CB}: Parasitic capacitance between Collector and Base
C_{CS}: Parasitic capacitance between Collector and substrate

Fig. 1.16. Circuit delay time (tpd) comparison between generations [56].

μm generation, temporarily halting the shrinking BJT development. On the other hand, this study continued to use the BJTs for the mainframe computers and to advance the shrinking BJT. It was also thought essential for the SiGe HBT to maintain superiority in the shrinking structure of the device.

1.3 Usefulness and Issues of Application of Thick-Layer SOI to BiCMOS for Analog Products

In communication LSIs, realizing discrete devices around the chip in the metallization layers on the chip has contributed to product cost reduction and product performance improvement by reducing the area of the entire system (Module). Therefore, improving the performance of on-chip passive devices such as capacitors (MIM: Metal Insulator Metal) and inductors in the front-end process has also been a significant challenge. In the on-chip implementation of passive devices, the parasitic resistance and the parasitic capacitance with substrates



(a) Dependence on dielectric layer thickness (b) Dependence on Al thickness

Fig. 1.17. Dependence of inductor Q value on metallization layer specifications.

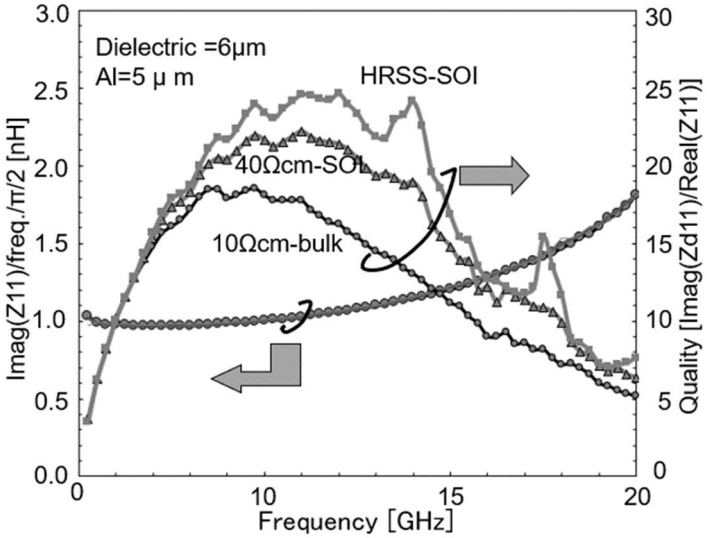
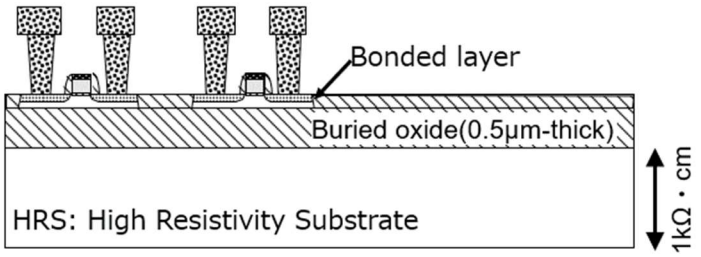
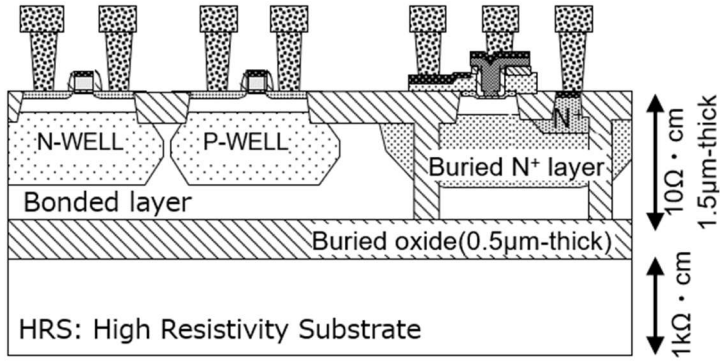


Fig.1.18. Dependence of on-chip inductor characteristics on Si substrate specification.

(Line/Space＝9/3 μm、Inner diameter=128 μm, 2 turns, octagonal shape)



(a) CMOS using a thin-layer SOI wafer



(b) BiCMOS using a thick-layer SOI wafer

Fig. 1.19. Cross-sectional comparison of CMOS using a thin-layer-SOI and BiCMOS using a thick-layer SOI.

significantly affect the operating frequency of analog circuits. Therefore, both the MIM and the inductor are formed the upper metallization layer. For example, because the thickness of the first to third layers of the wiring is only about 0.5 μm due to the wiring constituting logic circuits in the 0.18 μm SiGe BiCMOS, the series resistance is high, and a sufficient Q value of the inductor cannot be obtained. Therefore, an inductor was formed in the top layer which can maximize the thickness of the Al layer up to 3-5 μm thick. However, although the Q value was improved by the thickening of the interlayer dielectric layer and the thickening of the Al layer (Fig. 1.17), a significant improvement in characteristics is not expected even with changes to the wiring layout rule due to the extreme process conditions.

The Q value of the inductor could be significantly improved by changing the resistivity of the substrate (Fig. 1.18), but changing the resistivity of the substrate in a bulk wafer involves a significant change in CMOS IP (Intellectual Property) to change the device characteristics. On the other hand, the resistivity of the bonded Si layer on an SOI (Silicon On Insulator) substrate forming the devices remains unchanged, so the influence on CMOS IP can be minimized. However, the use of thick-layer SOI for high-speed applications was limited. BiCMOS had been used to prevent soft errors by α-rays when using LSIs for mainframe computers [52]-[54][56][58], and there were no published technical papers on crosstalk noise propagation in thick-layer SOI. In addition, in the thin-layer SOI, since a bonded layer thickness is 0.1 μm or less and the STI of the field oxide reaches the buried oxide layer, crosstalk noise propagates only to the base substrate side because only the bonded layer remains in the limited area for MOS formation (Fig. 1.19(a)). However, since the thick-layer SOI has a bonded layer of 1.5 μm, crosstalk noise that could be an issue in analog products propagates on both the base substrate and bonded layer sides (Fig. 1.19(b)). Therefore, it was necessary to clarify the effects of substrate resistivity and structure on the thick-layer SOI on crosstalk noise propagation.

1.4 Purposes of This Study

(1) Purposes of this Study

The purposes of this study are as follows.

Because Si BJTs were prioritized in the process construction in conventional Si BiCMOS, CMOS device characteristics and design rules should have been changed. It was necessary to develop a new PDK for each product. However, reconstruction of individual PDK and IP was challenging for small-lot, wide-variety communication products in terms of development costs and product development time. It was aimed in this study to utilize existing CMOS IP by establishing the SiGe BiCMOS technology that maintained consistency with the standard CMOS. It was attempted to reduce the thermal budget of the SiGe HBT formation process and optimize the device height to this end. In addition, it aimed to realize a SiGe HBT with high-frequency characteristics while shifting from a BJT-centered design rule to a CMOS-centered design rule and building a high-performance BiCMOS that conformed to standard CMOS.

In addition, because Si BJTs have the highest value of f_T at around 100 GHz, they could not be used in fields such as 5G, 40 Gbps optical communication, and radar. Since a significant factor was that a thickness of about 50 nm of the intrinsic base layer was the limit for conventional impurity ion implantation, the purpose of this study was to further improve the f_T by the SiGe epitaxial growth technology. This technology formed the thin intrinsic base layer and Ge profile generating the accelerated electric field. Furthermore, it was aimed to improve f_{MAX} by realizing a self-aligned structure even in the SiGe HBT by forming the SiGe selective epitaxial growth, and f_T and f_{MAX} of 250 GHz or more could achieve with minimal changes in device structure and layout. This study aimed to realize these aims as a mass production technology.

Another purpose of this study was to clarify the substrate structure dependence of the frequency characteristics of crosstalk noise propagation in thick-layer SOI substrates. Thick-layer SOI has the advantage that the resistivity of the bonded layer in which the devices are performed remains at 10 Ω·cm, so even if the base substrate has a high resistivity, there is little effect on IP. However, no technical paper has been published on crosstalk noise propagation in the thick-layer SOI substrate, including the bonded layer. This study aimed to clarify the guidelines for reducing crosstalk noise propagation by combining deep trenches isolating SiGe HBTs with the thick-layer SOI substrates.

(2) Overview of this paper

In this study, the CMOS devices from the 0.13-0.18 μm node could be integrated into the SiGe BiCMOS process without deteriorating the short channel characteristics by constructing the MOS priority process, and high-frequency characteristics of the SiGe HBT was achieved by forming the 2-nm-or-less SiGeC layer and reducing various parasitic resistances/capacitances. The low-thermal-budget process to maintain the short channel characteristics was realized by adopting single-wafer processes and the HCl-free selective SiGe epitaxial growth process. Furthermore, it was clarified that the moisture desorption from the CVD oxide layer was a particular issue for lowering the H_2 annealing temperature before SiGe epitaxial growth. A countermeasure was taken by changing to an HDP (High-Density Plasma) layer with less moisture desorption. 254 GHz of f_T and 325 GHz of f_{MAX} were achieved by shrinking the emitter size to 0.12×1.0 μm^2 with a p-SiGeC layer thickness of 2 nm. In addition, it was clarified the frequency characteristics of crosstalk noise propagation in thick-layer SOI which has been limited to

BiCMOS for high-frequency applications.

Chapter 2 describes a SiGe BiCMOS process with 0.13 μm to 0.18 μm CMOS. The thermal budget of the entire bipolar transistor formation process was suppressed by switching the heat-loading process from a batch process to a single-wafer process, and the temperature of the H_2 annealing before the selective epitaxial growth was lowered by adopting an oxide layer that emits less moisture. This allowed the CMOS device to be incorporated into the BiCMOS process without degrading the short-channel characteristics and affecting the SiGe HBT characteristics and yield. Although this technology was studied and developed based on the 0.18 μm node, it could be incorporated into BiCMOS up to the 0.13 μm node without deteriorating the short channel characteristics, demonstrating the scalability of the process.

Chapter 3 describes the selective SiGe epitaxial growth technology for forming the intrinsic base layer. The structure covering the base poly-Si electrode with an oxide layer enabled the selective SiGe epitaxial growth without adding HCl gas, and the temperature of the epitaxial growth process was lowered. In addition, it was found that the concentration of boron and Ge in the SiGe layer depended on the area of the growing region, and the monitoring pattern of the concentration of boron and Ge was fixed for accurate monitoring. The boron concentration was finally increased to 4.5×10^{20} cm^{-3}, the Ge concentration was increased to 30 %, and it was evaluated that 0.1-0.2 % carbon doping could suppress boron diffusion.

Chapter 4 describes that the SiGe HBT technology developed has suppressed parasitic capacitance and parasitic resistance through a self-aligned structure using the selective SiGe epitaxial growth technology. The step-type Ge profile with a high Ge concentration in the i-SiGe layer just under the p-SiGeC layer was able to improve f_T, and f_T of 200GHz has been achieved by thinning the intrinsic base layer and collector layer. In addition, the collector resistance was reduced by removing the intermediate STI between the collector plug and the intrinsic base region, and the f_T was improved from 226 GHz to 254 GHz. Furthermore, f_T = 307 GHz and f_{MAX} = 180 GHz were realized with a p-SiGeC layer thickness of 1 nm by reducing the collector time constant by narrowing the area of the connecting base region for reducing the collector-base parasitic capacitance (C_{CB}). In addition, the collector-base parasitic capacitance and base resistance were suppressed by narrowing the emitter width to 0.12 μm, and f_{MAX} =325 GHz was realized at f_T =254 GHz with the p-SiGeC layer thickness of 2 nm.

Chapter 5 describes that the deep trench pattern used for device isolation between SiGe HBTs should be considered as a means of suppressing crosstalk noise propagation in thick-layer SOI, depending on the resistivity of the base substrate. In particular, it was more effective to multiplex the deep trench pattern when the base substrate was a high-resistance substrate.

Chapter 6 describes that future issues for SiGe HBTs include the necessity of countermeasures against the increase in emitter resistance that accompanies the narrow emitter necessary for further performance improvement. One issue is the residue of the side wall oxide layer removed around the emitter. The other is the interfacial oxide layer between the emitter poly-Si electrode and the Si substrate. An epitaxial emitter structure was proposed to remove the interface native oxide layer between the emitter poly-Si electrode and the Si substrate surface. It obtained the same characteristics as the poly-Si emitter structure.

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2. BiCMOS Maintaining Compatibility with Standard CMOS Processes

2.1 Introduction

Because the power supply voltage of CMOS and f_T of SiGe HBT required by the application are different, the SiGe BiCMOS process of a combination of CMOS and SiGe HBT has been newly developed for each new significant product development. On the other hand, it has been necessary to prepare device parameters for circuit simulation, the description of the vertical structure of wiring, and design verification rules for layout design as the PDKs for circuit designers for each process. In addition, Intellectual Property (IP) for product design, such as CMOS standard logic cells and standard input/output circuits, has been prepared in parallel with device process development. Therefore, when the device parameters of CMOS change in a new BiCMOS process, it is necessary to develop a new IP, including re-characterization in the CMOS standard logic cell, leading to an increase in development cost and development time. In addition, the diversification of CMOS circuits along with the fine process has increased the number of preparation steps for IP for design. BiCMOS process designs that do not change from the device parameters and design rules in the original CMOS process have become crucial for these reasons.

Although there have been technical papers emphasizing compatibility with standard CMOS technology when developing new SiGe BiCMOS technology [1][2][3], the process methodology to ensure compatibility has yet to be detailed. When the temperature in the bipolar formation process is lowered not to affect the MOS characteristics, the challenges are not to degrade the performance of the bipolar transistor from that of the bipolar single process and not to affect the yield and reliability of devices.

2.2 The 0.18 μm SiGe BiCMOS Process in This Study

2.2.1 Challenges in the 0.18 μm SiGe BiCMOS Process Technology

In this study, in addition to developing a SiGe BiCMOS process that simultaneously equipped SiGe HBT and 0.18 μm node CMOS, the purpose was to confirm that there was a scalability that could also be applied to the 0.15 μm node and 0.13 μm node [4][5]. This study addressed the following challenges associated with fine CMOS processes.

(i) Maintaining the gate pitch of the standard CMOS in the BiCMOS process

Although the gate pitch of BiCMOS was more expansive than that of the standard CMOS of the same generation up to the 0.25 μm node that was the conventional BiCMOS technology, the gate pitch in this study became the same as that of the CMOS of the same generation. The issue was that the interlayer dielectric became thinner as the contact pitch became shorter following the fine process development progressed. The height of the SiGe HBT with a two-layer poly-Si emitter structure had to be brought closer to the height of the MOS gate with a single-layer poly-Si structure. In addition, there was concern that the SiGe HBT device size

would increase and affect the SiGe HBT characteristics by changing the layout rule that prioritized bipolar transistors to prioritize MOS.

(ii) Higher temperature and shorter final RTA as progressing the CMOS fine process

(Study contents will be described in Chapter 4)

The temperature of the final RTA was raised as the CMOS generation progressed to reduce the sheet resistance of the heavily doped S/D regions, and the RTA time was shortened to suppress impurity diffusion (Table 2.1). In the case of the 0.18 μm generation, raising the temperature from 875 ℃ to 1000 ℃ increased the impurities' activation rate and reduced the diffusion layer's resistivity. To these results, the S/D current (I_{DS}) increased by 4.5 % for NMOS and 15.6 % for PMOS (Fig. 2.1). However, raising the temperature of the final RTA in the BiCMOS process raised concerns about a decrease in Emitter-Base (EB) breakdown voltage (BV_{EBO}) due to enhanced diffusion of high-concentration phosphorus from the emitter poly-Si electrode and a reduction in f_T due to boron diffusion in the intrinsic base layer.

Table 2.1. Comparison of final annealing conditions by generation

node	Final RTA condition
0.25 μm	875 ℃, 10 sec.
0.18 μm	950 ℃, 3 sec.
0.13 μm	1000 ℃, 1 sec.
90 nm	1050 ℃, < 1 sec.

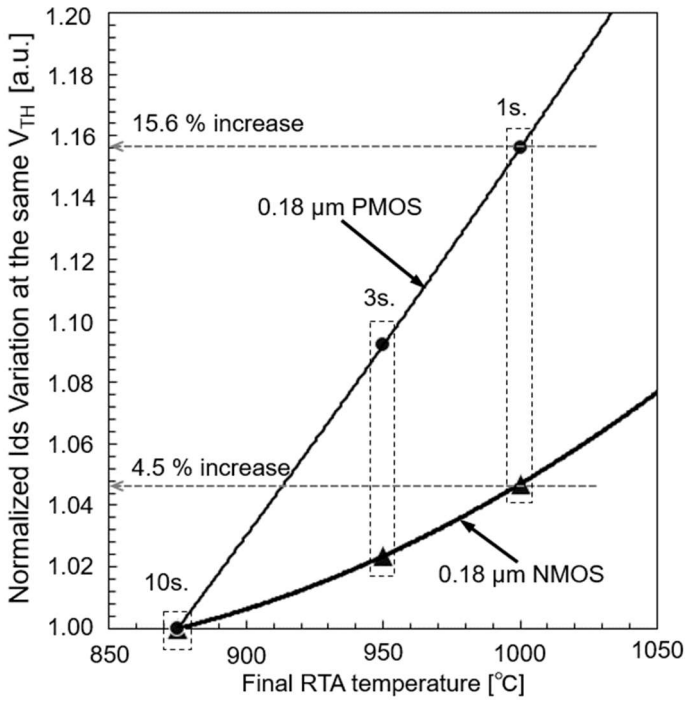


Fig. 2.1. Final RTA temperature dependence on I_{DS} of 0.18 μm MOS. An increase in I_{DS} was plotted from the value at 875 ºC. Annealing time was adjusted so that each condition's thermal budget was the same. I_{DS} values were normalized to that at the same V_{TH} for different annealing temperatures [14].

(iii) Low-temperature H_2 annealing before the SiGe epitaxial growth to prevent boron penetration from the p-type gate

PMOS up to the 0.25 μm generation has used n-type gates that induce a buried channel structure with a depleted channel. However, the p-type gates have been applied to the surface channel PMOS from the 0.18 μm generation to improve the short-channel characteristics. Therefore, suppression of boron penetration from the p-type gate through the thin gate oxide layer became an issue. The first countermeasure was a reduction of the thermal budget in the HBT formation process to maintain the short channel characteristics. On the other hand, it was also known that H_2 annealing to remove carbon and oxygen from the substrate surface before the SiGe epitaxial growth could promote boron diffusion [6]. It had been initially considered that there would be no influence on the MOS gate because a 50-nm-thick nitride layer and a 125-nm-thick oxide layer were covering the MOS gate. Still, the influence was so significant that it was necessary to take measures against enhanced boron diffusion by the H_2 annealing.

Regarding this issue, it was necessary to consider maintaining hydrogen termination to suppress natural oxide layer growth on the Si substrate. Si dangling bonds on the substrate surface are terminated by hydrogen atoms during dilute hydrofluoric acid wet cleaning, temporarily suppressing the formation of a natural oxide layer. Stable hydrogen termination is essential for lowering the temperature of the H_2 annealing. It became necessary to clarify the stable hydrogen termination formation conditions before SiGe epitaxial growth.

(iv) Minimize the thermal budget of SiGe HBT formation to prevent degradation of the CMOS short channel characteristics

Maintaining the short channel characteristics has become challenging in the CMOS fine process, so the Halo structure has been adopted from the 0.18 μm CMOS. Therefore, the conditions to suppress the thermal budget for forming SiGe HBTs to maintain the short channel characteristics of CMOS have been becoming stricter along with the CMOS fine process. It was investigated that the reduction of thermal budget to form SiGe HBTs so as not to affect the short channel characteristics of CMOS in this study.

In the 0.18 μm SiGe BiCMOS technology for being applied to the 43 Gbps optical communication semiconductor chip, the drain currents of NMOS and PMOS were increased to 660 μA/μm and 295 μA/μm respectively by lowering V_{TH} to handle 2.7-Gbps signal in CMOS circuits [5]. Further fine CMOS is needed for high-speed signal processing, and it is necessary to confirm the scalability that this technology, which was researched and developed based on the 0.18 μm node, could be applied to the 0.13 μm and 0.15 μm nodes.

2.2.2 Overview of the 0.18 μm SiGe BiCMOS Process Technology Developed in This Study

Even in conventional Si BiCMOS technology, there are two points for developing a new BiCMOS process: "Optimization of the order of processes considering the thermal budget in each process" and "Influence on processing accuracy due to level difference caused by devices structure." Therefore, the process flow has been designed to prevent interference between process modules. In the 0.18 μm SiGe BiCMOS process developed in this study, the bipolar transistor formation process was divided into three blocks and inserted at the optimal location in the standard CMOS process (Figs. 2.2, 2.3) [4]. This was the same for the 0.13 μm and 0.15 μm SiGe BiCMOS, which will be described later.

(1) NBL(N$^+$ Buried Layer) formation (Figs. 2.2(1), 2.3(1))

The heavy thermal processing steps for fabricating an N^+ buried layer (NBL), a collector Si epitaxial growth layer, collector plugs to an N^+ buried collector, and deep trenches were performed first. After processing the shallow trenches and forming a 30 nm thick pad oxide layer at 1000ºC, an HDP oxide layer was deposited, and the STI was formed flattening by CMP (Chemical Mechanical Polishing). Directional ions shall damage the Si layer during the deposition of the HDP layer using plasma technology, but the pad thermal oxide layer absorbed the damage to the Si layer surface caused by the plasma.

(2) Collector plug/deep trench formation (Figs. 2.2(2), 2.3(2))

The Collector plug layer, which was the region to connect with the NBL layer, was then formed by phosphorus ion implantation at an accelerating energy of 80 keV (dose=5×10^{15} cm^{-2}) and annealing at 950 ºC. The intermediate STI (in Fig. 2.2) was formed between a collector plug and an intrinsic base layer to thicken the oxide layer just below the extrinsic base poly-Si layer, thereby reducing the C_{CB}. In addition, since the lateral diffusion of the collector plug was blocked by the intermediate STI, a high Collector-Base () breakdown voltage (BV_{CBO}) was maintained even when the collector Si-epitaxial growth layer was thick.

After that, 0.4-μm-wide deep trenches were processed by dry etching in the Si substrate. The LP-CVD (Low Pressure-Chemical Vapor Deposition) embedded the oxide layer in the deep trench at 800 ºC after forming a 4-nm-thick thermal oxide layer on the sidewall at 750 ºC. Both oxide layers in the STI and the deep trench were heat treated at 950 ºC for 30 minutes to enhance oxide layer quality and prevent flatness deterioration due to wet etching for cleaning a substrate surface. The deep trenches were formed before MOS gate forming, although these were not related to MOS device operation, so the deep trenches, as well as STI, shall be planarized so as not to interfere

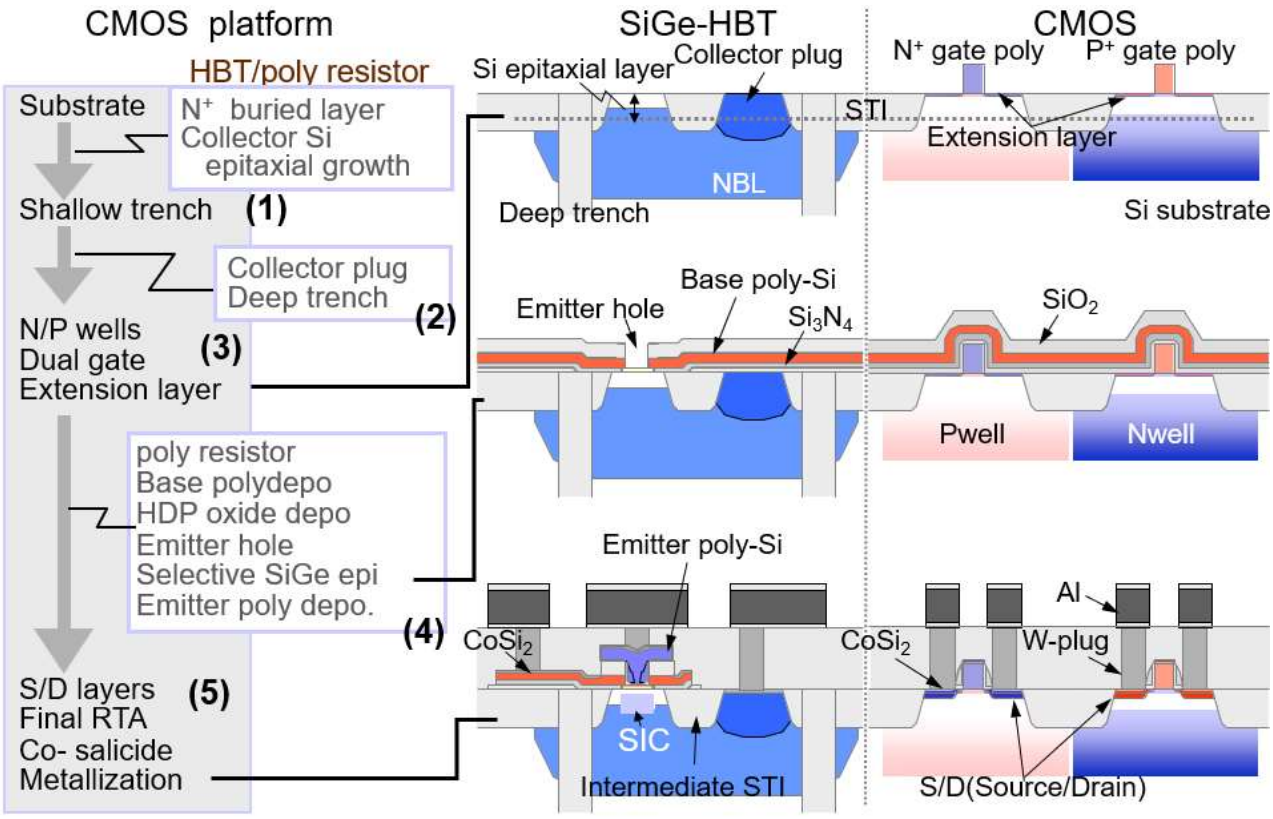


Fig. 2.2. Process flow of the 0.18 μm SiGe BiCMOS in this study [4].

with MOS gate fine pattern forming.

On the other hand, if the deep trench was widened, the substrate parasitic capacity could be reduced. However, if the deep trench was widened, the deposited oxide layer should be thickened, and there would be issues in productivity. LP-CVD deposited a total of 1.0 μm thick oxide layer to flatten the 0.4 μm wide trench. It meant that an oxide layer thickness should be 2.5 times thicker than the trench width. The width of the deep trench was set to 0.4 μm also at the viewpoint of productivity.

(3) Formation of MOS diffusion layers (Figs. 2.2(3), 2.3(3))

Dual gate oxide layers with thicknesses of 3.5 nm and 6.5 nm were fabricated for the 1.8 V MOS and 3.3 V MOS, respectively. The thermal budget required in the oxynitride process (1050 ºC for 30 seconds) was much larger than the final RTA at 1000 ℃ for 1 second. This oxynitride process was the biggest reason MOS gate formation was set before the SiGe HBT formation process. Deposition of a non-doped polysilicon layer was followed by N/P impurity MOS gate implantation and dry etch patterning. A processing step using rapid thermal annealing (RTA) at over 1000 ℃ was carried out immediately after extension implantation to reduce the transient enhanced diffusion (TED) of impurities implanted in the extension and halo regions. Because the TED effect has been usually observed in relatively low-temperature furnace annealing processes, RTA has been immediately used after implantation to suppress the short channel effects in CMOS devices from the 0.18 μm generation [7]. The gate sidewall (SW) formation process included the thermal deposition of an oxide layer at a relatively low

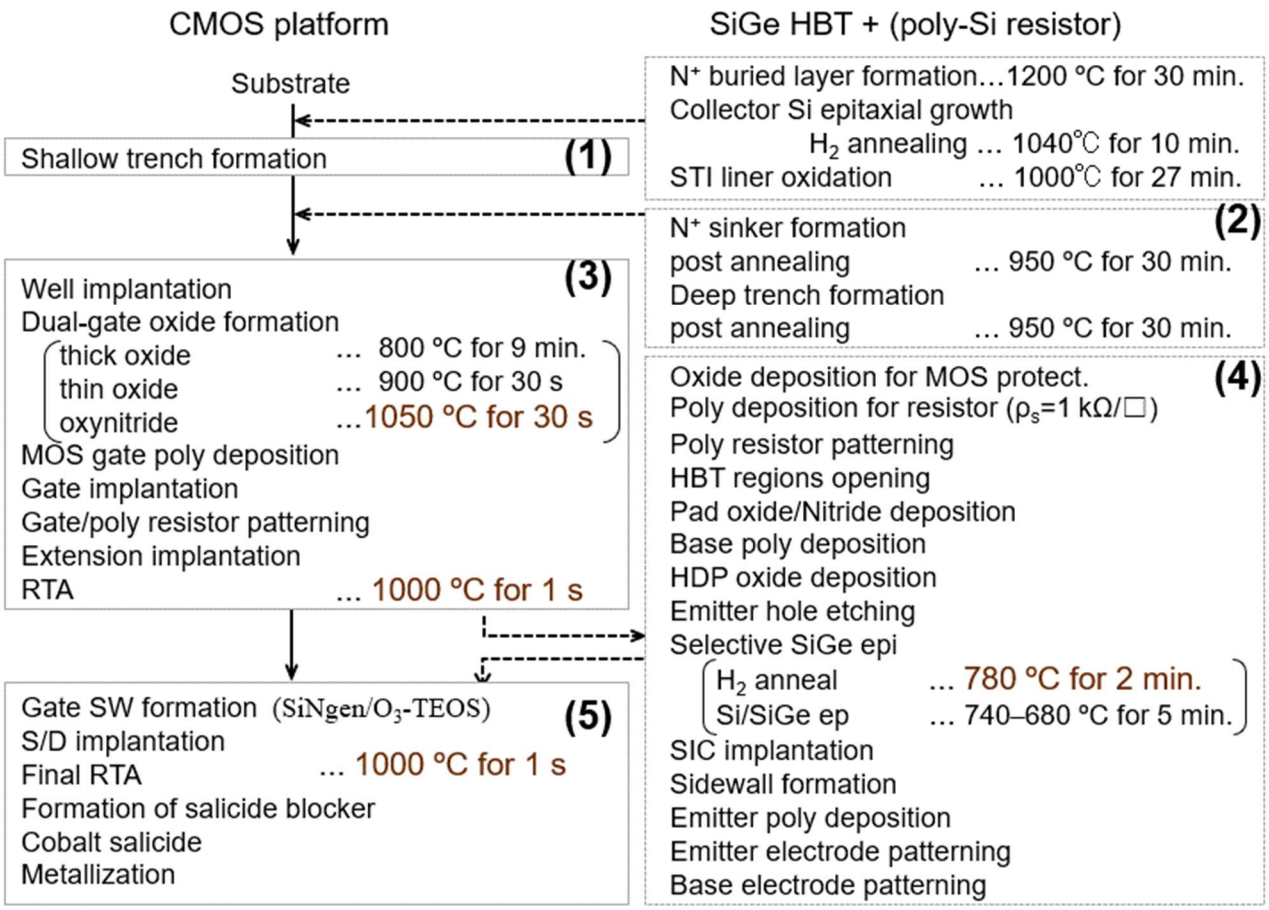


Fig. 2.3. Sequence of this study's 0.18 μm SiGe BiCMOS process. Explanation for the formation of passive components of metal-insulator-metal capacitors and Schottky barrier/varactor diodes is omitted [4].

temperature.

(4) Base/Emitter formation (Figs. 2.2(4), 2.3(4))

A SiGe HBT with a double-polysilicon self-aligned structure was formed in the collector region surrounded by the STI on the NBL (Fig. 2.4). There have been two ways for forming a SiGe layer: the blanket epitaxial growth technology for non-selective growth and the selective epitaxial growth technology, and various SiGe HBT structures and device manufacturing processes have been developed using each way. In this study, a SiGe epitaxial growth layer was selectively grown only in the emitter hole to take advantage of the conventional self-aligned structure. The extrinsic base can be formed in a self-aligned manner during the growth of the SiGe layer by adopting the selective growth technology, making it possible to shorten the emitter-base electrode separation region without limitation from alignment accuracy in the lithography process.

After depositing a stack of oxide and nitride layers on the MOS gates and poly-Si resistors, *in-situ* boron-doped poly-Si that served as the base electrode and an oxide layer were deposited to form an emitter hole for performing a SiGe HBT (Fig. 2.4(a)). The nitride and oxide layers deposited under the base poly-Si electrode were dry-etched after processing the base electrode and became sidewalls of the MOS gate. After a SiGe epitaxial growth layer was selectively grown in the emitter hole (Fig. 2.4(c)), the thermal CVD deposited an oxide layer and an *in-situ* phosphorus-doped poly-Si layer. This poly-Si layer was etched back to form a poly-Si sidewall in the emitter hole. After that, the oxide layer was wet-etched until the Si substrate was exposed, and the emitter-base electrode separation region was formed in a self-aligned manner (Fig. 2.4(e)).

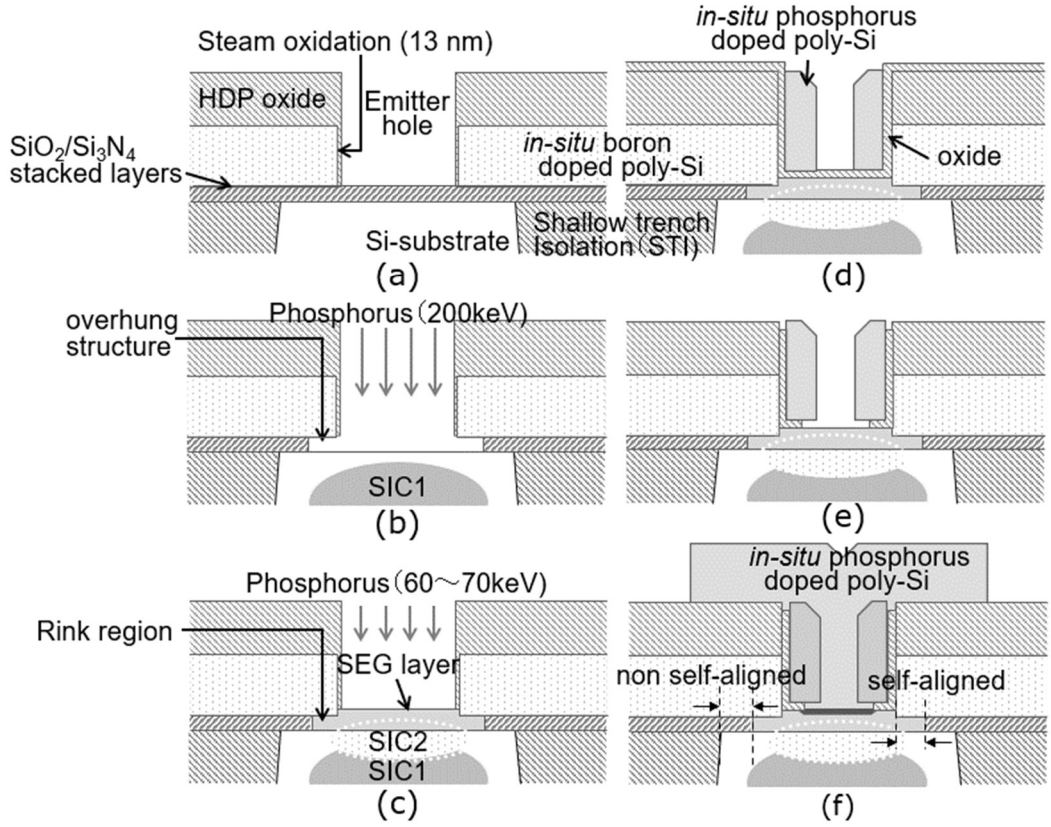


Fig. 2.4. Process flow for forming SiGe base region and emitter-base electrode separation wall as self-aligned structure. (SIC1: Phosphorus, 200 keV(Rp=253 nm, ΔRp=78 nm), SIC2: Phosphorus, 60 keV(Rp=73 nm, ΔRp=30 nm), Rp: Projected range, ΔRp: Projected standard deviation)

Phosphorus ion implantation into the collector layer was divided into the SIC1 region after opening the emitter hole (Fig. 2.4(b)) and the SIC2 area after the SiGe-layer formation (Fig. 2.4(c)). This way, a homogeneous SIC profile was formed under the SiGeC layer. Further deposition of an *in-situ* phosphorus-doped poly-Si layer followed by steps for patterning the emitter and base electrodes (Fig. 2.4(f)). During activating impurities in the diffusion and poly-Si layers by the final RTA, the emitter layer was formed by shallowly diffusing phosphorus from the emitter poly-Si electrode to the substrate surface.

(5) Source/Drain(S/D) formation (Figs. 2.2(5), 2.3(5))

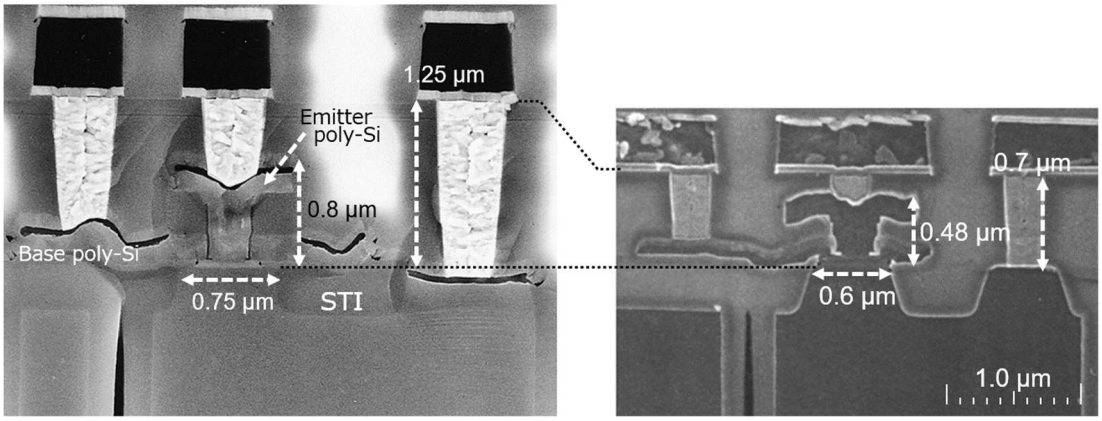
The position of the S/D formation process in the BiCMOS process was before the bipolar transistor formation process block until the 0.25 μm generation. However, this S/D formation process moved after the SiGe HBT formation block in the 0.18 μm generation. The S/D impurities were diffused due to the thermal budget in the bipolar transistor formation process until the 0.25 μm generation, so the layout design rules were changed from those of the CMOS process, such as increasing the sidewall (SW) length of the MOS gate and the gate length of the PMOS. However, the development policy from the 0.18 μm generation was to construct a BiCMOS process without changing the layout or device structure from the CMOS process. Since the impurity concentrations of the MOS extension and halo regions were lower than those of the S/D areas, these regions were less susceptible to thermal budget in the bipolar transistor formation process. However, the high-concentration ion implantation process into the S/D areas was set after the SiGe HBT formation process. After forming poly-Si electrodes for the base and emitter, the nitride layer and oxide layer were etched back to form the sidewalls of the MOS gate, and impurity ions were implanted into the S/D regions of the MOS.

After that, the final RTA activated the impurities, and Co salicide layers were formed on the diffusion layer.

2.3 Maintaining the Gate Pitch of Standard CMOS

(1) Inter-metal dielectric layer (IML) formation

Because the first SiGe process in this study was an HBT-only 0.25 μm process without CMOS, the thickness of the IML was thicker than that of logic CMOS to reduce the parasitic capacitance between wires. Therefore, a height of 0.8 μm of the SiGe HBT was no issue (Fig. 2.5). On the other hand, in the second-generation BiCMOS process, each layer was made thinner to lower the SiGe HBT height to 0.6 μm, and the IML thickness was 0.95 μm, which was the same as the 0.25 μm CMOS. Generally, the IML thickness has been determined according to the contact



(a) 1st generation of 0.25μm SiGe HBT (b) 0.18μm SiGe HBT

Fig. 2.5. SiGe HBT height comparison by generation.

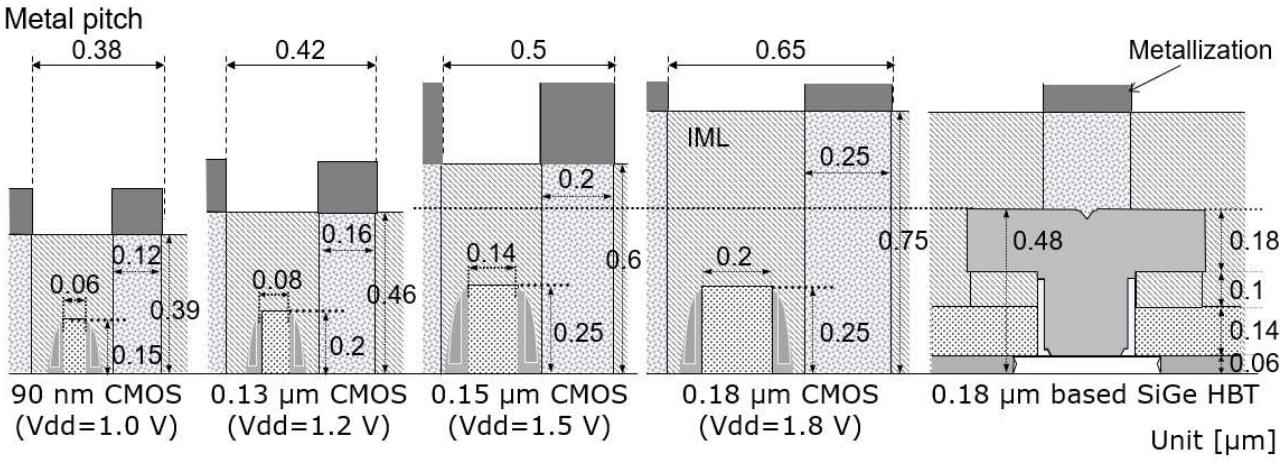


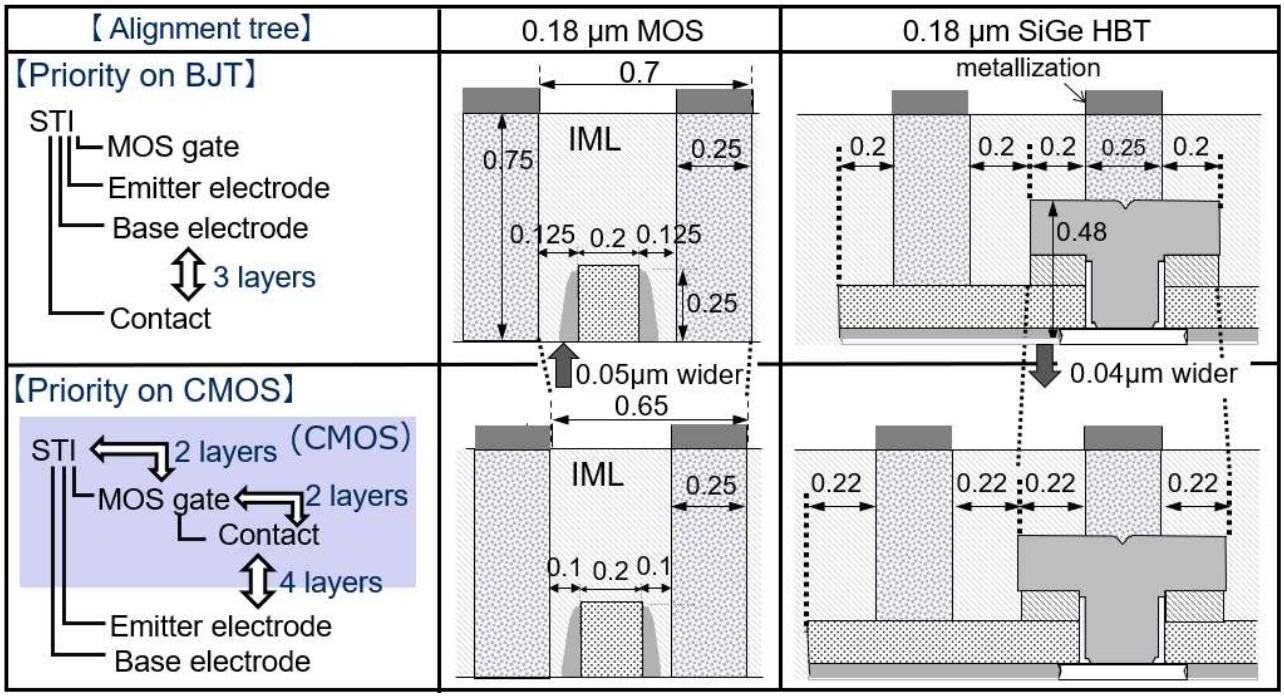
Fig. 2.6. Schematic cross-section and typical values for 0.18 μm SiGe HBT and 0.18 μm to 90 nm MOSFETs [4].

hole size, so the aspect ratio of the contact hole has been about three. Therefore, it was necessary to thin the IML in accordance with narrowing the wiring pitch. Furthermore, the IML became thinner in the 0.18 μm generation, so the SiGe HBT height was lowered to 0.48 μm (Fig. 2.6). On the other hand, the height of the 0.18 μm SiGe HBT can be used up to the 0.15 μm CMOS generation, but the 0.13 μm CMOS must reduce the height of the SiGe HBT by thinning the layer.

(2) Setting alignment relations in the lithography process

In the BiCMOS processes, the major diffusion layers (such as the MOS gate, emitter electrode, and contact hole) were aligned with the STI layer in the lithography process until the 0.25 μm generation. On the other hand, in CMOS, the contact hole has been aligned with the MOS gate because it is essential to shrink the gate pitch.

Table 2.2. Concept comparison of alignment tree regarding MOS and BJT in SiGe BiCMOS (Unit : μm).



Therefore, the BiCMOS process also changed to align the contact holes with the MOS gates from the 0.18 μm generation and later (Table 2.2). Considering the case of the 0.18 μm CMOS (when the gate pitch is 0.65 μm), if the variation in dimensions is ±10 %, the gate length could expand 0.01 μm on one side, and the contact hole size could expand 0.0125 μm on one side. Therefore, even if the distance between the contact hole and the gate was designed to be 0.1 μm, the actual distance could be 0.0755 μm. If the positional accuracy of the KrF stepper exposure apparatus is 0.06 μm, a margin of 0.0125 μm can be secured between the two layers. On the other hand, when the gate and the contact hole are in a relationship of alignment between the three layers, the amount of misalignment could be as below.

$$\text{Misalignment between the three layers} = \sqrt{0.06^2 + 0.06^2} = 0.0849\ \mu\text{m} \quad (2.1)$$

Because the misalignment between the three layers increases by 0.0249 μm compared to the two layers, it becomes necessary to widen the gate pitch accordingly. Gates and contact holes were aligned between three layers in BiCMOS up to the 0.25 μm generation, so it was required to modify the CMOS design properties again to expand the MOS gate pitch. Conversely, if the gate and the contact hole are aligned between two layers, the emitter electrode and the contact hole of the bipolar transistor are aligned between four layers, so the following is obtained.

$$\text{Misalignment between the four layers} = \sqrt{0.06^2 + 0.06^2 + 0.06^2} = 0.1039\ \mu\text{m} \quad (2.2)$$

Since the amount of misalignment increases by 0.0199 μm compared to the case of three layers, the emitter electrode should expand by 0.04 μm on both sides (Table 2.2). The increase in parasitic capacitance due to the expansion of the emitter electrode width was concerned until the 0.25 μm generation. Still, it became clear that there were more issues in redesigning the CMOS, and the same alignment tree as the CMOS was adopted from the 0.18 μm generation. As discussed in Chapter 6, it should be resolved by choosing a finer process rather than a SiGe HBT-prioritized alignment tree if reducing the size of the SiGe HBT would be essential for speeding up.

2.4 Low-temperature H_2 Annealing to Prevent Boron Penetration from the P-type Gate

2.4.1 Setting H_2 Annealing Conditions in the 0.25 μm Generation

In this study, the intrinsic base layer of the SiGe HBT was selectively formed in the emitter hole by single-wafer LP (Low Pressure)-CVD (AMAT Centura). In addition to the LP-CVD, there has been the UHV (Ultra High Vacuum)-CVD as a SiGe epitaxial growth technology. The UHV suppresses the natural oxide layer growth on the Si substrate surface by maintaining an ultra-high vacuum of 10^{-4} Torr in the process chamber to eliminate residual oxygen. However, since the material of the chamber has been the SUS (Stainless Used Steel) to maintain an ultra-high vacuum, corrosive gas cannot be used. Therefore, there has been an issue with the boron memory effect, in which the boron atmosphere is constantly released into the chamber due to deposits containing boron adhering to the inner wall of the chamber. On the other hand, since the pressure is as low as 10 Torr in the LP-CVD, using a quartz chamber makes it possible to perform a cleaning process in the chamber with HCl, thereby suppressing the boron memory effect. In addition, the growth of the native oxide layer on the Si substrate in the LP-CVD was stopped by an H_2 Jumbo flow of 35 ℓ/ minute at 15-Torr pressure. In this study, the LP-CVD expected to have higher productivity was selected.

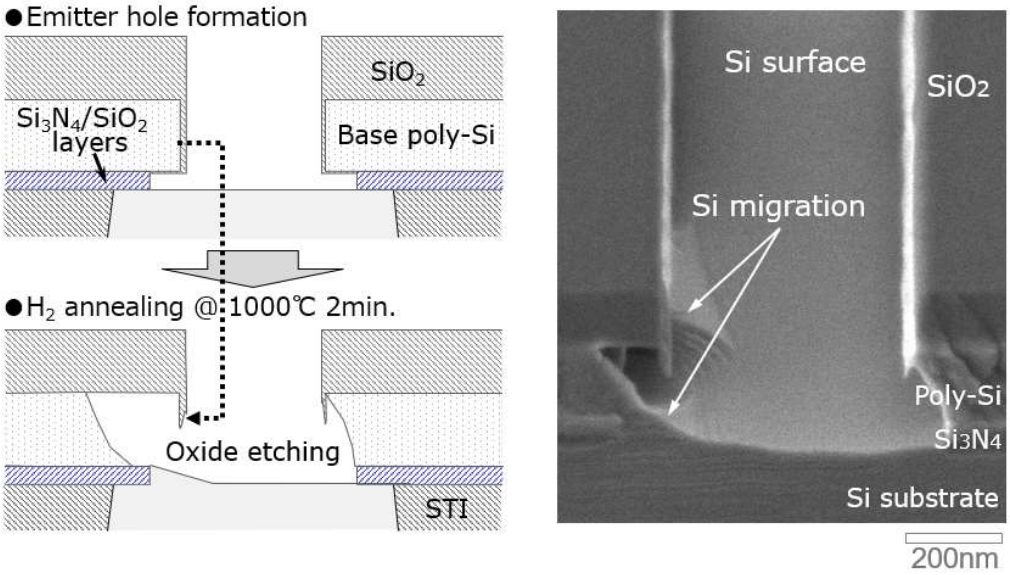


Fig. 2.7. Surface condition deterioration by H_2 annealing at 1000 ℃ for 2 minutes after emitter hole opening. (Process conditions: Pressure=15 Torr, H_2 flow rate=35 ℓ/min.)

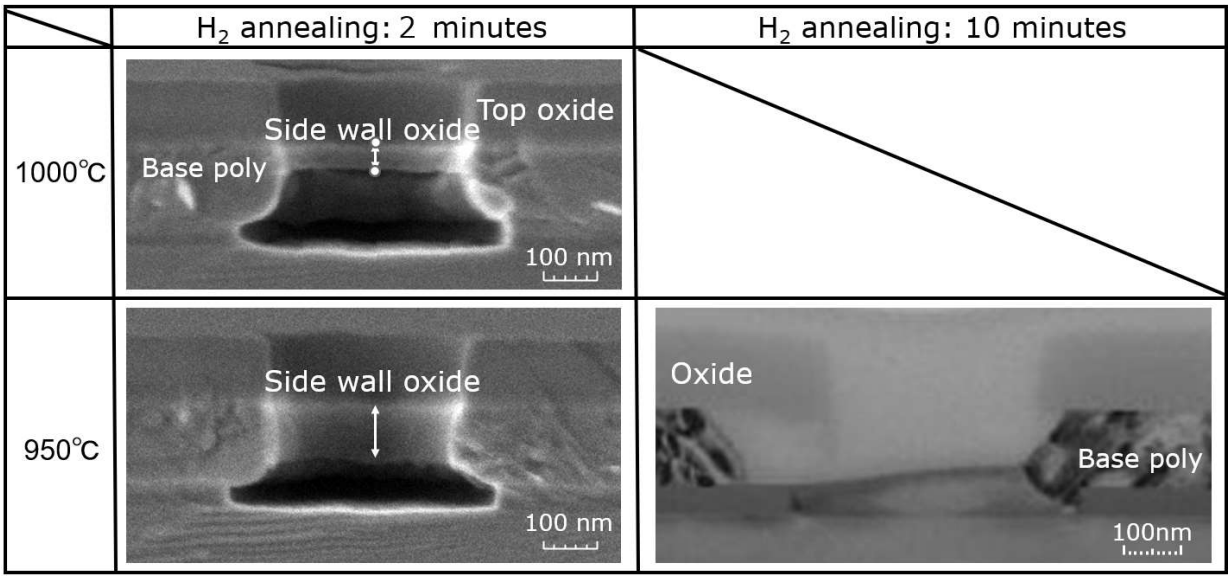
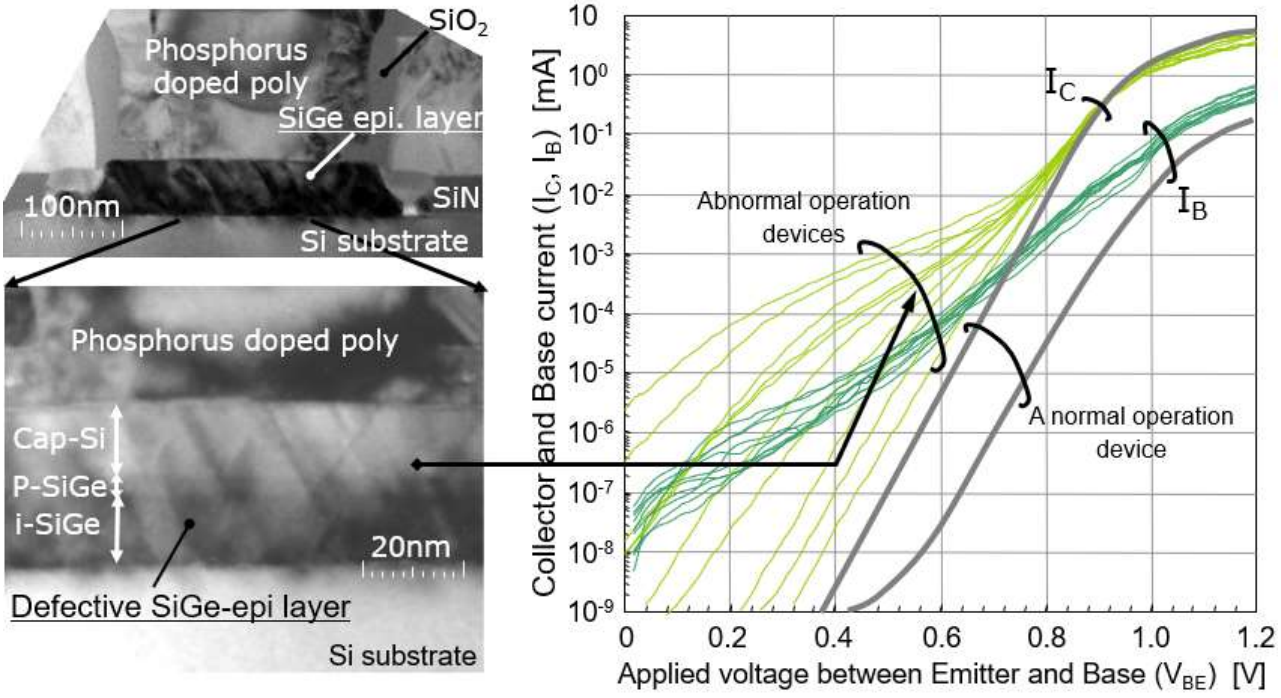


Fig. 2.8. Si migration during the H_2 annealing (15 Torr, H_2 35 ℓ/minute) after opening the emitter hole.

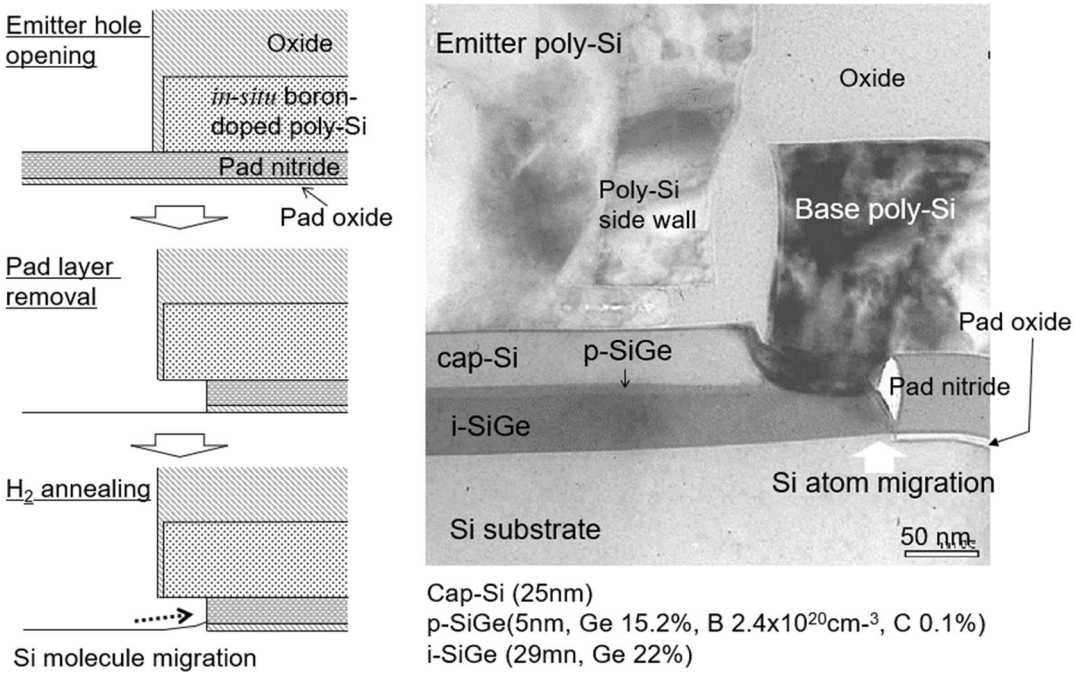
In SiGe HBT formation, the H_2 annealing step before the SiGe epitaxial growth in the LP-CVD requires a high thermal budget. It is a process to remove the natural oxide layer and residual carbon on the Si surface. In the conventional blanket Si epitaxial growth to form a collector layer, the standard conditions were 1040 ℃ for 10 minutes. Even though 1000 ℃ for two minutes, which was lower and shorter than the case of the collector Si epitaxial growth, was applied to the formation of the intrinsic base layer, severe Si migration occurred until the device structure was destroyed (Fig. 2.7). The oxide layer covering the base poly-Si electrode also became thin. The amount of etched oxide layer far exceeded the thickness of a natural oxide layer. Even when the temperature was lowered to 950 ℃, the sidewall oxide layer was etched. In addition, Si migrated from the poly-Si electrode and grew solid-phase epitaxial on the Si substrate surface (Fig. 2.8). The amount of Si migration depended on the H_2 annealing time, and it could be thought that the amount of Si migration was equivalent at 1000 ℃ for two

minutes and 950 ℃ for 10 minutes. It is presumed that the Si migration region contains boron from the *in-situ* boron-doped poly-Si, and there was concern about the effect on the characteristics. The standard conditions of Si epitaxial growth equipment manufacturers were set for defect-free Si epitaxial growth over the entire wafer surface. Still, these were extreme conditions for cleaning the limited area of the emitter hole.



(a) TEM cross-sections of crystal defects (b) Gummel plots

Fig. 2.9. Crystal defect occurrence in a SiGe layer due to residual oxygen on the substrate surface (H_2 annealing at 800 ℃ for 2 minutes, applied process conditions before countermeasures).



(a) Cross-section of cavity formation (b) TEM cross-sectional view of the base region of SiGe HBT

Fig. 2.10. Si migration during H_2 annealing at 875 ºC before epitaxial growth [4].

On the other hand, when H_2 annealing was performed at 800 ℃, the static characteristics of the SiGe HBTs showed leakage currents, and the SiGe epitaxial growth layer had crystal defects (Fig. 2.9). These results showed the removal of the natural oxide layer was not sufficient. In the case of the H_2 annealing at 875 ℃ for two minutes, there were no significant leakage currents in the static characteristics, and receding of the side wall oxide layer was not observed. An epitaxial growth layer without defects was formed, although there was slight migration of Si atoms. (Fig. 2.10). The slight migration of Si atoms at 875 ℃ was judged to prove that the natural oxide layer had been removed, so the H_2 annealing condition was set at 875 ℃ for two minutes in the 0.25 μm generation.

In addition to temperature, pressure, time, and H_2 flow rate are also presumed to affect the amount of oxide layer etched and Si migration. However, only low temperature was considered an item to be examined in this study.

2.4.2 Lower-temperature H_2 Annealing in the 0.18 μm Generation

(1) Factors of PMOS V_{TH} fluctuation due to H_2 annealing

When the condition of "875 ℃ for two minutes" was applied to the 0.18 μm SiGe BiCMOS process for H_2 annealing before the SiGe epitaxial growth, the PMOS threshold voltage (V_{TH}) changed by 0.42 V (Fig. 2.11). V_{TH} fluctuation of 0.16 V occurred even at 825 ℃ for two minutes, but V_{TH} fluctuation remained at 0.02 V after N_2 annealing at 850 ℃ for two minutes. A significant difference arose due to the atmosphere during the annealing. Since the V_{TH} fluctuated equally regardless of the gate length, it was not the deterioration of the short channel characteristics due to increased lateral diffusion of the S/D regions. It was determined that boron penetrated the gate oxide layer from the PMOS gate poly-Si and leaked into the channel region. During the SiGe epitaxial growth, the MOS gate was covered with a 150-nm-thick base poly-Si electrode, a 150-nm-thick HDP layer directly above the base poly-Si electrode, and a pad nitride layer and oxide layer below the base poly-Si electrode (Fig. 2.12). Hydrogen molecules passed through these stacked layers, accelerating the boron diffusion from the gate poly-Si.

PMOS generally used the same n-type gate as NMOS until the 0.25 μm generation, so the V_{TH} of PMOS did not change even under the conditions of H_2 annealing at 875 ℃ for two minutes. The PMOS gates have changed to the p-type gates from the 0.18 μm generation, and it has become necessary to take countermeasures against boron penetrating the channel during the H_2 annealing. Many reports have shown that H_2 promotes boron diffusion in oxide layers [10][11][12]. Here, the following equation expresses the temperature dependence of the diffusion amount of boron in the oxide layer [12].

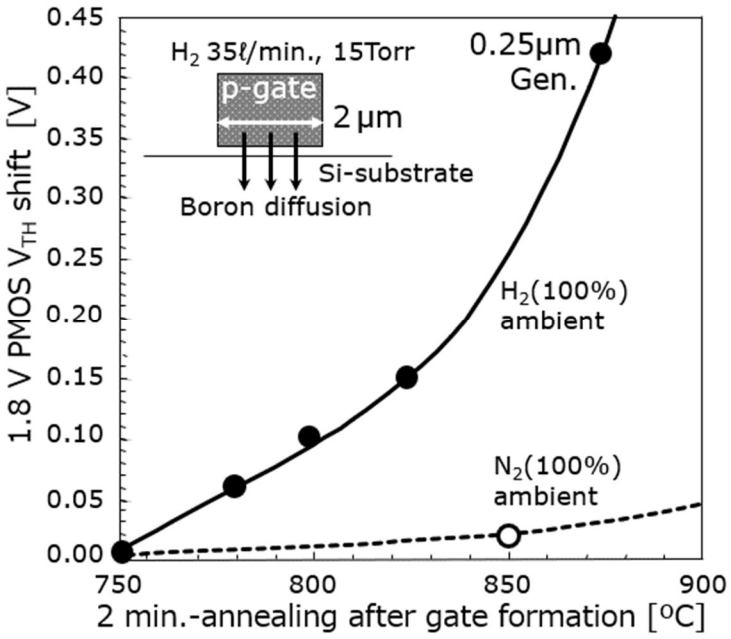
$$D_B = Do \exp(- qEa/kT) \quad (2.1)$$

Do: Diffusion constant

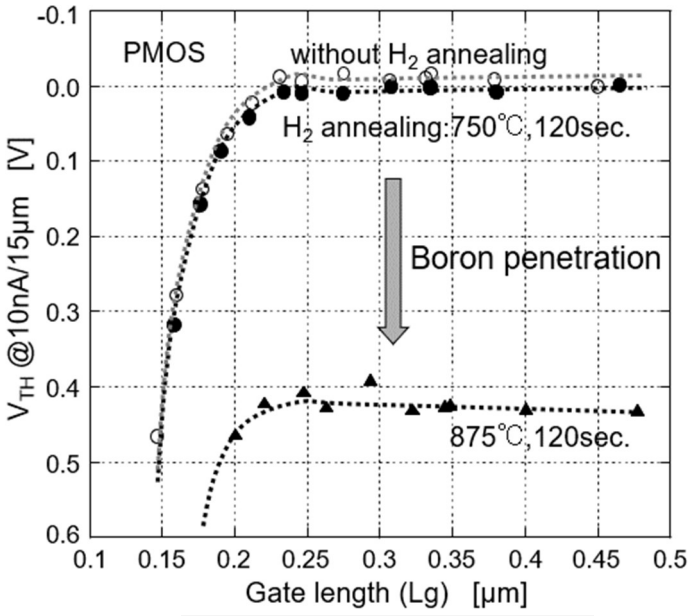
Ea: Activation energy

From the extrapolated value of the dependence of V_{TH} on the number of ions implanted into the channel region (Fig. 2.13(a)), the boron concentration that leaked into the channel region during H_2 annealing was predicted. The activation energy (Ea) was 2.2 eV from the temperature dependence of the amount of boron penetration through the gate oxide layer (Fig. 2.13(b)). The activation energy of boron diffusion in the oxide layer by N_2 annealing was reported to be 3.31 eV for the 2.5 nm thick oxide layer and 3.55 eV for the 11 nm thick oxide layer [6]. According to R. A. Street's paper [12], the Ea of the boron diffusion decreased to 3.00 eV in a mixed atmosphere of N_2/H_2 with 10 % H_2 added from 3.53 eV in N_2 annealing. This result indicated that the boron diffusion was facilitated by

hydrogen. On the other hand, the Ea of the diffusion rate of hydrogen was reported to be 1.4-1.5 eV in samples without impurities and 1.2-1.3 eV with impurities [13]. The result of this study was between the Ea of hydrogen diffusion and the Ea of the boron diffusion under N_2 annealing conditions. In the report of [12], it was speculated that hydrogen molecules played a role in disconnecting Si and boron as a mechanism for accelerating boron diffusion by hydrogens. Since Si atoms on the substrate migrate with H_2 annealing at 875 ℃, hydrogens promoted Si molecules' movement while cutting Si-Si connections. If hydrogen diffused first and boron diffused along the same route, it is reasonable that Ea resulted in an intermediate value between them. In addition, the low temperature



(a) H_2 annealing temperature dependence of PMOS V_{TH} variation (gate length=2 μm)



(b) Gate length dependence of PMOS V_{TH}

Fig. 2.11. PMOS V_{TH} shifts due to H_2 annealing before SiGe epitaxial growth. Gate oxide thickness was 3.5 nm for 0.18 μm CMOS [4].

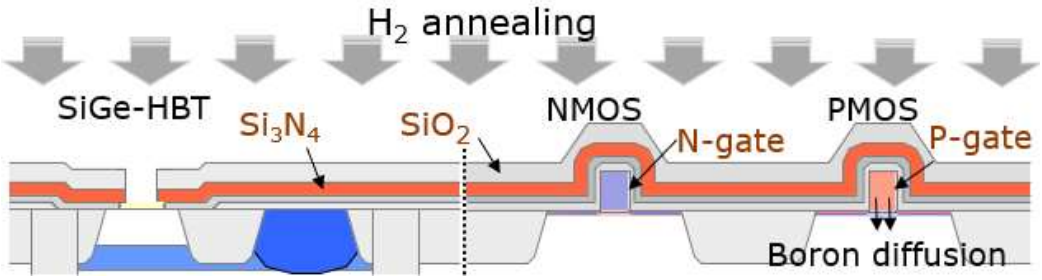
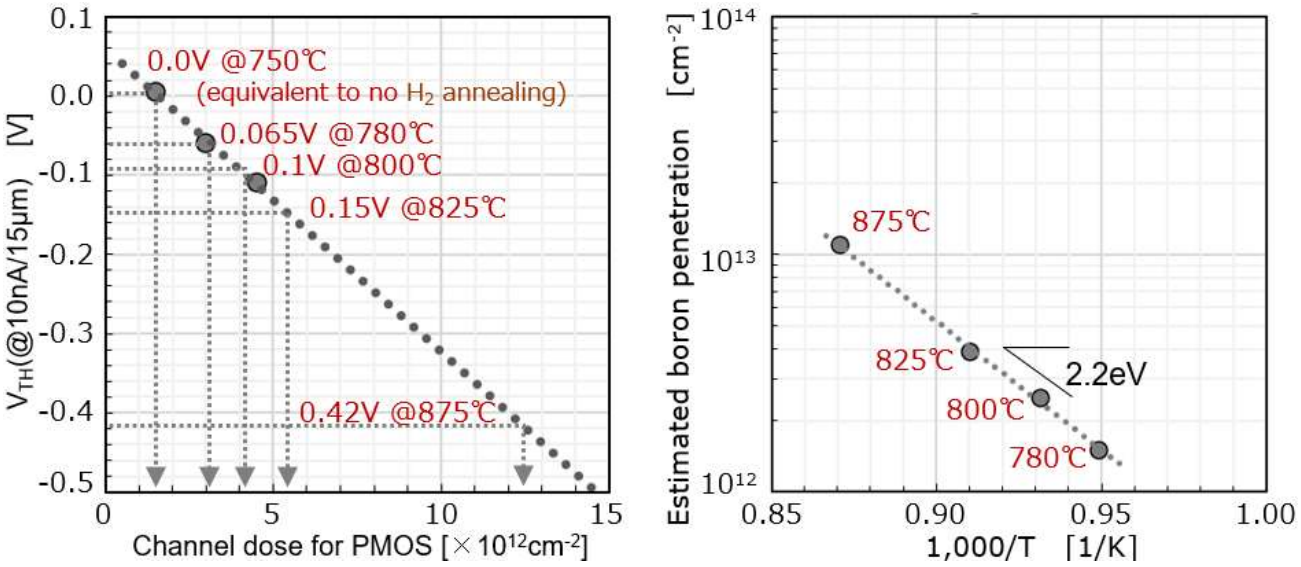


Fig. 2.12. SiGe BiCMOS cross-sectional structure during the SiGe epitaxial growth process



(a) Channel implantation dose dependence of V_{TH} (b) H_2 annealing temperature dependence of boron leakage

Fig. 2.13. H_2 annealing temperature dependence of V_{TH} of the 1.8 V PMOS (gate oxide layer thickness = 3.5 nm). Convert the amount of boron penetration from the amount after subtracting the initial 1.6×10^{12} cm^{-2}.

dependence of the penetration amount of boron through a gate oxide layer during H_2 annealing indicates the necessity of thoroughly lowering the temperature of the H_2 annealing.

This issue can be avoided by implanting boron ions into the gate poly-Si layer at the same time as impurity ion implantation into the S/D layers instead of implanting boron ions into the gate poly-Si layer of the PMOS before forming the SiGe HBT. At this time, because phosphorus has a slower diffusion rate than boron, the phosphorus doping into the n-type gate of the NMOS should be left as it was before the formation of the SiGe HBT. Because boron atoms are not contained in the PMOS gate during H_2 annealing before SiGe epitaxial growth, there is no need to worry about enhanced diffusion due to H_2 annealing. However, the thermal budget of the final RTA must be suppressed to prevent the distribution of the p-type intrinsic base layer of the SiGe HBT, and it conflicts with diffusing boron sufficiently in the gate poly-Si layer. In this case, a depletion layer that could be generated in the p-type gate shall degrade the PMOS characteristics, and this method was not adopted in this study.

(2) Surface oxidation due to moisture release during the device fabrication process

Next, the cause of crystal defects at the H_2 annealing of 800 ℃ in the 0.25 μm generation was pursued. A Si

layer was epitaxially grown on a bare wafer that had not undergone the process. The H_2 annealing temperature dependence of carbon and oxygen remaining at the growth layer/substrate interface was analyzed by SIMS (Secondary Ion Mass Spectrometry) (Fig. 2.14). Carbon and oxygen remained at the H_2 annealing of 740 ℃, but these were not detected at 760 ℃ or higher. An evaluation using a bare wafer showed that the H_2 annealing temperature could be lowered to 760 ℃.

Next, the difference between the state of the bare wafer and the in-process wafer was evaluated by TDS-APIMS (Thermal Desorption Gas Analysis by Atmospheric Pressure Ionization-Mass Spectrometry). A large amount of

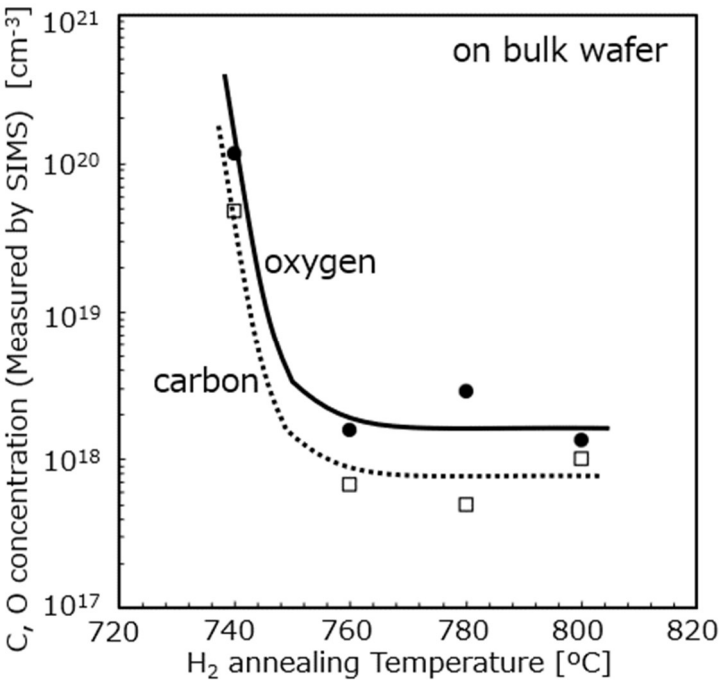


Fig. 2.14. Carbon and oxygen concentrations on the surface between SiGe epitaxial growth layer and Si substrate [4].

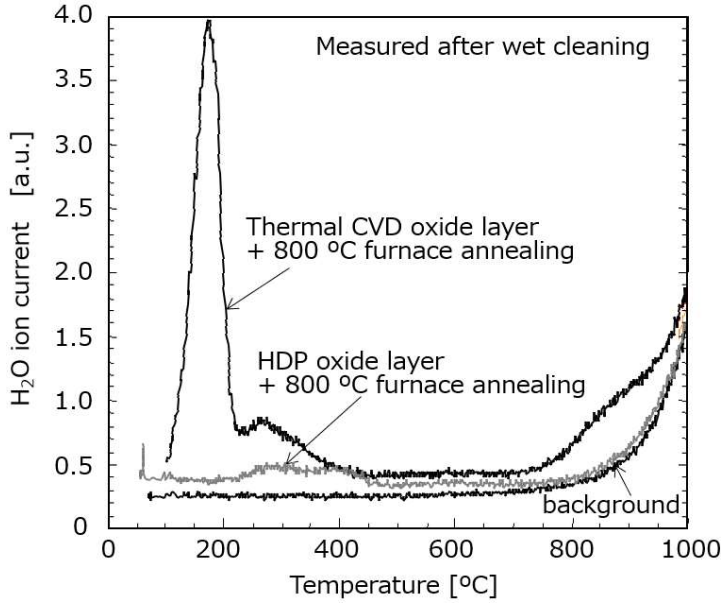


Fig. 2.15. Desorption spectrum of thermally stimulated moisture from oxide layers [4].

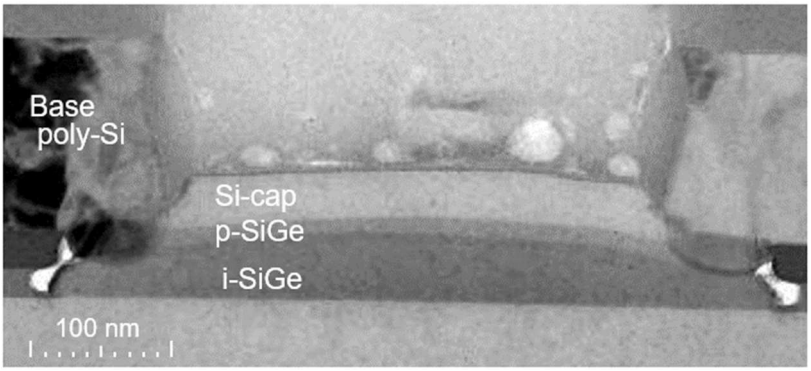
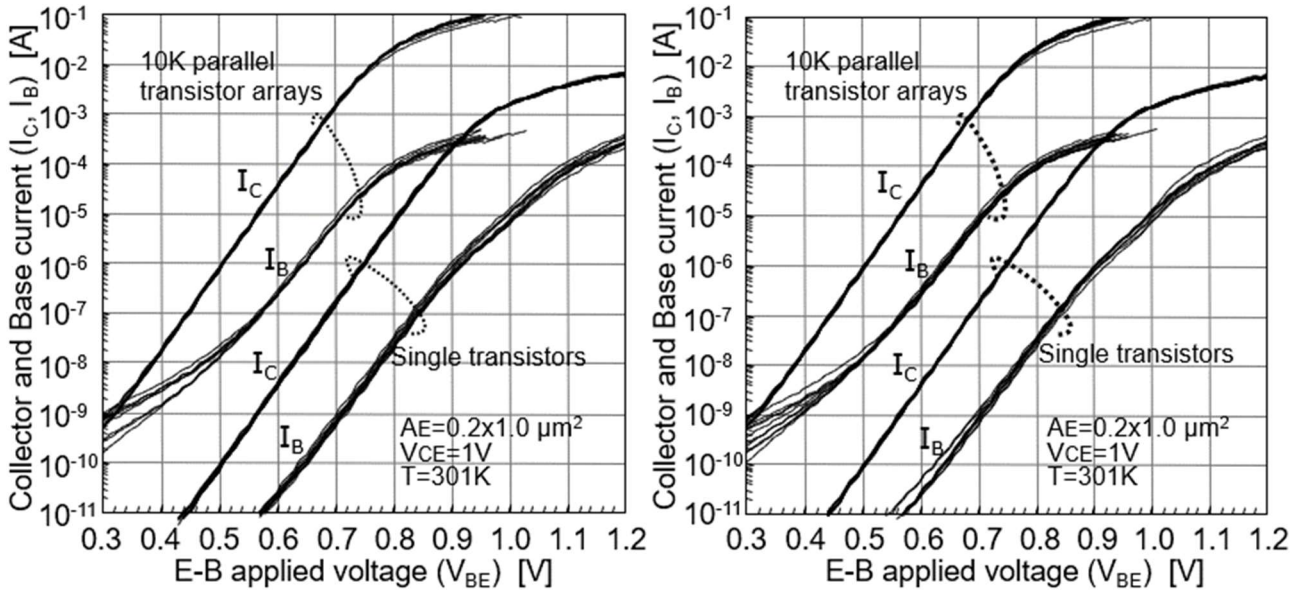


Fig. 2.16. TEM cross-section of the SiGe epitaxial growth layer after H_2 annealing at 780 ℃ for two minutes. A sample switched the oxide layer on the base poly-Si electrode from the thermal CVD layer to the HDP layer.



(a) H_2 annealing=800 ℃ for 2 minutes (b) H_2 annealing=760 ℃ for 2 minutes

Fig. 2.17. The Gummel plots of SiGe HBTs after changing the oxide layer to the HDP layer on the base poly-Si electrode. (Measured on ten chips in the same wafer).

moisture was released at 170 ºC, and a certain amount of moisture was released at temperatures above 750 ºC from the oxide layer deposited by the batch-type thermal LP-CVD method at 680 ºC using Dichlorosilane as the raw material (Fig. 2.15). It was presumed that there was a competitive state during the H_2 annealing between the accelerated oxidation by this moisture and the oxide layer etching by hydrogen. It was determined that the 800-ºC H_2 annealing was insufficient to remove the thermal oxide layer formed by moisture. It was assumed that the moisture desorbed at 170 ºC and 280 ºC was adsorbed on the surface during wet cleaning, and the moisture released at 800 ºC or higher was taken into the layer by combining hydrogen and oxygen in the source gas. On the other hand, the oxide layer formed by the HDP-CVD had little desorbed moisture even though it was deposited at 400 ℃. It was considered that the denser HDP layer absorbed less moisture during deposition and wet cleaning.

After the oxide layer on the base poly-Si layer was changed from the LP-CVD layer to the HDP layer, the crystallinity of the SiGe layer did not deteriorate even when the H_2 annealing temperature was set to 780 ℃ (Fig.

2.16). In addition, the static device characteristics evaluated by the Gummel plots showed no increase in leakage current even under the conditions of the H_2 annealing at 800 ℃ and 760 ℃ (Fig. 2.17), realizing a high bipolar transistor yield of 99.99993 %. While the H_2 annealing temperature was set at 780 ℃, the exact characteristics of the 0.18 μm CMOS were maintained on the SiGe BiCMOS process by changing the channel dose amount to adjust the V_{TH} fluctuation of about 70 mV.

(3) Hydrogen termination formation on the Si surface

It is known that the growth of the natural oxide layer can be suppressed for a certain period when hydrogen atoms terminate Si dangling bonds on the Si substrate surface in dilute hydrofluoric acid cleaning [14]. Here, the hydrogen termination amount was evaluated after removing the 13-nm-thick thermal oxide layer with dilute hydrofluoric acid. According to the XPS's evaluation result of the oxide layer wet etching rate (X-ray Photoelectron Spectroscopy), the oxide layer on the substrate surface was removed in 105 seconds (Fig. 2.18). Still, the evaluation result by FT-IR (Fourier Transform Infrared Spectroscopy) showed that no hydrogen termination layer was formed 50 seconds after the oxide layer was removed. The hydrogen termination amount reached saturation nearly 180 seconds after the oxide layer disappeared.

On the other hand, the prolonged wet cleaning with dilute hydrofluoric acid etched the oxide layer covering the base electrode layer, causing the SiGe layer growth on the base electrode due to the disappearance of the protective layer. Therefore, the pad oxide layer under the base poly-Si electrode had been a thermal oxide layer of 4.4 nm (Wet oxidation, 800 ℃ for 4 minutes) in the 0.25 μm generation, but that was changed to USG (Undoped Silicate Glass) oxide layer in the 0.18 μm generation. The wet etching rate of the USG layer is much faster than that of the thermal oxide layer. This change accelerated the exposure of the Si substrate to ensure the time for forming the hydrogen termination layer. The USG layers were deposited to 10 nm at 570 ℃ under low pressure by a reaction

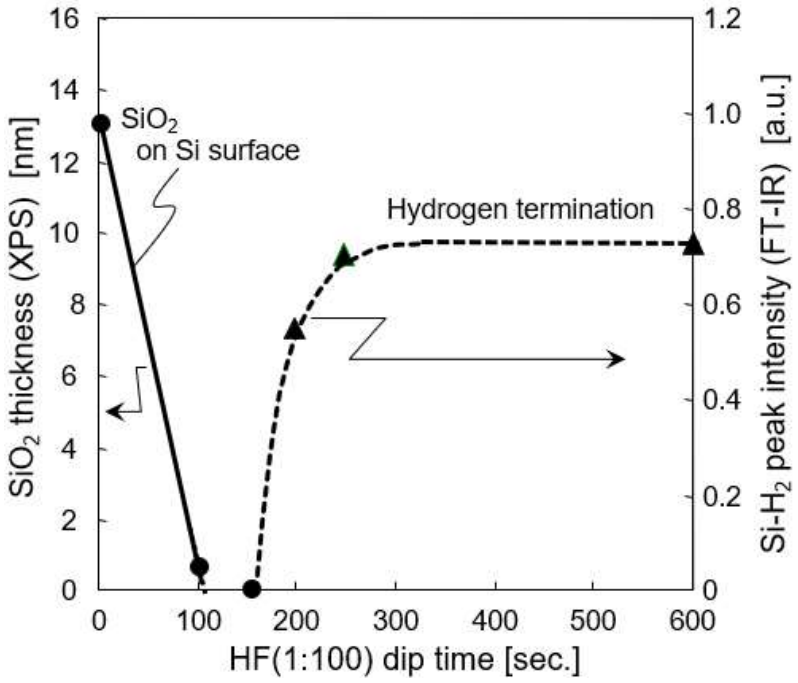


Fig. 2.18. Dependencies of oxide layer thickness and hydrogen termination on HF dip time. XPS measured the thickness of the thin oxide layer; the amount of hydrogen termination was measured by FT-IR. Si-H_2 intensity was measured because two dangling bonds are on Si(100) surface [4].

of organic silicon such as TEOS (TetraEthOxySilane, $Si(OC_2H_5)_4$) with O_3.

(4) Margin confirmation of the low-temperature H_2 annealing

Furthermore, when the retention time of the hydrogen termination on the Si substrate after wet cleaning was evaluated by FT-IR, it was found that hydrogen peeled off from the Si surface and oxidation progressed as the air exposure time after the cleaning was completed (Figs. 2.19, 2.20). No surface oxidation was observed until two hours after the wet cleaning, but about 20 % of hydrogen was desorbed after seven hours, and oxide layer formation started. Furthermore, hydrogen dissociation became about 40 % after 24 hours, and oxidation was progressing. When the hydrogen termination states were saturated after immersion in dilute hydrofluoric acid for 300 seconds, the device yield was not affected up to ten hours of the air exposure time if the H_2 annealing temperature was 760 ℃, but the device yield with a large emitter size particularly declined after exceeding ten hours of the air

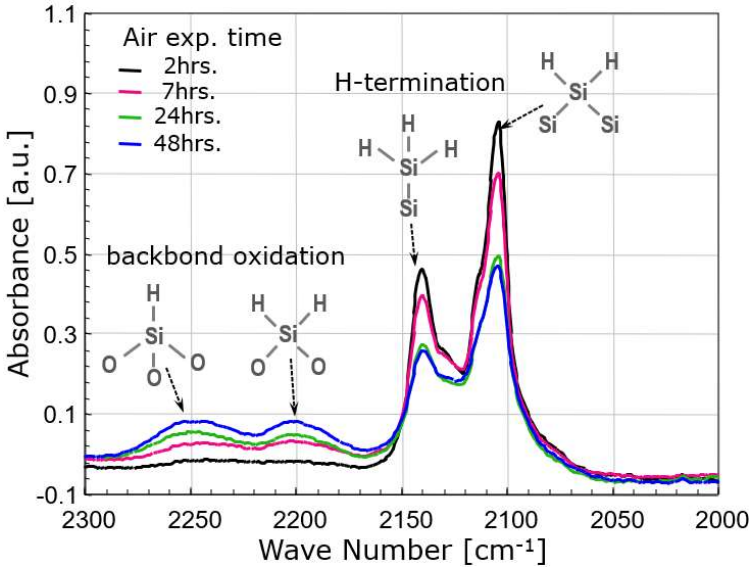


Fig. 2.19. Stability evaluation of hydrogen termination on Si substrate using a bare wafer (FT-IR spectrum).

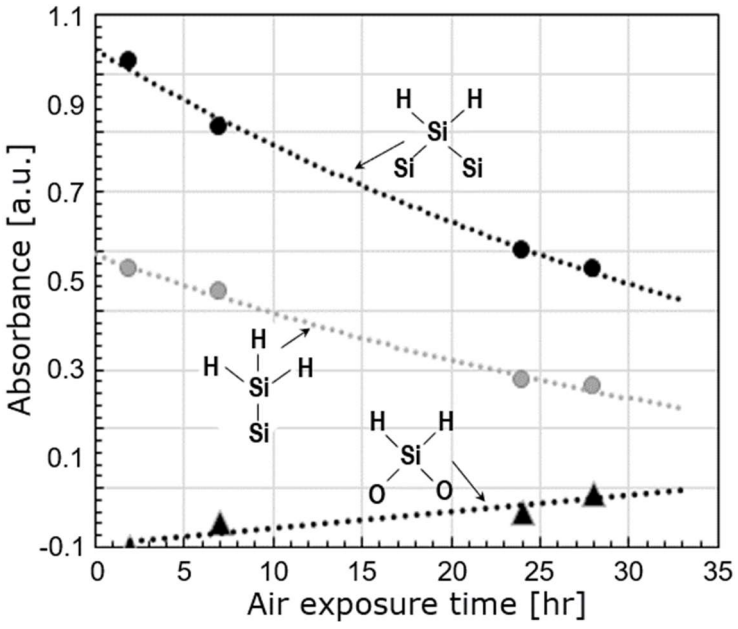
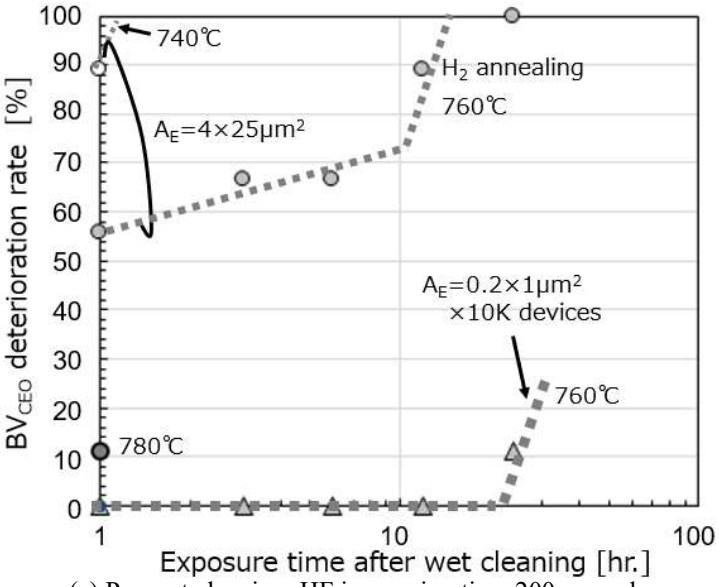
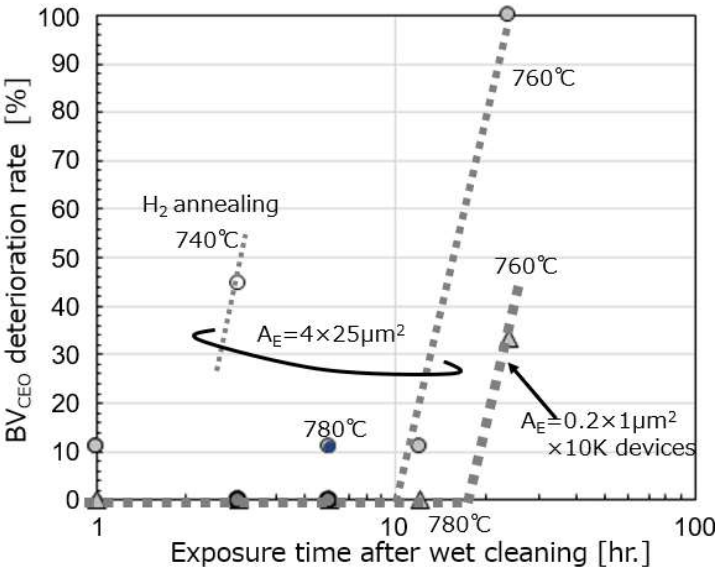


Fig. 2.20. Exposure time dependence of the amount of hydrogen termination on a bare wafer (FT-IR spectrum).

exposure time (Fig. 2.21). Considering this with the FT-IR measurement results, even if the hydrogen termination decreased by 15 % after seven hours from the wet cleaning, the surface oxide layer could be removed by the H_2 annealing at 760 ℃, and there was no influence on the device yield. However, if the air exposure time was longer than that, the oxide layer could not be removed entirely by the H_2 annealing at 760 ℃, and the device characteristics were affected. Furthermore, when the H_2 annealing temperature was 740 ℃, or when the HF immersion time was 200 seconds, the yield of devices with relatively large emitter sizes of 4×25 μm^2 deteriorated. The total area of 10,000 parallel 0.2×1 μm^2 is 2,000 μm^2, which is 20 times larger than the 100 μm^2 area of 4×25 μm^2. Still, the device yield of emitter size of 4×25 μm^2 was lower than 10,000 parallel 0.2×1 μm^2. Although the definite factor that tended to decrease has been unknown, the process conditions were determined considering the yield of devices with large emitter sizes.



(a) Pre-wet cleaning: HF immersion time 200 seconds



(b) Pre-wet cleaning: HF immersion time 300 seconds

Fig. 2.21. BV_{CEO} yield of SiGe HBT after switching oxidation layer on base poly-Si electrode to the HDP layer.
A_E: Emitter area size, dilute hydrofluoric acid cleaning time included 13 nm thick pad oxide layer removal time.

In addition, the time from the completion of wet cleaning to the start of the SiGe epitaxial growth process was limited to shorter than two hours to minimize detachment of the hydrogen termination from the Si surface as a standard process condition. In fact, after the wet cleaning, processing wafers were set in the epitaxial growth apparatus within one hour and were not exposed to the open air after that.

2.5 Reducing Thermal Budget to Prevent Short-Channel Characteristics from Deteriorating

The intrinsic base region of the 0.25 μm generation was formed by a combination of N_2 annealing at 950 ºC for 1 minute and wet thermal oxidation at 800 ºC for 5 minutes [8] (Fig. 2.22). The N_2 annealing recovered from the damage on the Si surface caused by the ion implantation, and the wet oxidation suppressed the boron concentration near the Si substrate surface and reduced the emitter-base junction leakage current. Boron atoms near the Si substrate surface were incorporated into the oxide layer by the surface oxidation process, and the boron concentration on the substrate side decreased. There is still room for shortening the N_2 annealing time at 950 ºC for 1 minute, but a certain amount of surface oxidation is required to suppress the boron concentration on the Si surface, and it could be considered that there are few rooms to reduce the wet oxidation time.

In forming the intrinsic base layer in this study, the LP-CVD method was used to selectively perform a cap-Si/p-SiGeC/i-SiGe stacked layers only in the emitter hole after opening it and removing the nitride layer and the oxide layer (Fig. 2.4(c)). The nitride layer worked as an etching-stopper layer. The step-type Ge profile consisted of a p-SiGeC layer of 15 %, an i-SiGe layer of around 25 %, and a 5-nm i-SiGe layer of 10 %. A 5-nm i-SiGe layer of 10 % becomes a buffer layer between a Si substrate and the i-SiGe layer with a Ge concentration of around 25 %. After that, a cap-Si layer was formed for forming an emitter layer by diffusing phosphorus from the emitter poly-Si layer. The higher the impurity concentration, the faster the growth rate. Therefore, i-SiGe and p-SiGeC layers were grown at 670 ℃, the buffer-SiGe layer at 720 ℃, and the cap-Si layer at 740 ℃ for two minutes. Including H_2 annealing at 780 ℃ for two minutes, the throughput was about 22 minutes/wafer. The thermal budget

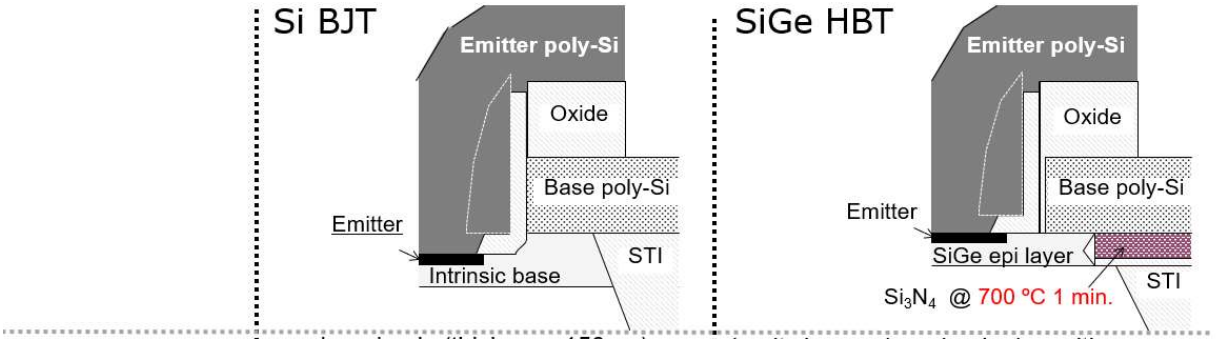


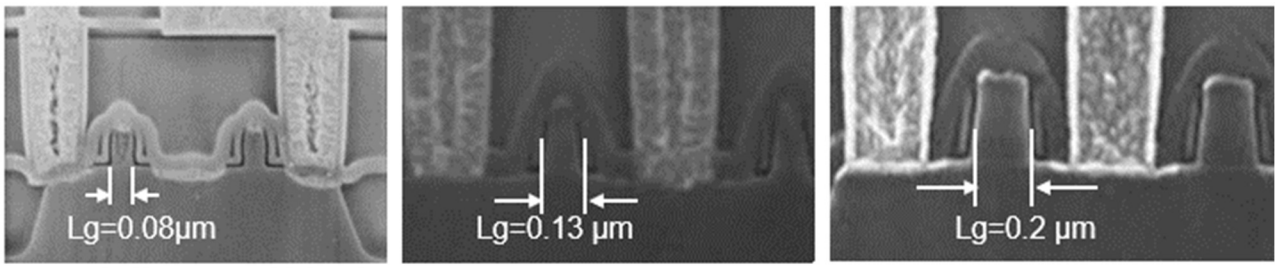
Fig. 2.22. Comparison of thermal budgets needed to form the 0.25 μm Si BJT and the 0.18 μm SiGe HBT [4][8].

for SiGe epitaxial growth was less than that of N_2 annealing for forming the intrinsic base layer of the 0.25 μm generation Si BJTs. Furthermore, the thermal budget in the SiGe HBT formation process was reduced in other processes as well. The effect of the temperature difference between 800 ºC and 700 ℃ on the amount of diffusion could be estimated to be equivalent to a one-digit difference in terms of diffusion time from the difference in impurity diffusion coefficient [9]. Including the waiting time after inserting the wafer into the equipment, a furnace process usually takes several hours, so even if the temperature is 680 ℃, the thermal budget could be greater than the single-wafer process at 800 ℃. Therefore, switching from the LP-CVD process to the HDP process was one of the effective means for reducing the thermal budget in the HBT formation process. The SiGe HBT process has a lower temperature for the intrinsic base formation than the Si BJT process, and it was considered necessary to select the SiGe HBT process when incorporating fine CMOS into the BiCMOS process.

2.6 Confirmation of Scalability that Enables the Installation of 0.13 μm CMOS in the BiCMOS

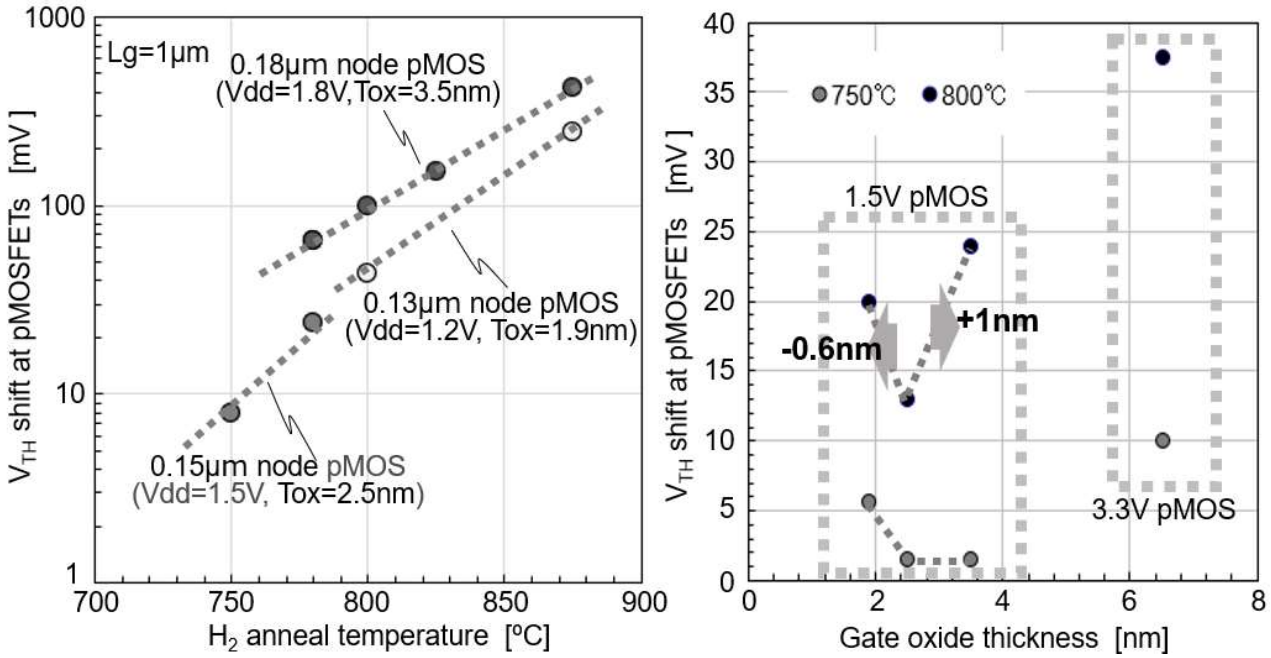
This section shows that the fine CMOS from the 0.13 μm to 0.18 μm generations could be incorporated into the SiGe BiCMOS while maintaining short-channel characteristics by using the low-thermal-budget SiGe HBT process. This study used the 0.18 μm SiGe BiCMOS as the base process. The scalability to 0.13 μm was examined by modifying the gate length, gate oxide thickness, and impurity profile of the base 0.18 μm process (Fig. 2.23). If the V_{TH} shift due to boron penetration was within 0.1 V, it was considered that it could be controlled by adjusting the implanted dose into the channel, and the H_2 annealing condition before the SiGe epitaxial growth was set at 780 ℃ for two minutes.

Fluctuations in PMOS characteristics due to H_2 annealing occurred at all nodes (Fig. 2.24). The variation of V_{TH} was more minor in the 0.13 μm PMOS with a thin gate oxide layer of 1.9 nm than in the 0.18 μm PMOS with a 3.5 nm thickness. Because the channel doses have increased as the fine process progresses (Phosphorus dose in the 0.13 μm node was 5×10^{12} cm^{-2}, that in the 0.18 μm node was 1.8×10^{12} cm^{-2}), it was thought that it became less susceptible to the boron penetration. In addition, no significant layer thickness dependence was observed in the V_{TH} shift amount from evaluation results of the dependence of the gate oxide layer thickness on the 0.15 μm PMOS (Fig. 2.24(b)). Unlike boron diffusion by N_2 annealing, boron diffusion by H_2 annealing was presumed to be rate-determined by the supply of hydrogen molecules.



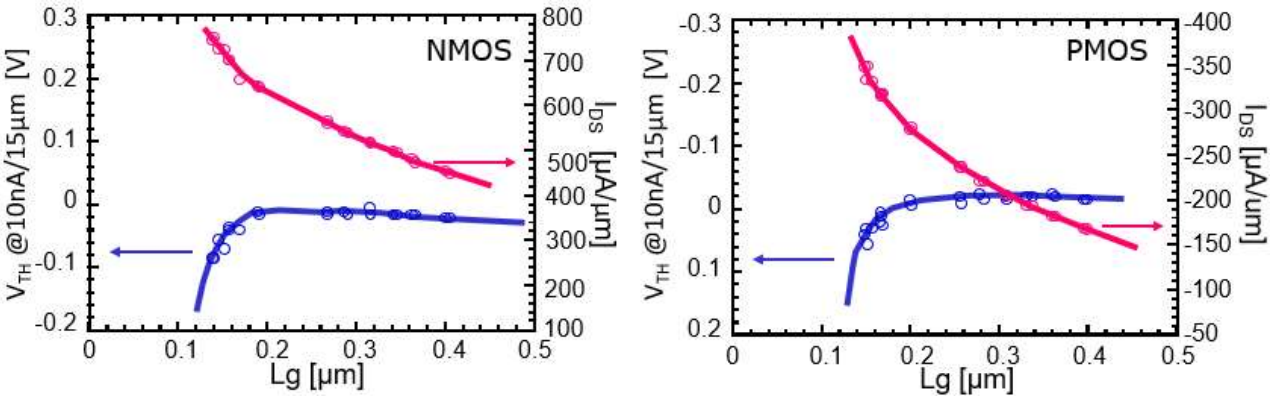
(a) 0.13 μm node	(b) 0.15 μm node	(c) 0.18 μm node
V_{DD}/T_{OX}= (1.2 V/1.5 nm)	(1.5 V/2.5 nm)	(1.8 V/3.5 nm)

Fig. 2.23. Cross-sectional SEM photograph of CMOS (0.18 μm node and 0.15 μm node are MOS in SiGe BiCMOS, 0.13 μm node is a substitute for MOS formed by CMOS process). V_{DD}: Supply voltage, T_{OX}: Gate oxide thickness.



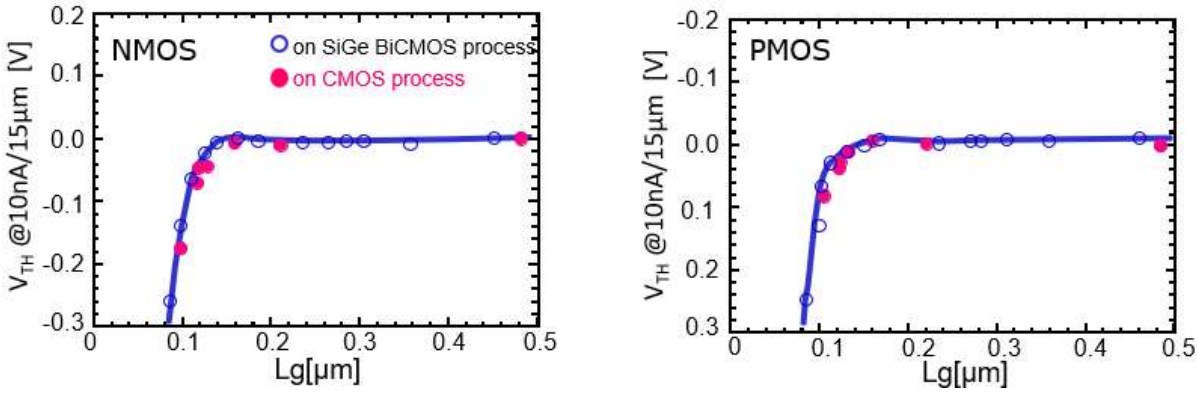
(a) Node dependence of V_{TH} shift (b) Gate oxide dependence of V_{TH} shift

Fig. 2.24. PMOS V_{TH} shift due to boron penetration accelerated by the H_2 annealing.



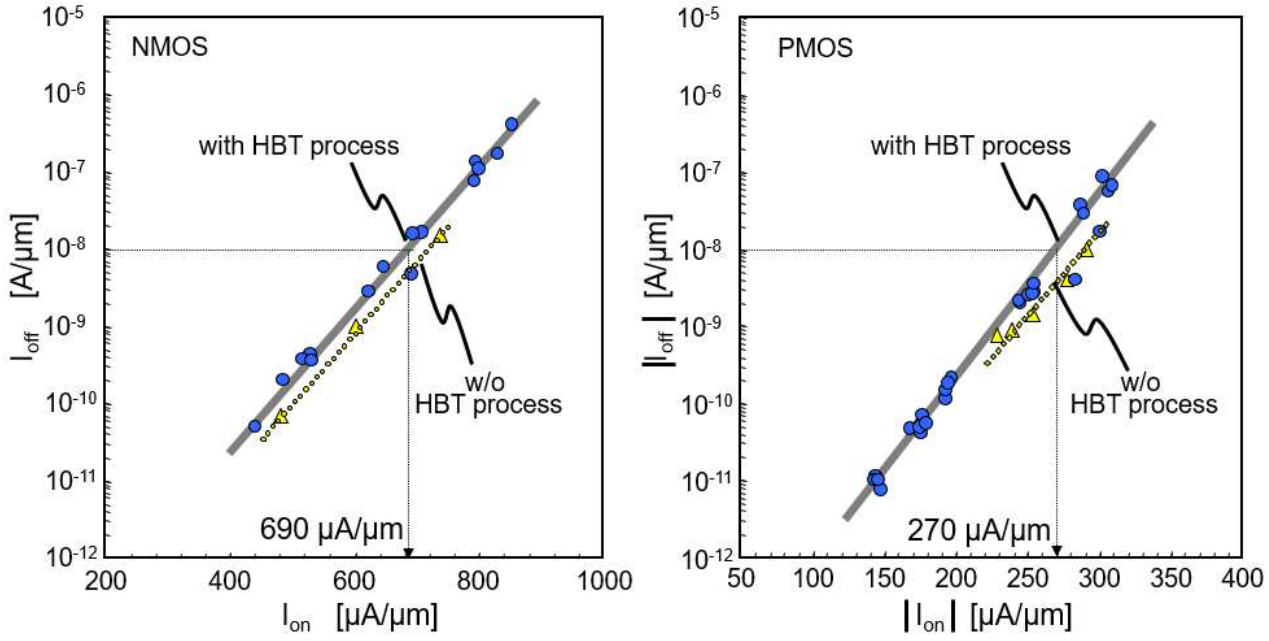
(a) NMOS (b) PMOS

Fig. 2.25. Gate length (L_g) dependence of V_{TH} and I_{DS} for the 0.18 μm CMOS (V_{DD}=1.8V, Lg=0.2μm).



(a) NMOS (b) PMOS

Fig. 2.26. Gate length (L_g) dependence of V_{TH} and I_{DS} for the 0.15 μm CMOS (V_{DD}=1.5V, Lg=0.12μm).



(a) NMOS, Gate length (Lg)=80 nm, V_{DD}=1.2 V (b) PMOS Gate length (Lg)=80 nm, V_{DD}=1.2 V

Fig. 2.27. Compare the 0.13 μm CMOS I_{on}-I_{off} characteristic between CMOS and SiGe BiCMOS processes.

No degradation of MOS short channel characteristics due to the SiGe HBT process was observed in the characterization of the 0.18 μm CMOS (Fig. 2.25) and the 0.15 μm CMOS (Fig. 2.26). In addition, the Ion-Ioff correlation in the 0.13 μm node CMOS showed little difference between the presence and absence of the SiGe HBT process, and it was obtained results that the thermal budget in the SiGe HBT formation process had almost no influence on the MOS characteristics (Fig. 2.27).

2.7 Conclusions

Process and layout rule of BiCMOS technology up to the 0.25μm generation has prioritized bipolar transistors. However, using the vast amount of CMOS IP has become an essential key to applying BiCMOS technologies to various applications, and it was examined in this study that the BiCMOS process was constructed while minimizing the modification of CMOS characteristics.

(1) The height of the SiGe HBT was suppressed according to an interlayer dielectric thickness of the standard 0.18 μm CMOS by reducing the thickness of each layer that makes up the double poly-Si self-aligned structure. In addition, the SiGe BiCMOS process was constructed not to modify the design rule of the CMOS part by matching the alignment tree in the lithography process to the CMOS process. Although the device size became more extensive than that of the layout rule when priority was given to bipolar transistors, it will be described in Chapter 4 that the device performance of f_T and f_{MAX} of 250 GHz or more was achieved.

(2) The boron-doped p-type gate has been used for the PMOS gate from the 0.18 μm generation, and the accelerated boron diffusion during H_2 annealing before SiGe epitaxial growth became an issue. H_2 annealing at 875 ℃ for two minutes changed the PMOS Vth by 0.42 V. The process conditions for the forming and maintaining hydrogen terminations on the Si surface were clarified, and the oxide layer on the base poly-Si

electrode was changed from the thermal CVD layer to the HDP layer to minimize moisture desorption from the oxide layer. The device yield was maintained by applying these process conditions at 99.99993 %, even at limiting the H_2 annealing temperature before epitaxial growth to 760 ºC.

(3) About 180 seconds of over-etch was needed after the pad oxide layer disappeared on the substrate surface to complete the hydrogen termination formation by dilute hydrofluoric acid wet cleaning. The relationship between device yield and process conditions has revealed that reliable hydrogen termination formation was necessary for lowering the temperature of H_2 annealing before SiGe epitaxial growth. In particular, the device with a larger emitter size was more susceptible to changes in process conditions even if the total area evaluation was much smaller. It was indicated that the H_2 annealing temperature and hydrogen termination formation conditions should be determined based on the yield of devices with a large emitter size.

(4) The thermal budget to form the SiGe HBT was reduced from that of the Si BJT process by switching from a batch process to a single-wafer process. As a result, conventional countermeasures for the deterioration of short channel characteristics, such as extending the gate length, are no longer necessary. Furthermore, the SiGe BiCMOS technology was constructed based on the 0.18μm process, but almost the same characteristics as the CMOS single process was obtained with the minimum adjustment of the channel dose even at each node of 0.15μm and 0.13μm. The SiGe BiCMOS with scalability down to the 0.13μm CMOS was established by the low thermal-budget technology of the SiGe HBT formation process.

2.8 References

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3. Selective SiGe Epitaxial Growth Technology for Intrinsic Base Layer

3.1 Introduction

The performance of Si-based bipolar transistors has been improved by the double-polysilicon self-aligned BJT structure and shallow junction formation, as described in Chapter 1. The self-aligned structure has been an effective means of reducing parasitic capacitance and resistance because the separation distance between E-B (Emitter-Base) electrodes can be determined without depending on the alignment accuracy of lithography technology [1]–[6]. Techniques for shallow junctions in the intrinsic base layer include a combination of low-acceleration ion implantation of BF_2 and RTA or the RVD (Rapid Vapor Phase Doping) process. The RVD finally realized f_T =100 GHz with a Si BJT [6][7]. However, the upper limit of the Si BJTs was about f_T=100 GHz, and the SiGe HBT technology has rapidly expanded its applications since the 2000s, mainly for high-speed communication applications. The concept of HBT was conceived from the early stages of the development of bipolar transistors [8][9], and SiGe HBTs have been rapidly developed for practical application with the maturation of SiGe epitaxial growth technology using the UHV-CVD (Ultra High Vacuum-Chemical Vapor Deposition) or the LP-CVD (Low-Pressure CVD).

There have been two types of SiGe epitaxial growth of blanket growth and selective growth, and there have also been two types of SiGe HBTs of the non-self-aligned and the self-aligned device structures (Fig. 3.1). It has been necessary to secure a separation distance between the emitter and extrinsic base that matches the alignment accuracy of lithography in the case of a combination of the blanket epitaxial growth and the non-self-aligned type.

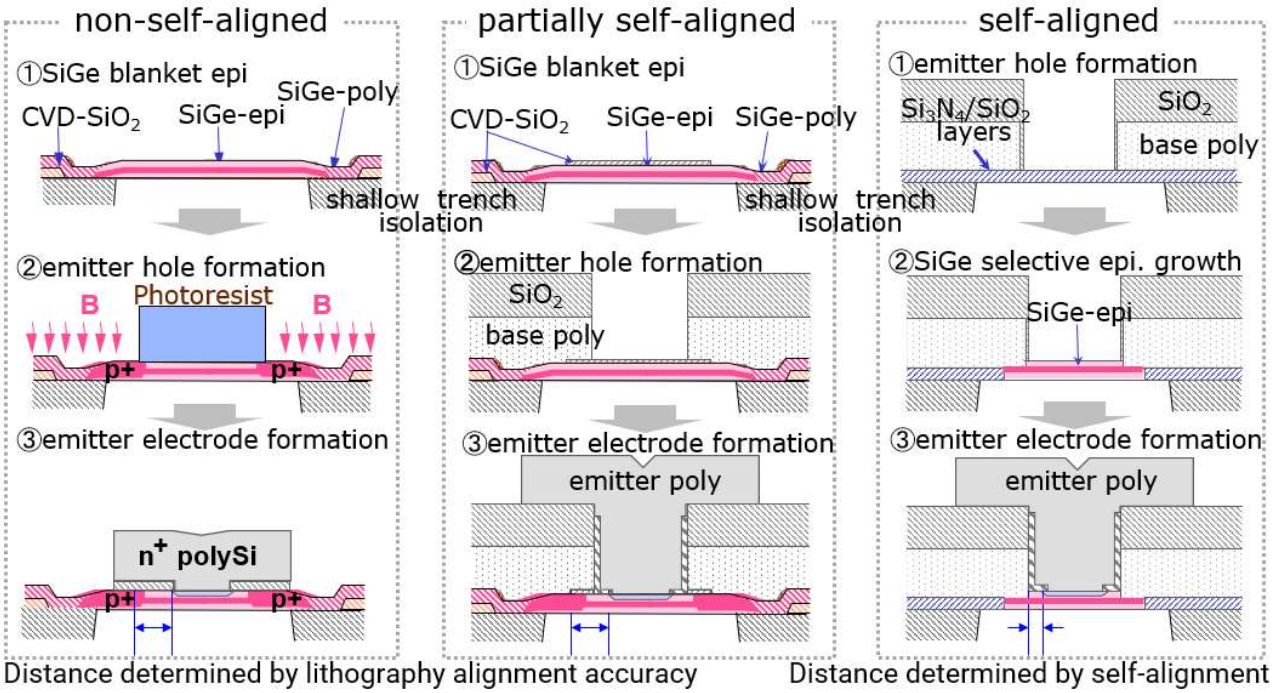


Fig. 3.1. SiGe HBT process flow comparison with different structures.

This structure shall increase the collector parasitic capacitance and base resistance, compared with the self-aligned structure. A self-aligned structure can be partially achieved even with the blanket growth, but the separation distance between the emitter and extrinsic base cannot be a self-aligned structure, so there is concern about an increase in base resistance. As mentioned in Chapter 1, while IBM and others stopped fining bipolar transistors in the 0.5 μm generation, this study continued to improve the performance of the self-aligned structure by combining it with fine technologies. A combination of the selective epitaxial growth technology and the self-aligned device structure was chosen to maintain its superiority.

This chapter discusses the results of this study on maintaining selectivity in the SiGe epitaxial growth technology and increasing the concentration of Ge and boron.

3.2 Challenges in the SiGe Epitaxial Growth

The following challenges as SiGe epitaxial growth technology were examined in this study, including lowering the process temperature so as not to affect the CMOS characteristics, as mentioned in Chapter 2.

(i) Realizing the self-aligned structure by forming the link region that connected the base poly-Si electrode and the intrinsic base layer during the selective epitaxial growth process step, and lowering the thermal budget of the selective epitaxial growth process to minimize the impact on the CMOS characteristics.

- Establishment of the selective SiGe epitaxial growth technology by minimizing the use of HCl gas.

(ii) Formation of boron and Ge profiles in SiGe epitaxial growth layer to improve device characteristics.

- Increase the boron concentration and reduce the layer thickness for f_T increasing and BV_{CEO} keeping.
- Generation of the carrier acceleration electric field by increasing Ge concentration in the step-type Ge profile.
- Suppression of boron diffusion during the final RTA by carbon doping.

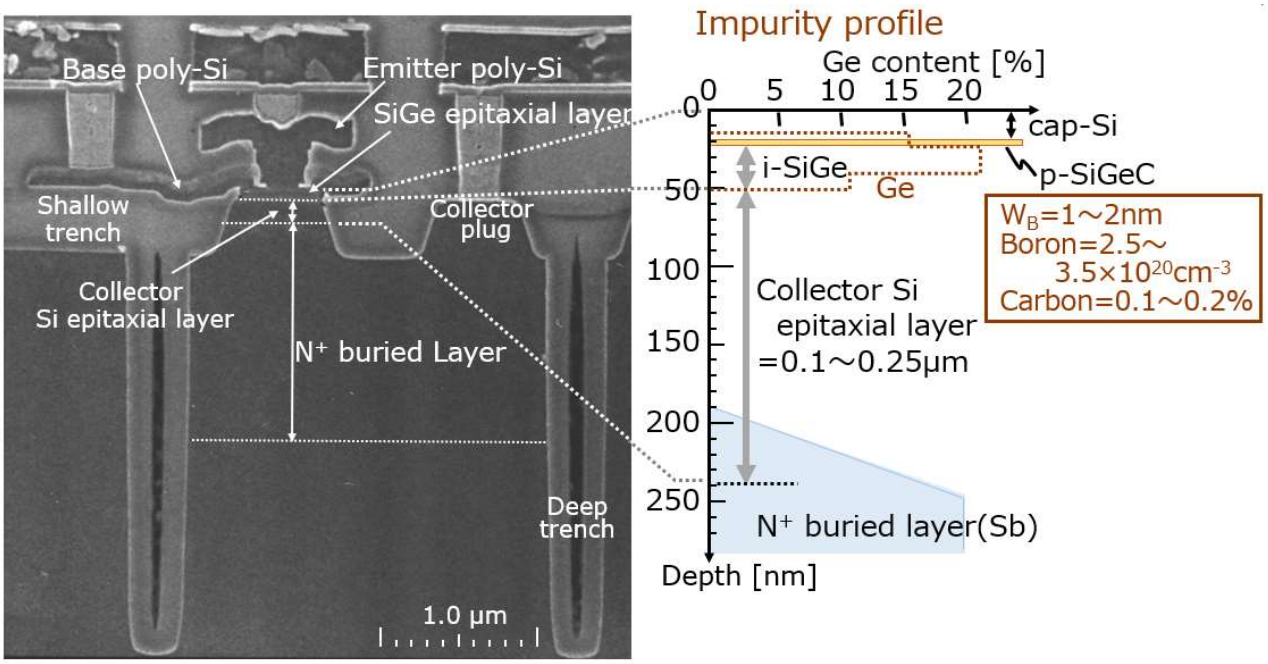


Fig. 3.2. SEM cross-sectional view of the 0.18 μm based SiGe HBT and schematics of impurity profile in as-grown SiGe layer. The cross-section of the sample was slightly wet etched using diluted HF [14].

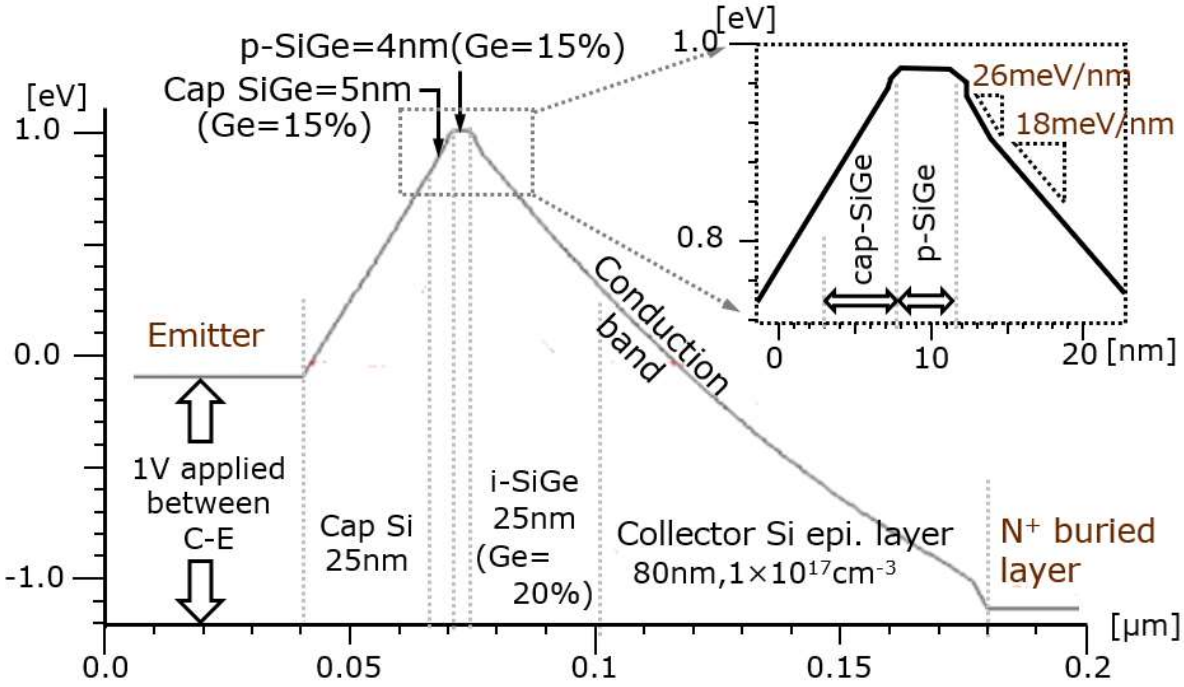


Fig. 3.3. Conduction band simulation (Synopsys Taurus Medici) results in SiGe HBT with the step-type Ge profile.

Other research institutes have achieved higher frequencies by generating a carrier acceleration electric field in the neutral intrinsic base layer by using the graded-type Ge profile. However, since the epitaxial growth rate fluctuates depending on the Ge concentration, there needs to be more concern about maintaining the reproducibility of forming the graded-type Ge profile in the production stage. Furthermore, it took much work to determine the layer thickness of the graded-type Ge profile, making it difficult to establish a method for immediate quality monitoring. Therefore, this study adopted the step-type Ge profile as a pseudo-graded-type Ge profile (Fig. 3.2) [10]. At the step-type Ge profile, it could be possible to monitor the layer thickness and impurity concentration by dividing into the three layers ((i) cap-Si layer, (ii) p-SiGeC layer, (iii) i-SiGe layer) according to the difference in Ge concentration, so quality monitoring in the production phase has become more accessible. The device simulation (Synopsys Taurus Medici) showed that the slope of the conduction band just under the intrinsic base layer became steeper at the step-type Ge profile by raising the Ge concentration from 15 % in the p-SiGeC layer to 20 % in the i-SiGe layer (Fig. 3.3). It was expected that a sharp slope in the conduction band in the i-SiGe layer just under the p-SiGeC would reduce the electron transit time.

Here, the purposes of each selective SiGe epitaxial growth layer are as follows.

- Cap-Si layer: Emitter diffusion layer formation by phosphorus diffusion from the emitter poly-Si layer
  Maintaining BV_{EBO}
- p-SiGeC layer: Intrinsic base layer formation (N_B=2.4-3.5×10^{20} cm^{-3}) Maintaining f_T, rbb', BV_{CEO}
- i-SiGe layer: Carrier acceleration electric field generated by increasing the Ge concentration higher than in the p-SiGeC layer Maintaining f_T

3.3 Ensuring Selectivity in the SiGe Epitaxial Growth

3.3.1 Overview of SiGe Epitaxial Growth Process that Realized the Self-aligned Structure

This study utilized the 0.25-0.13 μm process developed for 200-mmφ Si(100) wafers production line. As shown in the formation flow of the emitter/base region in Chapter 2 (Fig. 2.4), stacked layers of SiO_2/Si_3N_4/*in-situ* boron-doped poly-Si/SiO_2 were deposited from the bottom. Furthermore, after processing two layers of SiO_2 and *in-situ* boron-doped poly-Si in the upper layer of the stacked layers by a dry etching technique, a thermal oxide layer was formed on the side of the emitter hole. Afterward, the stacked layers of Si_3N_4/SiO_2 were wet-etched to perform an overhang structure under the base poly-Si electrode. Furthermore, a Si/SiGe layer was selectively grown on the exposed Si substrate in the emitter hole using Applied Materials Centura® Epi, a single-wafer low-pressure CVD system.

As described in Section 2.4.1, H_2 blowing at 35 ℓ/minute in 15 Torr and HCl etching gas suppressed boron retention in the chamber and prevented the boron memory effect in the LP-CVD system. SiH_2Cl_2 and GeH_4 were used as the source gas, B_2H_6 as the boron dopant gas, and 1 % CH_3SiH_3/H_2 as the carbon doping gas.

In this study, the thickness of the Si/SiGe layer was evaluated by SEM/TEM cross-sectional photographs and Spectroscopic Ellipsometry (NanoSpec® 9300, Nanometrics Inc.). Carbon concentration was evaluated by SIMS (Secondary Ion Mass Spectrometry), and SIMS and Spectroscopic Ellipsometry evaluated Ge concentration. SIMS and sheet resistance measurement indirectly evaluated boron concentration by the four-terminal van der Pauw pattern. When the emitter size was 0.2×1 μm^2, the size of the emitter hole was 0.35×1.35 μm^2 considering the poly-Si sidewall (SW) length. This was too small to be evaluated by SIMS or Spectroscopic Ellipsometry, and an open area of 400 μm□ was prepared as a test pattern (TEG, Test Element Group) to evaluate impurity concentration. The emitter holes did not occupy a large area in the bipolar transistor layout, and there was no product in which the bipolar transistors filled the chip. The total area of the emitter holes on the wafer was less than 0.1 % of the wafer in any product.

3.3.2 Selective SiGe Epitaxial Growth without HCl Gas Addition

The addition of HCl gas could improve the selectivity during the epitaxial growth of Si and SiGe layers, but increasing the amount of HCl gas shall reduce the growth rate (Fig. 3.4). In addition, the activation energy (Ea) obtained from the temperature dependence of the growth rate was 48 kcal/mol at 740 ℃ or higher, but the growth rate decreased at 720 ℃ or lower, and Ea increased to 64 kcal/mol at 10 mℓ/minute of HCl and to 95 kcal/mol at 40 mℓ/minute. On the other hand, it maintained 48 kcal/mol even below 700 ℃ without HCl. Because the bond energy of Si-Cl is 92 kcal/mol [20], the Si-Cl bond's desorption rate was considered rate-limiting at 40 mℓ/minute of HCl. On the other hand, the bond energy of Si-Si is 37 kcal/mol, and that of Si-Ge is 49 kcal/mol. Si-Si and Si-Ge bonds were determined to be rate-limiting in the absence of HCl. There was a 50 ℃ difference in growth temperature to achieve the same growth rate of 10 nm/minute compared to no HCl and an HCl flow rate of 40 mℓ/minute, and there was a 10-fold difference in growth rate between 40 mℓ/minute of HCl gas and no HCl gas at a growth temperature of 680 ℃. It was needed to minimize the HCl flow rate to reduce the thermal budget to minimize MOS characteristic fluctuations and to maintain an appropriate single-wafer process throughput.

On the other hand, in the SiGe epitaxial growth, there is an incubation time from the start of the raw material gas supply to the beginning of the SiGe layer growth. The incubation time was longer on the nitride layer than on

the Si substrate, and even longer on the oxide layer (Fig. 3.5). When the SiGe layer grows to a thickness of 110 nm on a Si substrate, the SiGe layer did not grow on the oxide layer even without HCl gas. When a SiGe layer with a thickness of 400 nm or more was grown, the selectivity was broken in a part starting from the nucleus on the oxide layer. Even though hillocks grew, there was no blanket growth (Fig. 3.6). Because the thickness of the epitaxial growth layer is actually as thin as about 60 nm, it was judged that the possibility of occurrence of hillocks

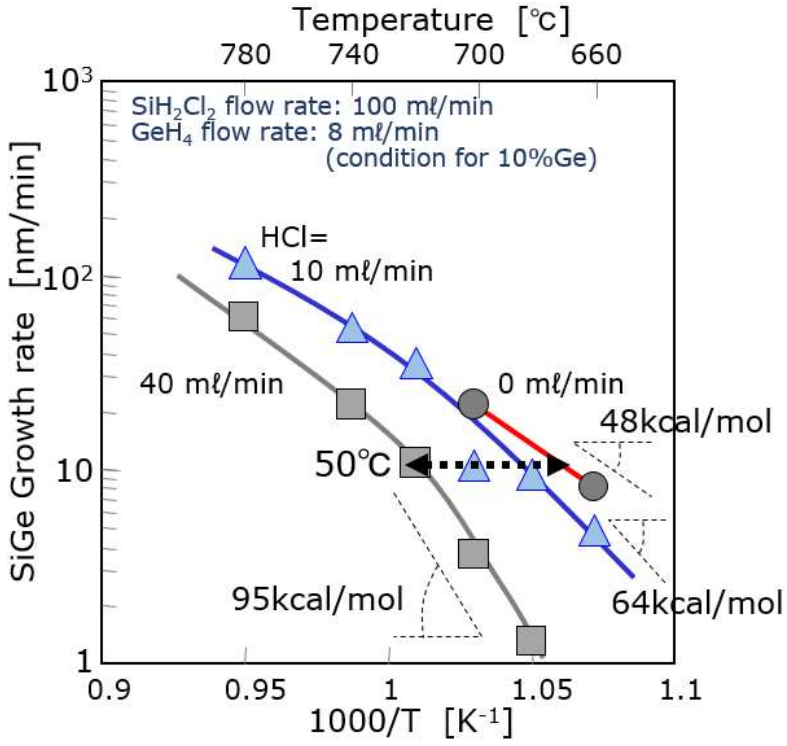


Fig. 3.4. Dependence of SiGe growth rate on HCl flow rate and temperature.

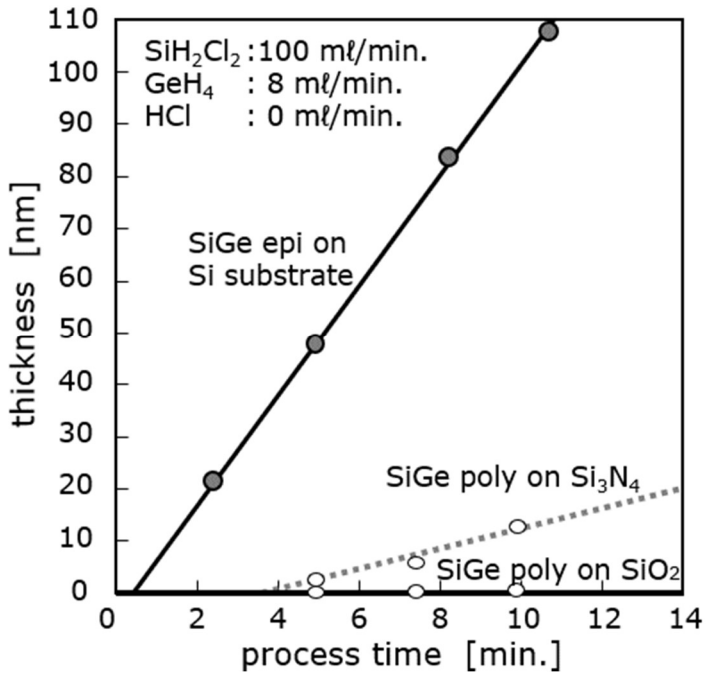


Fig. 3.5. Surface condition dependence of SiGe growth rate.

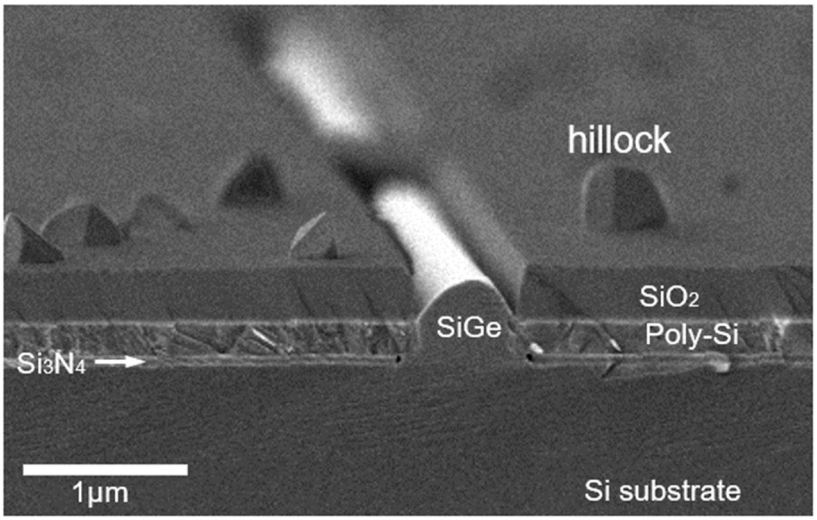
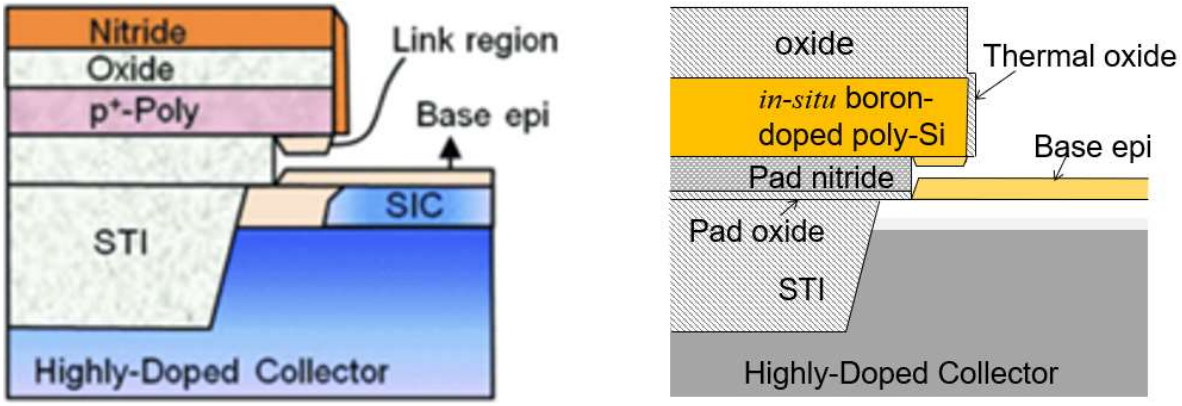


Fig. 3.6. SEM observation result after thick SiGe layer growth.



(a) SiGe HBT structure of IHP [19] (b) SiGe HBT structure of this work

Fig. 3.7. Comparison of SiGe HBT's cross-sectional schematic during SiGe layer growth.

was realistically low. It was found that the selectivity between the oxide layer and the Si substrate can be maintained only with Cl in the raw material SiH_2Cl_2, and the process conditions were such that HCl was not added by using an oxide layer as the protecting layer covering the base electrode.

Other research institutes have often chosen a nitride layer to cover the base electrode during the selective SiGe epitaxial growth (Fig. 3.7(a)). This is because it is necessary to protect the oxide layer on the base poly-Si and on the side walls at the same time when removing the oxide layer directly below the base poly-Si electrode in the emitter hole formation process. In this structure, it was presumed from data in Fig. 3.5 that HCl gas is necessary to suppress the SiGe layer growth on the nitride layer during selective growth. On the other hand, the nitride layer was directly below the base electrode in the structure adopted in this study (Fig. 3.7(b)), and a thin pad oxide layer was required right under the nitride layer to prevent Si etching with hot phosphoric acid. The oxide layer could be applied to cover the base electrode by thinning the pad oxide layer and minimizing HF etching, and the addition of the HCl gas in the selective SiGe epitaxial growth was made unnecessary.

3.3.3 Formation of Link Region in the Cavity under the Base Poly-Si Electrode

In the SiGe HBT structure in this study, the intrinsic base region and the base poly-Si electrode were connected in a self-aligned manner in the cavity just below the base poly-Si electrode during the SiGe epitaxial growth. This cavity was formed by lateral penetration of hot phosphoric acid etching into the Si_3N_4 layer. At the epitaxial growth process step, the poly-SiGe layer growing from the bottom surface of the base poly-Si electrode and the SiGe layer

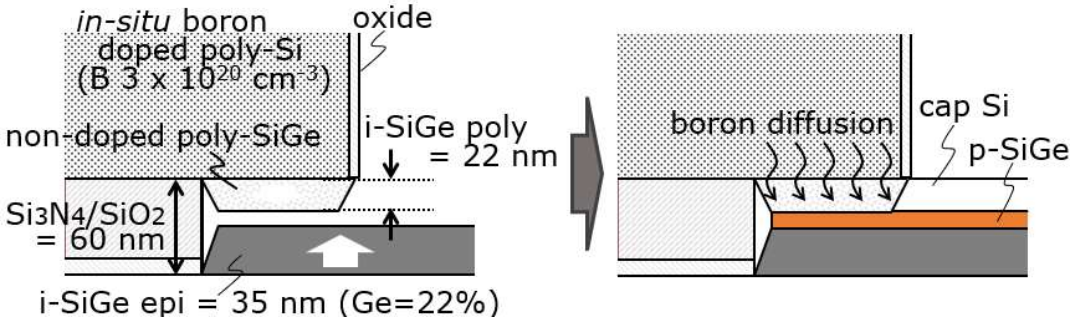
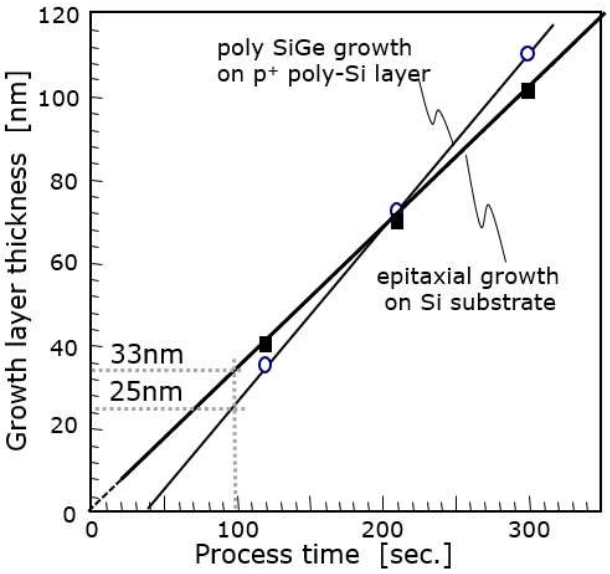
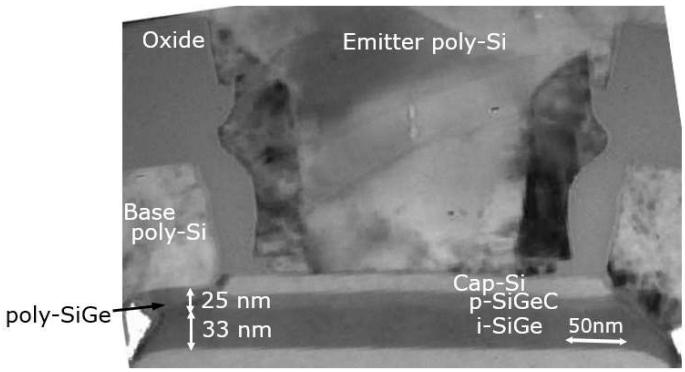


Fig. 3.8. Schematic diagram of connecting base layer formation in the cavity directly below the base poly-Si electrode (after i-SiGe layer formation → after completion of selective growth including cap-Si layer).

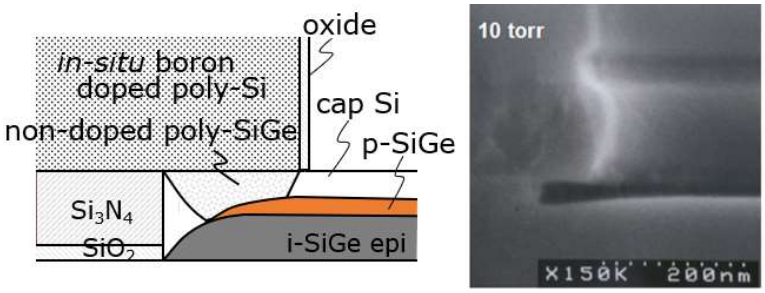


(a) SiGe epitaxial growth rate on a Si substrate and poly-Si layer

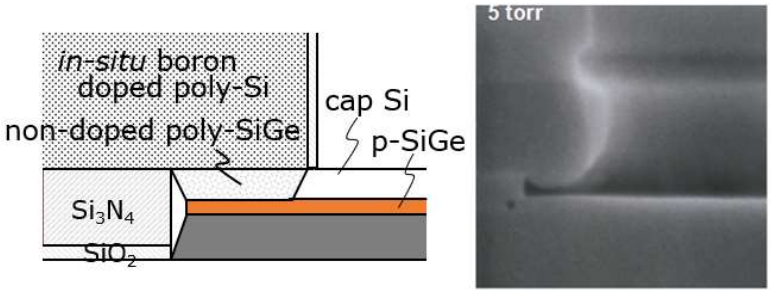


(b) Cross-sectional TEM photograph of SiGe HBT

Fig. 3.9. Comparison of SiGe-epitaxial growth rate on Si substrate and SiGe-poly growth rate on p^+ poly-SiGe layer.



(a) Process pressure during SiGe epitaxial growth was 10 Torr



(b) Process pressure during SiGe epitaxial growth was 5 Torr

Fig. 3.10. Cross-sectional structure of the contact region with SiGe growth layer just below the base electrode.

growing on the Si substrate surface were physically connected. After that, boron molecules were diffused into the poly-SiGe layer from the base poly-Si electrode by annealing, and the base poly-Si electrode was electrically connected to the p-SiGeC layer (Fig. 3.8). On the Si substrate, the SiGe epitaxial growth started faster than on the boron-doped poly-Si layer. This difference in incubation time could suppress the thickness of the non-doped poly-SiGe layer, and it could be thought to contribute to the low resistance of the connecting base region (Fig. 3.9).

On the other hand, the thickness of the i-SiGe layer on the Si substrate became thin in the inner part of the cavity at the growth pressure of 10 Torr in the LP-CVD (Fig. 3.10). Therefore, there was concern that the distance between the p-SiGeC layer and the base poly-Si electrode would become wider at the outer periphery. A flat i-SiGe layer could be formed by reducing the pressure to 5 Torr or less, and a reliable connecting base region could be performed in the cavity with a height of 60 nm (Fig.3.8).

3.4 Study on SiGe layer Specifications to Improve SiGe HBT Performance

This study investigated the following three points regarding the SiGe epitaxial growth to improve the SiGe HBT performance.

(i) Increasing Ge concentration in the i-SiGe layer to the extent that crystallinity can be maintained.

(ii) Increasing boron concentration up to the solid solubility limit.

(iii) Carbon doping to keep the boron-doped layer thin even after the final RTA.

Thinning the p-SiGeC layer and increasing the concentration of Ge improve f_T, and increasing the boron concentration prevents a decrease in BV_{CEO} due to the punch-through even if the layer was made thinner.

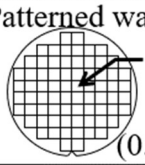
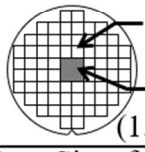
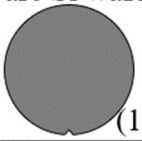
3.4.1 Concentration Increase of Ge and Boron in the SiGe Layer

(1) Pattern dependence of Ge and boron concentration in the SiGe layer

Between patterned wafers and bare Si wafers, boron concentrations in p-SiGe layers differed by a factor of 4-

23 times, the Ge concentration by 1.4 to 3.2 times, and the growth rate by 2.1 times (Table 3.1, Figs. 3.11, 3.12). Here, a 400-μm□ pattern was used to evaluate the p-SiGeC epitaxial growth layer on the patterned wafer with an oxide layer. In the patterned wafer, 99.9 % was covered with an oxide layer, and the Si substrate was exposed only to the emitter hole of the SiGe HBT. The p-SiGeC epitaxial growth area on the patterned wafer was limited to 0.1 % of the total, and it was thought that the supply speed limiting of the raw material gas caused the concentration

Table 3.1. Pattern dependence for p-SiGe epitaxial growth.

Measurement pattern (epi. growth area/wafer ratio)	Growth rate [nm/min]	Boron concentration [cm^{-3}]	Ge content [%]
Patterned wafer 	7.4	9.7×10^{20}	10.3
Patterned wafer 	7.2	—	10.1
	3.6	6.6×10^{19}	7.7
Bare Si wafer 	3.5	4.3×10^{19}	8.2

The number in parentheses indicates the ratio of the total area where the Si substrates were exposed.
Conditions: 660 ºC, pressure=5 Torr, SiH_2Cl_2=100 mℓ/min., HCl=0 mℓ/min., B_2H_6=10 mℓ/min., GeH_4=6.3 mℓ/min.

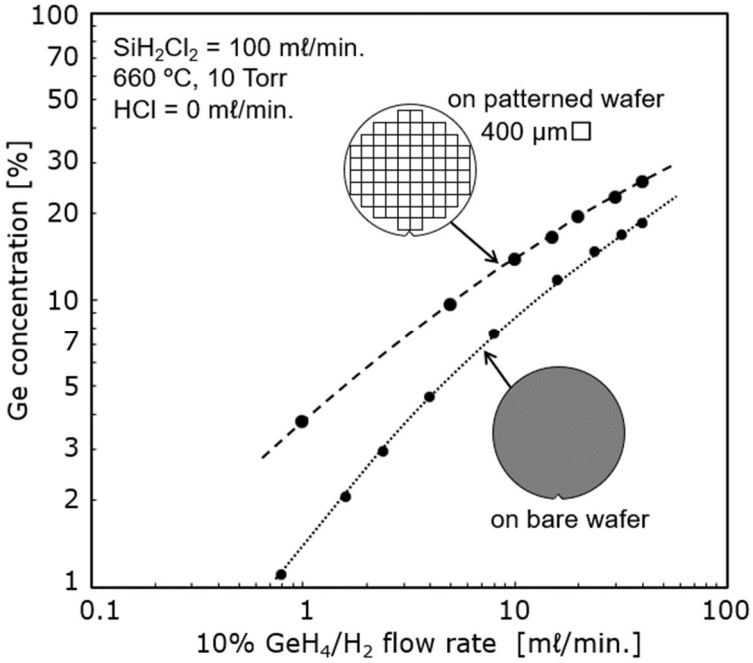


Fig. 3.11. GeH_4 flow rate dependence for Ge concentration.

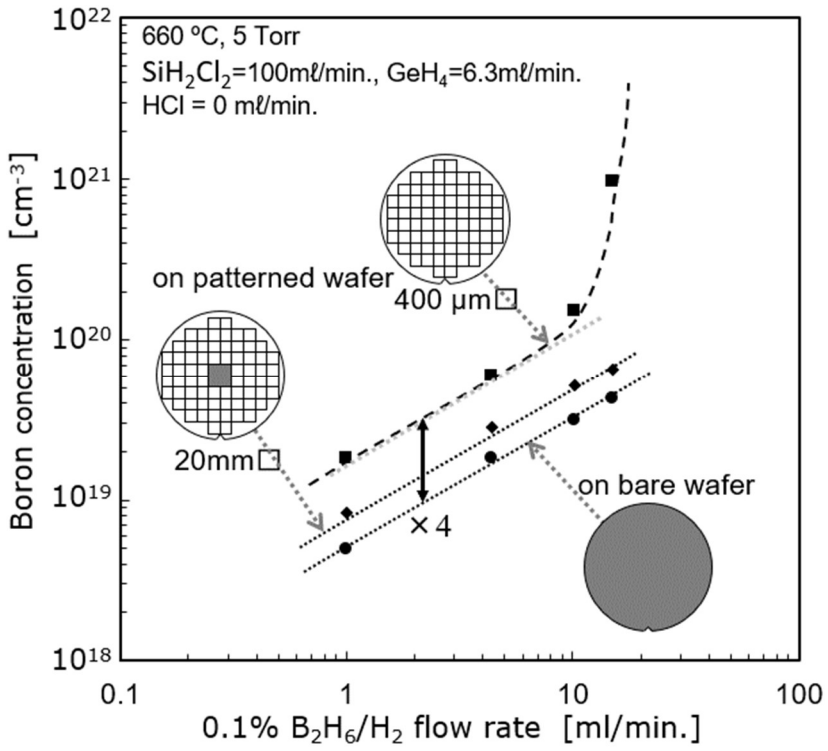


Fig. 3.12. B_2H_6 flow rate dependence for boron concentration.

difference. Even in comparison to the same wafer, in the region where the Si substrate was exposed to the chip size (20 mm□), the result was almost the same as that of the Si bare wafer. Because the mean free paths of boron and Ge molecules are two to three orders of magnitude shorter than the tip size, it was estimated that the supply of boron and Ge molecules could not keep up with the large open area despite the Si molecules maintaining surface reactions. On the other hand, in the 400 μm□ region, it was presumed that the concentration increased due to the supply of unreacted boron and Ge from the surrounding oxide layer. Because the growth rate depends on the Ge concentration, it was presumed that the difference in Ge concentration resulted in the difference in the growth rate.

It is challenging to perform SIMS analysis in an area of 100 μm□ or less, and there is no way to directly measure the impurity concentration in a small area. In addition, even Si BJTs based on a base layer forming method by ion implantation have size dependence on device characteristics, so it is difficult to analogize the size dependence of base impurity concentration from device characteristics of SiGe HBTs. Therefore, this study used the evaluation result of SIMS analysis with a 400-μm□ pattern as the boron concentration.

TEM observations between 0.35×1.35 μm^2 and 400 μm□ revealed no size dependence of the growth rate due to the local loading effects on hole size. Because there was no difference in the growth rate of the SiGeC layer, it could be indirectly thought that the impurity concentration did not have a significant dependence on the emitter hole size of less than 400 μm□.

(2) Suppression of crystallinity deterioration of SiGe layer at high concentration of Ge

When the Ge concentration becomes excessive, island-like crystal growth begins to reduce the stress produced by the mismatch between Ge and Si, resulting in an uneven shape. Because the lattice constants of Si and Ge are 5.4310 Å and 5.6575 Å respectively, there is a lattice mismatch of 4.17 %. Because the epitaxial growth conditions in this study (i-SiGe growth temperature of 680 ℃, layer thickness of 30 nm, Ge concentration of 28 %) was on

boundary condition in which the crystallinity could collapse to become a relaxed state (Fig. 3.13), it was expected that a slight difference in conditions would collapse the crystallinity. In fact, there was surface roughness under the needs of the i-SiGe growth layer thickness of 30 nm and Ge concentration of 30 % (Fig. 3.14(a)). On the other hand, the surface roughness of the i-SiGe layer could be suppressed by inserting a 4-nm-thick i-SiGe layer with a Ge concentration of 10 % under the i-SiGe layer with a high Ge concentration (Fig. 3.14(b)). It was speculated that the low-Ge-concentration i-SiGe layer was between the Si substrate and the Ge-rich layer and served as a buffer layer that relaxed the strain at the interface. A 20-nm thick i-SiGe layer with a Ge concentration of 30 % could be performed without surface roughening by using a buffer layer as an underlay.

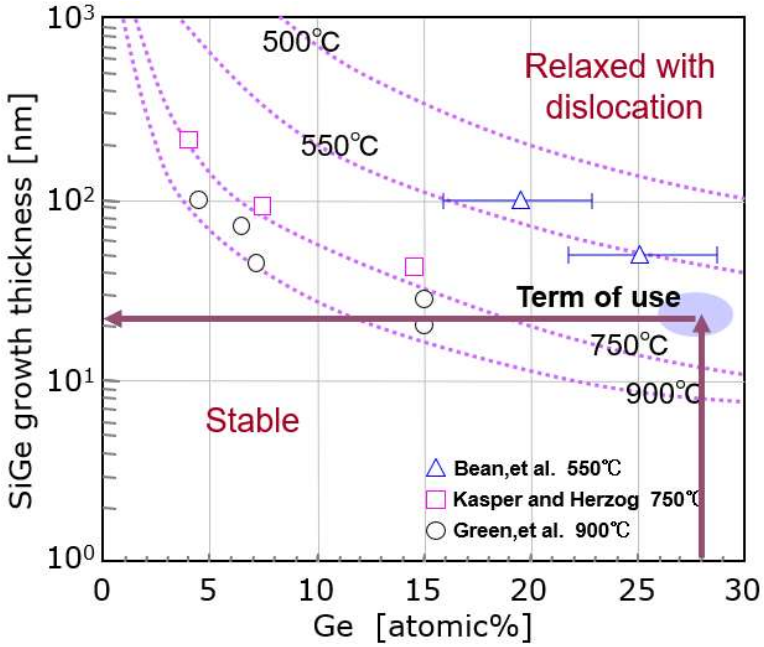
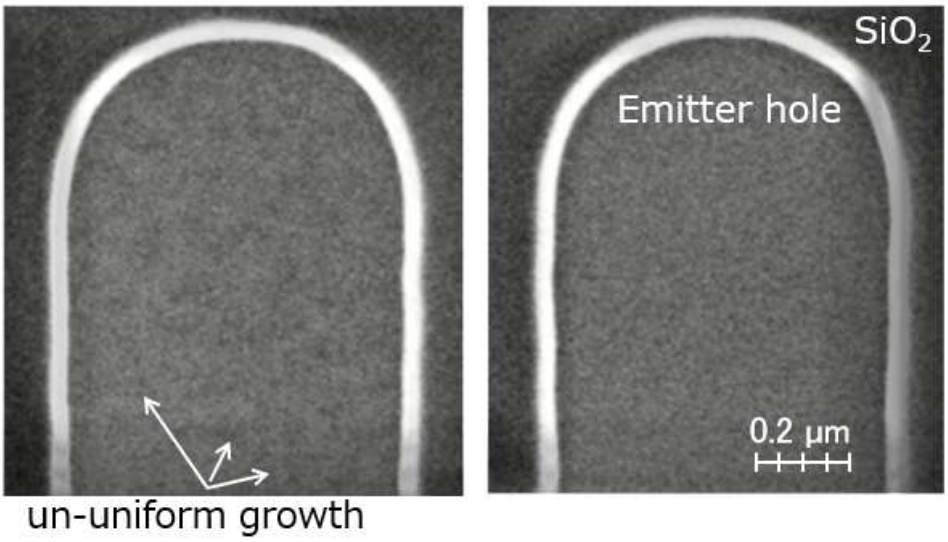
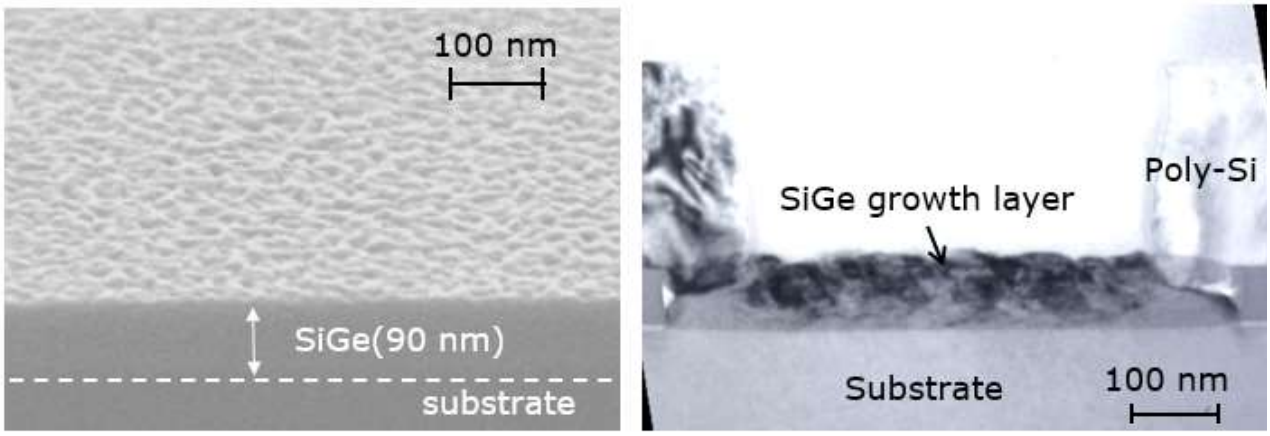


Fig. 3.13. Conditions under which the crystallinity of the SiGe layer formed on the (100) substrate can be maintained. [12]



(a) without the buffer layer (b) with the buffer layer (4 nm, Ge10 %)

Fig.3.14. Plane-view SEM inside emitter hole after SiGe epitaxial growth. The thickness and Ge concentration of the i-SiGe layer are 30 nm and 30 %.



(a) SEM planar view (b) TEM cross-sectional view

Fig. 3.15. SiGe crystallinity evaluation in the case of supersaturation of B_2H_6 gas.

(3) Degradation of crystallinity of SiGe layer due to high boron concentration

In the previous paper [11], it was already reported that the growth surface was roughened by a high flow rate of B_2H_6 gas exceeding 30 mℓ/minute. When the flow rate of B_2H_6 exceeded 10 mℓ/minute (Fig. 3.12), boron concentration sharply increased. Here, the crystallinity collapsed in the sample where the boron concentration increased rapidly (Fig. 3.15). One reason is that SiGe polycrystals grow with boron clusters acting as nuclei when the boron concentration becomes too high. Another reason is that the crystallinity of the epitaxially grown layer collapsed due to the occurrence of lattice mismatch due to the incorporation of excess boron into the SiGe layer.

(4) Raising the boron concentration to the solid solubility limit

The sheet resistance of the intrinsic base layer of the SiGe HBT was measured by forming the Van der Pauw pattern by independently connecting the four corners of the external poly-Si base while making use of the device structure. Here, the emitter and collector were set to 0 V. Although there are lot-to-lot variations, a result was obtained close to the impurity concentration dependence of p-type Si described in the literature [13] (Fig. 3.16, the literature values: dashed line in the figure). When compared within the same lot, no decrease in resistivity was observed from 6×10^{20} cm^{-3} to 8×10^{20} cm^{-3}, and it was estimated that the solid solubility limit of boron was reached at 6×10^{20} cm^{-3}. Also, the sheet resistance decreased by 30 % by raising the final RTA temperature from 875 ℃ to 1000 ℃ for both poly-Si and SiGe layers (Fig. 3.17). Although it was unclear whether all the impurities were activated at 1000 ℃, the activation rate of boron at 875 ℃ was estimated to be 70 % or less at least.

The width of the neutral region becomes narrow due to the extension of the depletion layers on both the emitter and collector sides in the intrinsic base layer sandwiched between the emitter layer and the collector layer. Therefore, the sheet resistance of the intrinsic base layer is called the "pinch base resistance" (ρ_{ebs}). Here, the following equation expresses the relationship between the depletion layer width and the impurity concentration in the PN junction.

$$N_D/N_A=lp/ln \tag{3.1}$$

N_D: Donor concentration ln : Layer width of the n-type region depletion

N_A: Acceptance concentration lp : Layer width of the p-type region depletion

According to the above formula, the extension of the depletion layer is determined by the reciprocal of the impurity concentration ratio of the n-type layer and the p-type layer. Boron peak concentration was on the order of 10^{18} cm^{-3} in Si BJTs with an intrinsic base layer formed by the boron ion implantation, but the boron concentration was on the order of 10^{20} cm^{-3} in SiGe HBTs with an intrinsic base layer formed by the epitaxial growth technique. The impurity concentration in the collector region was on the order of 10^{17} cm^{-3}, which was three orders of magnitude different from the intrinsic base impurity concentration. Also, the peak impurity concentration on the emitter side

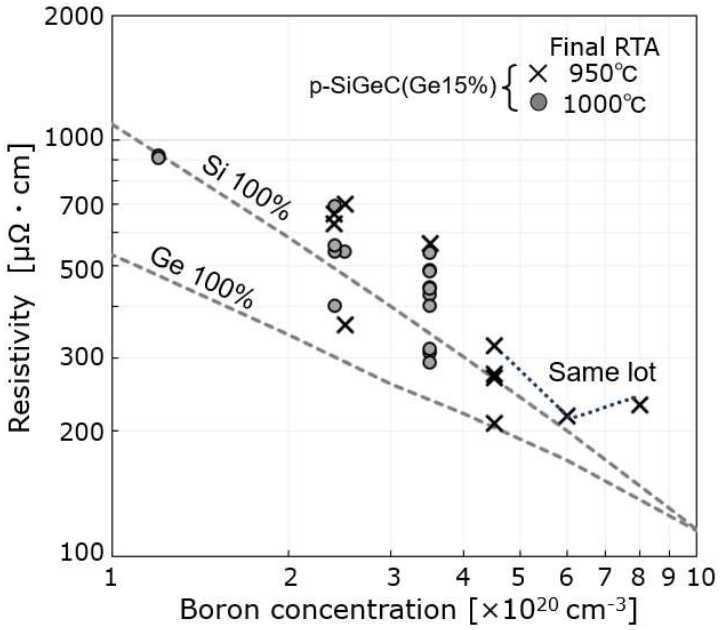


Fig. 3.16. Measurement results of the boron concentration dependence of resistivity of SiGe layer (Ge concentration 15 %). The dashed lines refer to the literature values of Sze [13].

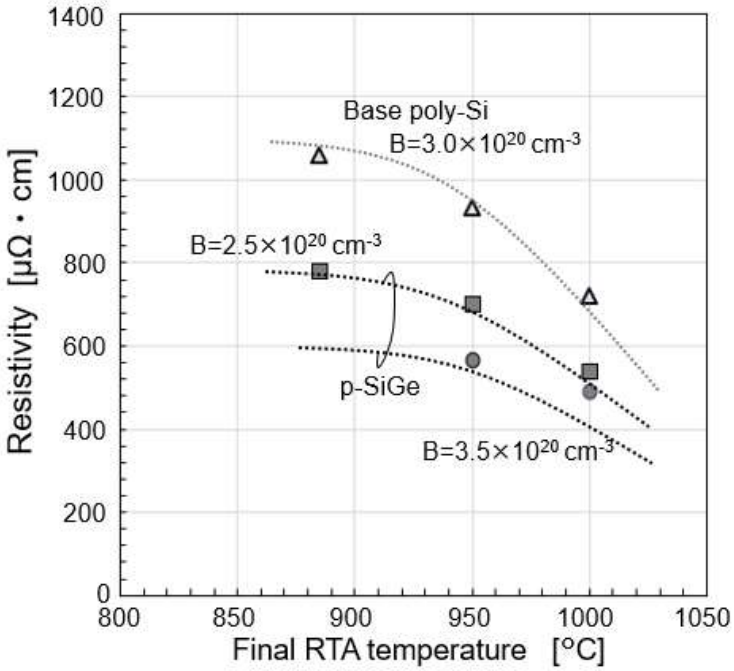
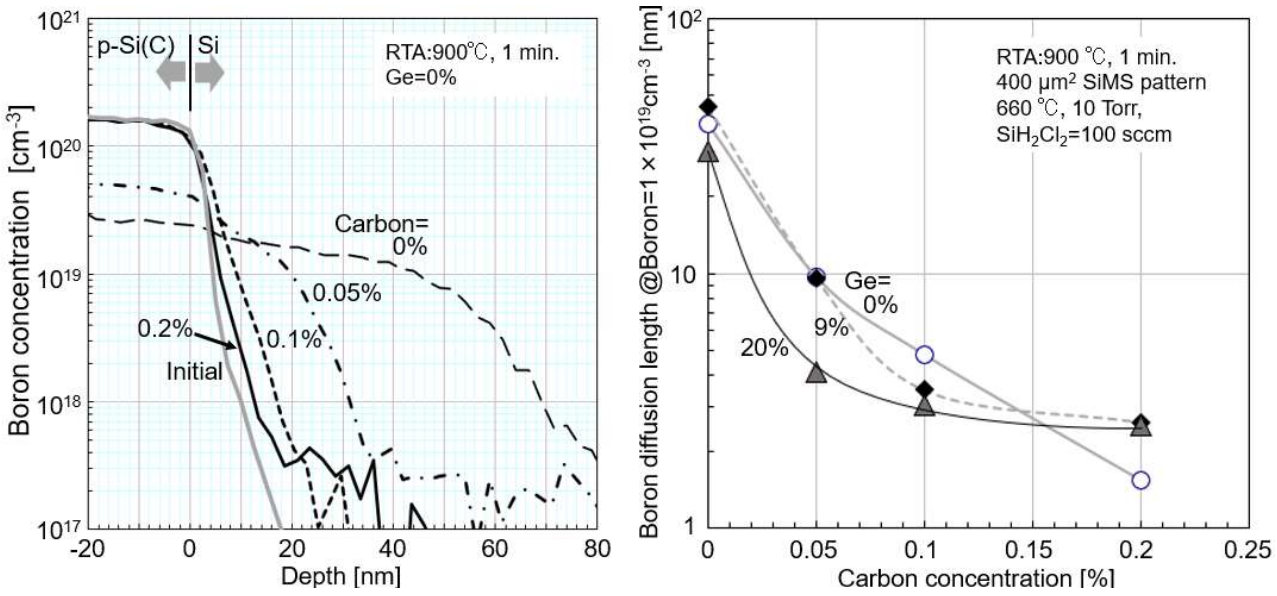


Fig. 3.17. Dependence of SiGe layer resistivity on boron concentration and heat treatment temperature.

was about the same, but the phosphorus on the emitter side should have a graded phosphorus profile due to diffusion from the *in-situ* doped poly-Si layer, so it could be assumed that the impurity concentration at the Emitter-Base (E-B) junction was higher on the intrinsic base side. From these points, it was considered that most of the intrinsic base layer of the SiGe HBT remained in the neutral region without extending the depletion layer.

3.4.2 Suppression of Boron Diffusion by Carbon Doping

Other papers have already reported that carbon doping could suppress boron diffusion [14][15]. The boron diffusion of 40 nm or more was observed without the carbon doping when the sample was annealed at 900 ℃ for 1 minute. This annealing time was six times longer than the actual annealing time. 0.05 % of the carbon doping suppressed boron diffusion to about 1/3, and 0.1 % suppressed it to about 1/6. The addition of 0.2 % carbon further suppressed the boron diffusion (Fig. 3.18(a)). Since only the boron-doped layer was carbon-doped, the boron diffusion after diffusing into the cap-Si layer or the i-SiGe layer could not be suppressed. It was considered that the diffusion length could have been shortened by suppressing the significant boron diffusion from the heavily boron-doped layer. In addition, the Ge concentration of 9 % did not affect the boron diffusion, but the boron diffusion distance was shortened at the Ge concentration of 20 % (Fig. 3.18(b)). Ge concentration of about 20 % was the amount assumed for doping the i-SiGe layer, and it was expected that the boron diffusion on the collector side would be suppressed more than on the emitter side.



(a) Boron diffusion profile from p-SiGeC layer (b) Boron diffusion length

Fig. 3.18. SIMS evaluation results of boron diffusion from p-SiGeC layer depending on carbon and Ge concentration. Diffusion length was defined as the distance of difference from the initial, where the amount of boron was 1×10^{19} cm^{-3}.

3.5 Conclusions

The selective SiGe epitaxial technique was developed and applied to the SiGe HBT process to retain the device characteristics advantage of the self-aligned bipolar transistor structure.

(1) HCl gas addition has been frequently used for selective epitaxial growth. In this study, the selectivity was maintained with only the main gas of SiH_2Cl_2 without adding HCl by covering the base electrode with an

oxide layer that can lengthen the incubation time to the SiGe growth start than with a nitride layer. It was possible to lower the temperature by 50 ℃ compared to when the HCl flow rate was 40 mℓ/minute by not using HCl gas to maintain the same growth rate.

(2) Thinning the SiGe growth layer in the cavity just under the base poly-Si electrode was suppressed by reducing the pressure during the formation of the i-SiGe layer from 10 Torr to 5 Torr, and the link region connecting the base poly-Si electrode and the intrinsic base layer was strengthened.

(3) The concentrations of boron and Ge in the p-SiGeC layer depended on the epitaxial growth area. There was a difference of 4 to 23 times in the boron concentration and 1.4 to 3.2 times in the Ge concentration between the case of forming on the entire wafer surface and the case of performing on a 400-μm□ area. 400 μm□ was used as the evaluation pattern for standard measurement in this study, and by fixing the evaluation pattern, the generation of measurement errors due to size dependence in monitoring during mass production was eliminated.

(4) Device simulation results were obtained for the conduction band in which an accelerating electric field for electrons was expected even in the step-type Ge profile. It was challenging to monitor the layer thickness and Ge concentration in the conventional graded-type Ge profile during production. Therefore, the step-type Ge profile was adopted in this study.

(5) Ge concentration could be increased to 30 % by inserting the buffer layer (10 % Ge), and this buffer layer suppressed the deterioration of crystallinity due to lattice mismatch with Si.

(6) The crystallinity could be maintained up to a concentration of 8×10^{20} cm^{-3}, but the decrease in the sheet resistance was saturated at 5×10^{20} cm^{-3}. It was expected that the base resistance reduction due to high concentration would be limited to 5×10^{20} cm^{-3}. In addition, 0.1-0.2 % carbon doping suppresses the boron diffusion, and the thinning of the intrinsic base layer is expected.

3.6 References

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4. Study on Improvement of Frequency Characterization on SiGe HBTs

4.1 Introduction

SiGe HBTs have rapidly advanced to practical application with the progress of the SiGe epitaxial growth technology around 2000. f_T of the SiGe HBTs has improved from the initial 100 GHz to over 300 GHz [1]-[19], and these were applied to the optical and millimeter-wave communications. As with Si BJTs, techniques to improve f_T have included the thinner intrinsic base layer and collector layer and higher impurity concentrations in both layers. In addition, a unique approach for SiGe HBTs has been the graded-type Ge profile to generate an electric field that accelerates electron transport in the intrinsic base layer [1]. In this study, the step-type Ge profile, which can be expected to have the same accelerating electric field, was adopted as a more productive technique.

On the other hand, there have been two techniques for SiGe epitaxial growth: "the blanket epitaxial growth" which forms a SiGe layer on the entire surface of the wafer, and "the selective epitaxial growth" which performs a SiGe layer only on the place where the Si substrate or poly-Si layer is exposed. Selective epitaxial growth is superior to blanket epitaxial growth technology in that it can realize a self-aligned structure without adding complicated processes [8][15][16], and selective growth was adopted in this study.

Furthermore, parasitic capacitance and resistance have been reduced to improve f_{MAX} in SiGe HBTs by incorporating fine technologies such as lithography technology, STI isolation, and salicide technology that CMOS technologies have driven development. This chapter describes the results of studies for improving the f_T and f_{MAX} of SiGe HBTs.

4.2 Items to be Addressed in Higher Frequency Characterization on SiGe HBTs

The following items should have been addressed to increase the device performance of SiGe HBTs, and these were also subjects of research and development in this study.

(1) Applying the advanced form of conventional items examined for Si BJT to SiGe HBT

(i) Improving f_T by thinning the intrinsic base layer.

… Maintaining BV_{CEO} by increasing the boron concentration in the intrinsic base layer and keeping the thickness of a thin intrinsic base layer by carbon doping.

(ii) Improving f_T by thinning the collector layer and increasing the impurity concentration in the collector layer.

(iii) Improving f_{MAX} by raising the final RTA temperature.

(iv) Improving f_{MAX} by narrowing the emitter width.

(2) Items that could not be considered for Si BJTs but could be regarded because of the structure of SiGe HBTs (f_T, f_{MAX} ～250 GHz)

(v) Improving f_T by optimizing the thickness of the cap-Si layer.

… Trade-off between emitter depletion layer transit time reduction and C_{EB} charge/discharge time.

(vi) Improving f_T by generating an accelerating electric field in the step-type Ge profile.

(vii) Improving f_{MAX} and f_T by reducing collector resistance and capacitance.

… Elimination of intermediate STI between collector plug and the intrinsic base region.

Reduction of length of a link region to connect a p-SiGeC layer and a base poly-Si electrode.

(viii) Improvement of f_{MAX} by optimizing i-SiGe layer thickness.

… rbb' reduction**.**

(3) Study items for aiming for f_{MAX} = 500 GHz (described in Chapter 6)

(ix) Improvement of f_{MAX} by shrinkage of the double poly-Si self-aligned structure.

… Reduced the distance between the emitter and the extrinsic base region.

4.3 Comparison of the Intrinsic Base Profile and Characteristics of Si BJT and SiGe HBT

As described in Section 1.2, the reciprocal of f_T can be decomposed into the emitter time constant (τ_E), the charge/discharge time (τ_C) of the collector parasitic capacitance (C_{CB}), the transit time in the intrinsic base region (τ_B) and the transit time in the collector layer (τ_{CSCL}).

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_C + \tau_B + \tau_{CSCL} = \frac{kT}{qI_c} C_{EB} + \left(\frac{kT}{qI_c} + R_C + R_E\right) C_{CB} + \gamma \frac{{W_B}^2}{D_n} + \frac{W_{CSCL}}{2v_{SAT}} \quad (4.1)$$

In the past, emphasis was placed on shortening the third term τ_B and the fourth term τ_{CSCL} to improve f_T, and the impurity profile has been made shallower for this reason. On the other hand, the CR time constant, which is the second term consisting of C_{CB} and collector resistance (R_C), has been a parameter that has been emphasized for shortening the circuit delay time (Fig. 1.16). The intrinsic base profile of SiGe-HBTs was roughly 1/25th in base

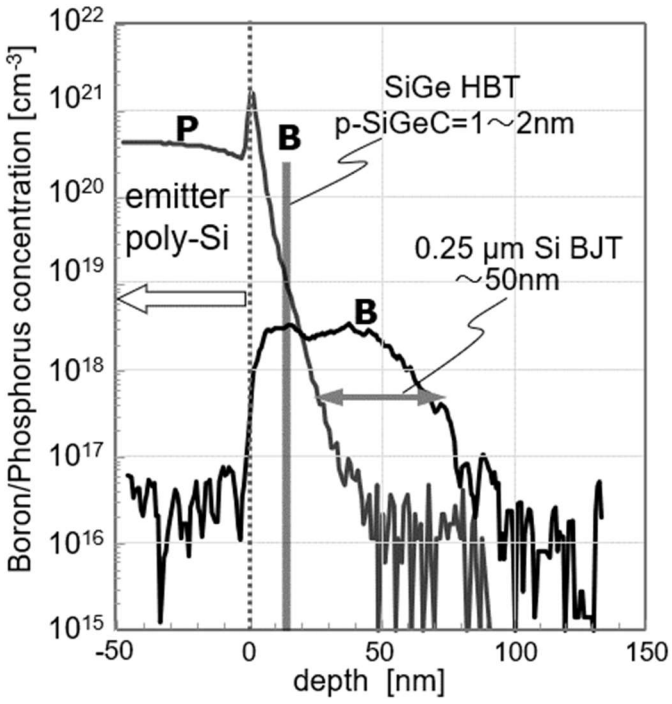


Fig. 4.1. Boron profile compares a Si-BJT and a SiGe HBT.

Table 4.1. Comparison of current gain of Si BJT and SiGe HBT profiles in a representative example in this study.

Device	N_B (cm^{-3})	W_B (nm)	$N_B \times W_B$ ($cm^{-3} \times nm$)	h_{FE}
Si-BJT	3×10^{18}	50	1.5×10^{20}	200
SiGe HBT	3×10^{20}	2	6×10^{20}	500

(Note) N_B: boron concentration, W_B: intrinsic base thickness

thickness and 100 times in concentration compared to Si BJTs, which formed the intrinsic base layer by the ion implantation (Fig. 4.1) (Table 4.1). τ_B was reduced by suppressing the thickness of the intrinsic base layer by order of magnitude. This thin layer was realized by a box-shaped boron profile formed at a low temperature of around 700 ℃ and the carbon doping to suppress the boron diffusion. In addition, the total amount of boron in the intrinsic base layer of the SiGe HBT was four times that of the Si BJT, which was expected to reduce the base resistance.

Here, the current amplification factor (h_{FE}、hybrid Forward Emitter) is the ratio of the electron current (I_{nE}) flowing from the intrinsic base layer to the emitter layer and the hole current (I_{pE}) flowing from the emitter layer to the intrinsic base layer (ratio of equation (4.2) and (4.3)).

$$I_{nE} = qA\frac{ni^2}{G_B}\left(\exp\left(-q\frac{V_{BE}}{kT}\right) - 1\right) \qquad G_B = \frac{N_B W_B}{D_{nB}} \tag{4.2}$$

$$I_{pE} = qA\frac{ni^2}{G_E}\left(\exp\left(-q\frac{V_{BE}}{kT}\right) - 1\right) \qquad G_E = \frac{N_E L_E}{D_{pE}} \tag{4.3}$$

G_B: Base Gummel number, G_E: Emitter Gummel number,
N_B: Impurity concentration in the intrinsic base region, N_E: Impurity concentration in the emitter region
W_B: Intrinsic base region thickness, L_E: Hole diffusion length in the emitter region
D_{nB}: Electron diffusion constant in the intrinsic base region, D_{pE}: Hole diffusion constant in the emitter region

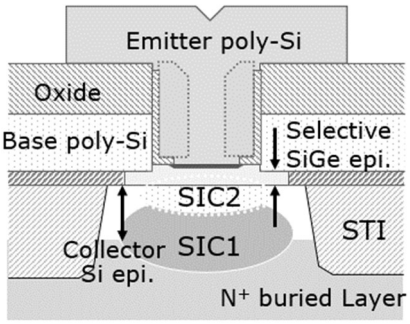
If G_E is constant, h_{FE} is roughly inversely proportional to the total amount of boron ($N_B \times W_B$) in the intrinsic base layer. However, although the SiGe HBT has four times the G_B as compared to the Si BJT, the addition of Ge and the bandgap narrowing by the high boron concentration resulted in an increase of 2.5 times in the h_{FE}.

4.4 Typical SiGe HBT Specifications in This Study

The SiGe HBT examined in this study has three major specifications, "10 Gbps specification" with f_T of about 80 GHz, "40 Gbps specification" with f_T of about 140 GHz, and "100 Gbps specification" with f_T = 200 to 300 GHz (Table 4.2). The 100 Gbps specification was aimed at applications such as 77 GHz band Radar or 100 Gbps optical communication. The boron concentration in the p-SiGeC layer was increased, the collector layer thickness was thinned, and its impurity concentration (SIC1, SIC2) was increased in order from 10 Gbps specification to 40 Gbps specification and 100 Gbps specification. In addition, the final RTA temperature was increased and shortened as generations progressed, as the 10 Gbps specification was intended to be combined with the 0.25 μm CMOS, the 40 Gbps specification with the 0.18 μm CMOS, and the 100 Gbps specification with the 0.13 μm CMOS.

Table 4.2. Representative specifications of SiGe HBTs in this study.

Spec.	cap-Si, -SiGe	P-SiGeC (i-SiGe=22.1%)	collector Si epi.	SIC(Phosphorus) [keV],[cm^{-2}]	final RTA
10Gbps spec.	10nm, 7nm	B≦$1.5\times10^{20}cm^{-3}$ Ge=15.2%, C∼0.1%	0.3μm	SIC1. 200, 5×10^{12} SIC2. 70, 2×10^{12}	885℃ 10sec.
40Gbps spec.	6nm, 4nm	B≧$2.4\times10^{20}cm^{-3}$ Ge=15.2%,C∼0.1%	0.25μm	SIC1. 200, 3×10^{13} SIC2. 60, 6×10^{12}	950℃ 2sec.
100Gbps spec.	13nm, 5nm	B≧$2.4\times10^{20}cm^{-3}$ Ge=15.2%,C∼0.15%	0.15μm	SIC1. 150, 3×10^{13} SIC2. 60, 1×10^{13}	1000℃ 1sec.



On the other hand, the cap-Si layer that determines the depletion layer width between the emitter and intrinsic base layers was thinner in the 40 Gbps specification than in the 10 Gbps specification, but that was thicker in the 100 Gbps specification than in the 40 Gbps specification. This is because the final RTA temperature of 1000 ℃ for one second for the 100 Gbps specification effectively has a higher thermal budget than the 950 ℃ for 2-3 seconds for the 40 Gbps specification.

4.5 Techniques for Higher Frequency as an Extension of Methods Used in Si BJTs

4.5.1 Thinning of the p-SiGeC Layer

(1) Device characteristics dependence on p-SiGeC layer thickness and boron concentration

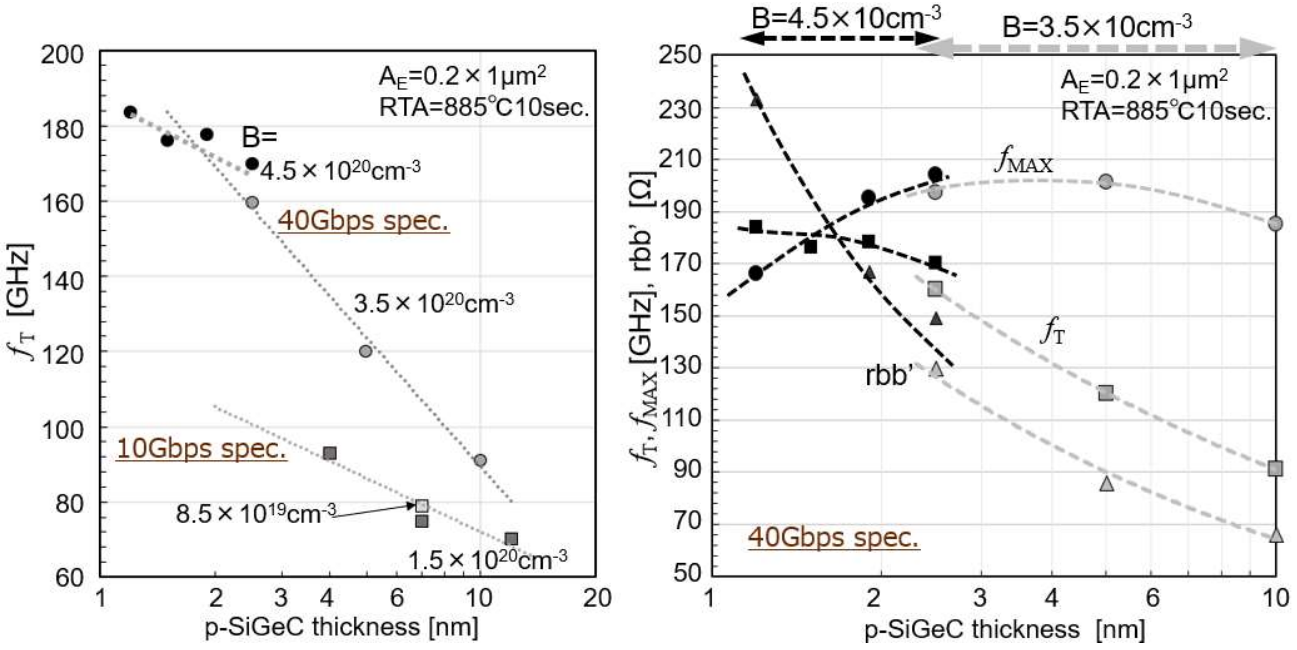
f_T increased by thinning the p-SiGeC layer for both 10 Gbps and 40 Gbps specifications (Fig. 4.2(a)). Furthermore, the 40 Gbps specification had a thinner collector Si epitaxial growth layer than the 10 Gbps specification and increased phosphorus ions implanted into the SIC region, resulting in a higher f_T even with the same p-SiGeC layer thickness. Compared with a p-SiGeC layer with a thickness of 4 nm, f_T improved from 92 GHz to 132 GHz due to the high impurity concentration in the SIC region. On the other hand, even in the 40 Gbps specification, when the thickness of the p-SiGeC layer was 2 nm or less, the f_T improvement slowed down, and it was presumed that terms other than the third term in equation (4.1) became dominant. Here, the relationship between f_T and f_{MAX} is expressed by the following equation.

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi \times C_{CB} \times rbb'}} \tag{4.4}$$

The base resistance (rbb') increased as the thickness of the p-SiGeC layer became thinner, whereas f_T did not increase as much as the thickness of the p-SiGeC layer became thinner than 2 nm, resulting in a decrease in f_{MAX} (Fig. 4.2(b)). It was shown that there was a limit to improving the characteristics only by thinning the p-SiGeC

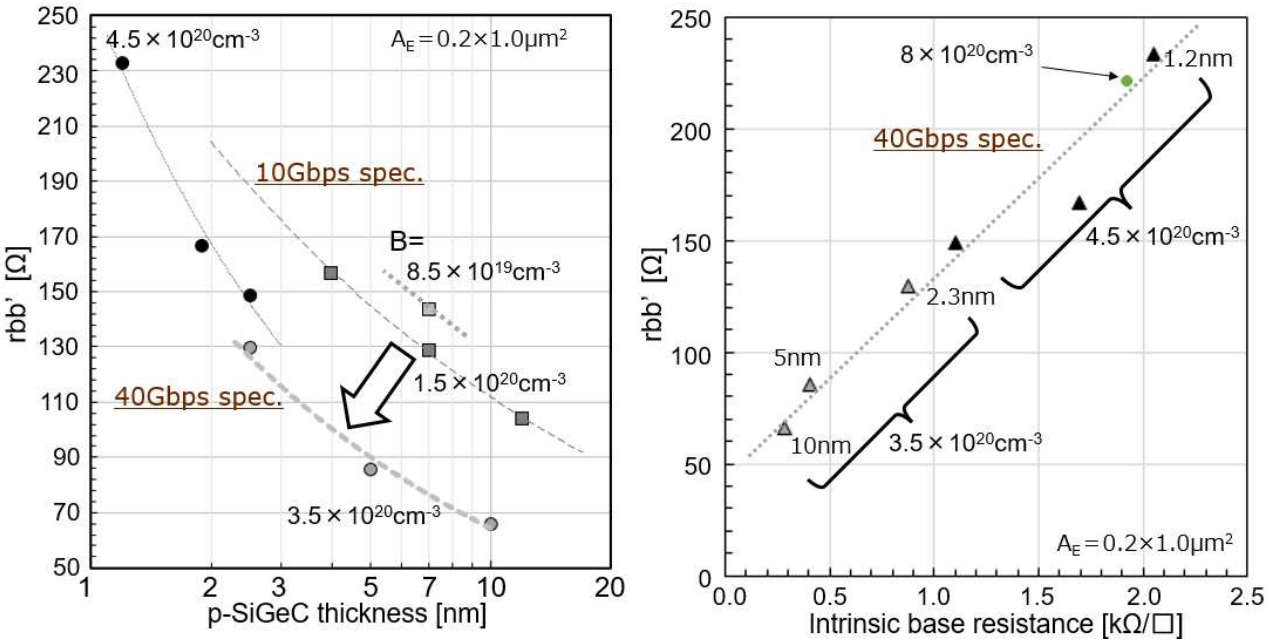
layer.

Next, the effect of increasing the boron concentration in the p-SiGeC layer was examined. For example, rbb' decreased by 42 % from 170 Ω to 98 Ω by increasing the boron concentration from 8.5×10^{19} cm^{-3} to 3.5×10^{20} cm^{-3} when the p-SiGeC layer had a thickness of 3.2 nm (Fig. 4.3(a)). On the other hand, the evaluation of the pinch base resistance (ρ_{ebs}), which is the sheet resistance of the intrinsic base layer in Fig. 3.16, decreased from 1000 μΩ·cm to 500 μΩ·cm was halved by increasing the boron concentration from 8.5×10^{19} cm^{-3} to 3.5×10^{20} cm^{-3}. In addition to the resistance of the intrinsic base layer, the base resistance (rbb') includes the series resistance of the



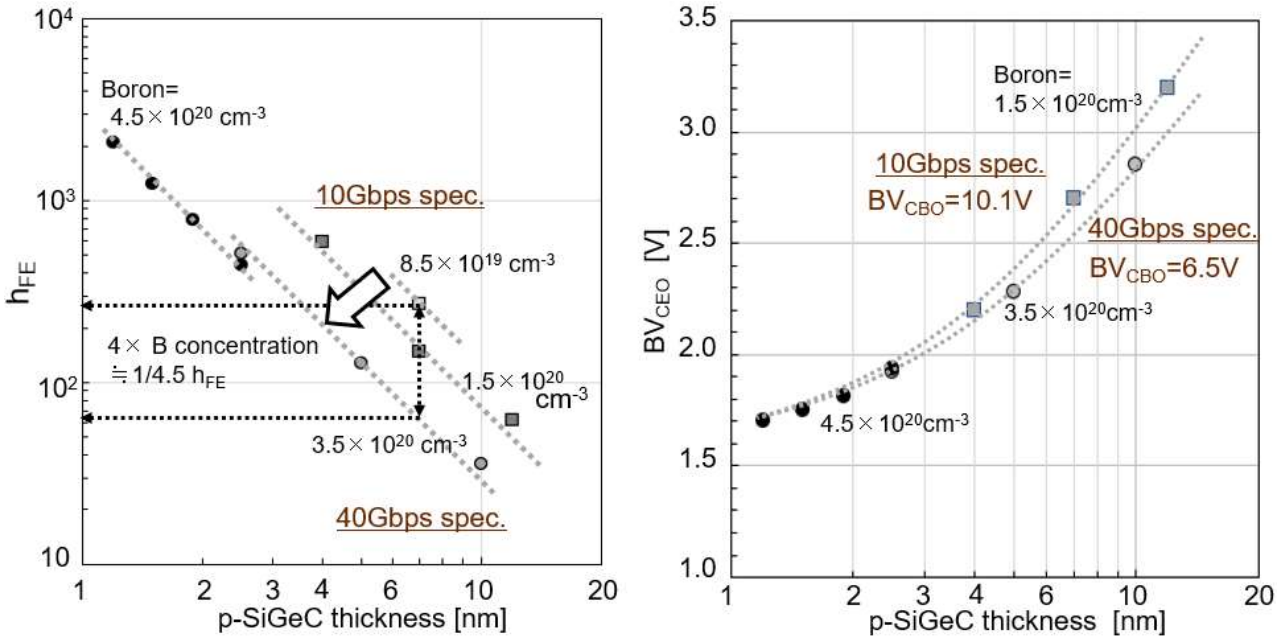
(a) f_T (b) f_{MAX}, rbb'

Fig. 4.2. Dependence of SiGe HBT frequency characteristics on device specifications (Final RTA=885 °C10sec.).



(a) Intrinsic base condition dependence of rbb' (b) Correlation between rbb' and base sheet resistance

Fig. 4.3. Base formation condition dependence of rbb' characteristics of SiGe HBTs (Final RTA=885 °C 10 seconds).



(a) h_{FE} (b) BV_{CEO}

Fig. 4.4. Dependence of SiGe HBT characteristics on p-SiGeC formation conditions (Final RTA=885 ℃ 10 seconds).

base poly-Si electrode and the extrinsic base (the connection between the base poly-Si electrode and the intrinsic base) resistance. The contact resistance with the silicide layer and the base poly-Si layer shall also be included in rbb'. ρ_{ebs} and rbb' were in a proportional relationship, and the parasitic component other than the intrinsic base resistance was estimated to be about 50 Ω from the Y-intercept where the pinch base resistance is zero (Fig. 4.3(b)). It was considered to cause the difference in the reduction rate of rbb' and ρ_{ebs} with increasing boron concentration.

Current gain (h_{FE}) became 1/4.5 by quadrupling the boron concentration from 8.5×10^{19} cm^{-3} to 3.5×10^{20} cm^{-3} (Fig. 4.4(a)). If the bandgap narrowing effect due to high boron concentration was not included, almost all boron molecules of 3.5×10^{20} cm^{-3} were activated and h_{FE} was lowered. On the other hand, even if the concentration was increased from 3.5×10^{20} cm^{-3} to 4.5×10^{20} cm^{-3}, there was no difference in rbb' or h_{FE}, and it was thought that the activation of boron did not progress from 3.5×10^{20} cm^{-3}. Although ρ_{ebs} could be reduced by increasing the concentration up to 5×10^{20} cm^{-3} (Fig. 3.16), rbb' and h_{FE} did not have the boron concentration dependence on the high concentration side like the evaluation with ρ_{ebs}. One of the reasons for the difference in the variation rate between the sheet resistance and the characteristics at 3.5×10^{20} cm^{-3} or more could be thought to be that the impurity activation rate was insufficient due to the final RTA temperature of 885 ℃, but this does not become the reason why the concentration dependence was eliminated at 4.5×10^{20} cm^{-3}. It is possible that the impurity concentration in the device size, which cannot be directly evaluated due to the limitations of SIMS analysis, might have been higher than expected, but the cause has not been identified.

On the other hand, there was no significant difference in the collector-emitter breakdown voltage (BV_{CEO}) between the 40 Gbps specification and the 10 Gbps specification when comparing the same intrinsic base layer thickness (Fig. 4.4(b)). BV_{CEO} is determined by that holes in the electron-hole pairs generated by the applied electric field between the collector and the base (C-B) enter the intrinsic base layer and cause the "Bipolar action." Therefore, the relationship between BV_{CEO} and the Collector-Base breakdown voltage (BV_{CBO}) is expressed by

the equation (4.4).

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{h_{FE}}} \qquad \text{n: constant number} \tag{4.4}$$

In the 40 Gbps specification, the thickness of the collector epitaxial growth layer is thinner, and the impurity concentration is higher, so the BV_{CBO} is lower than the 10 Gbps specification. But at the same time, the h_{FE} is also lowered by increasing the boron concentration, so the numerator and denominator are offset. It could be thought that the BV_{CEO} reached the same level between the two specifications as a result.

(2) Dependence of device yield on the p-SiGeC layer thickness

The Base-Emitter applied voltage (V_{BE}) at which the collector current of 10,000 SiGe HBTs connected in parallel was 100 μA was proportional to the logarithm of the intrinsic base thickness (W_B) (Fig. 4.5). This trend was suited with the relationship between V_{BE} and W_B expressed by equation (4.2). The sensitivity of V_{BE} to a 10 %

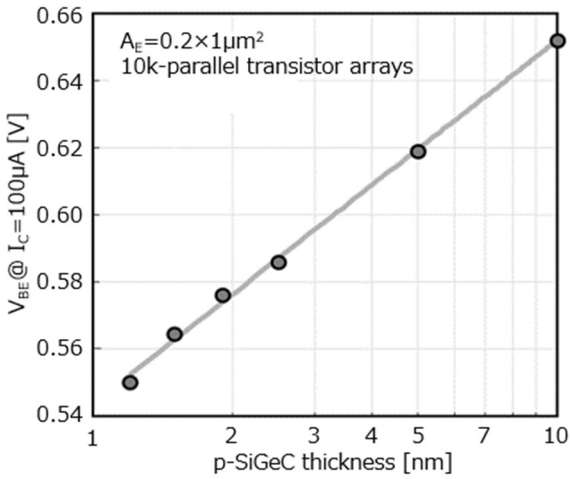
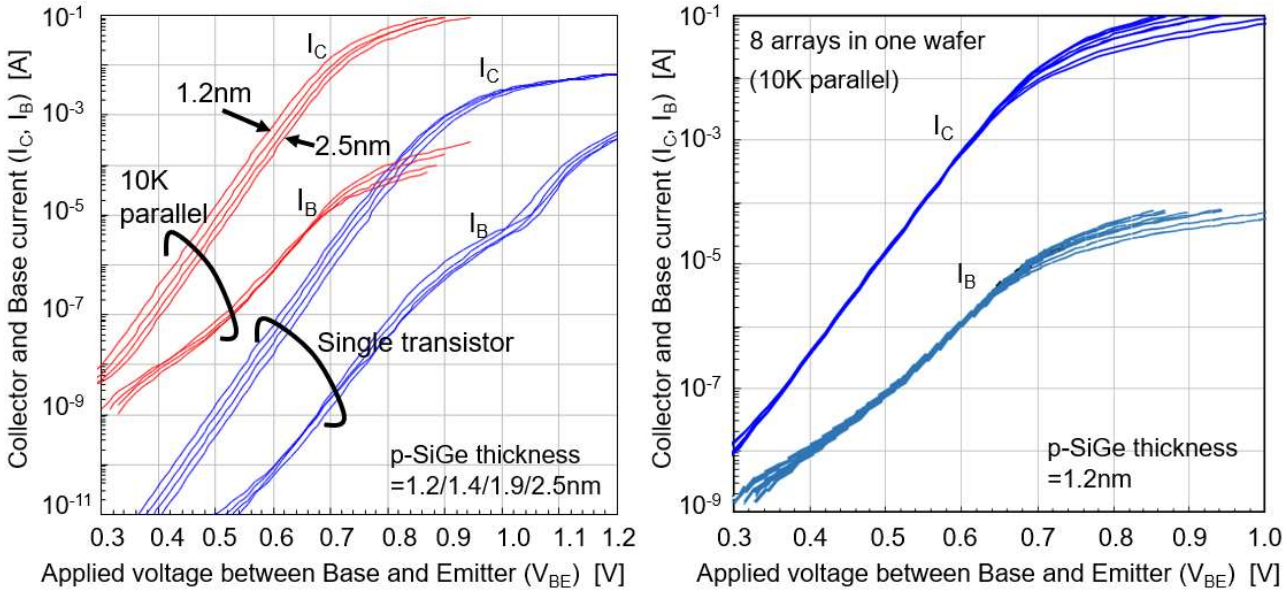


Fig. 4.5. Dependence of V_{BE} on the p-SiGeC thickness in a 10,000-parallel transistor array.



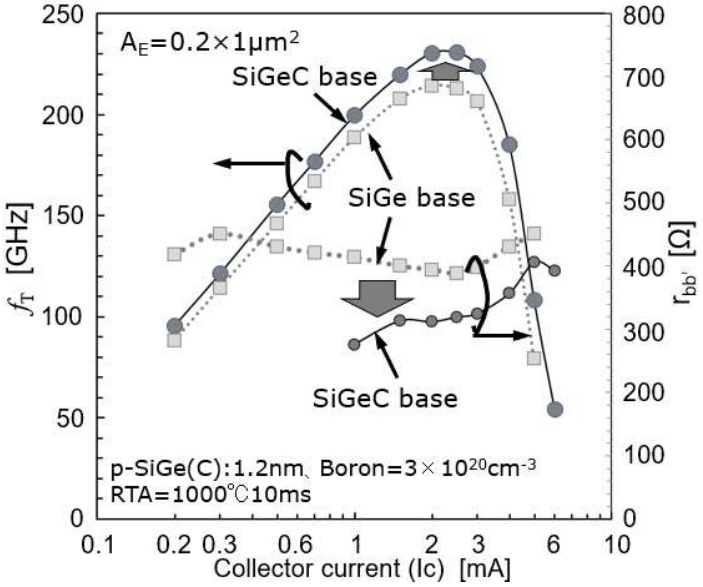
(a) p-SiGeC thickness dependence

(b) 10k-parallel transistor arrays on the entire wafer
p-SiGeC thickness=1.2 nm

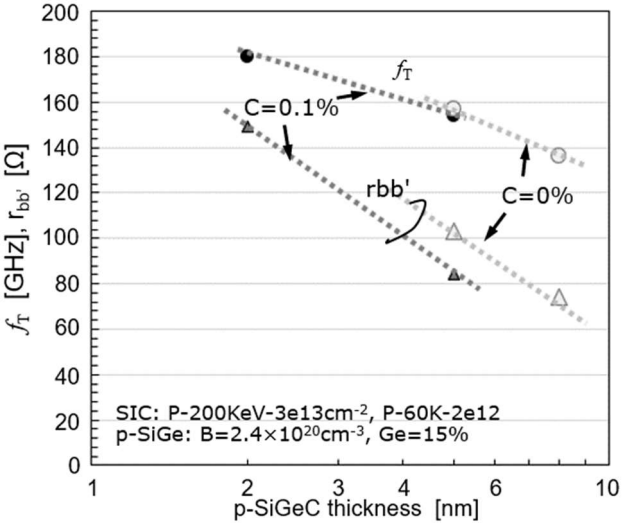
Fig. 4.6. The Gummel plots of SiGe HBTs with thin SiGeC epitaxial growth layer.

variation in the intrinsic base thickness was estimated to be ΔV_{BE}=4.5 mV. Because the actual width of V_{BE} variation on the wafer was 2.8 mV, it could be estimated that the thickness variation width of the p-SiGeC layer was 6.2 %. On the other hand, even if the thickness of the intrinsic base layer was reduced from 2.5 nm to 1.2 nm, there was no collector leakage current caused by the punch-through phenomenon in the base layer in the Gummel plots of 10,000 parallel transistors (Fig. 4.6(a)). In addition, no large leakage current was observed in both the base current and the collector current in evaluating the Gummel plot of 10,000 parallel-connected HBTs on the entire wafer (Fig. 4.6(b)).

On the other hand, there was a fluctuation in the base current, although there was no fluctuation in the collector current in the Gummel plot of a single device. This was because there was a difference in the injection of the hole current into the emitter electrode due to the variation of an interfacial natural oxide between an emitter electrode and a Si substrate. Here, there was no fluctuation in the base current value among the evaluation patterns with 10,000 parallel devices because the variation among single devices was canceled out among the devices.



(a) f_T and rbb'-I_C characteristics



(b) p-SiGe thickness dependence of f_T and rbb'.

Fig. 4.7. Evaluation result of f_T and rbb' with and without carbon doping.

4.5.2 Suppression of Boron Diffusion by Carbon Doping

(1) Carbon doping in the p-SiGeC layer

To increase the f_T, it is crucial not only to make the p-SiGeC layer thinner but also to suppress boron diffusion in the final RTA and maintain the width of the intrinsic base layer. This is why carbon doping technology was applied to the intrinsic base layer. Comparing the characteristics without carbon doping and with 0.1 % addition in the 100 Gbps specification, high f_T and low base resistance were maintained due to the suppression of boron diffusion by the carbon doping (Fig. 4.7(a)). An evaluation result of p-SiGeC layer thickness dependence in another lot showed no difference in f_T, but it effectively reduced rbb' (Fig. 4.7(b)).

On the other hand, the carbon doping amount of about 0.1 % could not wholly suppress boron diffusion in the SIMS analysis in Fig. 3.18 in Chapter 3, and a carbon doping of 0.4 % or more was needed for complete boron diffusion suppression. However, more carbon increased the base leakage current, increased rbb', and decreased f_T (Fig. 4.8). Because carbon molecules entered the interstitial space of the Si crystal and inhibited the diffusion of boron molecules, it was speculated that the presence of excess carbon between the interstitial spaces affected the crystallinity. On the other hand, ρ_{ebs} did not have a clear dependence on the carbon concentration, and it could not be thought that the increase in the carbon concentration caused an increase in the sheet resistance. In case of the carbon concentration was low, it could be considered that the depletion layer tended to extend in the intrinsic base layer due to the decrease in the boron concentration, resulting in a narrower effective base thickness to increase f_T. It is suggested that strengthening the connecting base regions should be performed in anticipation of the suppression of boron diffusion during carbon doping. Even if the carbon concentration is increased to 0.2 % or more, f_T and rbb' could not be improved significantly, so the carbon doping amount was limited to 0.1 to 0.2 %.

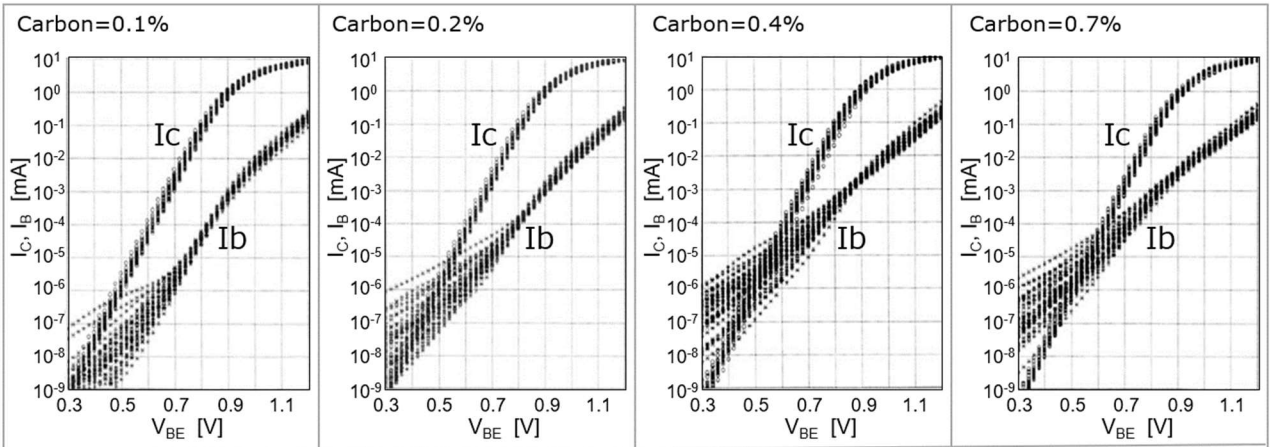


Fig. 4.8. Carbon concentration dependence of the Gummel plots (Measured 33 devices on one wafer).
A_E=0.2×1 μm^2, cap-Si=10 nm, 40 Gbps spec.

(2) A structure in which non-boron-doped SiC layers sandwiched a p-SiGe layer

In examining (1), carbon was added only to the p-SiGeC layer. However, the boron diffusion into the cap-Si of the upper layer and the i-SiGe of the lower layer should also be an issue, and it was thought at first it would be more effective to sandwich the p-SiGe layer between two carbon doping layers (Fig. 4.9). When a device based on this idea was created and evaluated, f_T increased, but rbb' doubled, and f_{MAX} decreased in the structure of the p-SiGe layer sandwiched by the two carbon doping layers (Table 4.3). This result proved that the p-SiGe layer sandwiching structure with the carbon doping layers was effective in suppressing the boron diffusion. Here, the p-SiGe layer could be electrically connected by the boron diffusion from the *in-situ* boron-doped poly-Si electrode. However, it was presumed that if there were a carbon doping layer in front of the p-SiGe layer, the diffusion of boron would be stopped by the non-boron-doped SiC layer, leaving the high resistance region. Therefore, it was decided not to adopt the p-SiGe layer sandwiching structure with the two carbon doping layers because the connection between the extrinsic base region and the intrinsic base region becomes imperfect in principle.

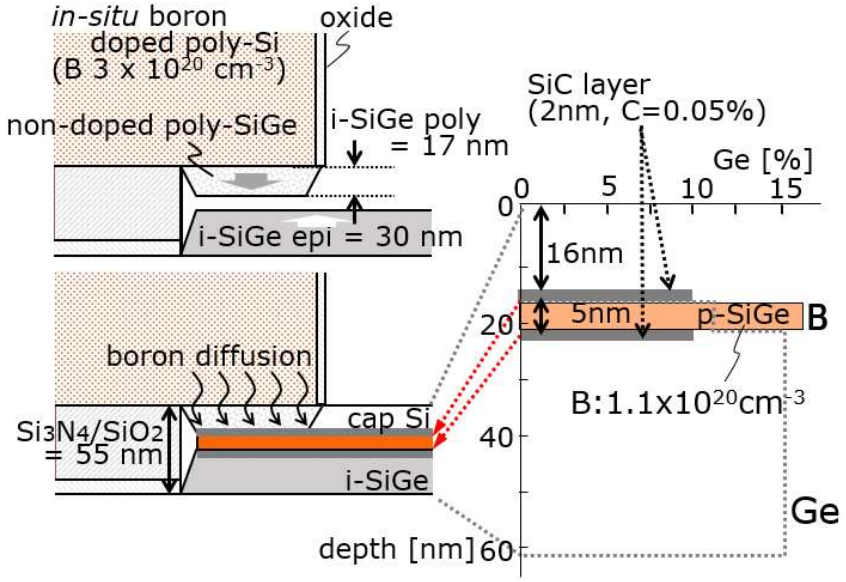


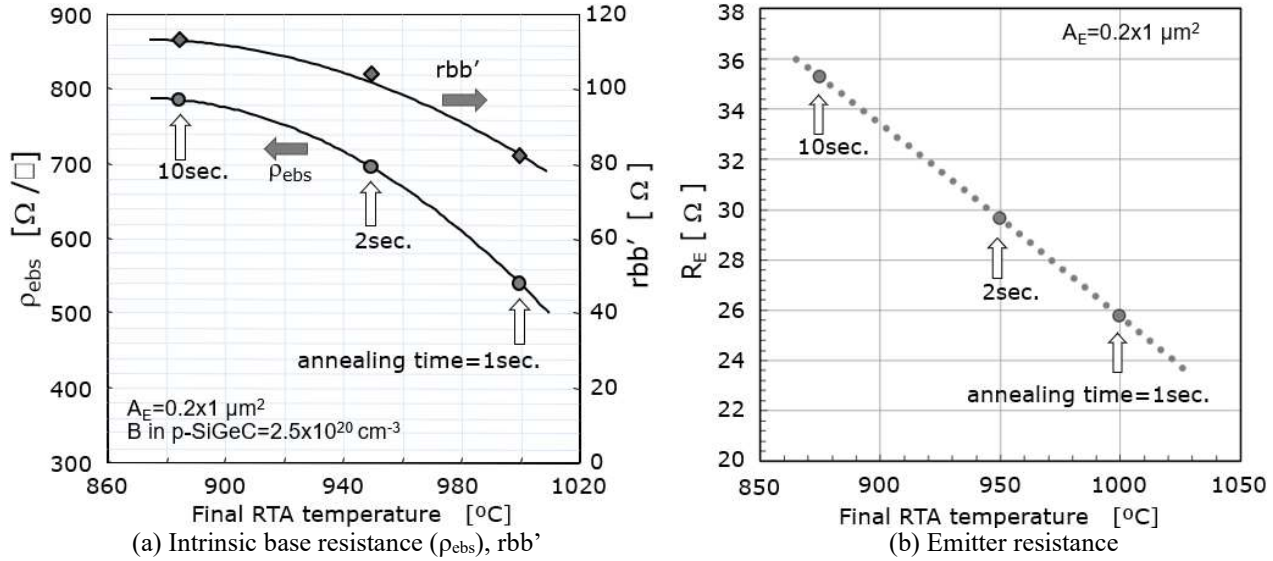
Fig. 4.9. A structure in which a p-SiGeC layer was sandwiched between carbon doping layers.
(SiC layer: Silicon Carbon layer)

Table 4.3. Device characteristic difference due to difference in position of carbon doping layer.

Device characteristics	p-SiGeC layer without SiC layer (Conventional structure)	p-SiGe layer with two SiC layers (Sandwich structure)
BV_{CEO}[V]	2.90	2.95
f_T [GHz]	87.7	98.9
rbb'[Ω]	163	339
f_{MAX} [GHz]	145	118

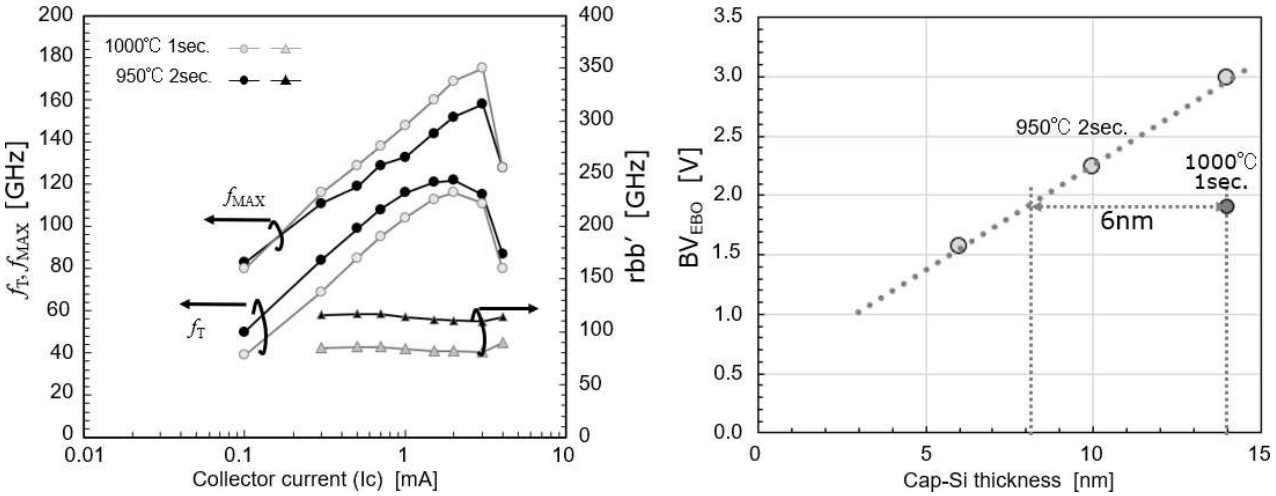
4.5.3 Increasing the Final Annealing Temperature

Similar to the low resistance in the S/D layer of CMOS, it could be expected that the parasitic resistance value in the bipolar transistor would be reduced by increasing the impurity activation rate at the high-temperature final RTA. By increasing the temperature from 875 ℃ to 1000 ℃, the sheet resistance of the intrinsic base layer decreased by 23 %, the base resistance by 20 %, and the emitter resistance (R_E) by 13 % (Fig. 4.10). Although f_{MAX} increased due to the decrease in base resistance, f_T decreased on the lower collector current side, as in the case of thining the cap-Si layer (Fig. 4.11(a)). From the data on the cap-Si layer thickness dependence of the Emitter-Base (EB) breakdown voltage (BV_{EBO}), it was estimated that there was a difference equivalent to 6 nm in the cap-Si thickness between 950 ℃ for 2 seconds and 1000 ℃ for 1 second (Fig. 4.11(b)). Boron diffusion can be suppressed to some extent by the addition of carbon to the p-SiGeC layer, and it could be thought that the depletion layer between the Emitter and Base has become shorter due to the increased diffusion of phosphorus from the emitter poly-Si electrode as the RTA temperature increased.



(a) Intrinsic base resistance (ρ_{ebs}), rbb' (b) Emitter resistance

Fig. 4.10. Final RTA temperature dependence of intrinsic base resistance, rbb', and emitter resistance.



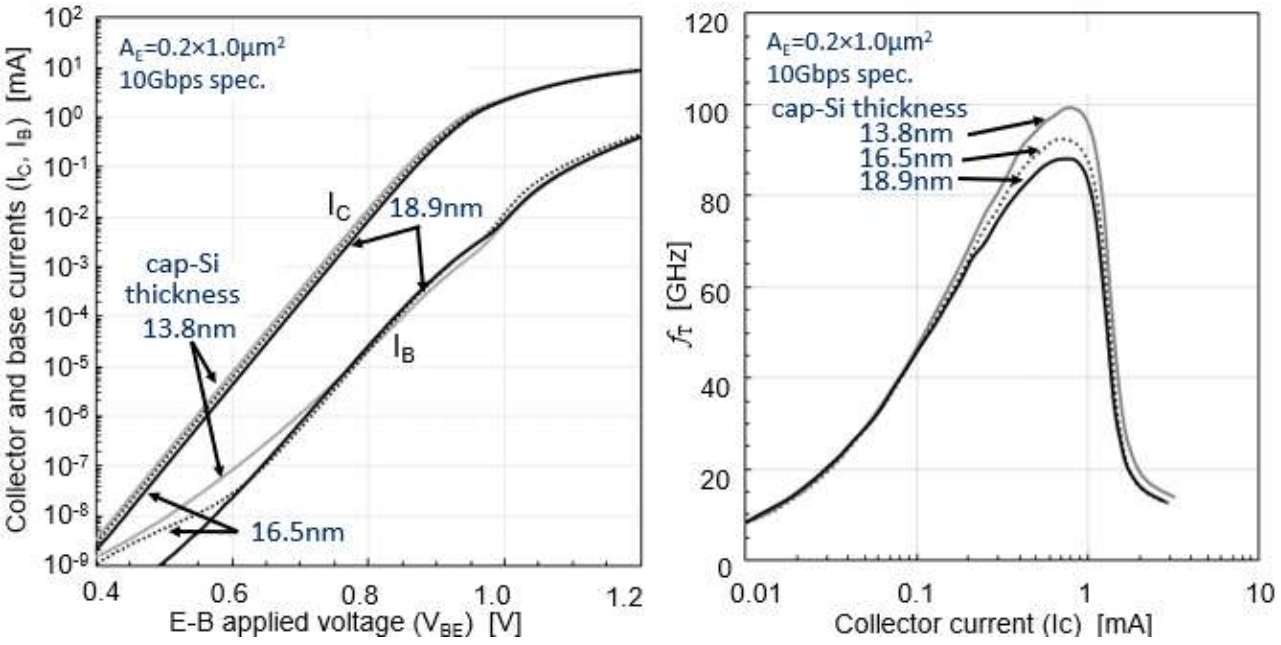
(a) f_T, f_{MAX} (b) Cap-Si thickness dependence of BV_{CEO}

Fig. 4.11. Comparison of thermal budgets at 1000 ℃ and 950 ℃.

4.6 New initiatives for Higher Frequency Characteristics that Si BJTs did not Address

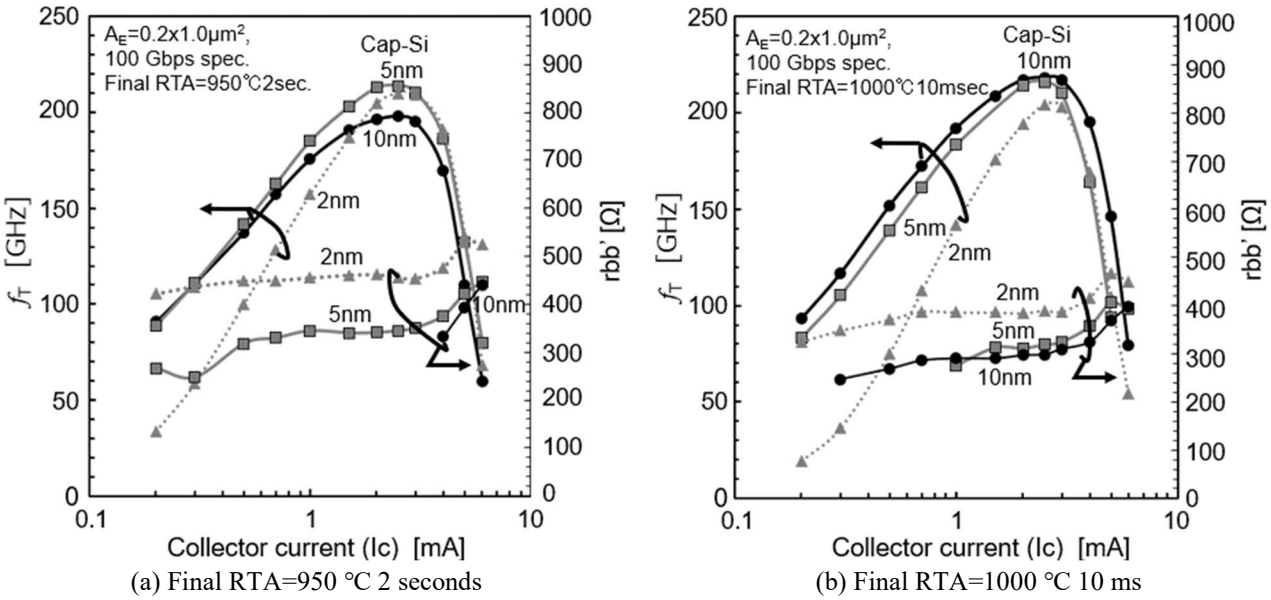
4.6.1 Optimization of Emitter-Base Depletion Layer Width

In the case of changing the thickness of the cap-Si layer between 13.8 nm and 18.9 nm for the 10 Gbps specification, f_T, collector current, and base leakage current increased as the cap-Si layer became thin (Fig. 4.12). When the cap-Si layer was thinned, the depletion layer between the E-B junction became narrower, and the electric field in the depletion layer became higher. Because the intrinsic base layer was pinched off, f_T increased, and the collector current increased due to a decrease in the base Gummel number (G_B). In addition, the proximity of the E-B junction increased the base leakage current due to the Zener breakdown.



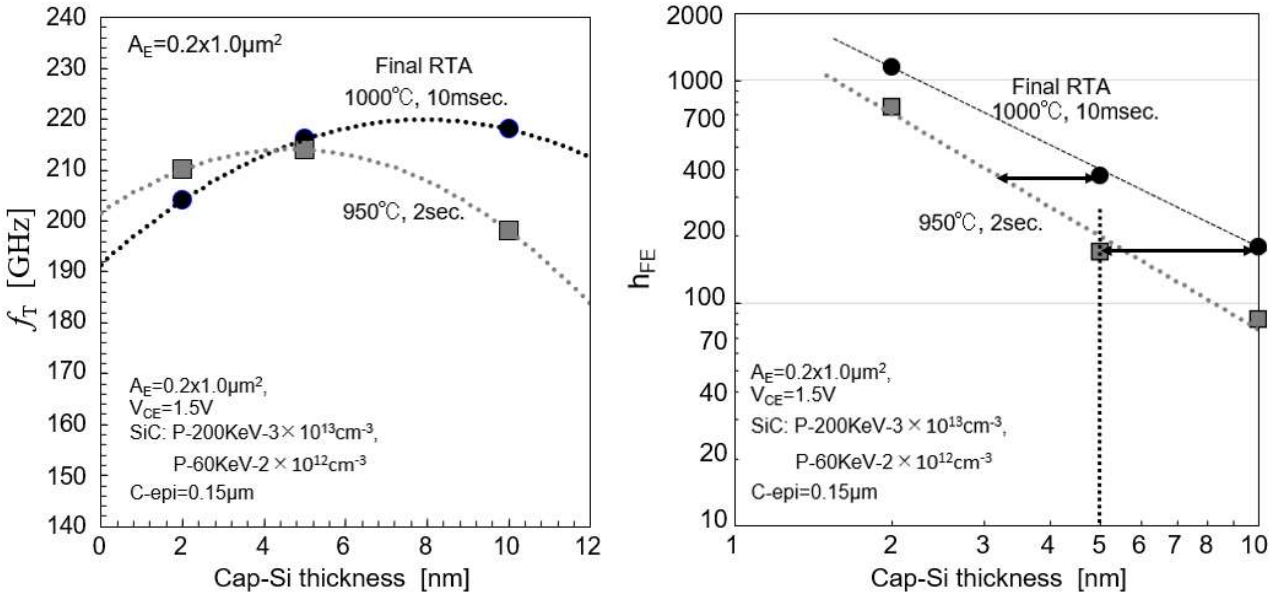
(a) Gummel plots (b) f_T -I_C characteristics

Fig. 4.12. Cap-Si layer thickness dependence of HBT characteristics of 10 Gbps spec. (Final RTA at 875℃ for 10



(a) Final RTA=950 ℃ 2 seconds (b) Final RTA=1000 ℃ 10 ms

Fig. 4.13. Cap-Si layer thickness dependence of f_T -Ic characteristics of 100 Gbps spec.



(a) f_T (b) h_{FE}

Fig. 4.14. Cap-Si thickness and final RTA temperature dependence of f_T and h_{FE}.

The possibility of increasing the frequency by thinning the cap-Si layer was examined in the 100 Gbps specification. When the final RTA condition was 950 ℃ for 2 seconds, f_T increased by 16 GHz and exceeded 200 GHz by thinning the cap-Si layer from 10 nm to 5 nm, but f_T decreased in the region of low collector current in the case of the 2-nm-thick cap-Si layer (Fig. 4.13). This was the same phenomenon as in Fig. 4.11, and it is thought that the increase in C_{EB} extended the C_{EB} charge/discharge time in the first term of Eq. (4.1), resulting in a decrease in f_T. In addition, rbb′ also increased at 2 nm thickness because the intrinsic base layer was pinched off due to the too-close E-B distance, resulting in an increase in ρ_{ebs}. On the other hand, the RTA time at 1000 ℃ was shortened from 1 second to 10 ms, but there was still a difference equivalent to 5 nm in cap-Si thickness compared to 950 ℃ 2 seconds. No significant shortening of the diffusion length was obtained by the short time of RTA of 10 ms (Fig. 4.14).

4.6.2 Cap-Si/cap-SiGe Structure

Because the carbon doping was set to a relatively low 0.1 to 0.2 % from the boron diffusion suppression viewpoint, the boron diffusion's influence on characteristics was evaluated (Fig.3.18). When a Ge-doped layer of

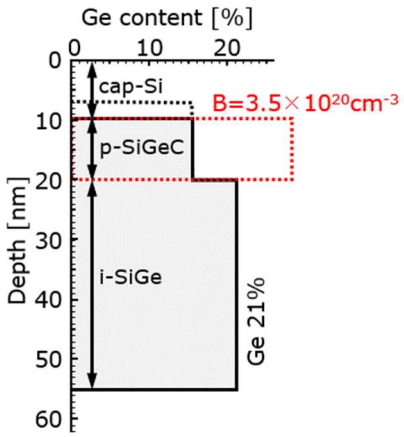
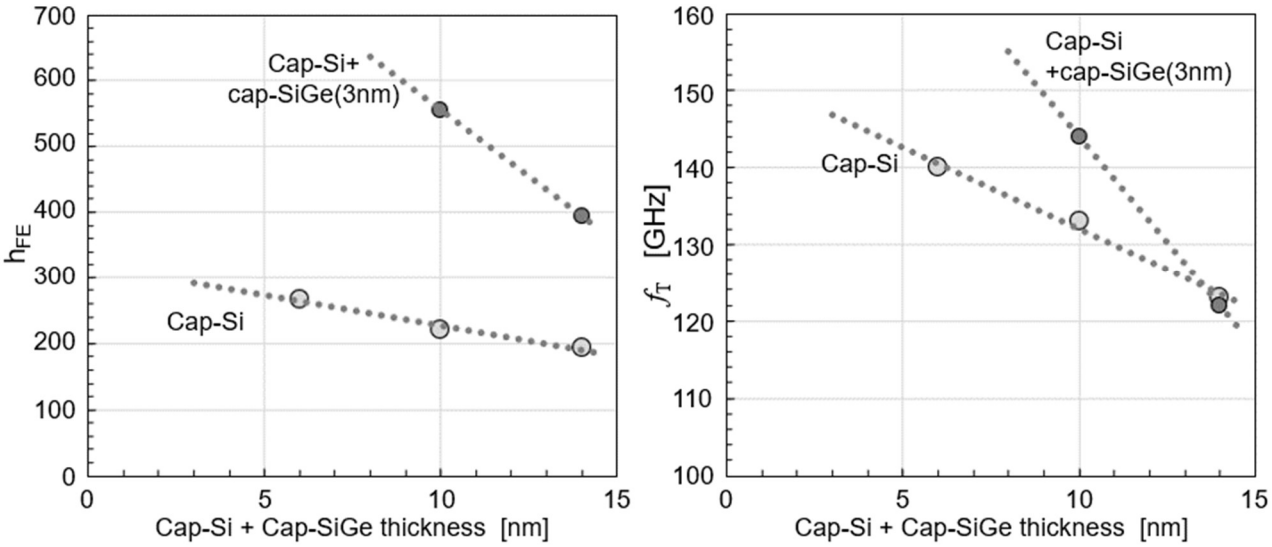


Fig. 4.15. Impurity profile with a cap-SiGe layer added to a cap-Si layer.



(a) h_{FE} (b) f_T

Fig. 4.16. Cap-Si/cap-SiGe structure dependence of h_{FE} and f_T.

3 nm was added to the emitter side to make the cap layer a cap-Si/cap-SiGe structure (Fig. 4.15), h_{FE} increased significantly compared to the case without the cap-SiGe layer (Fig. 4.16). This result was presumed to indicate boron diffused from the p-SiGeC layer and extended an intrinsic base region into a part of the cap-Si layer. On the other hand, f_T was higher with cap-SiGe when the layer thickness of the cap layer was 10 nm, but the reason why the difference disappeared when the layer thickness was 14 nm has been unknown. The f_T did not decrease even if the cap-SiGe layer was added. A cap-SiGe layer was provided on the emitter side because of assuming the boron diffusion.

4.6.3 Effects of Step-type Ge Profiles on Device Characteristics

The Ge concentration was kept constant at 18.2 % in the i-SiGe layer and changed only in the p-SiGeC layer to evaluate the characteristics in the 10 Gbps specification (Fig. 4.17). As the Ge concentration in the p-SiGeC layer increased, the h_{FE} increased, and the V_{BE} at I_C=10 μA decreased (Fig. 4.18(a)). In this case, it could be thought that the bandgap in the intrinsic base layer decreased, and the collector current increased. Because the difference in bandgap width between Ge (E_G=0.69 eV) and Si (E_G=1.12 eV) is 0.43 eV, a 20 % difference in Ge concentration will result in a change of 86 meV if the bandgap changes in proportion to the Ge concentration. The result in Fig.

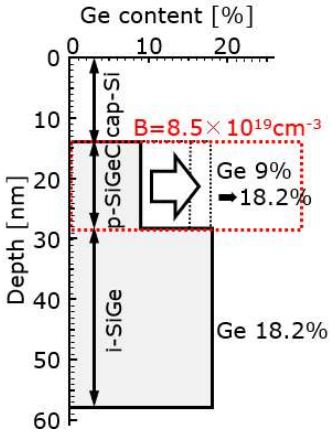
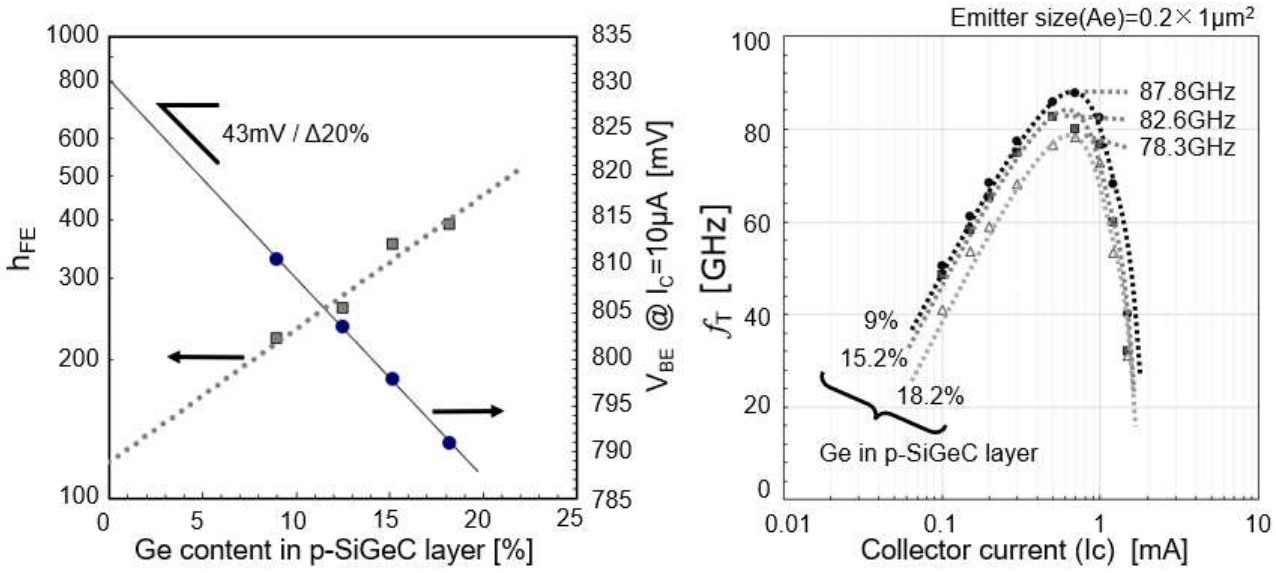


Fig. 4.17. The step-type Ge profile for the 10 Gbps specifications.

4.17 was half of this estimate.

On the other hand, f_T decreased when the Ge concentration in the p-SiGeC layer was close to that in the i-SiGe layer (Fig. 4.18(b)). In the 10 Gbps specification, a difference of 9.5 GHz occurred compared to the step-type profile when the Ge concentration of the p-SiGeC layer and the i-SiGe layer were the same (the flat-type Ge profile). Although the p-SiGe thickness in Fig. 4.18 was relatively thick at 14 nm, Fig. 4.19 shows the Ge concentration dependence of f_T with a thin thickness of 2.5 nm. Furthermore, it was verified that the difference in characteristics depended on the step position of the layer where the boron-doped layer was located, after changing the Ge profile from two steps to four steps. Here, the width of each step was 2.5 nm thick, the Ge concentration



(a) h_{FE}, V_{BE}(at Ic=10 μA) (b) f_T-Ic characteristics

Fig. 4.18. Improvement of f_T by the step-type Ge profile for 10 Gbps spec. (Ge content in i-SiGe layer=18.2 %).

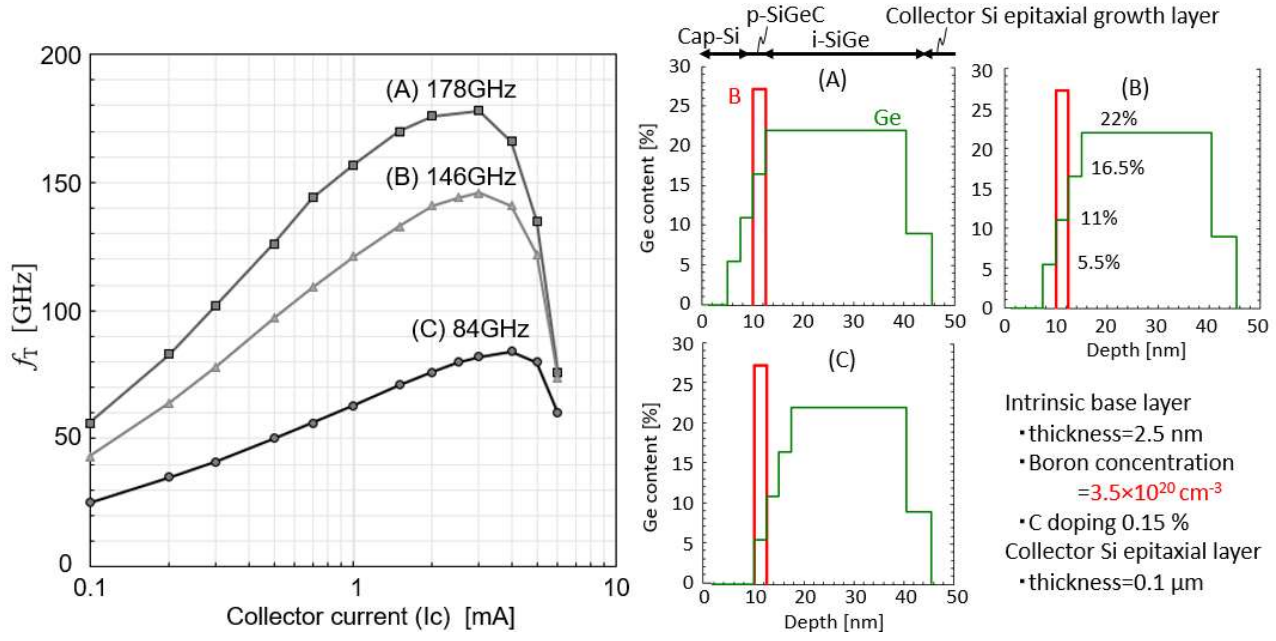


Fig. 4.19. Ge concentration dependence of f_T in case of using the step-type Ge profile.

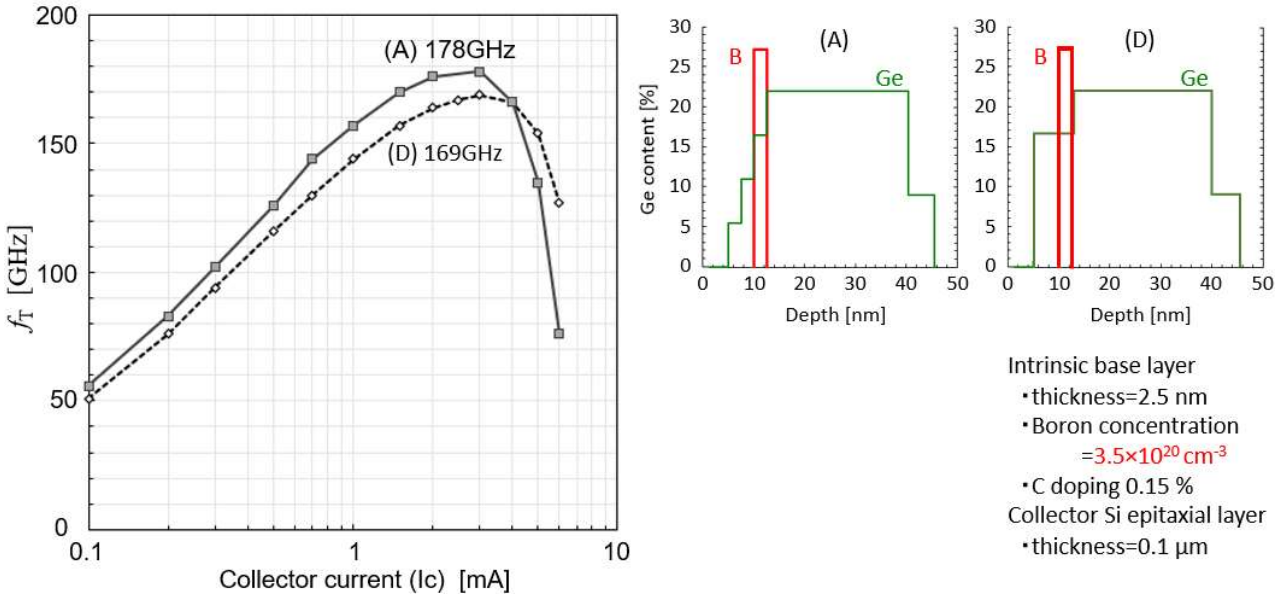


Fig. 4.20. Comparison of frequency characteristics when Ge concentration steps were set on the cap-SiGe layer side.

was changed by 5.5 % at each step, and the p-SiGeC position dependence of f_T was obtained. Even with the same concentration step of 5.5 %, f_T was 84 GHz in the region when the Ge concentration was low, but it increased to 178 GHz when the Ge concentration was high. An electric acceleration field was generated for electrons due to the Ge concentration difference between the p-SiGeC layer and the i-SiGe layer as assumed in Fig.3.3, and it was presumed that the necessary accelerating electric field would not be generated unless the Ge concentration right under p-SiGeC was high.

Furthermore, the frequency was 9 GHz higher with the step when comparing the characteristics with and without a Ge concentration step between the cap-SiGe layer and the p-SiGeC layer (Fig. 4.20). It was presumed that the accelerating electric field was generated in the intrinsic base layer by widening the bandgap on the cap-SiGe side from that in the intrinsic base layer. The multi-step Ge profile in Fig. 4.20(a) was the closest to the graded-type Ge profile adopted by other research institutes. The graded-type Ge profile was expected to generate the accelerating electric field most efficiently. But, since the difference between (A) and (D) in Fig. 4.20 was 9 GHz, it was assumed that the difference between the step-type Ge profile and the graded-type Ge profile was insignificant. Considering the ease of monitoring the SiGe growth layer, it can be regarded that the step-type profile is superior in the production stage.

From the above, experiments confirmed that the step-type Ge profile increases the frequency of the device characteristics. On the other hand, as shown in Section 4.6.2, the Boron profile was obtained during epitaxial growth. It is possible that the subsequent annealing spread the Boron profile and changed the relationship between the concentration change position of Ge and Boron. Therefore, there is a possibility that there was a phenomenon different from the simulation result of Fig.3.3. Still, the details are unknown because the accurate analysis of the Boron profile has not been performed.

4.7 Speeding up SiGe HBT by Suppressing Parasitic Characteristics

4.7.1 Reduction of Collector Resistance

Although the improvement in f_T peaked at around 180 GHz only by thinning the intrinsic base layer (Fig. 4.2), f_T of 210 GHz was achieved by thinning the collector Si epitaxial growth layer (Fig. 4.21). However, considering the one-dimensional simulation results with a device simulator (Synopsys Taurus Medici) using the box-type boron profile and the top data of IHP (The Leibniz Institute for High Performance Microelectronics), f_T was expected to be around 300 GHz if BV_{CBO} was 5 V. (Fig. 4.22). The result of 210 GHz of f_T at 5 V of BV_{CBO} was below the

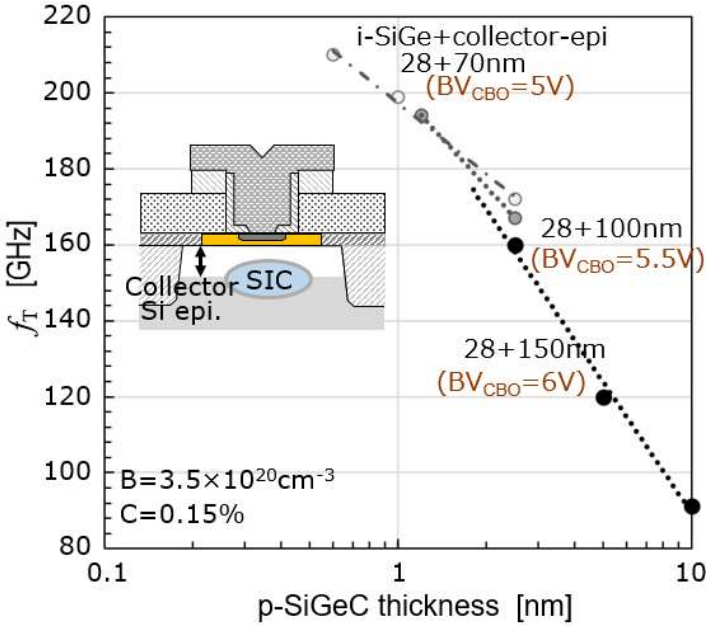


Fig. 4.21. f_T improvement by thinning the collector layer.

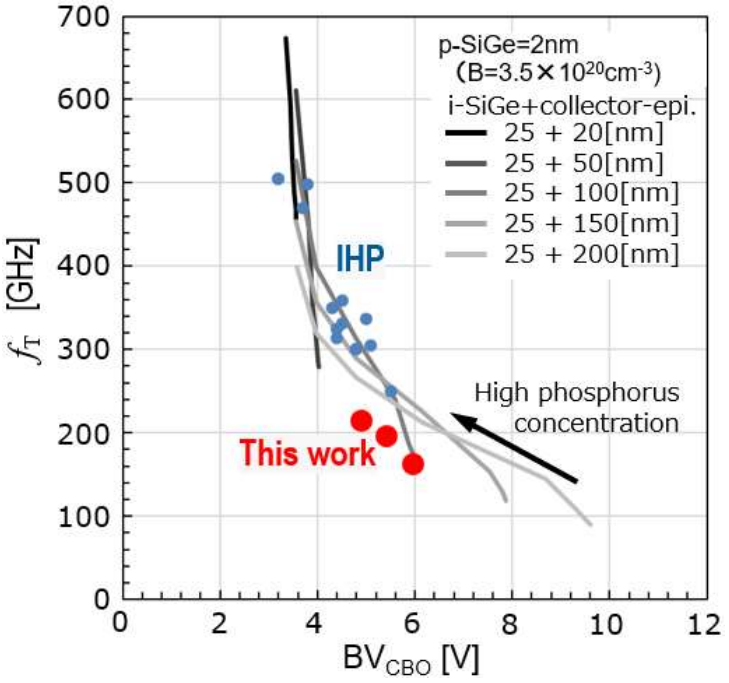


Fig. 4.22. Comparison of simulated and measured f_T-BV_{CBO} correlations. The solid lines are the simulation results; the

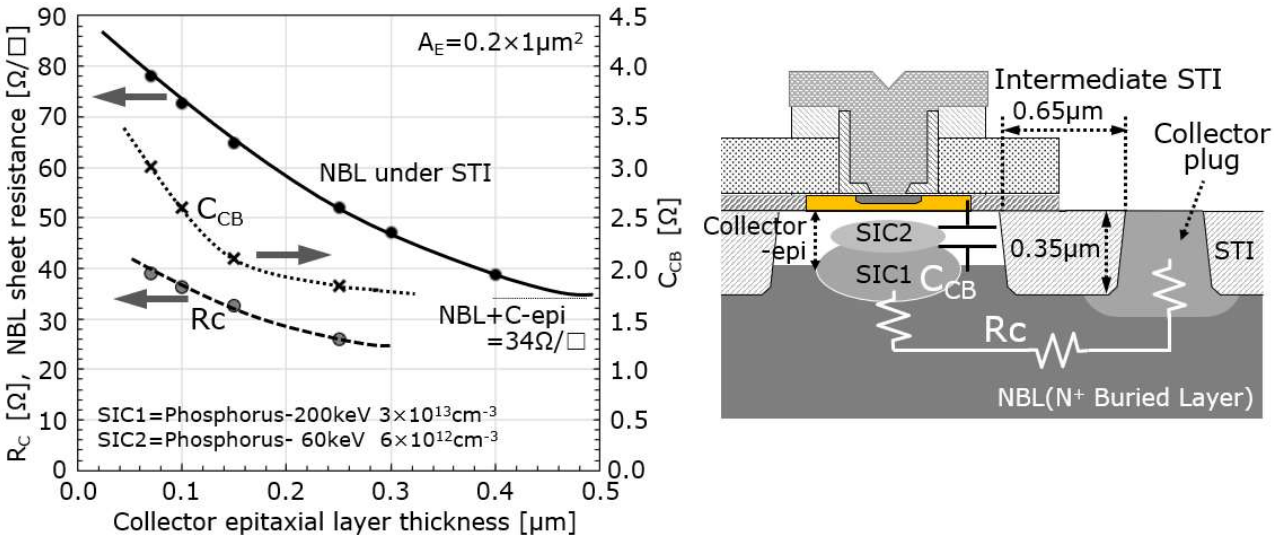


Fig. 4.23. Collector epitaxial layer thickness dependence of C_{CB} and R_C.

Table 4.4 Ratio of CR time constant to time constant conversion value of f_T.

Thickness of collector Si epi. [μm]	C_{CB} [fF]	Rcs [Ω]	CR time constant	f_T=300GHz ≒0.53ps	f_T=140GHz ≒1.14ps
0.07	3.0	39.0	0.12ps	23%	-
0.25	1.8	26.0	0.048ps	-	4%

expectation. Here, the horizontal axis of Fig. 4.22 was BV_{CBO} because BV_{CBO} is proportional to the transit time in the depletion layer on the collector side.

Here, the collector plug and the intrinsic base layer were separated by an intermediate STI with a depth of 0.35 μm (width of 0.65 μm). Therefore, when the collector Si epitaxial growth layer became thinner, the upper part of the N^+ buried layer (NBL) was etched during the STI process. Becoming the thinner NBL increased the sheet resistance of the NBL and increased the collector resistance (R_C) (Fig. 4.23). Reducing the thickness of the collector Si epitaxial growth layer from 0.25 μm to 0.07 μm increased the sheet resistance by 50 % and R_C by 34 %. Here, the NBL layer was formed by implanting Sb ions at 2×10^{15} cm^{-2}, and the sheet resistance was 34 Ω/□. The collector plug was formed by implanting phosphorus ions at 5×10^{15} cm^{-2} and had a sheet resistance of 20 Ω/□. In addition, when the collector Si epitaxial growth layer was 0.07 μm, it became thinner than the range of the SIC1 layer. Hence, the effect of suppressing the C_{CB} increase, which the SIC structure provided to some extent, disappeared. At the device of 140 GHz of f_T having the 0.25-μm thickness of the collector Si epitaxial layer, the ratio of the collector time constant to the f_T time constant conversion value of 1.14 ps was 4 %. Hence, it was not a big issue (Table 4.4). However, when the collector Si epitaxial growth layer was 0.07 μm, the collector constant became 0.12 ps. The ratio became 23 % for the time constant of 0.53 ps for the f_T of 300 GHz, and the influence cannot be ignored.

Until then, the same device layout was used for high-frequency devices to ensure compatibility with high-voltage bipolar transistors. The intermediate STI between the intrinsic base and the collector plug stopped the

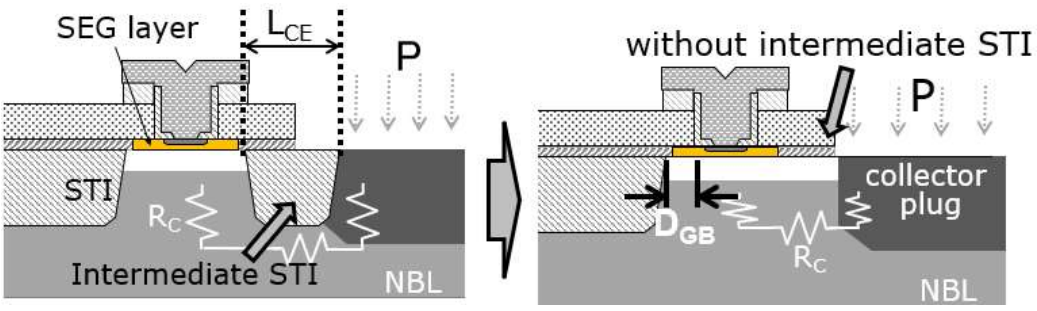
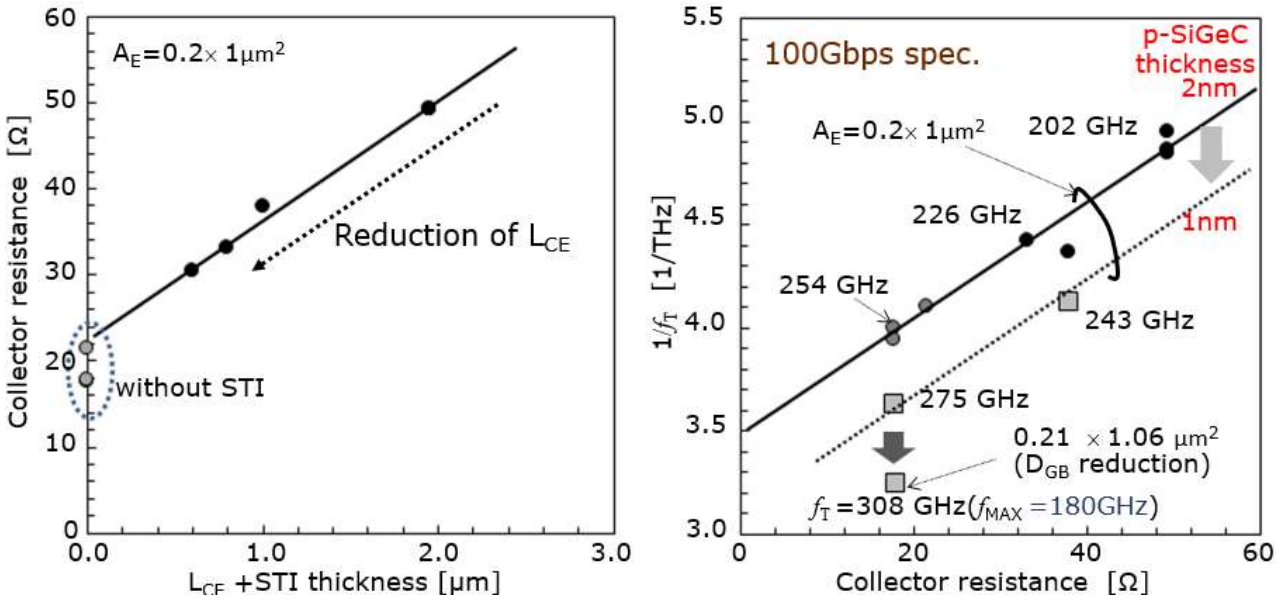


Fig. 4.24. R_C reduction by shortening the distance (L_{CE}) between the collector plug and the intrinsic base region or removing the STI.



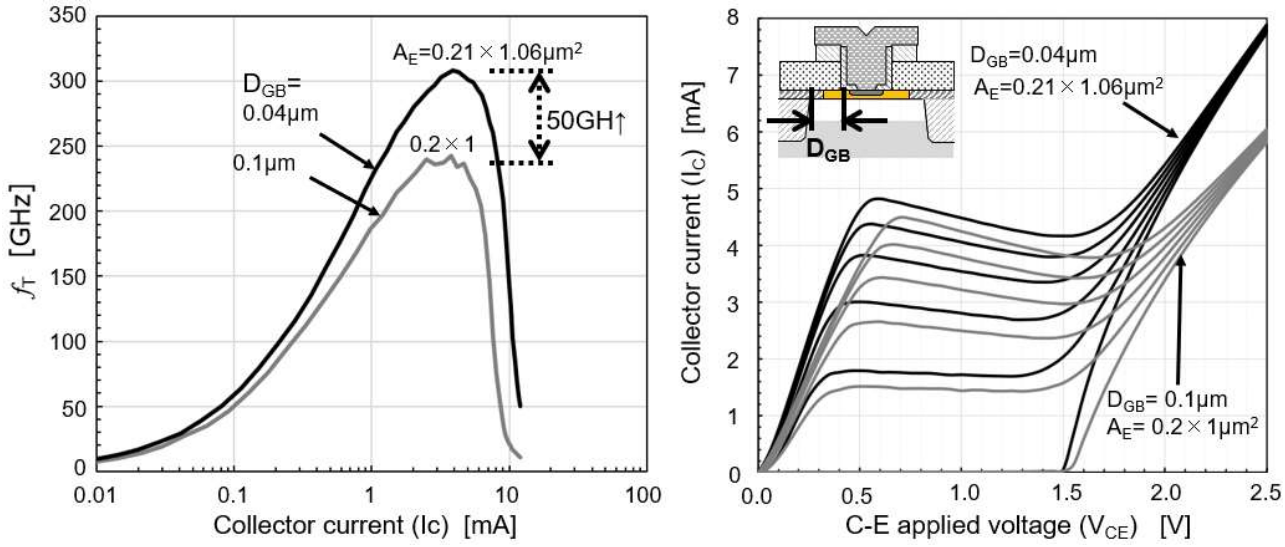
(a) Dependence of R_C on L_{CE}

(b) Dependence of f_T on collector resistance (R_C)

Fig. 4.25. Improved f_T by reducing collector resistance. L_{CE}: shallow trench width between the collector plug and the intrinsic base region, D_{GB}: Distance of the link region (shown in Figs.4.24 and 4.26(b))

lateral phosphorus diffusion from the collector plug, preventing the decrease in BV_{CBO}. However, the BV_{CBO} of high-frequency devices has become 6 V or less, and the need to consider the breakdown voltage drop in the lateral direction has decreased. Therefore, it was decided in this study to shorten the distance of the intermediate STI or change the structure to eliminate the intermediate STI (Fig. 4.24). As a result, collector parasitic resistance was reduced by shortening the distance of the intermediate STI, and R_C was finally halved by removing the intermediate STI (Fig. 4.25(a)). 226 GHz was achieved with the conventional STI isolation structure by setting the thickness of the collector Si epitaxial growth layer to 0.15 μm and setting the SIC2 dose to 6×10^{12} cm^{-2}. Furthermore, the 28 GHz improvement was achieved from the standard intermediate-STI distance of 0.65 μm by eliminating the intermediate STI and lowering the collector resistance (Fig. 4.25(b)).

Furthermore, f_T was raised to 21 GHz by thinning the p-SiGeC layer from 2 nm to 1 nm. Finally, the collector time constant was reduced, and f_T = 308 GHz (f_{MAX} = 180 GHz) was achieved by shortening the separation distance (D_{GB}) of the extrinsic base region from 0.1 μm to 0.04 μm and reducing the collector capacitance C_{CB} by an



(a) f_T-I_C characteristics (b) I_C-V_{CE} characteristics

Fig. 4.26. Characteristic variation due to shortening the distance (D_{GB}) between the emitter hole and the STI from 0.1 μm to 0.04 μm. The thickness of the p-SiGeC layer was 1 nm.

estimated 30 % (Figs. 4.25(b), 4.26(a)). Because the boron concentration was as high as 3.5×10^{20} cm^{-3} and the box-type boron profile was maintained, BV_{CEO} of 1.5 V was maintained even with a layer thickness of 1 nm. In addition, removing the intermediate STI did not affect the breakdown voltage (Fig. 4.26(b)).

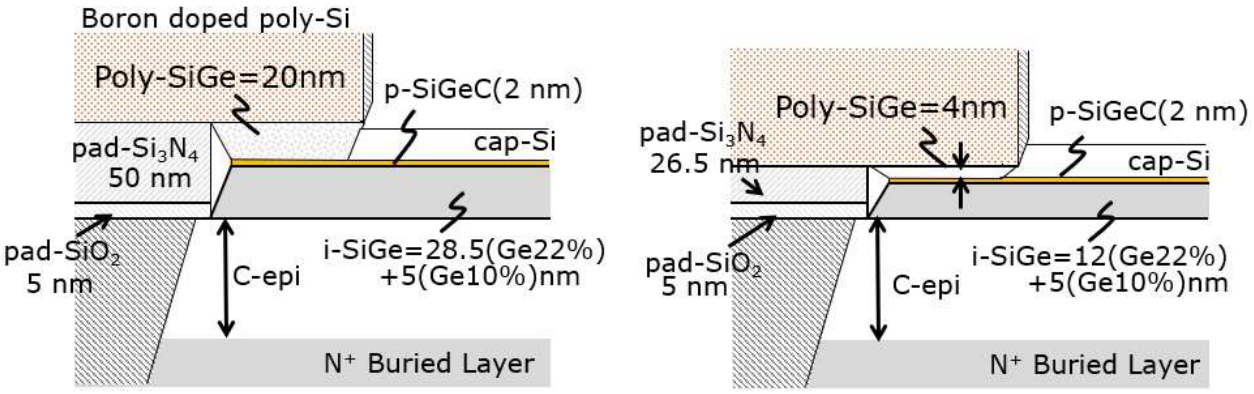
A previous study [25] showed that a steeper NBL dopant profile was needed to raise f_T to 200 GHz, but the removal of the intermediate STI to boost f_T was selected in this study. If the intermediate STI is removed, the collector-base breakdown voltage (BV_{CBO}) and collector-emitter breakdown voltage (BV_{CEO}) will vary depending on the positional accuracy of the resist pattern that determines the phosphorus ion implantation location in the collector plug. It is necessary for circuits that require high BV_{CBO} to apply a device with the intermediate STI. However, the SiGe HBT without the intermediate STI will be necessary to realize f_T of 250 GHz or more after strictly controlling the alignment accuracy of lithography to form a resist mask for impurity ion implantation into the collector plug.

4.7.2 Reduction of Base Resistance

Although f_T =308 GHz was achieved by thinning the p-SiGeC layer to 1 nm, f_{MAX} remained at 180 GHz due to the increase in base resistance by the thinner intrinsic base layer. The maximum oscillation frequency (f_{MAX}), which indicates the power amplification factor, expresses the operating limit of the circuit more than the cutoff frequency (f_T), which means the current amplification factor. Therefore, because the circuit's performance was determined by f_{MAX} of 180 GHz even if the SiGe HBT achieved f_T=308 GHz, f_{MAX} improvement beyond 300 GHz was investigated by reducing the intrinsic base resistance.

(1) Attempt to reduce base resistance by thinning the connecting region (poly-SiGe layer)

A poly-SiGe layer grew right under the base poly-Si electrode during the selective SiGe epitaxial growth as described in Figs. 3.8 and 4.27(a). The poly-SiGe layer was a region that connected the intrinsic base layer and the base poly-Si layer, which became a low-resistance layer due to boron diffusion from the base poly-Si layer.



(a) pad-Si_3N_4 thickness =50 nm (b) pad-Si_3N_4 thickness=26.5 nm

Fig. 4.27. Schematic cross-sectional views when intrinsic base layers were formed.

Table 4.5. Study the base resistance (rbb') reduction by thinning the i-SiGe layer.

Structure	Pad-Si_3N_4 [nm]	C-epi+i-SiGe		C_{CB} [fF]	SIC2 [cm^{-2}]	rbb' [Ω]	BV_{CBO} [V]	f_T [GHz]	f_{MAX} [GHz]
		C-epi [nm]	i-SiGe [nm]						
Thin i-SiGe structure	26.5	70	17	3.8	0	116	4.3	160	113
		100		3.1	2×10^{12}	148	5.0	144	114
Standard i-SiGe thickness structure	53.0	70	30	2.9	0	123	4.8	159	141
		100		2.9	2×10^{12}	123	5.0	159	141

SIC1=Phosphorus-200 KeV-3×10^{13} cm^{-2}, C-epi=Collector Si epitaxial growth layer

Intrinsic base thickness (W_B)=2 nm, 3.5×10^{20} cm^{-3} (Carbon=0.15 %), Emitter area size (A_E)=0.2×1 μm^2

Here, the incubation time until the SiGe epitaxial growth started was longer on the *in-situ* boron-doped poly-Si layer than on the Si substrate (Fig. 3.5 in Chapter 3). From the results of Fig. 3.5, the thickness of the poly-SiGe layer under the base electrode was expected to be as thin as 4 nm when the i-SiGe growth time was set to 45 seconds. In that case, since it was necessary to connect the upper and lower SiGe layers when the growth of the p-SiGeC layer was completed, it was essential to thin a pad Si_3N_4 layer. The pad Si_3N_4 layer was thinned from 53 nm to 26.5 nm, and the i-SiGe layer was thinned from 28.5 nm (22 % Ge) + 5 nm (10 % Ge) to 12nm (22 % Ge) + 5 nm (10 % Ge) (Fig. 4.27(b)).

This experiment used two collector-Si epitaxial thicknesses of 70 and 100 nm. When the collector Si epitaxial thickness was 70 nm, the base resistance could be reduced from 123 Ω in the conventional structure to 116 Ω, but when it was 100 nm, the base resistance increased to 148 Ω, and f_{MAX} decreased (Table 4.5). In addition, when the collector Si epitaxial thickness was 70 nm and the i-SiGe thickness was 12 nm (22 % Ge) + 5 nm (10 % Ge), a thin depletion layer between the collector and the base caused suppression of BV_{CBO}, an increase of C_{CB} and reduction of f_{MAX}. Regarding the decrease in BV_{CBO}, the tendency was consistent with the experimental results of other lots (Fig. 4.28), and it was considered that the increase in C_{CB} could be suppressed by thickening the collector Si epitaxial layer in accordance with the thinning of the i-SiGe layer.

On the other hand, it was believed that the reason why the base resistance increased by making the i-SiGe layer thinner was that there was no poly-SiGe layer directly below the base poly-Si electrode (Fig. 4.29). If the p-SiGeC

layer was right under the base poly-Si electrode, the lateral boron diffusion from the base poly-Si electrode was blocked due to the carbon doping in the p-SiGeC layer. On the other hand, if there was the poly-SiGe layer under the base electrode, the poly-SiGe layer was connected to the cap-Si layer in the lateral direction, so it was thought that boron diffused laterally from the base poly-Si electrode. As a result, the resistance of the emitter diffusion layer and the base poly-Si electrode was effectively reduced by the lateral boron diffusion. When the thickness of the poly-SiGe layer directly below the base poly-Si electrode was set as thin as 4 nm, it was speculated that the base resistance increased on some wafers due to the poly-SiGe growth rate fluctuation among the wafers. In this study, it was determined that there was room for optimization of the i-SiGe layer thickness.

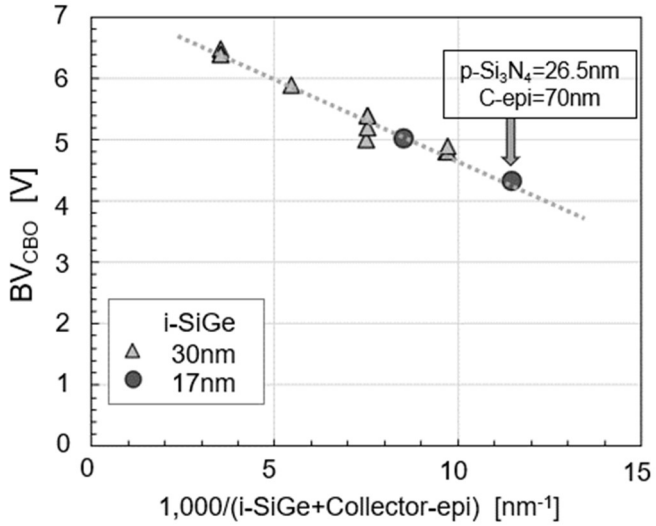


Fig. 4.28. Dependence of BV_{CBO} on collector epitaxial layer thickness.

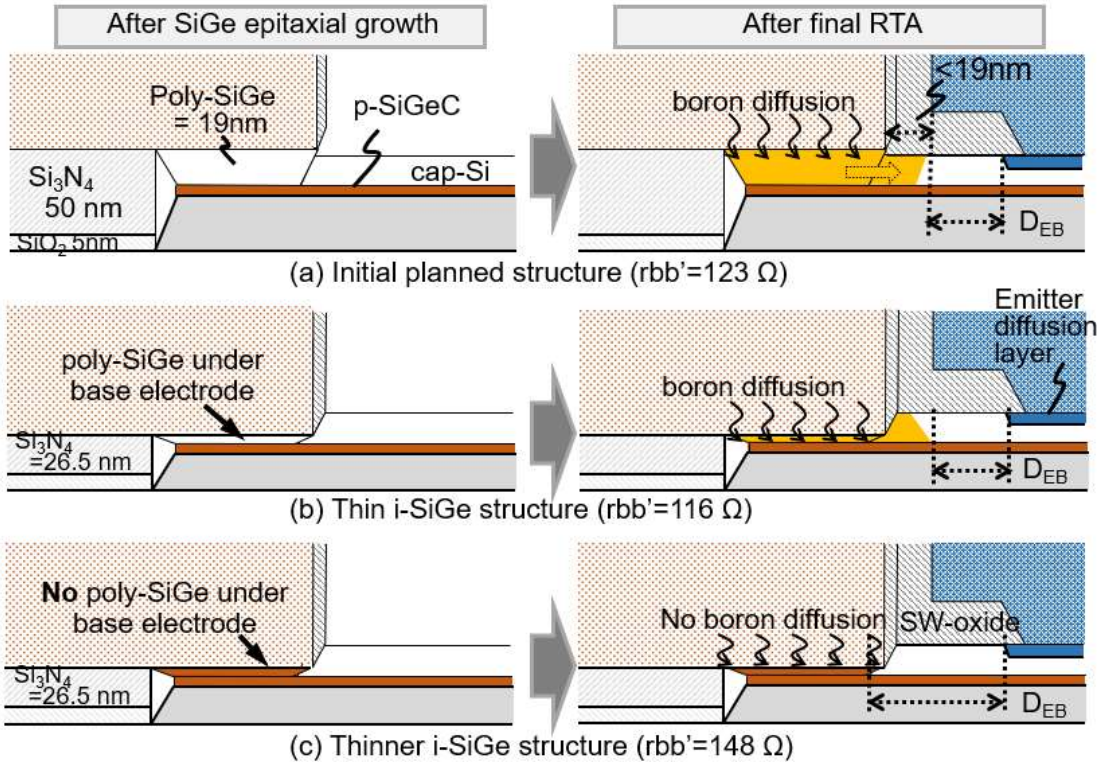
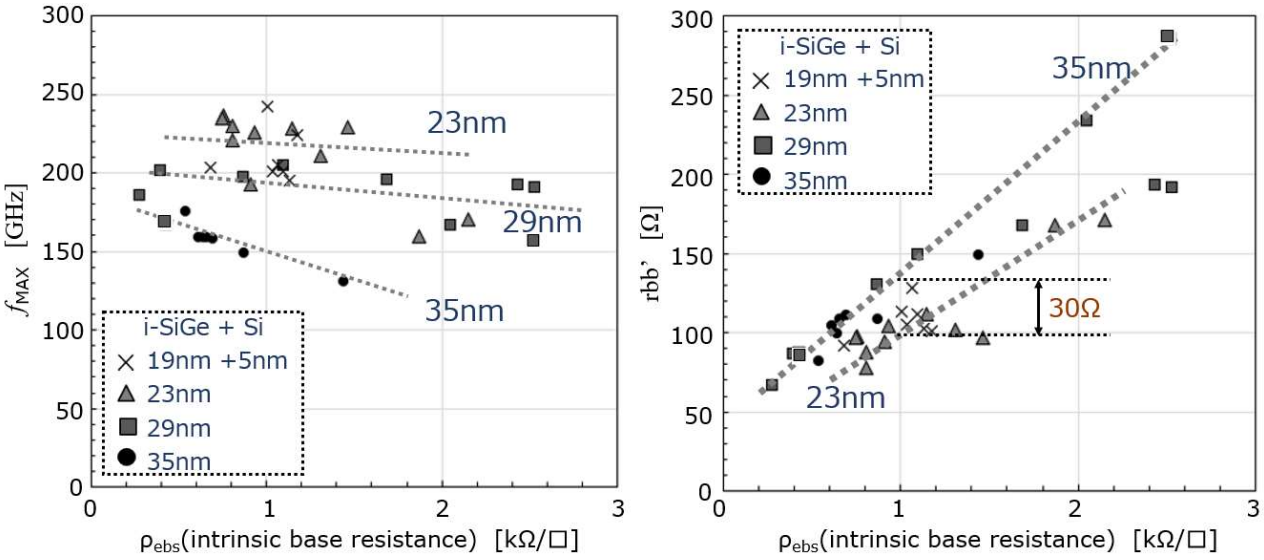


Fig. 4.29. Inferred diagrams of lateral boron diffusion from a base poly-Si layer.

(2) Review of i-SiGe layer specifications

The evaluation results so far have been rearranged in terms of the correlation between f_{MAX}, rbb', and pinch base resistance (ρ_{ebs}). Because the comparison was made in multiple lots with different prototype periods, the correlation was not clearly separated. Still, f_{MAX} tended to increase as the thickness of the i-SiGe layer decreased from 35 nm to 23 nm (Fig. 4.30). Regarding rbb', SiGe HBTs of the 23-nm i-SiGe layer were about 30 Ω lower than those of the 35-nm i-SiGe layer, and the trend of rbb' matched that of f_{MAX}. On the other hand, when the total value of the 5-nm Si-buffer layer and the i-SiGe layer was 24 nm, no significant difference was seen when comparing the i-



(a) f_{MAX} (b) rbb'

Fig. 4.30. Correlation between f_{MAX}, rbb' and pinch base resistance(ρ_{ebs}), emitter area (A_E)=0.2×1 μm^2.

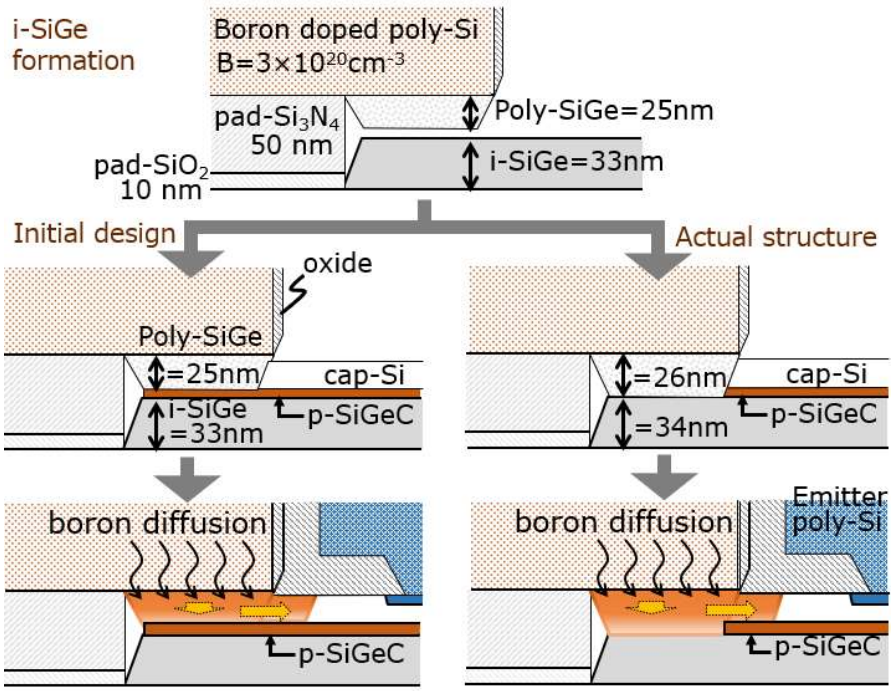


Fig. 4.31. Differences in the link base regions formed due to differences in i-SiGe layer thickness.

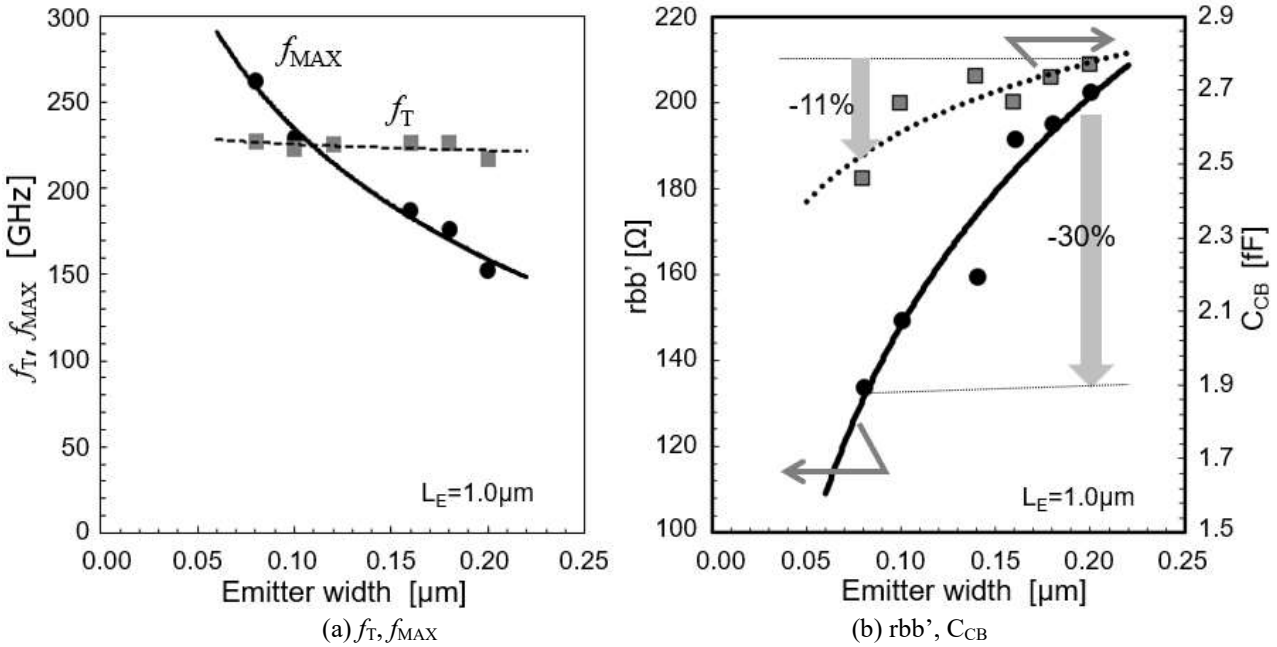
SiGe layer of 23-nm thickness. Here, the purpose of providing the 5-nm Si-buffer layer right under the i-SiGe layer was to reduce the stress in the i-SiGe layer by effectively thinning the i-SiGe layer.

In designing the device structure, the thickness of each layer was set so that the poly-SiGe grown from the base poly-Si electrode and the i-SiGe layer grown from the Si substrate sandwiched the p-SiGeC layer. Boron was diffused from the base poly-Si electrode and connected to the p-SiGeC layer on the entire area under the base poly-Si electrode (Fig. 4.31). However, considering that the i-SiGe layer, which was thinner than the initial condition, could lower rbb', it could be presumed that boron diffusion was insufficient to fill in the non-doped poly-SiGe region. In addition, it could be thought that the poly-SiGe and i-SiGe layers were connected before the growth of the p-SiGeC layer started. In this case, it was believed that the junction resistance increased because the p-SiGeC layer with low resistivity could not be grown under the base poly-Si electrode. Therefore, the i-SiGe layer of 23 nm including the 5-nm-thick-Si layer was used as the standard condition.

(3) Narrow Emitter Region

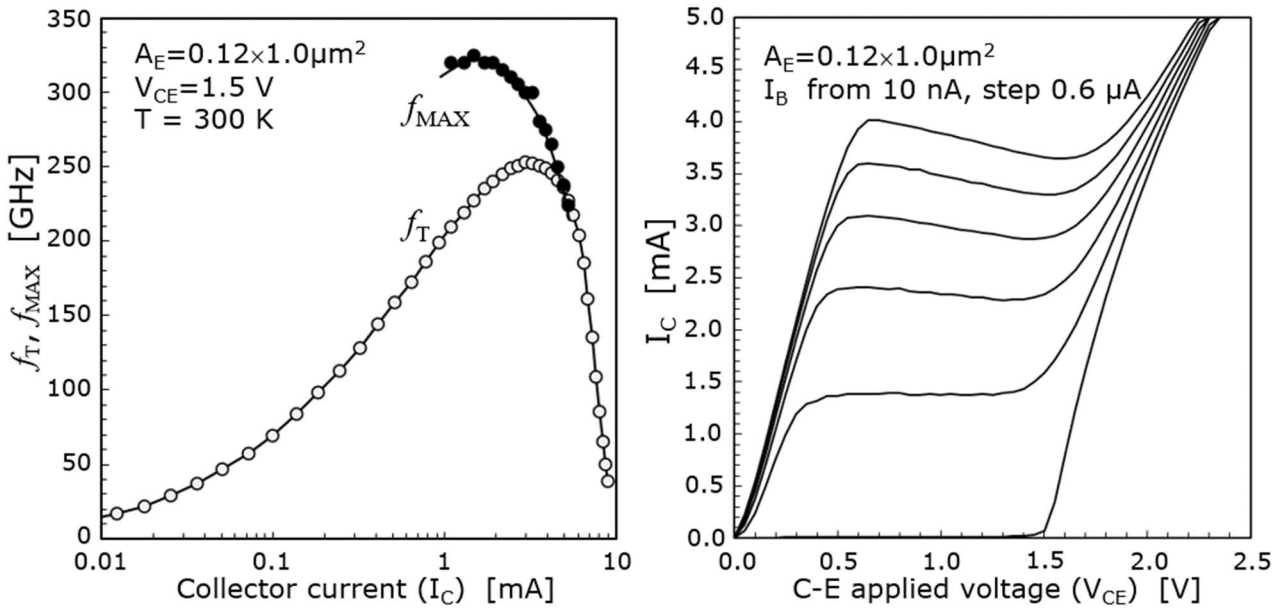
By narrowing the emitter width from 0.2 μm to 0.08 μm, the base resistance (rbb') could be reduced by 35 % and the collector-base parasitic capacitance (C_{CB}) by 15 %. As a result, f_{MAX} increased from 150 GHz at W_E = 0.2 μm to 262 GHz at W_E = 0.08 μm (Fig. 4.32).

f_{MAX} was improved by increasing the p-SiGeC thickness to 2 nm, which was thicker than the device that achieved f_T = 308 GHz. The device with the emitter width of 0.12 μm removed the intermediate STI between the intrinsic base layer and collector plug, the same as the structure in Fig. 4.2. Finally, this device achieved f_T =254 GHz and f_{MAX}=325 GHz at BV_{CEO}=1.5 V (Fig. 4.33). Any fine techniques beyond the layout rule or other process variations were not applied. The results of the SiGe BiCMOS technology studied at this time show that it is possible to realize LSIs for optical and millimeter wave communication at the mass production level.



(a) f_T, f_{MAX} (b) rbb', C_{CB}

Fig. 4.32. Emitter width dependence of device characteristics of the SiGe HBT. f_T = 227 GHz, the emitter length was 1.0 μm, SiGe HBT with STI between collector plug and intrinsic base region, p-SiGeC thickness=1 nm.



(a) f_T / f_{MAX}-collector current curve (b) Common-emitter output characteristics

Fig. 4.33. The measurement result of the highest f_{MAX} characteristics in this study. The SiGe HBT structure was without STI between the collector plug and the intrinsic base region, and the p-SiGeC thickness was 2 nm.

4.8 Conclusions

A SiGe HBT process using the selective SiGe epitaxial growth technique was established.

(1) f_T improved from 90 GHz to 180 GHz at 40 Gbps specification by thinning the p-SiGeC layer from 10 nm to 1.2 nm. Also, the base resistance was reduced, and the extreme increase in h_{FE} was suppressed by raising the boron concentration of the p-SiGe layer from 0.85-1.5×10^{20} cm^{-3} to 2.4-4.5×10^{20} cm^{-3}. Although the device yield was stable even with the 1.2-nm-thick p-SiGe layer, f_{MAX} decreased due to an increase in base resistance due to thinning of the p-SiGeC layer alone.

(2) Because the carbon doping suppressed the boron diffusion during the final RTA, the degradation of f_T due to the expansion of the intrinsic base and the reduction of BV_{CEO} due to the base concentration decrease could be suppressed. Furthermore, f_T was improved by the step-type Ge profile in the p-SiGeC/i-SiGe layer.

(3) There was an optimum value for the cap-Si layer thickness. f_T would decrease when it was too thick because the transit time of the emitter would become long. f_T would fall when it was too thin because the C_{EB} charge/discharge time would become long. When the final RTA temperature was set to 1000 ℃, f_T was lower on the low collector current side compared to 950 ℃ for two seconds even if the time was 10 ms. The result was the same as when the cap-Si layer was made too thin, and it was necessary to set the cap-Si layer thickness in anticipation of the increase in phosphorus diffusion.

(4) Compared to the case that the Ge concentration was the same in the p-SiGeC layer and the i-SiGe layer, f_T was improved in the step-type Ge profile. This result suggests that there is the possibility the step-type Ge profile could generate an accelerating electric field. At this time, even with the same Ge concentration step width, if the Ge concentration under the p-SiGeC layer was low, the f_T decreased. Increasing the Ge concentration under the p-SiGeC layer was necessary to generate a higher accelerating electric field.

(5) f_T of 200 GHz or more has been achieved by thinning the collector epitaxial growth layer. Furthermore, f_T has

increased from 226 GHz to 254 GHz by removing the intermediate STI separating the collector plug and intrinsic base region and reducing the collector resistance.

(6) f_T was improved by reducing the collector time constant by reducing the C_{CB} by narrowing the area of the Link base region that connected the base poly-Si layer and the intrinsic base region. f_T = 307 GHz and f_{MAX} = 180 GHz under the conditions of emitter size of 0.21×1.06 μm^2 and the p-SiGeC layer of 1-nm thickness were achieved.

(7) The p-SiGeC layer was sandwiched between the poly-SiGe layer grown from the base poly-Si electrode and the i-SiGe layer grown from the Si substrate to form a connecting base region. Initially, the thickness of the i-SiGe layer had been set to 32 nm. By thinning it to 23 nm, rbb' became lower, and f_{MAX} increased. It was presumed that the connecting resistance increased because the p-SiGeC layer with low resistivity could not be grown right under the base poly-Si electrode. On the other hand, rbb' increased when the i-SiGe layer was 17 nm. It is thought that the path for lateral diffusion of boron from the base poly-Si electrode was lost because the poly-SiGe layer could not be grown right under the base poly-Si electrode.

(8) The performance of f_T of 254 GHz and f_{MAX} of 325 GHz was achieved when the i-SiGe layer was 23 nm, the p-SiGeC layer was 2 nm, and the emitter size was reduced to 0.12×1.0 μm^2 to reduce the base resistance.

4.9 References

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5. Crosstalk Noise Propagation Characteristics in Thick-Layer SOI

5.1 Introduction and Purposes of This Study

Because analog circuit performance should be affected by the substrate structure including resistivity, SOI or high-resistance substrates might be selected depending on the application [1]-[11]. SOI substrates include thin-layer SOI substrates with a bonded Si layer thickness of approximately 0.1 μm or less and thick-layer SOI substrates with a thickness of 1 μm or more. The thin-layer SOI substrates have effectively improved MOS characteristics by reducing the short-channel effect and parasitic substrate capacitance [1][2]. On the other hand, the thick-layer SOI substrates have been used for applications such as BiCMOS and high-voltage MOS, where electrical isolation from the substrate side has been significant. Because the complete latch-up-free CMOS circuit can be realized by combining the thick-layer SOI wafer with a deep trench structure, it was used in combination with BiCMOS technology in systems that require high reliability, such as mainframe computers [3]. Furthermore, the thick-layer SOI having a high-resistance base substrate has been used to suppress noise propagation in the substrate in an RF circuit in which weak noise affects circuit characteristics. In high-voltage products, it has also been effective in ensuring the reliability of high-voltage switching ICs even in harsh environments affected by surge noise [9], [10].

The thick-layer SOI wafers have been used for the 0.25-μm generation SiGe BiCMOS for communication products (Fig. 5.1). The resistivity of bulk wafers used in CMOS Logic has been 10 Ω·cm. On the other hand, even though the bonded Si layer in which the devices are performed has the same 10 Ω·cm, a base substrate in the thick-

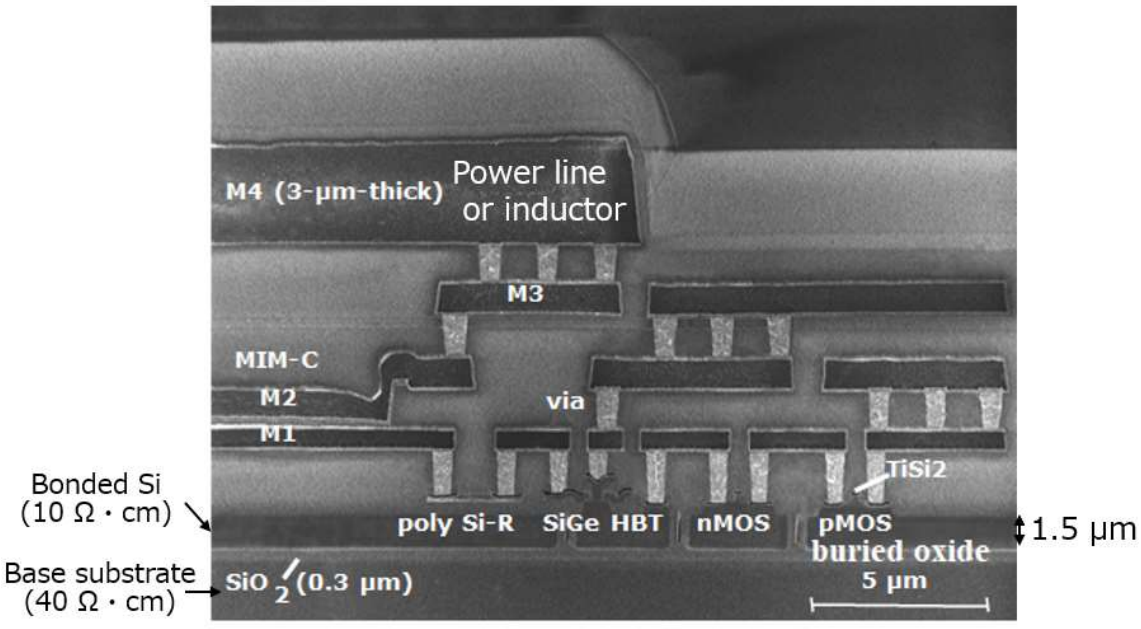


Fig. 5.1. SEM cross-sectional view of the 0.25 μm SiGe BiCMOS [7].

layer SOI wafers has been 40 Ω·cm or 1 kΩ·cm to suppress the crosstalk noise propagation. However, because the use of the thick-layer SOI for communication applications was limited to BiCMOS, there were no evaluation reports of signal propagation in thick-layer SOI, although there were technical papers on signal propagation characteristics in bulk wafers. This chapter clarifies the structure and resistivity dependence of crosstalk noise propagation in thick-layer SOI, which are essential in various applications of BiCMOS technologies, and describes improvement measures in layout design.

5.2 Outline of Study of Crosstalk Noise Propagation Characteristics

Propagation of crosstalk noise in a substrate varies depending on various parameters such as the structure or material of the substrate, including SOI [12]-[19]. Although many research results have been reported as guidelines for layout design optimization, the research results have focused on a non-SOI bulk substrate. Because the bonded Si layer other than the part where the device is formed is replaced with an oxide layer in the thin-layer SOI substrates, crosstalk noise propagates in the Si substrate just below the buried oxide layer. However, because the bonded Si layer remains after device formation in the thick-layer SOI substrates, it is necessary to consider crosstalk noise propagating in the bonded Si layer. This chapter examines crosstalk noise propagation through the thick-layer SOI and the narrow deep-trench isolation. Each device is completely isolated from a direct current by combining the deep trenches and the buried oxide layers. Still, alternating current passes through these isolation layers due to capacitive coupling. Crosstalk noise leads to malfunction of circuits and deterioration of analog signal quality. Accurately understanding the behavior of crosstalk noise on the deep trenches and SOI substrates applied to BiCMOS processes is an essential step in circuit design.

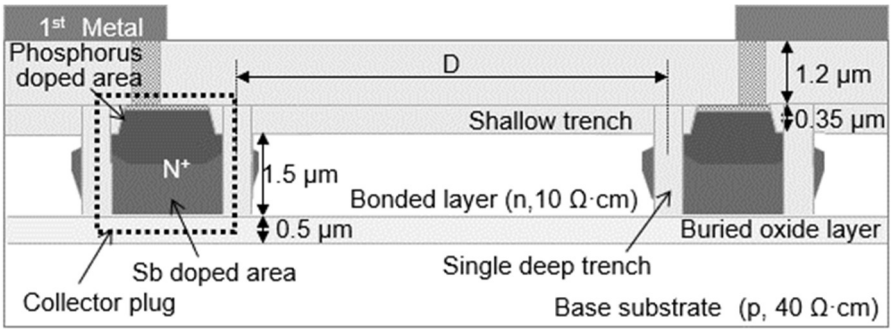
(1) Crosstalk noise propagation simulation

The three-dimensional (3-D) planar electromagnetic field (EM) ADS Momentum simulator [21] was used to simulate crosstalk-noise propagation in this study. In addition to ADS Momentum, crosstalk noise simulation results using the two-dimensional (2-D) device simulator (MEDICI) and the 3-D device simulator (DAVINCI) have been reported [12][16][21][22]. ADS Momentum can handle both permittivity and resistivity, but it cannot take the depletion layer caused by the effective impurity profile in the Si layer like these other device simulators. Because ADS Momentum has layers with only dielectric and resistive parameters, it cannot include the effects of a depletion layer tracing an accurate impurity profile. However, ADS Momentum is advantageous for device simulation because it has a close affinity with circuit simulation, and its EM simulation results can be directly used in circuit designs. Many analog circuit designers have widely used ADS Momentum, and it is advantageous for designers who do not own a device simulator to be able to simulate the effects of crosstalk in their designs. In this study, ADS Momentum's simulation results and the actual samples' measurement results were in good agreement. It was clear from the measurement results that deep trenches and SOI substrates had a particular effect in suppressing crosstalk noise propagation. It was found that the optimum design is possible through simulation.

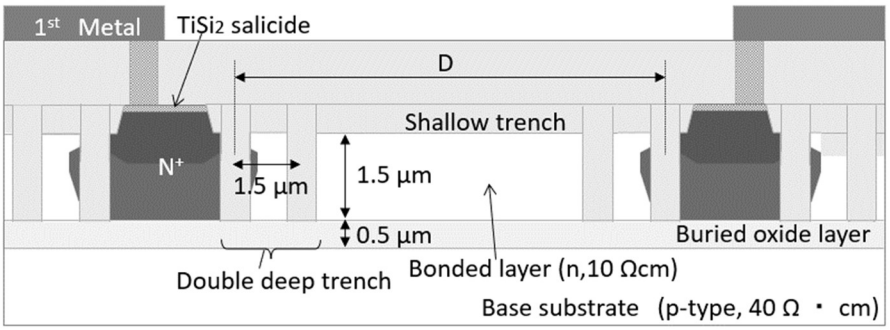
The crosstalk-noise propagation characteristics measured with various wafers and different deep-trench patterns were compared in this section. The optimal combination of thick-layer SOI substrate and deep-trench isolation was considered.

(2) Substrate configuration and test structure

Test structures were formed using the 0.25-μm SiGe-BiCMOS process in a 200-mm fabrication line [7]. N^+ doped buried layers, which were electrically connected with a substrate, were used as the collector plug regions of the collectors of NPN bipolar transistors. In the collector plug regions, Sb ions of 2×10^{15} cm^{-2} and phosphorus ions of 5×10^{15} cm^{-2} were implanted. Since Sb ions were diffused by one-hour annealing at 1200 ºC, the bottom of the collector plug region reached the buried oxide layer. Si epitaxial growth of 0.35-μm thickness was performed between the Sb implantation and phosphorus implantation processing steps. The sheet resistance of the Sb diffused layer was 38 Ω/□, and that of the phosphorus diffused layer was 20 Ω/□. The cross-section and top view of a typical configuration using a bonded SOI substrate were shown in Fig. 5.2 and Fig. 5.3. The bonded Si layer of the SOI wafer had the same resistivity of 10 Ω·cm (ordinary doping of n-type was 4×10^{14} cm^{-3}) as that of a standard bulk Si wafer to form MOS and bipolar transistors, but the p-substrate has relatively high resistivity of 40 Ω·cm (p–type impurity concentration was 3×10^{14} cm^{-3}) to achieve better signal propagation performance. The thicknesses of the bonded Si layer and the buried oxide layer were 1.5 μm and 0.5 μm, respectively. After the formation of 0.35-μm-thick shallow trenches, deep trenches were separately formed [6]. A 30-nm-thick pad oxide was performed at 1000 ºC before the deposition of high-density plasma (HDP) oxide for the shallow trenches, and a 4-nm-thick pad oxide was performed at 750 ºC before filling the deep trenches by thermal oxide deposition at 800 ºC. Both deposited oxide layers were densified at 950 ºC for 30 minutes. Double-deep trench isolation surrounding the collector plug regions in Fig. 5.2(b) was also investigated to suppress transmission crosstalk further. The Si island sandwiched by two trenches was electrically floating, so it did not work as a grounded shield.



(a) the single-deep trench isolation structure



(b) the double-deep trench isolation structure

Fig. 5.2. Schematic cross-section of test structures to measure the substrate coupling between two collector plug regions on the thick-layer SOI substrate.

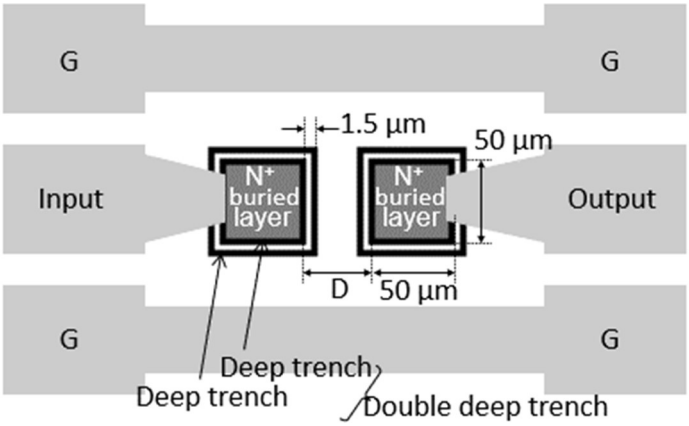


Fig. 5.3. Top view of a test structure for crosstalk analysis. The structure has the double-deep trench configuration shown in Fig. 5.2(b); the metallization pattern and collector plug region size are the same as those for the test pattern with a single-deep trench isolation structure.

$TiSi_2$ salicide was formed on diffusion layers to achieve sheet resistance of 3.5 Ω/□. A 1.2-µm-thick oxide layer was formed under the first metallization layer. The basic concept of this technology has been that deep trench isolation performs DC blocking even without a channel stopper [15], so channel stopper layers were not formed under shallow trench isolation in this investigation. The thickness of the 200-mm Si wafers was 725 µm. Because the backside of the wafers was covered by a thermally deposited oxide layer of 1.0-µm thickness, the backside was electrically floating during measurements at low frequencies. However, the wafer and measuring instrument stage were thought to be capacitively coupled at high frequencies.

Fig. 5.3 shows the top view of the test structure, which was the same as the test structures reported in [12] and [15]-[18]. Two 50-µm□ N^+-buried layers, which were used as a noise source and sensor, were surrounded by deep isolation trenches. The two N^+ doped layer contacts were separated by distances ranging from 10 µm to 100 µm. On-wafer two-port measurements were taken using two ground-signal-ground (GSG) microwave probes. An HP8510C vector network analyzer was used for the high-frequency range from 100 MHz to 40.1 GHz, and an HP4194 gain-phase analyzer for the low-frequency range under 100 MHz. The measurement system was calibrated by using the impedance standard substrate (ISS) of Cascade Microtech. Open calibration was not performed using an on-wafer pattern that did not make contact between the metallization pattern and the buried layers because it was assumed it would overestimate the effects of the pad capacitance at high frequency.

5.3 Consideration of Noise Propagation Suppression Effect by Deep Trenches

(1) Isolation effect of signal propagation by deep trench on SOI substrate with medium resistance (MR) SOI substrate

An SOI substrate having a base substrate of a 40-Ω·cm resistivity is called a medium resistance (MR) SOI substrate. The frequency dependence of S21 (pass characteristic from the input side) on the MR SOI substrates shows that deep trench isolation effectively reduced low-frequency crosstalk noise propagating through the thick-layer SOI substrates (Fig. 5.4). The frequency characteristics were almost flat up to about 5 GHz without the deep trench, and the coupling strength decreased as the distance (D) between the two ports increased. It means that no

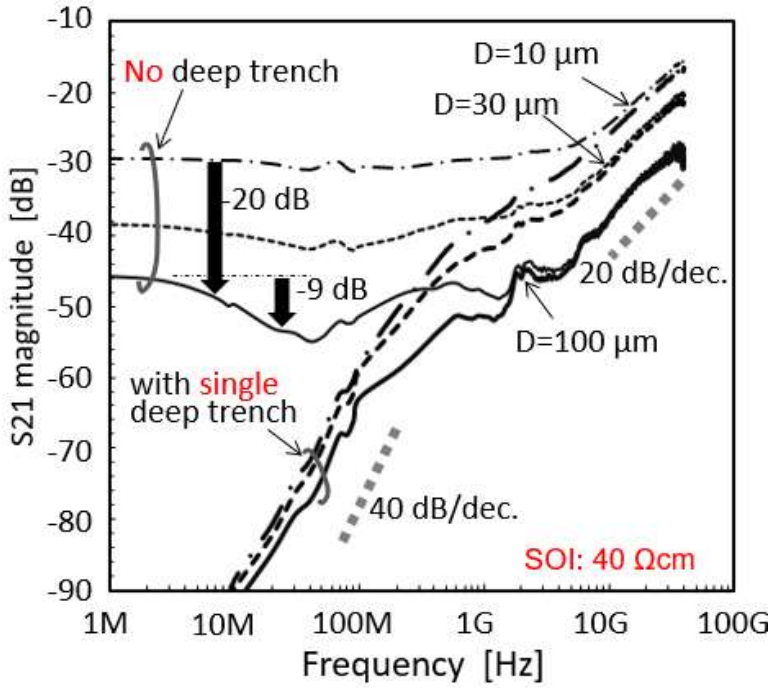


Fig. 5.4. Crosstalk measurement results on the thick-layer SOI substrate with and without a single-deep trench isolation structure.

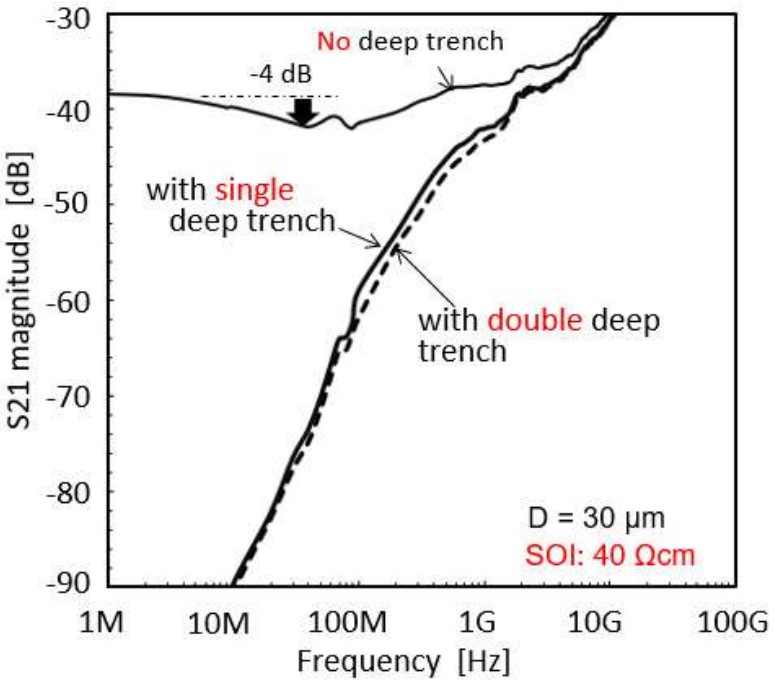


Fig. 5.5. Crosstalk measurement results on the thick 40-Ω·cm SOI substrate with no/single/double-deep trench isolation structure. The distance D between the two ports is 30 µm.

capacitive coupling caused frequency dependence in the case of no deep trench, and the noise was laterally propagating on the resistive coupling in the bonded Si layer. The deep trench guided the crosstalk noise downward into the substrate in this frequency range, and capacitive coupling through the buried oxide layer determined the

amount of transmission crosstalk. The thickness of the buried oxide layer and the width of the deep trench isolation structure were the same at 0.5 μm, but the 50 μm□ size of the N^+ collector plug area was about eight times that of the deep trench surrounding the collector plug region. The 40 dB/decade slope in the low-frequency region [12] with deep trenches indicated two capacitive couplings between the N^+ buried region and the Si substrate through the buried oxide layer on both sides of the signal input and the signal output. A stronger capacitive connection between the substrate and collector plug region determined crosstalk characteristics in the low-frequency range under 100 MHz. Transmission crosstalk for the configuration with deep trench isolation mainly flowed in the 40 Ω·cm substrate, and double-deep trench isolation was not effective for this case, as shown in Fig. 5.5. Consequently, the effectiveness of double-deep trench isolation was observed to be low from 100 MHz to 1 GHz. Under all configuration conditions, the scattering parameter S21 rises with a 20 dB/decade slope at frequencies above 5 GHz. In the high-frequency region of 5 GHz or higher, only one point of direct capacitive coupling between pads was dominant, so neither the buried oxide layer of SOI nor the deep trench had an isolation function.

Crosstalk noise transmission in the configuration without deep trench isolation mainly flowed inside the bonded layer. However, small capacitive coupling with the substrate through the buried oxide can be observed. The S21 parameter dropped 4 dB for a distance (D) of 30 μm, and it dropped 9 dB for D of 100 μm, as shown in Figs. 5.4 and 5.5. The small capacitive coupling can make part of the crosstalk noise transmission vertically downward into the 40-Ω·cm resistive substrate even without being guided by deep isolation trenches.

(2) Isolation effect of signal propagation by deep trench on bulk Si substrate

The transmission crosstalk in a bulk Si wafer was also investigated. The substrate resistivity and the depth of the deep trench isolation structure were 10 Ω·cm and 2.5 μm, respectively (Fig. 5.6). Because the type of doping for the bulk Si is different from that for the N^+ buried diffusion region, a depletion region spreads under the buried N^+ layer [27]. Capacitive coupling through the depletion region produces the frequency dependence shown in Fig. 5.7. An intermediate region between 20 dB/decade and 40 dB/decade in the slope of the frequency characteristics was seen in the bulk wafer as well as in SOI. The capacitive coupling with the substrate via the depletion region was in the frequency band of 1 GHz or less. In addition, signal propagation was determined by capacitive coupling between ports in the high-frequency band above 5 GHz, similar to SOI substrates. It did not depend on the structure of the substrate. Here, there was no difference in characteristics depending on the presence or absence of deep trenches in the case of bulk wafers. Deep trench isolation did not reduce transmission crosstalk for the bulk wafer case. This means that the addition of deep trenches extended the distance between the two ports by only 5 μm, which corresponds to the sum of the depths of the two deep trenches. It is assumed that the slight difference in

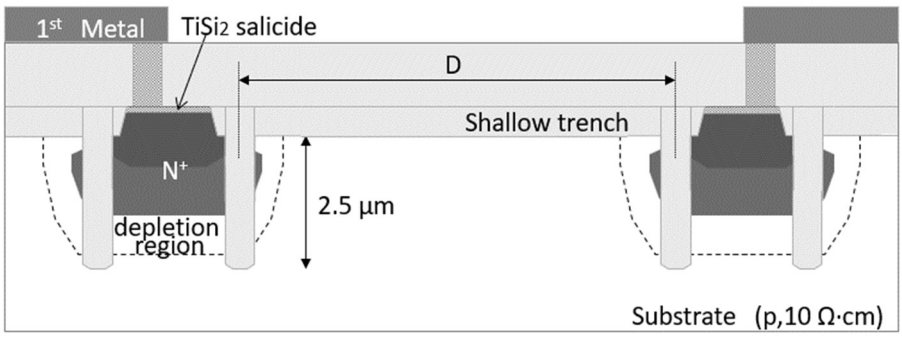


Fig. 5.6. Schematic cross-section of a configuration to measure crosstalk propagation on the bulk substrate.

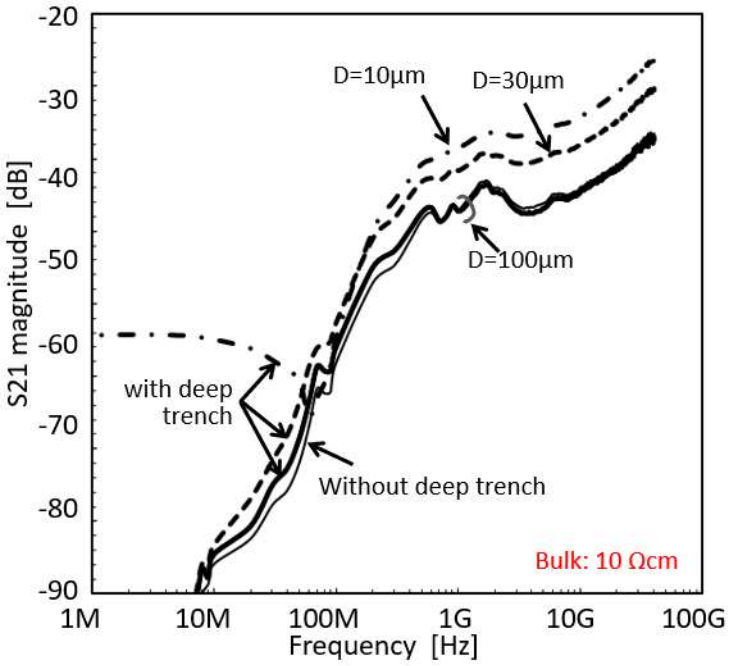


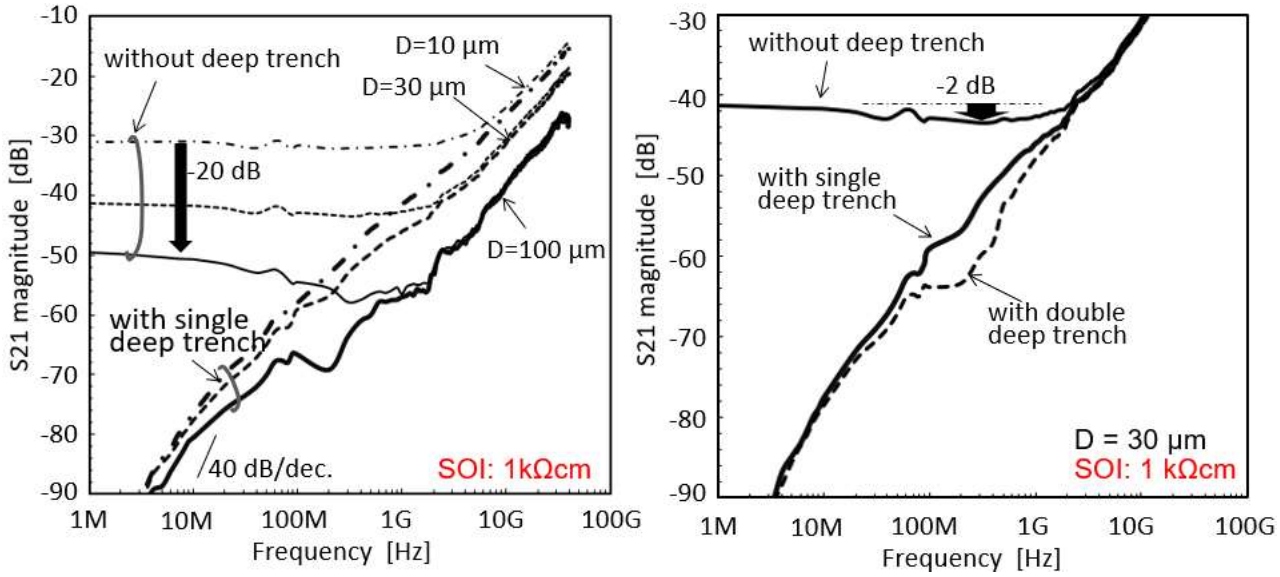
Fig. 5.7 Comparison of crosstalk propagation characteristics measured on the bulk substrate for no/single-deep trench isolation structure between an input and output terminal.

crosstalk characteristics among the different configurations is due to the different depletion region widths caused by deep trench isolation. In addition, when the distance between pads was 10 μm, the propagation characteristic was about -60 dB in the low-frequency region, and there was almost no frequency dependence. It was presumed that this phenomenon did not occur with an SOI substrate even if the base substrate was 10 Ω·cm because the isolation characteristics were not perfect due to no use of an SOI substrate.

(3) Isolation effect of signal propagation by deep trench on HR SOI substrate

High resistivity (HR) substrates have been attracting wide attention among RF circuit designers [23]-[24] because they can suppress crosstalk noises [12]. When a medium (40 Ω·cm) resistivity substrate was replaced with an HR (1-kΩ·cm) substrate, the resistivity of a bonded Si layer on the HR substrate was the same 10 Ω·cm as that for the bonded Si layer on the 40-Ω·cm substrate in Fig. 5.2. Since the HR substrate's impurity concentration is a very low $1'10^{13}$ cm^{-3}, the substrate's resistivity might fluctuate easily. Wafer vendor specifications guarantee at least 1-kΩ·cm resistivity. Thermal donor generation could be a parameter that induces fluctuation in HR substrate resistivity during the processing steps due to oxygen precipitation [25], [26]. Ref. [26] suggests that 1000 ºC furnace annealing to form diffusion layers of devices could suppress new donor generation at relatively low-temperature annealing of 450 ºC during metallization formation, so the final resistivity of the HR substrate should maintain the initial 1 kΩ·cm during all of the processing steps.

Even when the base substrate was replaced from the MR SOI substrate to the HR SOI substrate, the crosstalk noise passing through the bonded layer was cut off by the deep trenches, significantly reducing the propagation strength (Fig. 5.8). The reduction effect of the double-deep-trench structure, which showed no effect in the MR SOI substrate, was observed in the frequency range from 100 MHz to 1 GHz. The 20 dB/decade slope region expanded to the low-frequency region. This phenomenon appeared as a measurement result even in a structure



(a) Dependence on pad distance (b) Dependence on the number of deep trenches

Fig. 5.8. Comparison of crosstalk performance measured on the thick HR SOI substrate for the no/single/double-deep trench isolation structures.

without deep trenches. In the case of the MR SOI substrate without deep trenches, the S21 drop was 4 dB at around 30 MHz (Fig. 5.4). On the other hand, in the HR SOI substrate, the drop in S21 near 20 MHz was only 2 dB without deep trenches (Fig. 5.8). In addition, the frequency region where the S21 drop in the HR SOI substrate appeared was shifted to the high-frequency side by 40 MHz or more. The crosstalk noise propagation to the Si substrate side through the buried oxide layer in the intermediate frequency band decreased due to the increased substrate resistivity.

5.4 Resistivity Dependence of the Base Substrates

Fig. 5.9 compares crosstalk characteristics measured on the Si substrates with different resistivity. A plateau could be observed between the 20 dB/decade slope for the higher frequency range and the 40 dB/decade slope for the lower frequency range. The coupling with the substrate through the buried oxide or depletion region leads to a plateau in the mid-frequency range from 100 MHz to 10 GHz, and the effect of increasing the substrate resistivity was to lower the plateau [12]. Transmission crosstalk was effectively suppressed when increasing the resistivity from 10 Ω·cm to 40 Ω·cm, but raising it from 40 Ω·cm to 1 kΩ·cm showed little effect. First, it could be thought that a single-deep trench was insufficient to suppress noise current flow in a bonded layer. It has become clear that the effect of changing the substrate resistance cannot be sufficiently obtained unless the deep trenches are multiplexed when a high-resistance substrate is used.

Additionally, the substrate's high resistivity characteristics might be negatively affected by the parasitic surface conduction underneath the buried oxide layer [28][29]. Even though the composition surface of the bonded SOI wafer was between the buried oxide layer and a high resistivity Si substrate, it was thought that high-temperature annealing at 1200 ºC during the fabrication process should eliminate the fixed oxide charge Q_{ox} at the SiO_2/Si interface. However, the low-frequency slope of S21, which experiment results showed was close to 20 dB/decade, suggested the existence of Q_{ox}.

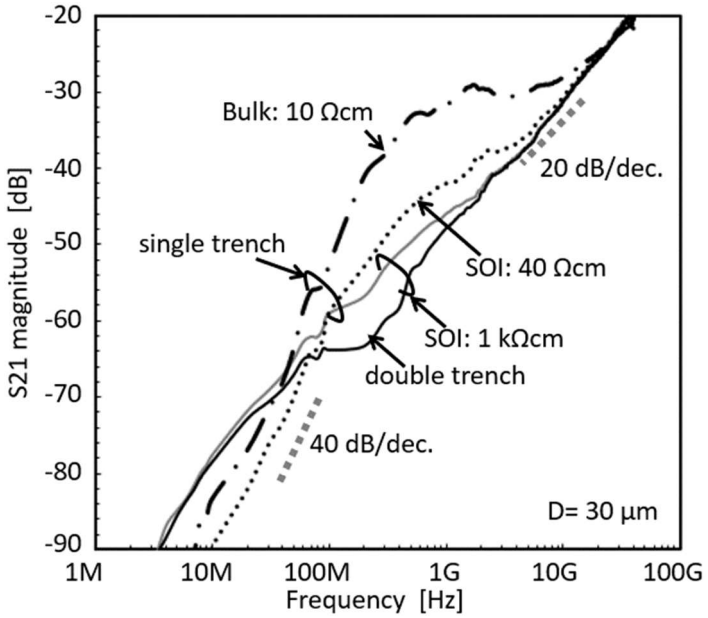


Fig. 5.9. Comparison of measured crosstalk propagation with single-deep trench isolation structure among bulk substrate, thick MR SOI wafer, and thick HR SOI wafer.

5.5 Optimal Design Derived from Simulation

Fig. 5.10 shows good agreement between measurement and EM simulation results for the 40-Ω·cm SOI substrate. The 40 dB/decade slope around 100 MHz obtained in the EM simulation was in good agreement with the device simulation and theoretical approach described in [12]. On the other hand, the EM simulation for the 1-kΩ·cm SOI substrate shows slightly lower transmission characteristics than measurement results (Fig. 5.11). This comparison also suggests high resistivity of the HR substrate was a little lower during the fabrication process.

The number of trial-and-error methods is limited, but simulation helps reach an optimized layout. The simulation

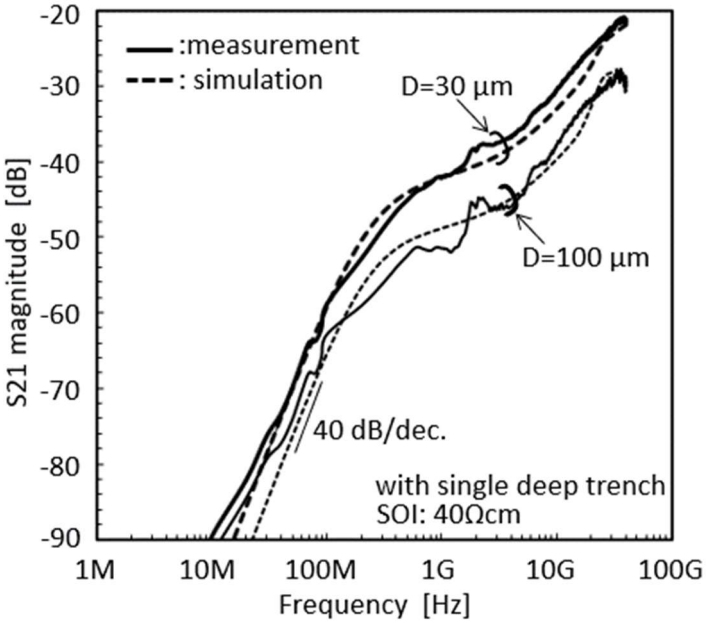


Fig. 5.10. Comparison of measurement and EM simulation results for the MR substrate with single-deep trench isolation.

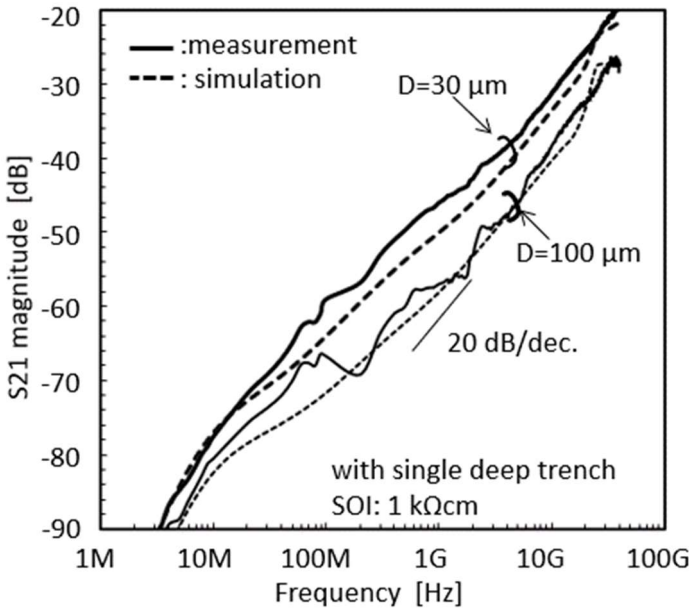
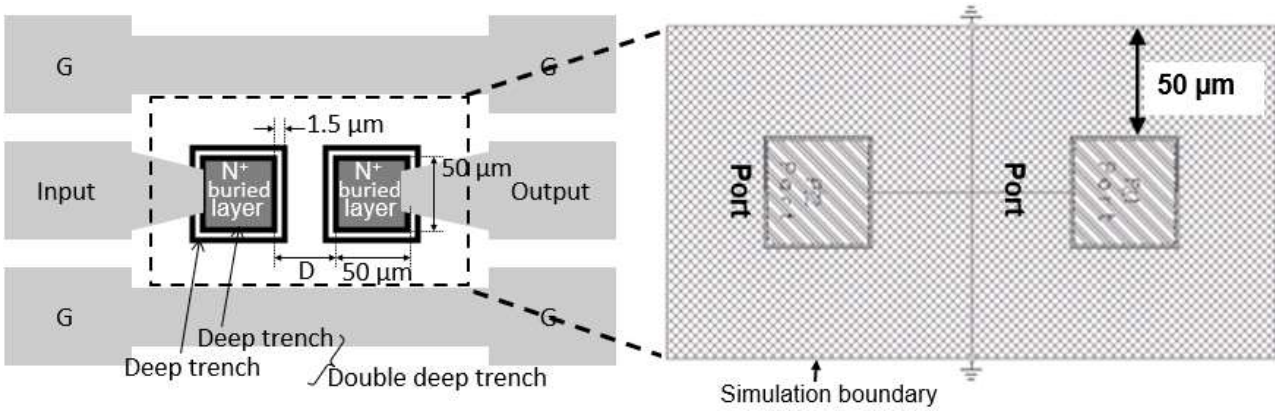


Fig. 5.11. Comparison of measurement and EM simulation results for the HR substrate with single-deep trench isolation.

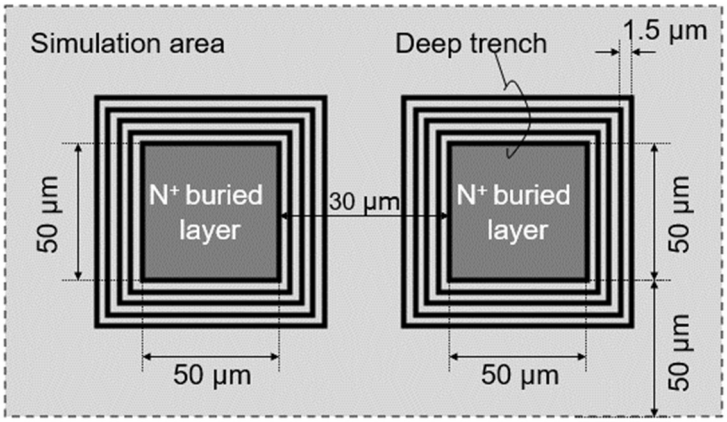


(a) Schematic view of the actual measurement pattern (b) Pattern of ADS Momentum Visualization

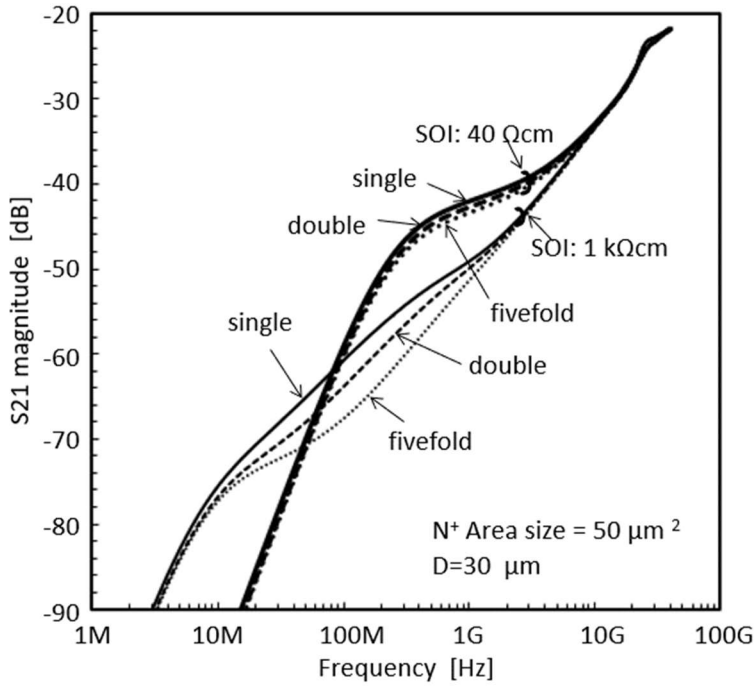
Fig. 5.12. Relation of ADS Momentum visualization pattern on the screen and actual measurement layout. The actual pattern includes a metallization layer, but the simulation pattern for ADS Momentum includes only Si and SiO_2 layers.

pattern described in this paper (Fig. 5.12) does not include a metallization layer to avoid parasitic capacitance effects between the substrate and the metallization layer. The simulation area includes the Si layer that has a 50 µm distance between its boundary and the edge of a buried doped layer surrounded by a deep trench filled with an oxide layer. If this distance is too short, reflection waves from the simulation boundary will appear in the simulation results. The 50-µm distance was long enough to avoid this effect. The substrate was grounded during the simulation, although its backside was floating during the measurements. Since the frequency characteristics of the simulation and the measured values matched, it was considered that the wafer and the stage of the measuring instrument were capacitively connected in the measurement frequency domain.

An optimized layout design leads to less transmission crosstalk, and more accurate simulation is critical to achieving sophisticated RF circuit design. Fig. 5.4 shows that extension of the distance from the noise source at



(a) Schematic view of the installed layout



(b) EM Simulation results

Fig. 5.13. EM simulation of deep trench and substrate resistivity dependence of crosstalk noise.

low frequency was ineffective, but reducing the circuit area size of the noise source can be expected to suppress the amount of transmission crosstalk. It calculated the degree to which noise could be stopped by reducing the circuit area size through the EM simulation. Fig. 5.13 shows simulation results for the deep trench isolation dependence as one example of crosstalk noise suppression. The EM simulation results indicated that the isolation effect of multiple deep trenches was small for the 40-Ω·cm SOI substrate and significant for the HR SOI substrate. This was the same tendency as that shown in Figs. 5.4 and 5.8. For the MR substrate, a single-deep trench isolation structure is enough to suppress the transaction crosstalk noise. A multiple deep trench configuration for the HR substrate suppresses the transmission crosstalk in the frequency range from 10 MHz to 1 GHz. It could be therefore considered that implementing deep trench isolation as much as possible will be effective in the case of using an HR substrate.

The following design guidelines are derived from the above results. In the low-frequency region under about 100 MHz, the crosstalk noise reaches the common metal measurement stage under the backside of the wafer after flowing on the Si substrate side via the buried oxide layer. It can be represented by an equivalent circuit in which two CR high-pass filters on the input and output sides are connected in series. Therefore, it has a frequency dependence of 40 dB/decade and no distance dependence in its transmission characteristics. Consequently, it is necessary to reduce the area of the circuit that is the noise source. On the other hand, crosstalk noise propagates in the lateral direction of the bonded layer in the high-frequency region above about 5 GHz. An equivalent circuit can be expressed as a single CR low-pass filter that directly connects pads and has a frequency dependence of 20 dB/decade. There is no effect of applying a high-resistance substrate or a deep trench, and only keeping a distance from a noise source to suppress noise propagation. The intermediate frequency region between about 100 MHz and about 5 GHz is a transition region between the low-frequency region under about 100 MHz and the high-frequency area above approximately 5 GHz and has little frequency dependence. In this frequency range, the reactance of the capacitive connection through the buried oxide layer was reduced to a negligible level, and only the resistance connection through the substrate worked. It is practical to increase the distance from the noise source, and the increase in the number of deep trench patterns is also effective when using a high-resistance substrate.

In this study, the collector plug region of an NPN transistor was chosen as the buried diffused layer. It was confirmed by ADS Momentum that a resistivity change in a buried doped layer does not significantly affect transmission simulation results. Replacing the N-well layer of a P-MOS transistor with the collector plug region of an NPN transistor did not change the simulation results. The ordinary P-well layer of an N-MOS transistor and the N-well of a P-MOS transistor both have a sheet resistance of around 1 kΩ/□, and it should be expected that a depletion layer will be formed in such relatively low impurity concentration layers. However, ADS Momentum cannot handle the parasitic capacitance in a depletion layer since it would change the amount of transmission crosstalk. If the N^+ buried diffusion region of the NPN bipolar transistor is changed to a MOS well layer, there is a possibility that the crosstalk noise characteristics will be different due to the depletion layer.

5.6 Conclusions

The resistivity of the bonded layer of the thick-layer SOI remains the same as the bulk wafer, while the base substrate's resistivity can be higher. Since the resistivity of the bonded layer in which the devices are formed is the same as that of the bulk wafer, modification of the PDK is kept to a minimum. And at the same time, the crosstalk noise propagation has been supposed to be reduced in high-speed applications such as 5G wireless communication by utilizing a high-resistivity base substrate. However, the use of thick-layer SOI in high-speed communication has been limited to BiCMOS, and there have yet to be any reports dealing with the crosstalk noise propagation characteristics of the thick-layer SOI.

This study evaluated the propagation characteristics of crosstalk noise in the thick-layer SOI and obtained the following findings.

(1) The 1.5 μm-thick bonded layer was also a propagation path for the crosstalk noise. Still, the crosstalk noise propagating in the bonded layer was suppressed significantly in the low-frequency range by surrounding the

noise source with deep trenches that isolated the bipolar transistors.

(2) Even though the lateral propagation of crosstalk noise was inhibited by surrounding the noise source with deep trenches, it propagated through the buried oxide layer to the supporting substrate side. When the resistivity of the base substrate was 40 Ω·cm, the propagation characteristics did not change even though the deep trenches surrounding the noise source were multiplexed. However, the crosstalk noise propagation was more suppressed by multiplexing on the high-resistance substrate. It was shown that only one deep trench was not enough to stop the noise propagation in the 10-Ω·cm-resistivity bonded layer in the case of the high-resistance substrate.

(3) At 100 MHz or less, the crosstalk noise propagates on the common metal measurement stage just under the base substrate as an intermediary. At this frequency range, the crosstalk noise propagation path was regarded as a high-pass filter consisting of two CR circuits on the input and output sides. Therefore, distance dependency between the noise source and the measurement terminal was not observed. At 1 GHz or over, it was a high-pass filter consisting of one CR circuit, and there was distance dependence between the two terminals. It became clear that it was essential to keep the distance from the noise source to suppress the noise propagation on the high-frequency side.

(4) There was good consistency between the electromagnetic (EM) simulation and measurement results. Based on the frequency to be considered and the required crosstalk noise attenuation dependent on the frequency, the distance from the noise source and the deep trench's patterns could be determined from the simulation.

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6. Technical Challenges to be Studied in the Future

6.1 Comparison of SiGe HBT Performance Levels

(1) Trends of device characteristics at each research institute and positioning of this result

Major R&D institutes for SiGe HBTs include Hitachi [1]-[6], IBM [7]-[10], IHP [11]-[18], Infineon [19]- [21], ST Microelectronics [22]-[26], Tower Jazz [27]-[29] and Freescale [30]-[32]. Because early SiGe HBTs of IBM and IHP adopted the SiGe blanket epitaxial growth technique, the device structure was a non-self-aligned structure type [33][34]. On the other hand, in this study, SiGe selective epitaxial growth technology was selected to maintain the superiority of the self-aligned structure that has been developed for a long time. When the SiGe layer was grown only on a Si substrate surface in an emitter hole using the selective epitaxial growth technique for forming the intrinsic base layer, the width of the extrinsic base region could be determined in a self-aligned manner, which reduced the base resistance and collector-base parasitic capacitance. Therefore, the f_{MAX} of the self-aligned structure was higher than that of the non-self-aligned structure with the same f_T. Since then, each company has achieved competitive performance by adopting a self-aligned structure while still using the SiGe Blanket epitaxial growth technique or combining the selective epitaxial growth and self-aligned structures. In 2014 when the results of this study were published in the technical paper [4], f_T = 320 GHz, f_{MAX} = 445 GHz [15] announced by IHP in 2011 was the highest frequency, and IBM [8][9] and STMicroelectronics [23][24] were ahead of others (Fig. 6.1). After that, while many research and development institutes stopped new development of SiGe HBT and BiCMOS

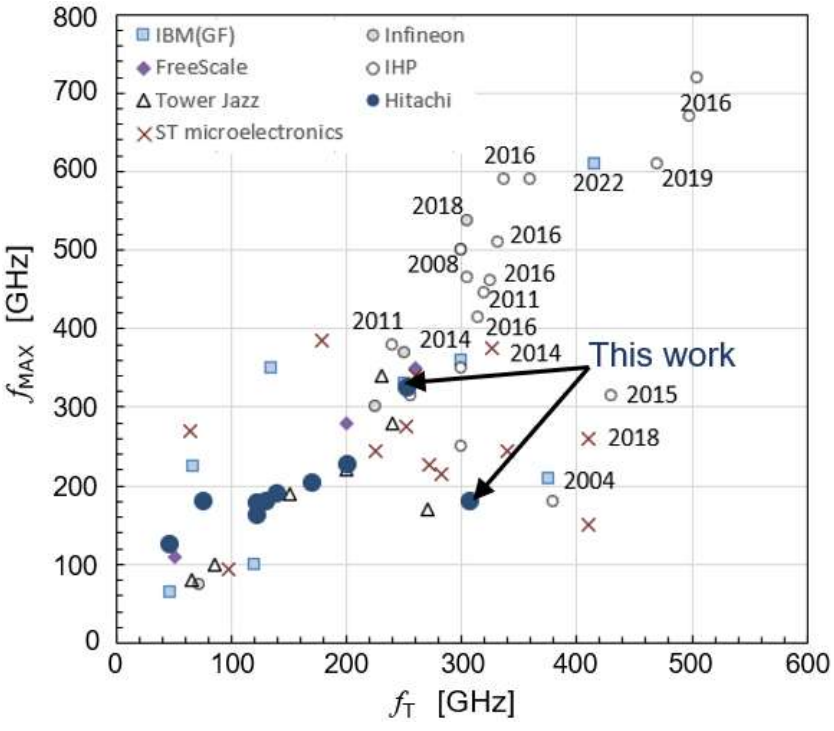


Fig. 6.1. Correlations between f_{MAX} and f_T in previous reports [1]-[34].

technology, IHP and European companies such as Infineon and STMicroelectronics, which have been jointly researching with IHP, have realized a significant increase in frequency since 2016.

On the other hand, BV_{CBO} is proportional to the reciprocal of collector transit time. In fact, there is a clear correlation between BV_{CBO} and f_T from the published values of each company (Fig. 6.2). Because the evaluation results of this study were on this straight correlation line, it was considered that the base transit time decided by the formation of the shallow junction of the intrinsic base layer was at a level comparable to others.

(2) Improvement points revealed by performance comparison with the highest performance

Comparing the cross-section of the SiGe HBT in this study with the IHP device that achieved the highest performance (f_T =505 GHz, f_{MAX} =720 GHz, BV_{CBO} =3.2 V) shown in Fig. 6.1 on the same scale, the width of the diffusion layer surrounded by the STI had a significant difference (0.48 μm vs. 0.27 μm). This difference in the width of the diffusion layer caused a considerable difference in C_{CB}, which could be presumed to have also affected

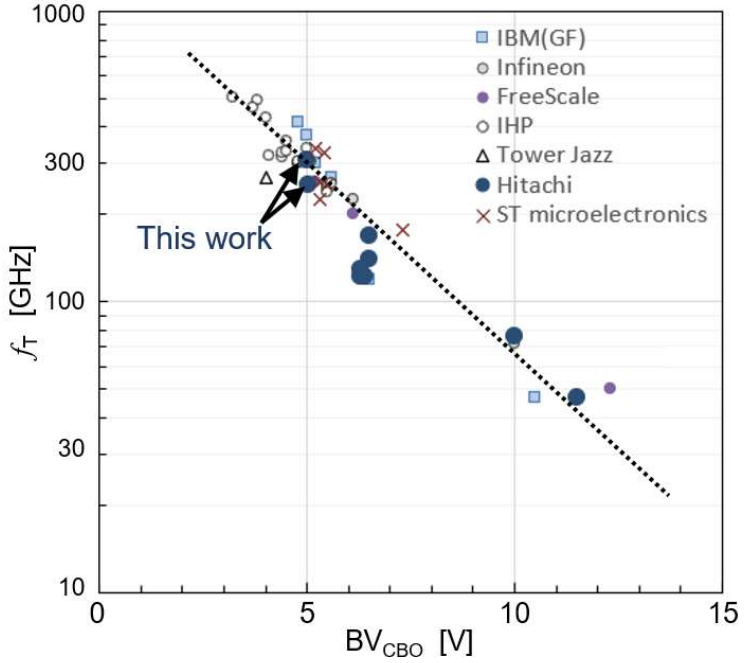
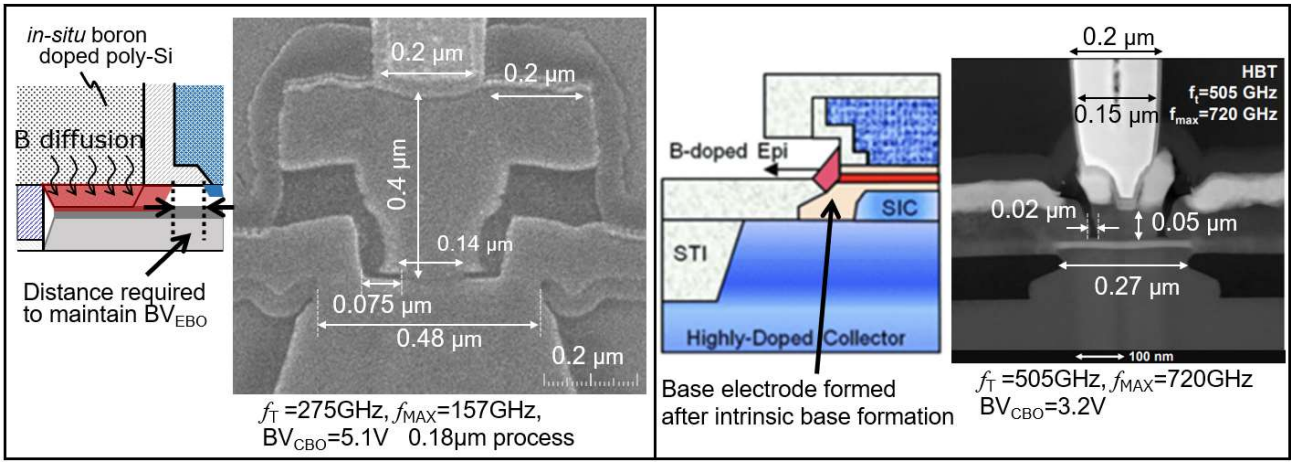


Fig. 6.2. Comparison of correlation of collector-base breakdown voltage (BV_{CBO}) and f_T with other research institutes [1]-[39].



(a) This work (2014) (b) IHP (2015)

Fig. 6.3. Cross-sectional comparison of the SiGe HBT developed in this study with IHP's SiGe HBT [18].

f_T and f_{MAX} (Fig. 6.3). Also, it was speculated that the difference in the sidewall length (0.075 μm vs. 0.02 μm) caused a difference in rbb', resulting in a significant difference in f_{MAX}. In addition, there was a marked difference in the thickness of the emitter poly-Si electrode, and a difference in the emitter resistance was presumed. This study's structure was not significantly changed based on the 0.18 μm SiGe HBT. It was judged that it had been necessary to review the details, such as the sidewall length.

On the other hand, there was no margin for aligning the emitter electrode and the contact hole in the IHP device structure. Because the BiCMOS process needs three-layer or four-layer alignment mediated by the MOS gate pattern, this IHP device would require more work to secure the yield at the production time. It could be thought from the contact hole size that the 0.13 μm process was applied in the IHP, but it is believed that the fine contact hole using the 90 nm process and expansion of the emitter electrode is necessary.

A low BV_{CBO} of 3.2 V at the device of IHP was also determined to be the cause of the significant difference in f_T. The thickness of the collector Si epitaxial growth layer was estimated to be about 50 nm, which was out of the scope of this study.

In the past, the IHP also used the same method for forming the contact between the base poly-Si electrode and the intrinsic base layer, as shown in Fig. 3.7(a). However, they determined that reducing the base resistance with this method was problematic. Therefore, the process was changed to form the base electrode by selective growth after forming up to the emitter electrode. This study considers that the connecting base resistance can be lowered even in Fig. 3.7(b), but this will be a future issue.

6.2 Further Speed Improvement and the 90 nm Node SiGe BiCMOS Process

The scalability up to the 0.13μm node SiGe BiCMOS was secured based on this study's 0.18 μm SiGe BiCMOS. On the other hand, the 90 nm node process is needed to reduce further parasitic capacitance and resistance for realizing f_T of 300 GHz or higher on a mass production basis while ensuring reproducibility, as mentioned in Section 6.1. As a development from this study results, the challenges in developing the 90 nm node SiGe BiCMOS are below.

(1) For realizing mixed with the 90 nm node CMOS

(i) Lowering the thermal budget of the SiGe epitaxial process so as not to affect the device characteristics of the 90 nm node CMOS

(ii) Suppression of the SiGe HBT height consistent with the 90 nm node process

(iii) Higher final RTA temperature from 1050 ℃ to 1075 ℃ and preservation of BV_{EBO} characteristics of the SiGe HBT

(iv) Verification of the influence of selective SiGe epitaxial growth process step that forms the strained Si in the S/D region on SiGe HBT performance

(2) For further improving the characteristics of the SiGe HBT

(v) Narrow emitter width to reduce rbb'

(vi) Review of base electrode formation method to reduce rbb'

The above issues are detailed below.

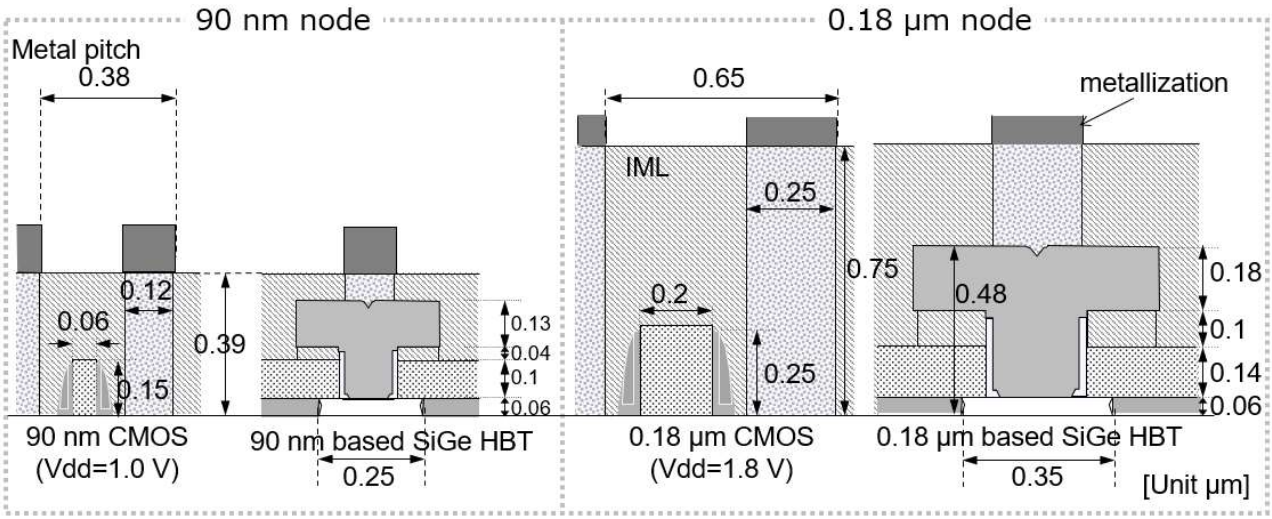


Fig. 6.4. Comparison of each dimension of the 90 nm node SiGe HBT and the 90 nm node SiGe HBT.

(i) Lowering the thermal budget of the SiGe epitaxial process so as not to affect the device characteristics of the 90 nm node CMOS

The impurity profile in the 90 nm node CMOS became further shallow and narrow, so it is expected that the SiGe HBT process is needed to be further suppressed in the thermal budget. Even when the H_2 annealing temperature was further lowered from 760 ℃ to 740 ℃, there was no issue with the emitter size of 0.2×1 μm^2 at the 100,000 devices in parallel. Still, leakage current occurred at a single device of the emitter size of 4×25 μm^2. H_2 annealing before the SiGe epitaxial growth has mainly been studied to lower the temperature until now, and the thermal budget reduction in parameters other than temperature, such as pressure and time reduction, has not been sufficiently studied (Fig. 2.21). Considering the thermal budget reduction other than temperature, it will be necessary to explore ways to improve the efficiency of oxide layer removal by changing the specifications of other items.

(ii) Suppression of the SiGe HBT height consistent with the 90 nm node process

The thickness of the collector Si epitaxial growth layer should be reduced until BV_{CBO} becomes 3 V to achieve f_T = 500 GHz and f_{MAX} = 750 GHz like IHP. It will also be necessary to use the 90 nm node process to reduce the CR time constant by junction area reduction of SiGe HBT and a short current path to achieve f_{MAX} = 750 GHz. At that time, it is necessary to reduce the height of the SiGe HBT from the 0.18 μm node, as described in Chapter 2, by thinning the base poly-Si electrode and the emitter poly-Si electrode (Fig. 6.4). In addition, it is necessary to narrow the contact hole (0.15 μm → 0.1 μm) at the IHP's 500-GHz-device process for securing the alignment margin between the emitter poly-Si electrode and the contact hole.

(iii) Higher final RTA temperature from 1050 °C to 1075 °C and maintenance of BV_{EBO} characteristics of the SiGe HBT

A final RTA temperature of 1050-1075 ℃ is assumed for the 90 nm node CMOS. It was necessary to thicken the cap-Si layer when changing from 950 ℃ for two seconds to 1000 ℃ for one second in the evaluation result of phosphorus diffusion from the emitter electrode. This thermal budget difference did not change even at 1000 ℃ for 10 ms. This result might indicate that the thermal budget during heating and cooling was not sufficiently

reduced, and it is necessary to consider reducing the thermal budget, including the heating and cooling speed at the time of applying 1050-1075 ℃.

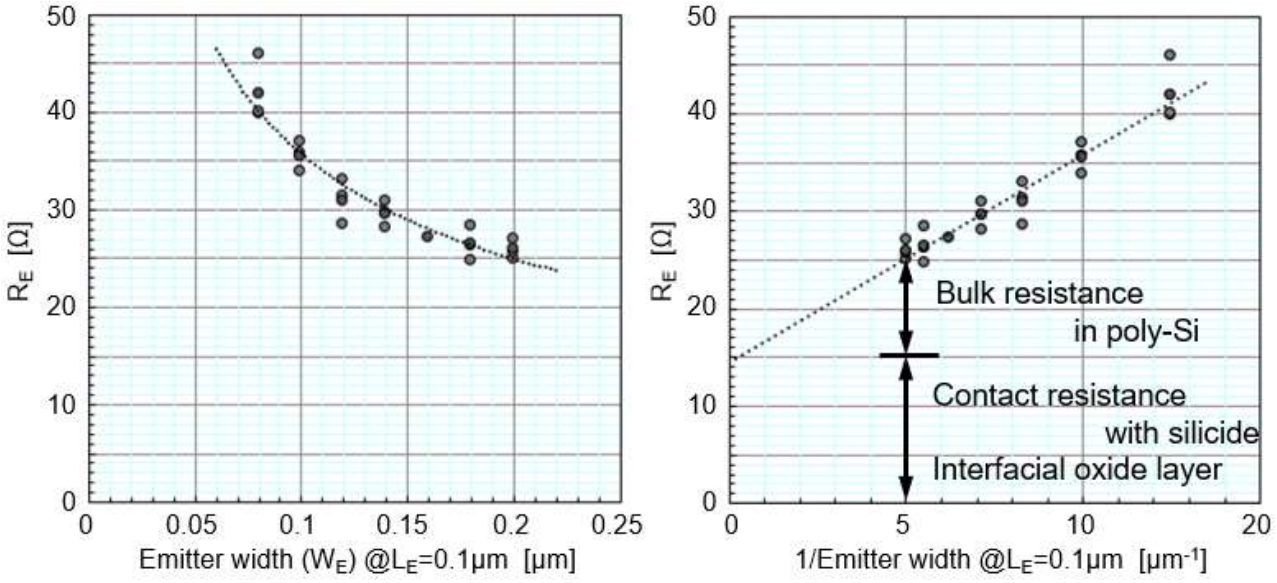
(iv) Verification of the influence of selective SiGe epitaxial growth process step that forms the strained Si in the S/D region on SiGe HBT performance

Strained Si structure, formed by a selective SiGe epitaxial growth layer to perform S/D regions, has been used from the 90 nm node CMOS to improve MOS characteristics. S/D formation is assumed after SiGe HBT formation, and it will be necessary to verify the influence of the S/D formation process on SiGe HBT characteristics. Since the SiGe epitaxial growth that forms the S/D regions is about 125 nm thicker than the SiGe HBT base formation, there is concern about the diffusion of the boron profile of the intrinsic base layer due to an increase in thermal budget.

(v) Narrow emitter width to reduce base resistance (rbb')

It is necessary to narrow the emitter width to reduce rbb' to improve $f_{MAX,}$ but the issue is how to suppress the emitter resistance (R_E) increase. R_E in a device with an emitter area of 0.2×1 μm^2 was 25 Ω, of which the poly-Si bulk resistance was 7 Ω. The conductivity of *in-situ* phosphorus-doped poly-Si was as low as 2.2×10^{-4} Ω·cm, so the bulk resistance ratio of poly-Si was not high (Fig. 6.5). Therefore, the increase in R_E when the emitter width is narrowed was not necessarily due to the narrowing of the current path of the poly-Si electrode. R_E is decomposed into elements of contact resistance between the silicide and the emitter poly-Si layer, bulk resistance of the emitter poly-Si layer, and interfacial resistance between the emitter poly-Si layer and the Si substrate. After decomposing the elements, it is necessary to take measures against the most significant factor.

The LP-CVD deposited the emitter poly-Si at 510-540 ℃, and there has always been an interfacial natural oxide layer between the emitter poly-Si and the Si substrate. However, a thicker interfacial oxide layer was found on the edge of the E-B electrode separation sidewall (SW) than on the middle of the emitter region (Fig. 6.6). It is presumed that the wet etching rate in the narrow area right under the base poly-Si electrode decreased during forming of the SW, and this was a reason for the increase in R_E when the emitter width was narrowed.



(a) Horizontal axis: emitter width (b) Horizontal axis: reciprocal of emitter width

Fig. 6.5. Emitter width dependence of emitter resistance (Emitter length = 1 μm constant).

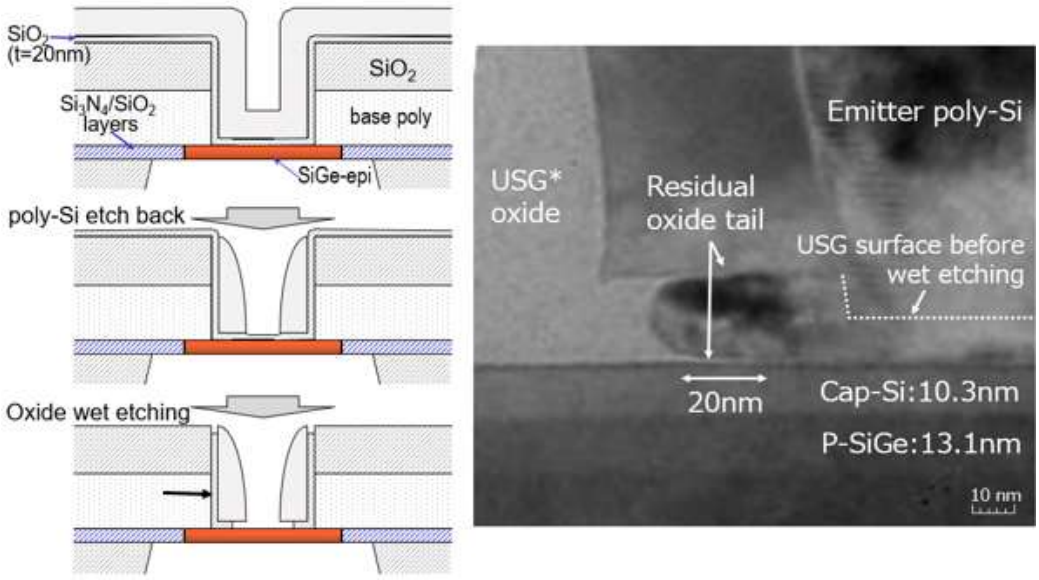
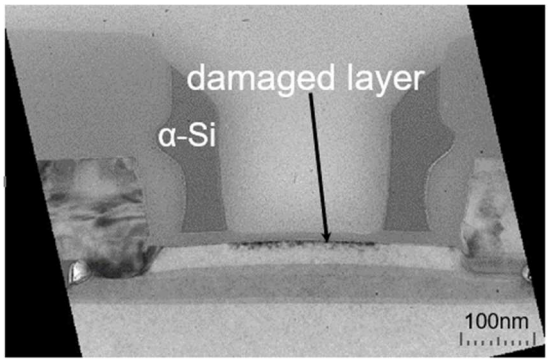
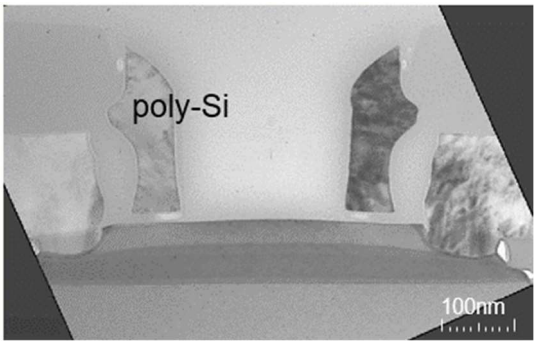


Fig. 6.6. The residual oxide layer occurred at the wet etching of the oxide layer of emitter-base (E-B) electrode separation.



(a) after the formation of poly-Si Sidewall



(b) after 800 ℃ annealing

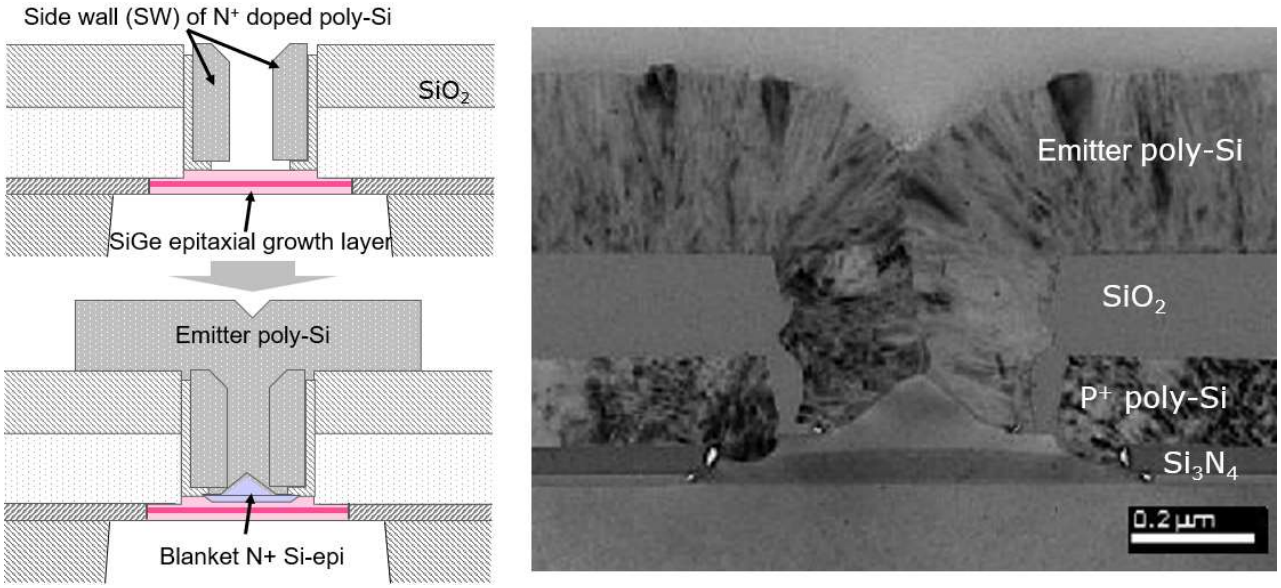
Fig. 6.7. TEM observation of dry etching damage in the cap-Si layer during poly-Si sidewall formation.

If the pad oxide layer under the base poly-Si layer of the SW is thinned and the amount of etching is reduced, the residual oxide layer would be reduced. At the time of thinning the SW pad oxide layer, the dry etching damage to the substrate must be cared for at the etching back to form the sidewall in the emitter hole. The dry etching should have stopped on the oxide layer. Still, the hydrogen molecules penetrated the 20 nm thick oxide layer and

damaged the cap-Si layer to a depth of about 10 nm (Fig. 6.7). In the case of the 20-nm pad oxide layer, the damaged layer disappeared even with H_2 annealing at 800 ℃, and the device yield was not affected. If the pad oxide layer becomes thinner, it will be necessary to confirm its influence on the p-SiGeC profile.

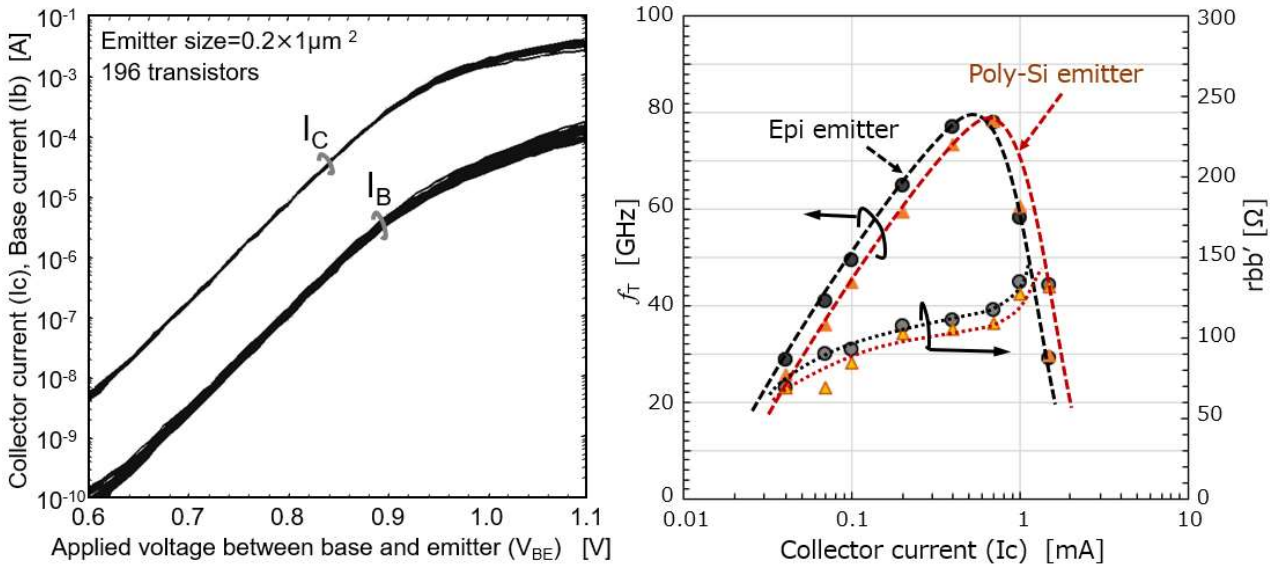
Another technique for lowering the emitter resistance is to form an emitter electrode using an epitaxial growth technique. An interfacial natural oxide layer was performed due to entrapped oxygen when the *in-situ* phosphorus-doped poly-Si layer was deposited at a batch furnace process of 510-540 ℃. This interfacial oxide layer has increased the emitter resistance. Instead of the emitter poly-Si deposition by the furnace LP-CVD, the emitter electrode without the interfacial oxide layer was formed by the single-wafer epitaxial growth technique used for performing the intrinsic base layers in this study. This technique has the potential to reduce emitter resistance. At this time, the blanket epitaxial growth of the phosphorus-doped Si layer was used for forming the emitter electrode. A Si crystal layer grew from the cap-Si layer, and a poly-Si layer grew from the sidewall poly-Si layer simultaneously (Fig. 6.8). Boron diffusion in the intrinsic base layer was of concern due to the H_2 anneal before epitaxial growth. In this experiment, H_2 annealing was performed at 800 ℃ for 2 minutes to remove the surface natural oxide layer before the epitaxial growth. There was no interfacial oxide layer between the substrate and the emitter epitaxial growth layer. The same AMAT Centra® Epi used for SiGe epitaxial growth was used for the bracket epitaxial growth.

The epi-emitter devices also showed no leakage current, as well as poly-Si emitter devices (Fig. 6.9(a)). The poly-Si emitter devices realized 2.68 V of BV_{EBO}, and the Epi-emitter devices realized 2.9 V with the same impurity profile of the 10 Gbps specification. The fact that the actual phosphorus concentration was 7.5×10^{19} cm^{-3} in the blanket epitaxial growth layer, much lower than the original target of 4×10^{20} cm^{-3}, was thought to have influenced the widening of the depletion layer between the emitter layer and the base layer. On the other hand, the emitter resistance increased only from 24 Ω to 27 Ω compared to the poly-Si emitter device, although the phosphorus concentration was much lower. It is thought that this was offset by the reduction due to the disappearance of the



(a) Formation flow from SW to Epi emitter (b) TEM cross-section after the Epi emitter formation

Fig. 6.8. Cross-sectional view of the epi-emitter and TEM observation results.



(a) I_C, I_B-V_{BE} characteristics (b) f_T, $r_{bb'}$-I_C characteristics (A_E=0.2×1 μm^2)

Fig. 6.9. Characteristics evaluation results of epitaxial emitter structure (10 Gbps spec.).

interfacial oxide layer, but the cause has not been clarified.

80 GHz of f_T, which was about the same as the poly-Si emitter structure, was realized with the impurity profile of 10 Gbps specification (Fig. 6.9(b)), and the epi-emitter structure did not affect the frequency characteristics. This result showed no sign indicating accelerating boron diffusion by H_2 annealing. Applying the epi-emitter structure to the 90 nm SiGe BiCMOS is expected to realize the fine SiGe HBT.

(vi) Review of base electrode formation method to reduce rbb'

IHP had conventionally used the technique of connecting the space right under the base poly-Si electrode by the selective SiGe epitaxial growth, which is the same as the structure adopted in this study (Fig. 3.7). However, they changed the base electrode formation process to achieve the high f_{MAX} of 600 GHz or higher. They proposed the structure in which the extrinsic base electrode was lately formed by the selective growth to be directly connected to the previously formed intrinsic base layer (Fig. 6.3(b)).

Although the details are unknown, another poly-Si layer was patterned under the base electrode contact hole. It is presumed that the base electrode was formed by the combination of the lateral epitaxial growth from the edge of the intrinsic base layer and the vertical growth from another poly-Si pattern, as shown in the cross-sectional TEM of Fig. 6.3(b). Forming the base electrode after forming the intrinsic base is the same method as SICOS in Fig. 1.15(b). This structure does not need to consider the intervening low-impurity layer right under the base electrode discussed in Section 4.7, and high f_{MAX} has been achieved by reducing the base resistance. A concern with this structure is the increase in C_{CB} and BV_{CBO} due to the proximity of the junction between the intrinsic base layer and the extrinsic base layer to the collector layer. Although high f_{MAX} and good f_T-BV_{CEO} correlation data were shown in the technical papers, the base poly-Si electrode structure in the 90 nm SiGe BiCMOS shall be determined after considering manufacturing variability in mass production.

6.3 Challenges in This Study in Comparison with Other Research Institutions Related to High Resistance Substrates

Trap-rich high resistivity SOI substrate has been commercialized since 2012 [35]. Holes are easily produced at the interface between the buried oxide layer (Buried OXide: BOX) and the substrate, and a channel layer through which electrons pass is likely to occur. On the other hand, electron propagation at the interface can be prevented by providing a poly-Si layer with a dangling bond that traps electrons right under the buried oxide layer. It has been reported that a nanometer-sized poly-Si layer right under the buried oxide effectively reduces the substrate resistance in the GHz band [36]-[40]. Although there was a significant difference in characteristics between the 10 Ω·cm bulk wafer and the 40 Ω·cm SOI in this study, the suppression of crosstalk on the high-resistance substrate was not as high as predicted by the simulation, and it was expected to be caused by fluctuations in resistivity during the process. Suppose channel inversion had occurred at the interface between the buried oxide layer and the Si base substrate. In that case, it can be thought that a similar phenomenon could happen, and it is considered that re-verification with the trap-rich substrate is necessary.

6.4 Conclusions

The following issues were described in this chapter as the future issues regarding improving high-frequency characteristics by the SiGe BiCMOS technology and the thick-layer SOI.

(1) It is necessary to reduce parasitic resistance and parasitic capacitance by lateral shrinkage using the 90 nm node process to achieve both f_T and f_{MAX} of 500 GHz or more, and the emitter width will also become about 80 nm. When applying the shrunk emitter, it is necessary to suppress the increase in emitter resistance. It is expected to take a countermeasure against the issue that the interfacial oxide layer between the emitter poly-Si electrode and the Si substrate is thickened right under the base poly-Si electrode. The interfacial oxide layer thickness right under the base poly-Si electrode can be made thinner by making the pad oxide layer thinner to form the sidewall (SW) structure. At that time, it is necessary to confirm the recovery of crystallinity because the etching damage caused by the poly-Si etching back will enter the substrate side through the thinned pad oxide layer.

(2) The epi-emitter device, which used the blanket epitaxial growth technique for the emitter electrode, is expected to suppress the reduction of emitter resistance because there is no interfacial oxide layer between the emitter electrode and Si substrate. In the first experiment with 10 Gbps specifications, good static and frequency characteristics could be achieved that were the same as those of the poly-Si emitter devices. Application to the 90 nm SiGe BiCMOS is an issue after addressing process issues such as the phosphorus concentration remaining at 7.5×10^{19} cm^{-3} compared to the target of 4×10^{20} cm^{-3}.

(3) It was impossible to confirm the excellent crosstalk noise propagation suppression effect of the high-resistance substrate compared to the 40-Ω·cm-resistivity substrate in this study. There was a possibility that the interface states right under the buried oxide layer in the SOI substrate affected the crosstalk noise propagation. It is necessary to evaluate the crosstalk noise propagation in a bonded layer without the effects of interface traps right under the buried oxide layer by using the trap-rich high resistivity SOI.

6.5 References

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7. Conclusions of This Study

The SiGe BiCMOS technology was constructed realizing the SiGe HBT with high-frequency characteristics of 250 GHz or higher and keeping compatibility with the standard CMOS. Furthermore, the frequency characteristics of crosstalk noise propagation were clarified in a thick-layer SOI, which has been limited to use in BiCMOS for high-frequency applications.

(1) The 0.13-0.18 μm CMOS was implemented on the SiGe BiCMOS with only minor channel dose modifications.

- Changed the layout rule from the HBT priority to the CMOS priority. High-speed HBT characteristics were achieved, although there was an effect on the device size of the HBT.
- Moisture desorbed from the CVD oxide layer on the base poly-Si formed an oxide layer on the substrate surface. The growth of the oxide layer was suppressed by changing the CVD oxide layer to the HDP layer, and the temperature of the H_2 annealing before the SiGe epitaxial growth was reduced to 760 °C. This minimized boron penetration through the gate oxide layer from the p-type gate during H_2 annealing.
- The base formation process changed from a combination of ion implantation and RTA to the SiGe epitaxial growth in addition to changing the batch-type furnace process to a single wafer type one, resulting in a significant reduction in temperature compared to the Si BJT process. Furthermore, the thermal budget in the SiGe epitaxial growth was reduced by adopting the SiGe selective growth without HCl gas. As a result, it could construct a BiCMOS process from 0.13 μm to 0.18 μm without degrading the short channel characteristics.

(2) Mass production technology for the SiGe epitaxial growth using LP-CVD was established.

- It was found that the accelerating electric field for the electron traveling was expected even in the step-type Ge profile from the result of the device simulation.
- Selective growth in SiGe epitaxial growth was secured even without HCl by using an oxide layer instead of a nitride layer for the insulating layer on the base poly-Si.
- It was clarified that the concentration of boron and Ge in the p-SiGeC layer depended on the area size of the epitaxial growth area. The layer quality deteriorated due to the influence of boron clusters when boron was doped above 1×10^{21} cm^{-3}, but the crystallinity was maintained up to 8×10^{20} cm^{-3}. In addition, 0.1-0.2 % carbon doping suppresses the boron diffusion, and the thinning of the intrinsic base layer was expected.
- Crystallinity was maintained up to 29.4 % Ge by adding a buffer layer (10 % Ge) right under the i-SiGe layer with a high Ge concentration.

(3) Achieved f_T and f_{MAX} over 250 GHz for 5G wireless and 77 GHz band Radar.

- f_T improved from 90 GHz to 180 GHz by thinning the p-SiGeC layer from 10 nm to 1.2 nm, but the thinning of the p-SiGeC layer alone did not reach 200 GHz. f_{MAX} decreased due to the increase in rbb' at 1.2 nm thickness.
- The carbon doping suppressed the f_T value decrease due to the intrinsic base thickness increase and the BV_{CEO} decrease due to the intrinsic base concentration decrease because the boron diffusion due to final RTA was

suppressed. In addition, an accelerating electric field could be formed to improve f_T by the step-type Ge profile in the p-SiGeC and i-SiGe layers. Furthermore, the transit time of the emitter became longer when the cap-Si layer was too thick, and the C_{EB} charge-discharge time became longer when it was too thin. It was clarified that there was an optimum thickness of the cap-Si layer to maintain a high f_T.

- 254 GHz of f_T was achieved by reducing R_C by eliminating intermediate STI between the intrinsic base layer and collector plug and lowering the collector time constant. In addition, the C_{CB} was decreased by narrowing the connecting base region, and f_T = 308 GHz and f_{MAX} = 180 GHz were achieved with the p-SiGeC thickness of 1 nm and $A_E = 0.21 \times 1.06$ μm^2.
- It was presumed that the increase in rbb' was due to insufficient growth of the p-SiGeC layer right under the base poly-Si electrode at the thickness of the i-SiGe layer was set to 32 nm at the beginning of this study. Reducing the thickness of the i-SiGe layer to 23 nm reduced rbb' and increased f_{MAX}. With the reduction of the base resistance by reducing the emitter size to 0.12×1.0 μm^2, the performance of 254 GHz of f_T and 325 GHz of f_{MAX} was realized with a p-SiGeC layer thickness of 2 nm.

(4) There were no technical reports of crosstalk noise propagation in a thick-layer SOI substrate because using thick-layer SOI in high-frequency applications has been limited to the BiCMOS. Therefore, it was necessary to clarify the crosstalk noise propagation characteristics.

- Deep-trench isolation suppressed the propagation of crosstalk noise through the bonded Si layer on the thick-layer SOI substrate. In particular, it was shown that multiple trenches were effective when using a high-resistivity substrate.
- There was good consistency between the electromagnetic (EM) simulation and measurement results. It was shown from actual measurements and simulations that the crosstalk noise transmission path depends on the frequency. The results also suggested that the distance from the noise source and the multiplicity of deep trenches must be determined from the frequency to be used and the required crosstalk noise attenuation.

(5) The following items were presented as future studies.

- It is necessary to reduce the emitter width to about 80 nm to realize f_T and f_{MAX} over 500 GHz. To realize the 80-nm emitter SiGe HBT, it is also necessary to reduce the thickness of the sidewall (SW) formation oxide layer as a countermeasure against the increase in the emitter resistance. At that time, it was suggested that confirming the recovery of crystallinity would be necessary because etching damage during the poly-Si-SW formation entered the substrate side through the pad oxide layer.
- It was shown that it is necessary to evaluate crosstalk noise propagation in a bonded SOI layer in a state where the influence of interface traps right under the buried oxide layer by trap-rich high resistivity SOI is eliminated.

Research Achievements

1.1 Submission of Articles to Academic Journals

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1.3 Patents

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