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# 論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）


Nonvolatile memories (NVMs) have been investigated for analog memory applications which require high-speed and low-power consumption. Recently, metal-ferroelectric-semiconductor field-effect-transistors (MFSFETs) are attracting much interest for analog memory applications due to its high-speed and low-voltage operation. Ferroelectric $HfO_2$ films have been investigated for MFSFET due to its scalability and Si compatibility. Although the doping has been generally used to induce the ferroelectric phases of $HfO_2$ film, it requires high-temperature crystallization annealing which leads to thick interfacial $SiO_2$ formation between $HfO_2$ film and Si substrates. It causes the depolarization field and consequently leads to the degradation of the retention characteristic of MFSFET. On the other hand, ferroelectric nondoped $HfO_2$ (FeND-$HfO_2$) thin films have been investigated for MFSFET application with its low-temperature process and threshold voltage ($V_{TH}$) controllability. Previously, MFSFET with 10-nm-thick FeND-$HfO_2$ gate insulator was realized by controlling the oxygen concentration during the reactive sputtering with Hf target. The memory window (MW) of 1.2 V was obtained by Pt gate electrode and post-metallization annealing (PMA) process. Meanwhile, further scaling of FeND-$HfO_2$ film thickness below 10 nm is necessary for high-speed and low-voltage operation. However, MFSFET with 5-nm-thick FeND-$HfO_2$ has not been realized due to an issue of leakage current of FeND-$HfO_2$ film below 10 nm. In this dissertation, the process conditions for thinner FeND-$HfO_2$ film formation below 10 nm were investigated. Then, the $V_{TH}$ control of MFSFET with 5-nm-thick FeND-$HfO_2$ gate insulator was examined for analog memory applications.

RF magnetron sputtering system was utilized for the deposition of 5-nm-thick FeND-$HfO_2$ gate insulator and the Pt gate electrode. MFSFETs were fabricated with the conventional gate-last process. After the channel stop and source/drain (S/D) region formation, 5-nm-thick FeND-$HfO_2$ films were deposited by reactive sputtering with $Kr/O_2$ gas flow ratio of 2.0/0.2 sccm and the sputtering power of 40–60 W at room temperature (RT). Then, 20-nm-thick Pt films were in-situ deposited using Ar or Kr gas flow rate of 4.4 sccm with the sputtering power of 30–80 W. After the S/D contacts formation by etching the Pt electrodes utilizing aqua regia, the PMA process was carried out at 500 °C for 30 s in $N_2$ ambient. Gate length (L) and width (W) were 3–10/15–90 μm, respectively.

First, the importance of plasma damage reduction for Pt gate electrode and FeND-$HfO_2$ below 10 nm was investigated. The ferroelectric properties of MFS diodes were investigated as the

sputtering power for Pt deposition was changed from 30 W to 80 W. The highest leakage current density of $1.5\times10^{-7}$ A/cm$^2$ at $V_G$ of -1.5 V was observed in case of the conventional condition of 80 W for Pt electrode deposition, while it was decreased to $2.8\times10^{-8}$ A/cm$^2$ in case of 40 W. Next, the sputtering power of 50 W for 5-nm-thick FeND-$HfO_2$ film formation was the most effective to reduce the leakage current, and the lowest leakage current of $1.2\times10^{-8}$ A/cm$^2$ was obtained at $V_G$ of -1.5 V. Furthermore, the highest remanent polarization ($2P_r$) of 4.5 μC/cm$^2$ was observed in P-V characteristics due to the reduction of leakage current and the improvement of crystallinity. Therefore, plasma damage reduction was effective to improve the ferroelectric property of MFS diode with the improvement of interface property and the quality of 5-nm-thick FeND-$HfO_2$ film.

Next, MFSFETs with 5-nm-thick FeND-$HfO_2$ gate insulator were fabricated utilizing the optimized conditions, and the device characteristics were examined. The etching time for gate region formation was precisely controlled because the deposition rate and etching rate of Pt electrode strongly depended on the sputtering conditions. In $I_D$-$V_G$ characteristics of MFSFET with 5-nm-thick FeND-$HfO_2$ gate insulator, counterclockwise hysteresis loops were observed indicating the ferroelectric property with the $V_G$ sweep range of ±1.5 V and the sweep rate of 0.24 V/s. Kr-plasma sputtering was effective to improve the ferroelectric property of MFSFET (L/W=3/15 μm) with the MW of 0.58 V with the program/erase (P/E) pulses of -5/5 V, 100 ms. Furthermore, the MW of 0.3 V was obtained with shorter P/E pulses of -5/5 V, 100 ns. The memory characteristic was expected to be maintained over 10 years of retention time with the erase/program current ratio ($I_{ERS}/I_{PRG}$) of $7.2\times10^3$ by Kr-plasma sputtering. The lowest noise spectral density ($S_{I_D}$) of $1.4\times10^{-17}$ A$^2$/Hz was shown in MFSFET (L/W=3/15 μm) at the frequency of 10 Hz. Therefore, the plasma damage reduction was effective to reduce the gate leakage current and to improve the memory characteristic of MFSFET with FeND-$HfO_2$ below 10 nm.

Finally, the $V_{TH}$ control of MFSFET with 5-nm-thick FeND-$HfO_2$ gate insulator was investigated for analog memory applications. The $V_{TH}$ of MFSFET was controlled with the number of input pulses. The input pulses were changed as 1–5 V for 100 ns–1 ms. The $V_{TH}$ of MFSFET was controllable as the number of identical erase pulses of 5 V/100 ns was changed from 1 to $10^4$. The $V_{TH}$ shift ($\Delta V_{TH}$) of 0.24 V was observed with the erase pulse of 5 V/100 ns, and the largest $\Delta V_{TH}$ of 0.34 V was obtained with the erase pulse number of $10^4$ which corresponds to 1 ms.

In conclusion, the MFSFET with 5-nm-thick FeND-$HfO_2$ gate insulator and Pt gate electrode was realized with decreasing the plasma damage for analog memory application. The reduction of plasma damage was effective to improve the ferroelectric property of MFSFET with 5-nm-thick FeND-$HfO_2$ gate insulator, and the $V_{TH}$ control of MFSFET was realized by input operation. Therefore, it is promising to realize high-speed and low-voltage operation of MFSFETs for analog memory application.