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Low-k 層間絶縁膜の界面熱抵抗に与えるアニーリング処理の効果

Effects of Annealing on Thermal Boundary Resistance of Low-k Interlayer Dielectrics

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Abstract

With the spread of applications that utilize technologies such as IoT, AI, and 5G, the demand for high-performance logic semiconductors that process enormous amounts of data continues to keep growing. Over the past several decades, higher performance and lower power consumption of semiconductors have been achieved mainly through miniaturization. However, with further miniaturization, the increase in current density due to finer wiring in interconnect structures generates a large amount of Joule heat, which leads to performance degradation of logic semiconductors. In previous studies, simulations using finite element methods have revealed that the thermal boundary resistance (TBR) between the metal and the interlayer dielectric in interconnect structures plays an important role in the temperature rise in logic semiconductors [1]. Therefore, investigation and improvement of the thermal properties in the boundary formed by interconnected metals and dielectrics are crucial for thermal management in logic semiconductor devices.

As shown in Figure 1, simulating films (Cu/Ta/TaN/SOG/Si-substrate) in stacking structure were fabricated on Si substrate, where dielectric layer was selected to be siloxane spin-on glass (SOG, one kind of low-k materials made by Honeywell International, Inc.): 111 and 512B, were deposited by spin coating. The thickness of the SOG layers were adjusted by changing the rotational speed and were determined by ellipsometer. On the top of SOG layer, the interconnect metal layer including a Cu layer of 10 nm, a liner layer (Ta) of 10 nm and barrier layer (TaN) of 10 nm was formed by sputtering. Subsequently, the simulating films were divided into two groups, one was annealed by an electric furnace. Finally, in order to evaluate the TBR of the simulating films, one more 100 nm-thick Au layer was deposited on the top of Cu/Ta/TaN/SOG/Si-substrate. Frequency-domain thermoreflectance method (FDTR) was employed to measure the thermal resistance and TBR of Cu/Ta/TaN/Si-substrate films, from which the thermal conductivity can be calculated [2], as shown in Figure 2(a).

Figure 2(a) presents the comparisons of thermal conductivities of 111 and 512B-SOG layers before and after annealing treatment. The conductivity was enhanced from 0.6 to 0.83 W/Km for 111-SOG layers, while from 0.34 to 0.45 W/Km for 512B-SOG layers. Accordingly, annealing treatment can enhance the thermal conductivity of 111-SOG films as well as 512B-SOG films, playing a conducive effect on thermal properties. Furthermore, in order to investigate the mechanisms and other effects on the thermal properties of SOG layers, interface analysis was also carried out by Fourier Transform Infrared Spectroscopy (FT-IR).

References

1. Zhan, T. *et al. ACS Appl. Mater. Interfaces* 12, 22347–22356 (2020).
2. Kato, R., Xu, Y. & Goto, M. *Jpn. J. Appl. Phys.* 50, 106602 (2011).

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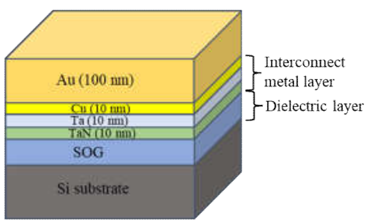

Figure 1. Schematic diagram of the interconnect metal layer (metal/liner/barrier)/dielectric film stacks simulating the interconnect structure.

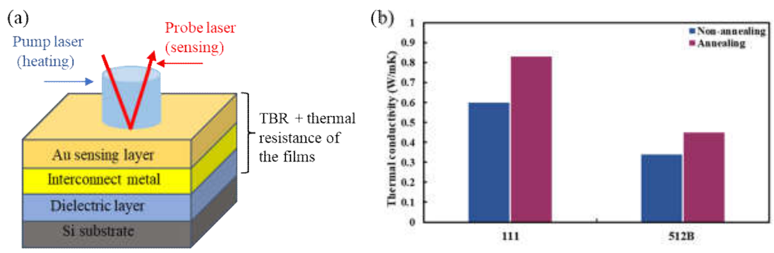

Figure 2. (a) Schematic diagram of the FDTR measurement system and (b) comparisons of thermal conductivities of 111, 512B-SOG dielectric layers before and after annealing.