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題目(和文)	
Title(English)	A study of charge sensing techniques in physically defined silicon quantum dots
著者(和文)	溝口来成
Author(English)	Raisei Mizokuchi
出典(和文)	学位:博士（工学）, 学位授与機関:東京工業大学, 報告番号:甲第12144号, 授与年月日:2021年12月31日, 学位の種別:課程博士, 審査員:小寺 哲夫,波多野 睦子,宮本 恭幸,若林 整,鈴木 左文,河野 行雄,小田 俊理,小林 正治
Citation(English)	Degree:Doctor (Engineering), Conferring organization: Tokyo Institute of Technology, Report number:甲第12144号, Conferred date:2021/12/31, Degree Type:Course doctor, Examiner:,,,,,,,
学位種別(和文)	博士論文
Type(English)	Doctoral Thesis

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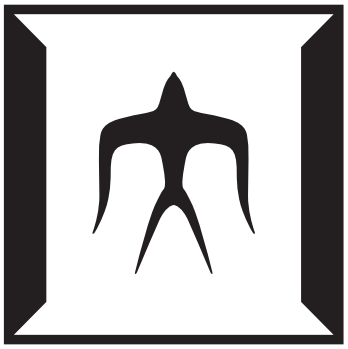
A study of charge sensing techniques in physically defined silicon quantum dots

14D14045
Raisei Mizokuchi

A dissertation submitted
for the degree of Doctor of Engineering

Supervised by
Associate Professor Tetsuo Kodera



Tokyo Institute of Technology
November 2021

Abstract

Qubits based on various quantum systems have been studied to build large-scale qubit systems. One promising qubit for larger-scale integration is a spin qubit in a silicon quantum dot, which has a small structure, long coherence time, and compatibility with existing CMOS technology. For the readout of a spin qubit, one measures spin-dependent charge distribution from the impedance change of the charge sensor via spin-to-charge conversion techniques. For quantum error correction, a fast (wide-bandwidth) measurement within the coherence time (about $10\,\mu$s) is of particular importance. On the other hand, a wide bandwidth will inevitably increase the noise; hence, it is not easy to achieve high-speed spin detection.

In this thesis, we study charge sensing techniques applied to silicon quantum dots. At first, we explore the low-temperature transport properties of two types of triple quantum dot devices: linear and triangular ones. The linear device has three tunnel-coupled quantum dots in line while the triangular device at each vertex of a triangle. This quantum dot system has the following advantages for large scale integration: 1) it is fabricated from an industry-standard silicon-on-insulator wafer; and 2) it is physically defined by the shape of the silicon channel layer itself, so that there is no need to use gate electrodes to define the quantum dot structure. In experiment, we studied charge transport through the systems by directly measuring the current and by charge sensing technique using additional QD structures. The results reveal the formation of each triple quantum dot system without unintentional QDs as expected. The present work realized a triangular triple quantum dot in silicon, which may pave a way for two-dimensional silicon QD system.

Next, we detect single tunneling events in a physically defined silicon triple quantum dot system. In measurements, we observe single-shot tunneling events by using a charge sensor; however, it turned out that the signals are too weak to acquire tunneling statistics by binary thresholding. To overcome this problem, we apply numerical treatments, one of which utilizes the maximum log-likelihood ratio test, and thereby, the step position is precisely indicated. Its superiority is confirmed by comparing a digital filtering in the simulation. The results demonstrate its potential for spin readouts from noisy environments.

Finally, we apply radio-frequency reflectometry technique to a physically defined silicon quantum dot system. To readout spins in this system, as in many other quantum dot systems, the radio-frequency reflectometry will be of a significant importance; however, measuring clear reflectometry signals depending on quantum states has so far been elusive. This is likely attributed to the top gate structure overlapping reservoirs, which causes leakage of radio-frequency signals. To avoid

this common problem of insensitivity, here we employ physically defined quantum dots without the top gate structure, leading to successful reflectometry as expected. Moreover, we observe large phase shifts corresponding to conductance peak of quantum dot (~ 45 degree). To reveal the mechanism, we analyze the data based on an equivalent circuit consisting of an inductor, a capacitor, a quantum dot impedance, and their parasitic components which are typically neglected in previous reflectometry studies. By a simulation with the equivalent circuit, the measurement data is successfully reproduced, which allows us to conclude that reflectometry phase signals can be greatly enhanced by a good impedance matching and an appropriate frequency detuning.

In conclusion, we have developed elemental technologies for fast charge detection using physically-defined silicon quantum dots: detection of charge states in a triangular triple quantum dot structure, which is the smallest unit of integration; single-shot measurement of single tunneling events of electrons supported by log-likelihood ratio test; realization of radio-frequency reflectometry in physically defined quantum dot for broadband sensing and the analysis using equivalent circuit. We believe that this work paves the way for large-scale QD integration and fast spin readout.

Contents

Chapter 1

Introduction

1.1 Quantum computation

General-purpose quantum computers are considered to enable solving problems which cannot be solved by classical computers on a practical time scale.[1] They are formed by minimum units called quantum bits or qubits. The qubits have two-level quantum states, and in analogy with bits in ordinary computers, the two levels of each qubit are encoded to "0" or "1"; in addition, superposition of the two digits is allowed, $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α and β are complex constants, and $|0\rangle$ and $|1\rangle$ are the quantum states. For a well-known quantum error correction code, two-dimensional arrays of several tens of million physical qubits are required to solve practical problems.[2] So far, various quantum systems have been developed as qubits: photons,[3] superconducting circuits,[4] spins in semiconductor quantum dots,[5] etc.

Following recent progresses in the quantum information field, major information technology companies like Google, IBM, and Intel have started to join this field. In 2019, Google demonstrated the quantum supremacy, the supremacy over classical computers, using 53 superconducting qubits.[6] In the paper, they claim that a problem which takes ten thousand years with supercomputer was solved in two

hundred seconds by quantum computer. The calculation by the quantum computer also demonstrated that the energy consumption is lower by a factor of 10^5 than for the same calculation by a supercomputer, due to the shorter calculation time and smaller power consumption. This result lets us envision the reality of practical quantum computation.

One of the reasons for the recent success of superconducting qubits is its structural similarity to classical circuits that facilitates the qubit design; the structure is an LC resonator that consists of a capacitor and a non-linear inductor using superconductor-insulator-superconductor junction (Josephson junction). When focusing on the most popular type of superconducting qubit called transmon, the energy contained in capacitance is designed to be much smaller than that of the Josephson junction, making the qubit insensitive to charge noise. This improves qubit characteristics and enables multiple qubit integrations. However, the footprint of one qubit ($\sim 1\,\mathrm{mm}^2$) is relatively larger than of other qubit systems. In addition, the qubit operation temperature is typically in tens of millikelvins to keep noise small. The combination of these two obstacles will limit further qubit integrations because of the restriction of cryogenic space with respect to size and cooling power. Hence, smaller qubits possibly working at higher temperature where cooling power is higher are more preferable.

Trapped ion qubits are one of candidates for quantum computation. This qubit utilizes charged ions trapped in a vacuum by oscillating electromagnetic field, having long coherence time due to almost no external disturbances. In addition, this qubit can be realized even at room temperature, and cryogenic operation (at $\sim 4\,\mathrm{K}$) improves the characteristics. Integration of several tens of trapped ion qubits have been reported recently.[7] However, large-scale qubit integration with this system may be challenging because of relatively large footprint per one qubit ($\sim 1\,\mu\mathrm{m}^2$) and because standard trapping techniques limits qubit arrays to one-dimensional ones. Therefore, other quantum systems suitable for two-dimensional integration

are desirable.

1.2 Semiconductor quantum dot qubits

Aiming towards the million-qubit systems, spin qubits based on semiconductor quantum dots (QDs) are promising because of the physical smallness and electrical tunability.[8, 9] A QD is a nano-size semiconductor block ($10 \sim 100\,\mathrm{nm}$) and can confine electrons or holes whose spins can be regarded as qubits.

The QD structure is superior to other spin qubits like dopant qubits, which utilizes sharp, identical quantum confinements of single dopants (phosphorus donor, typically) in silicon. Even though such dopant qubits show the significantly long coherence times, the sharp confinement prevents controlling couplings between dopant qubits, leading to difficulty in two-qubit gates.

As the semiconductor material for QDs, GaAs/AlGaAs heterostructures had been intensively studied in 2000s thanks to its low-disorder quantum well and low electron effective mass leading to clear quantum effects. However, it turned out that nuclear spins significantly degrade the coherence time of spin qubit, and hence, in 2010s, silicon, whose dominant isotopes are spinless, began to be preferred instead of GaAs, all of whose isotopes have nuclear spins. On the other hand, higher effective mass in silicon decreases energy level spacings in QD than in GaAs, so that smaller silicon QDs are required to compensate it. By overcoming these challenges, silicon-QD spin qubits have been realized, and the long coherence times have been observed as expected,[10] further boosted by isotopically purification.[11, 12]

Recently, integration of silicon QDs has been investigated. For quantum error correction, two-dimensional qubit integration will be important. A well-known error correction scheme [2] allows high error probability (around 1%) by considering nearest-neighbor couplings of two-dimensional qubit array. Taking into account the present state-of-the-art fidelity ([fidelity] = 1 – [error probability], roughly) of spin qubit operations, thousands of (physical) qubits are required to encode a (log-

ical) qubit. Recently, integrations of nine QDs and three qubits in linear arrays were reported, respectively.[13, 14] In addition, CEA-LETI, a research institute for electronics and information technologies in France, fabricated a two-by-four QD array with standard CMOS process.[15] For large-scale integration, such matured, present semiconductor technologies should play important roles. In these days, Intel and IBM also has fabricated their own QD qubit systems with their semiconductor technologies.[16, 17] However, these structures are dedicated to one-dimensional QD arrays, so that the development of expandable two-dimensional qubit array has still been anticipated.

Turning to the readout of spin qubits, charge sensing plays a crucial role. Readout of qubit is necessary for quantum computation, but, in addition to fragility of qubit, spin readout by a sensor is not easy, because spins do not couple with electrical environment directly. In the literature, spin-to-charge conversion techniques were developed,[18, 19] via which "spin" states are read out by "charge" sensing. The charge sensing is desired to be performed within spin operation time (e.g., $\sim 1\,\mu$s for electron spins) not to limit the quantum computation speed. To speed up qubit readouts, software and hardware techniques have been developed. From a software aspect, digital signal processing techniques can support readout, e.g., by precise step signal detection from noisy measurement results.[20] From a hardware aspect, radio-frequency (RF) reflectometry is commonly used to avoid low-frequency noise.[21] The technique is that RF signal is applied to device, and the reflected signal, related to device impedance, is measured. Here, RF is typically on the order of 100 MHz, so that the technique is immune from low-frequency noise such as $1/f$ noise.

1.3 Three eras for quantum computing

Aiming towards fault-tolerant quantum computing, there are three eras: 1. small-scale integration of qubits, 2. Noisy Intermediate-Scale Quantum devices

(NISQ), and 3. large-scale fault-tolerant quantum systems. Here, we briefly discuss each of them with possible milestones for silicon-QD spin qubits.

1. Small-scale integration of qubits (with ~ 10 qubits)

- Expandable qubit structure
- Qubit initialization
- Long coherence time
- Single-qubit gate
- Two-qubit gate
- Qubit readout

Era when researchers have been developing different qubits and seeking their future architecture. As of now, research for spin qubits is here. The above milestones are described by DiVicenzo's criteria.[22] State-of-the-art techniques realized a linear three spin qubit array in silicon, with agreement on the criteria.[14] Unlike this bottom-up approach, there are attempts based on a top-down one. In this approach, QDs are integrated with cryogenic electronics in a large-scale first, and then, each system component will be elaborated. [23]

2. Noisy Intermediate-Scale Quantum devices (NISQ) (with $50 \sim 100$ qubits):

- Intermediate-scale integration with a simple structure
- Moderately high fidelity
- High yield ratio of working qubit
- Cryogenic electronics
- Suppression of crosstalk between qubits

Era for quantum computing without error corrections; therefore, cumulative errors (mainly) limit the size of quantum calculations. Nevertheless, it is considered to be

meaningful for some practical calculations like quantum simulations.[24] For integration, the number of gate electrodes should be at minimum. In addition, three-dimensional gate electrodes and multilayer fan-out will be necessary. Spin readout with gate electrodes will further simplify the structure.[25] This gate-based readout utilizes RF reflectometry to read out small capacitance changes corresponding to spin states, so that signal multiplexing techniques enable simultaneous multi-qubit readout. A fast gate-based readout with a superconducting resonator ($\sim$ μs [26]) was reported, which is comparable to qubit operation sequences ($<$ coherence time, $\sim 10\,\mu$s). In addition, gate-based charge sensing within 50 ns has recently been performed by circuit improvement and using devices with strong gate-QD coupling,[27] so that hopefully it will not become the burden for NISQ calculation in future.

Yield ratio should be high enough, and its improvement may be the most challenging part in this era. This is because single atoms in tunnel barriers and/or a single atomic layer of silicon channel strongly affect the qubit characteristics. Simply thinking, the probability of $> 99\%$ that a qubit works will be required to obtain a working one from ten fabricated NISQ chips each including 100 qubits. It is not clear whether this value is feasible or not as of now, but industrial MOSFET fabrication techniques will be applicable and improve the yield ratio, as shown by the fact that ten billion of MOSFETs work in a latest CPU.

To realize dense spin qubit arrays, cryogenic electronics is important. For example, if each qubit has an LC resonator for RF reflectometry, the footprint of the LC resonators will be problematic. Cryogenic architectures in analogy with dynamic random access memory have been proposed, which can facilitate this problem.[28] The architectures enable time-domain multiplexing of RF signals and thereby reduces the number of LC resonators. The architectures can decrease the number of wires for potential controlling as well, leading to reduction of thermal budget from a bunch of cables (Fig. 1.1).[29, 30] Electronics like microwave generator and arbitrary waveform generator are also preferable to be located at cryogenic temperature

stages to reduce the thermal budget. The central challenge of cryo-electronics is the power dissipation. At 20 mK in a dilution refrigerator, cooling power of only 10 μW is available. One way to avoid this problem is placing the control chip at a higher temperature stage with a larger cooling power. Intel has been developing such a control chip, code-named "Horse Ridge".[31] This chip can output IQ-modulated microwave signals for spin qubit manipulations at cryogenic temperature (at 3 K, with 384 mW power consumption as described in Ref. 31). This signal generator works well so that the qubit performance keeps so high as with a room-temperature controller (99.7% fidelity). Another approach is integrating cryogenic controllers on the same chip as of qubits, further reducing the number of wires. This has a trade-off with power consumption. As mentioned above, cooling power of a mK stage is limited to μW, so that high temperature operation of qubit is needed. In the literature, it has demonstrated that spin qubits in silicon QDs works at 1 K, [32, 33] where the cooling power is several tens of milliwatt.

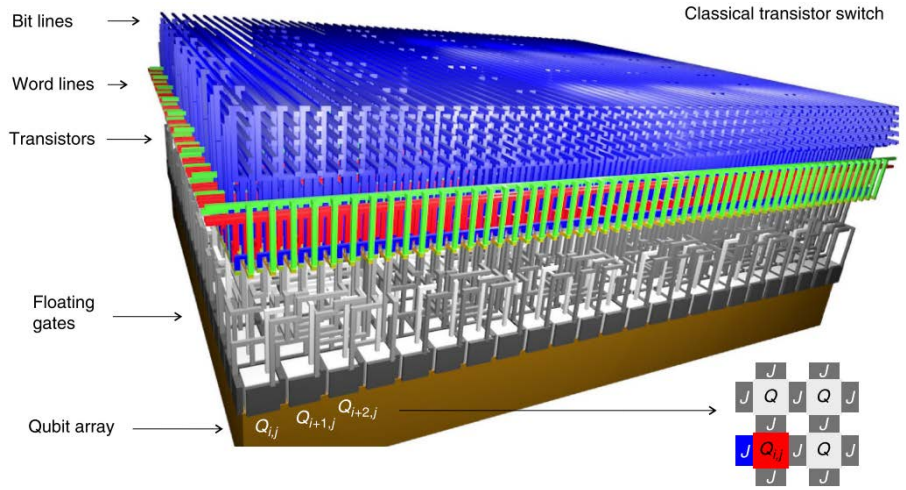


Figure 1.1: A two-dimensional qubit array with an architecture based on dynamic random access memory to control the potential of the qubits with a reduced number of wires. The number of wires are proportional to the square root of the number of qubits. This figure is adopted from Ref. 30.

QD arrays may suffer from crosstalk more strongly than other qubit systems

due to its high density of gate electrodes. Here, the crosstalk has two components; unintended qubit rotation by intended qubit operations via capacitive cross couplings and signal leakage from one line to others through capacitive couplings. The former can be suppressed by setting the operation resonance frequencies of qubits away from each others. Recently, results with 0.02% crosstalk has been reported.[34] The latter crosstalk component will also be suppressed by shielding of each high-frequency lines although it may take a lot of effort to develop device fabrication techniques.

3. Large-scale fault-tolerant quantum systems ($>$ 10 million qubits):

- Higher fidelity than error-correction threshold
- Quantum non-demolition measurement
- Long-range interaction
- ...

Era for practical quantum computing with quantum error correction. In error correction schemes, a (logical) qubit state is spread onto a state of multiple (physical) qubits. Such a redundancy makes a qubit robust against noises by checking errors in each physical qubit. For the correction, the fidelity of each physical qubit should be high enough, and it is theoretically demonstrated that 99% fidelity of several thousand of qubits in a two-dimensional array is required for error correction.[2] Even though 99.9% fidelity has been realized using spin qubits in silicon,[11] it is apparently a formidable task to expand it on a large scale.

Actually, there will still be a lot of milestones to realize fault-tolerant quantum computation. For example, non-demolition measurement plays an important role to feedback qubit error information,[35, 36] and long-range interaction can bridge different qubit arrays and make spaces for on-chip cryo-electronics.[29, 37, 38] Such

underlying techniques have been developed one by one in these days, so that merging them into a large quantum system will be one of main tasks in this era.

1.4 Silicon quantum dot structures

There are several structures to form silicon QD structures. We introduce three of them below: Gate-defined, Si nanowire, and physically defined QDs.

The gate-defined QDs are the conventional structure following standard GaAs QDs. This structure has fine gates on the surface of the Si/SiGe heterostructure or silicon substrate typically covered with an insulator layer. Small gates above a two-dimensional electron gas in silicon quantum well enable precise local control of the potential around the electrons, leading to almost ideal QD structures. In fact, so far, a lot of essential ingredients for general-purpose quantum computers have been established in this type of devices: high-fidelity single spin qubit,[11, 12] two-qubit operation,[39–42] spin-photon coupling for distant qubit coupling,[38] qubit operation at high temperature,[33] and quantum non-demolition measurement which is demanded for quantum error correction.[35, 36] On the other hand, the number of gates tends to be larger than other QD structures; large-scale integration with this structure is challenging.[43]

As another type of silicon QDs, Si nanowire QDs are well known. This structure has basically the same structure as MOSFETs; it consists of a drain and a source of a Si nanowire and a gate per one QD. Thanks to the thin effective oxide thickness of gate oxide, the gate-QD coupling is very strong, enabling fast gate-based sensing.[25] The gate-based sensing utilizes gate electrodes which can tune the potential of QDs for qubit readout and therefore is the most promising way to readout densely integrated QDs. In addition, the Si nanowire structure is completely compatible to classical circuits, which is advantageous for realization of on-chip cryogenic controller.[44] In these points, the structure is advantageous but, problematic in the respect of two-qubit gate operations where an additional gate between two

QDs is practically required to tune the QD-QD coupling. In addition, the structure based on a Si nanowire is one-dimensional-like, and therefore, there are difficulty for two-dimensional qubit integration.

As the third type of Si QDs, we introduce here physically defined QD (PD-QD) structure. A PD-QD is fabricated from an industry-standard silicon-on-insulator wafer and physically defined by electron beam lithography and dry etching processes, therefore having a good compatibility to CMOS techniques as well as Si nanowire QDs. This is advantageous for the integration because of no need to define quantum dot structure by gates and affording flexibility in QD arrangement.[45–51] This physical quantum confinement forms sharp, fine potential wells, which enlarges feature energy and will be thus suitable for high temperature operation. The realization of spin qubits with PD-QDs are in progress.

In this thesis, we develop charge sensing techniques by using PD-QDs. As mentioned above, two-dimensional integration of silicon QDs has been proposed and shown having an importance for error correction, but had not yet succeeded experimentally. This is possibly because of weak tunnel couplings due to low effective mass in silicon. In the present work, we first fabricate a unit of two-dimensional array, triangular triple QDs (TTQDs), by overcoming the difficulty with strong, sharp quantum confinements of physically defined QD structures. After confirming formation of TTQD, we developed readout techniques from the aspects of software and hardware using the QDs. The techniques are applicable to other QD systems, and we anticipate that it paves the way to improve readout in speed and accuracy.

1.5 This thesis

This thesis consists of seven chapters. Next to this chapter (Chapter 1 "**Introduction**"), we shall describe a theory for the charge transport through quantum dots and charge configuration (Chapter 2 "**Theoretical background**"). Here, the basics of an important charge sensing technique called RF reflectometry is ex-

plained as well. In Chapter 3 "**Device fabrication**," processes for fabrication of the PD-QDs are explained one by one. In the three following chapters, measurement results for charge sensing of the PD-QDs are presented. Chapter 4 "**Physically defined triple quantum dot systems in silicon on insulator**" reports realization of multiple-QD systems with three QDs. It shows the possibility of dense two-dimensional integration of spin qubits. Chapter 5 "**Tunneling event detection using single-shot measurements improved by numerical treatments**" focuses on detection of single-shot tunneling events, but the signals are weak and hidden in noise. To overcome this, log-likelihood ratio test is applied, and the capability of precise signal detection is demonstrated. Chapter 6 "**Radio-frequency single electron transistors with a sensitive phase response**" is devoted to RF reflectometry in a PD-QD. In the results, huge signals are observed, which are attributed to good impedance matching and a small frequency detuning from the resonance frequency. Finally, research perspectives towards qubit integration and fast qubit readout are given in the last chapter (Chapter 7 "**Conclusions**").

Chapter 2

Theoretical background

In this chapter, we explain characteristics of single, double, and triple quantum dot structures. In addition, the basic idea of single-shot spin readout by charge sensing is also mentioned. Finally, radio-frequency reflectometry, which plays an important role for fast charge sensing, is described from the point of view of electrical circuit theory.

2.1 Introduction

A quantum dot (QD) is a sub-μm-order semiconductor island charged with electrons or holes. Due to its three-dimensional quantum confinement, the structure is zero-dimensional, so that the eigenenergy is completely discretized. In the structure, charges are locally concentrated, and therefore, Coulomb interaction dominates the energy scale, and then the number of charges contained in a QD is restricted to be integer. When two and three QDs are connected, the structures are called double and triple QDs (DQD and TQD), respectively. In this chapter, first, we theoretically characterize these basic QD structures. Next, the basic ideas for charge sensing and radio frequency (RF) reflectometry are explained as well.

2.2 Single quantum dot

2.2.1 Charge states in a quantum dot

Spectroscopy of QD system has an importance to acquire the energy levels. Tunnel-coupled reservoirs facilitate the spectroscopy because the spectra are probed by current through the QD (Fig. 2.1(a)). Charges can tunnel one by one from one reservoir to the other through the discrete energy levels in QD, resulting in current peaks corresponding to the levels. From the transport behavior, QD system is sometimes referred to as single electron/hole transistor (SET/SHT). At first, we explain the discrete energy levels in a single QD (SQD) from a semi-classical description. Here, for simplicity, we shall consider a constant interaction model where Coulomb repulsion is independent of the number of electrons in the QD. Then, the total energy of electrons in the QD , $U(N)$, is

$$U(N) = \frac{(eN - C_{\mathrm{d}}V_{\mathrm{d}} - C_{\mathrm{s}}V_{\mathrm{s}} - C_{\mathrm{g}}V_{\mathrm{g}})^2}{2C} + \sum_{j=1}^{N} \varepsilon_j, \tag{2.1}$$

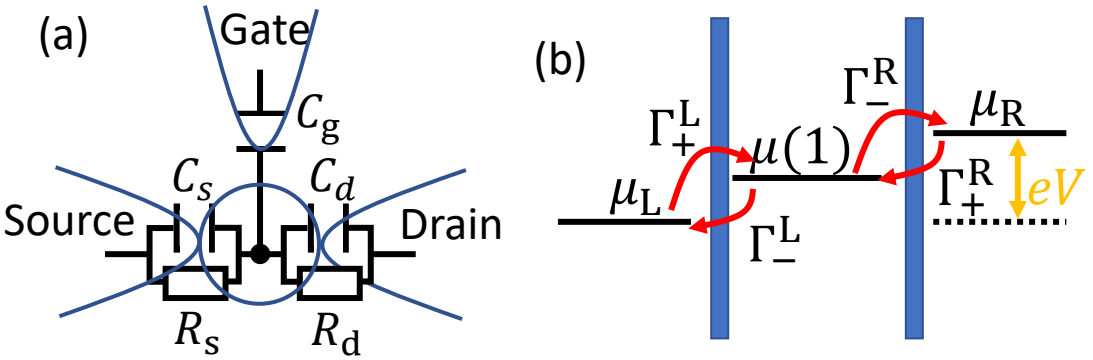


Figure 2.1: (a) An equivalent circuit for a SQD. SQD and gate are capacitively coupled (C_{g}), while drain and source reservoirs are tunnel-coupled to the SQD. A tunnel coupling is described parallel RC circuit (R_a and C_a where a = d, or s). (b) A toy model for master equation to estimate SQD conductance. Charges tunnel on and off the SQD with tunneling rates Γ. Here, only a single energy level in the SQD is assumed.

where e is a single electron charge, N the number of electrons in the QD, C the total capacitance of the QD, C_i the capacitance of electrode i, V_i the voltage applied to electrode i, and i = d, s, g corresponds to drain, source, and gate. ε_j is j-th eigenenergy of a single-particle Schrödinger equation for the QD confinement. From Eq. 2.1, the electrochemical potential required for adding N-th electron, $\mu(N)$, is obtained:

$$\mu(N) = U(N) - U(N-1) = \left(N - \frac{1}{2}\right) E_{\mathrm{C}} - \alpha_{\mathrm{d}} V_{\mathrm{d}} - \alpha_{\mathrm{s}} V_{\mathrm{s}} - \alpha_{\mathrm{g}} V_{\mathrm{g}} + \varepsilon_N \qquad (2.2)$$

where $E_{\mathrm{C}} = e^2/C$ and $\alpha_i = e(C_{\mathrm{i}}/C)$. E_{C} and α are important parameters to characterize QD, and thus named as charging energy and conversion factor, respectively. From Eq. 2.2, the energy spacing between two sequential electrochemical potentials, referred to as addition energy $E_{\mathrm{add}}(N)$, is

$$E_{\mathrm{add}}(N) = \mu(N+1) - \mu(N) = E_{\mathrm{C}} + (\varepsilon_{N+1} - \varepsilon_N). \qquad (2.3)$$

Therefore, it turns out that the energy levels are mainly determined by E_{C}.

In a simple case, C is described by summation of gate, drain, and source capacitances; in reality, self-capacitance C_{self} should also affects. A self-capacitance is a capacitance of the object itself, in other words, capacitance between the object and the infinitely away reference point. The value is a function of the radius of the object. For a two-dimensional disk, which corresponds to our silicon QDs in this thesis, $C_{\mathrm{self}} = 4\epsilon_{\mathrm{r}}\epsilon_0 d$, where ϵ_0 is the vacuum permittivity, ϵ_{r} the relative permittivity of the material, d the diameter of the disk.[52] When C_{self} is dominant in C, the diameters of QDs can be estimated from measured E_{C} by the rough approximation that $C \sim C_{\mathrm{self}}$.

2.2.2 Transport through a quantum dot

Next, we shall derive steady current through a SQD from a classical master equations for a toy model where a single electrochemical potential in QD and two reservoirs are tunnel-coupled with energy-dependent tunneling rates (Fig. 2.1(b)).[53, 54] We therefore assume two states in QD, with and without a single electron, and hence we define two possibilities whether one finds the electron or not, P_1 and P_0, respectively. Considering the tunneling rates for adding an electron and removing an electron, Γ_+ and Γ_-, respectively, one obtains a classical master equation as below:

$$P_0 + P_1 = 1, \tag{2.4}$$

$$\frac{dP_0}{dt} = -\Gamma^+ P_0 + \Gamma^- P_1 = -\frac{dP_1}{dt}. \tag{2.5}$$

where $\Gamma^\sigma = \Gamma^\sigma_{\rm L} + \Gamma^\sigma_{\rm R}$, $\sigma = +$ or $-$, and $\Gamma^\sigma_{\rm L}$ and $\Gamma^\sigma_{\rm R}$ are tunneling rate for left and right barriers, respectively. Current through the QD, I, is equal to currents through left and right barriers ($I_{\rm L}$ and $I_{\rm R}$) when the polarity is ignored, and then, in the limit that $dP_0/dt = 0$,

$$I = I_{\rm L} = -I_{\rm R} = e(\Gamma^+_{\rm L} P_0 - \Gamma^-_{\rm L} P_1) \tag{2.6}$$

$$= \frac{e(\Gamma^+_{\rm L}\Gamma^-_{\rm R} - \Gamma^-_{\rm L}\Gamma^+_{\rm R})}{\Gamma^-\Gamma^+} \tag{2.7}$$

$$= \frac{2e}{\hbar}\frac{\gamma_{\rm L}\gamma_{\rm R}}{\gamma_{\rm L}+\gamma_{\rm R}}(f_{\rm L}(\varepsilon) - f_{\rm R}(\varepsilon)), \tag{2.8}$$

where e is a single electron charge, $\Gamma^+_\alpha = 2\gamma_\alpha/\hbar * f_\alpha(\varepsilon)$, $\Gamma^-_\alpha = 2\gamma_\alpha/\hbar * (1 - f_\alpha(\varepsilon))$, $f_\alpha(\varepsilon) = 1/(1 + \exp((\varepsilon - \mu_\alpha)/k_{\rm B}T))$ is a Fermi distribution function, $\hbar$ is the Dirac constant, ε is the energy of the QD state, μ_α is the Fermi level in the reservoir, T is the temperature of charges and $\alpha =$ L or R. To obtain Eq. 2.7, we have substituted Eq. 2.4 and have assumed a steady current where Eq. 2.5 is equal to zero. Here, γ includes a tunnel coupling between the QD and a reservoir and density of states in

the reservoir.[53] Eq. 2.8 for multiple charge states is plotted as a function of ε and as a function of bias voltage $V = \mu_{\mathrm{R}} - \mu_{\mathrm{L}}$, where peaks and a current blockade area appear, respectively (Fig. 2.2(a) and (b)). The peaks are called Coulomb peaks, while the current blockade is called Coulomb blockade. When multiple energy levels are taken into account, and the QD current is plotted as a function of V and gate voltage V_{g}, the blockade areas seems diamond-like in V-V_{g} plane, which are referred to as Coulomob diamonds (Fig. 2.2(c)). One can obtain the addition energy and conversion factor of a SQD from this Coulomb diamond measurement. At the vertexes of the diamond for $V_{\mathrm{ds}} \neq 0\,\mathrm{V}$, the bias voltage aligns with energy spacing between QD electrochemical potentials with charge numbers different by one. Thus, the height of the diamond from zero bias voltage is equal to addition energy: $E_{\mathrm{add}} = e\Delta V_{\mathrm{ds}}$. The diagonal length of the diamond at $V_{\mathrm{ds}} = 0\,\mathrm{V}$, ΔV_{g}, also coincides the addition energy. Therefore, $\alpha = e\Delta V_{\mathrm{ds}}/\Delta V_{\mathrm{g}}$. We note that ΔV_{g} directly relates with the gate capacitance C_{g} due to the single electron behavior; $C_{\mathrm{g}} \sim e/\Delta V_{\mathrm{g}}$

We now turn back to Eq. 2.8, and then differential conductance G can be derived from it:

$$G = \frac{dI}{dV} = \frac{2e^2}{\hbar}\left(\frac{1}{\gamma_{\mathrm{L}}} + \frac{1}{\gamma_{\mathrm{R}}}\right)^{-1} \frac{1}{4k_{\mathrm{B}}T\cosh^2((\varepsilon - eV)/2k_{\mathrm{B}}T)}, \tag{2.9}$$

where we have utilized $\partial f/\partial\mu = -1/\{4k_{\mathrm{B}}T\cosh^2((\varepsilon-\mu)/2k_{\mathrm{B}}T)\}$. We have also set $\mu_{\mathrm{L}} = 0$ without losing the generality, and then, bias voltage $V = \mu_{\mathrm{R}}/e$. Figure 2.3 shows a plot of Eq. 2.9 as a function of ε, where a peak appears as well as QD current. Actually, Eq. 2.9 can also be obtained from quantum mechanics as a limit of $k_{\mathrm{B}}T \gg \Gamma = \Gamma_{\mathrm{R}} + \Gamma_{\mathrm{L}}$. Note that the width of the peak in energy is determined by thermal energy, and thereby, the temperature of the charges can be acquired. Practically, zero bias conductance is used for that, because other levels can contribute to the conductance when a bias voltage is applied. In this limitation, as seen in Eq. 2.9,

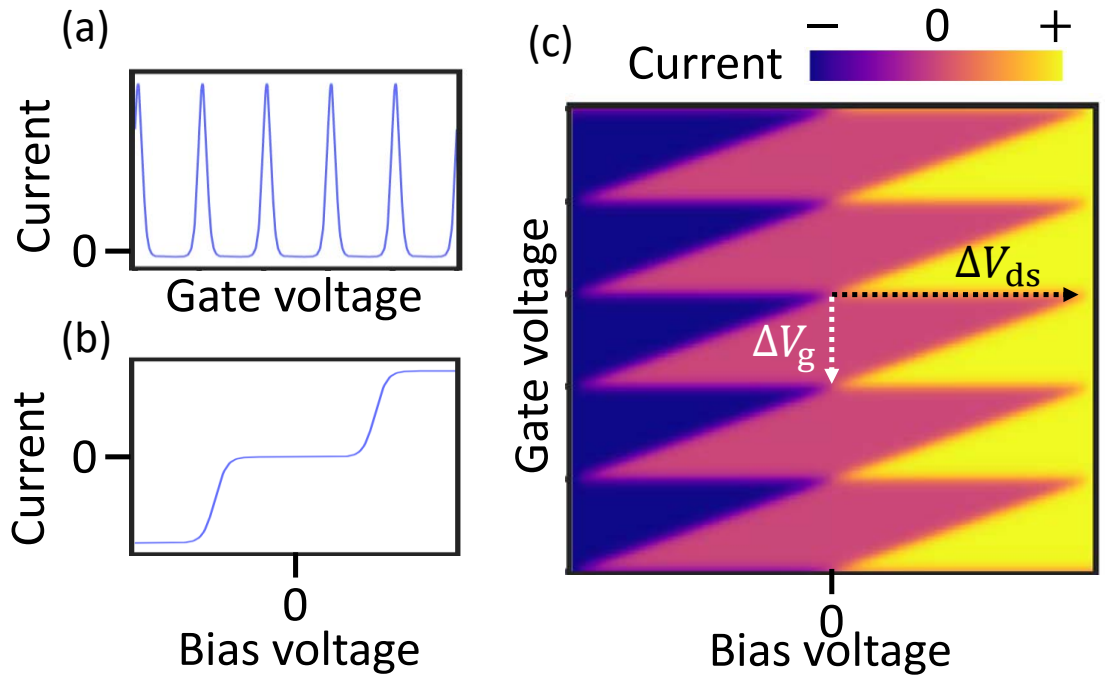


Figure 2.2: (a) Simulated current through a SQD as a function of gate voltage. Here, multiple charge states are taken into account. (b) Simulated current through a SQD as a function of bias voltage. Current is suppressed around zero bias voltage. (c) Simulated current through a SQD as a function of gate voltage and bias voltage. Current is suppressed in characteristic diamond-shaped areas. Here, ΔV_g is the diagonal length of the diamond at $V_{ds} = 0\,\mathrm{V}$ in V_g. ΔV_{ds} indicates the height of the diamond from zero bias voltage.

QD resistance $1/G$ can be regarded as two series resistors, meaning that each tunnel barrier has a resistance (sequential tunneling). Meanwhile, in the opposite limitation that $k_B T \ll \Gamma$,

$$G = \frac{2e^2}{h} \frac{4\Gamma_L \Gamma_R}{(\varepsilon - \mu)^2 + \Gamma^2}, \tag{2.10}$$

where V is set to be zero. In this case, the width of the Lorentzian peak is determined by Γ (resonant tunneling).

In reality, finite conductance can exist even in Coulomb blockade conditions, which can be caused by co-tunneling (Fig. 2.4).[55] This tunneling is named after the fact that high-order tunneling events with multiple charges contribute to the tunneling. For the explanation, we shall consider two-electron processes, the sim-

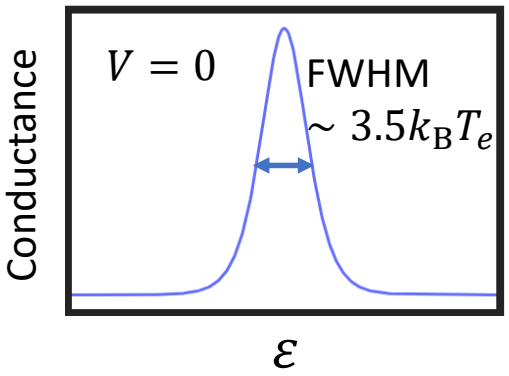


Figure 2.3: A simulated conductance peak of a SQD at $V = 0\,\mathrm{V}$. Its full width at half maximum (FWHM) corresponds to the electron temperature.

plest case, which is the leading-order term and describe the co-tunneling in a QD with two tunnel-coupled reservoirs (Fig. 2.4). Here, we assume three energies of states for zero to two charges: $E_0 = 0$, $E_1 = \varepsilon_0$, and $E_2 = 2\varepsilon_0 + U$, where ε is the energy of the (first) orbital and U is the charging energy. Therefore, two energies for adding and removing an electron are calculated: $E_+ = (E_2 - E_1) - \mu = \varepsilon_0 + U - \mu$ and $E_- = \mu - (E_1 - E_0) = \mu - \varepsilon_0$, where μ is the Fermi energy of the reservoirs. If an charge tunnels out of the QD, the system energy increases by E_- (Fig. 2.4(a)). In classical physics, this transition is completely restricted; however, quantum physics allow it for a short time, $\Delta t \sim \hbar/E_-$ based on uncertainty principle. During Δt, another charge tunnels into QD, and thereby, the violation of the law of conservation of energy is compensated. This happens also for E_+ in analogy (Fig. 2.4(b)).

2.3 Multi-quantum dot structure

2.3.1 Double quantum dot

Next, we explain DQD characteristics (Fig. 2.5(a)). One can also obtain the electrochemical potential for DQDs in analogy with single QD:

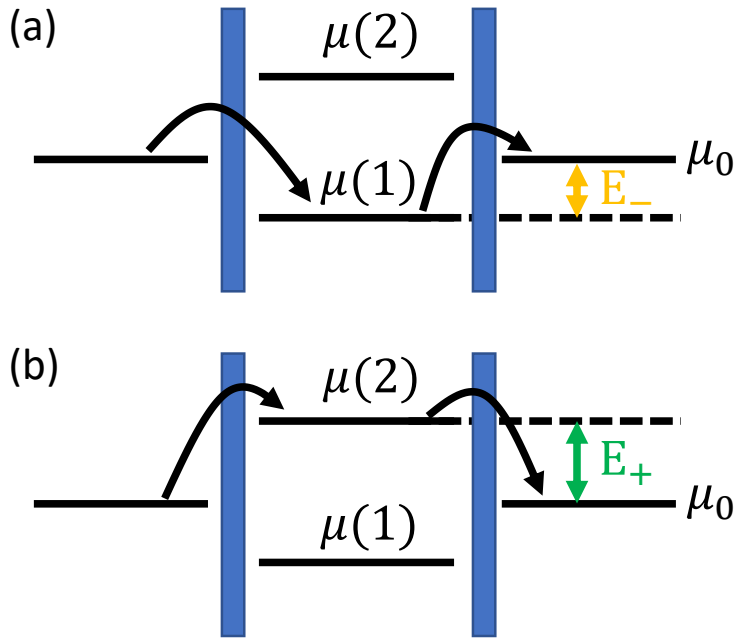


Figure 2.4: Co-tunneling through a QD. Here, tunneling events occur disregarding energy conservation, which is allowed by the uncertainty principle. (a) Co-tunneling via lower energy level. (b) Co-tunneling via higher energy level.

$$\begin{aligned}\mu_1(N_1,N_2) =& U(N_1,N_2) - U(N_1-1,N_2)\\ =& (N_1-\frac{1}{2})E_{\mathrm{C1}} + N_2 E_{\mathrm{Cm}}\\ & - \frac{E_{\mathrm{C1}}}{|e|}\sum_j C_{1\mathrm{j}}V_j + \frac{E_{\mathrm{Cm}}}{|e|}\sum_j C_{2\mathrm{j}}V_j,\end{aligned} \tag{2.11}$$

where $E_{\mathrm{C}i} = e^2/\{C_i(1-C_{\mathrm{m}}^2/C_1C_2)\}$ is the charging energy of QDi, $E_{\mathrm{Cm}} = e^2/\{C_{\mathrm{m}}(C_1C_2/C_{\mathrm{m}}^2-1)\}$ is the coupling energy, j is an index for electrodes ($j = g1, g2, s, d$), and single-particle levels are here ignored. $\mu_2(N_1,N_2)$ can be obtained in analogy with $\mu_1(N_1,N_2)$. One can map out the DQD stability diagram by sweeping voltages of two gates, g1 and g2 (Fig. 2.5(b)). As seen in Fig. 2.5(b), each Coulomb blockade area is bordered by three different slopes, forming a honeycomb structure. μ_1 (μ_2) corresponds to a line with the most nearly vertical (horizontal) negative slope, reflecting the different gate-QD couplings. Interdot charge transitions occur across the lines with the positive slope. Focusing on a single honeycomb

structure, two lines with the same negative slope corresponds to electrochemical potentials with the charge numbers different by one. One can therefore obtain gate capacitances between gate k and QD i, $C_{gk}^{\mathrm{QD}i}$ in an approximation; $C_{gk}^{\mathrm{QD}i} \sim e/\Delta V_{gk}^{\mathrm{QD}i}$ (Fig. 2.5(b)).

Current through DQD is suppressed except for the conditions that energy levels for each QD are in bias window and ordered not to prevent current flowing (Fig. 2.5(c)). Without bias voltage, current can flow at points where energy levels of both QDs are aligned with the Fermi levels of the reservoirs. Figures. 2.5(d) and (e) shows two examples of current-flow points for four energy levels, $\mu_1(1,0)$, $\mu_1(1,0)$, $\mu_2(0,1)$, and $\mu_2(1,1)$ (Fig. 2.5(c)). At the black dot in Fig. 2.5(c), single electrons can tunnel through the DQD via a cycle of charge configurations: (0,0) $\rightarrow$ (1,0) $\rightarrow$ (0,1) $\rightarrow$ (0,0) (Fig. 2.5(d)). On the other hand, at the white dot in Fig. 2.5(c), another cycle transports charges: (1,1) $\rightarrow$ (1,0) $\rightarrow$ (0,1) $\rightarrow$ (1,1) (Fig. 2.5(e)). Each cycle has three charge configurations, so that the points are called (charge) triple points. It is known that a finite bias voltage expands the points into triangles, so-called bias triangles (Fig. 2.5(c)). The size of the triangle is proportional to the applied bias voltage, and thereby, one can acquire the conversion factor between gate k and QD i from measurements with two different bias voltages in an approximation; $\alpha_{gk}^{\mathrm{QD}i} \sim e\delta V_{\mathrm{ds}}/\delta V_{gk}^{\mathrm{QD}i}$, where δV_{ds} is different in bias voltages and $\delta V_{gk}^{\mathrm{QD}i}$ is shift of a charge transition line in V_{gk}.

2.3.2 Triple quantum dot

It is also possible to calculate energy levels for TQDs in analogy with DQD (Fig. 2.6(a)). Here, we skip the formulation because of its complexity, but instead, mention the general features. As predicted from DQD characteristics, TQD shows three different negative slopes each corresponding to charge transitions in a QD of TQD as a function of two gate voltages (Fig. 2.6(b)). This behavior can be understood by three-dimensional charge stability diagram in a space spanned by

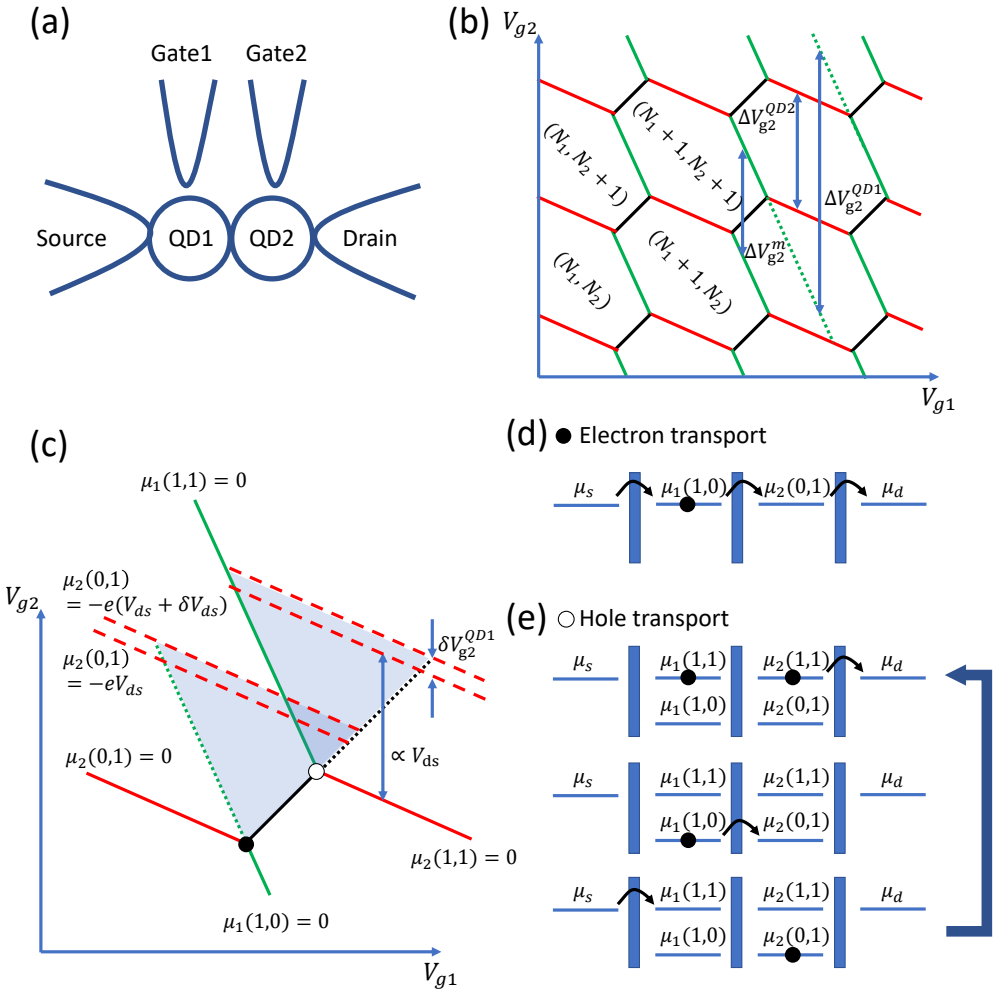


Figure 2.5: (a) Schematic of DQD. Each of gate1, gate2, drain, and source is capacitively coupled to QD1 and QD2, respectively. (b) Schematic of charge stability diagram for DQD as a function of two gate voltages. Two negative slopes appear corresponding to charge transitions in each QD. Coulomb blockade areas are bordered like honeycomb structures by charge transition lines. The distance between adjacent charge transition lines can be used to calculate characteristic energies. $\Delta V_{g2}^{\mathrm{m}}$ corresponds to shift in energy of QD1 by a charge transition in QD2. $\Delta V_{g2}^{\mathrm{QD1}}$ ($\Delta V_{g2}^{\mathrm{QD2}}$) corresponds to the distance between QD1 (QD2) charge transitions with one charge difference without charge transition in QD2 (QD1). (c) Schematic of current through DQD as a function of two gate voltages. The figure focuses on a charge degeneracy point in (b). Solid lines corresponds to the charge transition lines in (b). Without bias voltage, current flows at black and white points, while, with a finite bias voltage, current-flowing area forms triangles, called triple point. Because the size of the triangles proportional to bias voltage, one can know the conversion factors from the triple points with different bias voltages. (d,e) Charge transport at black and white points in (c), respectively. At the black point, electrons pass through the tunnel barriers one by one ((d)); on the other hand, at white point, holes transport ((e)).

three gate voltages, which is composed by three types of charge transition planes corresponding to the charge transitions in TQD (Fig. 2.6(c)). Current through TQD is restricted as well as DQD. For TQD, the current-flow point is referred to as quadruple point where four charge states contributes to the current: e.g., (0,0,0) → (1,0,0) → (0,1,0) → (0,0,1) → (0,0,0). When all the three QDs have tunnel-coupled reservoirs, the restriction is mitigated, and then, current through triple points flows. [56]

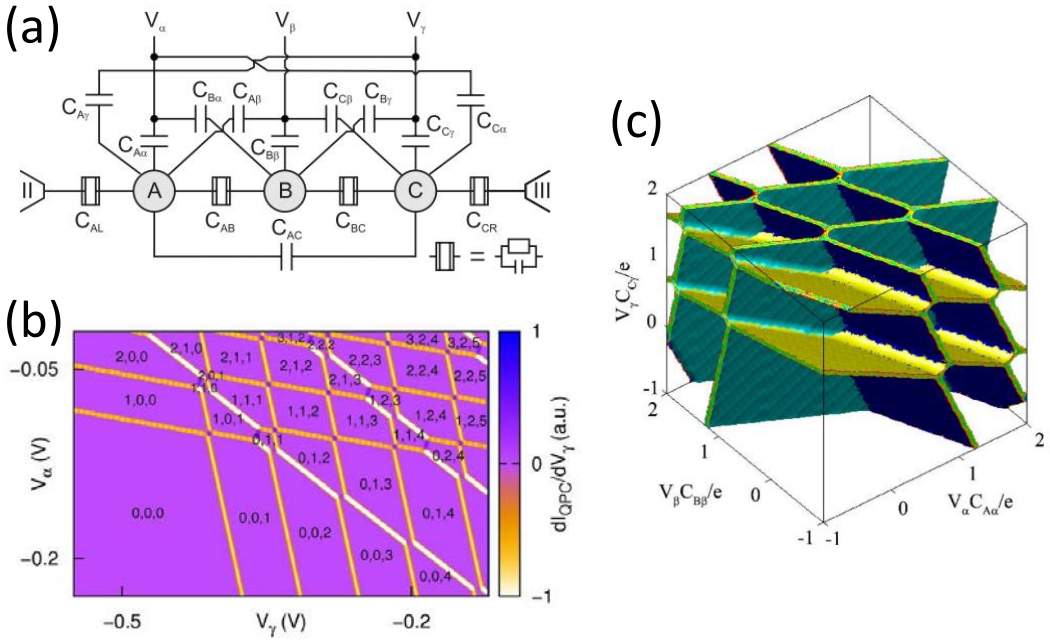


Figure 2.6: (a)Equivalent circuit diagram for linear TQD. (b) Numerically calculated stability diagram of the TQD device in (a). (c) Simulated three-dimensional charging diagram of a TQD. The figures are adapted from Ref. 57.

2.4 Charge sensing

As shown in the previous section, the conductance of a QD has sharp peaks as a function of electrical potential, meaning that it is sensitive to electrical environment. This is useful to detect charge transitions in other QDs. In measurement, a charge transition shifts the conductance of charge sensor (CS) via the capacitive coupling, resulting in a kink (Fig. 2.7(a)). In other words, the positions of kinks indicate the

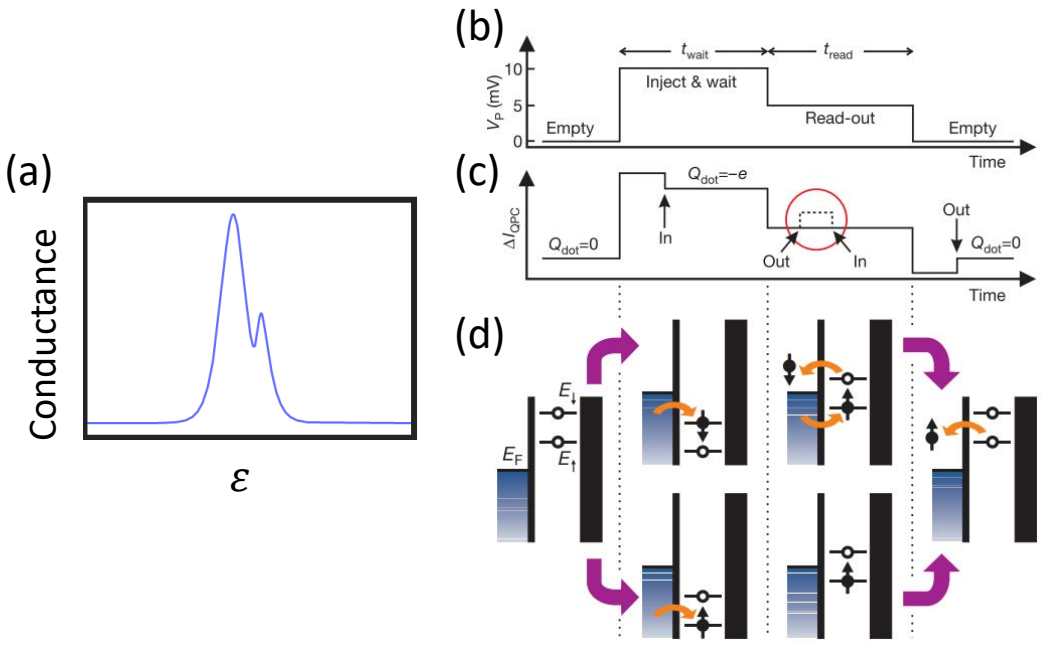


Figure 2.7: (a) Schematic of charge sensing. Compared with Fig. 2.3, a charge sensing kink appears,corresponding to a charge transition in a target QD. (b-d) A scheme for spin readout. See main text for detail. Figures (b-d) are adapted from Ref. 18.

positions of charge transitions in target QDs. When one takes a map as a function of two gate voltages, kinks appear as lines in the map. This is one way to confirm whether a kink relates to a charge transition or noise.

By using charge sensing, spin qubit states can be acquired via spin-to-charge conversion techniques.[19, 18] The techniques enables spin-dependent tunneling events where QD charge configurations changes depending on spin states. We shall briefly explain a single-shot spin readout sequence for a system consisting of a SQD with tunnel-coupled reservoir and a CS (Figs. 2.7(b), (c), and (d)). Here, "single-shot" means measurement of a single event (for example, a single tunneling of a single electron) unlike measurements of QD current which is an ensemble of many tunneling events. The single-shot measurement is required to acquire spin states because the spin state can be stochastically obtained due to quantum superposition of the parallel spin states. One of the easiest ways to demonstrate the spin readout is re-

peatedly applying a three-step sequence: initialization, (random spin) preparation, and spin readout. This can be performed by applying corresponding three-step pulses by, e.g., arbitrary waveform generator. Fig. 2.7(b), applied gate voltage pulse is displayed. There are three levels which are to empty a QD, to load an electron into QD, and to read out the spin state, respectively. In this case, the spin in each sequence is randomly loaded. Fig. 2.7 (c) shows a schematic for the CS response to the pulse. As highlighted by red circle, a pulse-like signal appears in the read-out level depending on the spin state. As explained in Fig. 2.7 (d), if the spin state is in higher energy level, spin can tunnel out of the QD, and then, another one tunnels into the QD, while it does not happen if the spin state is in lower energy level. This measurement should be performed within a spin relaxation time ($\sim$ 100 ms); otherwise, spin information will be lost.

2.5 RF reflectometry

2.5.1 LCR circuit

RF reflectometry is commonly used for fast charge sensing. In the circuit, device electrode (reservoirs of CS or gates) is connected to transmission line (coaxial line from low temperature stage to outside of fridge) through impedance conversion circuit, and the RF reflection is measured. The impedance of a QD ($\sim 1\,\mathrm{M}\Omega$) is much higher than the characteristic impedance of a coaxial line $Z_0 = 50\,\Omega$, so that the impedance is converted by LC tank circuit. An equivalent circuit for the RF reflectometry is an LCR circuit as shown in Fig. 2.8. Hereafter, we formulate the RF reflectometry from electrical circuit and transmission theories. The impedance of the load circuit Z_{load} is

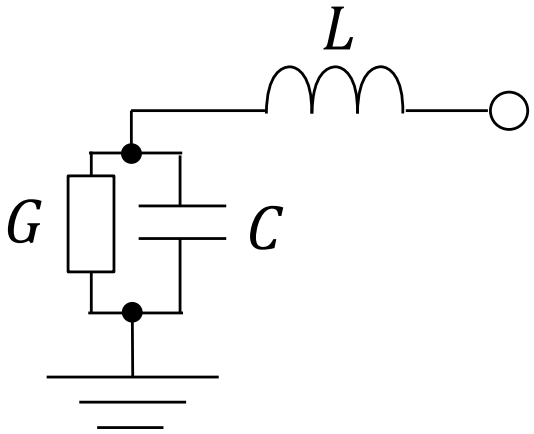


Figure 2.8: LCR circuit for RF reflectometry. G and C include QD impedance and parasitic components like dielectric loss of printed circuit board.

$$\begin{aligned} Z_{\text{load}} &= j\omega L + \frac{1}{j\omega C + G} \\ &= \frac{1 - \omega^2 LC + j\omega LG}{G + j\omega C}, \end{aligned} \tag{2.12}$$

where L, C, and G are inductance, capacitance, and conductance of the LCR circuit, respectively, and ω is angular frequency of carrier wave. In reality, G comprises device conductance and dielectric loss, and C include parasitic capacitance in addition to device capacitance. L actually has parasitic components; however, they are ignored here for simplicity.

LC circuit at resonance has no reactance (which means that power consumption of the impedance is at maximum); therefore, the resonance angular frequency ω_0 of Eq. 2.12 is

$$\omega_0 = \sqrt{\frac{1}{LC} \times \frac{C - LG^2}{C}} \simeq \frac{1}{\sqrt{LC}}, \tag{2.13}$$

where $C \gg LG^2$ is assumed because (parasitic) capacitance, (quantum dot) conductance, and (chip) inductance are typically in the order of 1 pF, 1 μS, and 100 nF, respectively. Then, Z_{load} at resonance is turned out

$$Z_{\mathrm{res}} = \frac{jLG/\sqrt{LC}}{G + jC/\sqrt{LC}} \simeq \frac{LG}{C}, \tag{2.14}$$

where $C \gg LG^2$ is assumed again.

The reflection coefficient of the load impedance Γ is defined as

$$\Gamma = \frac{Z_{\mathrm{load}} - Z_0}{Z_{\mathrm{load}} + Z_0}, \tag{2.15}$$

where Z_0 is the characteristic impedance of transmission line, normally equal to 50 Ω. When $Z_{\mathrm{load}} = Z_0$, no reflection occurs, which is feasible by tuning circuit parameters. When G belongs to a charge sensor, Γ senses charge transition in target QDs via charge sensor conductance. This technique is called RF-SET. The Γ shift at resonance, $\Delta\Gamma_{\mathrm{res}}$, can be derived as follows. Assuming that a charge transition in target QD shifts Z_{res} by a small value ΔZ_{res}, reflection coefficient at resonance in this condition, Γ'_{res}, is

$$\begin{aligned} \Gamma'_{\mathrm{res}} &= \frac{Z_{\mathrm{res}} + \Delta Z_{\mathrm{res}} - Z_0}{Z_{\mathrm{res}} + \Delta Z_{\mathrm{res}} + Z_0} \\ &\sim \Gamma_{\mathrm{res}} + \frac{2\Delta Z_{\mathrm{res}} Z_0}{(Z_{\mathrm{res}} + Z_0)^2}, \end{aligned} \tag{2.16}$$

where $Z_{\mathrm{res}} + Z_0 \gg \Delta Z_{\mathrm{res}}$ and $\Gamma_{\mathrm{res}} = (Z_{\mathrm{res}} - Z_0)/(Z_{\mathrm{res}} + Z_0)$, and then, normalized shift in Γ_{res} is

$$\frac{\Delta\Gamma_{\mathrm{res}}}{\Gamma_{\mathrm{res}}} = \frac{\Gamma'_{\mathrm{res}} - \Gamma_{\mathrm{res}}}{\Gamma_{\mathrm{res}}} = \frac{2\Delta Z_{\mathrm{res}} Z_0}{(Z_{\mathrm{res}}^2 - Z_0^2)}. \tag{2.17}$$

Eq. 2.17 indicates that a good impedance matching $Z_{\mathrm{res}} \sim Z_0$ significantly contributes a large reflection change.

The RF-SET allows multiplexing of signals, meaning simultaneous readouts of multiple qubits. So far, frequency-domain and time-domain multiplexing techniques have been investigated.[58, 28] These techniques will be essential for fault-tolerant quantum computing where millions of qubits are corrected in parallel.

2.5.2 Capacitance for RF-SET

In the community, the capacitance for the LC tank circuit is referred to as parasitic capacitance because parasitic capacitance is always used to make the RF reflectometry sensitive to impedance change in the QD as described in Eq. 2.14. However, the capacitance is essential for the best performance of practical RF reflectometry as seen below. Figure 2.9(a) shows a simulation result of $|\Delta\Gamma|$, the difference between two conductance conditions which correspond to a Coulomb blockade and a Coulomb peak, respectively. The equivalent circuit used in the simulation has the conductance (capacitance) the same as in Fig. 2.8, however consisting of QD one, G_{QD} (C_{QD}) and an offset value, G_0 (C_0). Assuming G_0 comes from the dielectric loss of printed circuit board, $G_0 = \omega C_0 \tan\delta$, where ω is the carrier angular frequency and $\tan\delta$ is the loss-tangent. As seen in the Fig. 2.9(a), $|\Delta\Gamma|$ as a function of C_0 shows a maximum at a small $C_0 \sim 4\,\mathrm{fF}$, indicating the necessity of capacitance of the circuit. Typically, C_0 is in the order of 100 fF due to parasitic capacitances of printed circuit board (PCB) and two-dimensional electron gas. The $\tan\delta$ of 0.001, used for the simulation, is close to the value of one of PCB materials with the lowest dielectric constants, and C_0 for maximum $|\Delta\Gamma|$ does not change so much even when $\tan\delta$ increases from the simulation value (Fig. 2.9(b)). Therefore, a finite C_0 is always needed for an optimal RF-SET condition.

2.5.3 RF components

Here, we briefly describe electric RF components for RF reflectometry. Practically, in order to measure the reflected signal, it is necessary to derive the reflected signal from incident signal. Typically, directional couplers are used for this purpose. Directional couplers are passive devices with four ports, and the four ports have two types: transmission, and coupled ports. Two of the four ports are the transmission ports. On the other hand, the other two ports are coupled ports which weakly

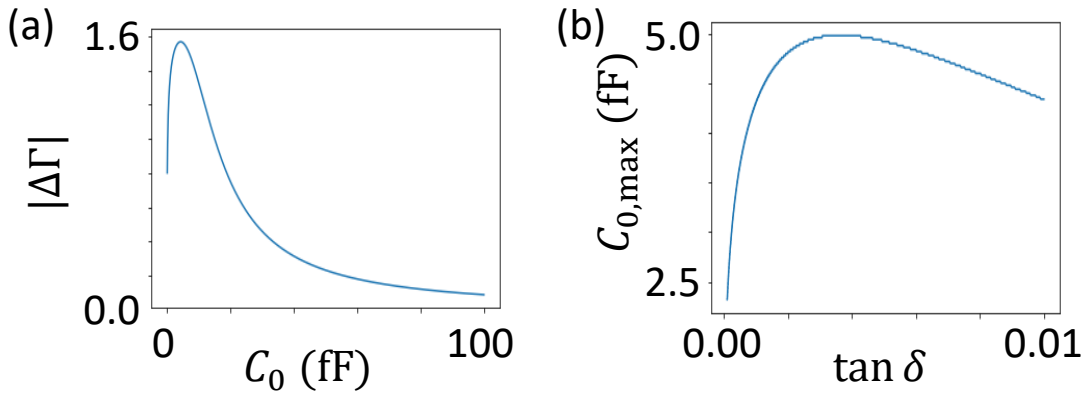


Figure 2.9: (a) Difference in Γ between Coulomb peak and blockade, $|\Delta\Gamma|$ as a function of the capacitance of an RF-SET circuit. It shows a maximum at a finite capacitance value. (b) The capacitance for the maximum value of $|\Delta\Gamma|$ as a function of $\tan\delta$.

couples to each transmission port.

In the RF reflectometry, to extract reflected signal, incident wave is applied to a coupled port (CPL) which couples a transmission port (IN). This IN port is connected to a device under test (DUT), and hence, the signal is reflected. The reflected signal (mainly) passes from the IN port to the other transmission port (OUT) instead of the CPL port because the coupling between CPL-IN (20 dB, typically) is designed to be much weaker than for IN-OUT (< 1 dB). Finally, only the reflected signal is obtained by monitoring the OUT output. (The other coupled port is not needed, so that it is terminated with 50 Ω, or three-terminal directional coupler is used.) Note that CPL-OUT leakage (40 dB, typically) is inevitable and interferes with the reflected signal, resulting in undesired frequency dependence (See Ch. 6).

The weak CPL-IN coupling strongly attenuates the incident signal, which actually matches a requirement for suppression of heat transfer. Weak power input is essential (~ -100 dBm) at DUT located at a cryogenic temperature. In addition, attenuators are located at different cold stages and also works as thermal anchors which cool down transporting electrons step by step. This is needed to lower the electron temperature and to observe clear quantum effects. Directional coupler also

plays a role such that reflected signal avoids the strong attenuations.

In measurements, RF amplifiers are needed because of the low RF power of the reflected signals. In addition to the low power applied to DUT ($< -100\,\mathrm{dBm}$), reflection coefficient at DUT has another attenuation because of the impedance matching, further lowering the signal power. RF amplifiers can recover the power even though it deteriorates the signal-to-noise ratio (SNR) compared with the one at DUT, which is inherent in amplifier. One way to suppress this effect is use of cryogenic amplifiers. The amplifier has been developed for cryogenic use, which is important to reduce thermal noise. The thermal noise in voltage V_n is expressed by $\sqrt{4k_\mathrm{B}TBR}$, where k_B is the Boltzmann constant, T a temperature, B a bandwidth, and R a resistance which is the source of the noise. Comparing V_n at inputs of room temperature amplifier and cryogenic amplifier, the ratio is estimated to ~ 5 by taking into account the voltage division between the device impedance and the input impedance of the amplifier and assuming the device impedance close to the characteristic impedance. In addition, the noise figures of the amplifiers (the figure indicating how much times larger output noise power is than that for the input) are different, resulting in 16 dB improvement of power SNR in total. This value can be interpreted into ~ 6 times improvement of voltage SNR. .

2.6 Summary

In this chapter, we explained the characteristics of QD systems and charge sensing techniques. Even though we did not describe them here because they are out of scope of this thesis, the QD systems can show an abundant physical phenomena and interactions such as Kondo effect, Aharonov-Bohm effect, spin resonance, exchange coupling, spin-orbit interaction, some of which directly relates with spin qubit operations. This is also interesting aspect of QD systems.

Regarding spin readout, readout within coherence time ($\sim 1\,\mu\mathrm{s}$) is required for fault-tolerant quantum computing, which is challenging but recently start to be

realized.[26, 59] Still, development of faster readout technique is required.

Chapter 3

Device fabrication

In this thesis, physically defined quantum dots are studied. The devices are fabricated utilizing the mature CMOS technologies. This chapter describes the fabrication process flow step by step.

3.1 SOI thinning

Thin silicon quantum well is preferable from the point of view of the quantum confinement. When the out-of-plane confinement of a quantum dot (QD) is determined by the thickness of quantum well, thinner quantum wells give rise to strong out-of-plane confinements, and thereby, qubit states can be isolated from undesired quantum states. On the other hand, thinner silicon on SOI layers will have larger channel resistances, which will prevent fast charge sensing. Multi-step SOI thinning will enable thin QD and thick electrodes but we do not adapt the technique for simplicity.[60] Then, we chose a moderate thickness $\sim 30\,\mathrm{nm}$. The wafer used here has a 100-nm thick SOI layer and a 145-nm thick buried oxide (BOX) layer before any processes.

Chip cleaning:

- Pure water cleaning with ultra sonic cleaner 1 min
- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min for removing

organic and metallic impurities

- Running water cleaning 5 min

- SC1 ($NH_4OH : H_2O_2 : H_2O = 1 : 5 : 25$) cleaning at 150 °C, 10 min for removing organic impurities and silicon particles

- Running water cleaning 5 min

- 1.5 % HF cleaning, 1 min for removing the oxide of SOI surface and metal impurities

- Running water cleaning 30 sec

- SC2 ($HCl : H_2O_2 : H_2O = 1 : 1 : 5$) cleaning at 150 °C, 10 min for removing metallic impurities

- Running water cleaning 5 min

Thermal oxidation:

At 1000°C, 100 min; by this process, SOI layer thickness decreases from 100 nm to $\sim$ 30 nm.

Oxide removal:

- Pure water cleaning with ultra sonic cleaner 1 min

- Buffered HF (BHF) cleaning 3 min; the etching rate for SiO_2 is $\sim$ 70 nm/min.

- Pure water cleaning with ultra sonic cleaner 1 min

3.2 Quantum dot patterning

Electron beam lithography (EBL) and reactive ion etching (RIE) are used to form the QDs as well as side gates and charge sensors in the SOI substrate. The pattern around the quantum dots is a nano-size structure, but patterning in micro-size areas is also required to make disconnections between electrodes and between devices. Therefore, we separately applied electron beams with the small-current exposure for the nanostructure and with the large-current exposure for the pad

for the micro-size electrode. The electron beam exposures are continuously carried out without removing the sample from the chamber and without alignment for the exposures. Possible position shifts between the two exposure are compensated by taking alignment margins in the patterns.

Chip cleaning:

- Pure water cleaning with ultra sonic cleaner 1 min
- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min
- Pure water cleaning with ultra sonic cleaner 1 min
- HF cleaning, 1 min for removing the native oxide of SOI surface
- Pure water cleaning with ultra sonic cleaner, 1 min

EBL resist coating:

- Baking in oven at 180 °C, 10 min
- Spin coating of an EBL resist (ZEP520A : ZEP-A = 1 : 1 containing fullerene), 1^{st} step 1000 rpm, 5 sec, 2^{nd} step 3000 rpm, 60 sec

-Prebake on a hot plate at 180 °C, 10 min

EBL:

- 1^{st} exposure: 50 kV, 60 pA for fine patterns
- 2^{nd} exposure: 50 kV, 7500 pA for device isolation patterns

Developpment:

ZED-N50 30 sec, IPA 30 sec

SEM:

To confirm whether EBL fine patters are formed as expected or not by observing dummy patterns. Carbon tapes are used to fix the chips.

RIE:

$Cl_2 = 50$ sccm, 50 W, $\sim$ 40 sec; The etching rate is $\sim$ 80 nm/min. The etching time is chosen so that etching depth is roughly twice of SOI thickness.

EBL resist removal:

-ZD-MAC 10 min

-IPA cleaning 3 min

- Pure water cleaning with ultra sonic cleaner 1 min

- Acetone 3 min

- Pure water cleaning with ultra sonic cleaner 1 min

- SPM ($H_2SO_4 : H_2O_2 = 3 : 1$) cleaning at 120 °C, 10 min

- Pure water cleaning with ultra sonic cleaner 1 min

SEM:

To confirm whether physical fine patters are formed as expected or not by observing dummy patterns. Carbon tapes are used to fix the chips.

Chip cleaning:

- Pure water cleaning with ultra sonic cleaner 1 min

- SPM ($H_2SO_4 : H_2O_2 = 3 : 1$) cleaning at 120 °C, 10 min

- Pure water cleaning with ultra sonic cleaner 1 min

- HF cleaning, 1 min for removing the native oxide of SOI surface

- Pure water cleaning with ultra sonic cleaner 1 min

3.3 Top gate deposition

Before forming top gate structure used for charge accumulation, SOI layer is thermally oxidized for a better interface quality. Although poly-silicon is deposited for the top gate, the poly-silicon layer can screen electric fields from side gates when it gets into the gap between side gates and QD. Therefore, SiO_2 is deposited by Low Pressure Chemical Vapor Deposition (LP-CVD). (This LP-CVD was done by Hiramoto group in Tokyo Univ.) Then, poly-silicon doped with a high concentration of phosphorus is separately deposited by LP-CVD. After the depositions, photolithography and plasma etching are performed to form the top gate.

Chip cleaning:

- Pure water cleaning with ultra sonic cleaner 1 min

- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min

- Running water cleaning 5 min

- 1.5 % HF cleaning, 1 min

- Running water cleaning 30 sec

- SC2 ($HCl : H_2O_2 : H_2O = 1 : 1 : 5$) cleaning at 150 °C, 10 min

- Running water cleaning 5 min

Surface passivation:

At 1000°C, 5 min; By this process, The surface of SOI layer is passivated by covering 10-nm thick SiO_2.

Gate oxide deposition:

SiO_2 deposition by LP-CVD at 840 °C, $SiH_2SO_4 + N_2O$; $\sim$ 50-nm thick SiO_2 is deposited.

Chip cleaning:

- Pure water cleaning with ultra sonic cleaner 1 min

- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min

- Pure water cleaning with ultra sonic cleaner 1 min

- 1.5 % HF cleaning, 3 min for removing the oxide of SOI surface and metal impurities

- Pure water cleaning with ultra sonic cleaner 1 min

Poly-silicon deposition:

Highly P^+-doped poly-Si deposition by LP-CVD, Si_2H_6 0.3 sccm, PH_3 7 sccm, 500 °C, 40 min; $\sim$ 200-nm thick poly-silicon is deposited.

Photolithography for top gate pattening:

- Baking in oven at 120 °C, 10 min

- Spin coating of hexamethyldisilazane (HDMS) which works as an adhesion promoter for photoresist, 1^{st} step 1000 rpm, 3 sec, 2^{nd} step 2000 rpm,

30 sec

- Spin coating of photoresist (S1818), 1st step 1000 rpm, 5 sec, 2nd step 3000 rpm, 60 sec

- Prebake on a hot plate at 110 °C, 1 min - Photolithography 100 mJ

- Development MF320 90 sec, pure water 30 sec

Plasma etching:

CF_4 100 sccm (max), O_2 11 sccm, 250 W, 50 sec

Photoresist removal:

- O_2 ashing, O_2 30 sccm, 50 W, 60 sec

- Pure water cleaning with ultra sonic cleaner 1 min

- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min

- Pure water cleaning with ultra sonic cleaner 1 min

3.4 Ion implantation

In order to make ohmic contact at cryogenic temperature, the SOI substrate needs to be doped with a high concentration of impurities. Therefore, impurity doping is carried out by ion implantation. Ion implantation is a low-temperature process in which dopants are injected into the substrate with high energies. The ion concentration can be made to have a peak at a desired depth by adjusting the acceleration energy. In our case, phosphorus is used as the dopant for electron transport. The SiO_2 formed as the gate insulator can moderate the irradiation damage in SOI layer, but it may still remain. In addition, if the implanted impurities are not at the lattice positions, the impurities do not work as dopants. Thermal annealing, here referred to as drive-in annealing, restores the crystalline state of the SOI layer and introduces the injected impurities into the lattice positions, making it electrically active. If impurities are doped into the QD, their nuclear spins will disturb spins in QD. Therefore, the top gate is used as a mask for the channel,

resulting in self-aligned source and drain formation. For device without top gate structure, resist mask is used to protect QD during ion implantation instead. The drive-in also plays a role in the recrystallization of poly-silicon.

(Photolithography for resist mask:)

- Baking in oven at 120 °C, 10 min
- Spin coating of HDMS, 1st step 1000 rpm, 3 sec, 2nd step 2000 rpm, 30 sec
- Spin coating of S1818, 1st step 1000 rpm, 5 sec, 2nd step 3000 rpm, 60 sec
- Prebake on a hot plate at 110 °C, 1 min
- Photolithography 100 mJ
- Development MF320 90 sec, pure water 30 sec

Ion implantation:

Phosphorus (P^+) doping, $1 \times 10^{15}\,cm^{-2}$; The silicon substrate of a back gate device is also doped with P^+.

Chip cleaning

- Pure water cleaning with ultra sonic cleaner 1 min
- SPM ($H_2SO_4 : H_2O_2 = 1 : 1$) cleaning at 120 °C, 10 min
- Running water cleaning 5 min
- SC1 ($NH_4OH : H_2O_2 : H_2O = 1 : 5 : 25$) cleaning at 150 °C, 10 min
- Running water cleaning 5 min
- 1.5 % HF cleaning, 1 min
- Running water cleaning 30 sec
- SC2 ($HCl : H_2O_2 : H_2O = 1 : 1 : 5$) cleaning at 150 °C, 10 min
- Running water cleaning 5 min

Drive-in annealing:

At 1000 °C, 30 min

3.5 Contact pad deposition

Next, aluminum pads for wire bonding are fabricated using photolithography and vacuum evaporator, and as the last step of device fabrication, the device is annealed in forming gas atmosphere to terminate dangling bonds at the interface of the SOI layer.

Photolithography for resist mask:

- Baking in oven at 120 °C, 10 min
- Spin coating of HDMS, 1st step 1000 rpm, 3 sec, 2nd step 2000 rpm, 30 sec
- Spin coating of S1818, 1st step 1000 rpm, 5 sec, 2nd step 3000 rpm, 60 sec
- Prebake on a hot plate at 110 °C, 1 min
- Photolithography 100 mJ
- Hardening the resist surface by soaking the chip into chlorobenzene for 135 sec; The chip should immediately be dried after picking it up from chlorobenzene.
- Development MF320 90 sec, pure water 30 sec
- Postbake on a hot plate at 110 °C, 1 min

Oxide removal:

- Pure water cleaning with ultra sonic cleaner 1 min
- BHF cleaning, 90 sec
- Pure water cleaning with ultra sonic cleaner 1 min

Thermal metal deposition:

- Deposition of 300-nm thick aluminum, deposition of 100-nm thick aluminum only for devices without top gates
- Lift-off of aluminum as follows: soaking the chip into acetone overnight; ultra sonic cleaning with acetone
- Optical micrography to check if lift-off works well.

Forming gas annealing:

At 400 °C, 10 min, $NH_2 : O_2 = 95 : 5$, 100 sccm

Chapter 4

Physically defined triple quantum dot systems in silicon on insulator

In this chapter, we report characterizations of two types of Si triple quantum dot (TQD) devices with charge sensors, with the aim of integrating spin qubits. The QDs of a linear TQD device are connected in line to adjacent QD(s), while all QDs are tunnel-coupled to each other in the other device to form a triangle. Both TQD systems are physically defined on silicon-on-insulator substrates using electron beam lithography and dry etching. From electron transport measurements of each type of TQD system at 4.2 K, we demonstrate the formation of tunnel-coupled TQD systems and the tunability of their electric potentials. This work is published in *Applied Physics Letters*.[49]

4.1 Introduction

In this chapter, we demonstrate the integration of Si quantum dot (QD) structures by examining linear triple QD (LTQD) and triangular triple QD (TTQD) structures. In the TQD structures, three QDs have the tunnel couplings that are required to perform quantum operations between two spin qubits via an exchange interaction. [5] In addition, the TQD structures can be considered as exchange-only qubits, which enable fast single-qubit operations using the exchange interaction. [22, 61] Moreover, theoretical studies have revealed the existence of various physi-

cal phenomena in TTQD structures, e.g., spin/charge frustration, [62, 63] chirality qubits, [64–66] quantum cellular automata, [67, 68] and the Aharonov–Bohm effect. [69–71] These studies were motivated by the fact that a TTQD is the minimum QD configuration for many-body physics, a closed-loop system. Moreover, for well-known quantum error correction codes,[2] two-dimensional qubit arrays of millions of qubits are considered to be needed. [72–76]

In previous studies, complicated structures were used to form TTQD devices (except for the device described in Ref. 74), e.g., by combining etching and deposition of fine gates, [77] by bridge gate structures, [63] or by a special gate in another layer. [71, 76] It would be very difficult to form a deep potential barrier at the center of a TTQD in order to separate the QDs while maintaining the inter-dot couplings. Except for the lithographic patterning, our simple fabrication process to form a deep potential barrier is the same as that used for more fundamental QD systems, such as a single QD system. It is expected that such a simple fabrication process may help realize two-dimensional spin qubit systems in combination with three-dimensional gate structures.

4.2 Device structure

Scanning electron micrographs of the LTQD and TTQD are shown in Figs. 4.1(a) and (b), respectively. Both types of TQD have three QDs (QD1, QD2, and QD3: the numbered white dotted circles), and the dots of the TTQD form a triangle. A set of SG structures is used to tune the potential around each TQD structure. A CS utilizing a QD is integrated next to each TQD structure to detect changes in the number of electrons in the dots. [78]

In the measurements, currents through the QD systems were investigated as a function of gate voltages. The currents show characteristic peaks due to single-electron transport (SET). SET through a (multi-) QD system is allowed when the quantized levels in each QD are in a voltage bias window. When electrons pass

through two sequential QDs one by one, the condition is referred to as a triple point because the current path involves three charge states, namely, (N, M), $(N+1, M)$, and $(N, M+1)$, where the parentheses indicate the charge configuration of the double QD system, and N and M are integers. Analogously, for electrons passing through three sequential QDs, the point is referred to as a quadruple point. In an LTQD, a current path through all the dots is possible only at quadruple points, while a TTQD has two paths from one reservoir to another reservoir, at triple and quadruple points, as shown in Fig. 4.1(b) by the green and blue arrows, respectively.

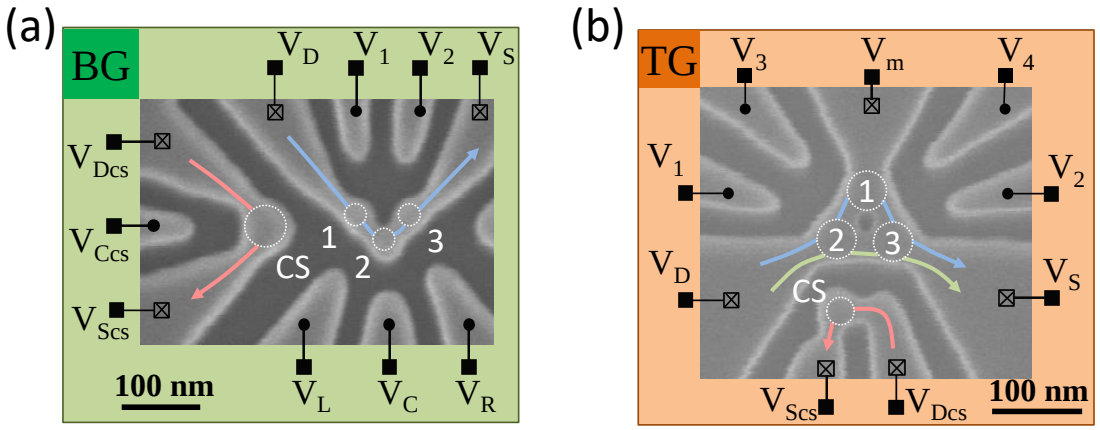


Figure 4.1: Scanning electron micrographs of (a) linear triple quantum dot (LTQD) and (b) triangular TQD (TTQD). QDs in these TQDs are indicated by white dotted circles. The QD located next to the TQD is used as a charge sensor (CS). Silicon gate electrodes to which V_x is applied are also placed near the QDs to modify the potential of the systems (x = 1, 2, 3, 4, L, C, or R). Drain and source reservoirs are connected to each TQD and each CS. V_{D} and V_{S} (V_{Dcs} and V_{Scs}) are applied to the TQD (CS) drain and source reservoirs, respectively. In the TTQD, there is an additional reservoir connected to another QD; however, the connection is electrically restricted by voltages applied to the two upper gates (V_3 and V_4). Blue and/or green (pink) arrows show the current paths through the TQD (CS). In the LTQD system (a), a back gate (BG) is used to accumulate electrons, while the TTQD system (b) has a top gate structure (TG) for electron accumulation.

4.3 Linear triple quantum dot

First, we focus on the LTQD device (Fig. 4.1(a)). Numerical derivatives of currents through the LTQD and its CS with respect to a gate voltage V_2 at 4.2 K are shown as functions of gate voltages V_1 and V_2 in Figs. 4.2(a) and 4.2(b). V_1 and V_2 primarily control the potential of the nearest QD (QD1 and QD3, respectively). Note that the cross-couplings with other QDs and tunnel barriers are not negligible; thus, the number of electrons in QD2 and the CS change with V_1 and V_2. Other gate voltages (V_L, V_C, V_R, and the back gate voltage) are fixed during the measurements presented here. No current flows through the LTQD in almost the entire area of Fig. 4.2(a), because V_1 and V_2 are below their thresholds, while charge transitions in the LTQD are detected by the CS (Fig. 4.2(b)). The transitions appear as lines with different slopes in Fig. 4.2(b), indicating differences between couplings of each QD

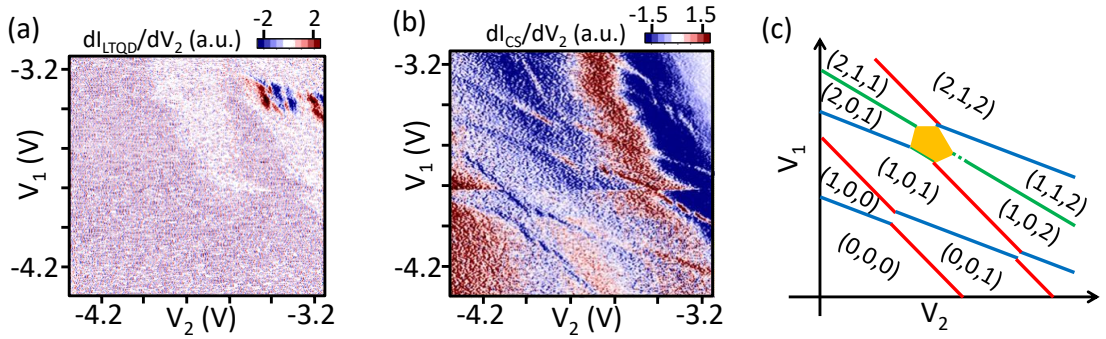


Figure 4.2: Derivatives of currents through (a) an LTQD (dI_LTQD/dV_2) and (b) a CS (dI_CS/dV_2) as functions of two gate voltages V_2 and V_1 at 4.2 K. $V_\mathrm{D} = 1\,\mathrm{mV}$, $V_\mathrm{Dcs} = 5\,\mathrm{mV}$, $V_\mathrm{L} = V_\mathrm{R} = -3.25\,\mathrm{V}$, $V_\mathrm{C} = V_\mathrm{Ccs} = V_\mathrm{S} = V_\mathrm{Scs} = 0\,\mathrm{V}$, and $V_\mathrm{BG} = 5\,\mathrm{V}$, where V_BG is the back gate voltage. For clarity, I_LTQD and I_CS are differentiated numerically with respect to V_2. In (a), the LTQD current is almost suppressed, while, in (b), charge transitions in the LTQD can be detected by the CS as lines on the red/blue background. (c) Charge transition lines manually extracted from (b). The lines have three different slopes (blue, green, and red), each corresponding to a change in the number of electrons in one QD in the TQD (QD1, QD2, and QD3, respectively). The number of electrons in the LTQD is indicated by parentheses (N_1, N_2, N_3), where N_i $(i = 1, 2, 3)$ is the relative number of electrons in QDi, counted from the $(0, 0, 0)$ region, revealing the charge transitions. The $(1, 1, 1)$ and $(1, 2, 1)$ configurations should be in the orange region, even though this is not obvious in (b) owing to the low CS sensitivity.

with the two swept SG voltages (V_1 and V_2). For example, among the three dots, QD1 (QD3) is the closest to the gate to which V_1 (V_2) is applied and should result in the most nearly horizontal (vertical) transition lines in V_1–V_2 space. QD2 is located between QD1 and QD3; thus, the transition lines are expected to have the most nearly diagonal gradient. For clarity, the transitions are extracted and classified by color according to the hypothesis explained above and the relative number of charges in the LTQD are indicated in parentheses (N_1, N_2, N_3) where N_i $(i = 1, 2, 3)$ is the electron number of QDi (Fig. 4.2(c)). The blue, green, and red lines correspond to the changes in the number of electrons in QD1, QD2, and QD3, respectively. In the orange region, QD1 and QD3 lines could exist; however, they are not visible because of the low sensitivity. Owing to the fact that only three different slopes are found, we conclude that no unintended QD is formed. The few-electron regime is not achieved, because strong cross-coupling to tunnel barriers suppresses tunneling events before the QDs become empty (not shown). Optimization of the QD design will enable the few-electron regime in a physically defined LTQD.

4.4 Triangular triple quantum dot

We also studied electron transport through the TTQD with a CS at 4.2 K. Although each dot of the TTQD has a tunnel-coupled reservoir, the one with QD1 is electrically disconnected by the application of V_3 and V_4 to simplify the system. This disconnection is confirmed by monitoring the current through the reservoir.

Figure 4.3(a) shows the current through the TTQD, I_{TTQD}, and Fig. 4.3(b) the numerical derivative of the current through CS, dI_{CS}/dV_1 at 4.2 K. These were measured at the same time as functions of V_1 and V_2. As shown in Fig. 4.3(b), there are lines with three different slopes, each corresponding to charge transitions in a dot, which is the same as in the target LTQD system. Again, three clear slopes indicate no additional dot formation (Fig. 4.3(c)).

Standard bias dependence measurements on the TTQD were also performed to

estimate the addition energies: $(E_1, E_2, E_3) = (5.3, 4.4, 4.5)$ in meV, where E_i is the addition energy of QDi in the range of the measurements. From the addition energy, the diameter of a quantum dot can be estimated approximately. By using the classical two-dimensional disk self-capacitance C, we have $E_{\mathrm{add}} \sim e^2/C = e^2/4\epsilon_{\mathrm{r}}\epsilon_0 d$ (Ref. 52), where E_{add} is the addition energy, e is the elementary charge, ϵ_{r} is the dielectric constant of a QD, ϵ_0 is the vacuum permittivity, and d is the diameter of the dot. The diameters of the QDs are estimated as $(d_{\mathrm{QD1}}, d_{\mathrm{QD2}}, d_{\mathrm{QD3}}) = (73, 89, 87)$ in nm, where $\epsilon_{\mathrm{Si}} = 11.68$. These values roughly agree with those estimated from Fig. 4.1(b) (about 60 nm), which implies that the charge transitions occur as expected in the physically defined QDs, not in unintentional dots. The discrepancy between the estimated diameters can be attributed to capacitance couplings with gates and reservoirs.

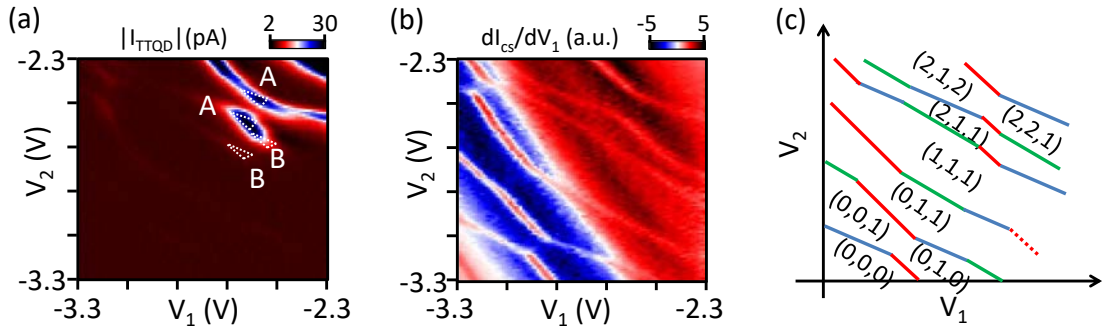


Figure 4.3: (a) Current through a TTQD (I_{TTQD}) and (b) derivative of CS current with respect to V_2 (dI_{CS}/dV_2) as functions of gate voltages V_1 and V_2 at 4.2 K. $V_{\mathrm{D}} = -0.5$ mV, $V_{\mathrm{Dcs}} = 10$ mV, $V_3 = V_4 = -3$ V, $V_{\mathrm{S}} = V_{\mathrm{Scs}} = 0$ V, and $V_{\mathrm{TG}} = 1.2$ V, where V_{TG} is the top gate voltage. Two types of triple points A and B can be found (white dotted triangle). (b) dI_{CS}/dV_2 shows charge transition lines of the TTQD. (c) Extracted charge transition lines. Parentheses indicate the relative electron numbers in the TTQD. Some lines show a discrepancy with those found in (b) because the charge sensing lines are not straight around charge degeneracy points owing to strong tunnel coupling between QDs.

4.5 Quadruple point

To prove the existence of couplings between each two quantum dots, we focus on two types of charge triple points (TPs), namely, a pair of apparent TPs ("A" in Figs. 4.3(a) and 4.4) and a pair of TPs with a vague peak ("B"). The weak current at point B can be considered as a TP where current flows through three quantum dots, with one QD being skipped via co-tunneling processes owing to the strong tunnel couplings of QD3 with the dots and the reservoir (Fig. 4.4(b)).[79–81] The strong couplings can be acquired from a non-resonance current on the charge transition lines of a QD (the white dashed line in Fig. 4.4).

We repeated the same measurements at different $V_3 = V_4$ (Figs. 4.4(d) and 4.4(e)) and observed the change in TPs. As $V_3 = V_4$ increases negatively, TP B becomes closer to TP A, which indicates that TPs A and B are current peaks through different sets of two serial QDs (Fig. 4.4(d)). Thus, we conclude that all the QDs are tunnel-coupled, because TP A indicates one of three inter-dot couplings (QD2–QD3) and TP B indicates the others (QD1–QD2 and QD1–QD3).

At further increased $V_3 = V_4$, TP A merges with TP B, resulting in a quadruple point (QP) (Fig. 4.4(e)). At a QP, all the energy levels of the three dots align with each other.[82, 83] The observation of this QP demonstrates the tunability of the proposed system.

4.6 Summary

To perform fault-tolerant quantum computing, two-dimensional integration of millions of qubits will be important. In this chapter, two types of physically defined TQD systems, each with a charge sensor, have been studied. One of these has a linear TQD while the other has a triangular TQD. Both were fabricated on a silicon-on-insulator wafer using standard fabrication techniques for Si MOSFETs. The TQD configuration was achieved easily, by simply modifying the lithographic

pattern for a simpler QD system using electron beam lithography and dry etching techniques. The current through these systems was measured at 4.2 K as a function of SG voltages and clearly showed the realization of a TQD without unintentional QDs in each system. This work demonstrates the realization of a promising QD-

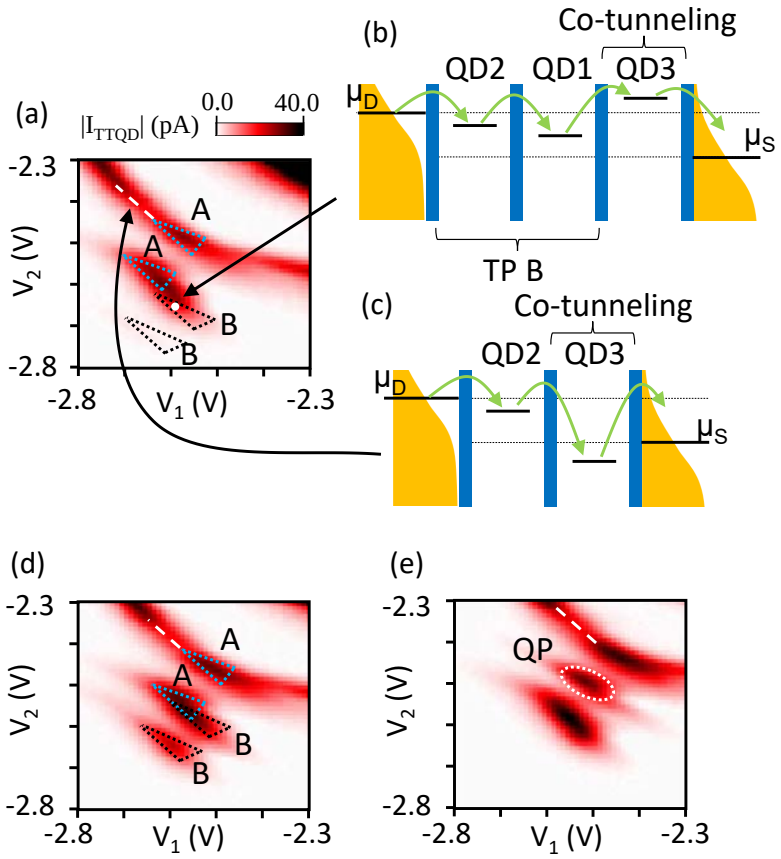


Figure 4.4: (a) Current through a TTQD shows TPs close to a QP as a function of V_1 and V_2 at $V_3 = V_4 = -3.00\,\mathrm{V}$. The voltages applied to the other gates are the same as those shown in Fig. 4.3. TPs between QD2 and QD3 are observed ("A"; blue dotted triangle). One of the TPs between QD1 and QD2 ("B"; black dotted triangle) is unclear because high-order tunneling is dominant. (b, c) Schematic energy diagrams of the TTQD: (b) at TP B (white dot in (a)) and (c) along the line corresponding to a charge transition in QD2 (white dashed line in (a)) where non-resonant current flows. The Fermi levels of the reservoirs, μ_D and μ_S, are broadened by thermal energy. (d, e) Current measured at (d) $V_3 = V_4 = -3.05\,\mathrm{V}$ and (e) $-3.10\,\mathrm{V}$. The color scale and range of V_1 and V_2 are the same as in (a). (d) As $V_3 = V_4$ becomes more negative, TP B (QD1–QD2) becomes closer to TP A. (e) TPs A and B merge, resulting in a QP (white dotted circle).

array unit for the two-dimensional integration of millions of spin qubits.

Chapter 5

Tunneling event detection using single-shot measurements improved by numerical treatments

In this chapter, we report detection of single tunneling event of electron in a physically defined silicon quantum dot system using numerical treatments. In the measurement, we observed single-shot tunneling events in a quantum dot using a charge sensor; however the tunneling statistics are difficult to acquire because of their weak signals. Hence, two numerical treatments using a digital filter and a change point detection technique are applied, and the latter enables precise signal detection, which is confirmed in the simulation. We expect the combination of such digital processing with integrated circuits to enable a fast qubit readout from a noisy system. This work is published in *Applied Physics Express*.[84]

5.1 Introduction

Qubit readout is an important component of quantum computing. Digital signal processing can facilitate qubit readout which often requires detection of two-level step signals. In the literature, a step detection technique known as Canny's edge detection has been demonstrated to enable more precise edge detections than simple thresholding.[85–88] Moreover, change point detection techniques are useful for pre-

cisely detecting steps, where the maximum log-likelihood ratio (LLR) is estimated between likelihoods for two conditions with and without a change point.[89, 20] Furthermore, it has been reported that the maximum LLR technique improves spin detection in the nitrogen-vacancy center.[90–92] These studies indicate the possibility that numerical treatments improve readout of spin qubit states. In the present study, we observed single tunneling events in a physically defined silicon quantum dot (PD-QD) system. We performed detection of tunneling events in a PD-QD system by monitoring current through a charge sensor (CS). However, the CS distant from the target QD resulted in low signal-to-noise ratio (SNR), preventing clear acquisition of tunneling events. To overcome this, we applied posterior numerical treatments and demonstrated the capability of one of the treatments to detect tunneling events from noisy signal.

5.2 Measurement setup

Figure 5.1 shows the PD-QD system used in this study. The QD device comprised a triangular triple QD (TTQD), CS, a top gate (TG), and four side gates (SGs). Two of the four SGs (R1 and R2) were open as well as the reservoir of the TTQD (T3) because of the limited number of available DC lines. DC voltages from floating voltage sources were applied to the other SGs (L1 and L2), TG, CS drain (D_{CS}), and other reservoirs of the TTQD (T1 and T2). A voltage, V_{TTQD}, was applied to both T1 and T2 to tune the potential of the TTQD in an offset bias voltage manner.[46] The PD-QD system was mounted on a printed circuit board together with RC LPFs for noise suppression. For TG, T1, and T2, RC filters with a low cut-off frequency f_c were used ($R = 390\,\mathrm{k\Omega}$, $C = 4.7\,\mathrm{nF}$, $f_c \sim 87\,\mathrm{Hz}$). On the other hand, RC filters for reservoirs of the CS were set to have higher frequencies not to prevent step detections ($R = 3\,\mathrm{k\Omega}$, $C = 220\,\mathrm{pF}$, $f_c \sim 240\,\mathrm{kHz}$ for D_{CS}, $R = 510\,\Omega$, $C = 220\,\mathrm{pF}$, $f_c \sim 1.42\,\mathrm{MHz}$ for S_{CS}). Moreover, AC voltages from an arbitrary waveform generator (AWG) were combined with the DC voltages applied to L1

and L2 using resistive voltage adders. The current flowing through the source of CS (S_{CS}), I_{CS}, was measured using an oscilloscope after the following treatments: conversion into voltage, further filtering with an active Bessel LPF with a cutoff frequency of 10 kHz, and amplification by a factor of 5. The Bessel filter determines the cutoff frequency of the system.

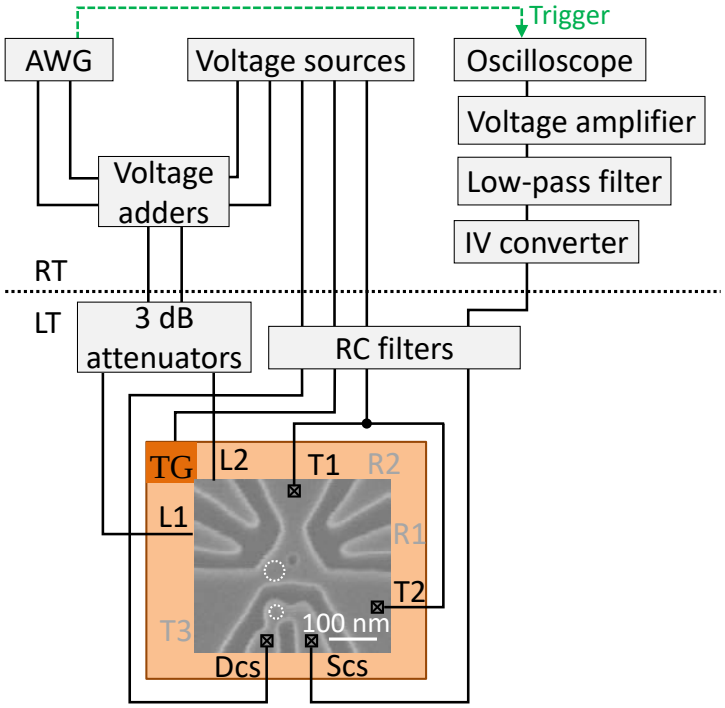


Figure 5.1: Measurement setup with scanning electron micrograph of quantum dot (QD) device nominally identical to measured one. White dotted circles indicate of the supposed positions of the target QD and charge sensor, respectively. See main text for details.

5.3 Charge sensing and the position of the quantum dot

We measured CS characteristics at 300 mK in advance to measurements for tunneling event detection. Here, only DC voltage sources and DC current monitor were used. Fig. 5.2 shows numerical differential conductance dI_{CS}/dV_{DSCS} as a function

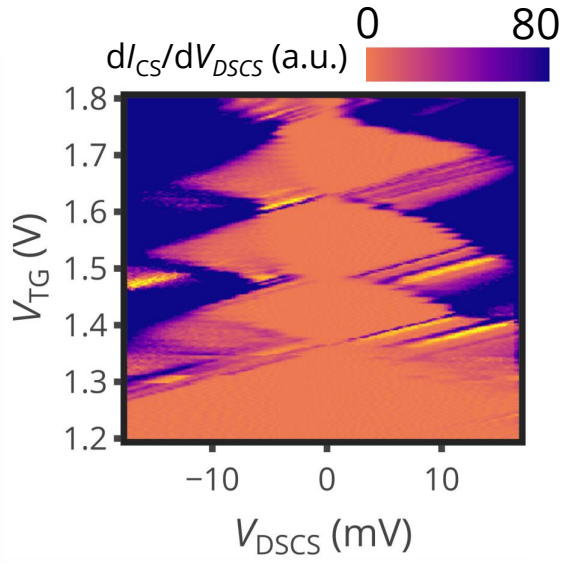


Figure 5.2: Coulomb diamond measurements on CS at 300 mK. $V_{\mathrm{L1}} = V_{\mathrm{L2}} = 0\,\mathrm{V}$.

of CS bias voltage V_{DSCS} and V_{TG}. There are clear Coulomb diamonds, indicating a formation of a well-defined single QD as expected.

Next, we tried charge sensing with the sensor by applying DC voltages. Fig. 5.3(a) shows $dI_{\mathrm{CS}}/dV_{\mathrm{SG}}$ as a function of V_{TG} and DC voltage commonly applied to L1 and L2, V_{SG}. In Fig. 5.3(a), charge sensing lines with a single slope appear in a wide range of voltage, indicating the formation of a single QD against expectation from QD design (Fig. 5.1). This may be because of strong QD-reservoir coupling of two of three QDs in TTQD. We also measured CS current as a function of V_{L1} and V_{L2} (not shown), but no charge sensing lines were recognized , possibly because of large steps for the voltage sweep and the charge sensing lines almost parallel to Coulomb peaks of CS. These results show the system was not ideal but still single-shot readout was possible as seen as follows. Another charge sensing measurement was performed with the setup in Fig. 5.1 except for voltage adders. In this measurement, voltage adders were omitted for wider AWG voltage range. We measured I_{CS} as a function of voltages applied to L1 and L2, i.e., V_{L1} and V_{L2}, respectively (Fig. 5.3 (b)) at 300 mK. In the measurement, a ramped voltage from -0.5 to 0.0 V was applied to L2, and the I_{CS} response was averaged 16 times at V_{L1},

while V_{L1} was changed step by step. As shown in the results, clear charge sensing lines appeared where charge transition occurred in one QD of the TTQD. To infer the position of the target QD, We checked the distance of the two lines in V_{L1} (in V_{L2}), and thereby the gate-QD capacitance is estimated to $\sim 0.38\,\mathrm{aF}$ ($\sim 0.29\,\mathrm{aF}$) by taking into account 3 dB attenuation for L1 (L2). The capacitance for L1 is close to the one between a gate and its closest QD estimated for a TTQD used in our previous study ($\sim 0.4\,\mathrm{aF}$).[49] Hence, we conclude that the target quantum dot was located at the QD connected to T3.

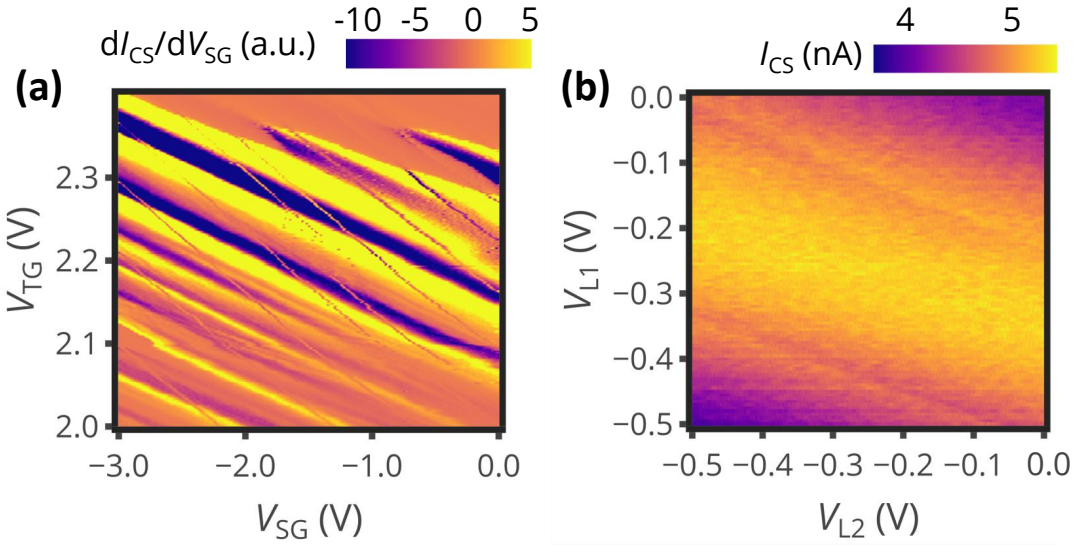


Figure 5.3: Charge sensing lines in a wide voltage range. (a) dI_{CS}/dV_{SG} as a function of V_{TG} and DC voltage commonly applied to L1 and L2, V_{SG}. $V_{DSCS} = -10\,\mathrm{mV}$, $V_{TTQD} = 0\,\mathrm{V}$. Charge sensing lines with a single slope appeared, implying a formation of a single QD in the TTQD. (b) I_{CS} as a function of V_{L1} (step) and V_{L2} (ramp). In the measurement, voltage adders for L1 and L2 were not used, so that actual gate voltages were twice as high as with the voltage adders. From the distance of the two sensing lines, gate-QD capacitances were estimated.

5.4 Single-shot tunneling detection

To identify a favorable condition for the single-shot readout, we measured I_{CS} as a function of V_{L1} and V_{L2} with a different parameters in the setup in Fig. 5.1

(Fig. 5.4(a)). In the measurement, a ramped voltage from -1.0 to $0.0\,\mathrm{V}$ was applied to L2 in addition to a DC constant voltage of $-0.5\,\mathrm{V}$ via a voltage adder while V_{L1} was changed step by step from -1.0 to $0.0\,\mathrm{V}$. For tunneling detection measurements, we fixed $V_{\mathrm{L2}} = -0.21\,\mathrm{V}$ because of the excellent sensitivity.

Next, we applied voltage pulses to L2 and observed single tunneling events in a single-shot manner (Figs. 5.4(c) and (d)). The applied pulse comprised three levels, as shown in Fig. 5.4(c), each corresponding to the position of the same symbol in Fig. 5.4(a). The functions of the three levels were to load an electron into the QD ("load" level, $V_{\mathrm{L2}} = -0.5\,\mathrm{V}$), to read a tunneling event from the QD to its reservoir ("read" level, $V_{\mathrm{L2}} = -1.0\,\mathrm{V}$), and to ensure that the QD was empty ("empty" level, $V_{\mathrm{L2}} = -1.5\,\mathrm{V}$). The "read" level was selected as a voltage sufficiently close to the charge transition point with a moderate tunneling rate.

An example of the pulse response is shown in Fig.. 5.4(d). As indicated by the orange arrow, a time-dependent step signal appeared owing to single electron's tunneling out of the QD. We repeated the pulse measurement 864 times under the same DC voltage to acquire the statistics of the tunneling events. The inset of Fig. 5.4(d) shows the averaged current in the "read" level over all the pulse measurements. As expected for a Poisson distribution with a rate Γ within the tunneling time, the averaged current exhibited an exponential decay, with a distortion. From the latter half of the averaged current, Γ was estimated to be $\sim 100\,\mathrm{Hz}$.

To acquire the tunneling rate around the charge sensing line in Fig. 5.4(a), we measured averaged pulse response as a function of V_{L1}. In the measurement, the pulse voltage in Fig. 5.4(c) was applied to L2 while VL1 was changed step by step. Here, I_{CS} was averaged 16-times by a built-in function of the oscilloscope instead of numerical averaging which was used in the inset of Fig. 5.4(d). In the V_{L1} range, "load" and "empty" levels were always far away from the charge sensing line. Thereby, the measured current at "read" level shows exponential curves reflecting the single tunneling events as a function of distance from the charge sensing line

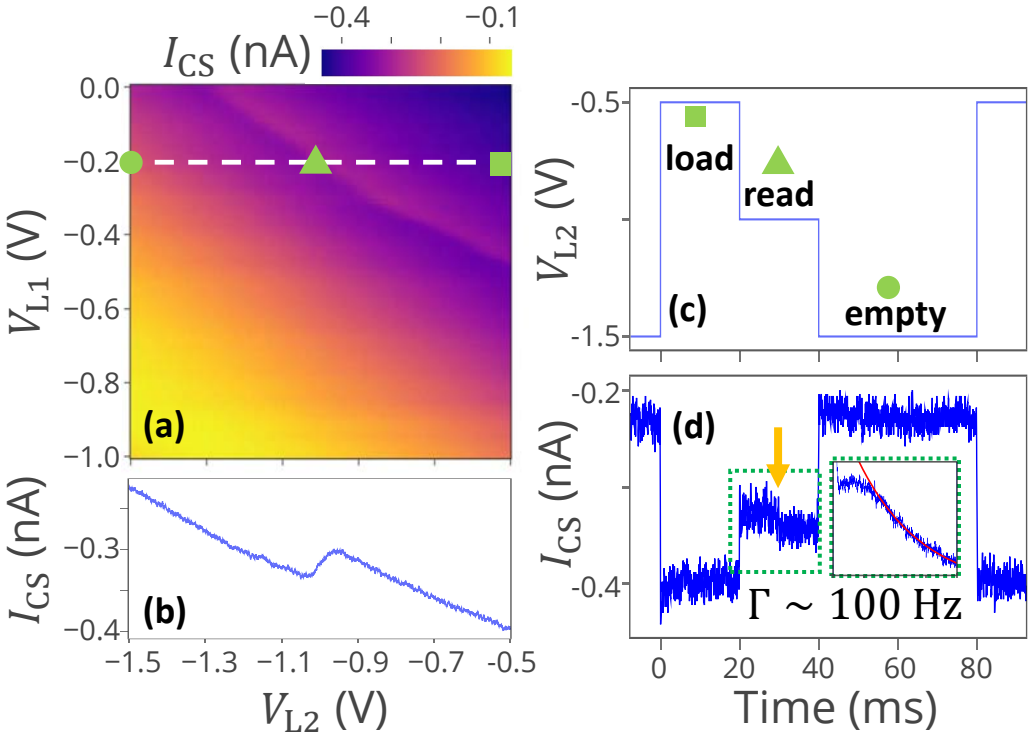


Figure 5.4: (a) 16-times averaged charge sensor current I_{CS} as a function of two side-gate voltages V_{L2} and V_{L1}. A clear charge-sensing line appeared. Symbols on dashed line (circle, triangle, and square) represent three levels of pulse used in the single-shot measurement in (c) and (d). $V_{TG} = 1.795\,V$, $V_{Dcs} = 30\,mV$, and $V_{TTQD} = 25\,mV$. (b) Horizontal cut of (a) at $V_{L1} = -0.21\,V$ (white dashed line in (a)). Kink indicates the position where electron transition occurred in one QD of the TTQD. (c, d) Three-level voltage pulse (c) and response (d). As indicated by the orange arrow in (d), a time-dependent tunneling event was obtained. Inset: I_{CS} at the "read" level averaged over 864 pulse measurements (blue). Latter half of current was fitted with an exponential function (red), and Γ was estimated to be $\sim 100\,Hz$.

(Fig. 5.5(a)). As a result, the exponential decays around $V_{L1} = -0.25\,V$ show different amplitudes and decay times, corresponding to changes in sensor sensitivity and tunneling time, respectively (Fig. 5.5(b)). Even though we would have liked to set the condition with maximum sensitivity and a good tunneling rate, shifts of applied voltage prevented it. The cause of the shifts is unclear, but it may come from measurement system rather than device characteristics. This is because the shift was reproducible and depended on the start voltage of a measurement.

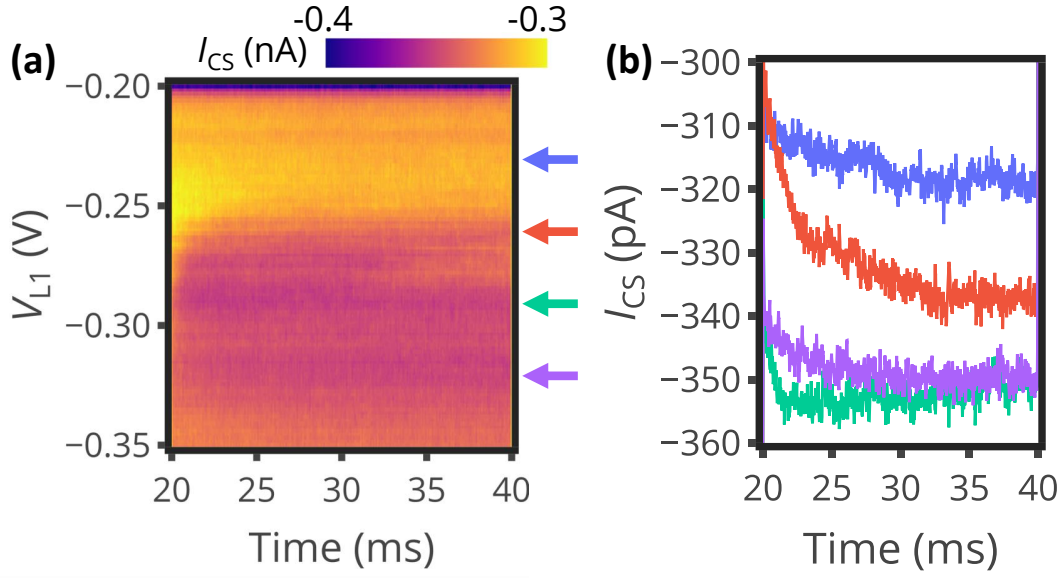


Figure 5.5: (a) Averaged pulse response of I_{CS} at "read" level at different V_{L1}. The current was averaged by a built-in function of the oscilloscope. (b) Horizontal cut of (a) at $V_{L1} = -0.23\,V$ (blue), $-0.26\,V$ (red), $-0.29\,V$ (green), and $-0.32\,V$ (purple). V_{L1} for each trace corresponds to the position indicated by an arrow with the same color in (a). The exponential decays show different amplitudes and decay times, corresponding to changes in sensor sensitivity and tunneling time, respectively.

5.5 Digital low-pass filtering

As shown in Fig. 5.4(d), the SNR of the step signals was not sufficiently high for single-shot tunneling event detection, at least, by a simple thresholding. Hence, we applied two posterior treatments separately to extract the location where tunneling events occurred: digital LPF and change point detection using LLR. First, we applied a digital LPF to the data for noise suppression. The filter was applied after subtracting the average current in the "empty" level for each single-shot trace to suppress fluctuations among all the repeated measurements. As the digital filter, we selected a 10th-order digital Bessel LPF with a -3-dB cutoff frequency $f_c = 500\,Hz$ using Python package "scipy." Figure 5.6(a) shows a comparison of the pulse response at the "read" level before and after the LPF treatment. As shown, the LPF suppressed the noise significantly. After the LPF treatment, tunneling positions in the pulse measurements were detected by thresholding each pulse response at the

"read" level. To obtain the optimal threshold, we referred to a histogram of I_{CS} at the "read" level including all the repetitions, and it indicated a clear bimodal characteristic (Fig. 5.6(b)). Therefore, we set the threshold current for tunneling detection to the minimum count position between the two peaks. By detecting the falling edge with the threshold, a histogram for the tunneling time was obtained, and a fitting over the whole x-axis range of the data points with an exponential function revealed Γ to be $\sim 180\,\mathrm{Hz}$ (Fig. 5.6(c)). However, this value was almost twice larger than that obtained from the averaged current in the inset of Fig. 5.4(d), and the fitting exhibited a clear exponential decay without distortion, unlike the averaged current, implying errors in the step detection. These discrepancies may be attributed to slow fluctuations during each pulse measurement, whose frequency was supposed to be significantly lower than the cutoff frequency and hence difficult to suppress.

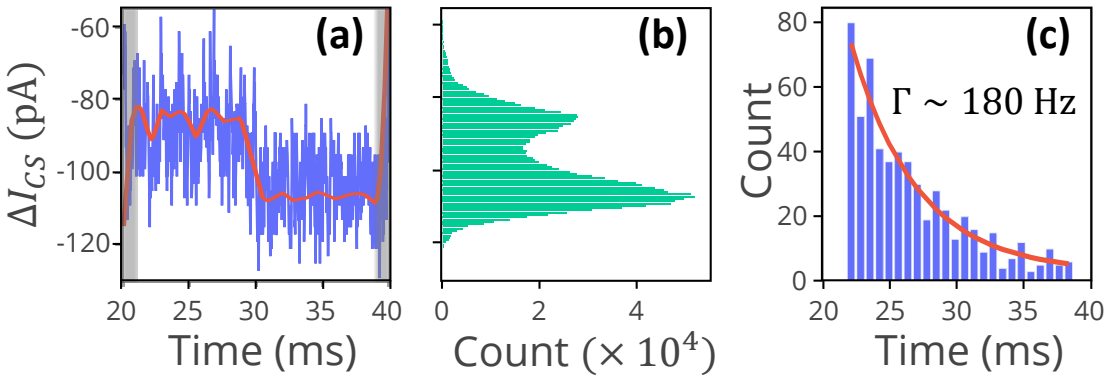


Figure 5.6: (a) Example of comparison between pulse responses at "read" level before and after digital LPF treatment (blue and red traces, respectively). Offset due to the filtering was compensated by subtracting the difference between averaged currents before and after digital filtering at the "read" level. (b) Histogram of pulse measurements after LPF treatment. LPF treatment elongated transient responses, as shown in gray shades in (a); therefore, the histogram was used for the data points between the shades. (c) Histogram of tunneling times obtained by thresholding digitally filtered single-shot data (blue). It was fitted with an exponential function (red), and Γ was estimated to be $\sim 180\,\mathrm{Hz}$.

5.6 Change point detection

Next, we applied the other numerical treatment based on change point detection theory.[89, 20] In the present study, we used the simplest one involving the LLR, which is effective for step detection.[93, 94] This technique has been utilized in some studies using GaAs QDs to count tunnel events or to study hidden Markov models.[95, 96] Meanwhile, we applied this technique to investigate noisy tunneling event signals in a silicon QD. The LLR can be calculated by taking the logarithm of the ratio of a likelihood $\mathcal{L}(H_1)$ for a single change point hypothesis H_1 to another likelihood $\mathcal{L}(H_0)$ for a null hypothesis H_0 is estimated. Each likelihood can be expressed as below:

$$\mathcal{L}(H_0) = p(X|H_0) = \prod_{i=1}^{N} p(x[i]|\bar{x}_N), \tag{5.1}$$

$$\mathcal{L}(H_1) = p(X|H_1) = \prod_{i=1}^{r} p(x[i]|\bar{x}_r) \prod_{j=r+1}^{N} p(x[j]|\bar{x}_{N-r}), \tag{5.2}$$

where $p(x|\theta)$ is a probability density function for x given θ, r is an assumed change point, $\bar{x}_N = \sum_{i=0}^{N-1} x[i]/N$, $\bar{x}_r = \sum_{i=0}^{r} x[i]/(r+1)$, and $\bar{x}_{N-r} = \sum_{i=r+1}^{N-1} x[i]/(N-r-1)$. When $p(x|\theta)$ is a Gaussian distribution function with a standard deviation σ as seen in Fig. 5.6(b), $p(x|\theta) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\theta)^2}{2\sigma^2}}$, the log-likelihood $\mathcal{R}$ is

$$\begin{aligned}
\mathcal{R}[r] &= \ln\left(\frac{\mathcal{L}(H_1)}{\mathcal{L}(H_0)}\right) \\
&= -\frac{1}{2\sigma^2}\left\{\sum_{i=0}^{r}(x[i]-\bar{x}_r)^2 + \sum_{j=r+1}^{N-1}(x[j]-\bar{x}_{N-r})^2 - \sum_{k=0}^{N-1}(x[k]-\bar{x}_N)^2\right\} \\
&= -\frac{1}{2\sigma^2}\left\{-(r+1)\bar{x}_r^2 - (N-r-1)\bar{x}_{N-r}^2 + N\bar{x}_N^2\right\} \\
&= -\frac{(\bar{x}_{N-r}-\bar{x}_r)^2}{2\sigma^2((r+1)^{-1}+(N-r-1)^{-1})}.
\end{aligned} \tag{5.3}$$

Then, the index whose $\mathcal{R}$ shows a maximum value, $\hat{r} = \underset{0\le r\le N-1}{argmax}(\mathcal{R})$, is most likely to be the change point.

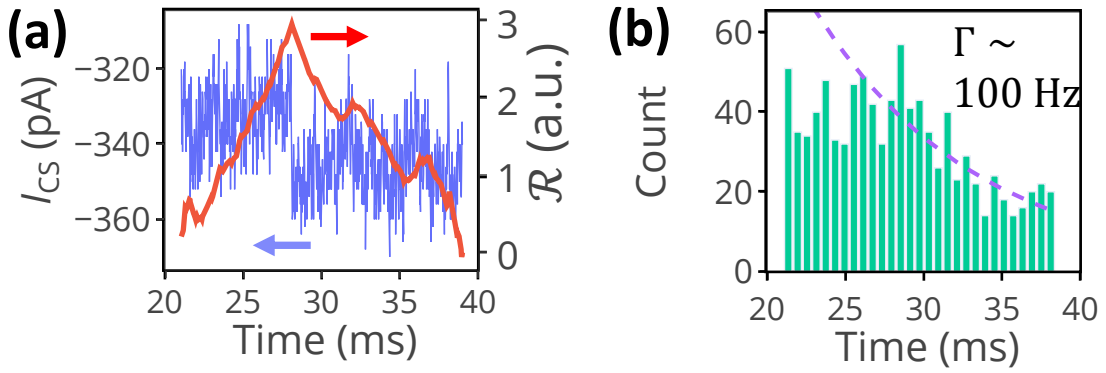


Figure 5.7: (a) Raw data at "read" level (blue) and its log-likelihood ratio (LLR), R (red). Maximum position of R indicates step position. (b) Histogram of tunneling time obtained by LLR estimation (green). It exhibited an exponential decay with a distortion, as expected. From an exponential fitting of the latter half of the histogram (purple dashed line), Γ was estimated to be ∼ 100 Hz, which agrees well with that estimated from the averaged current (inset in Fig. 5.4(d)).

Figure 5.7(a) shows the measured pulse response, I_{CS}, and the corresponding LLR result. As shown in the figure, the maximum position in $\mathcal{R}$ detected the step position of the noisy raw data. We repeated the LLR calculation over all the pulse responses and obtained a histogram of the tunneling times (Fig. 5.7(b)). Unlike the digital LPF result, the distortion was qualitatively reproduced, implying its better validity. By fitting the histogram, Γ was estimated to be ∼ 100 Hz. This value corresponds to that estimated from the averaged current and is therefore supposed to be more reliable than that for the digital LPF treatment.

5.7 Simulation for comparison of the digital signal process techniques

To confirm the significance of the maximum LLR test, we compared the two numerical treatments in the simulation. For the simulation, noisy steps corresponding to the measured responses were generated. Each signal had a step with a height of 2,

2000 data points corresponding to a time scale from 20 to 40 ms in the measurements, and a step length determined probabilistically using a Poisson distribution. First, we tried adding white noise and 1/f noise to the ideal steps using a python package "colorednoise". The results are shown in the Fig. 5.8(a-d). Fig. 5.8(a) shows a fast Fourier transform (FFT) of squares of measurement and simulation results. By tuning the balance between white noise and 1/f noise, the simulation has a qualitatively good agreement with measurement result. Figs. 5.8(b) and (c) show comparisons in single step and in histogram of all the single-shot traces. In Fig. 5.8(c), the peak position of measurement result is shifted by 337 pA, and the amplitude of the simulation is divided by a factor of 0.7 for obvious comparison between simulation and measurement. It reveals that the standard deviations for both histogram peaks are almost the same. On the other hand, after digital LPF treatments, the histogram of the simulation result could not reproduce the measurement result (Fig. 5.8(d)). This may be attributed to the effect from other types of noise such as Brownian noise.[97] Brownian noises can have Lorentzian spectra which deviate from and become weaker than $1/f^2$ characteristics for low frequencies.

Next, we added noise comprised white Gaussian noise (mean = 0; standard deviation = 1) and different offsets for step signals that mimicked the slow fluctuation in the measurements, resulting in an SNR of ~ 1 in the step signals, as observed in the measurements (Fig. 5.9). The offsets exhibited a Gaussian distribution (mean = 0; standard deviation = 0.55) and qualitatively reproduced the histogram in Fig. 5.6(b) (Fig. 5.9(a)). In Fig. 5.9(b), we compare the histograms of step positions detected using the two numerical treatments with the histogram of the original step positions. Even though the digital LPF result (green solid line) agreed well with the original step histogram (red dotted line), unlike the measurement result, the maximum LLR test result (blue solid line) indicated a better result with an almost complete agreement with the original one, revealing its strong ability in detecting steps.

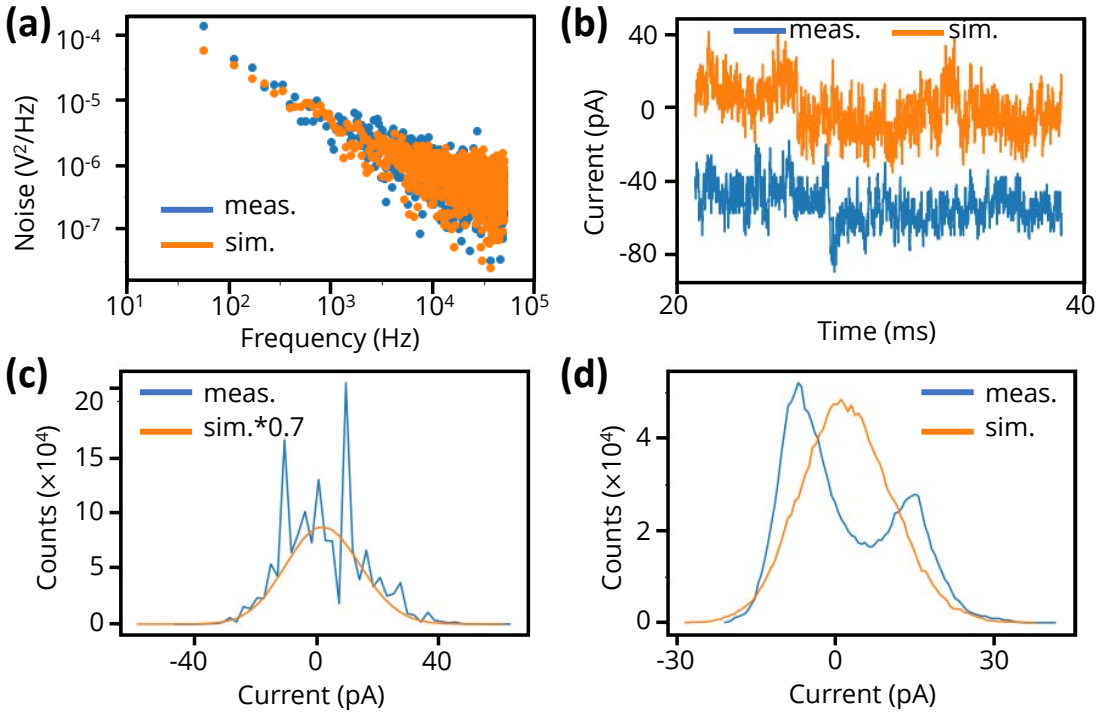


Figure 5.8: Simulation including $1/f$ noise. (a) Noise spectra in the measurement (blue) and simulation (orange). To obtain each spectrum, fast Fourier transforms were performed on squared single traces separately and averaged over all the obtained FFT spectra. The simulation agrees with the measurement result well. (b) Comparison of single signals from simulation and measurement results. (c) Comparison of histograms from simulation and measurement results. For visibility of peak width, the height of the histogram for simulation decreased by a factor of 0.7, and the peak position of the histogram for measurement result was shifted by 337 pA. (d) Comparison of histograms from simulation and measurement results after digital LPF treatments. The peak position of the histogram for measurement result was shifted by 100 pA. A single peak appeared in the histogram for simulation, while a bimodal peak appeared in the histogram for measurement results in Fig. 5.6(b). This discrepancy may be attributed to difference between simulation and measurement in $1/f$ noise.

5.8 Summary

In this chapter, we successfully observed tunneling events in a single-shot manner in PD-QDs. Even though the SNR of the charge sensor signal was lower than unity, the digital LPF treatment and the change point detection technique applied enabled tunneling event detection. For the digital LPF, a 10th-order Bessel LPF was

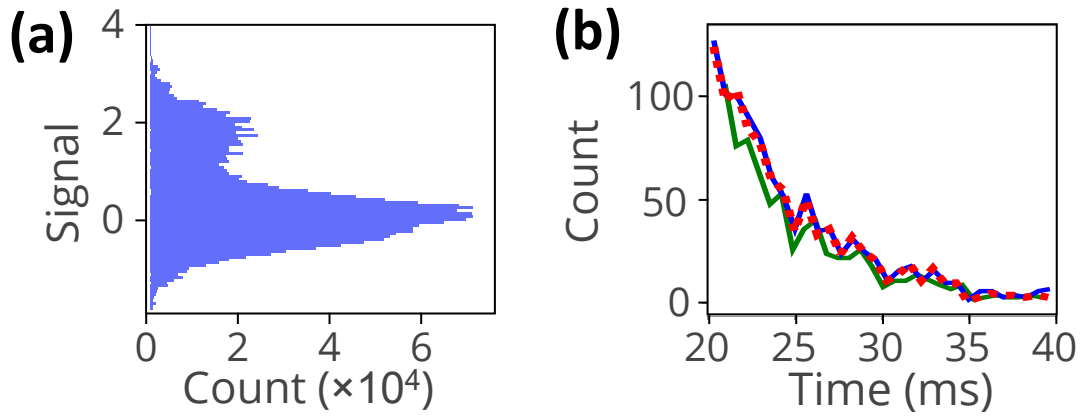


Figure 5.9: (a) Histogram of data points in all step signals after digital LPF treatment. Noise was selected such that the histogram resembled that in Fig. 5.6(b). (b) Comparison between histograms of step positions obtained from two numerical treatments in simulation. First, we generated the same 1000 step signals except for the step lengths determined probabilistically via a Poisson distribution. At this point, a histogram of tunneling time was created from the data (red dotted line). Subsequently, noise was added to the signals, and histograms of step positions detected after a digital LPF (green solid line) and by change point detection using LLR (blue solid line) were obtained.

utilized, and its noise suppression facilitated step detection even though Γ appeared to be overestimated, likely owing to slow fluctuations in the signals. Meanwhile, a change point detection technique using the LLR was applied to the raw measurement data; it was discovered that the LLR precisely indicated the step position as its maximum position. Finally, we compared the two techniques by applying them to generated step signals and demonstrated the significance of the maximum LLR test technique. This step detection may be useful for spin readouts where the step signal appears.[98–100] In addition, according to Ref. 94, the technique is applicable to pulse detection, which is often required for a spin readout using tunneling between a QD and its reservoir.[101, 18, 41] We expect that this technique facilitates qubit characterizations, and that its combination with an integrated circuit enables a fast qubit readout from a noisy system.

Chapter 6

Radio-frequency single electron transistors with a sensitive phase response

Radio-frequency reflectometry techniques are instrumental for spin qubit readout in semiconductor quantum dots. However, a large phase response is difficult to achieve in practice. In this chapter, we report radio-frequency single electron transistors using physically defined quantum dots in silicon-on-insulator. We study quantum dots which do not have the top gate structure considered to hinder radio frequency reflectometry measurements using physically defined quantum dots. Based on the model which properly takes into account the parasitic components, we precisely determine the gate-dependent device admittance. Clear Coulomb peaks are observed in the amplitude and the phase of the reflection coefficient, with a remarkably large phase signal of ~ 45 degree. Electrical circuit analysis indicates that it can be attributed to a good impedance matching and a detuning from the resonance frequency. We anticipate that our results will be useful in designing and simulating reflectometry circuits to optimize qubit readout sensitivity and speed. This work is published in *Scientific Reports*.[102]

6.1 Introduction

To adapt to the requirements for fast and quantum-non-demolition spin readout for fault-tolerant quantum computing,[2, 29, 30] radio-frequency (RF) reflectometry has been widely studied in the QD systems.[59, 103, 25, 104, 105, 35, 106] This technique utilizes impedance matching between the transmission line and the QD system within a resonator.[21] Therefore, modifications are often necessary to apply this technique to nanostructures with different designs. Recently, fast spin readout within coherence times was realized in a gate-defined silicon QD with a RF single electron transistor (RF-SET) charge sensor.[59]

Physically defined silicon QDs (PD-QDs) based on the silicon-on-insulator (SOI) technology[45–51, 84] would offer high flexibility in QD arrangement and suitability to dense two-dimensional QD integration without the need of gates for quantum confinement.[49] However, the PD-QD with the top gate structure is yet to be successfully combined with the RF-SET, possibly because of formation of a RC filter due to the reservoir of a resistive silicon channel and the capacitance of a 20-μm square top gate.[59, 103, 107, 108] One way to avoid this problem is to simply reduce the size of the top gate.[59, 108] An alternative solution would be to completely remove the top gate structure, made possible thanks to the SOI-based QD structures.[49, 109] In this work, we report a large phase response and a detailed circuit analysis of RF-SET measurement in PD-QDs without the top gate structure.

6.2 Device fabrication and measurement setup

The PD-QD devices were fabricated in line with our previous studies.[49] In each device, the top gate structure is omitted to avoid RF leakage to the top gate; instead, the back gate is used to accumulate electrons. A scanning electron micrograph (SEM) of a PD-QD nominally identical to the ones used in this work is shown in Fig. 6.1. A charge sensor and side gates (SGs) are also formed in the same SOI

layer as the QDs. However, some of them are set to be floating and do not play a role in the following experiments. A positive back gate voltage is applied to the Si substrate of the SOI wafer across the 145-nm thick buried oxide layer to accumulate electrons. The device is mounted on a printed circuit board (PCB) along with components for the bias tee and for the LC resonance circuit for RF-SET (Fig. 6.1). Parasitic capacitances of the PCB and the device form part of the LC circuit. All measurements in this paper are performed with devices immersed in liquid helium and hence at 4.2 K. We use a vector network analyzer (VNA) and apply the RF power output from port 1 of the VNA to the device after 60-dB attenuation. The signal reflected at the device is input into port 2 of the VNA after amplification of 35 dB. We note that the signal is amplified only at room temperature, not at cryogenic temperature.

6.3 Frequency dependence and electrical circuit analysis

We also perform fitting of frequency dependence of the RF-SET without additional parasitic components (Fig. 6.2). The equivalent circuit consisting of the inductance L, capacitance C, and conductance G is shown in Fig. 6.2(a). In Figs. 6.2(b) and (c), the amplitudes and the phases of the measured reflection coefficient are plotted, respectively, along with the simulated results. Here, the measurement results are the same as the ones in Fig. 6.3 in the main text. We fit the data without introducing the additional parasitic components (red dotted lines in Figs. 6.2(b) and (c)). The results agree well with the measurement result; however, (the value of) L used for the fitting is 2.36 μH which is 3.5 times larger than the nominal inductance. This can be understood by the same mechanism as the self-resonance of the inductor due to its parasitic capacitance. As the frequency approaches the self-resonance, the inductance increases until the inductor starts to behave like a capacitor above the

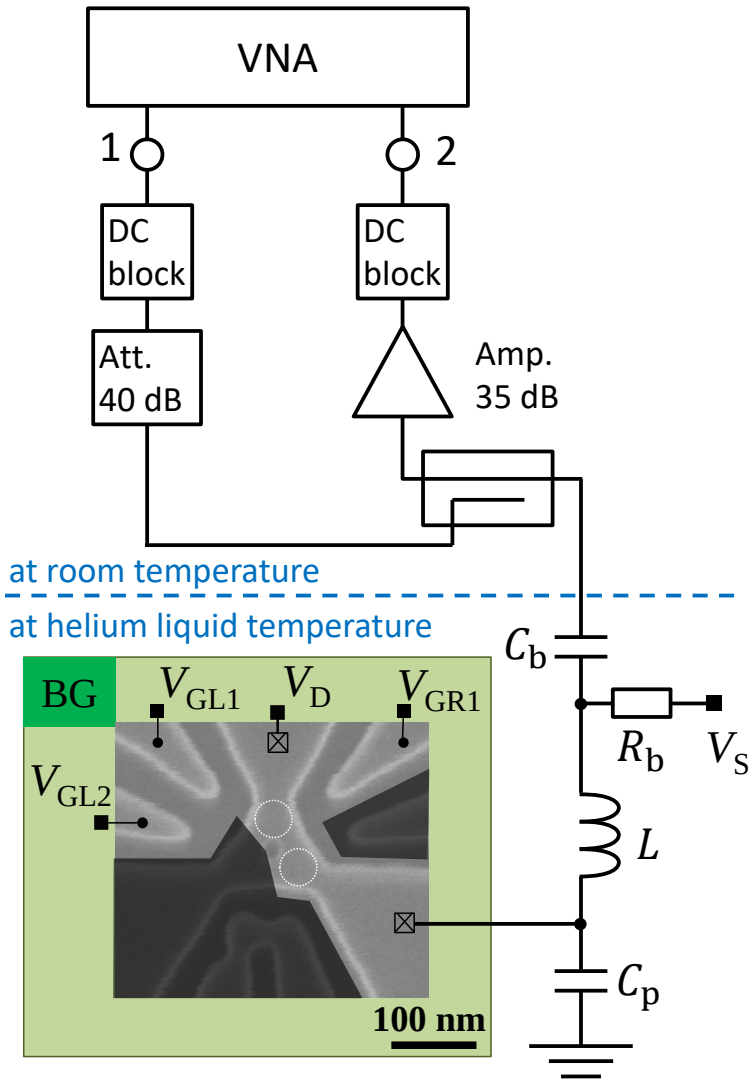


Figure 6.1: Measurement setup with a scanning electron micrograph of a physically defined quantum dot (PD-QD) device nominally identical to the measured ones. The PD-QDs do not have top gates. Drain voltage, V_D, source voltage, V_S, side gate voltages, V_{GL1}, V_{GL2}, and V_{GR1}, and back gate voltage, V_{BG}, can be applied. Shadowed areas indicate unused floating electrodes: a side gate, a single QD charge sensor, and a reservoir. An LC resonance circuit for impedance matching, which comprises a surface mount wire-wound inductor with an inductance $L = 680\,\mathrm{nH}$ and parasitic capacitance C_p , is connected to the source of the QD. In addition, an RC bias tee ($R_b = 5\,\mathrm{k\Omega}$ and $C_b = 4.7\,\mu\mathrm{F}$) is connected to the LC circuit in series to apply a DC voltage V_S. For RF measurement, a vector network analyzer (VNA) outputs the RF signal from port 1, which is applied to the device after attenuation to suppress heating up the QD. The signal reflected from the device is branched by directional coupler and input to port 2 of VNA after amplification.

resonance frequency. This result indicates the necessity of introducing the additional parasitic components for the fitting.

For the completeness, we also simulate the characteristics with L fixed to the nominal value, 680 nH (green dotted lines in Figs. 6.2(b) and (c)). G and C are estimated from the load impedance calculated from the reflection at the resonance and from the resonance frequency. The result apparently deviates from the measurement data, also indicating requirements for additional parasitic components for the fitting.

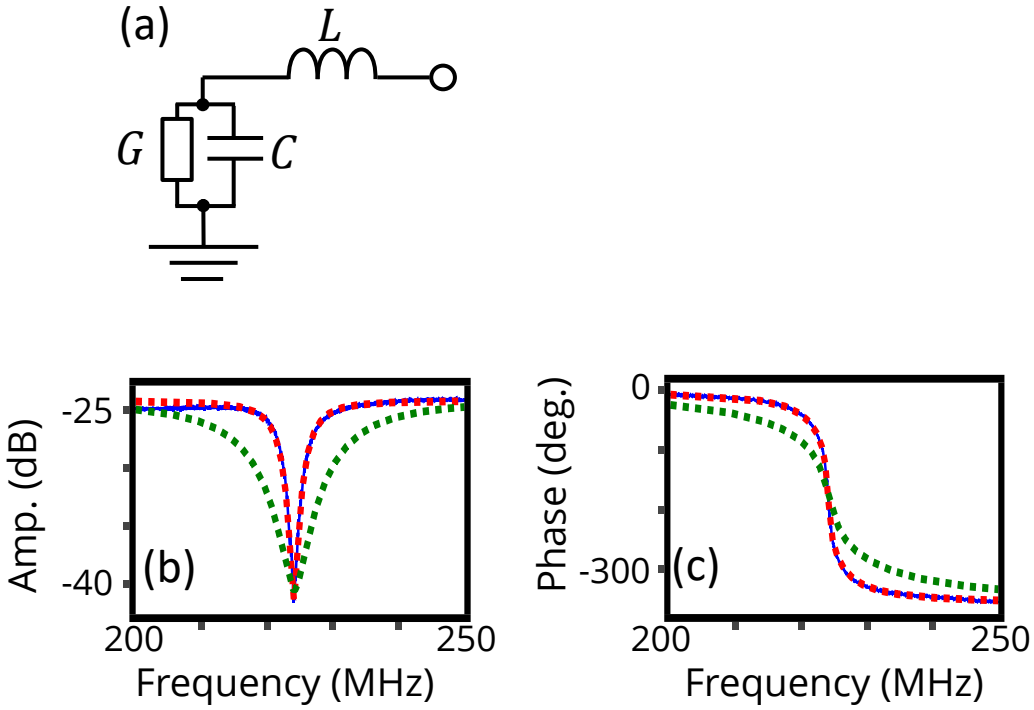


Figure 6.2: An equivalent circuit without additional parasitic components for RF reflectometry. (b,c) Amplitude and phase of the reflection coefficients as a function of carrier frequency. Measurement results (blue solid line) which are also shown in Fig. 6.3 in the main text are fitted based on the equivalent circuit in (a) (red dotted line), yielding $L = 2.36\,\mu$H, $C = 214$ fF, and $G = 3.43\,\mu$S. Green dotted line shows a simulation result for which L is fixed to its nominal value, 680 nH, while the other parameters are obtained from the resonance frequency and the amplitude of reflection coefficient at resonance: $G = 40\,\mu$S and $C = 740$ fF.

6.4 Fitting with additional parasitic components

First, we study the frequency dependence of the reflection coefficient at the device, Γ, without carrier accumulation using the back gate voltage $V_{\mathrm{BG}} = 0\,\mathrm{V}$ (blue solid lines in Fig. 6.3(a) and (b)). Here, the charge sensor and all SGs are set to be floating for simplicity. A dip appears at a frequency which corresponds to the resonance of the circuit ($f_{\mathrm{r}} = 224.063\,\mathrm{MHz}$). In a simple description of the LC resonance circuit, the load impedance, Z_{load}, is proportional to device conductance at resonance; this would suggest that Z_{load} should be close to zero in this case, which would result in almost complete reflection. This apparent discrepancy can be explained by the dielectric loss in the PCB which contributes as a conductance parallel to the device.[25] Given this, Z_{load} has a finite value (at frequencies around the resonance) and $\Gamma = (Z_{\mathrm{load}} - Z_0)/(Z_{\mathrm{load}} + Z_0)$ can approach zero, where $Z_0 = 50\Omega$ is the characteristic impedance of the external signal line.

As we will see below, the frequency dependence of observed reflection can be described by the equivalent circuit shown in Fig. 6.3(c). The circuit mainly consists of an inductance, L, a parasitic capacitance, C_{p}, and a QD impedance composed of a parallel circuit of a conductance G_{QD} and a capacitance C_{QD}; however, each component has additional parasitic components in reality. Here, we take into account the parasitic capacitance and resistance in the coil, C_{L} and R_{L}, and the parasitic conductance in the capacitor, G_{p}. G_{p} and R_{L} are due to dielectric loss and skin effect, respectively, so that each has a frequency dependence: $G_{\mathrm{p}} = \omega C_{\mathrm{p}} \tan\delta$ and $R_{\mathrm{L}} = \rho_{\mathrm{L}}\sqrt{\omega}$, where $\omega = 2\pi f$ is the angular frequency, $\tan\delta$ is loss tangent, and ρ_{L} denotes a coefficient.[110] In addition, the effects of external components are considered, such as coaxial cables, attenuators, and amplifiers. Attenuation and amplification offset the amplitude of the reflected signal, and the coaxial cable causes a linear phase shift as a function of frequency due to its propagation constant.

Figures 6.3(b) and (c) show fitting results for the amplitude and the phase of

the observed reflection at $V_{\mathrm{BG}} = 0\,\mathrm{V}$ based on the equivalent circuit with following parameters (red dotted lines): $L = 680\,\mathrm{nH}$, $\rho_{\mathrm{L}} = 190\,\mu\Omega/\sqrt{\mathrm{rad/s}}$, $C_{\mathrm{L}} = 348\,\mathrm{fF}$, $C_{\mathrm{p}} = 394\,\mathrm{fF}$, and $\tan\delta = 0.00614$. Here, to reduce the number of fitting parameters, the nominal value of L is assumed, and ρ_{L} is separately estimated from the measured transmission characteristic of an inductor nominally identical to the one used in these measurements (supporting information). The fittings have good agreements with the measurement results, proving the validity of the equivalent circuit model. The small deviation at off-resonance frequencies can be attributed to a background frequency dependence due to interference between the reflected signal and the isolation leakage in the directional coupler.[110] The necessity for additional parasitic components can be confirmed from fitting with a simple LCR circuit without taking into account additional parasitic components, where an inductance 3.5 times larger than L is required for a good fitting (see supporting information for details).

6.5 Estimation of parasitic components of the inductor at liquid helium temperature

To analyze the RF-SET characteristics, we obtain parasitic components of nominally the same inductor as used in the main text separately and in advance. Values of such parasitic components at room temperature are available in the datasheet of the inductor, but they will change at cryogenic temperatures due, e.g., to a decrease in copper wire resistance and a change in the permeability of the core.

The inductor impedance including parasitic components, Z_{L}, are extracted from transmission measurement at 4 K using a nominally identical inductor to that used in the main text (LQW2BASR68J00L, Murata Electronics). To do this, we first solder the inductor on a PCB to make a transmission path through the inductor. Next, we connect the PCB to a vector network analyzer (VNA) and then measure the transmission from port 1 to port 2, S_{21}, with the inductor at helium liquid

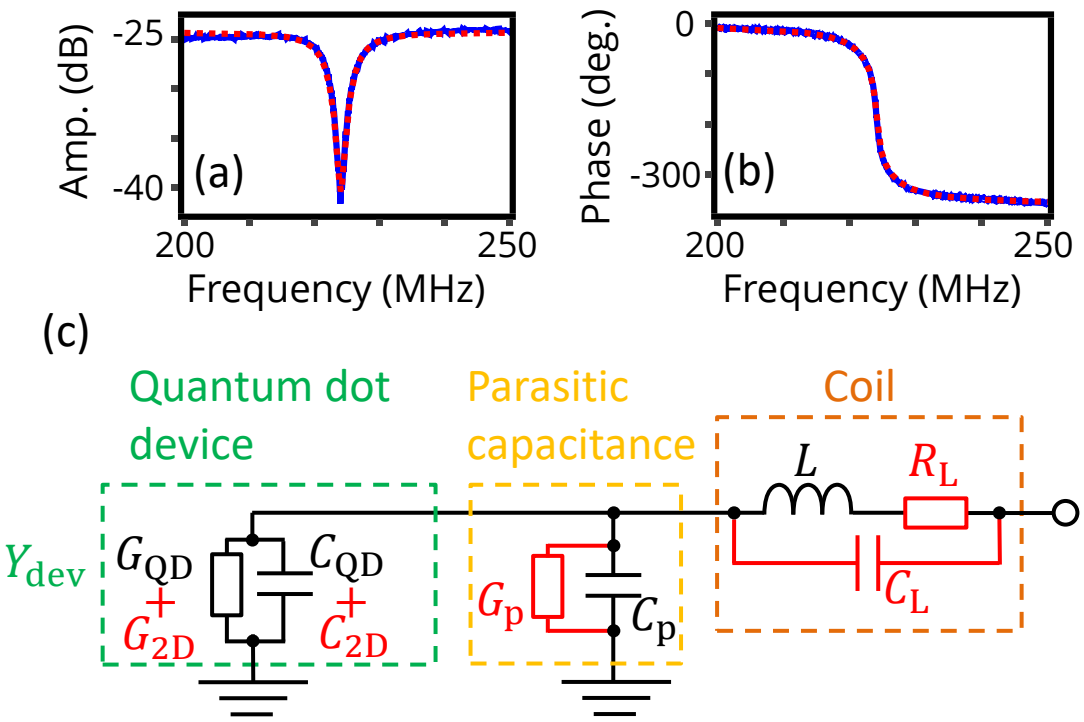


Figure 6.3: (a,b) Amplitude and phase of the measured transmission signal from port 1 to port 2 at liquid helium temperature as a function of carrier frequency (blue solid lines). No DC voltages are applied to the device. Results from fitting based on the equivalent circuit in (c) are shown as well (red dotted lines). (c) An equivalent circuit for the load impedance, in which additional parasitic components are also taken into account.

temperature (blue solid lines in Figs. 6.4(b) and (c)). As expected, $|S_{21}|$ shows a dip corresponding to self-resonance due to parasitic capacitance of the inductor.

To fit the results, S_{21} is formulated as follows. The voltage at each point in Fig. 6.4(a) can be described by:

$$V_{\mathrm{A}} = V_{\mathrm{i}} + V_{\mathrm{r}} \tag{6.1}$$

$$V_{\mathrm{B}} = (1 + \Gamma_{\mathrm{B}}) V_{\mathrm{i}} e^{-\mathrm{i}\beta \mathrm{l}} \tag{6.2}$$

$$V_{\mathrm{C}} = V_{\mathrm{B}} Z_0 / (Z_{\mathrm{L}} + Z_0) \tag{6.3}$$

$$V_{\mathrm{D}} = V_{\mathrm{C}} e^{-\mathrm{i}\beta \mathrm{l}'} \tag{6.4}$$

where V_{i} and V_{r} are incident and reflected voltages at point A, $\Gamma_{\mathrm{B}} = Z_{\mathrm{L}}/(Z_{\mathrm{L}} +$

$2Z_0$) is the reflection coefficient at point B seen from left-hand side, $Z_0 = 50\,\Omega$ is the characteristic impedance, $l(l')$ is the length of the coaxial cable between points A and B (C and D), and β is the propagation constant without attenuation of the coaxial cables which is proportional to carrier frequency. In addition, it is assumed that reflection at each VNA port does not occur thanks to impedance matching. Thereby, the transmission coefficient S_{21} is

$$S_{21} = V_{\rm D}/V_{\rm i} = 2Z_0/(Z_{\rm L} + 2Z_0)e^{-{\rm i}\beta({\rm l}+{\rm l}')}. \tag{6.5}$$

Using this equation, we perform a fitting with $Z_{\rm L}$ including the parasitic capacitance $C_{\rm L}$ and resistance $R_{\rm L} = \rho_{\rm L}\sqrt{\omega}$. In Figs. 6.4(b) and (c), the fitting results are shown, which agree well with the measurements (red dotted lines). Here, the inductance is fixed to the nominal value of the inductor. From the fitting, following parameters are obtained: $C_{\rm L} = 0.30\,{\rm pF}$, and $\rho_{\rm L} = 190\mu\Omega/\sqrt{{\rm rad/s}}$. The estimated value of $\rho_{\rm L}$ is utilized for the fitting in the main text while that of $C_{\rm L}$ is not because it depends on soldering condition.

At frequencies higher than the self-resonance frequency, a deviation from the fitting in the transmission appears, which may be attributed to other parasitic components such as the inductance of bonding wires. Here, their contributions are ignored because they are effective outside the frequency range used in the main text.

6.6 Back gate voltage sweeping

Next, we investigate the reflection dependence on back gate voltage, $V_{\rm BG}$, at a constant frequency, $f = 223.464\,{\rm MHz}$ which corresponds to the resonance frequency at $V_{\rm BG} = 5.4\,{\rm V}$. Figures 6.5(a) and (b) show the DC QD current, $I_{\rm QD}$, and the amplitude of Γ, $|\Gamma|$, as a function of $V_{\rm BG}$. Hereafter, the amplitude and the phase of Γ as a function of a gate voltage are corrected in a similar manner described above by taking into account the external components. The QD device can also have par-

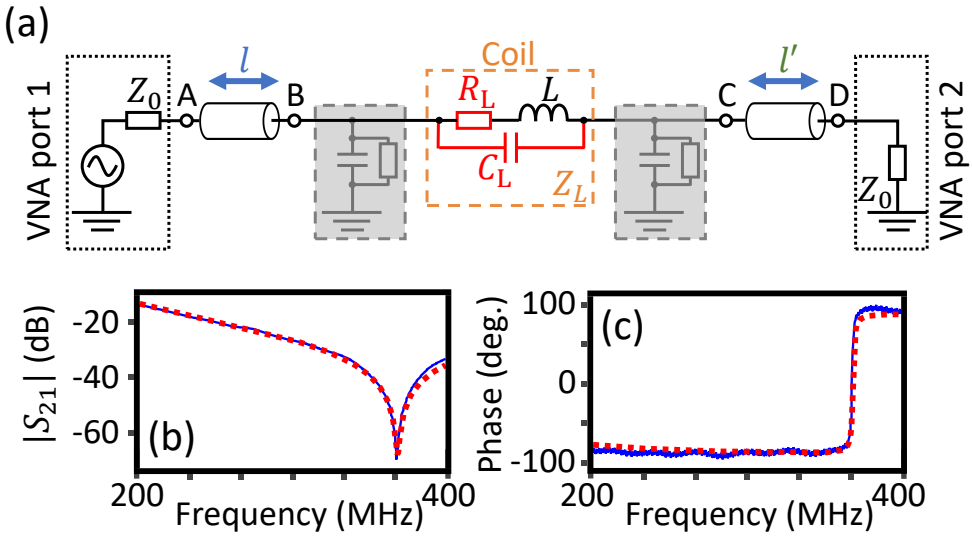


Figure 6.4: (a) An equivalent circuit for transmission measurement of an inductor at helium liquid temperature. Parasitic components in the PCB are ignored because of their large impedance compared to characteristic impedance $Z_0 = 50\,\Omega$. Transmission through the inductor with $L = 680\,\mathrm{nH}$ was measured using vector network analyzer. (b,c) Amplitude and phase of the transmission through the inductor as a function of carrier frequency. Measurement results (blue solid lines) are fitted with an equation from the equivalent circuit model (red dotted lines).

asitic components such as gate capacitance, C_{2D}, and its dielectric loss, G_{2D}. We derive the device admittance, $Y_{dev} = G_{dev} + i\omega C_{dev}$, where $G_{dev} = G_{QD} + G_{2D}$ and $C_{dev} = C_{QD} + C_{2D}$, from the V_{BG} dependence by subtracting impedances of inductance and parasitic capacitance together with their additional parasitic components (Figs. 6.5(c) and (d)). As seen in Fig. 6.5(c), C_{dev} qualitatively agrees with a result in standard CV measurements of MOS capacitors,[104] which is reasonable because the only difference is the direction of signal: from gate to semiconductor (CV measurement of MOS capacitors) or from semiconductor to gate (RF reflectometry of QDs). The peak in G_{dev} around $V_{BG} = 2.5\,\mathrm{V}$ is also similar to the one for CV measurements which can be explained by the effect of dielectric loss related to oxide (Fig. 6.5(d)).[111–113] In addition to being useful for establishing a detailed device model, understanding this in-situ tunability can potentially provide an on-chip implementation of gate-tunable reflectometry circuits previously achieved via external

components such as varactors.[114–116] At higher voltages, oscillations appear in $|\Gamma|$, corresponding to Coulomb peaks in I_{QD}, which implies the successful realization of RF-SET.

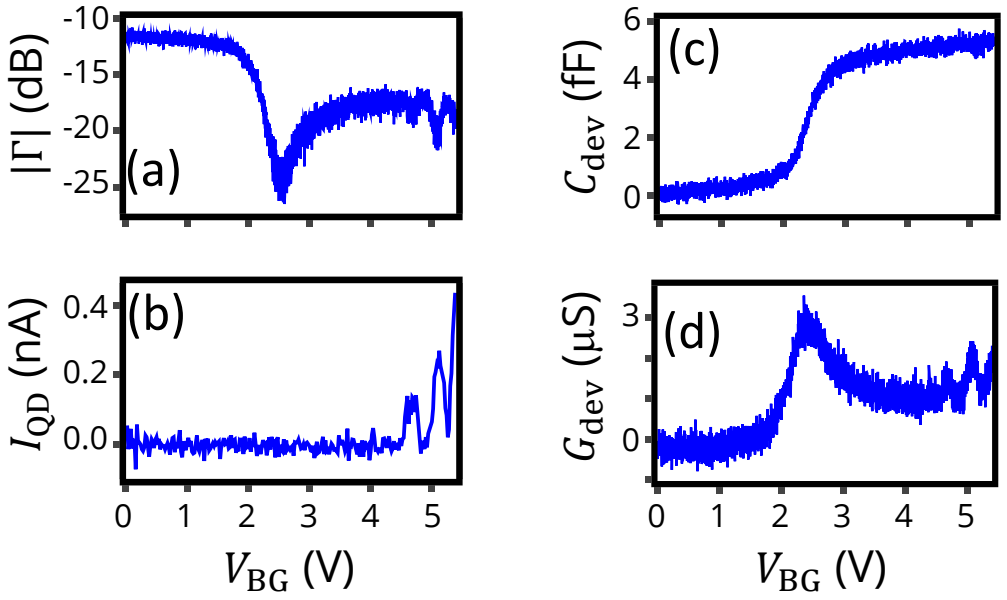


Figure 6.5: (a,b) Amplitude of the reflection coefficient, $|\Gamma|$, and QD current, I_{QD}, as a function of V_{BG} at liquid helium temperature. Carrier frequency $f = 223.464\,\mathrm{MHz}$, $V_{\mathrm{DS}} = 5\,\mathrm{mV}$. V_{GL1}, V_{GL2}, and V_{GR1} are floating. As V_{BG} is increased, a large dip appears in $|\Gamma|$ around $V_{\mathrm{BG}} = 2.5\,\mathrm{V}$, implying electron accumulation in the reservoir. At V_{BG} higher than 4 V, several small dips appear in the amplitude, corresponding to Coulomb peaks seen in (b). (c,d) Extracted device capacitance C_{dev} and conductance G_{dev} as a function of V_{BG}. These are obtained by subtracting the inductor and capacitance impedances with parasitic components from the measured load impedance.

6.7 Side gate voltage sweeping

We can expect the conductance sensitivity to further increase, when a SG voltage is swept instead of a back gate to suppress these changes in the device admittance related to the turn-on process. To perform such an experiment, we use another QD device with a nominally identical design and set the charge sensor and one of the side gates to be floating to avoid unintended RF paths. The measured RF reflectometry

signals as a function of a SG voltage, V_{GR1} are shown in Figs. 6.6(a) and (b). We find that peaks (dips) in amplitude (phase) of Γ nicely reproduce the Coulomb peaks of I_{QD} in Fig. 6.6(c). Strikingly, the observed phase shift ($\sim 45\,\mathrm{deg.}$) is significantly larger than those observed in other RF-SETs.[117, 105]

To understand the origin of the large phase shifts, we simulate the V_{GR1} dependence of the reflected signal. In Fig. 6.6(d), the simulation results are plotted in a Smith chart (orange dotted circle and purple dashed circles) together with the V_{GR1} dependence (blue solid line). For the one shown by the purple dashed circle, G_{QD} is set to be higher than for the other one represented by the orange dotted circle by $3.7\,\mu\mathrm{S}$, in order to approximately simulate the Coulomb peak conductance, with the other parameters obtained by fitting the frequency dependence. Both simulation results show constant resistance circles as expected from the equivalent circuit in Fig. 6.3(c). Remarkably, the orange one passes through almost the center of the Smith chart, meaning that the load impedance at resonance is closely matched to Z_0. The results at given frequencies are indicated by the red triangles (223.464 MHz) and the green dots (224.157 MHz) in the Smith chart: the red ones are for the frequency used in the measurement (223.464 MHz) and the green ones for the resonance frequency for the orange circle condition (224.157 MHz). As expected, the red triangles agree with the V_{GR1} dependence experimentally observed. We also calculate the frequency dependence of the phase difference $\Delta\varphi$ expected for the same ($3.7\,\mu\mathrm{S}$) conductance change in Fig. 6.6(e), with a red triangle and a green dot highlighting the same two frequencies as in Fig. 6.6(d). It turns out that there are two maximums in the absolute value of $\Delta\varphi$. We note that the resonance frequency (marked by the green dot) is located in between the two maximum points and has a small phase shift ($\sim 2\,\mathrm{deg.}$). On the other hand, the frequency used in the measurement (the red triangle) is located close to one of the maximums, and the large phase shift ($\sim 45\,\mathrm{deg.}$) agrees excellently with data. This large phase shift will not occur if the load impedance at resonance is away from impedance match-

ing, where larger or smaller constant resistance circles would appear. Therefore, we conclude that a good impedance matching and a small frequency detuning from the resonance frequency are the necessary ingredients for the large phase shift caused by Coulomb oscillations. We note that this large phase shift is caused by a conductance change, rather than a change in quantum or tunnel capacitances, for which much smaller phase shifts are typically reported (e.g. Refs. 117 and 105). Observation of reflectometry phase shift due to a conductance change is scarce. However, in theory, the phase change can be as large as 180 degree when the system passes exactly across the matching condition. To the best of our knowledge, our result is one of the closest to this ideal situation in the literature.

6.8 Summary

RF reflectometry is a promising method for fast spin readouts. Understanding of RF-reflectometry circuits is important to adopt this technique to various nanostructures. In this chapter, we have performed RF-SET using PD-QDs without the top gate structure, and, based on an equivalent circuit for load impedance, the parasitic circuit parameters are estimated from the frequency dependence of RF reflection coefficient. Our method will be useful when one needs to modify the RF reflectometry technique to apply to new device structures. Furthermore, we find huge phase shifts corresponding to Coulomb peaks ($\sim 45\,\mathrm{deg.}$), as a result of the combination of a good impedance matching and a detuning from resonance frequency. The large signals will be useful to charge sensing by combining them with a cryogenic amplifier and/or a strong CS-QD coupling. Assuming a strong CS-QD coupling such that a charge transition in the target QD causes a shift of a CS Coulomb peak by a half width of the peak, a 100-kHz spin readout will be possible as expected from the phase response in Fig. 6.6(b). The large phase shifts are confirmed by simulation using the equivalent circuit model. We believe that our results will be helpful in designing reflectometry circuits through simulation in order to improve the sensitivity

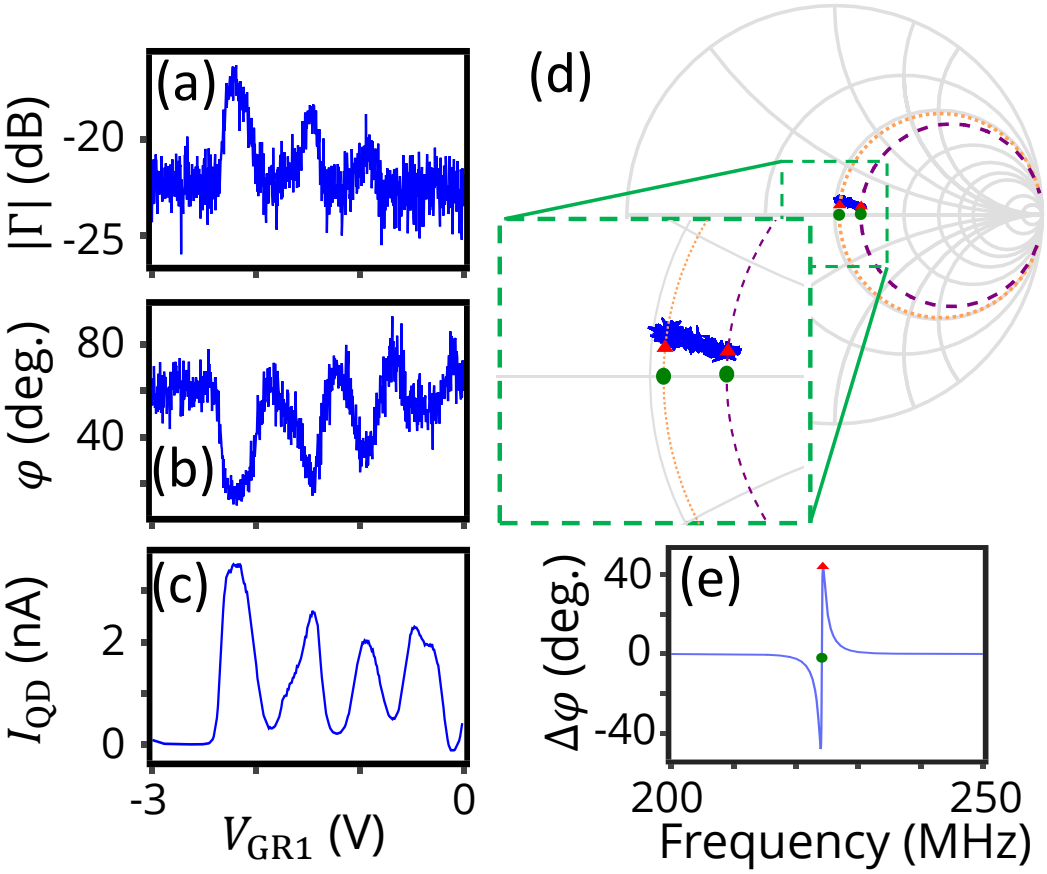


Figure 6.6: (a-c) Amplitude and phase of $\Gamma = |\Gamma|e^{i\varphi}$, and I_{QD} as a function of SG voltage, V_{GR1}, at liquid helium temperature. $V_{BG} = 6\,\mathrm{V}$, $V_{DS} = 1\,\mathrm{mV}$, $V_{GL1} = V_{GL2} = 0\,\mathrm{V}$, and $f = 224.3\,\mathrm{MHz}$. IF bandwidth is 100 kHz. (d) Smith chart for the Γ dependence together with frequency dependences of simulated reflection coefficient using the equivalent circuit in Fig. 6.3(c) (orange dotted circle and purple dashed circle). For the simulations, $L = 680\,\mathrm{nH}$, $\rho_L = 190\mu\Omega/\sqrt{\mathrm{rad/s}}$, $C_L = 350\,\mathrm{fF}$, $C_p + C_{dev} = 391\,\mathrm{fF}$, and $\tan\delta = 0.00614$. G_{dev} is set to be $4.73\,\mu\mathrm{S}$ for the orange circle and $8.43\,\mu\mathrm{S}$ for the purple circle. Red triangles (green dots) indicate Γ at $f = 223.464\,\mathrm{MHz}$ ($224.157\,\mathrm{MHz}$). Red triangles qualitatively reproduce the Γ change by Coulomb peaks. (e) Frequency dependence of phase difference between the two device conductance values, $\Delta\varphi$. A red triangle and a green dot correspond to the two frequency values used in (d).

and speed of spin qubit readout.

Chapter 7

Conclusions

7.1 Summary

In this PhD thesis, we have presented experimental research on LTQD and TTQD and development of charge sensing techniques. Integration of QDs is essential for large-scale spin qubit systems. A TTQD structure can be regarded as the minimum unit cell for dense two-dimensional integration.[118] In the first part of this thesis, we focused on the fabrication of TQDs. Although the basic techniques had already been developed previously, it was still necessary to optimize quantum dot designs. We developed designs for linear and triangular TQDs by repeating EBL test and SEM observation for different patterns. Especially, the hole at the center of TTQD is difficult to make and therefore, the realization of working devices took time. The potential barrier of the center hole may be a difficult part of device fabrication also in other QD systems, and that is possibly why only a few studies for TTQDs have been reported. Our fabricated devices were evaluated from currents through them and charge sensors at helium temperature. Both structures are confirmed to have three quantum dots as expected. In addition, tunnel couplings in the TTQD structure were successfully confirmed from two- and three-QD transports. We demonstrated that the sharp quantum confinement by physical etching, which

is difficult for gate-defined devices because of QD confinements by electric fields, may be the key ingredient in expanded two-dimensional QD array.

Charge sensing is also essential part of spin qubit systems. Spin states can be read out by charge sensors via spin-to-charge conversion techniques. To achieve qubit readout within a coherence time, a fast charge readout in single-shot manner is desired. We tried the single-shot charge sensing with TTQD structure. Unlike charge sensing with DC current, the single-shot measurements requires a large enough bandwidth to pass fast signals and also high-frequency noises inevitably. The simple way to remove noise with wide bandwidth is to remove the origin of noise. To do this, we mainly worked on breaking ground loops, one main source of noise, by trying cutting ground connection point by point. Moreover, we also made significant efforts to make programs to control measurement equipment such as arbitrary waveform generator and oscilloscope. In the measurements, we repeatedly applied voltage pulse sequences to a gate such that only a single electron tunnels out of the target QD in each sequence. In the result, we observed step signals in CS current corresponding to the tunnel events; however, the SNR was too low to detect the step by simply thresholding. We then applied a statistics theory using LLR and confirmed the capability of detecting the step position, or in other words, precise charge sensing. This work demonstrated the importance of numerical treatments for quantum information field.

In order to reduce noise, we also attempted a homodyne measurement technique called RF reflectometry, which utilizes RF signal ($\sim 200\,\mathrm{MHz}$) to avoid low-frequency noise like $1/f$ noise. The RF-SET results of this thesis are the first successful observations of RF reflectometry in PD-QD devices after years of development in our group. While the exact mechanism remains unknown, this may be attributed to top gate structure which can make RC low-pass filter for the channel of SOI layer. Based on this idea, we tried PD-QDs without top gate structures and confirmed that it worked out expectedly. In the measurements reflected RF

signals were monitored as functions of gate voltages, and it was confirmed that peak-like conductance characteristics of QDs were reflected in the RF signals. The signals showed large phase shifts, reproduced by simulation with equivalent circuit including parasitic components. We believe that the analysis is useful for design of reflectometry circuits.

These readout techniques, numerical treatment and RF reflectometry, can be combined to further improve the charge sensing. In addition, the SNR for RF reflectometry whose can be easily improved by a factor of 6 by using cryogenic amplifier. A tunnel coupling between a CS and its target QD will also improve the SNR. We anticipate that careful device designs and optimized setups enable spin readout even for a dense QD structures like TTQDs.

7.2 Perspective

Before we conclude, we would like to discuss the possible prospects of my research work. This work showed a unit structure for dense two-dimensional QD array as described in Ch. 4, whose structure is expandable to a rectangle QD array. The rectangle array is suitable to the well-known fault-tolerant scheme,[2] possibly with a dynamic random-access memory (DRAM) architecture.[28] In another scenario, the TTQD structure can be directly expanded because the TTQD lattice may be more powerful as a two-dimensional array unit than rectangle QD arrangement. For example, the TTQD structure can be a unit for another fault-tolerant scheme possibly facilitating decoherence error thresholds.[118] In any case, QD structure itself can easily be expanded even though the in-plane gate structures have to be replaced with out-of-plane ones by three-dimensional wiring. Figure 7.1 shows an example of such a structure. There is a two-dimensional QD array with two types of out-of-plane gates which control QD potentials and QD-QD tunnel couplings, respectively. By applying microwave and RF signals to the former gates, it is possible to control single-qubit states and read out the qubits, respectively. The digital

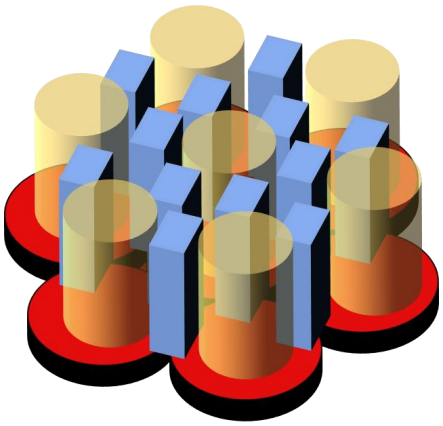


Figure 7.1: A two-dimensional QD array based on TTQD structure with out-of-plane gates. Yellow cylinders correspond to gates to control each qubit potential, and blue prisms correspond to gates to control two-qubit couplings.

signal processing technique in Ch. 5 and the equivalent circuit analysis described in Ch. 6 will be useful to make the gate-based readout highly sensitive to qubit states. The other type of gates is used for two-qubit gates by tuning tunnel couplings. We confirmed the existence of tunneling couplings in our two-dimensional QD array as explained in Ch. 4, which are partly defined by physical confinements. The combination of such physical confinements and out-of-plane gates may lead to a good ON/OFF ratio in the couplings. Recently, Hughes Research Laboratories group, in USA, has fabricated silicon spin qubits by using standard CMOS fabrication techniques, where out-of-plane gate structures are formed.[119] This structure may be further extended by stacking multi-layers to fan out gates.

Another possibility is replacement of silicon with other materials where the effective mass of charges are lower than ones in silicon, which facilitates qubit integration. Germanium which comprises 92.3 % spinless isotopes is one of such materials where holes in germanium has lighter effective mass than charges in silicon and also strong spin-orbit interaction useful for fast spin manipulation. In these days, it has been demonstrated that the advantages result in single-qubit operations[100] and fast two-qubit operations with high fidelity.[120] Recently, a four-qubit system in germanium QDs was reported.[121] The fast progress in germanium spin qubit lets us envision realization of large-scaled spin qubit system in the near future.

Turning to the charge sensing techniques in this thesis, we believe that they works irrespectively of device structure. The LLR may be useful for fast measurement with wide bandwidth where signal-to-noise ratio becomes lower. The LLR enables precise step detection but takes wait time until a set of data points is acquired as well as calculation time. Segmentation of measurement data points can make the technique more "real-time" at the expense of detection preciseness. In another way, field-programmable gate array (FPGA) can enable fast calculation, benefiting from its real-time and parallel processing. By FPGA, the LLR technique may even be performed within several clocks corresponding to several tens of nanoseconds with 100 MHz clock. The calculation time is ignorable compared to the single measurement time (40 ms), so that the combination of FPGA and the segmentation may realize a "real-time" detection.

The findings from the RF reflectometry results can be applicable to other systems. In the results, we have considered a parasitic capacitance of the inductor in the RF reflectometry circuit. The capacitance is typically neglected in previous reflectometry studies but can significantly modify the effective inductance due to its self-resonance effect. We have also confirmed that RF leakage from one electrode to the other affects the sensitivity of RF signal. Removing top gate structure leads to successful RF reflectometry, and further improvement will be possible. As mentioned in Ch. 6, a CS and a side gate adjacent to QD have been set to be floating because of RF leakages, indicating capacitive couplings of the electrodes to the RF channel. Suppression of the couplings may enable further large signal in RF reflectometry.[122] Actually, by increasing the gap between electrodes, charge sensing by an RF-SET with PD-QD structure has been performed. In addition, these PD-QDs have TGs with reduced areas, therefore enabling RF reflectometry with a good controllability as before.

In closing, we conclude this PhD work. In this work, we realized a two-dimensional QD array expandable to the one like the integrated QD structure in

Fig. 7.1 (red circles) and also developed readout techniques which can be applied to gate sensing, for example, using local gates in Fig. 7.1. Expansion of the TTQD structure to a large two-dimensional QD array is promising for quantum information processing. Aiming toward this, a lot of improvements are required. We are now in the first step toward quantum computer based on PD-QDs. In this thesis, we developed readout techniques for an expandable qubit system. The techniques are from software and hardware aspects and therefore, complementary to each other, hopefully enabling fast spin readout by combination with spin-to-charge conversion. In another study, spin operation in a p-type PD-QD succeeded. Merging these techniques to establish a spin qubit is the short-term next step for PD-QD based qubits.

References

[1] D. Deutsch. Quantum theory, the church–turing principle and the universal quantum computer. *Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, **400** 97, 1985.

[2] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland. Surface codes: Towards practical large-scale quantum computation. *Phys. Rev. A*, **86** 032324, 2012.

[3] E. Knill, R. Laflamme, and G. J. Milburn. A scheme for efficient quantum computation with linear optics. *Nature*, **409** 46, 2001.

[4] Y. Nakamura, Y. A. Pashkin, and J. S. Tsai. Coherent control of macroscopic quantum states in a single-cooper-pair box. *Nature*, **398** 786, 1999.

[5] D. Loss and D. P. DiVincenzo. Quantum computation with quantum dots. *Phys. Rev. A*, **57** 120, 1998.

[6] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. S. L. Brandao, D. A. Buell, B. Burkett, Y. Chen, Z. Chen, B. Chiaro, R. Collins, W. Courtney, A. Dunsworth, E. Farhi, B. Foxen, A. Fowler, C. Gidney, M. Giustina, R. Graff, K. Guerin, S. Habegger, M. P. Harrigan, M. J. Hartmann, A. Ho, M. Hoffmann, T. Huang, T. S. Humble, S. V. Isakov, E. Jeffrey, Z. Jiang, D. Kafri, K. Kechedzhi, J. Kelly, P. V. Klimov, S. Knysh, A. Korotkov, F. Kostritsa, D. Landhuis, M. Lindmark,

E. Lucero, D. Lyakh, S. Mandrà, J. R. McClean, M. McEwen, A. Megrant, X. Mi, K. Michielsen, M. Mohseni, J. Mutus, O. Naaman, M. Neeley, C. Neill, M. Y. Niu, E. Ostby, A. Petukhov, J. C. Platt, C. Quintana, E. G. Rieffel, P. Roushan, N. C. Rubin, D. Sank, K. J. Satzinger, V. Smelyanskiy, K. J. Sung, M. D. Trevithick, A. Vainsencher, B. Villalonga, T. White, Z. J. Yao, P. Yeh, A. Zalcman, H. Neven, and J. M. Martinis. Quantum supremacy using a programmable superconducting processor. *Nature*, **574** 505, 2019.

[7] N. Friis, O. Marty, C. Maier, C. Hempel, M. Holzäpfel, P. Jurcevic, M. B. Plenio, M. Huber, C. Roos, R. Blatt, and B. Lanyon. Observation of entangled states of a fully controlled 20-qubit system. *Phys. Rev. X*, **8** 021012, 2018.

[8] K. C. Nowack, F. H. L. Koppens, Y. V. Nazarov, and L. M. K. Vandersypen. Coherent control of a single electron spin with electric fields. *Science*, **318** 1430, 2007.

[9] M. Pioro-Ladrière, T. Obata, Y. Tokura, Y.-S. Shin, T. Kubo, K. Yoshida, T. Taniyama, and S. Tarucha. Electrically driven single-electron spin resonance in a slanting zeeman field. *Nature Physics*, **4** 776, 2008.

[10] B. M. Maune, M. G. Borselli, B. Huang, T. D. Ladd, P. W. Deelman, K. S. Holabird, A. A. Kiselev, I. Alvarado-Rodriguez, R. S. Ross, A. E. Schmitz, M. Sokolich, C. A. Watson, M. F. Gyure, and A. T. Hunter. Coherent singlet-triplet oscillations in a silicon-based double quantum dot. *Nature*, **481** 344, 2012.

[11] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh, and S. Tarucha. A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%. *Nature Nanotechnology*, **13** 102, 2018.

[12] C. H. Yang, K. W. Chan, R. Harper, W. Huang, T. Evans, J. C. C. Hwang, B. Hensen, A. Laucht, T. Tanttu, F. E. Hudson, S. T. Flammia, K. M. Itoh, A. Morello, S. D. Bartlett, and A. S. Dzurak. Silicon qubit fidelities approaching incoherent noise limits via pulse engineering. *Nature Electronics*, **2** 151, 2019.

[13] D. M. Zajac, T. M. Hazard, X. Mi, E. Nielsen, and J. R. Petta. Scalable gate architecture for a one-dimensional array of semiconductor spin qubits. *Phys. Rev. Applied*, **6** 054013, 2016.

[14] K. Takeda, A. Noiri, T. Nakajima, J. Yoneda, T. Kobayashi, and S. Tarucha. Quantum tomography of an entangled three-qubit state in silicon. *Nature Nanotechnology*, **16** 965, 2021.

[15] F. Ansaloni, A. Chatterjee, H. Bohuslavskyi, B. Bertrand, L. Hutin, M. Vinet, and F. Kuemmeth. Single-electron operations in a foundry-fabricated array of quantum dots. *Nature Communications*, **11** 6399, 2020.

[16] A. Zwerver, T. Krähenmann, T. Watson, L. Lampert, H. George, R. Pillarisetty, S. Bojarski, P. Amin, S. Amitonov, J. Boter, *et al.* Qubits made by advanced semiconductor manufacturing. *arXiv preprint arXiv:2101.12650*, 2021.

[17] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann. A spin qubit in a fin field-effect transistor. *arXiv preprint arXiv:2103.07369*, 2021.

[18] J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven. Single-shot read-out of an individual electron spin in a quantum dot. *Nature*, **430** 431, 2004.

[19] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha. Current rectification by pauli exclusion in a weakly coupled double quantum dot system. *Science*, **297** 1313, 2002.

[20] S. Aminikhanghahi and D. J. Cook. A survey of methods for time series change point detection. *Knowledge and Information Systems*, **51** 339, 2017.

[21] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober. The radio-frequency single-electron transistor (rf-set): A fast and ultrasensitive electrometer. *Science*, **280** 1238, 1998.

[22] D. P. DiVincenzo, D. Bacon, J. Kempe, G. Burkard, and K. B. Whaley. Universal quantum computation with the exchange interaction. *Nature*, **408** 339, 2000.

[23] N. Lee, R. Tsuchiya, G. Shinkai, Y. Kanno, T. Mine, T. Takahama, R. Mizokuchi, T. Kodera, D. Hisamoto, and H. Mizuno. Enhancing electrostatic coupling in silicon quantum dot array by dual gate oxide thickness for large-scale integration. *Applied Physics Letters*, **116** 162106, 2020.

[24] J. Preskill. Quantum Computing in the NISQ era and beyond. *Quantum*, **2** 79, 2018.

[25] M. F. Gonzalez-Zalba, S. Barraud, A. J. Ferguson, and A. C. Betz. Probing the limits of gate-based charge sensing. *Nature Communications*, **6** 6084, 2015.

[26] G. Zheng, N. Samkharadze, M. L. Noordam, N. Kalhor, D. Brousse, A. Sammak, G. Scappucci, and L. M. K. Vandersypen. Rapid gate-based spin read-out in silicon using an on-chip resonator. *Nature Nanotechnology*, **14** 742, 2019.

[27] D. J. Ibberson, T. Lundberg, J. A. Haigh, L. Hutin, B. Bertrand, S. Barraud, C.-M. Lee, N. A. Stelmashenko, G. A. Oakes, L. Cochrane, J. W. Robinson,

M. Vinet, M. F. Gonzalez-Zalba, and L. A. Ibberson. Large dispersive interaction between a cmos double quantum dot and microwave photons. *PRX Quantum*, **2** 020315, 2021.

[28] S. Schaal, A. Rossi, V. N. Ciriano-Tejel, T.-Y. Yang, S. Barraud, J. J. L. Morton, and M. F. Gonzalez-Zalba. A cmos dynamic random access architecture for radio-frequency readout of quantum devices. *Nature Electronics*, **2** 236, 2019.

[29] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst. Interfacing spin qubits in quantum dots and donors–hot, dense, and coherent. *npj Quantum Information*, **3** 34, 2017.

[30] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak. Silicon cmos architecture for a spin-based quantum computer. *Nature Communications*, **8** 1766, 2017.

[31] X. Xue, B. Patra, J. P. G. van Dijk, N. Samkharadze, S. Subramanian, A. Corna, B. Paquelet Wuetz, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, H. Rampurawala, B. Carlton, S. Ravikumar, C. Nieva, S. Kim, H.-J. Lee, A. Sammak, G. Scappucci, M. Veldhorst, F. Sebastiano, M. Babaie, S. Pellerano, E. Charbon, and L. M. K. Vandersypen. Cmos-based cryogenic control of silicon quantum circuits. *Nature*, **593** 205, 2021.

[32] L. Petit, H. G. J. Eenink, M. Russ, W. I. L. Lawrie, N. W. Hendrickx, S. G. J. Philips, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst. Universal quantum logic in hot silicon qubits. *Nature*, **580** 355, 2020.

[33] C. H. Yang, R. C. C. Leon, J. C. C. Hwang, A. Saraiva, T. Tanttu, W. Huang, J. Camirand Lemyre, K. W. Chan, K. Y. Tan, F. E. Hudson, K. M. Itoh,

A. Morello, M. Pioro-Ladrière, A. Laucht, and A. S. Dzurak. Operation of a silicon quantum processor unit cell above one kelvin. *Nature*, **580** 350, 2020.

[34] K. Takeda, J. Kamioka, T. Otsuka, J. Yoneda, T. Nakajima, M. R. Delbecq, S. Amaha, G. Allison, T. Kodera, S. Oda, and S. Tarucha. A fault-tolerant addressable spin qubit in a natural silicon quantum dot. *Science Advances*, **2**, 2016.

[35] J. Yoneda, K. Takeda, A. Noiri, T. Nakajima, S. Li, J. Kamioka, T. Kodera, and S. Tarucha. Quantum non-demolition readout of an electron spin in silicon. *Nature Communications*, **11** 1144, 2020.

[36] X. Xue, B. D'Anjou, T. F. Watson, D. R. Ward, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, W. A. Coish, and L. M. K. Vandersypen. Repetitive quantum nondemolition measurement and soft decoding of a silicon spin qubit. *Phys. Rev. X*, **10** 021006, 2020.

[37] X. Mi, M. Benito, S. Putz, D. M. Zajac, J. M. Taylor, G. Burkard, and J. R. Petta. A coherent spin–photon interface in silicon. *Nature*, **555** 599, 2018.

[38] N. Samkharadze, G. Zheng, N. Kalhor, D. Brousse, A. Sammak, U. C. Mendes, A. Blais, G. Scappucci, and L. M. K. Vandersypen. Strong spin-photon coupling in silicon. *Science*, **359** 1123, 2018.

[39] M. Veldhorst, C. H. Yang, J. C. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. A two-qubit logic gate in silicon. *Nature*, **526** 410, 2015.

[40] D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta. Resonantly driven cnot gate for electron spins. *Science*, **359** 439, 2018.

[41] T. F. Watson, S. G. J. Philips, E. Kawakami, D. R. Ward, P. Scarlino, M. Veldhorst, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. A programmable two-qubit quantum processor in silicon. *Nature*, **555** 633, 2018.

[42] W. Huang, C. H. Yang, K. W. Chan, T. Tanttu, B. Hensen, R. C. C. Leon, M. A. Fogarty, J. C. C. Hwang, F. E. Hudson, K. M. Itoh, A. Morello, A. Laucht, and A. S. Dzurak. Fidelity benchmarks for two-qubit gates in silicon. *Nature*, **569** 532, 2019.

[43] M. Tadokoro, T. Nakajima, T. Kobayashi, K. Takeda, A. Noiri, K. Tomari, J. Yoneda, S. Tarucha, and T. Kodera. Designs for a two-dimensional si quantum dot array with spin qubit addressability. *Scientific Reports*, **11** 19406, 2021.

[44] L. L. Guevel, G. Billiot, S. De Franceschi, A. Morel, X. Jehl, A. Jansen, and G. Pillonnet. Compact gate-based read-out of multiplexed quantum devices with a cryogenic cmos active inductor. *arXiv preprint arXiv:2102.04364*, 2021.

[45] G. Yamahata, T. Kodera, H. O. H. Churchill, K. Uchida, C. M. Marcus, and S. Oda. Magnetic field dependence of pauli spin blockade: A window into the sources of spin relaxation in silicon quantum dots. *Phys. Rev. B*, **86** 115322, 2012.

[46] T. Kambara, T. Kodera, Y. Arakawa, and S. Oda. Dual function of single electron transistor coupled with double quantum dot: Gating and charge sensing. *Japanese Journal of Applied Physics*, **52** 04CJ01, 2013.

[47] K. Horibe, T. Kodera, and S. Oda. Lithographically defined few-electron silicon quantum dots based on a silicon-on-insulator substrate. *Applied Physics Letters*, **106** 083111, 2015.

[48] Y. Yamaoka, K. Iwasaki, S. Oda, and T. Kodera. Charge sensing and spin-related transport property of p-channel silicon quantum dots. *Japanese Journal of Applied Physics*, **56** 04CK07, 2017.

[49] R. Mizokuchi, S. Oda, and T. Kodera. Physically defined triple quantum dot systems in silicon on insulator. *Applied Physics Letters*, **114** 073104, 2019.

[50] S. Hiraoka, K. Horibe, R. Ishihara, S. Oda, and T. Kodera. Physically defined silicon triple quantum dots charged with few electrons in metal-oxide-semiconductor structures. *Applied Physics Letters*, **117** 074001, 2020.

[51] M. Tadokoro, R. Mizokuchi, and T. Kodera. Pauli spin blockade in a silicon triangular triple quantum dot. *Japanese Journal of Applied Physics*, **59** SGGI01, 2020.

[52] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen. *Electron Transport in Quantum Dots*, pp. 105–214. Springer Netherlands, Dordrecht, 1997.

[53] R. Kotlyar and S. Das Sarma. Nonlinear transport through coupled double-quantum-dot systems. *Phys. Rev. B*, **56** 13235, 1997.

[54] B. Muralidharan and S. Datta. Generic model for current collapse in spin-blockaded transport. *Phys. Rev. B*, **76** 035432, 2007.

[55] D. V. Averin and Y. V. Nazarov. Virtual electron diffusion during quantum tunneling of the electric charge. *Phys. Rev. Lett.*, **65** 2446, 1990.

[56] A. Noiri, T. Takakura, T. Obata, T. Otsuka, T. Nakajima, J. Yoneda, and S. Tarucha. Cotunneling spin blockade observed in a three-terminal triple quantum dot. *Phys. Rev. B*, **96** 155414, 2017.

[57] D. Schröer, A. D. Greentree, L. Gaudreau, K. Eberl, L. C. L. Hollenberg, J. P. Kotthaus, and S. Ludwig. Electrostatically defined serial triple quantum dot charged with few electrons. *Phys. Rev. B*, **76** 075306, 2007.

[58] J. M. Hornibrook, J. I. Colless, A. C. Mahoney, X. G. Croot, S. Blanvillain, H. Lu, A. C. Gossard, and D. J. Reilly. Frequency multiplexing for readout of spin qubits. *Applied Physics Letters*, **104** 103108, 2014.

[59] A. Noiri, K. Takeda, J. Yoneda, T. Nakajima, T. Kodera, and S. Tarucha. Radio-frequency-detected fast charge sensing in undoped silicon quantum dots. *Nano Letters*, **20** 947, 2020.

[60] S. Ihara, A. Andreev, D. A. Williams, T. Kodera, and S. Oda. Quantum dots in single electron transistors with ultrathin silicon-on-insulator structures. *Applied Physics Letters*, **107** 013102, 2015.

[61] K. Eng, T. D. Ladd, A. Smith, M. G. Borselli, A. A. Kiselev, B. H. Fong, K. S. Holabird, T. M. Hazard, B. Huang, P. W. Deelman, I. Milosavljevic, A. E. Schmitz, R. S. Ross, M. F. Gyure, and A. T. Hunter. Isotopically enhanced triple-quantum-dot qubit. *Science Advances*, **1**, 2015.

[62] L. Balents. Spin liquids in frustrated magnets. *Nature*, **464** 199, 2010.

[63] M. Seo, H. K. Choi, S.-Y. Lee, N. Kim, Y. Chung, H.-S. Sim, V. Umansky, and D. Mahalu. Charge frustration in a triangular triple quantum dot. *Phys. Rev. Lett.*, **110** 046803, 2013.

[64] V. W. Scarola, K. Park, and S. D. Sarma. Chirality in quantum computation with spin cluster qubits. *Phys. Rev. Lett.*, **93** 120503, 2004.

[65] C.-Y. Hsieh and P. Hawrylak. Quantum circuits based on coded qubits encoded in chirality of electron spin complexes in triple quantum dots. *Phys. Rev. B*, **82** 205311, 2010.

[66] F. Troiani, D. Stepanenko, and D. Loss. Hyperfine-induced decoherence in triangular spin-cluster qubits. *Phys. Rev. B*, **86** 161409, 2012.

[67] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, and G. L. Snider. Digital logic gate using quantum-dot cellular automata. *Science*, **284** 289, 1999.

[68] L. Gaudreau, S. A. Studenikin, A. S. Sachrajda, P. Zawadzki, A. Kam, J. Lapointe, M. Korkusinski, and P. Hawrylak. Stability diagram of a few-electron triple dot. *Phys. Rev. Lett.*, **97** 036807, 2006.

[69] F. Delgado, Y.-P. Shim, M. Korkusinski, L. Gaudreau, S. A. Studenikin, A. S. Sachrajda, and P. Hawrylak. Spin-selective aharonov-bohm oscillations in a lateral triple quantum dot. *Phys. Rev. Lett.*, **101** 226810, 2008.

[70] M. Busl, R. Sánchez, and G. Platero. Control of spin blockade by ac magnetic fields in triple quantum dots. *Phys. Rev. B*, **81** 121306, 2010.

[71] A. Noiri, K. Kawasaki, T. Otsuka, T. Nakajima, J. Yoneda, S. Amaha, M. R. Delbecq, K. Takeda, G. Allison, A. Ludwig, A. D. Wieck, and S. Tarucha. A triangular triple quantum dot with tunable tunnel couplings. *Semiconductor Science and Technology*, **32** 084004, 2017.

[72] R. Thalineau, S. Hermelin, A. D. Wieck, C. Bäerle, L. Saminadayar, and T. Meunier. A few-electron quadruple quantum dot in a closed loop. *Applied Physics Letters*, **101** 103102, 2012.

[73] A. C. Betz, M. L. V. Tagliaferri, M. Vinet, M. Broström, M. Sanquer, A. J. Ferguson, and M. F. Gonzalez-Zalba. Reconfigurable quadruple quantum dots in a silicon nanowire transistor. *Applied Physics Letters*, **108** 203108, 2016.

[74] H. Flentje, P.-A. Mortemousque, R. Thalineau, A. Ludwig, A. D. Wieck, C. Bäuerle, and T. Meunier. Coherent long-distance displacement of individual electron spins. *Nature Communications*, **8** 501, 2017.

[75] P.-A. Mortemousque, E. Chanrion, B. Jadot, H. Flentje, A. Ludwig, A. D. Wieck, M. Urdampilleta, C. Bauerle, and T. Meunier. Coherent control of individual electron spins in a two dimensional array of quantum dots. *arXiv preprint arXiv:1808.06180*, 2018.

[76] U. Mukhopadhyay, J. P. Dehollain, C. Reichl, W. Wegscheider, and L. M. K. Vandersypen. A 2×2 quantum dot array with controllable inter-dot tunnel couplings. *Applied Physics Letters*, **112** 183505, 2018.

[77] A. Vidan, R. M. Westervelt, M. Stopa, M. Hanson, and A. C. Gossard. Charging and spin effects in triple dot artificial molecules. *Journal of Superconductivity*, **18** 223, 2005.

[78] J. M. Elzerman, R. Hanson, J. S. Greidanus, L. H. Willems van Beveren, S. De Franceschi, L. M. K. Vandersypen, S. Tarucha, and L. P. Kouwenhoven. Few-electron quantum dot circuit with integrated charge read out. *Phys. Rev. B*, **67** 161308, 2003.

[79] D. Averin and Y. V. Nazarov. Macroscopic quantum tunneling of charge and co-tunneling. In *Single Charge Tunneling*, pp. 217–247. Springer, 1992.

[80] S. De Franceschi, S. Sasaki, J. M. Elzerman, W. G. van der Wiel, S. Tarucha, and L. P. Kouwenhoven. Electron cotunneling in a semiconductor quantum dot. *Phys. Rev. Lett.*, **86** 878, 2001.

[81] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven. Electron transport through double quantum dots. *Rev. Mod. Phys.*, **75** 1, 2002.

[82] L. Gaudreau, A. Kam, G. Granger, S. A. Studenikin, P. Zawadzki, and A. S. Sachrajda. A tunable few electron triple quantum dot. *Applied Physics Letters*, **95** 193101, 2009.

[83] G. Yamahata, Y. Tsuchiya, H. Mizuta, K. Uchida, and S. Oda. Electron transport through silicon serial triple quantum dots. *Solid-State Electronics*, **53** 779 , 2009.

[84] R. Mizokuchi, M. Tadokoro, and T. Kodera. Detection of tunneling events in physically defined silicon quantum dot using single-shot measurements improved by numerical treatments. *Applied Physics Express*, **13** 121004, 2020.

[85] J. Canny. A computational approach to edge detection. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, **PAMI-8** 679, 1986.

[86] J. R. Prance, B. J. V. Bael, C. B. Simmons, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, and M. A. Eriksson. Identifying single electron charge sensor events using wavelet edge detection. *Nanotechnology*, **26** 215201, 2015.

[87] C. B. Simmons, J. R. Prance, B. J. Van Bael, T. S. Koh, Z. Shi, D. E. Savage, M. G. Lagally, R. Joynt, M. Friesen, S. N. Coppersmith, and M. A. Eriksson. Tunable spin loading and T_1 of a silicon spin qubit measured by single-shot readout. *Phys. Rev. Lett.*, **106** 156804, 2011.

[88] C. Volk, A. Chatterjee, F. Ansaloni, C. M. Marcus, and F. Kuemmeth. Fast charge sensing of si/sige quantum dots via a high-frequency accumulation gate. *Nano Letters*, **19** 5628, 2019.

[89] E. S. Page. Continuous inspection schemes. *Biometrika*, **41** 100, 1954.

[90] B. D'Anjou and W. A. Coish. Optimal post-processing for a generic single-shot qubit readout. *Phys. Rev. A*, **89** 012313, 2014.

[91] B. D'Anjou, L. Kuret, L. Childress, and W. A. Coish. Maximal adaptive-decision speedups in quantum-state readout. *Phys. Rev. X*, **6** 011017, 2016.

[92] J. Zhang, L. Xu, T. Shi, G. Bian, P. Fan, M. Li, P. Chen, C. Xu, N. Zhang, and H. Yuan. An improved spin readout for nitrogen vacancy center ensemble based on a maximum likelihood estimation method. *Journal of Physics D: Applied Physics*, **53** 455305, 2020.

[93] A. Sen and M. S. Srivastava. On tests for detecting change in mean. *The Annals of statistics*, **3** 98, 1975.

[94] A. B. Olshen, E. S. Venkatraman, R. Lucito, and M. Wigler. Circular binary segmentation for the analysis of array-based DNA copy number data. *Biostatistics*, **5** 557, 2004.

[95] W. Lu, Z. Ji, L. Pfeiffer, K. W. West, and A. J. Rimberg. Real-time detection of electron tunnelling in a quantum dot. *Nature*, **423** 422, 2003.

[96] M. G. House, H. W. Jiang, and X. C. Zhang. Analysis of electron tunneling events with the hidden markov model. *Phys. Rev. B*, **80** 113308, 2009.

[97] J. Kamioka, T. Kodera, K. Takeda, T. Obata, S. Tarucha, and S. Oda. Charge noise analysis of metal oxide semiconductor dual-gate si/sige quantum point contacts. *Journal of Applied Physics*, **115** 203709, 2014.

[98] P. Harvey-Collard, B. D'Anjou, M. Rudolph, N. T. Jacobson, J. Dominguez, G. A. Ten Eyck, J. R. Wendt, T. Pluym, M. P. Lilly, W. A. Coish, M. Pioro-Ladrière, and M. S. Carroll. High-fidelity single-shot readout for a spin qubit via an enhanced latching mechanism. *Phys. Rev. X*, **8** 021046, 2018.

[99] M. Urdampilleta, D. J. Niegemann, E. Chanrion, B. Jadot, C. Spence, P.-A. Mortemousque, C. Bäuerle, L. Hutin, B. Bertrand, S. Barraud, R. Maurand, M. Sanquer, X. Jehl, S. De Franceschi, M. Vinet, and T. Meunier. Gate-based

high fidelity spin readout in a cmos device. *Nature Nanotechnology*, **14** 737, 2019.

[100] N. W. Hendrickx, W. I. L. Lawrie, L. Petit, A. Sammak, G. Scappucci, and M. Veldhorst. A single-hole spin qubit. *Nature Communications*, **11** 3478, 2020.

[101] A. Morello, J. J. Pla, F. A. Zwanenburg, K. W. Chan, K. Y. Tan, H. Huebl, M. Möttönen, C. D. Nugroho, C. Yang, J. A. van Donkelaar, A. D. C. Alves, D. N. Jamieson, C. C. Escott, L. C. L. Hollenberg, R. G. Clark, and A. S. Dzurak. Single-shot readout of an electron spin in silicon. *Nature*, **467** 687, 2010.

[102] R. Mizokuchi, S. Bugu, M. Hirayama, J. Yoneda, and T. Kodera. Radio-frequency single electron transistors in physically defined silicon quantum dots with a sensitive phase response. *Scientific Reports*, **11** 5863, 2021.

[103] E. J. Connors, J. Nelson, and J. M. Nichol. Rapid high-fidelity spin-state readout in Si/Si-Ge quantum dots via rf reflectometry. *Phys. Rev. Applied*, **13** 024019, 2020.

[104] S. J. Angus, A. J. Ferguson, A. S. Dzurak, and R. G. Clark. A silicon radio-frequency single electron transistor. *Applied Physics Letters*, **92** 112103, 2008.

[105] M. Jung, M. D. Schroer, K. D. Petersson, and J. R. Petta. Radio frequency charge sensing in inas nanowire double quantum dots. *Applied Physics Letters*, **100** 253508, 2012.

[106] D. Keith, M. G. House, M. B. Donnelly, T. F. Watson, B. Weber, and M. Y. Simmons. Single-shot spin readout in semiconductors near the shot-noise sensitivity limit. *Phys. Rev. X*, **9** 041003, 2019.

[107] L. J. Taskinen, R. P. Starrett, T. P. Martin, A. P. Micolich, A. R. Hamilton, M. Y. Simmons, D. A. Ritchie, and M. Pepper. Radio-frequency reflectometry on large gated two-dimensional systems. *Review of Scientific Instruments*, **79** 123901, 2008.

[108] S. Bugu, S. Nishiyama, K. Kato, Y. Liu, T. Mori, and T. Kodera. Rf reflectometry for readout of charge transition in a physically defined pmos silicon quantum dot. *arXiv preprint arXiv:2010.07566*, 2020.

[109] A. Rossi, T. Ferrus, and D. A. Williams. Electron temperature in electrically isolated si double quantum dots. *Applied Physics Letters*, **100** 133503, 2012.

[110] A. N. Pearson, K. E. Khosla, M. Mergenthaler, G. A. D. Briggs, E. A. Laird, and N. Ares. Radio-frequency optomechanical characterization of a silicon nitride drum. *Scientific Reports*, **10** 1654, 2020.

[111] T. P. Martin, A. Szorkovszky, A. P. Micolich, A. R. Hamilton, C. A. Marlow, H. Linke, R. P. Taylor, and L. Samuelson. Enhanced zeeman splitting in ga0.25in0.75as quantum point contacts. *Applied Physics Letters*, **93** 012105, 2008.

[112] W. Vandendaele, C. Malaquin, A. Ghorbel, M. Cassé, F. Allibert, and G. Reimbold. Novel cv/gv technique for top and bottom box interfaces traps density extraction on fdsoi wafers. In *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–3. 2017.

[113] H. J. Quah, Z. Hassan, and W. F. Lim. Passivation of silicon substrate using two-step grown ternary aluminium doped zirconium oxide. *Applied Surface Science*, **493** 411 , 2019.

[114] N. Ares, F. J. Schupp, A. Mavalankar, G. Rogers, J. Griffiths, G. A. C. Jones, I. Farrer, D. A. Ritchie, C. G. Smith, A. Cottet, G. A. D. Briggs, and E. A.

Laird. Sensitive radio-frequency measurements of a quantum dot by tuning to perfect impedance matching. *Phys. Rev. Applied*, **5** 034011, 2016.

[115] T. Müller, T. Choi, S. Hellmüller, K. Ensslin, T. Ihn, and S. Schön. A circuit analysis of an in situ tunable radio-frequency quantum point contact. *Review of Scientific Instruments*, **84** 083902, 2013.

[116] M. G. House, I. Bartlett, P. Pakkiam, M. Koch, E. Peretz, J. van der Heijden, T. Kobayashi, S. Rogge, and M. Y. Simmons. High-sensitivity charge detection with a single-lead quantum dot for scalable quantum computation. *Phys. Rev. Applied*, **6** 044016, 2016.

[117] S. J. Chorley, J. Wabnig, Z. V. Penfold-Fitch, K. D. Petersson, J. Frake, C. G. Smith, and M. R. Buitelaar. Measuring the complex admittance of a carbon nanotube double quantum dot. *Phys. Rev. Lett.*, **108** 036802, 2012.

[118] K. Fujii and Y. Tokunaga. Error and loss tolerances of surface codes with general lattice structures. *Phys. Rev. A*, **86** 020303, 2012.

[119] W. Ha, S. D. Ha, M. D. Choi, Y. Tang, A. E. Schmitz, M. P. Levendorf, K. Lee, J. M. Chappell, T. S. Adams, D. R. Hulbert, *et al.* A flexible design platform for si/sige exchange-only qubits with low disorder. *arXiv preprint arXiv:2107.10916*, 2021.

[120] N. W. Hendrickx, D. Franke, A. Sammak, G. Scappucci, and M. Veldhorst. Fast two-qubit logic with holes in germanium. *Nature*, **577** 487, 2020.

[121] N. Hendrickx, W. Lawrie, M. Russ, F. van Riggelen, S. de Snoo, R. Schouten, A. Sammak, G. Scappucci, and M. Veldhorst. A four-qubit germanium quantum processor. *arXiv preprint arXiv:2009.04268*, 2020.

[122] S. Blanvillain, J. I. Colless, D. J. Reilly, H. Lu, and A. C. Gossard. Suppressing on-chip electromagnetic crosstalk for spin qubit devices. *Journal of Applied Physics*, **112** 064315, 2012.

Acknowledgements

First of all, I would like to thank Associate prof. Tetsuo Kodera for supervising my PhD thesis. He has been my mentor since I was a bachelor student. He always guided me to the correct direction. I would also like to express my gratitude to Emeritus Prof. Shunri Oda for his supervision. Since my bachelor thesis which he supervised, he has always encouraged me. I thank him also for joining the committee of this thesis.

My deepest appreciations go to Prof. Mutsuko Hatano, Prof. Yasuyuki Miyamoto, Prof. Hitoshi Wakabayashi, Associate Prof. Safumi Suzuki, Associate Prof. Yukio Kawano, and Associate Prof. Masaharu Kobayashi for examining this thesis.

I thank Prof. Toshiro Hiramoto for his kindness that his group deposited SiO_2 with LPCVD for our devices. I am also grateful to Prof. Yasuhiko Arakawa for his generous permission to use the cryostat, which was indispensable to realize the present thesis.

I owe a very important debt to Project Associate Prof. Jun Yoneda. His insightful and inspiring comments and suggestions helped me a lot.

I want to thank Dr. Tomohiro Kambara and Dr. Kousuke Horibe from whom I took over the device fabrication techniques and the measurement methods during my bachelor and master theses. As for the device fabrication, I am also indebted to Dr. Koichi Usami for his support.

Special thanks to Dr. Tomohiro Noguchi, Dr. Daichi Suzuki, Jun Kamioka,

Nobuhiro Kondo, Ko Yamada, and Takayoshi Kuga, with whom I worked when I was a student in Oda lab. The time I spent with them and the discussion we had has always been valuable, intellectually and mentally.

I also thank the other ex- and present lab members. Especially, I am deeply grateful to Mizuki Kobayashi, Masahiro Tadokoro, and Masaru Hirayama for fruitful discussions.

Last but not least, I thank my family for supporting me during the years.

Publications

Scientific articles relating to this PhD thesis

1. R. Mizokuchi, S. Oda, T. Kodera,
   "Physically defined triple quantum dot systems in silicon on insulator,"
   Applied Physics Letters **114**, 073104 (2019).

2. R. Mizokuchi, M. Tadokoro, T. Kodera,
   "Detection of tunneling events in physically defined silicon quantum dot using single-shot measurements improved by numerical treatments,"
   Applied Physics Express **13**, 121004 (2020).

3. R. Mizokuchi, S. Bugu, M. Hirayama, J. Yoneda, and T. Kodera
   "Radio-frequency single electron transistors in physically defined silicon quantum dots with a sensitive phase response,"
   Scientific Reports **11**, 5863 (2021).

Scientific articles before this PhD

1. R. Mizokuchi, P. Torresani, R. Maurand, Z. Zeng, Y.-M. Niquet, M. Myronov, S. De Franceschi,
   "Hole weak anti-localization in a strained-Ge surface quantum well."
   Applied Physics Letters **111**, 063102 (2017).

2. R. Mizokuchi, R. Maurand, F. Vigneau, M. Myronov, S. De Franceschi, "Ballistic One-Dimensional Holes with Strong g - Factor Anisotropy in Germanium."
   Nano Letters **18**, 4861 (2018).

Co-authored scientific articles

1. F. Vigneau, R. Mizokuchi, D. C. Zanuz, X. Huang, S. Tan, R. Maurand, S. Frolov, A. Sammak, G. Scappucci, F. Lefloch, and S. De Franceschi
   "Germanium Quantum-Well Josephson Field-Effect Transistors and Interferometers,"
   Nano Letters **19**, 1023 (2019)

2. N. Lee, R. Tsuchiya, G. Shinkai, Y. Kanno, T. Mine, T. Takahama, R. Mizokuchi, T. Kodera, D. Hisamoto, and H. Mizuno,
   "Enhancing electrostatic coupling in silicon quantum dot array by dual gate oxide thickness for large-scale integration,"
   Applied Physics Letters **116**, 162106 (2020).

3. M. Tadokoro, R. Mizokuchi, and T. KODERA,
   "Pauli spin blockade in a silicon triangular triple quantum dot,"
   Japanese Journal of Applied Physics **59**, SGGI01 (2020).

4. H. Wei, S. Mizoguchi, R. Mizokuchi, and T. Kodera,
   "Estimation of hole spin g-factors in p-channel silicon single and double quantum dots towards spin manipulation,"
   Japanese Journal of Applied Physics **59**, SGGI10 (2020).

5. 米田 淳, 溝口 来成, 小寺 哲夫,
   "シリコン量子ドット単一キャリアスピンの高周波反射計測,"
   固体物理 **56**, 265 (2021).

International conference presentations

1. R. Mizokuchi, T. Kodera, K. Horibe, Y. Kawano, and S. Oda
   "Charge sensing of a Si triple quantum dot system using single electron transistors,"
   IEEE Silicon Nanoelectronics Workshop, June 2012, Honolulu (poster)

2. R. Mizokuchi, T. Kodera, K. Horibe, Y. Kawano, Y. Arakawa, and S. Oda
   "Observation of electron transitions in triple quantum dot by using charge sensor,"
   IEEE EDS WIMNACT-37, February 2013, Tokyo (poster)

3. R. Mizokuchi, T. Kodera, K. Horibe and S. Oda
   "Perpendicular magnetic field dependence of triangular triple silicon quantum dot system,"
   2014 Silicon Nanoelectronics Workshop, June 2014, Honolulu (poster)

4. R. Mizokuchi, S. Bugu, M. Hirayama, M. Tadokoro, and T. Kodera
   "RF reflectometry on physically defined triangular triple quantum dot,"
   Topical Conference on Quantum Computing 2019, December 2019, Kyoto (poster)

5. R. Mizokuchi, M. Hirayama, S. Nishiyama, K. Kato, Y. Liu, S. Murakami, T. Mori, J. Yoneda, T. Kodera
   "Equivalent Circuit Analysis of RF Reflectometry of Physically Defined Quantum Dot Systems,"
   Joint Conference EP2DS-24/MSS-20, November 2021, Online (oral)