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Study of Three-phase Inverter Using Multiple Bidirectional Choppers Intended for Utility-scale PV Systems

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Dedication

This dissertation is completed with help from my supervisor and my best friends in my laboratory and support from my family. I did not know why I came so far, but now I feel I can move further. To every important people in my life so far, I appreciate your accompany.

Abstract

This dissertation presents a detailed study of a novel three-phase inverter for utility-scale PV systems where multiple cascaded bidirectional chopper cells and a three-phase line-frequency transformer with a three-limb core are used. The proposed inverter can achieve a wider MPPT operation voltage range. In addition, the elimination of the high-frequency circulating current under the simultaneous parallel operation of inverters is also achieved. Two different control methods are carried out and tested successively to increase the stability of the entire circuit. Meanwhile, the initial charging of the floating capacitors is also achieved for the inverter operation. Furthermore, the LVRT capability of the proposed inverter under the grid fault is addressed, and the theoretical analysis and the experimental verification are carried out. In the end, the evaluation of chopper-cell number of the proposed inverter is conducted based on experimental verification and mathematical analysis.

Acknowledgments

If you ask me 'Should I pursue a PhD degree?' for 100 times, I will give you the same answer 'Think carefully. It is not what you think.' every time. This journey is long and lonely. However, I am glad that I am lucky enough to have so many people that will help me when I feel lost.

Associate Professor **Makoto Hagiwara** (萩原　誠), my first mentor and advisor in Japan. Thank you for accepting me to the Hagiwara Lab even though my major was different from your research topics. I have to say I never know a professor like you that will help the students that much in both life and research. Without you, I will be still wandering and end up in nowhere.

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Professor **Hideaki Fujita** (藤田　英明), will ask me some difficult questions sometimes to make me realize that I am still far away from understanding the entire research topic. You taught me that a researcher should not only focus on his own research. Instead, a research should learn as much as he can and pay attention to the difference between theory and practice, which is a very useful advice.

Dr. **Nikola Krneta**, my best friend in the laboratory. We have similar background and interests. During these three years, we helped each other and he helped me more, frankly. Thank you for giving me advices on my research and teaching me many things I did not know. I will miss the days we worked in lab and played games together.

Contents

List of Figures

List of Tables

List of Abbreviations

3P	three-phase xvi, 13, 14, 83, 84, 95, 103–105, 115, 121, 127, 129, 130
AC	alternating current xvii, xxiii, xxv, xxvii, 1, 6, 8, 11, 14, 15, 17, 18, 26, 27, 34, 37, 39, 40, 42, 51, 54, 56–58, 63, 76, 83–85, 87–89, 95, 99, 111, 115, 131, 132
BESS	battery energy storage system 8, 10
BTB	back-to-back 11
CB	combiner box 5
DAB	dual-active-bridge xiii, 18
DC	direct current xiv, xv, xxiii–xxix, 1, 5, 6, 8, 11–13, 16–18, 20, 26, 27, 31–40, 42–44, 46, 48, 50, 51, 53–56, 58–63, 65, 69, 71, 73–76, 79, 80, 83–89, 91, 92, 95, 98–100, 103, 106, 110, 111, 114, 115, 118, 121, 130
DER	distributed energy resource 20
DSBC	double-star bridge-cells xiii, 8, 10, 11
DSCC	double-star chopper-cells xiii, 8, 10, 11
DSP	digital signal processor 43, 59
EU	European Union xiii, 3
FPGA	field-programmable gate array 43, 59
HCC	hybrid cascade converter 20, 22
HERIC	high efficient and reliable inverter concept xiii, 16
HVDC	high-voltage direct current 11, 22, 109
IEA	international energy agency 2, 3

IGBT	insulated-gate bipolar transistor 5, 11, 20, 22, 73, 74, 110
LVRT	low-voltage ride-through v, xvi, 12–15, 19, 20, 23, 83, 94, 103, 106, 121, 131, 132
MAF	moving average filter 54, 87, 99
MMCC	modular multilevel cascade converter xiii, 8, 10–13, 15, 19, 20, 22, 23, 40, 51, 109, 110
MOSFET	metal-oxide-semiconductor field-effect transistor 20
MPPT	maximum-power-point-tracking v, xv–xvii, 6, 8, 11, 16–19, 27, 37, 51, 74–78, 81, 110, 111, 113, 131, 132
NSC	negative-sequence current 20
PCS	power conditioning system 11
PI	proportional-integral xxvii, 40, 89, 132
PLL	Phase locked loop xxviii, 28, 86, 90
PV	photovoltaic v, xiii, xv, xvii, xxiv, xxv, xxvii, 1–8, 11–19, 22, 23, 25–27, 42, 51, 58, 71, 76, 84, 95, 106, 109, 114, 115, 131, 132
PWM	pulse-width modulation 17, 19, 26, 36, 37, 42
RMS	root-mean-square xxv, xxvii, 6, 27, 28, 33, 43, 46, 76, 115, 118
SDBC	single-delta bridge-cells xiii, 8, 10, 20, 22, 40
SLG	single-line-to-ground xv, xvi, xxiii–xxviii, 13, 83–92, 94–103, 106, 115, 121, 123, 125, 130, 131
SSBC	single-star bridge-cells xiii, 8, 10, 20, 22
STATCOM	static synchronous compensator 8, 10, 20
SVPWM	space-vector pulse-width modulation 19
THD	total harmonic distortion 13, 14, 71, 118, 130, 132
US	United States xiii, 2, 17
ZCS	zero-current switching xiii, 29–31, 33–35, 37, 46, 62, 65, 110, 118
ZSC	zero-sequence current xxvi, 20, 22, 27, 39, 40, 46, 61
ZSV	zero-sequence voltage 20, 36, 37

Nomenclature

$(v_{\mathrm{AuF}})_{\mathrm{dc}}$	DC component of u-phase auxiliary converter output voltage during SLG fault
$(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$	Fundamental-frequency component of u-phase auxiliary converter output voltage
$(v_{\mathrm{Au}})_{\mathrm{dc}}$	DC component of u-phase auxiliary converter output voltage
$(v_{\mathrm{Au}})_{\mathrm{max}}$	Maximum output voltage of u-phase auxiliary converter
$(v_{\mathrm{Au}})_{\mathrm{ripple}}$	High frequency component of u-phase auxiliary converter output voltage
$(v_{\mathrm{CAvg}})_{\mathrm{dc}}$	DC component of v_{CAvg}
$(v_{\mathrm{Cu}})_{\mathrm{ac}}$	AC component of v_{CuAvg}
$(v_{\mathrm{Cu}})_{\mathrm{dc}}$	DC component of v_{CuAvg}
$(v_{\mathrm{Cv}})_{\mathrm{ac}}$	AC component of v_{CvAvg}
$(v_{\mathrm{Cv}})_{\mathrm{dc}}$	DC component of v_{CvAvg}
$(v_{\mathrm{Cw}})_{\mathrm{ac}}$	AC component of v_{CwAvg}
$(v_{\mathrm{Cw}})_{\mathrm{dc}}$	DC component of v_{CwAvg}
$(v_{\mathrm{Mu}})_{50\,\mathrm{Hz}}$	Fundamental-frequency component of u-phase main converter output voltage
$\lvert i_{\mathrm{u2F}}\rvert_{\mathrm{Max}}$	Peak value of i_{u2F} during SLG fault
$\lvert i_{\mathrm{v2F}}\rvert_{\mathrm{Max}}$	Peak value of i_{v2F} during SLG fault
α	Turn-on (turn-off) angle of the main converter

α_{F}	Turn-on (turn-off) angle of the main converter during SLG fault
Δi_{u2F}	Variation of i_{u2F} during SLG fault
Δi_{udc0}	DC current introduced for u-phase DC-capacitor voltage control
Δi_{v2F}	Variation of i_{v2F} during SLG fault
Δi_{z0}	Variation of i_{z0}
Δp_{Cu}	Power flows into u-phase auxiliary converter originating from $(v_{\mathrm{Au}})_{\mathrm{dc}}$ and i_{udc0}
Δp_{Cv}	Power flows into v-phase auxiliary converter originating from $(v_{\mathrm{Av}})_{\mathrm{dc}}$ and i_{vdc0}
Δp_{Cw}	Power flows into w-phase auxiliary converter originating from $(v_{\mathrm{Aw}})_{\mathrm{dc}}$ and i_{wdc0}
ΔP_{inu}	Variation of DC input power of u-phase inverter
ΔP_{uac}	U-phase cluster balancing power
η	Power efficiency of PV array
ω	Radius velocity
ϕ	Phase jump angle during SLG fault
θ	Phase angle of u-phase
a	Transformer voltage ratio
C	Cell capacitor
D_{M}	Duty cycle of main converter
E	DC input voltage of PV system
E_{a}	Voltage of PV array in simulation
E_{min}	Minimum input voltage of PV system
f_{SA}	Carrier frequency of each chopper cell

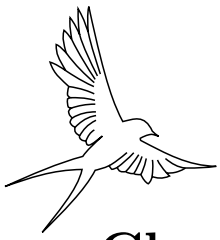
f_{SM}	Grid frequency/Carrier frequency of main converter
I_{ac}	RMS value of u-phase inductor current fundamental-frequency component
I_{a}	Output current of PV array in simulation
I_{dcF}	DC component of inductor current during SLG fault
I_{dc}	DC component of inductor current
i_{dc}^{*}	Reference value of I_{dc}
i_{d}	D-axis current in current control
i_{d}^{*}	Reference value of i_{d}
i_{inu}	DC input current of u-phase
i_{in}	DC input current of three phases
i_{n}	Neutral current
i_{q}	Q-axis current in current control
i_{q}^{*}	Reference value of i_{q}
i_{u1}	Grid current of u-phase
i_{u2F}	Inductor current of u-phase during SLG fault
i_{u2}	Inductor current of u-phase
i_{u2}^{*}	Reference value of i_{u2}
i_{uac}^{*}	Reference value of AC component of u-phase inductor current
i_{ucomp}^{*}	Reference value of AC component of u-phase inductor current after phase compensation
i_{udc0}	DC current introduced for u-phase DC-capacitor voltage control
i_{udc0}^{*}	Reference value of i_{udc0}
i_{udc}	Total DC current introduced in u-phase

i^*_{udc}	Reference value of i_{udc}
i_{v2F}	Inductor current of v-phase during SLG fault
i_{v2}	Inductor current of v-phase
i^*_{v2}	Reference value of i_{v2}
i_{vdc0}	DC current introduced for v-phase DC-capacitor voltage control
i^*_{vdc0}	Reference value of i_{vdc0}
i_{vdc}	Total DC current introduced in v-phase
i^*_{vdc}	Reference value of i_{vdc}
i_{w2F}	Inductor current of w-phase during SLG fault
i_{w2}	Inductor current of w-phase
i^*_{w2}	Reference value of i_{w2}
i_{wdc0}	DC current introduced for w-phase DC-capacitor voltage control
i^*_{wdc0}	Reference value of i_{wdc0}
i_{wdc}	Total DC current introduced in w-phase
i^*_{wdc}	Reference value of i_{wdc}
i_{z0}	ZSC introduced for DC-capacitor overall voltage control
i^*_{z0}	Reference value of i_{z0}
i_{zp}	ZSC introduced for DC-capacitor cluster balancing control
i^*_{zp}	Reference value of i_{zp}
i_{z}	ZSC introduced in each phase inductor current
i^*_{z}	Reference value of i_{z}
k	Ratio of I_{dc} and I_{ac} in high DC input voltage case
K_{P}	Proportional coefficient of the individual current control

K_{vI}	Integral coefficient of the DC-capacitor voltage PI control
K_{vP}	Proportional coefficient of the DC-capacitor voltage PI control
L	Inductor
l	Leakage inductance of Transformer
m	Voltage sag coefficient
N	Chopper-cell number per phase
p^*	Reference value of three-phase output active power
P_{a}	Output power of PV array in simulation
P_{inu}	DC input power of u-phase inverter
$p_{\max(t)}$	Maximum output of PV array
P_{outu}	AC output power of u-phase inverter
$p_{\mathrm{out}(t)}$	Output function of PV array
$P_{dis\mathrm{u}}$	Power disturbance of u-phase caused by SLG fault
$P_{dis\mathrm{v}}$	Power disturbance of v-phase caused by SLG fault
$P_{dis\mathrm{w}}$	Power disturbance of w-phase caused by SLG fault
q^*	Reference value of three-phase output reactive power
V_{ac}	RMS value of the AC side line-to-neutral phase grid voltage
v^*_{Auj}	Reference value of the output voltage of the j-th cell in u-phase auxiliary converter
v_{Au}	Auxiliary converter output voltage of u-phase
v^*_{Au}	Reference value of v_{Au}
v_{CAvg}	Arithmetic average value of all the DC-capacitor voltage of three phases
v_{Cmin}	Minimum DC-capacitor voltage of each cell

v_{conu}	Inverter line-to-neutral output voltage of u-phase
v^*_{conu}	Reference value of v_{conu}
v_{conv}	Inverter line-to-neutral output voltage of v-phase
v^*_{conv}	Reference value of v_{conv}
v_{conw}	Inverter line-to-neutral output voltage of w-phase
v^*_{conw}	Reference value of v_{conw}
v_{Cu1}	DC-capacitor voltage of the first cell of u-phase
v_{CuAvg}	Arithmetic average value of all the DC-capacitor voltage of u-phase
v_{CuN}	DC-capacitor voltage of the N-th cell of u-phase
v_{Cv1}	DC-capacitor voltage of the first cell of v-phase
v_{CvAvg}	Arithmetic average value of all the DC-capacitor voltage of v-phase
v_{CvN}	DC-capacitor voltage of the N-th cell of v-phase
v_{Cw1}	DC-capacitor voltage of the first cell of w-phase
v_{CwAvg}	Arithmetic average value of all the DC-capacitor voltage of w-phase
v_{CwN}	DC-capacitor voltage of the N-th cell of w-phase
V_{dF}	D-axis component of transformer secondary voltage used in PLL during SLG fault
V_{d}	D-axis component of transformer secondary voltage used in PLL
v_{d}	D-axis voltage in current control
v_{MuF}	Main converter output voltage of u-phase during SLG fault
v_{Mu}	Main converter output voltage of u-phase
v^*_{Mu}	Reference value of v_{Mu}
v_{MvF}	Main converter output voltage of v-phase during SLG fault

v_{q}	Q-axis voltage in current control
v_{u1F}	U-phase line-to-neutral primary (grid) voltage of transformer during fault
v_{u2F}	U-phase line-to-neutral secondary voltage of transformer during fault
v_{u2}	U-phase line-to-neutral secondary voltage of transformer
v^*_{u2}	Reference value of v_{u2}
v^*_{udc}	Output of proportional regulator in individual current control
v_{uw1}	Line-to-line (u-w) grid voltage
v_{v1F}	V-phase line-to-neutral primary (grid) voltage of transformer during fault
v_{v2F}	V-phase line-to-neutral secondary voltage of transformer during fault
v_{v2}	V-phase line-to-neutral secondary voltage of transformer
v^*_{v2}	Reference value of v_{v2}
v_{vu1}	Line-to-line (v-u) grid voltage
v_{w1F}	U-phase line-to-neutral primary (grid) voltage of transformer during fault
v_{w2F}	U-phase line-to-neutral secondary voltage of transformer during fault
v_{w2}	W-phase line-to-neutral secondary voltage of transformer
v^*_{w2}	Reference value of v_{w2}
v_{wv1}	Line-to-line (w-v) grid voltage
V^*_C	Reference value of DC-capacitor voltage



Chapter 1

Introduction

This dissertation presents a detailed study of a novel three-phase inverter for utility-scale PV (photovoltaic) systems where multiple cascaded bidirectional chopper cells and a three-phase line-frequency transformer with a three-limb core are used. With the accelerated development of the PV generation systems, the generation capacity of the PV systems is growing into utility scale, and it brings challenges to conventional PV inverters [1]–[6]. Therefore, new topology structure of PV inverter is required.

1.1 Research Background

Nowadays, PV generation system is no more an unfamiliar concept to everyone. It could be as small as several square meters which is able to be put on your rooftop or as large as tens of square kilometers which takes you several hours to walk across it. The former is preferred to be regarded as a PV chargeable battery connected to some electrical furnitures, and the latter is called as utility-scale PV generation system. For existing utility-scale PV generation systems connected to grids, conventional two- or three-level three-phase PV inverters are used as the connection interface between them because it is necessary to convert DC (direct current) power into AC (alternating current) power. However, the fast development of the PV generation systems brings challenges to them.

1.1.1 Development of PV Energy

To reduce the consumption of fossil fuels (coil, gas, oil), which cause more pollution and will be exhausted someday [7], the contribution from the renewable energy sources is being increased. Among them, the PV energy is the fastest developing one. It is reported that

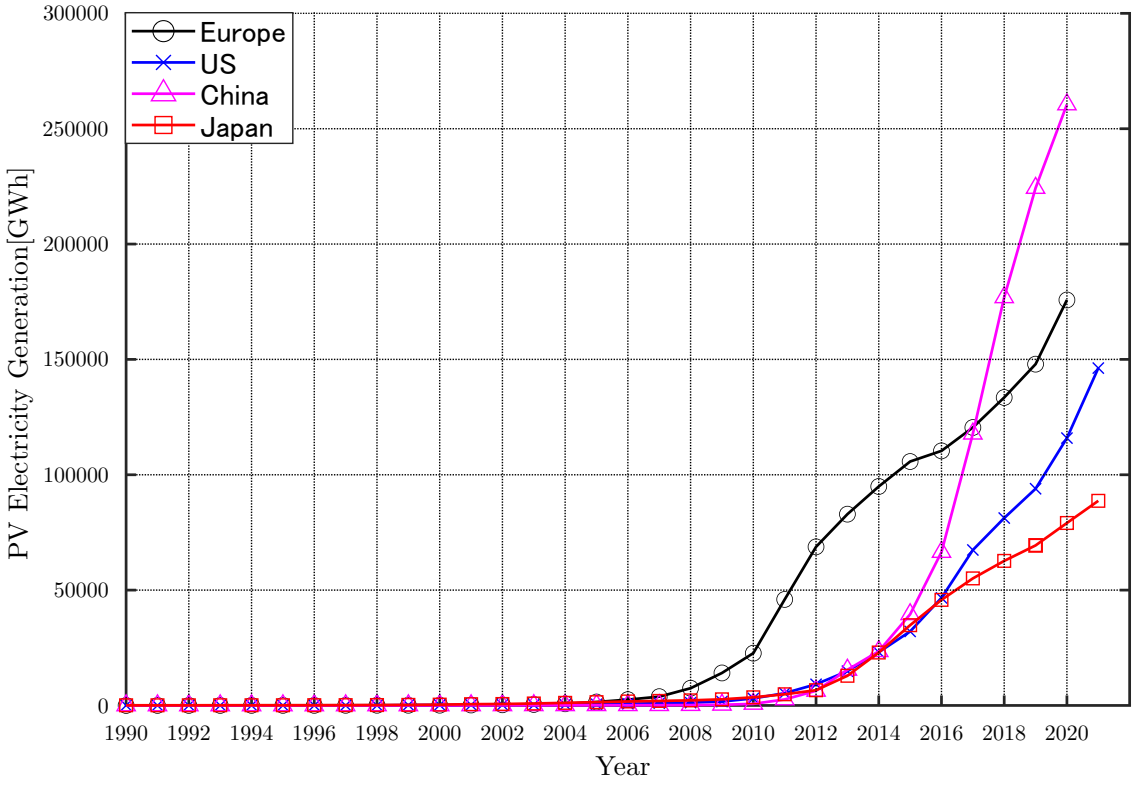


Figure 1.1: PV electricity generation of Europe, US, China, and Japan.

the global PV energy production in 2021 is over 1000 TWh and it is estimated that this number should reach 6970 TWh to achieve long-term carbon neutrality [8], which means the developing speed will be even faster.

Fig. 1.1 shows the contribution of PV electricity generation of four regions, the PV generation technology development of which are boosting in last ten years [9]–[12]. According to Fig. 1.1, it is obvious that China has the most contribution of PV electricity generation, which reached 260.5 TWh in 2020. The fast increase of PV generation contribution of China is the result of following the president's call for an "energy revolution" and the "fight against pollution" [11]. But it is also the result pushed by the large consumption requirement because of its large population. The data from IEA (international energy agency) show that the contribution of PV generation of Europe and US (United States) have similar trend and it is estimated that both regions are in positions to deliver more reliable, more affordable, and more environmental sustainable energy systems. Japan has the lowest relative contribution of PV generation among them. However, this number increased from 4839 GWh to 88 701 GWh in the last decade, which is an 18-fold increase and it will increase even faster to achieve its ambition of carbon-neutrality by 2050.

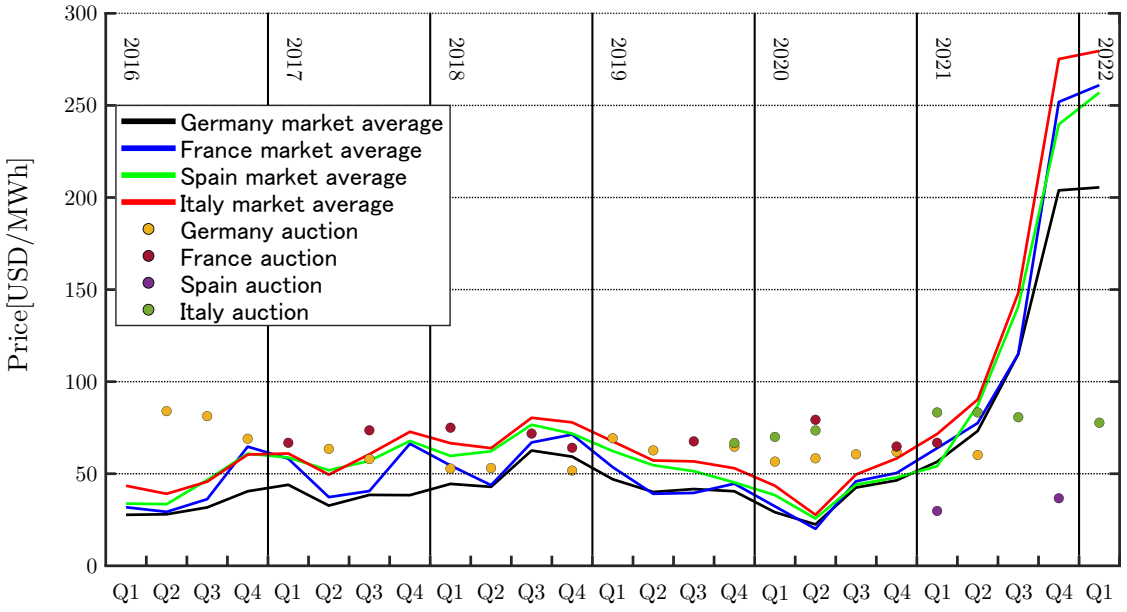


Figure 1.2: Utility-scale solar PV auction contract and wholesale prices in four EU countries, quarterly averages from 2016-2022.

Meanwhile, the energy market also stimulates the development of PV energy generation. Historically, long-term contract prices from utility-scale PV generation systems have been higher than wholesale prices of fossil fuels in many large EU (European Union) markets. However, significant change happened in 2021 according to the report from IEA [13]. The prices of fossil fuels have risen at an incredible rapid speed since the last quarter of 2021, which broke historic records in many parts of the world and this is caused by the war. Consequently, even the highest price of utility-scale PV generation system contracts over the last five years is much lower than the wholesale prices of fossil fuels nowadays, which is shown in Fig. 1.2 [14].

Because of this dramatic change in the energy market, more and more investment is poured into the PV generation system, which is shown as Fig. 1.3 [15]. It is shown in Fig. 1.3 that the investment in the fossil fuels is kept at a low level compared with the renewable energy, and the investment in the PV generation system is estimated to be over 360 billion dollars in 2023. As a result, more and more utility-scale PV generation systems are built and their capacity are increasing rapidly, which brings challenges to the conventional PV inverters.

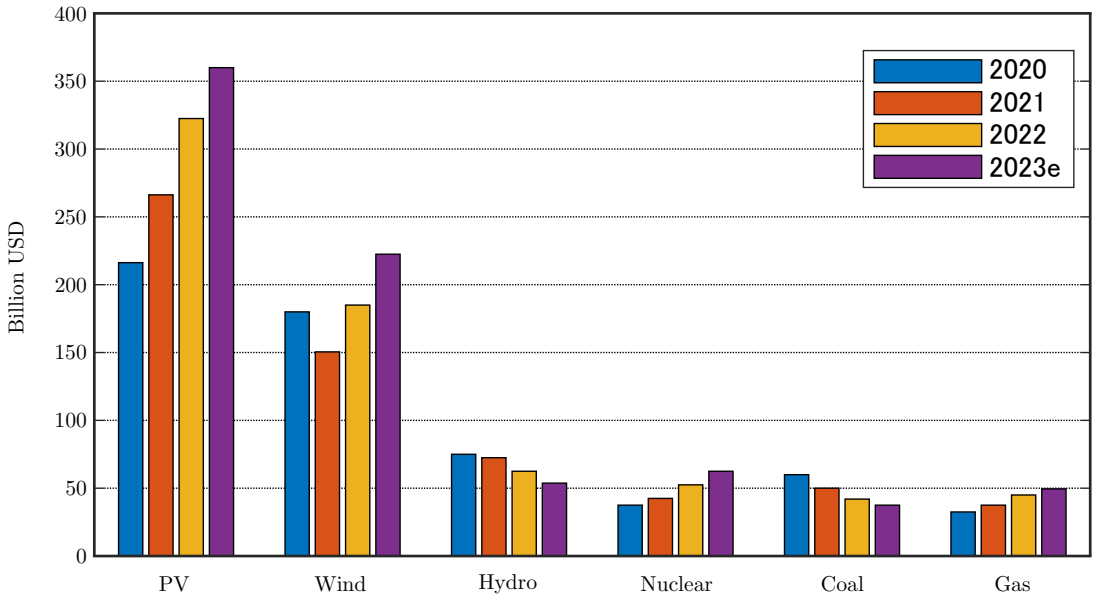


Figure 1.3: Global annual investment in energy generation.

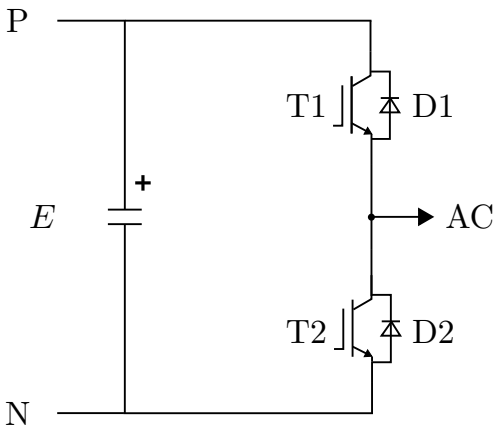


Figure 1.4: Conventional two-level PV inverters.

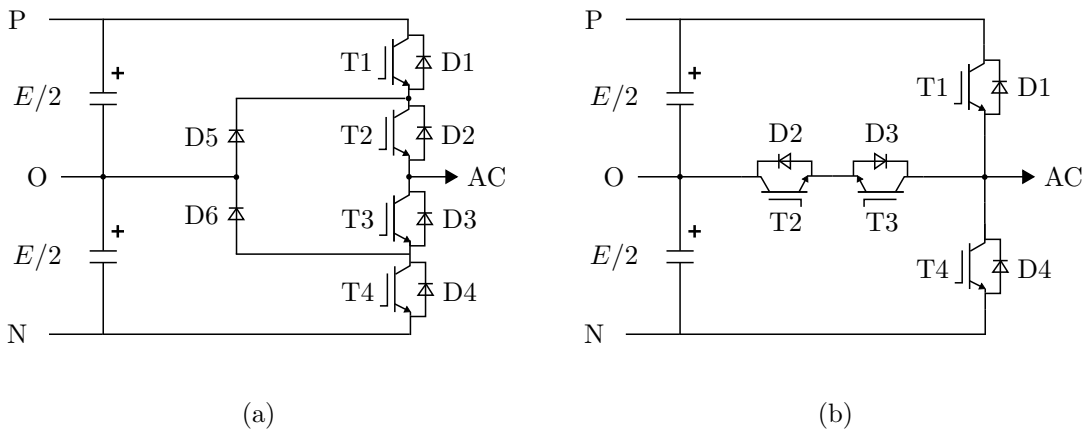


Figure 1.5: Conventional three-level PV inverters: a) three-level I-type, b) three-level T-type.

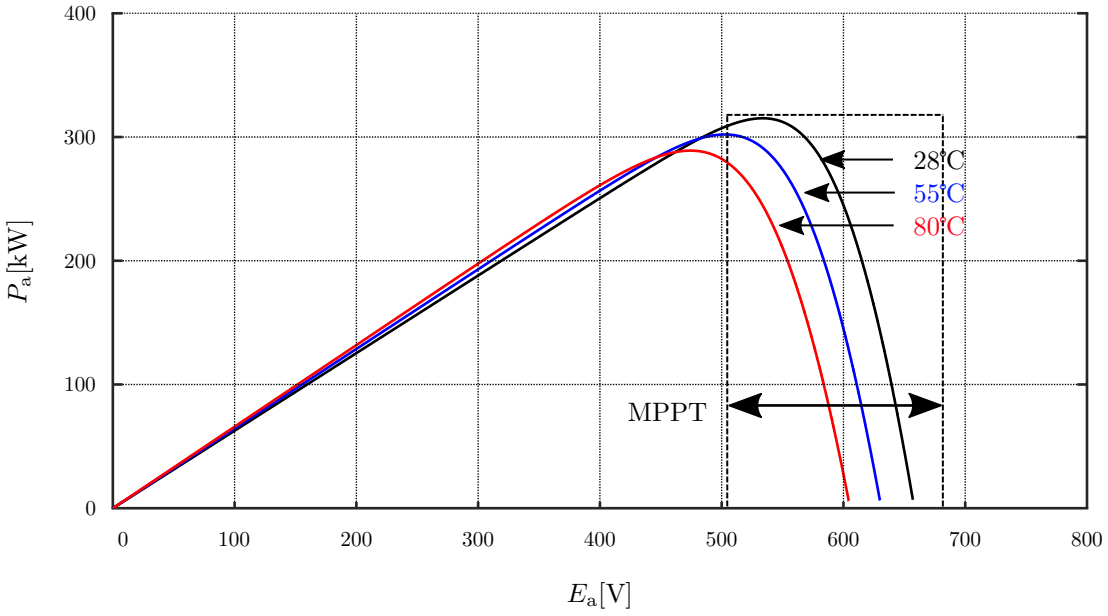
1.1.2 Conventional PV Inverter

The utility-scale PV generation system can be divided into the grid-connected system and the stand-alone system [16], [17], where the former uses the conventional two- or three-level inverters for grid connection. With the development of the utility-scale PV generation systems, the DC input voltage has been increasing. Recent studies reveal that the installation cost can be reduced significantly by increasing the DC input voltage from 1 kV to 1.5 kV [18]–[21]. Because of the higher DC input voltage, more PV modules are able to be installed per string, which decreases the conductor mass and the number of CBs (combiner boxs) [22]. In this situation, the conventional two-level inverters shown in Fig. 1.4, which are widely applied to existing 1-kVdc PV systems, cannot satisfy the requirements of the systems because the power losses are large and the filtering requirement is high [23]–[26]. In contrast, the three-level inverters are widely used in the existing 1.5-kVdc PV systems, and two well-known topologies of three-level inverters are shown in Figs. 1.5a and 1.5b. Compared to the two-level inverter, the three-level ones have lower total cost and higher efficiency when switching frequency is over 2 kHz. There are two more diodes in the three-level I-type inverter and it is noteworthy that the voltage ratings of the four IGBTs (insulated-gate bipolar transistors) are the same in the three-level I-type inverter, whereas the voltage ratings of T1 and T4 are higher than those of T2 and T3 in the three-level T-type inverter. Specifically, the efficiency performance of three-level T-type inverter is better than that of the three-level I-type one in most of the applications in 1.5-kVdc PV generation systems [1], [27].

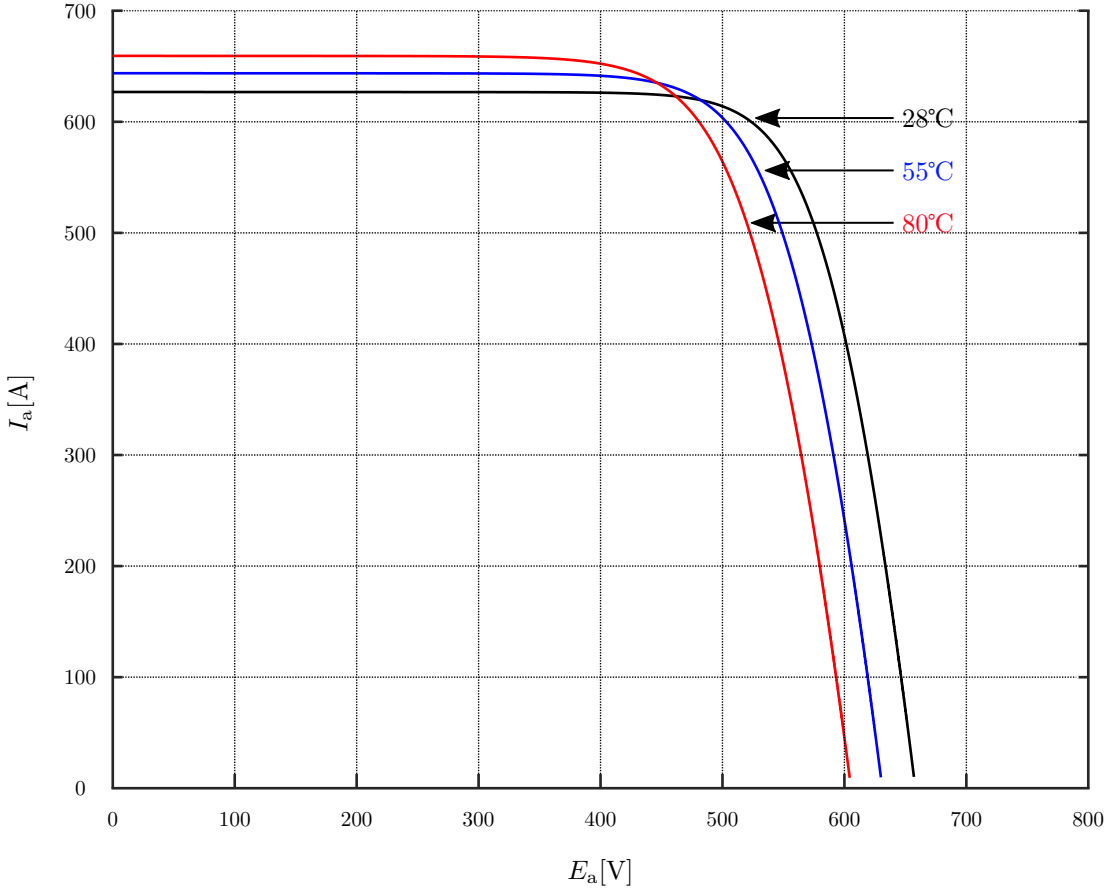
On the other hand, the power rating of the utility-scale PV generation systems has grown into megawatt level [1], [27]–[30] as the consumption requirement increases. Meanwhile, this trend put the conventional three-level inverter in a dilemma because of the power characteristic of the PV array. The relationships between the PV array voltage, E_{a}, output current, I_{a}, and the output power, P_{a}, at different temperatures are shown in Figs. 1.6a and 1.6b. The P_{a}-$V_{\mathbf{a}}$ and I_{a}-V_{a} characteristics are obtained from a PSCAD simulation under a irradiation level of $1000\,\mathrm{W/s^2}$. It is noteworthy that this simulation is not based on reality data and it is only for a brief explanation. It is obvious that the P_{a}-$V_{\mathbf{a}}$ and I_{a}-V_{a} characteristics are affected by the ambient temperature and the maximum power point fluctuates during the day. In order to keep the PV array output at the maximum point all the time, the PV generation system has an MPPT (maximum-power-point-tracking) function to adjust the output voltage of the PV array. The upper limit of the MPPT range is mostly decided by the voltage rating of the power devices, which is not a concern. However, the lower limit of it is decided by the voltage relationship between the DC side and the AC side. In the case of using conventional three-level inverters, this relationship is shown as

$$E \geq \sqrt{6}V_{\mathrm{ac}}, \tag{1.1}$$

with third-order harmonics component introduced, where E is the input voltage of DC side and V_{ac} is the RMS (root-mean-square) value of the AC side line-to-neutral phase grid voltage. To operate the PV system throughout the year, V_{ac} has to be set based on the minimum DC input voltage at the highest temperature in summer, which results in a large AC current and a large conduction loss, especially in a megawatt level PV system. In order to reduce the conduction loss, one of the methods is to increase V_{ac}. However, this method narrows the range of MPPT. For example, a PV system with an RMS line-to-line AC voltage of 660 V ($\sqrt{3}V_{\mathrm{ac}} = 660\,\mathrm{V}$) with an MPPT range of 960 V to 1300 V was development and this range was narrowed down to 1005 V to 1300 V when the RMS line-to-line AC voltage increased to 690 V [31]. In other words, the available MPPT range will be curtailed if the conventional three-level inverters are applied to utility-scale PV generation systems. When the MPPT range is narrowed, the power efficiency of the PV



(a)



(b)

Figure 1.6: PV array power characteristics obtained from PSCAD simulation: a) P_a-V_a, b) I_a-V_a.

array will decrease, which is defined as:

$$\eta = \frac{\int p_{\text{out}}(t)\,\mathrm{d}t}{\int p_{\text{max}}(t)\,\mathrm{d}t}. \tag{1.2}$$

On the other hand, if the MPPT range can be widened, more output power can be obtained.

Consequently, PV systems based on state-of-the-art MMCC (modular multilevel cascade converter) topologies have drawn attention as the connection interface between the PV systems and the grid in recent years [32]–[35].

1.1.3 The MMCC

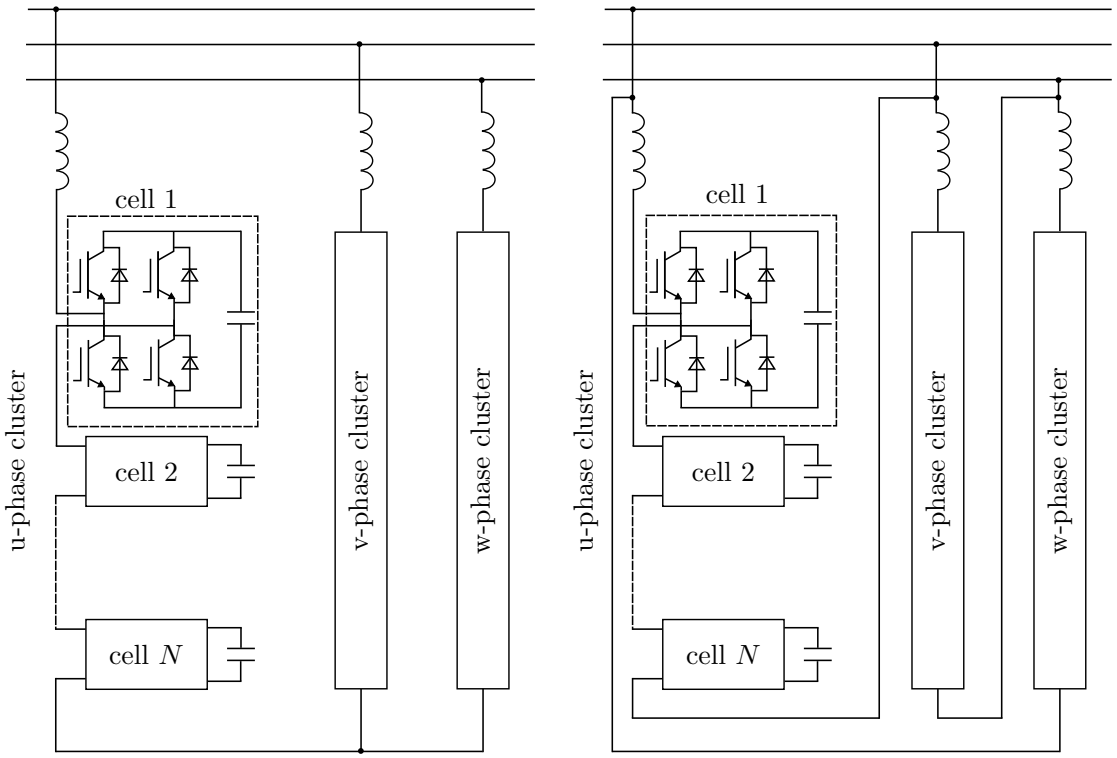
Nowadays, the MMCC technology is well-developed and the MMCCs are more and more used in AC-DC and DC-DC systems. This section will give out a brief introduction of MMCC. Basically, there are four circuit configurations of MMCC [32]:

1. SSBC (single-star bridge-cells) (Fig. 1.7a);
2. SDBC (single-delta bridge-cells) (Fig. 1.7b);
3. DSCC (double-star chopper-cells) (Fig. 1.7c with cell Fig. 1.7d);
4. DSBC (double-star bridge-cells) (Fig. 1.7c with cell Fig. 1.7e).

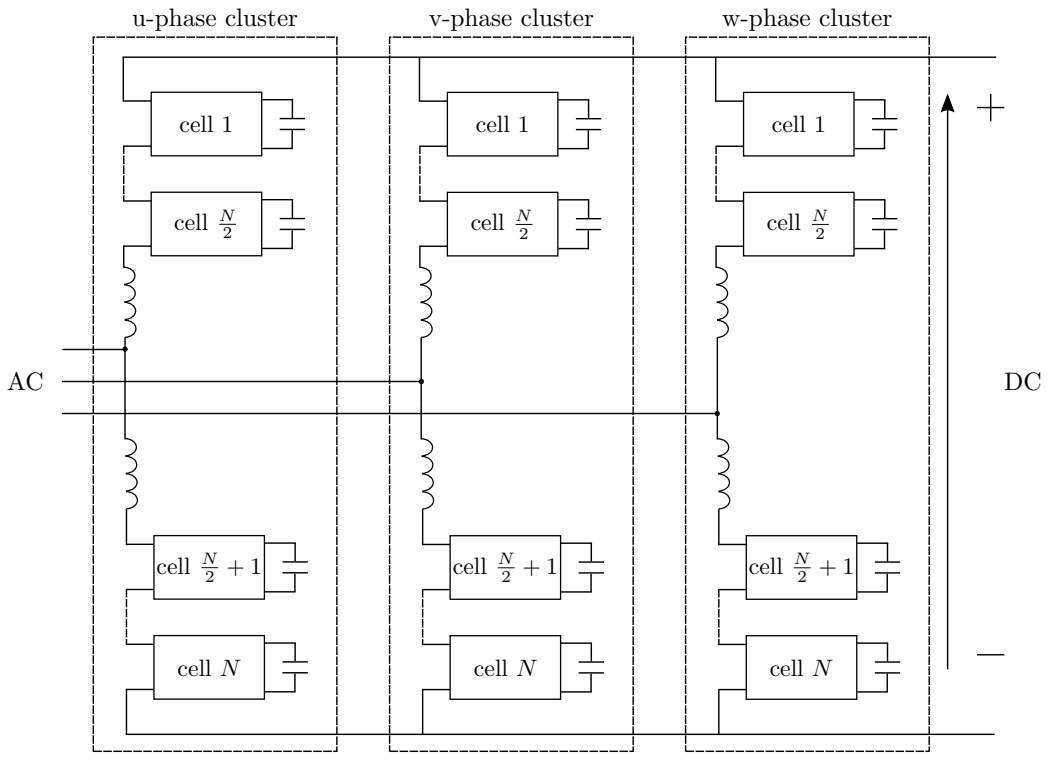
The SSBC is different from the SDBC in the connection topology of three-phase clusters, whereas the DSCC is different from the DSBC in the types of the cells. It is noteworthy that the two non-coupled inductors on the same phase cluster can be replaced by one coupled inductor to reduce the size and the weight. These MMCCs can output multilevel waveforms, which can reduce the size of passive filter in the grid-connected applications. Besides, owing to their different structures, each of them has their unique application cases.

1.1.3.1 Application of the SSBC

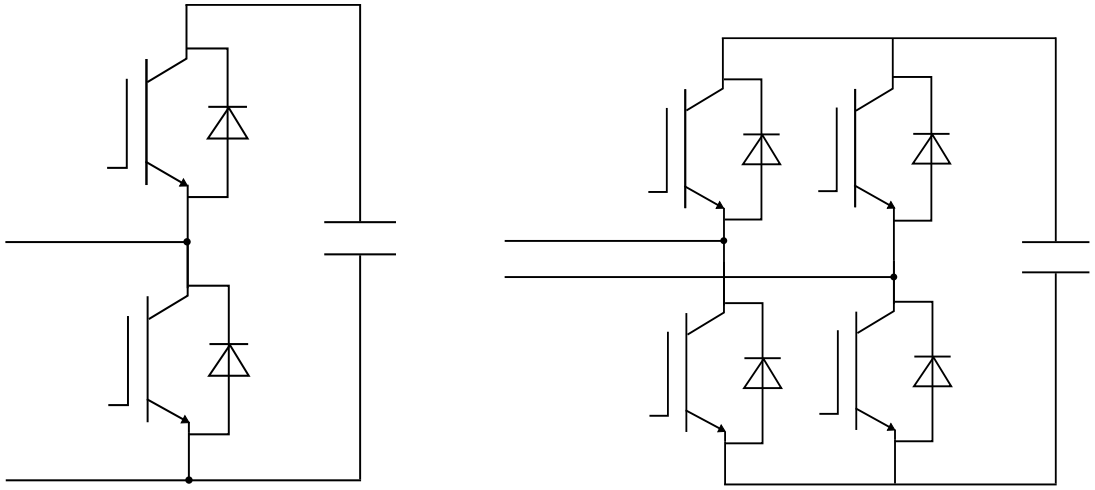
Because of the star-connection of the three-phase clusters in SSBC, there is no flowing route for the zero-sequence current. Therefore, the SSBC can only control the positive-sequence leading and lagging reactive power. Consequently, the best application case of the SSBC is not STATCOM (static synchronous compensator) but the BESS (battery


cell 1
cell 2
cell N
u-phase cluster
v-phase cluster
w-phase cluster
cell 1
cell 2
cell N
u-phase cluster
v-phase cluster
w-phase cluster

(a) (b)


u-phase cluster
v-phase cluster
w-phase cluster
cell 1
cell $\frac{N}{2}$
cell $\frac{N}{2}+1$
cell N
AC
DC
+
—

(c)



(d) (e)

Figure 1.7: Basic circuit configurations of MMCC and their cell circuit configurations: a) SSBC, b) SDBC, c) DSCC or DSBC, d) Chopper cell, e) Bridge cell.

energy storage system) [36], [37]. When it comes to the case of grid-level BESS, the SSBC can function as an active power controller at the lowest cost compared with other three MMCCs. Therefore, the cell number of the SSBC, N, is always the minimum among these four MMCCs.

1.1.3.2 Application of the SDBC

Compared to the SSBC, the zero-sequence current can flow in the three-phase clusters of SDBC because of the delta-connection. Consequently, the SDBC has the capability of controlling not only the positive-sequence reactive power but also the negative-sequence reactive power, which means that the SDBC can be used as a STATCOM. Even though the DSCC and the DSBC also have the circulating routes for the zero-sequence current, the SDBC has the minimum cell number in the same application case, which leads to a lower cost. As a result, the SDBC is mostly applied to the STATCOM [38]. In addition, the SDBC has the capability to control the positive-sequence reactive power, negative-sequence reactive power, and low-frequency active power at the same time. References [39] and [40] verified the experimental performance of the SDBC used in STATCOM with a downscaled model.

1.1.3.3 Application of the DSCC and the DSBC

The DSCC and the DSBC have almost the same circuit configuration and control method except for the types of cells. However, the application of them are different because of the difference in cell types. The DSCC is mainly applied to HVDC (high-voltage direct current) systems for high quality power transmission or to BTB (back-to-back) systems for changing the frequency between two different systems [41]. Also, it could be used as a multilevel inverter for medium-voltage motor drive [42] or for DC energy source grid connection [43].

Theoretically, the DSBC is able to be applied to most of the cases where the DSCC is used. However, the bridge cell has two more IGBT units than the chopper cell, which will increase the cost of the system. Therefore, the DSBC is only applied to some unique systems, such as the wind power systems and the PV systems. These systems are know as the PCS (power conditioning system) system [32], the DC-link voltage of which has a wide range of variation. The buck and boost function of the DSBC owing to the bridge cells is able to deal with this situation [44].

1.2 Research Objectives

The purpose of this dissertation is to introduce a novel three-phase PV inverter based on MMCC technologies that could solve the problems that the conventional two- or three-level inverter are facing. The main research objectives of this dissertation are:

- **A single-stage three-phase PV inverter with high AC output voltage and wide MPPT range** for utility-scale grid-connected PV systems based on the MMCC technologies. As explained in the previous section, the available MPPT range is narrow when the conventional three-level inverter is applied to utility-scale PV systems. Therefore, it is necessary to widen the MPPT range to increase the power efficiency. Even though a front-end boost converter can widen the MPPT range of the conventional three-level inverter, it can also cause more loss. In other words, a single-stage PV inverter is the best choice to decrease the loss. By using inverters based on MMCC technologies, the volume of the passive filters can be decreased. It is noteworthy that the MPPT control can be achieved with a PV simulator and a common method. However, it is not the main topic of this dissertation.

Therefore, a voltage source is used in this dissertation, instead.

- **Initial charging of the DC-capacitor voltage** in each cell of the MMCC technologies based PV inverter. Without charging the DC-capacitor voltage to a reference value, the MMCC circuit cannot operate the startup process. In the practical application, it is unrealistic to attach additional charging circuits to the capacitors in MMCCs in terms of cost and reliability. Therefore, it is necessary to propose an initial charging method without using additional components.

- **Test of the LVRT (low-voltage ride-through) capability** of the proposed PV inverter under the common grid faults. Since the proposed PV inverter is based on the MMCC technology, each capacitor may suffer from overvoltage/undervoltage during the fault, which may result in the destruction of power devices and/or operational failures. Similarly, the potential overcurrent during the fault may cause damage to power devices [45], [46]. Therefore, the LVRT capability of the proposed PV inverter should be tested.

- **Evaluation of the proposed PV inverter** in terms of cost and efficiency. Generally speaking, the selection of the cascaded cell (submodule) number of the MMCCs is crucial. When the MMCCs are applied to high-voltage applications such as high-voltage direct-current systems, the required cell number is mainly determined by the required voltage levels, and the number of cells can reach several hundreds, which eventually increases the cost and volume of the converter [32], [38]. Therefore, performance comparison between the proposed PV inverter using different number of cells may help to find out how to optimize the proposed PV inverter.

1.3 Dissertation Outline

The main body of this dissertation is divided into seven Chapters with one Appendix. The Chapters of the dissertation deal with the main ideas of the research efforts. A list of publications and achievements follows after the last Chapter.

- **Chapter 1** provides an introduction of the research topic that is explained in this dissertation. It starts with the research background that describes the development of PV energy, indicates the problems that the conventional two- or three-level PV

inverters are facing, and introduces the concept of MMCC. Research objectives follow the above section, which are carried out to solve the problems describe above. In the end, this Chapter offers an outline of the entire dissertation, where the main content of each Chapter is summarized for the convenience of readers.

- **Chapter 2** provides a detailed literature review of all the individual research topics which are discussed in each Chapter, including PV inverters, LVRT capability of MMCC inverters, and decreasing the cost and loss of MMCC inverters. The necessity of the research in this dissertation is revealed by the end of this Chapter.

- **Chapter 3** presents the novel three-phase PV inverter for utility-scale PV systems using multiple bidirectional choppers in detail. The circuit configuration, the operation principles, and the current control method based on three-phase d-q-0 transformation are explained with figures and theoretical equations. A new DC-capacitor voltage initial charging method is also proposed in this Chapter. The experimental verification is conducted using a downscaled model and the waveforms of the initial charging and different operational cases are shown. In the end, the remaining problem is discussed.

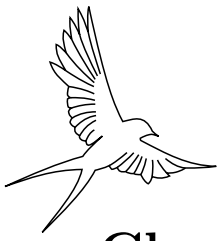
- **Chapter 4** proposes a new individual phase current control instead of the three-phase current control introduced in **Chapter 3** to solve the problem describe in the above Chapter. The new current control method is explained with block diagrams and theoretical equations. Similar to **Chapter 3**, the experimental verification is carried out using the same downscaled model to prove the reliability of the new current control method and the waveforms in different operation situations are shown. In addition, the loss breakdown and the efficiency comparison between the proposed PV inverter and the conventional three-level T-type inverter are also performed theoretically. In the end, the THD (total harmonic distortion) performance and the efficiency of the downscaled model are shown.

- **Chapter 5** presents the LVRT capability of the proposed PV inverter under the SLG (single-line-to-ground) and 3P (three-phase) faults. A theoretical analysis focusing on the LVRT behaviors of the proposed inverter, which includes the capacitor voltage fluctuation, the reason for the overmodulation and the current spikes, and the limit of the LVRT capability/safety operation zone under the SLG fault is also provided.

Since the analysis under the 3P can be done similar, it is left out in this dissertation. The LVRT capability is tested using the same downscaled model with a new AC power supply that can simulate the fault situations. The waveforms under different fault are shown and the comparison with the theoretical analysis results proves the reliability of the theoretical analysis.

- **Chapter 6** compares the performance of the proposed PV inverter with two chopper cells and three chopper cells in terms of loss, efficiency, THD performance, and experimental performance during steady and fault states to evaluate the chopper-cell number. The comparisons are based on theoretical calculation and experimental verification. The main purpose of this Chapter is to optimize the performance of the proposed PV inverter in practical application.

- **Chapter 7** conclude the entire research work and summarized all the results achieved in the previous Chapters. In addition, some future works are provided for the convenience of subsequent researchers.



Chapter 2

Literature Review

With the development of PV systems, the conventional two- or three-level inverters introduced in Chapter 1 are facing problems to satisfy the systems requirement. To solve the problems, different kinds of PV inverters have been studied. Each of them has different topology and unique application. However, they are not suitable to the application case in this dissertation, which is a utility-scale (1.5-kVdc) grid-connected PV system with a AC grid voltage of 6.6 kV.

This Chapter will provide a detailed literature review of all the research topics that will be discussed in the following Chapters. Specifically, it will start with a review of different PV inverter topologies to explain the necessity of the PV inverter topology proposed in this dissertation. Afterward, the importance of LVRT capability of the MMCC based inverter will be presented. Finally, some efforts on optimizing the MMCC systems will be demonstrated.

2.1 Topologies of PV Inverters

Basically, the PV inverters are classified into two types based on the power processing stages [47]:

- Single-stage inverters;
- Multiple-stage inverters.

As shown in Fig. 2.1, there is only one power processing stage in the single-stage inverter, whereas there are more than one power processing stage in the multiple-stage inverter. In

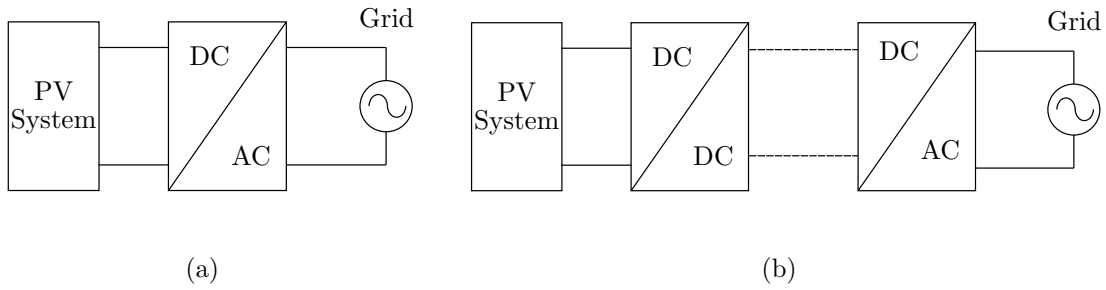


Figure 2.1: PV inverter types: a) single-stage inverter, b) multiple-stage inverter.

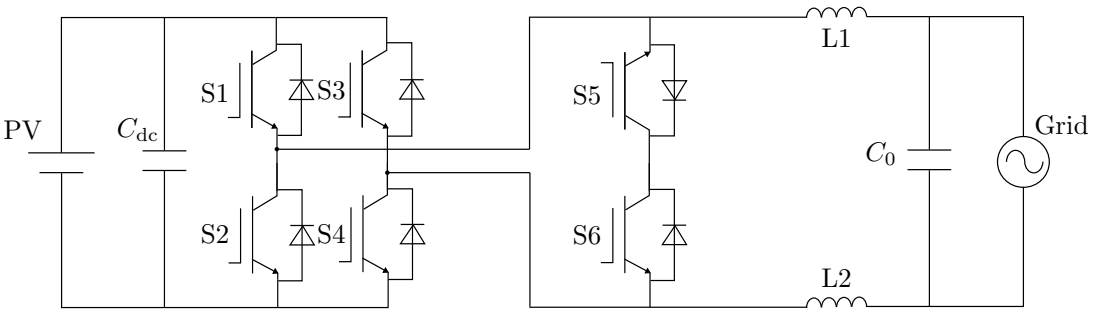


Figure 2.2: HERIC topology.

addition, surveys reveal that these two types of PV inverters are developed in different ways to adapt the change of the PV systems.

2.1.1 Single-stage Inverters

Because most topologies of the single-stage inverters are based on the conventional two- or three-level inverters [48], it is hard for them to widen the range of DC input voltage, which means it is hard to widen the MPPT range. Even though some single-stage boost or buck-boost inverter topologies proposed in [49]–[52] can amplify the DC input voltage for MPPT, these type of single-stage inverters still suffers from narrow range of DC input voltage, lower power capacity, and low power quality [48]. Therefore, a large amount of research has been carried out to increase the efficiency and the circuit reliability of the single-stage inverter. For example, the line frequency transformer is removed from the single-stage inverter because it accounts for 2 % of the total loss at peak efficiency and a large part of the the inverter's weight [53]. One of the famous single-stage inverter topologies is know as HERIC (high efficient and reliable inverter concept) topology [54], which is shown in Fig. 2.2. S5 is on in the positive half cycle of the grid voltage and off in the negative half cycle of it, whereas S6 is off in the positive half cycle of the grid voltage

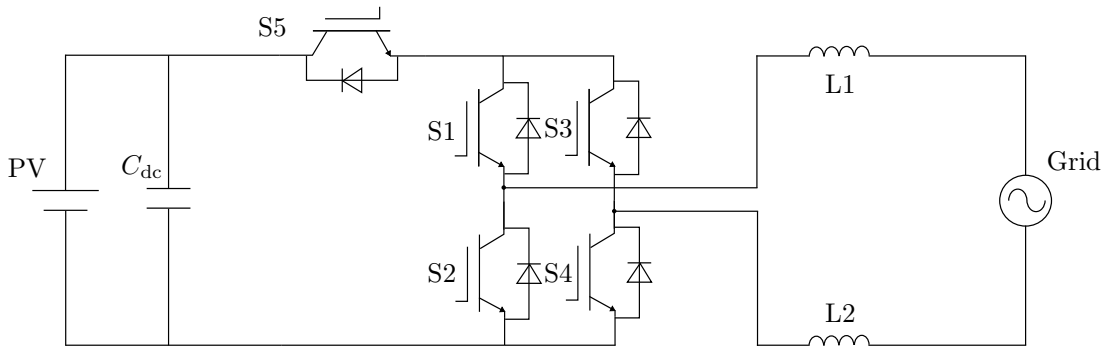


Figure 2.3: H5 topology.

and on in the negative half cycle of it. By this operational principle, the output current on the AC (grid) side during the current free-wheeling period will not flow in the diodes of the H-bridge inverter on the DC side, which means that the DC (PV) side is isolated from the AC (grid) side during this period. Another famous single-stage inverter topology is the H5 topology shown in Fig. 2.3 [54]. It is famous for its simple topology and can also isolate the PV system from the grid during the current free-wheeling period. In Fig. 2.3, S1 and S2 switch at grid frequency, while S3, S4, and S5 switch at higher frequency under the PWM (pulse-width modulation) control. It is noteworthy that the switching of S5 is synchronized with S3 and S4, which means that the PV system is isolated from the grid during the current free-wheeling period.

In summary, most of the single-stage inverters have transformerless topologies to achieve a higher frequency [55] and the topologies are of high reliability even without the isolation provided by the transformer. However, these transformerless high-efficiency single-stage PV inverters cannot be applied to the utility-scale PV systems because transformer is necessary to step-up the voltage of the PV systems to the voltage level of the medium-voltage AC grids [56]–[58], e.g., 6.6 kV in Japan or 13.8 kV in US.

2.1.2 Multiple-stage Inverters

On the other hand, the multiple-stage inverters attached with front-end boost converters can be applied instead of the single-stage inverters to widen the MPPT range [59]–[61]. The conventional non-isolated boost converters are widely used in utility-scale PV systems (e.g., in [30]), whereas the introduction of the boost converters may result in increased

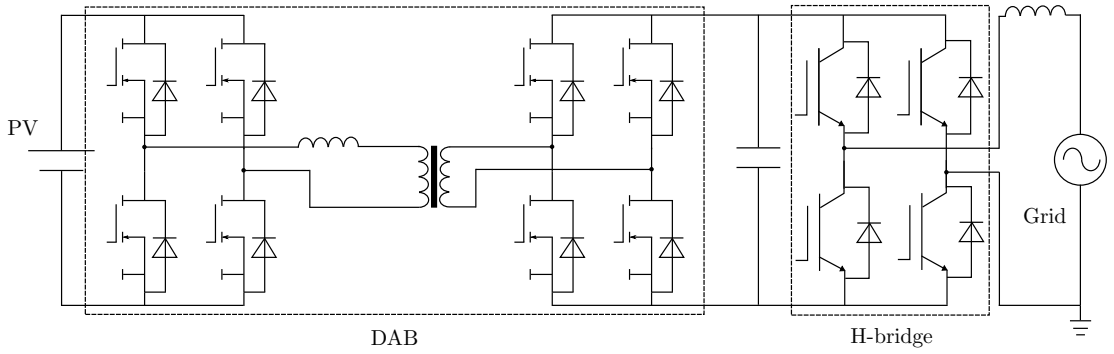


Figure 2.4: DAB application in PV systems.

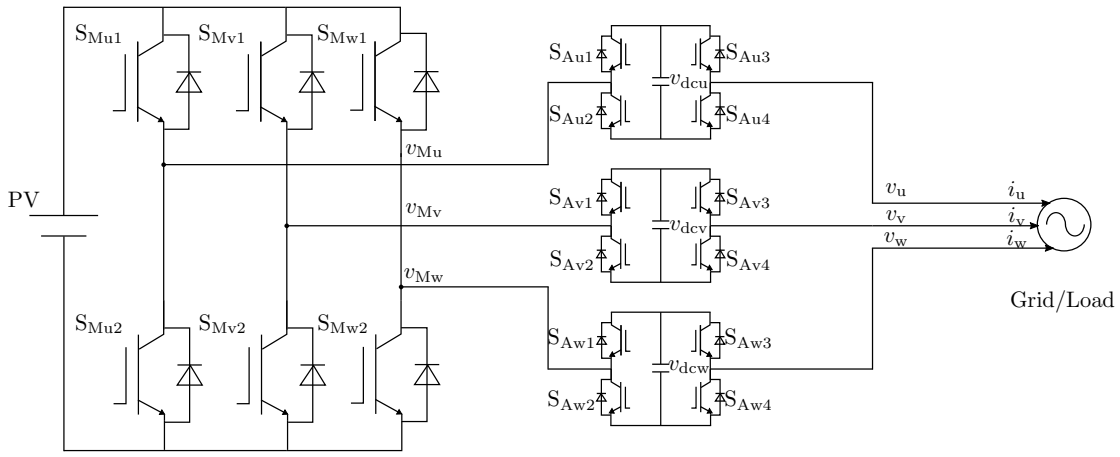


Figure 2.5: Gradational voltage inverter.

cost and loss. A method of applying string mini-boost converters at the input of the PV inverter was presented to widen the available MPPT range [62]. Specifically, the mini-boost converters are applied to every string of the PV array and boost the different DC input voltages of each PV array to the same voltage, which is acceptable for the PV inverter input. However, this may increase the complexity of the control of the entire system, especially in utility-scale PV systems with many strings. DAB (dual-active-bridge) converters have also been applied to some PV systems owing to their high efficiency, small size, and flexible connection [63]–[65]. However, the DAB converter is also connected with a DC-AC inverter as a part of a multiple-stage inverter as shown in Fig. 2.4, which will sacrifice the high efficiency and the flexibility of the DAB converters. In addition, the implementation would be more difficult as the system scales up.

Table 2.1: Differences between gradational voltage inverter and proposed PV inverter.

	Gradational voltage inverter	Proposed PV inverter
Cell structure	1 bridge cell	Multiple chopper cells
Neutral line	No	Yes
Main conv. control method	SVPWM	Fixed duty
Aux. conv. control method	SVPWM	Phase-shifted PWM
Main conv. switching frequency	1 kHz	50 Hz
Aux. conv. switching frequency	10 kHz	7.2 kHz

2.1.3 Gradational Voltage Inverters

An MMCC based single-stage inverter is proposed by Mitsubishi Electric [66] and the circuit configuration is shown in Fig. 2.5. In this inverter, a bridge cell is cascaded connected to a conventional two-level inverter (main converter) in each phase. The bridge cell works as an auxiliary converter switching at a higher frequency, which can decrease the high frequency harmonics components. In addition, the SVPWM (space-vector pulse-width modulation) control is used. The main idea of the PV inverter proposed in this dissertation is similar to this gradational voltage inverter. However, there are many differences between them, which are concluded in the following table. The detail of the content in Table 2.1 will be illustrated later.

In order to widen the MPPT range and achieve the high efficiency at the same time, a new single-stage three-phase utility-scale MMCC technology based PV inverter is proposed in this dissertation. It is composed of a three-phase inverter and a three-phase line-frequency transformer with a three-limb core working as a step-up transformer for grid connection. The inverter is composed of a main converter, which is a bidirectional chopper, and an auxiliary converter, which is composed of multiple chopper cells. The detail of it will be described in Chapters 3 and 4.

2.2 LVRT Capability of MMCC Topologies

The LVRT capability of the MMCC topologies is always an issue for the MMCC rectifiers/inverters because of their complex operation principles and controls. It is required that the MMCC rectifiers/inverters should be able to maintain the grid-connected operation for several fundamental cycles during the fault and restore the normal operation after the fault is cleared. However, the floating capacitor in the cells may suffer from

overvoltage/undervoltage during the fault which may result in the destruction of power devices and/or operational failures. Similarly, the potential overcurrent during the fault may cause damage to power devices, especially the MOSFETs (metal-oxide-semiconductor field-effect transistors) and the IGBTs [45], [46]. Among these problems, the unbalance between the DC-capacitor voltages of each phase cluster of the MMCC during the grid faults attracts most concerns [67]–[71].

So far, a significant amount of research has been carried out for verifying the LVRT capability of various MMCC inverters. A combination of ZSV (zero-sequence voltage) injection and NSC (negative-sequence current) injection was proposed in [72] for the MMCC-SSBC to regulate each capacitor voltage during the grid fault. Specifically, the MMCC-SSBC is used as a STATCOM in [72]. By the specific ZSV and NSC injection, the modulation index and the output peak current can be limited so that over-modulation and overcurrent will not happen while the control is trying to balance the DC-capacitor voltages.

In [73], the LVRT capability was studied for MMCC-SDBC. A flexible DC-capacitor voltage balancing control was proposed to improve the LVRT capability of MMCC-SDBC in the DERs (distributed energy resources) systems. By adjusting the proportion of NSC and ZSC (zero-sequence current) in the injection current, the MMCC-SDBC is able to operate under unbalance power condition caused by the grid faults. In addition, it is shown by the comparisons that the LVRT capability of MMCC-SDBC is worse than that of MMCC-SSBC, even though the balancing capability of MMCC-SDBC is better.

In [74], the LVRT capability was studied for HCC (hybrid cascade converter). The HCC topology is shown in Fig. 2.6 and bridge cells shown in Fig. 1.7e are used in the cell blocks. By replacing some of bridge cells in SSBC with a three-phase two-level cell, the switching loss of HCC was reduced significantly compared with that of SSBC. In addition, a new control block was added to the previous control and the LVRT capability of the HCC was proved well.

Since the proposed inverter is based on the MMCC technology, i.e., using the cascaded bidirectional chopper cells, the LVRT capability of it under the grid faults should be addressed for improving the reliability of the inverter. It is also necessary to check out whether the proposed DC-capacitor voltage control is able to handle the voltage fluctuation caused by the unbalance power during the grid faults.

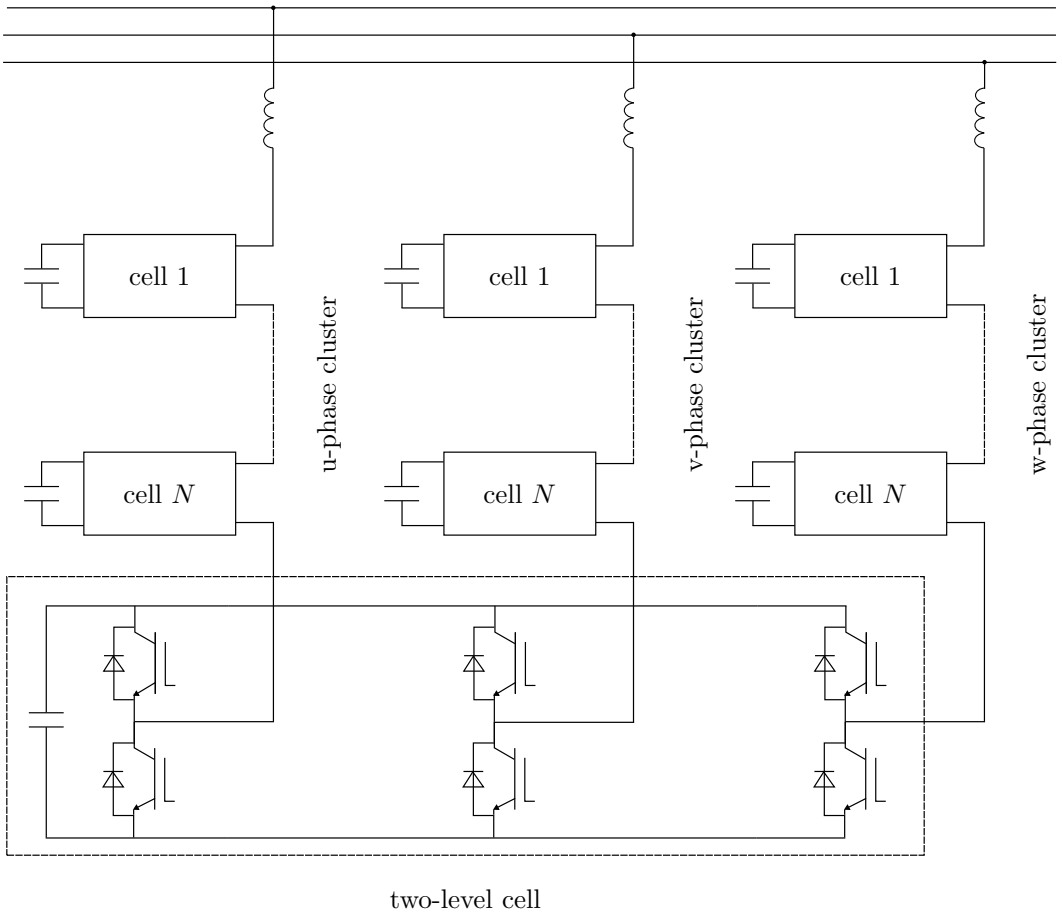


Figure 2.6: HCC topology.

2.3 Loss and Cost Decreasing of MMCC Topologies

Generally speaking, the selection of the cascaded cell (submodule) number of the MMCCs is crucial. When the MMCCs are applied to high-voltage applications such as HVDC systems, the required cell number is mainly determined by the required voltage levels, and the number of cells can reach several hundreds, which eventually increases the cost and volume of the converter [32], [75].

A significant amount of research has been carried out to reduce the cost and volume of the MMCCs. Among them, some new MMCC topologies are proposed. The HCC topology introduced above [74] is also a topology to reduce the cost and volume of the SSBC topology. In addition, the switching loss is greatly reduced without sacrificing the output performance. Another new MMCC topology is used in [76] as an active power filter. The new topology is similar to that of SSBC except that the chopper cells are used instead of bridge cells, which can save half of the switches for each cell. In addition, one of the phase cluster is replaced by a capacitor. By using this three-phase two-leg topology, the cost and volume of the converter could be reduced significantly. However, it sacrifices the performance of the active filter and large size inductors need to be used. In addition, this work stops at the simulation stage.

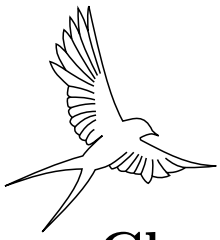
SiC based MMCC are used for HVDC in [77]. By using SiC devices, capacitance of the chopper cells decreased by 17 %. SiC devices are famous for their high efficiency and the calculation showed that about 50 % semiconductor loss reduction was achieved. The volume of submodule decreased by 21 % and the weight decreased by 14 %. However, the price of the SiC device is usually twice or three times of that of the IGBT.

A capacitor voltage oscillation reduction method by using third-order harmonic ZSC is proposed for MMCC-SDBC in [78]. As a result, the required capacitance and the capacitor bank volume decreased by 20 % without increasing the semiconductor loss. However, this work also only proceeded to the theoretical stage.

In summary, so many efforts have been made to reduce the cost and volume of the MMCC converters without sacrificing the advantages of the MMCC topologies. Therefore, it is necessary to find out whether the proposed PV inverter can be optimized by reducing the cost and volume of it. The detail of it will be described in Chapter 6.

2.4 Conclusion

This Chapter provides a literature review on all the topics that will be discussed in the following Chapters. The overview of the PV inverter topologies reveals the necessity of the PV inverter proposed in this dissertation. The introduction of the LVRT capability of the MMCC rectifiers/inverters emphasizes that the LVRT capability of the proposed PVinverter under the grid faults should be addressed for improving the reliability of the inverter. The summary of other efforts in reducing the cost and volume of the MMCC leads to the content of Chapter 6, which is the evaluation of cell number used in the proposed PV inverter.



Chapter 3

Three-phase PV Inverter with Conventional d-q-0 Control

This Chapter will present the proposed single-stage three-phase inverter for utility-scale PV systems where multiple cascaded bidirectional choppers and a three-phase line-frequency transformer transformer with a three-limb core are used. The circuit configuration and the operation principles are explained in detail with figures and mathematical equations. The conventional control method based on three-phase d-q-0 transformation, which is the first proposed control method of this PV inverter, is also illustrated. The validity of the circuit configuration, the operation principles, and the control method are verified by the simulation in the software PSCAD® first and the experimental verifications are carried out using a downscaled model, finally.

3.1 Proposed Circuit Configuration

The circuit configuration of the proposed three-phase PV inverter is shown as Fig. 3.1. It is composed of a three-phase inverter and a three-phase line-frequency transformer with a three-limb core working as a step-up transformer for grid connection. Since three phases share the same circuit configuration and control method, the following explanation will focus on the u-phase inverter. The inverter is composed of a main converter, which is equivalent to a single bidirectional chopper, and an auxiliary converter, which is composed of multiple cascaded connected bidirectional chopper cells. Unlike the multiple-stage inverter, neither the main converter nor the auxiliary converter can work independently.

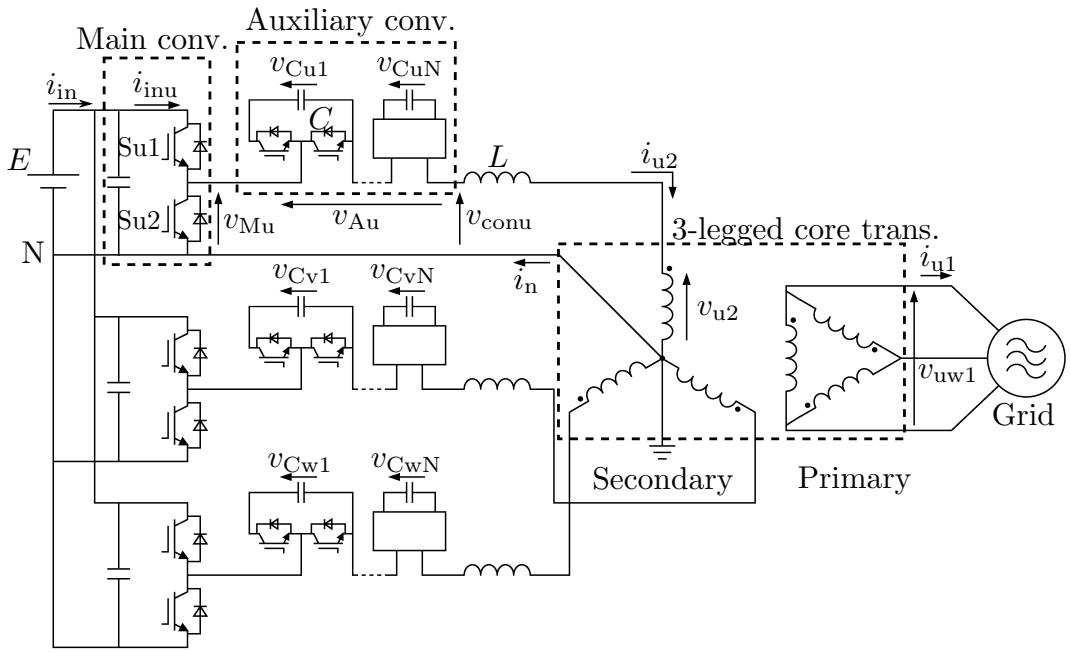


Figure 3.1: Circuit configuration of three-phase PV inverter based on multiple bidirectional choppers for utility-scale PV systems.

Therefore, the proposed inverter is still a single-stage inverter. The number of the chopper cells could be set to any natural number and was set to $N = 3$ in Chapter 3 and Chapter 4. The main converter switches at a frequency of 50 Hz to match the grid frequency, whereas each chopper cell of the auxiliary converter switches at a much higher frequency, e.g., 7.2 kHz in Chapters 3 and Chapter 4, and behave as an active-power-filter to reduce the high-frequency harmonic components. The phase-shifted PWM is applied to the auxiliary converter to reduce the harmonic voltage/current. The AC output side of the inverter is connected to the secondary side of the three-phase transformer with a three-limb core via an AC-link inductor. The primary side (i.e., grid side) of the three-phase transformer is in Δ connection and the secondary side (i.e., inverter side) is in Y connection. Normally, the Δ connection side is the low voltage side and the the Y connection side is the high voltage side. However, there is no route for DC current in Δ connection structure. Therefore, the DC side has to be in Y connection structure. On the other hand, the Δ connection structure is necessary for the third-order harmonics current to achieve a sinusoidal flux waveform because of the hysteresis loop of the three-limb core. Therefore, the Y-Δ connection with neutral line on the secondary side is applied to the proposed inverter. The Y-Y connection with neutral line on the secondary side is also available for

steady-state operation. However, there will be no route for third-order harmonic if the inverter stops switching, which will happen at the moment before disconnection from the grid. Therefore, it is not applied to the proposed circuit.

The proposed circuit of the three-phase inverter is based on the one presented in [79], but the neutral terminal of the Y-connected windings, O, is directly connected to the negative terminal of the PV array, N, while it is floated in [79]. The proposed circuit is characterized in that a DC current flows to the mid-point of the transformer for boost operation, while it does not affect the transformer operation because it corresponds to the ZSC in the three-phase circuit. Specifically, the three-limb core has an infinite magnetic impedance against the electromagnetic force produced by the DC current ideally. Therefore, the DC current has no effect on the transformer operation. As a result, the inverter voltage could rise to $\sqrt{3}$ times that of the conventional 2- or 3-level inverter with the same DC input voltage. In addition, the DC current will be used for the control of each DC-capacitor voltage. The AC inductor could be eliminated from the circuit if the leakage inductance is large enough. As a result, a smaller RMS current and a wider available MPPT range could be satisfied simultaneously by the proposed inverter circuit. Furthermore, owing to the direct connection between the negative terminal of the PV array and the ground, no high-frequency circulating current flows via the stray capacitance, which makes the parallel operation of the inverters easier. In summary, the proposed inverter can achieve boost operation and zero circulating current simultaneously, which is not achievable by the conventional inverter such as the Z-source inverter [80], where only boost operation is achievable.

The variables in Fig. 3.1 are described as follows. E is the DC voltage corresponding to the PV array voltage, v_{Mu} is the main converter output voltage, v_{Cu1} and v_{CuN} are the DC-capacitor voltages, v_{Au} is the auxiliary converter output voltage, v_{conu} is the inverter line-to-neutral output voltage, v_{u2} is the line-to-neutral secondary voltage of the transformer, v_{uw1} is the line-to-line grid voltage, i_{inu} is the DC input current, i_{n} is the neutral current, i_{u1} is the grid current and i_{u2} is the inductor current. The phases of v_{uw1} and v_{u2} are the same with the assumption that an ideal transformer is used.

3.2 Operation Principles

Because the operation principles of the three phases are identical, only those of the u-phase inverter will be described in this section. It is noteworthy that the operation principles explained in Section 3.1 are based on the cases where active power control is implemented. In reactive power control cases, some of the principles could be broken. Since it is not the main point of this dissertation, the explanation of reactive power control operation principles is not included. In active power control cases, the following assumptions are made.

- The voltage of the inductor including the leakage inductance, the on-state voltage, and the resistance and inductance of the leading wires are zero;
- The fundamental-frequency component in i_{u2} is in phase with that in v_{u2};
- Switching-ripple components in v_{Au} and i_{u2} are zero.

The following equation is obtained when the first assumption holds true:

$$v_{\mathrm{Au}} = v_{\mathrm{Mu}} - v_{\mathrm{conu}} = v_{\mathrm{Mu}} - v_{\mathrm{u2}}. \tag{3.1}$$

In (3.1), v_{u2} is given by

$$v_{\mathrm{u2}} = \sqrt{2}V_{\mathrm{ac}} \cos\theta = \sqrt{2}V_{\mathrm{ac}} \cos 2\pi f_{\mathrm{SM}} t, \tag{3.2}$$

where V_{ac} is the RMS value of the line-to-neutral secondary voltage and f_{SM} is the grid frequency (50 Hz). It is noteworthy that V_{ac} is obtained as

$$V_{\mathrm{ac}} = V_{\mathrm{d}}/\sqrt{3}, \tag{3.3}$$

where V_{d} is the d-axis component of the transformer secondary voltage used in PLL (Phase locked loop), and it is a constant in this study. Further, V_{ac} is expressed as

$$V_{\mathrm{ac}} = V_{\mathrm{grid}}/(\sqrt{3}a), \tag{3.4}$$

where V_{grid} is the RMS value of the grid line-to-line voltage and a is the transformer voltage ratio. With the second assumption, the inverter could achieve unity-power-factor

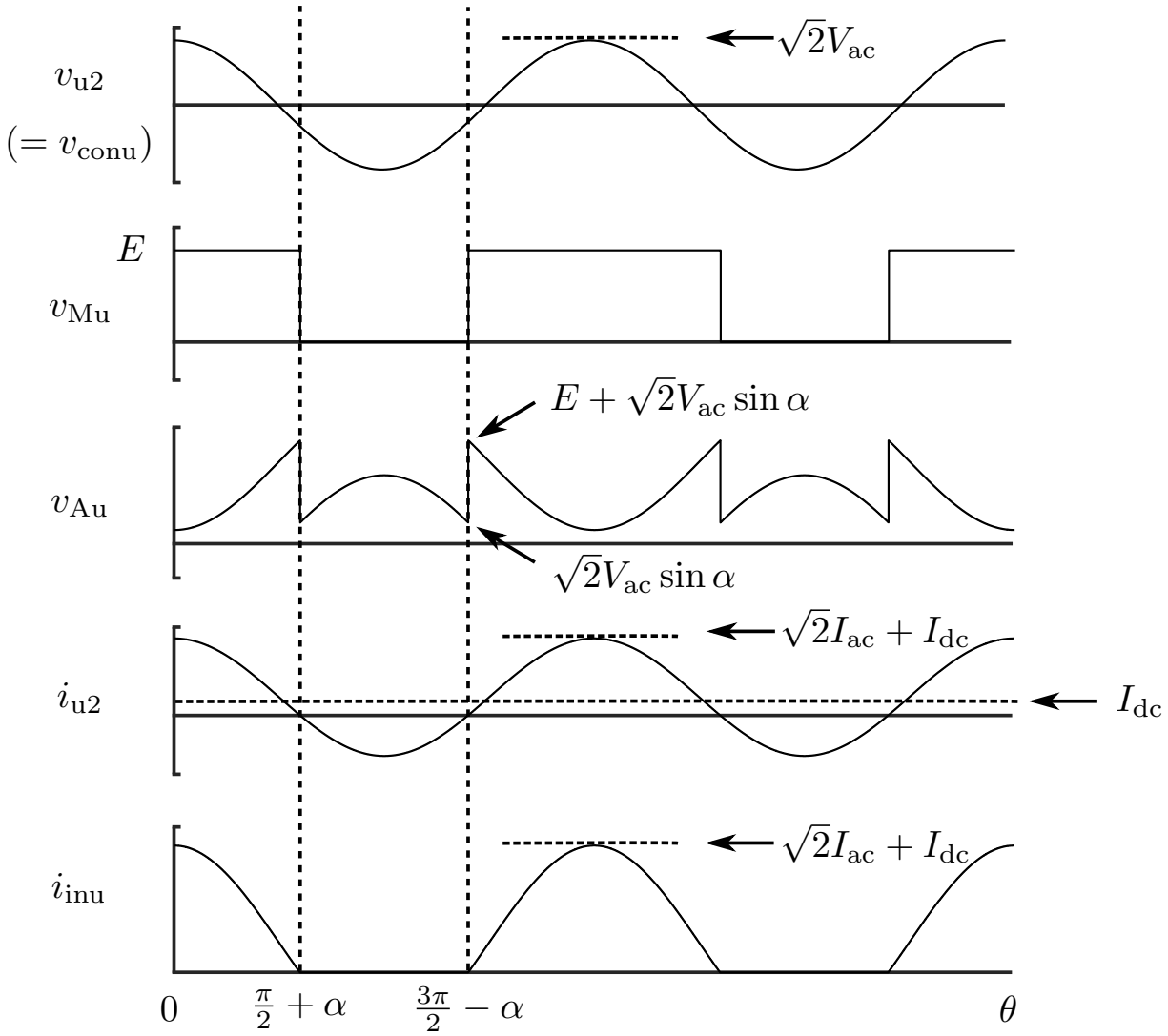


Figure 3.2: Ideal u-phase voltage and current waveforms of Fig. 3.1 circuit with ZCS.

operation. The third assumption could be satisfied by increasing the number of the chopper cells and/or the switching frequency. The ideal voltage and current waveforms of the u-phase inverter are shown in Fig. 3.2 with the three assumptions above, where the ZCS (zero-current switching) is achieved in the main converter. On the other hand, the voltage and current waveforms without the ZCS are shown in Fig. 3.3. The difference between them will be explained in the following subsections.

3.2.1 Operation Principles of Main Converter

The main converter voltage, v_{Mu}, is a 50-Hz square-wave voltage, where the fundamental-frequency component is in phase with v_{u2} whereas their amplitudes are different from each

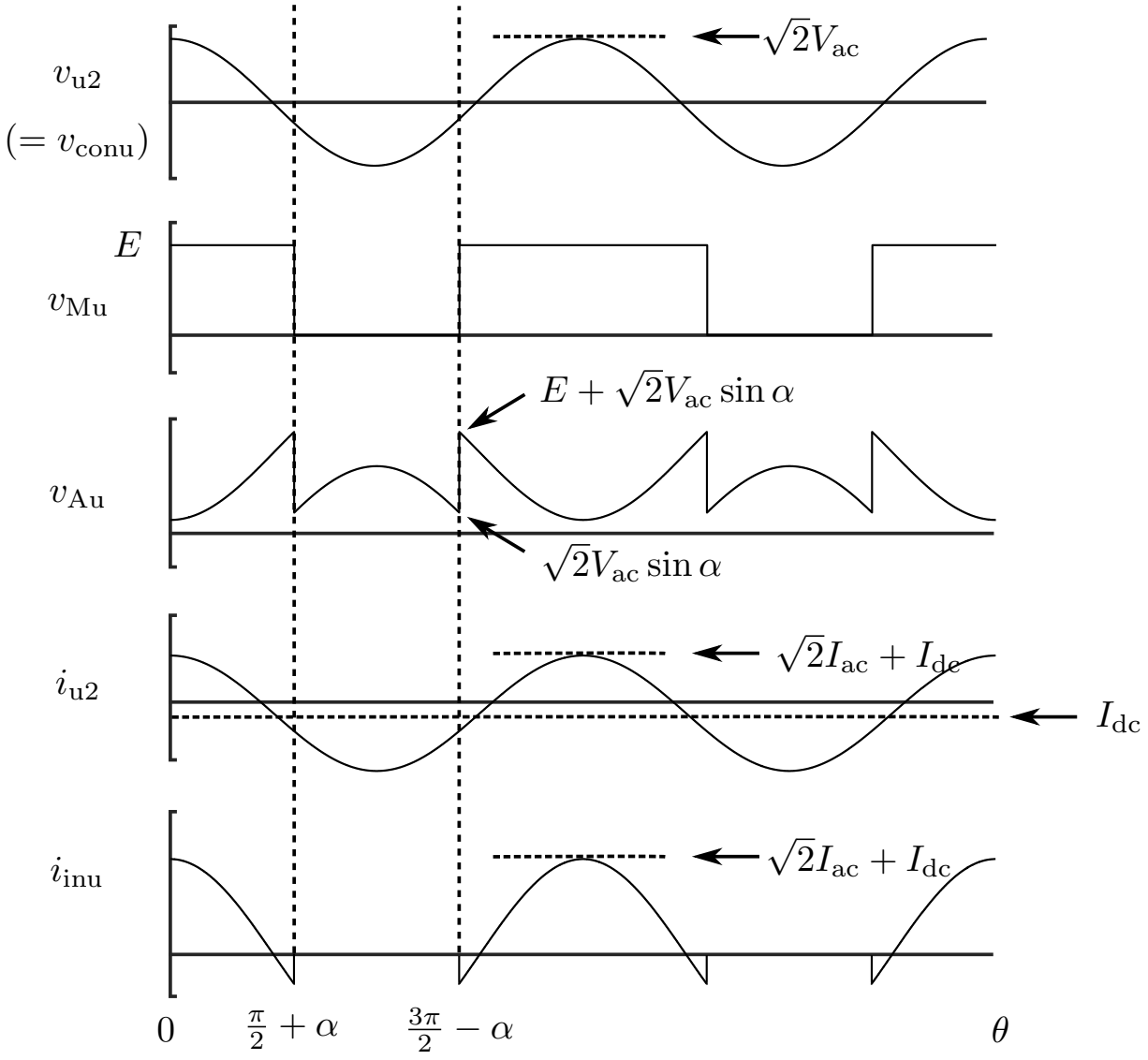


Figure 3.3: Ideal u-phase voltage and current waveforms of Fig. 3.1 circuit without ZCS.

other. Specifically, v_{Mu} is given by

$$v_{\mathrm{Mu}} = \begin{cases} E & (0 \leq \theta \leq \frac{\pi}{2} + \alpha, \frac{3\pi}{2} - \alpha \leq \theta \leq 2\pi) \\ 0 & (\frac{\pi}{2} + \alpha < \theta < \frac{3\pi}{2} - \alpha), \end{cases} \tag{3.5}$$

where α is the turn-on (turn-off) angle of the main converter.

Furthermore, the relationship $v_{\mathrm{Au}} \geq 0$ should always hold because a chopper cell can only produce a voltage that is equal to or higher than zero. With (3.1), (3.2), (3.5), and the relationship $v_{\mathrm{Au}} \geq 0$, E and α should satisfy the following relationships:

$$E \geq \sqrt{2} V_{\mathrm{ac}}, \tag{3.6}$$

$$0 \leq \alpha \leq \frac{\pi}{2}. \tag{3.7}$$

According to (3.6), the minimum DC input voltage, E_{min}, is expressed by

$$E_{\mathrm{min}} = \sqrt{2} V_{\mathrm{ac}}. \tag{3.8}$$

It should be noted that there is no upper limit of E as long as it is lower than the voltage ratings of the power devices in the inverter circuit.

On the other hand, α could be any value as long as (3.7) holds. In Chapter 3 and Chapter 4, α is set according to (3.22) when (3.6) and (3.23) hold for achieving the ZCS of the power devices used in the main converter and it is set to zero when (3.24) holds for minimizing the converter loss, where ZCS is not achievable. The detailed explanation will be provided in the following subsections.

3.2.2 Operating Principles of Auxiliary Converter

According to (3.1), (3.2), and (3.5), v_{Au} is derived as

$$v_{\mathrm{Au}} = \begin{cases} E - \sqrt{2} V_{\mathrm{ac}} \cos\theta & (0 \leq \theta \leq \frac{\pi}{2} + \alpha, \frac{3\pi}{2} - \alpha \leq \theta \leq 2\pi) \\ -\sqrt{2} V_{\mathrm{ac}} \cos\theta & (\frac{\pi}{2} + \alpha < \theta < \frac{3\pi}{2} - \alpha). \end{cases} \tag{3.9}$$

The maximum value of v_{Au}, $(v_{\mathrm{Au}})_{\max}$, is obtained from (3.9) and Fig. 3.2 as

$$(v_{\mathrm{Au}})_{\max} = E + \sqrt{2}V_{\mathrm{ac}} \sin\alpha. \tag{3.10}$$

It is obvious from (3.10) and Fig. 3.2 that the minimum DC-capacitor voltage, v_{Cmin}, should satisfy the following relationship:

$$v_{\mathrm{Cmin}} \geq (E + \sqrt{2}V_{\mathrm{ac}} \sin\alpha)/N, \tag{3.11}$$

where N is the number of chopper cells per phase. v_{Au} is the sum of the high-frequency component, $(v_{\mathrm{Au}})_{\mathrm{ripple}}$, the DC component, $(v_{\mathrm{Au}})_{\mathrm{dc}}$, and the fundamental-frequency component, $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$, which is shown as

$$v_{\mathrm{Au}} = (v_{\mathrm{Au}})_{\mathrm{ripple}} + (v_{\mathrm{Au}})_{\mathrm{dc}} + (v_{\mathrm{Au}})_{50\,\mathrm{Hz}}. \tag{3.12}$$

$(v_{\mathrm{Au}})_{\mathrm{ripple}}$ corresponds to the harmonic components included in v_{Mu}. In other words, the auxiliary converter works as a series-type active power filter to reduce the high-frequency components in v_{conu}. From (3.1) and (3.2), $(v_{\mathrm{Au}})_{\mathrm{dc}}$ equals the DC component included in v_{Mu}:

$$(v_{\mathrm{Au}})_{\mathrm{dc}} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{Mu}}\, d\theta = E(\frac{1}{2} + \frac{\alpha}{\pi}). \tag{3.13}$$

Meanwhile, equations (3.1) and (3.2) show that $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ is given by a difference between the fundamental frequency components included in v_{Mu}, $(v_{\mathrm{Mu}})_{50\,\mathrm{Hz}}$, and v_{u2}. $(v_{\mathrm{Mu}})_{50\,\mathrm{Hz}}$ is calculated from (3.5) as follows:

$$(v_{\mathrm{Mu}})_{50\,\mathrm{Hz}} = (\frac{1}{\pi}\int_0^{2\pi} v_{\mathrm{Mu}} \sin\phi\, d\phi)\cos\theta = \frac{2E}{\pi}\cos\alpha\cos\theta. \tag{3.14}$$

From (3.1), (3.2) and (3.14), $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ is derived as

$$(v_{\mathrm{Au}})_{50\,\mathrm{Hz}} = (\frac{2E}{\pi}\cos\alpha - \sqrt{2}V_{\mathrm{ac}})\cos\theta. \tag{3.15}$$

Equations (3.2) and (3.15) imply that $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ is in phase with v_{u2} or 180° out of phase with each other which depends on the values of E, α and V_{ac}.

3.2.3 Derivation of α

In this dissertation, the DC input voltage is considered to be low if (3.6) and (3.23) hold, and it is considered to be high if (3.24) holds.

3.2.3.1 Case of Low DC Input Voltage

The coefficient of $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ given by (3.15) is negative when the following relationship holds:

$$E \leq \frac{\sqrt{2}\pi V_{\mathrm{ac}}}{2\cos\alpha}. \tag{3.16}$$

It is evident from (3.2), (3.15) and (3.16) that $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ and v_{u2} are 180° out of phase with each other, and the fundamental-frequency component of i_{u2} is in phase with v_{u2} based on the third assumption above. Therefore, the product of v_{u2} and the fundamental-frequency component in i_{u2} produces negative power. This implies that positive power must be produced between $(v_{\mathrm{Au}})_{\mathrm{dc}}$ and the DC component in i_{u2} for the power balance in each chopper. As a result, i_{u2} is expressed as

$$i_{\mathrm{u2}} = \sqrt{2}I_{\mathrm{ac}}\cos\theta + I_{\mathrm{dc}}, \tag{3.17}$$

where I_{ac} is the RMS value of the fundamental-frequency component and I_{dc} represents the DC component ($I_{\mathrm{dc}} > 0$). A method of calculating the value of α to achieve the ZCS of the main converter will be explained in the following. If the DC input current i_{inu} is zero at $\pi + \alpha$ and $2\pi - \alpha$ as shown in Fig. 3.2, the ZCS of the power devices used in the main converter is achieved. The following equation holds between I_{dc} and I_{ac} because the relationship $i_{\mathrm{u2}}(\theta)\,|_{\theta=\pi+\alpha} = 0$ holds in (3.17).

$$I_{\mathrm{dc}} = \sqrt{2}I_{\mathrm{ac}}\sin\alpha. \tag{3.18}$$

The DC input power of u-phase, P_{inu}, is calculated as

$$\begin{aligned} P_{\text{inu}} &= \frac{1}{2\pi}\int_{0}^{2\pi} E i_{\text{inu}}\, d\theta \\ &= \frac{1}{2\pi}\int_{-\alpha}^{\pi+\alpha} E(\sqrt{2}I_{\text{ac}}\cos\theta + I_{\text{dc}})\, d\theta \\ &= \frac{1}{2\pi}\int_{-\alpha}^{\pi+\alpha} E(\sqrt{2}I_{\text{ac}}\cos\theta + \sqrt{2}I_{\text{ac}}\sin\alpha)\, d\theta \\ &= \sqrt{2}EI_{\text{ac}}(\frac{\cos\alpha}{\pi} + \frac{\pi+2\alpha}{2\pi}\sin\alpha). \end{aligned} \tag{3.19}$$

On the other hand, the AC output power of u-phase is obtained from (3.2) and (3.17) as

$$P_{\text{outu}} = V_{\text{ac}}I_{\text{ac}}. \tag{3.20}$$

The relationship $P_{\text{inu}} = P_{\text{outu}}$ is always true in steady-state conditions so that the following equation is obtained as

$$\sqrt{2}EI_{\text{ac}}(\frac{\cos\alpha}{\pi} + \frac{\pi+2\alpha}{2\pi}\sin\alpha) = V_{\text{ac}}I_{\text{ac}}. \tag{3.21}$$

α is obtained by solving (3.21) with the reasonable approximations of $\sin\alpha \cong \alpha$ and $\cos\alpha \cong 1 - \frac{\alpha^2}{2}$ as

$$\alpha = -\frac{\pi}{2} + \frac{1}{2}\sqrt{\pi^2 - 8 + 4\pi\frac{\sqrt{2}V_{\text{ac}}}{E}}, \tag{3.22}$$

where (3.7) is considered. Equation (3.22) indicates that the value of α is determined by V_{ac} and E and irrelevant to power (i.e., current). In (3.22), the following relationship should hold to satisfy (3.7) as

$$\begin{aligned} -8 + 4\pi\frac{\sqrt{2}V_{\text{ac}}}{E} &\geq 0 \\ E &\leq \frac{\sqrt{2}\pi V_{\text{ac}}}{2}. \end{aligned} \tag{3.23}$$

In conclusion, the ZCS of the main converter can be achieved under the voltage ranges given by (3.6) and (3.23).

3.2.3.2 Case of High DC Input Voltage

The coefficient of $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ given by (3.15) is positive when the following relationship holds:

$$E \geq \frac{\sqrt{2}\pi V_{\mathrm{ac}}}{2}. \tag{3.24}$$

When the DC input voltage is high, I_{dc} in (3.17) should be negative to achieve $P_{\mathrm{in}} = P_{\mathrm{out}}$. Fig. 3.3 shows the ideal u-phase voltage and current waveforms when (3.24) holds where the ZCS cannot be achieved because of the negative value of I_{dc}. In this case, the value of α could be set to any value specified by (3.7). On the other hand, it is obvious from Fig. 3.3 that the increased α results in the increased absolute value of I_{dc}, which increases the conduction loss and the switching loss of the inverter. Hence, α is set to zero when E is specified by (3.24) to minimize I_{dc}. The following will describe how to derive I_{dc} when (3.24) and $\alpha = 0$ holds. When the ZCS is not achievable, the relationship (3.18) no longer holds, and it is changed to:

$$I_{\mathrm{dc}} = kI_{\mathrm{ac}}, \tag{3.25}$$

where k is the variable describing the ratio between I_{dc} and I_{ac}, and the conclusion that k is negative could be obtained by logical analysis. It is clear that $I_{\mathrm{dc}} = 0$ is true at the edge case of low DC input voltage and high DC input voltage, which also means that $k = 0$ holds according to (3.25). As E becomes larger in the high DC input voltage case, k has to become negative to maintain the power balance between the input and the output power according to (3.26) and (3.20). The following mathematical analysis will yield the same conclusion, which is described by (3.24) and (3.29). With k defined by (3.25), (3.19) is changed to

$$\begin{aligned} P_{\mathrm{inu}} &= \frac{1}{2\pi}\int_{0}^{2\pi} Ei_{\mathrm{inu}}\,d\theta \\ &= \frac{1}{2\pi}\int_{-\alpha}^{\pi+\alpha} E(\sqrt{2}I_{\mathrm{ac}}\cos\theta + I_{\mathrm{dc}})\,d\theta \\ &= \frac{1}{2\pi}\int_{-\alpha}^{\pi+\alpha} E(\sqrt{2}I_{\mathrm{ac}}\cos\theta + kI_{\mathrm{ac}})\,d\theta \\ &= EI_{\mathrm{ac}}(\frac{\sqrt{2}\cos\alpha}{\pi} + \frac{k(\pi+2\alpha)}{2\pi}). \end{aligned} \tag{3.26}$$

According to (3.20), (3.21) is changed to

$$EI_{\mathrm{ac}}(\frac{\sqrt{2}\cos\alpha}{\pi}+\frac{k(\pi+2\alpha)}{2\pi})=V_{\mathrm{ac}}I_{\mathrm{ac}}. \tag{3.27}$$

α could be obtained by solving (3.27) using the same approximations for solving (3.21). Finally, α is obtained as

$$\alpha=\frac{k}{\sqrt{2}}+\sqrt{\frac{k^2}{2}+\frac{\sqrt{2}k\pi}{2}+2-\frac{\sqrt{2}\pi V_{\mathrm{ac}}}{E}}. \tag{3.28}$$

Since $\alpha=0$ should hold in order to reduce the loss of the inverter as mentioned above, the value of k could be obtained from (3.28) as

$$k=\frac{2V_{\mathrm{ac}}}{E}-\frac{2\sqrt{2}}{\pi}, \tag{3.29}$$

Thus, the value of I_{dc} is obtained from (3.25) and (3.29) as

$$I_{\mathrm{dc}}=(\frac{2V_{\mathrm{ac}}}{E}-\frac{2\sqrt{2}}{\pi})I_{\mathrm{ac}}. \tag{3.30}$$

3.2.3.3 Conclusion

Concluding from the analysis above, the value of α and I_{dc} can be derived as:

$$\alpha=\begin{cases}-\frac{\pi}{2}+\frac{1}{2}\sqrt{\pi^2-8+4\pi\frac{\sqrt{2}V_{\mathrm{ac}}}{E}} & \text{(ZCS achievable)}\\ 0 & \text{(ZCS not achievable),}\end{cases} \tag{3.31}$$

$$I_{\mathrm{dc}}=\frac{2\pi I_{\mathrm{ac}}}{\pi+2\alpha}(\frac{V_{\mathrm{ac}}}{E}-\frac{\sqrt{2}}{\pi}\cos\alpha). \tag{3.32}$$

3.2.4 Comparison of Minimum DC Input Voltage

It is known that the conventional two- or three-level three-phase PWM inverter produces the maximum line-to-neutral voltage of $0.5E$ without the ZSV injection. With the ZSV injection, it can be increased to $2/\sqrt{3}(=1.15)$ times of $0.5E$. Therefore, the relationship between the minimum DC input voltage of the two- or three-level PWM inverter and the

grid voltage with the ZSV injection is shown as

$$E_{\min} = \sqrt{6}V_{\mathrm{ac}}. \tag{3.33}$$

Meanwhile, the following relationship holds in the inverter presented in [79]:

$$E_{\min} = \frac{\sqrt{2}\pi V_{\mathrm{ac}}}{2}. \tag{3.34}$$

Equations (3.8), (3.33), and (3.34) indicate that the DC input voltage can be reduced to $1/\sqrt{3}$ times compared with the conventional two- or three-level PWM inverter and reduced to $2/\pi$ times compared with the inverter presented in [79] under the same value of V_{ac}, which widens the MPPT range.

3.3 Control Method

The control of the main converter is composed of feedforward control of D_{M}, which is the duty ratio of the upper power devices (e.g., Su1 in Fig. 3.1), and it is common to all phases.

On the other hand, the control of the auxiliary converter is composed of the following sub-controls:

- DC-capacitor voltage control
- Inductor current control

3.3.1 Feedforward Control of D_{M}

The following relationship holds between D_{M} and α given by (3.31) as

$$D_{\mathrm{M}} = \frac{\pi + 2\alpha}{2\pi} = 0.5 + \alpha/\pi. \tag{3.35}$$

Equations (3.31) and (3.35) indicate that D_{M} is given by the feedforward control, where V_{ac} and E are the input signals. V_{ac} is calculated using the detected grid voltage. As mentioned in the previous section, the ZCS of the power devices used in the main converter can be achieved under the voltage ranges expressed by (3.6) and (3.23) with α given as (3.31). Different DC input voltages and AC grid voltages will lead to different duty cycles.

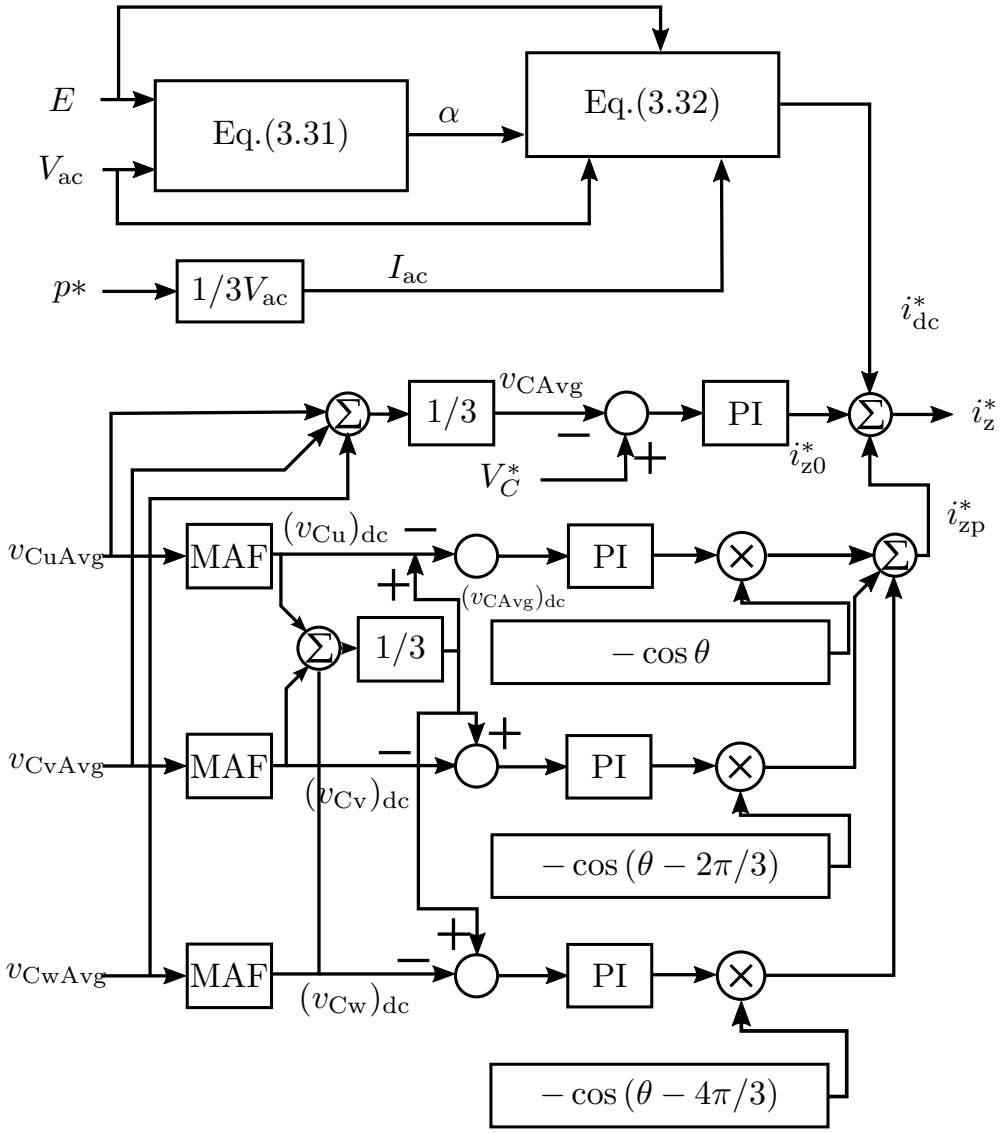


Figure 3.4: Block diagram of overall voltage control and cluster balancing control.

It is noteworthy that D_{M} will always be 0.5 when the relationship (3.24) holds because α is always set to zero in this range.

3.3.2 DC-capacitor Voltage Control

The DC-capacitor voltage control comprises the following three parts:

- Overall voltage control
- Cluster balancing control
- Individual balancing control

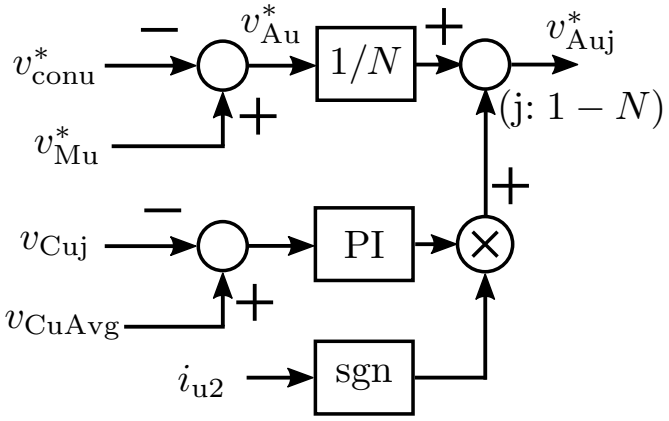


Figure 3.5: Block diagram of output voltage calculation for u-phase cell including individual balancing control.

Fig. 3.4 shows the control block diagram of the overall voltage control and the cluster balancing control. Fig. 3.5 shows that of the individual balancing control. The overall voltage control is achieved using the DC component in the zero-sequence current i_{z}, and the cluster balancing control is achieved by adjusting the amplitude and phase of the fundamental-frequency AC component in i_{z}. The following relationship holds between i_{z} and the neutral current i_{n}:

$$i_{\mathrm{z}} = \frac{i_{\mathrm{n}}}{3} = \frac{i_{\mathrm{u2}} + i_{\mathrm{v2}} + i_{\mathrm{w2}}}{3}. \tag{3.36}$$

3.3.2.1 Overall Voltage Control

The role of the overall voltage control is to regulate the arithmetic average value of all the DC-capacitor voltages used in the auxiliary converters, v_{CAvg}, to its reference value V_C^*, and this can be achieved by superimposing the DC-ZSC, i_{z0}, to the inductor currents. The variation of i_{z0} is expressed as Δi_{z0} and the variation of the DC input power ΔP_{inu} originating from Δi_{z0} is given by

$$\Delta P_{\mathrm{inu}} = D_{\mathrm{M}} E \Delta i_{\mathrm{z0}}. \tag{3.37}$$

Meanwhile, i_{z0} forms no active power with v_{u2}, which is the secondary line-to-neutral voltage of the transformer, because the former is DC current and the latter is AC voltage. In other words, the AC output power of the converter is not affected by i_{z0}, whereas it

can adjust the DC input power. Consequently, v_{CAvg} increases when the DC input power is larger than the AC output power, and decreases when the DC input power is smaller than the AC output power.

3.3.2.2 Cluster Balancing Control

The role of the cluster balancing control is to regulate the DC component of arithmetic average value of the DC-capacitor voltages used in the auxiliary converter of each phase, $(v_{\mathrm{Cu}})_{\mathrm{dc}}$, $(v_{\mathrm{Cv}})_{\mathrm{dc}}$, $(v_{\mathrm{Cw}})_{\mathrm{dc}}$, to their reference value $(v_{\mathrm{CAvg}})_{\mathrm{dc}}$, and this can be achieved by superimposing the zero-sequence fundamental-frequency current, i_{zp}, to the inductor currents. Specifically, the difference of $(v_{\mathrm{CAvg}})_{\mathrm{dc}}$ and $(v_{\mathrm{Cu}})_{\mathrm{dc}}$ (i.e., $(v_{\mathrm{CAvg}})_{\mathrm{dc}} - (v_{\mathrm{Cu}})_{\mathrm{dc}}$) is given as the input signal for the PI (proportional-integral) controller of u-phase as shown in Fig. 3.4. Then, the output signals of the three PI controllers are multiplied by $-\cos\theta$, $-\cos(\theta - 2\pi/3)$, or $-\cos(\theta - 4\pi/3)$, respectively, and i^*_{zp}, which is the reference for i_{zp}, is formed by summing them up. It should be noted that $-\cos\theta$ is out of phase with v_{u2} by 180°, and there are no AC components included in $(v_{\mathrm{Cu}})_{\mathrm{dc}}$, $(v_{\mathrm{Cv}})_{\mathrm{dc}}$, and $(v_{\mathrm{Cw}})_{\mathrm{dc}}$ because they are eliminated by applying moving average filters of 50 Hz.

Specifically, if $(v_{\mathrm{CAvg}})_{\mathrm{dc}} > (v_{\mathrm{Cu}})_{\mathrm{dc}}$ and i_{zp} contains the $-\cos\theta$ component, i_{zp} and $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ given by (3.15) forms positive active power, thereby increasing $(v_{\mathrm{CAvg}})_{\mathrm{dc}}$. A similar technique can also be applied to MMCC-SDBC . It is noteworthy that i_{zp} produces no effect on the transformer operation because it is ZSC. As a result, the primary currents of the transformer are balanced whereas the AC secondary currents are unbalanced due to the cluster balancing control.

3.3.2.3 Individual Balancing Control

The role of the individual balancing control is to achieve the balancing of the AC-capacitor voltages used in each auxiliary converter, and it can be achieved by adjusting the amplitude of output voltage of each cell appropriately according to the polarity of the converter current. Fig. 3.5 shows the control block diagram for the individual balancing control, where "sgn" means a sign function that produces +1 when $i_{\mathrm{u2}} \geq 0$ and −1 when $i_{\mathrm{u2}} < 0$. A similar technique is used for MMCC in [81].

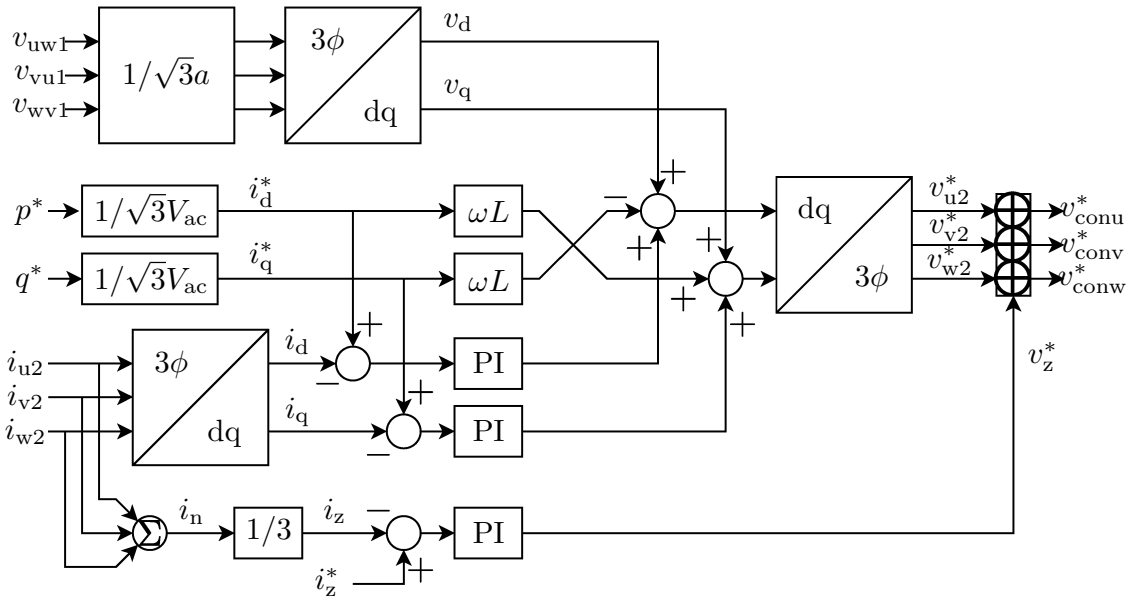


Figure 3.6: Block diagram of current control.

3.3.2.4 Inductor Current Control

Fig. 3.6 shows the control block diagram for the inductor current control, where p^* and q^* are the reference values for instantaneous active and reactive power of three phases, respectively, i_{d}^* and i_{q}^* are the reference values for d- and q-axis currents, respectively, a is the voltage ratio of the transformer, ω $(= 2\pi f_{\mathrm{SM}})$ is the grid radius frequency. The inductor current control is based on the conventional decoupled current control using d-q transformation including the zero-sequence current control. Consequently, the reference for the converter output line-to-neutral voltage, $v_{\mathrm{conu,v,w}}^*$, is the sum of $v_{\mathrm{u2,v2,w2}}^*$, which is the reference for the positive-sequence voltage, and v_{z}^*, which is the reference for the zero-sequence voltage that is common to three phases.

According to Fig. 3.4, the reference for the zero-sequence current i_{z}^* comprises the following three components:

- DC reference current i_{dc}^* given by feedforward control
- DC reference current i_{z0}^* given by overall voltage control
- AC reference current i_{zp}^* given by cluster balancing control

Hence, i_{z}^* is represented by

$$i_{\mathrm{z}}^* = i_{\mathrm{dc}}^* + i_{\mathrm{z0}}^* + i_{\mathrm{zp}}^*, \tag{3.38}$$

where i^*_{dc} is the reference value of I_{dc} and obtained by substituting the relationship $I_{\mathrm{ac}} = i^*_{\mathrm{d}}/\sqrt{3}$ into (3.32). The role of the feedforward control is to improve the transient performance of the converter under a steep change in p^*.

3.3.2.5 Output Voltage Calculation of Auxiliary Converter

The block diagram of the output voltage calculation for the u-phase cells is shown in Fig. 3.5. As shown in (3.12), the auxiliary converter produces the harmonic voltage, DC voltage, and the fundamental-frequency voltage simultaneously. Specifically, the reference for the u-phase output voltage of the auxiliary converter, v^*_{Au}, is given by

$$v^*_{\mathrm{Au}} = v^*_{\mathrm{Mu}} - v^*_{\mathrm{conu}}, \tag{3.39}$$

where v^*_{Mu} is calculated based on the detected DC input voltage E and the switching signals of the main converter. The output voltage of each cell is the sum of v^*_{Au}/N and the voltage component produced by the individual balancing control as $v^*_{\mathrm{Auj}}(j : 1 - N)$. v^*_{Auj} is normalized by the corresponding DC capacitor voltage v_{Cuj}. Then, it is compared with the triangular waveforms with a maximum value of unity and a minimum value of zero, where the phase-shifted PWM with an initial phase difference of $360°/N$ is applied to each cell.

3.4 Experimental Verification

3.4.1 Experimental Conditions

The photograph of the downscaled system used for experiments is shown in Fig. 3.7, and the circuit parameters are summarized in Table 3.1. Considering the difficulty to build a utility-scale PV system in a laboratory, the authors used this downscaled model and it is reasonable because it will not affect the results of the experimental verification [82]–[84]. It is notable that the AC power source shown in Fig. 3.7 has not been available until Chapter 5. The reference for the d-axis current is set to $i^*_{\mathrm{d}} = 16.7\,\mathrm{A}$ for evaluating the steady-state performance, which corresponds to $p^* = 1.7\,\mathrm{kW}$. Meanwhile, it is set to either $i^*_{\mathrm{d}} = 16.7\,\mathrm{A}$ or $i^*_{\mathrm{d}} = 3.3\,\mathrm{A}$ (i.e., $p^* = 0.3\,\mathrm{kW}$) for evaluating the transient-state performance. The reference for the q-axis current is set to $i^*_{\mathrm{q}} = -1.73\,\mathrm{A}$ in steady- and

Table 3.1: Circuit parameters used for experiments.

D-axis current reference	i_{d}^*	16.7 A or 3.3 A
Q-axis current reference	i_{q}^*	-1.73 A (lagging)
Active power reference	p^*	1.7 kW or 0.3 kW
DC input voltage	E	85 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell number per phase	N	3
DC-capacitor voltage reference	V_C^*	45 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	7.2 kHz

transient-state conditions, which corresponds to the lagging reactive power. The DC input voltage and the nominal line-to-line RMS grid voltage are $E = 85$ V and $V_{\mathrm{grid}} = 200$ V, respectively. The voltage ratio of the transformer is set to $a = 2$ so that the secondary line-to-neutral (phase) RMS voltage of the transformer is $V_{\mathrm{ac}} = V_{\mathrm{grid}}/(\sqrt{3}a) = 58$ V. In this case, the voltage ratio of E and $\sqrt{2}V_{\mathrm{ac}}$ is given by

$$E : \sqrt{2}V_{\mathrm{ac}} = 85 : 82 = 1 : 0.97, \tag{3.40}$$

which satisfies (3.6). The chopper-cell number per phase is set to $N = 3$, and the reference for the DC-capacitor voltage is set to $V_C^* = 45$ V. It is notable that the initial charging of the experiments in Chapter 3 is achieved by additional circuits. The initial charging method without additional circuits will be introduced in Chapter 4. The capacitance of the DC-capacitor used in each cell is set to $C = 4.4$ mF, and the inductance is set to $L = 0.21$ mH. Hence, the total inductance including the leakage inductance of $l = 0.27$ mH is 0.48 mH. The carrier frequencies of the main and auxiliary converters are set to $f_{\mathrm{SM}} = 50$ Hz and $f_{\mathrm{SA}} = 7.2$ kHz, respectively. The dead time of the main and auxiliary converters are both set to 4.0 µs.

The control system comprises a DSP (digital signal processor) unit utilizing Texas Instruments TMS320C6678 and a FPGA (field-programmable gate array) unit utilizing Altera Cyclone IV. The voltage and current waveforms are measured using Textronics DPO4104B-L with a frequency band of 1 GHz, Textronics TMDP0200 with a frequency

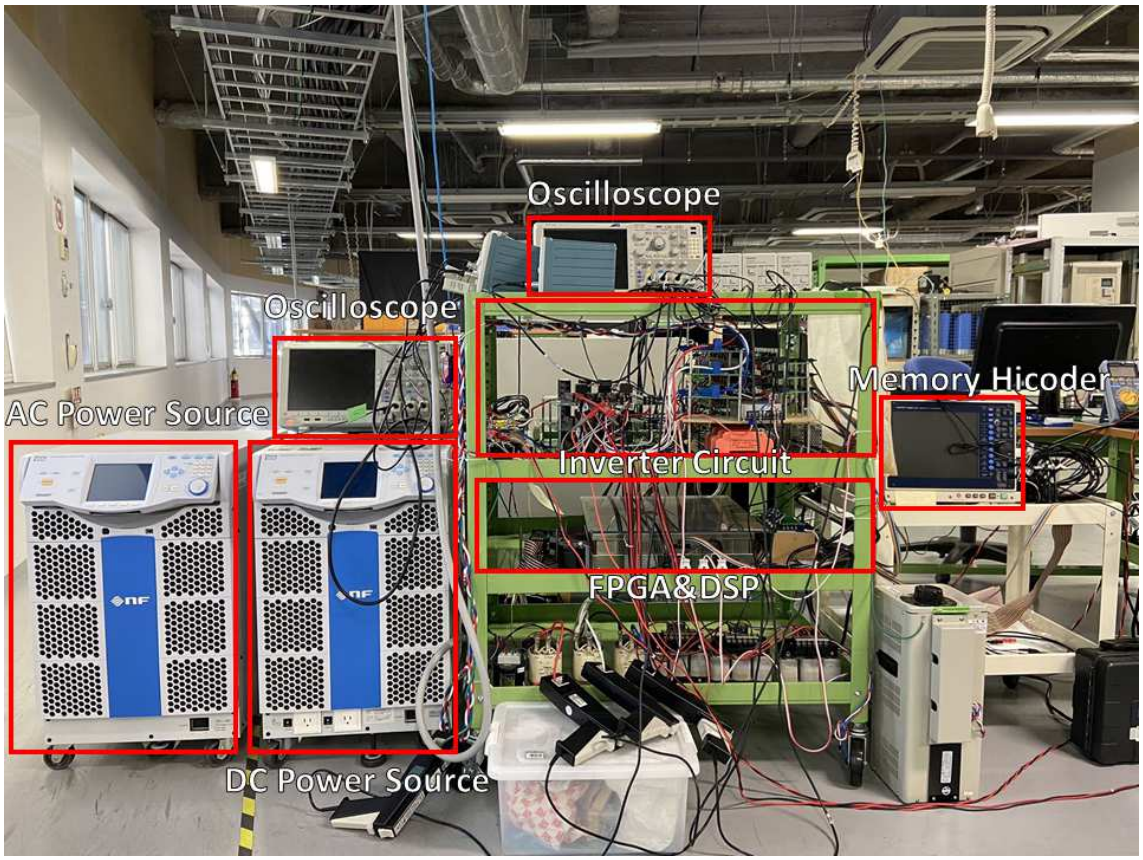


Figure 3.7: Photograph of downscaled experiment system.

band of 200 MHz, Textronics TCP0030A with a frequency band of 120 MHz, and Hioki Memory Hicoder 8861-50.

3.4.2 Steady-state Performance with d-q-0 Control

Fig. 3.8 shows the experimental waveforms under steady state, where the voltage and current waveforms correspond to those shown in Fig. 3.1. The main converter voltage v_{Mu} is formed by a 50-Hz square wave with the phase angle $\alpha = 0.28$, which is slightly smaller than a theoretical value of 0.3 obtained by substituting the circuit parameters summarized in Table 3.1 into (3.22). The reason for this is that the actual values of E and V_{ac} are different from those summarized in Table 3.1.

The converter line-to-neutral voltage v_{conu} corresponds to the voltage difference between v_{Mu} and the auxiliary converter voltage v_{Au}, and it is a five-level multilevel waveform. The fundamental-frequency component in v_{conu} is in phase with the supply line-to-line voltage v_{uw1}.

The inductor current i_{u2} contains the fundamental-frequency and DC components,

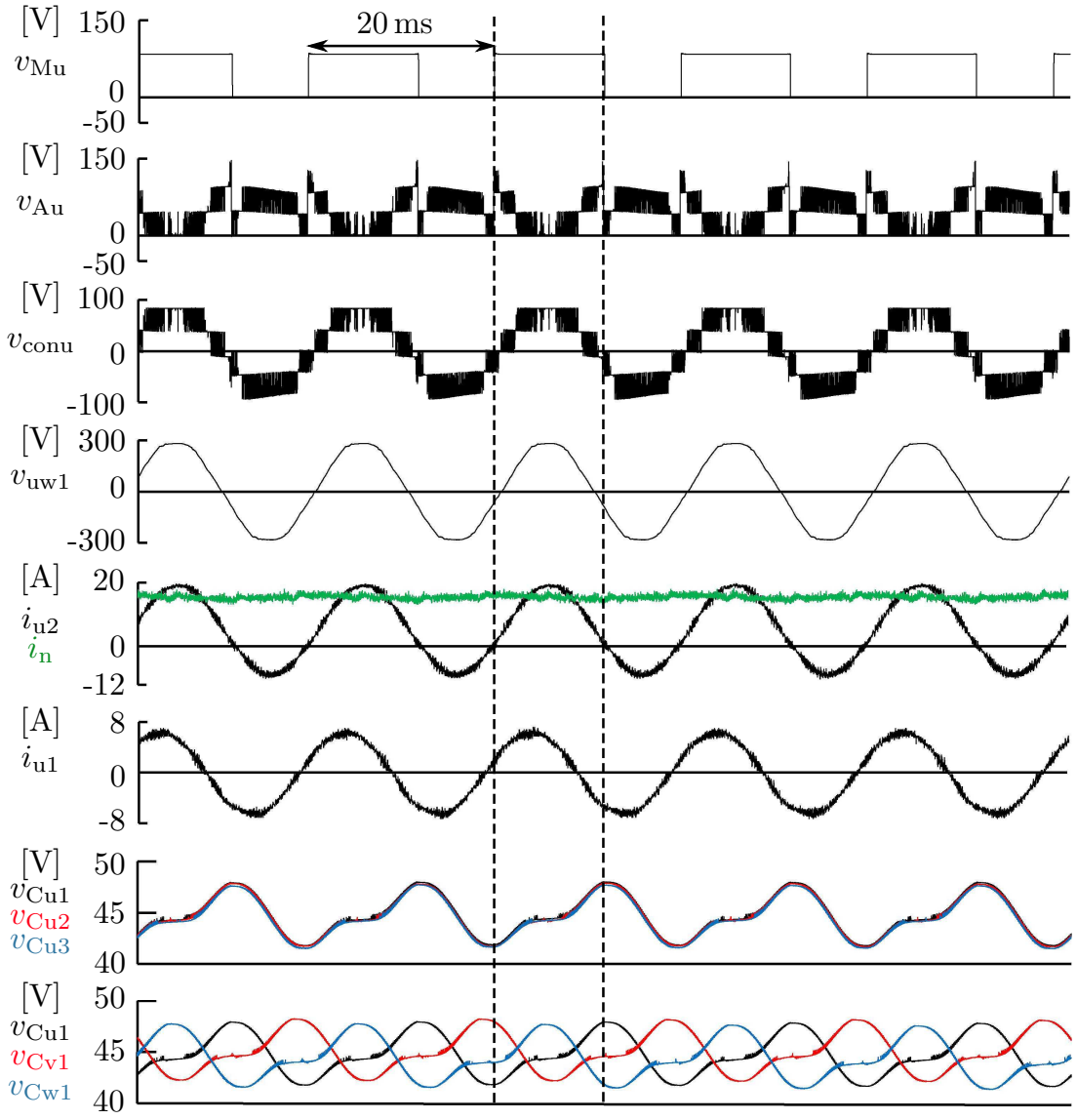


Figure 3.8: Experimental waveforms under steady state where $p^* = 1.7\,\mathrm{kW}$.

and the RMS value of the fundamental-frequency component is $I_{\mathrm{ac}} = 9.9\,\mathrm{A}$. Hence, the three-phase output power is calculated from (3.20) as $3P_{\mathrm{outu}} = 3 \times 58\,\mathrm{V} \times 9.9\,\mathrm{A} = 1.723\,\mathrm{kW}$. Meanwhile, substituting the circuit parameters summarized in Table 3.1 and the relationship $\alpha = 0.28$ into (3.18) yields $I_{\mathrm{dc}} = 3.87\,\mathrm{A}$, which is smaller than the experimental result of 4.97 A. This interesting phenomenon occurs because an additional DC current is required for compensating the converter loss in the auxiliary converter. The fundamental-frequency component in i_{u2} is in phase with that in v_{conu}, and the power factor is almost unity. The neutral current i_{n} is always positive and the DC component is 15.3 A. The DC component is the sum of the DC-ZSCs included in the three inductor currents. Carefully looking into the dashed lines and the waveforms of v_{Mu} and i_{u2} reveal that the ZCS of the power devices used in the main converter can be achieved. The grid current i_{u1} is a sinusoidal waveform which leads i_{u2} by 30° due to the Y-Δ connection of the transformer. The DC components of each DC capacitor voltage are regulated to the reference value of 45 V without any steady-state error.

3.4.3 Transient-state Performance with d-q-0 Control

Fig. 3.9 shows the experimental waveforms under transient state where the d-axis current command i_{d}^{*} was increased from 3.3 A to 16.7 A under a step change, which means that p^{*} was increased from 0.3 kW to 1.7 kW. Fig. 3.10 shows the experimental DC-capacitor voltage waveforms with a longer duration (5 s) of measurement under the same experimental condition as Fig. 3.9.

The amplitude of the fundamental-frequency component and the DC component in the inductor current i_{u2} increased immediately after i_{d}^{*} was increased from 3.3 A to 16.7 A under a step change. The DC components in the neutral current i_{n} and the ZSC i_{z} also increased immediately after the change in i_{d}^{*}, while an amount of 50-Hz component is superimposed in i_{n} and i_{z} as shown in Fig. 3.9. These 50-Hz components are related to the cluster balancing control. The voltage unbalance occurs in v_{Cu1}, v_{Cv1}, and v_{Cw1} in terms of the DC components immediately after the change in i_{d}^{*} as shown in Fig. 3.9. For mitigating the voltage imbalance, the 50-Hz component is included in i_{zp}^{*} as shown in Fig. 3.4, and it appears in i_{n} and i_{z}. In other words, the 50-Hz components play a role in achieving the voltage balancing between the clusters. The grid current i_{u1} is a sinusoidal waveform which leads i_{u2} by 30°, and no overcurrent occurs during the transient state.

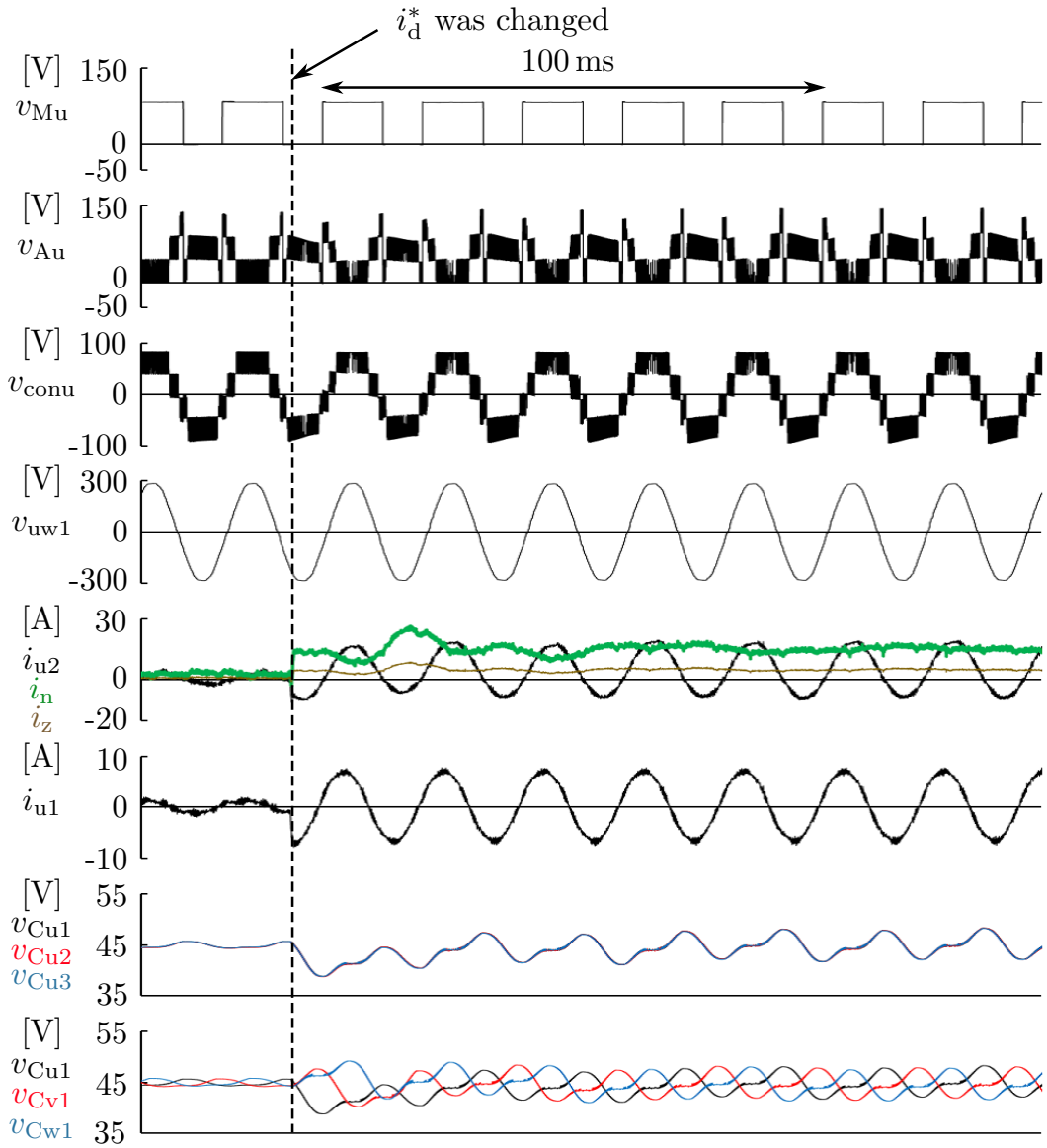


Figure 3.9: Experimental waveforms where i_d^* was changed from 3.3 A to 16.7 A under step change.

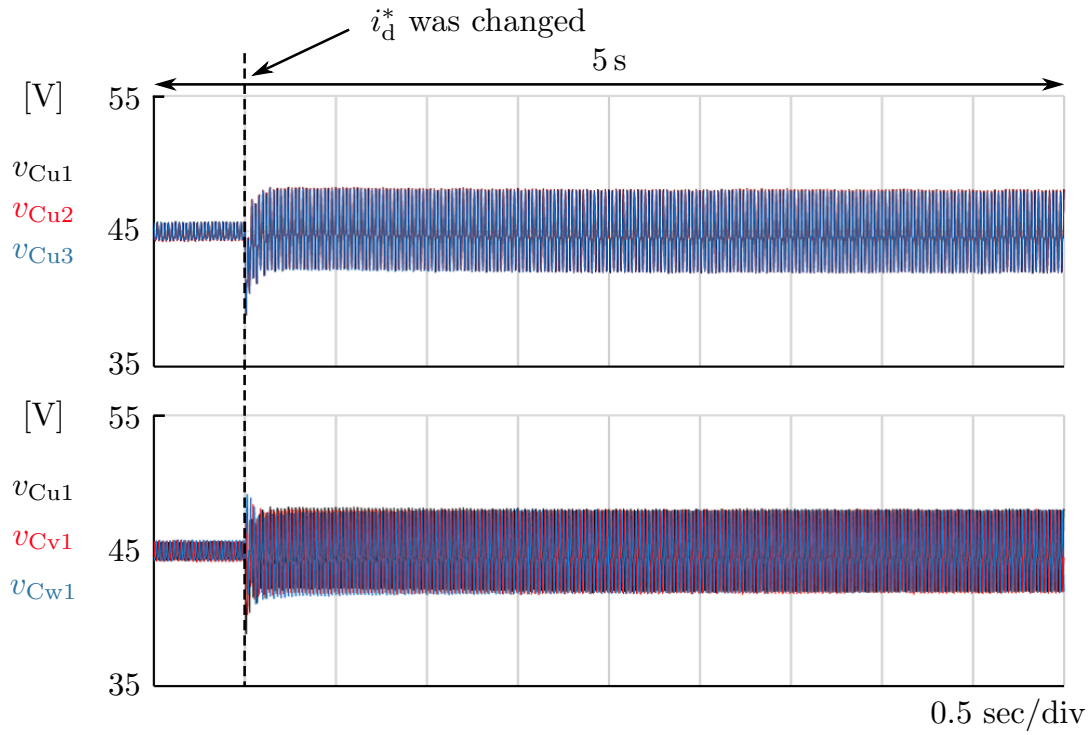


Figure 3.10: Experimental DC-capacitor voltage waveforms where i_d^* was changed from 3.3 A to 16.7 A under step change in 5 seconds period.

Figs. 3.9 and 3.10 show that the voltage unbalance occurs in the DC-capacitor voltages of each phase immediately after the change in i_d^*. However, the DC-capacitor voltages of each phase are balanced owing to the cluster balancing control without any overvoltage or overcurrent in the end.

Fig. 3.11 shows the experimental waveforms under transient state where the d-axis current command i_d^* was decreased from 16.7 A to 3.3 A under a step change, which means that p^* was decreased from 1.7 kW to 0.3 kW. Fig. 3.12 shows the experimental DC-capacitor voltage waveforms with a longer duration (5 s) of measurement under the same experimental condition as Fig. 3.11. The waveforms are similar to those shown in Figs. 3.9 and 3.10, and the inverter exhibits good transient performance without any overvoltage or overcurrent.

However, unbalance will happen among DC-capacitor voltages when $E = 135$ V and $V_C^* = 65$ V, which is shown as Fig. 3.13b. The DC-capacitor voltage of v-phase increased, whereas that of u-phase is stable and that of w-phase decreased. Even though the individual balance control works well in this case, it is verified that the d-q-0 control method will make the DC-capacitor voltage of three phases unstable when the DC input voltage,

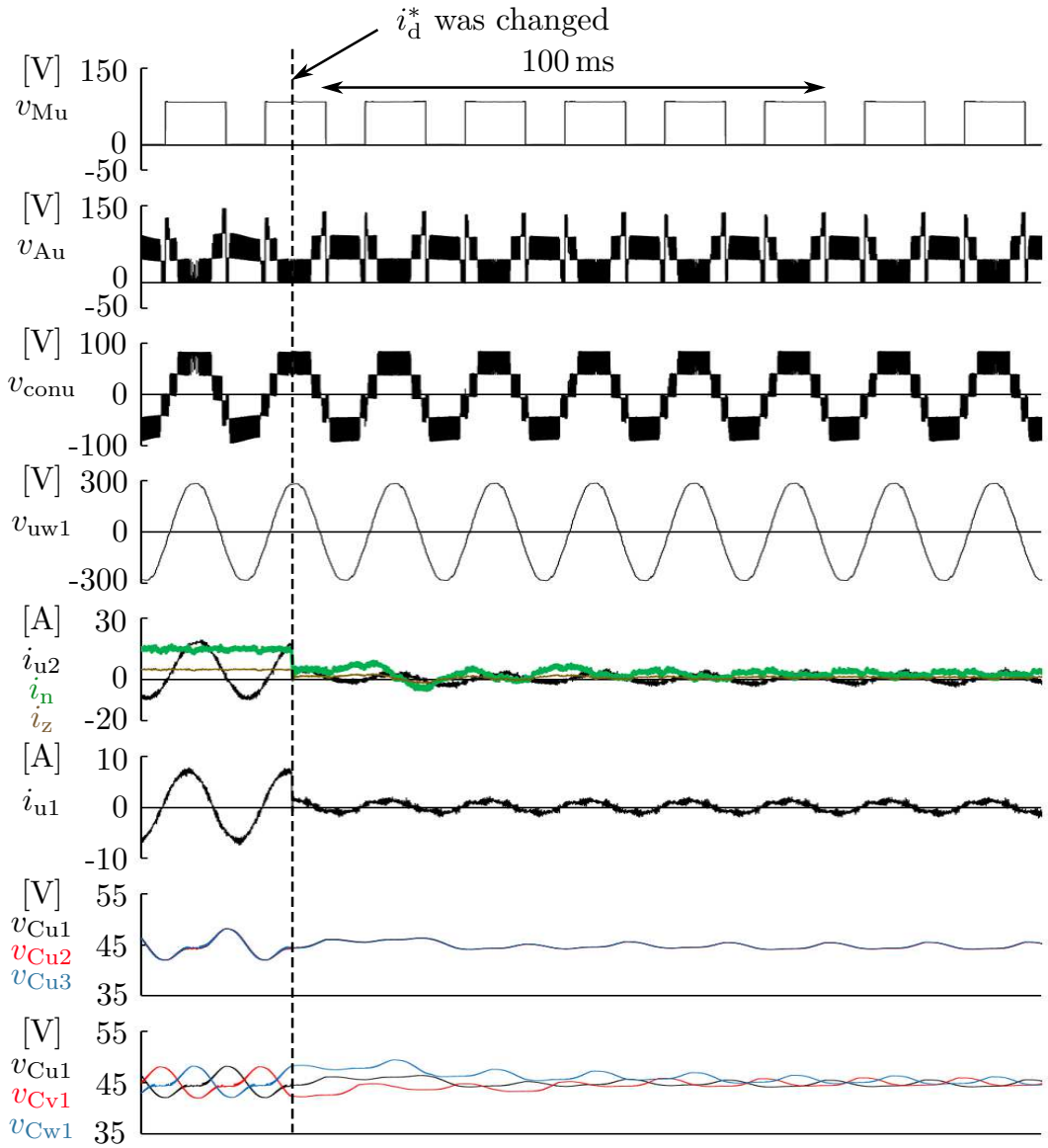


Figure 3.11: Experimental waveforms where i_d^* was changed from 16.7 A to 3.3 A under step change.

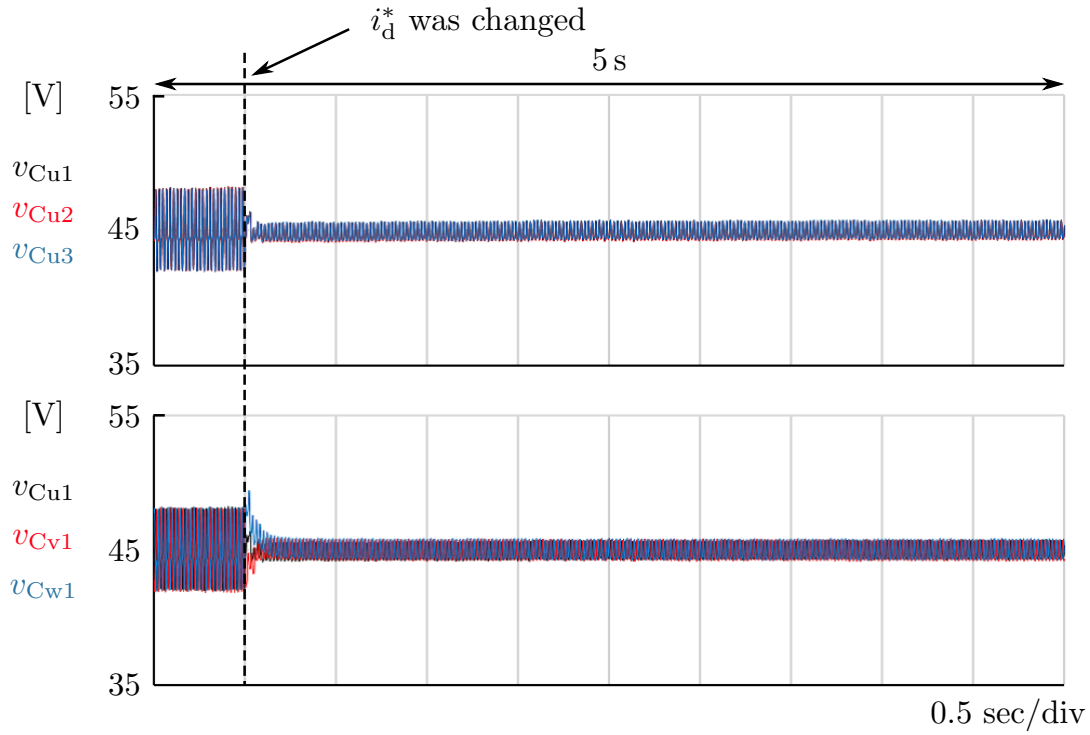


Figure 3.12: Experimental DC-capacitor voltage waveforms where i_d^* was changed from 16.7 A to 3.3 A under step change in 5 seconds period.

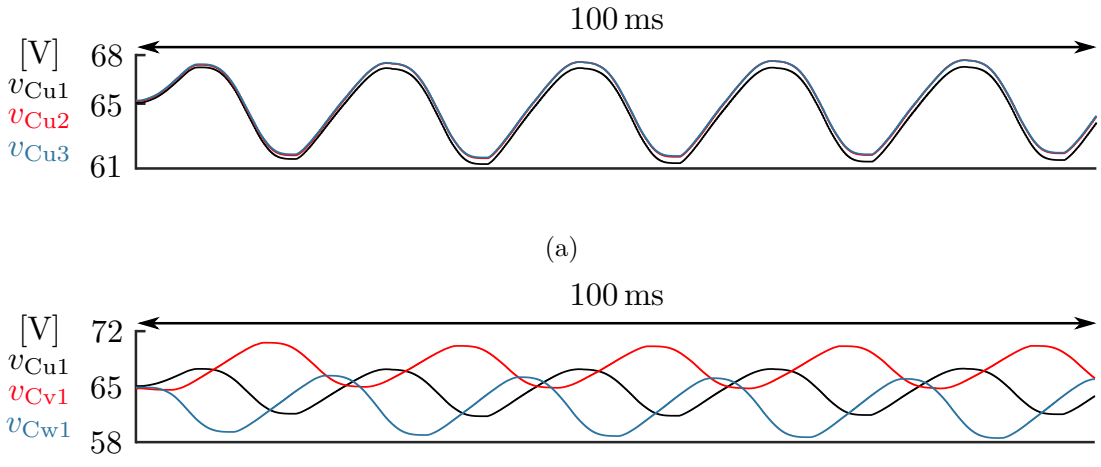


Figure 3.13: Experimental DC-capacitor voltage waveforms in steady state where E = 135 V and V_C^* = 65 V: a) DC-capacitor voltage waveforms of three cells of u-phase, b) DC-capacitor voltage waveforms of first cell of three phases.

E, is in high DC input region. The borderline between the low and high DC input voltage region is 128 V for the downscaled model, which can be obtained by substituting the parameters in Table 3.1 into (3.16) and (3.24).

The reason for this unbalance is caused by the singular point, where $E = 128\,\mathrm{V}$. The power originating from i^*_{zp} and v_{Au} is shown as:

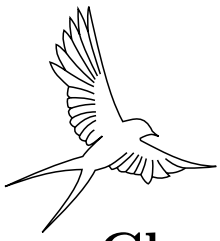
$$\Delta P_{\mathrm{uac}} = (v_{\mathrm{Au}})_{50\,\mathrm{Hz}} * i^*_{\mathrm{zp}} = (\frac{2E}{\pi}\cos\alpha - \sqrt{2}V_{\mathrm{ac}})\cos\theta * i^*_{\mathrm{zp}}. \tag{3.41}$$

Because $(v_{\mathrm{Au}})_{50\,\mathrm{Hz}}$ is almost zero when the DC input voltage is around 128 V, the performance of the cluster balancing control is bad.

3.5 Conclusion

This Chapter provides a detailed introduction of the proposed three-phase PV inverter, including the circuit configuration, the operation principle, and the d-q-0 control method. The circuit configuration is composed of a three-phase inverter and a three-phase line-frequency transformer with a three-limb core working as a step-up transformer for grid connection. The inverter of each phase is composed of a main converter and an auxiliary converter, which is composed of multiple cascaded connected bidirectional chopper cells. With the MMCC based topology, a wider MPPT range can be achieved with a higher AC output voltage, which can reduce the conduction loss. In addition, the multilevel output of the inverter can also contribute to the reduction of the passive filter cost. Further, because of the direct connection between the negative terminal of the PV array and the ground, no high-frequency circulating current flows via the stray capacitance, which makes the parallel operation of the inverters becomes easier.

However, the d-q-0 control method is not enough to stabilize the DC-capacitor voltages when a high DC input voltage is imposed to the system. Therefore, another new control method is necessary to be proposed to make the system stable in both low and high DC input voltage region.



Chapter 4

Individual Current Control and Performance Verification of Proposed Three-phase PV Inverter

Although the control method based on d-q-0 transformation proposed in Chapter 3 works well in the case of low DC input voltage, the DC-capacitor voltages becomes unbalanced in the case of high DC input voltage, which is not suitable to the application of the proposed inverter.

A new control method based on individual current control will be presented in this Chapter. Since the operation principles do not change, only the new control methods will be explained with block diagrams and equations. The performance of the proposed inverter with the new control method will be verified using the same downscaled system. In addition, the initial charging method for the DC-capacitor voltages will also be presented and verified in this Chapter. Further, the loss and efficiency analysis and comparison with that of the three-level T-type inverter will also be conducted.

4.1 Control Method Based On Individual Current Control

The new control method in this Chapter is based on the individual current control, which means the control of each phase is done individually. Since three phases share the same

control method, the following will use u-phase as an example to explain the new proposed control method. It is notable that the control of the main converter does not change. Therefore, the feedforward control introduced in Chapter 3 is still applied to the main converter in this Chapter.

4.1.1 DC-capacitor Voltage Control

The DC-capacitor voltage control contains the following two parts:

- Phase DC-capacitor voltage control
- Individual balancing control

Fig. 4.1 shows the control block diagram of the u-phase DC-capacitor voltage control and Fig. 4.2 shows that of the individual balancing control. The phase DC-capacitor voltage control is achieved by using the DC component included in i_{u2}, i_{udc}, and the individual balancing control is achieved by adjusting the output of each cell individually. It is noteworthy that the sum of i_{udc}, i_{vdc} and i_{wdc} is not equal to zero and it equals to the neutral current i_{n}. Even though the value of i_{n} could be very large, the values of i_{udc}, i_{vdc} and i_{wdc} are 1/3 of it. In addition, the flux induced by these DC components are cancelled by each other, theoretically. Furthermore, the zero-sequence inductance of a transformer could be very small. Therefore, the influences that the DC components brings to the three-phase with three-limb core can be neglected. The following will focus on the control of the u-phase inverter.

4.1.1.1 Phase DC-capacitor Voltage Control

Fig. 4.1 shows the control block diagram of the u-phase DC-capacitor voltage control. i^*_{dc} is the reference value of I_{dc} shown in (3.18). v_{CuAvg} is the arithmetic average value of all the capacitor voltages in u-phase auxiliary converter which includes both DC and AC components. The role of the phase DC-capacitor voltage control is to regulate the DC component of v_{CuAvg}, $(v_{\mathrm{Cu}})_{\mathrm{dc}}$, to its reference value V^*_C using the DC component i^*_{udc0}. The MAF (moving average filter) with a frequency of 50 Hz is used to detect the DC component. Let the variation of i_{udc0} be Δi_{udc0}. The variation of the DC input power

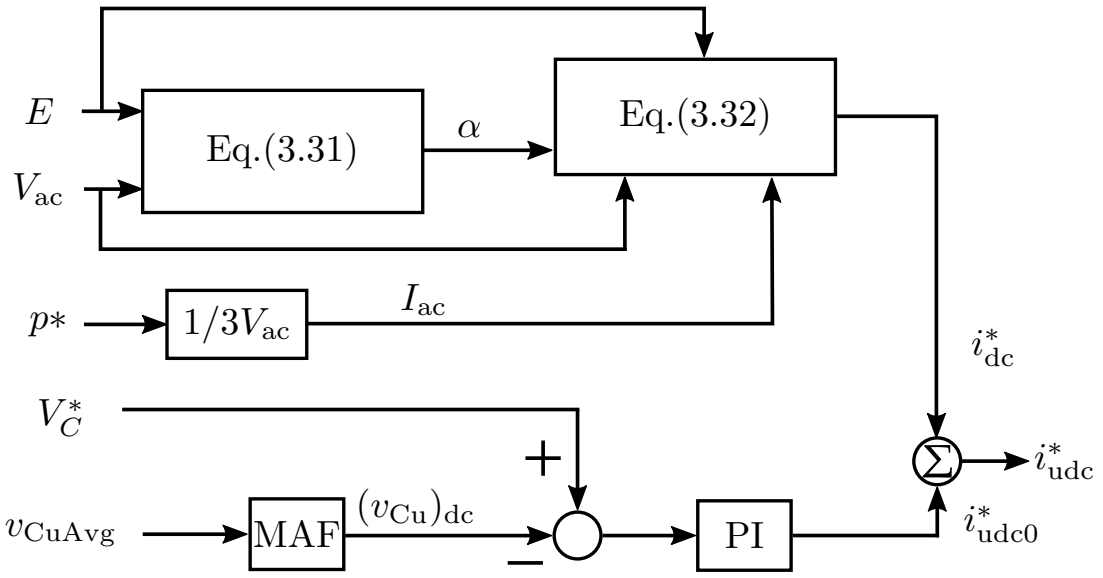


Figure 4.1: Block diagram of u-phase DC-capacitor voltage control.

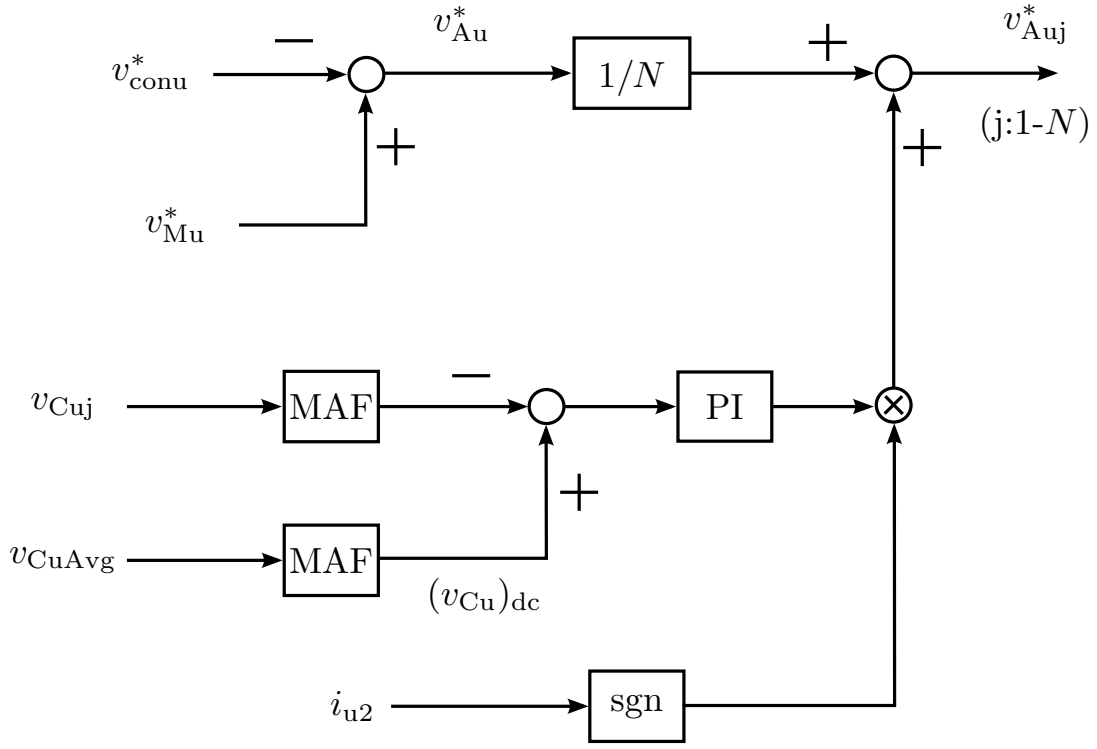


Figure 4.2: Block diagram of output voltage calculation for u-phase cells including individual balancing control.

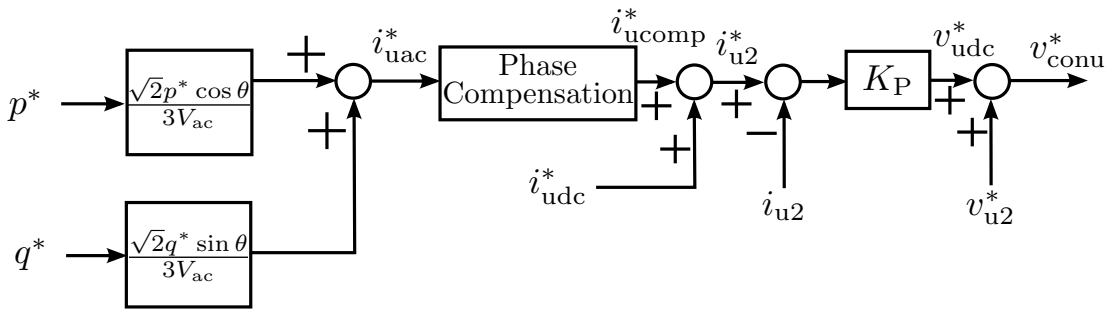


Figure 4.3: Block diagram of u-phase inductor current control.

ΔP_{inu} caused by Δi_{udc0} is given by

$$\Delta P_{\mathrm{inu}} = D_{\mathrm{M}} E \Delta i_{\mathrm{udc0}}. \tag{4.1}$$

i_{udc0} forms no active power with v_{u2} given by (3.2), because the former is DC current and the latter is AC voltage. In other words, the output AC power of the inverter is not affected by i_{udc0}, even though it can adjust the DC input power. v_{CuAvg} increases when the DC input power is larger than the AC output power, and decreases when the DC input power is smaller than the AC output power. The value of i^*_{dc} could be obtained using equation (3.18) or (3.30) according to the DC input voltage, which are also shown in Fig. 4.1. The sum of i^*_{udc0} and i^*_{dc}, i^*_{udc}, is used in current control, which is shown in Fig. 4.3.

4.1.1.2 Individual Balancing Control

The function of the individual balancing control is to achieve the balancing of the DC-capacitor voltages used in each auxiliary converter since there could be differences between the DC-capacitor voltages even though the arithmetic average value is regulated to the reference value. The control block diagram for the individual balancing control is shown in Fig. 4.2 and it does not change from Fig. 3.5.

4.1.2 Inductor Current Control

Fig. 4.3 shows the control block diagram for the u-phase inductor current control. With p^* and q^*, which are the reference values of active and reactive power, the reference value

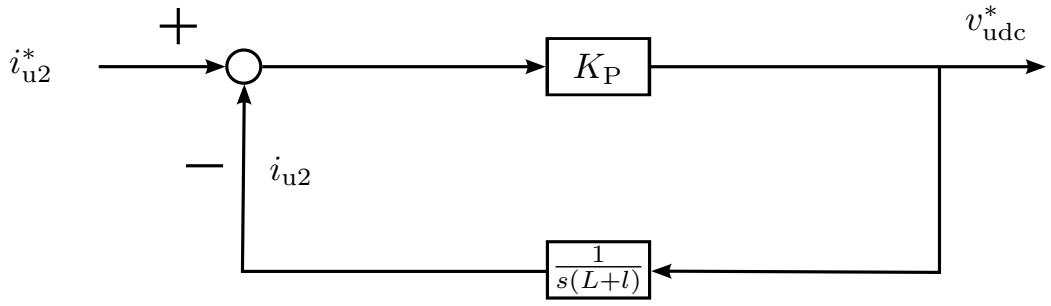


Figure 4.4: Relationship between i^*_{u2} and i_{u2}.

of the AC inductor current is given by

$$i^*_{uac} = \frac{\sqrt{2}p^*}{3V_{ac}}\cos\theta + \frac{\sqrt{2}q^*}{3V_{ac}}\sin\theta, \tag{4.2}$$

where θ is the phase angle of u-phase obtained from the phase locked loop (PLL).

4.1.2.1 Phase Compensation

Generally, phase delay between the AC components included in i^*_{u2} and i_{u2} occurs because the conventional proportional control is applied to the current control. Therefore, the phase compensation method is used to cancel the delay. Fig. 4.4 indicates the relationship between i^*_{u2} and i_{u2}. It is noteworthy that the relationship $v_{udc} \simeq v^*_{udc}$ is assumed. Thus, the relationship between i^*_{u2} and i_{u2} in s domain is expressed by

$$i^*_{u2}(s) = (1 + \frac{L+l}{K_p}s)i_{u2}(s), \tag{4.3}$$

where L is the inductor inductance, l is the leakage inductance of the transformer and K_p is the proportional gain of the current control. The aim of phase compensation is to realize the relationship $i_{u2} = i^*_{uac}$ in Fig. 4.3. Specifically, the AC inductor current reference after

the phase compensation i^*_{ucomp} in t domain is given by

$$\begin{aligned} i^*_{\mathrm{ucomp}} &= i^*_{\mathrm{uac}} + \frac{L+l}{K_{\mathrm{p}}}\frac{\mathrm{d}i^*_{\mathrm{uac}}}{\mathrm{d}t} \\ &= \frac{\sqrt{2}p^*}{3V_{\mathrm{ac}}}\cos\theta + \frac{\sqrt{2}q^*}{3V_{\mathrm{ac}}}\sin\theta \\ &\quad - \frac{\sqrt{2}\omega(L+l)p^*}{3V_{\mathrm{ac}}K_{\mathrm{p}}}\sin\theta + \frac{\sqrt{2}\omega(L+l)q^*}{3V_{\mathrm{ac}}K_{\mathrm{p}}}\cos\theta. \end{aligned} \tag{4.4}$$

4.1.2.2 Output Voltage Calculation of Auxiliary Converter

The final reference value of the u-phase inductor current after phase compensation is obtained as i^*_{u2}. According to Fig. 4.1 and Fig. 4.3, i^*_{u2} is composed of the following three components:

- DC reference current i^*_{dc} given by feedforward control
- DC reference current i^*_{udc0} given by phase DC-capacitor voltage control
- AC reference current i^*_{ucomp} given by phase compensation

Hence, i^*_{u2} is represented by

$$i^*_{\mathrm{u2}} = i^*_{\mathrm{dc}} + i^*_{\mathrm{udc0}} + i^*_{\mathrm{ucomp}}, \tag{4.5}$$

With the feedback control of the inductor current i_{u2} based on the conventional proportional control, the u-phase DC voltage reference v^*_{udc} is obtained. In Fig. 4.3, v^*_{u2} corresponds to the line-to-neutral voltage reference of the transformer with zero leakage inductance and resistance, which is obtained by detecting the grid voltage and using the turns ratio of the transformer. Finally, the reference of the inverter line-to-neutral voltage, v^*_{conu}, is obtained. Consequently, the reference of the u-phase output voltage of the auxiliary converter, v^*_{Au}, is given by (3.39).

4.2 Experimental Verification

4.2.1 Experimental Conditions

The same downscaled system shown in Fig. 3.7 was used for experiments and the circuit parameters are summarized in Table 4.1. The DC input voltage corresponding to the PV

Table 4.1: Circuit parameters used for experiments.

Active power reference	p^*	1.5 kW or 0.3 kW or 0
Reactive power reference	q^*	0 or 1.5 kVar
DC input voltage	E	85 V or 135 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	3
DC-capacitor voltage reference	V_C^*	45 V or 65 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	7200 Hz

array voltage, E, was produced using a stiff voltage source so that the active power is controlled by the inverter. In active power control cases, the reference value of the active power was 1.5 kW in the steady-state operation and was changed from 0.3 kW to 1.5 kW in the transient-state operation. The reference value of the reactive power was always zero. In reactive power control cases, the reference value of the reactive power was set to 1.5 kVar while the active power was zero. The reference value of the DC-capacitor voltage was set to 45 V when the DC input voltage was 85 V and was set to 65 V when the DC input voltage was 135 V considering (3.10). The deadtime was set to 4.0 µs for the main and the auxiliary converters. The voltage ratio of the transformer was set to $a = 2$.

The control system is composed of a DSP unit utilizing Texas Instruments TMS320C6678 and a FPGA unit utilizing Altera Cyclone IV. The voltage and current waveforms were measured using Textronics DPO4104B-L with a frequency band of 1 GHz, Textronics TMDP0200 with a frequency band of 200 MHz, Textronics TCP0030A with a frequency band of 120 MHz, and Hioki Memory Hicoder 8861-50.

4.2.2 Initial Charging of DC-capacitor Voltage

The initial charging of each DC-capacitor voltage should be achieved for the operation of the Fig. 3.1 circuit, and the initial charging can be achieved by either connecting an auxiliary circuit to the DC side of each capacitor, or using the common DC input voltage E [79], [85]. However, the former method is inapplicable to the actual system because of its high cost and low reliability as described in the introduction. The following two methods using the common DC input voltage, E, were proposed in [79], [85]. A method

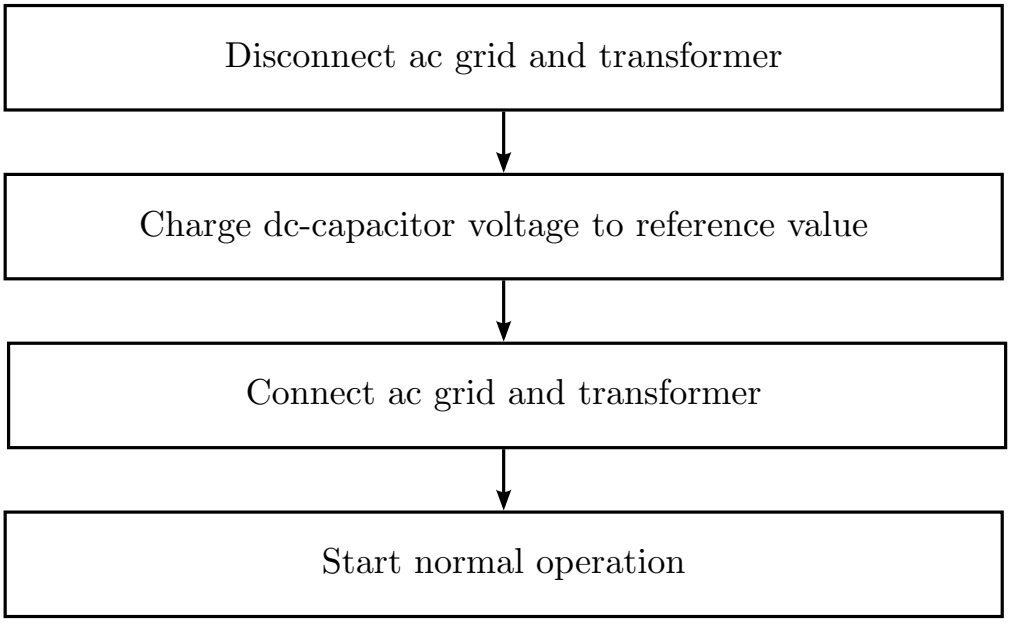


Figure 4.5: Flowchart of initial charging process.

based on extra electromagnetic switches and resistors is presented in [79], with which all capacitor voltages can be charged simultaneously. Meanwhile, a method based on voltage feedback control and sequential control is presented in [85], which is characterized in that the initial charging is achieved with no resistors. The former method is inapplicable to the Fig. 3.1 circuit because the initial DC-capacitor voltage is limited to E/N and it is not enough for the operation of the Fig. 3.1 circuit where the relationship (3.11) should hold. The latter method is not directly applicable to the Fig. 3.1 circuit because the method presented in [85] is aimed for the bidirectional chopper (i.e., DC-DC converter) with auxiliary converters composed of the cascaded single-phase full-bridge converters.

This subsection presents an initial charging method applicable to the Fig. 3.1 circuit which is based on voltage feedback control and sequential control along with utilizing electromagnetic switches that are typically used for grid-connected converters. With this method, each DC capacitor voltage can be charged up to E, which is enough for satisfying (3.11). The flowchart of the initial charging process is shown in Fig. 4.5.

At the initial state, the grid and the transformer are disconnected using electromagnetic switches and all DC-capacitor voltages are zero. Then, the capacitor of each chopper cell is charged sequentially based on the method presented in [85]. The charging process of v_{Cu1} will be explained in the following. Fig. 4.6 shows an example of the current path

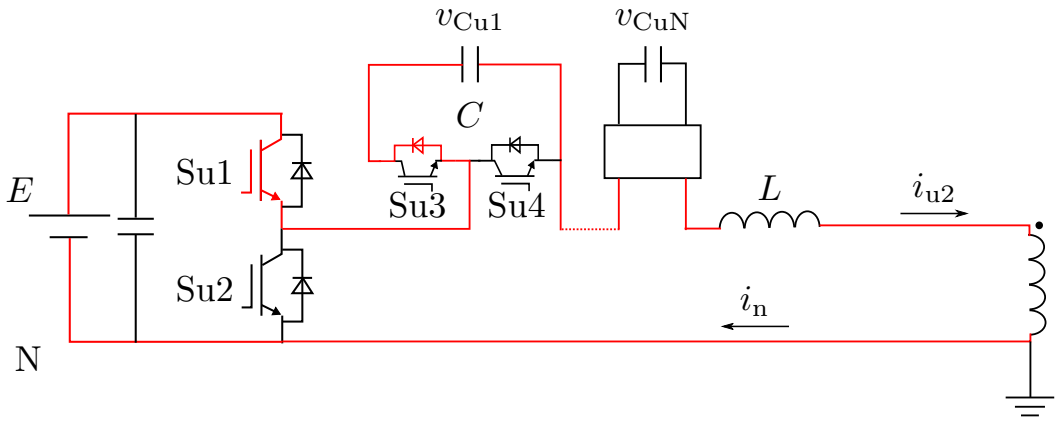


Figure 4.6: Example of current path when v_{Cu1} is charged.

when v_{Cu1} is charged. When v_{Cu1} is being charged, Su3 in the cell numbered 1 is always on and Su4 in the corresponding cell is always off. The other cells operate under the short-circuit mode so that Su3 is always off and Su4 is always on, which are not depicted in Fig. 4.6. Meanwhile, the switchings of Su1 and Su2 are determined by the feedback control of v_{Cu1} [85]. Specifically, when v_{Cu1} is smaller than its reference, the duty ratio of Su1 is increased and a larger current may flow into the capacitor. When Su2 and Su3 are on, the inductor current (i.e., i_{u2}) flows via diodes in Su2 and Su3, and they keep conducting until i_{u2} becomes zero. This sequence will be repeated every switching period of Su1 and Su2, where the choice of the switching frequency should not be the grid frequency of 50 Hz used in the normal operating condition. A higher frequency is applicable because the charging period is less than 1 s and the loss during the charging process may not be a big issue. In the following experiment, the switching frequency of Su1 and Su2 during the initial charging process is set to 450 Hz.

Figs. 4.7 and 4.8 show the experimental waveforms of the initial charging process. The experiment was carried out using the same downscaled system. Fig. 4.7 shows the waveforms when v_{Cu1}, v_{Cv1}, and v_{Cw1} are charged simultaneously. It shows that they increased to the reference value of 45 V under a ramp change in 200 ms. The waveform of i_{u2} shows that it includes a DC current during the initial charging, and those of i_{v2} and i_{w2} also include the same amount of DC components. Meanwhile, these DC components have no effects on transformer operation because they correspond to the ZSC which produces no magnetic flux in the three-phase three-limb core ideally. Fig. 4.8 shows the waveforms

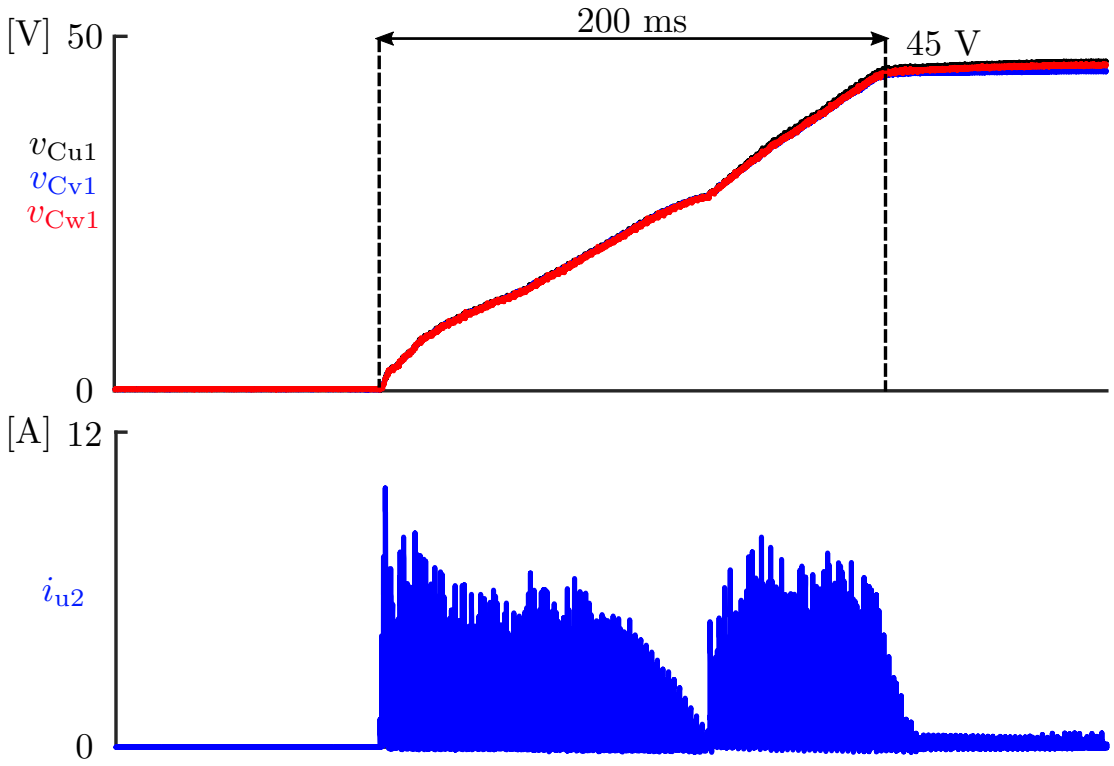


Figure 4.7: Experimental waveforms of initial charging where v_{Cu1}, v_{Cv1}, and v_{Cw1} were charged.

of v_{Cu1}, v_{Cu2}, and v_{Cu3}, which were charged sequentially, and no overvoltage or overcurrent occurred. After each DC-capacitor voltage is charged to the reference value, the grid and the transformer are connected using electromagnetic switches, and the inverter circuit starts normal operation.

4.2.3 Active Power Control Steady-State Performance

Fig. 4.9 shows the experimental waveforms of the proposed inverter under a steady-state when $p^* = 1.5\,\mathrm{kW}$ and $E = 85\,\mathrm{V}$. It corresponds to the low DC input voltage region where the ZCS can be achieved since the relationship (3.23) is satisfied. The main converter voltage v_{Mu} is a square wave with a fundamental frequency of 50 Hz. The phase angle is obtained from Fig. 4.9 as $\alpha = 0.32$, which is slightly larger than a theoretical value of 0.30 obtained by substituting the circuit parameters summarized in Table 4.1 into (3.31). This difference occurs because the actual values of E and V_{ac} are slightly different from those summarized in Table 4.1. The inverter line-to-neutral voltage, v_{conu}, corresponds to the voltage difference between v_{Mu} and v_{Au}, which is a five-level waveform. The fundamental-frequency component in v_{conu} is in phase with the line-to-line grid voltage v_{uw1}. The

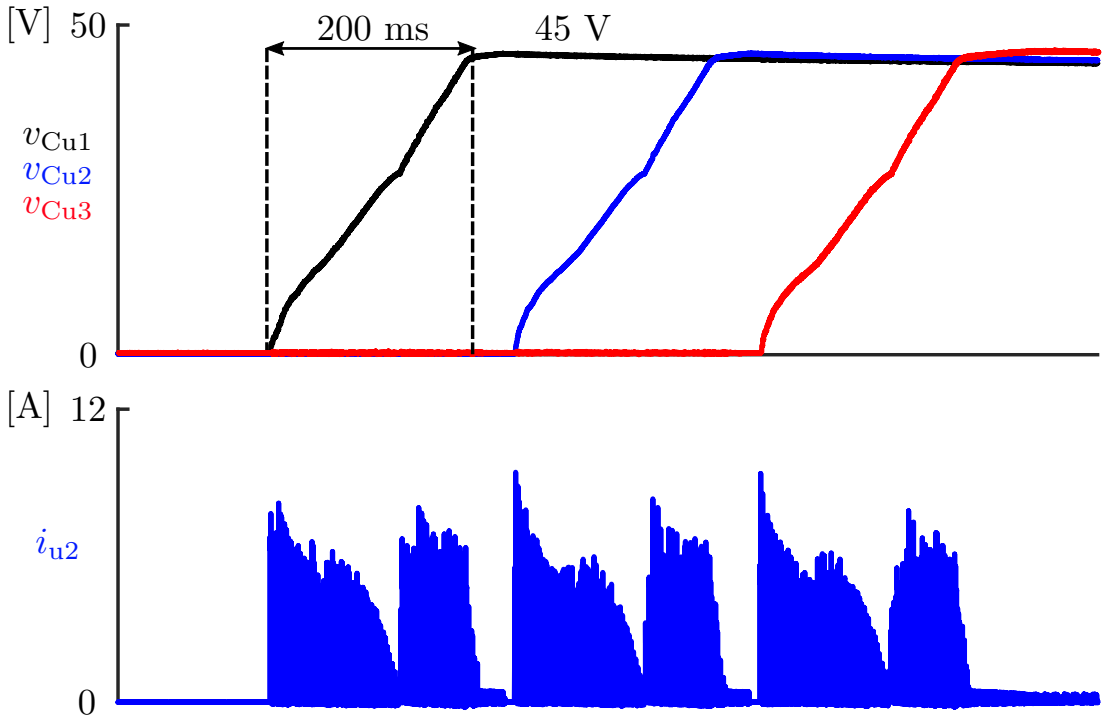


Figure 4.8: Experimental waveforms of initial charging where v_{Cu1}, v_{Cu2}, and v_{Cu3} were charged sequentially.

fundamental-frequency component of i_{u2} is in phase with that of v_{conu}. The power factor is unity since q^* was set to zero. The neutral current i_n is always positive because the relationship (3.16) holds when $E = 85\,\mathrm{V}$ and $\alpha = 0.32$, which means that I_{dc} is positive in (3.17). Careful observation of the dashed lines and the single-cycle waveforms of v_{Mu} and i_{u2} reveal that the current i_{u2} is almost zero at the rising edge and the falling edge of the main converter output voltage v_{Mu}. It is noteworthy that the actual value of i_{u2} may not be exactly zero because of switching ripples. However, if the current at the switching point is small enough compared with the rated current of the inverter, it could be regarded as zero-current switching. The grid current i_{u1} is a sinusoidal waveform which leads i_{u2} by 30° because of the transformer connection. The DC-capacitor voltages are regulated to the reference value of 45 V without any steady-state error. Fig. 4.10 shows the waveforms of i_{in}, which is the DC input current, and i_{inu}, which is the DC current that flows into the u-phase main converter. As we know, the AC output of the three phases is always constant, while the DC input of this inverter is oscillating all the time. The reason for this phenomenon is that the auxiliary converter will compensate the power difference between the DC side and the AC side. The integral equation of the auxiliary converter power shows

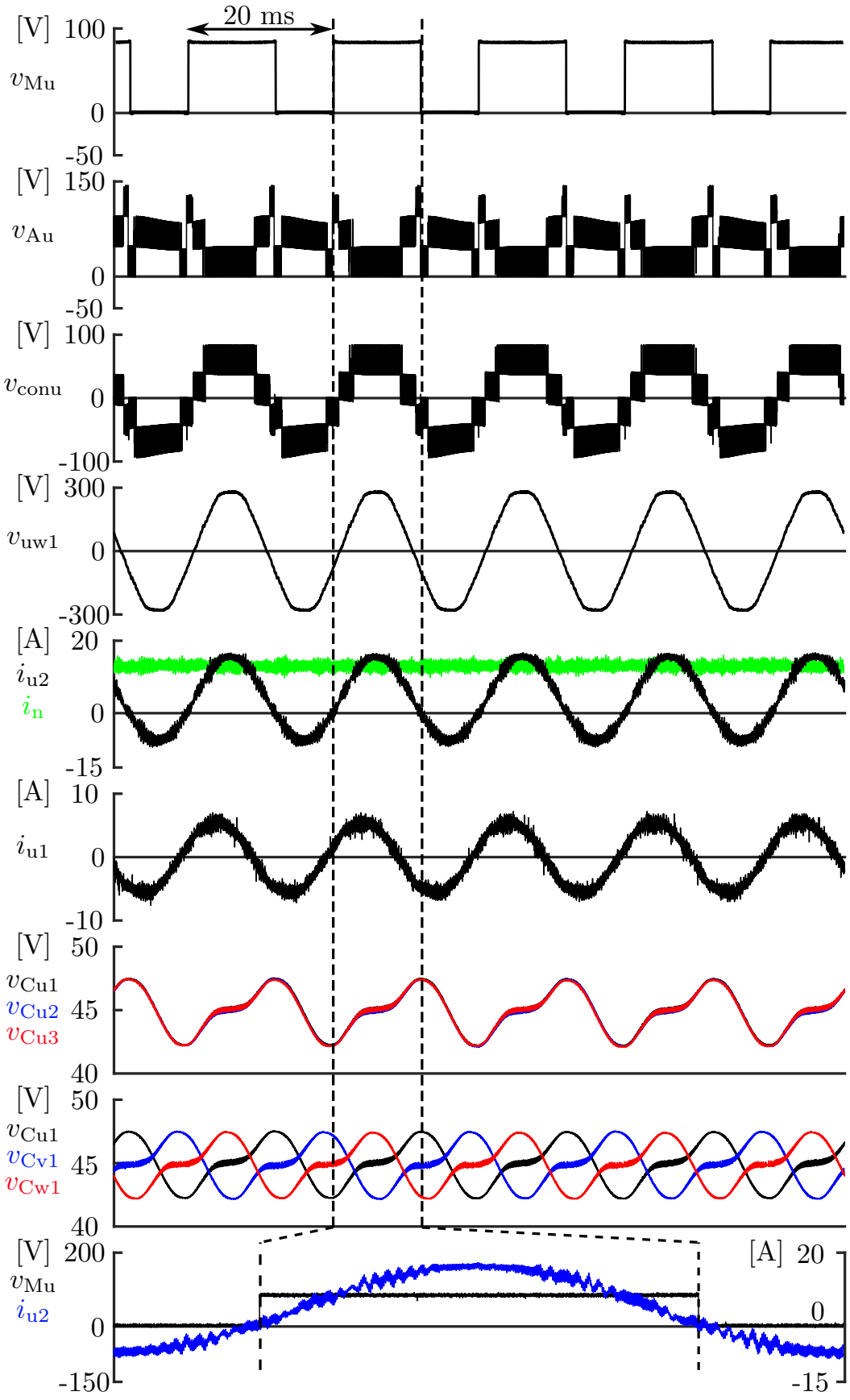


Figure 4.9: Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 85\,\mathrm{V}$.

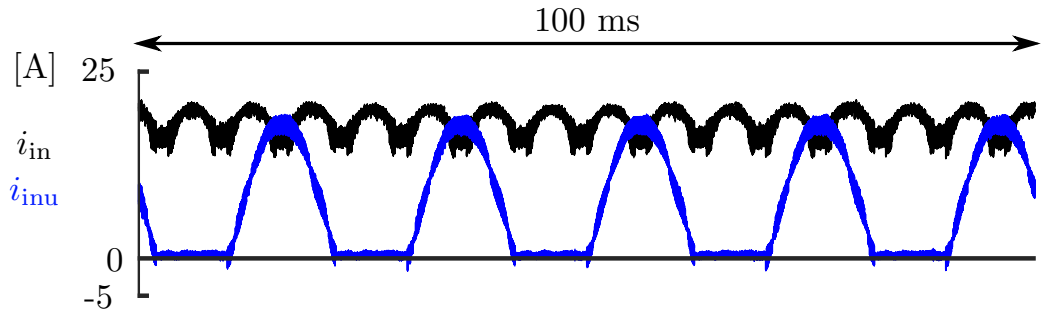


Figure 4.10: Experimental waveforms of i_{in} and i_{inu}.

that the average power of the auxiliary converter is zero, which means that the auxiliary converter does not consume power. The input power and the output power are always balanced.

Fig. 4.11 shows the waveforms when the power and DC input voltage are set to $p^* = 1.5\,\mathrm{kW}$ and $E = 128\,\mathrm{V}$, respectively, which is the edge case between the low DC input voltage and the high DC input voltage. The operation of the proposed inverter at this edge case does not exhibit any instability.

Fig. 4.12 shows the waveforms of another experiment under a steady-state when $p^* = 1.5\,\mathrm{kW}$ and $E = 135\,\mathrm{V}$. It corresponds to the high DC input voltage region where the relationship (3.24) is satisfied. Because (3.24) holds when $E = 135\,\mathrm{V}$, α is fixed to zero. Therefore, ZCS cannot be achieved in this region, theoretically. However, the current at the switching point is also small enough compared with the rated current of the inverter. The other waveforms are basically the same as those shown in Fig. 4.9 except that the DC component included in the neutral current i_{n} is negative due to the increased E. Furthermore, the harmonic components included in i_{n} increases because the DC-capacitor voltage increased from 45 V to 65 V. However, since i_{n} is the zero-sequence current of the three-phase circuit and the zero-sequence components of the three phases have the same phase angle and the same magnitude, the magnetic flux of each zero-sequence component is cancelled out by the other two because of the three-limb core magnetic circuit structure. Therefore, additional eddy currents that cause excessive heating of the metallic enclosure will not occur even though there are high-frequency harmonic components in i_{n}.

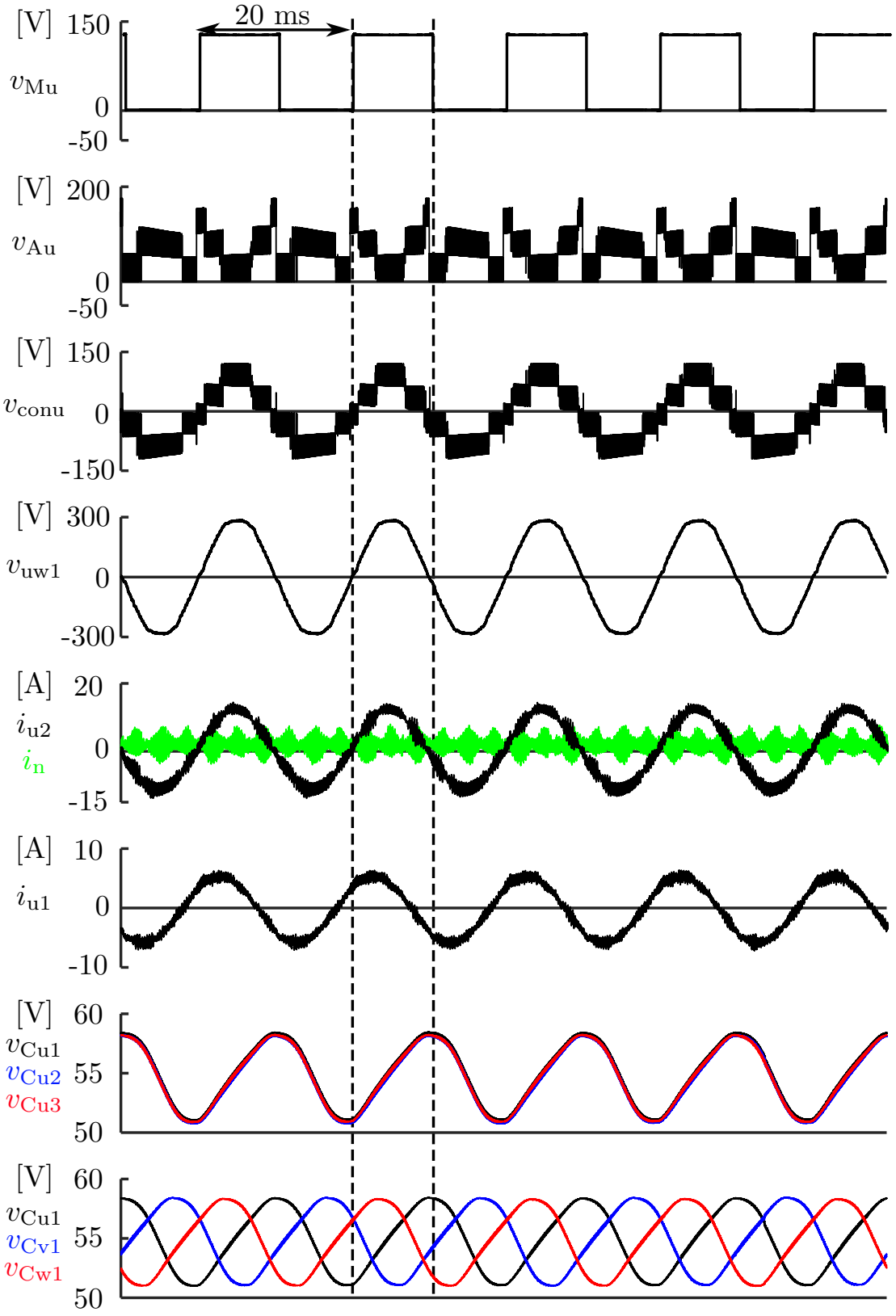


Figure 4.11: Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 128\,\mathrm{V}$.

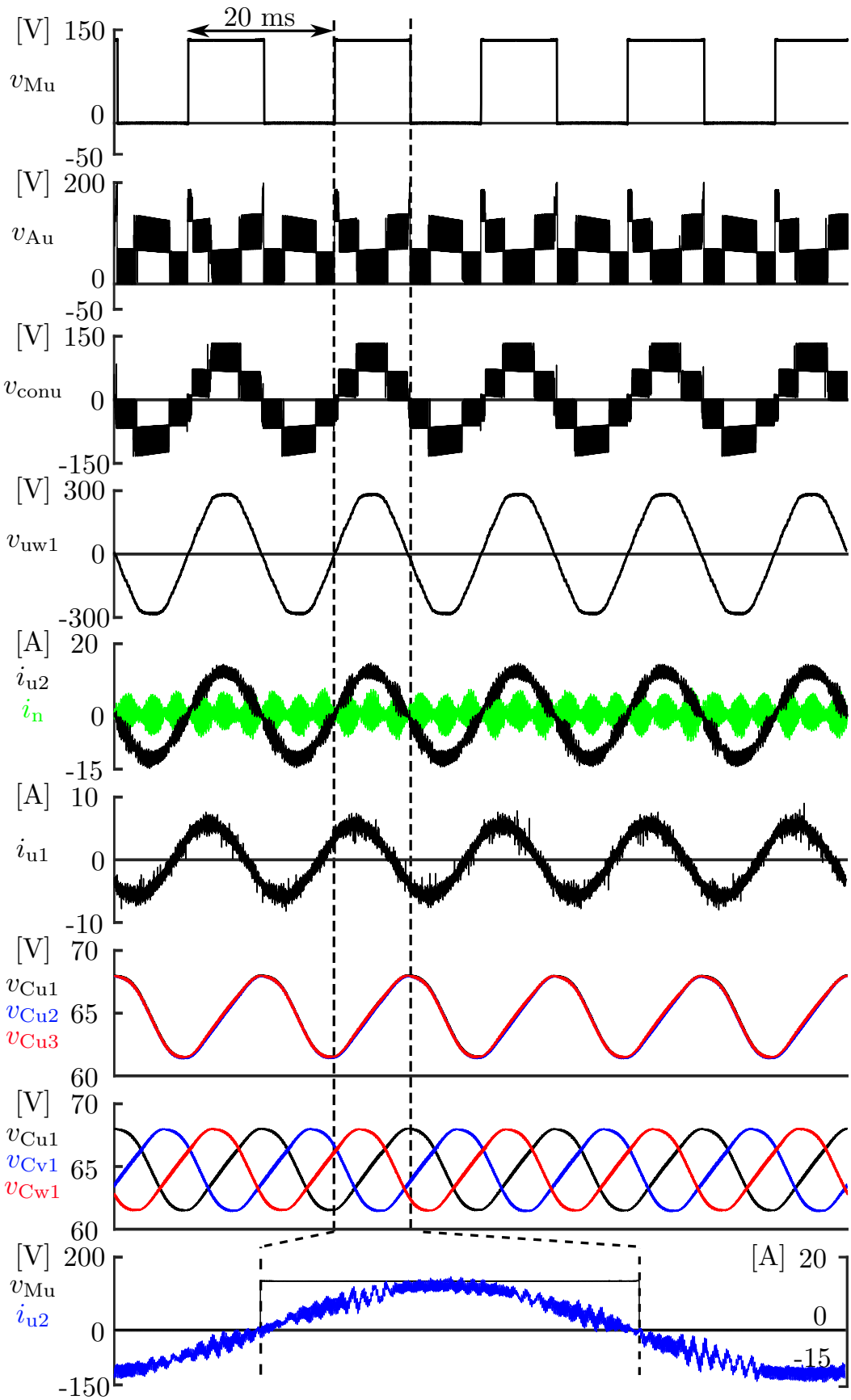


Figure 4.12: Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 135\,\mathrm{V}$.

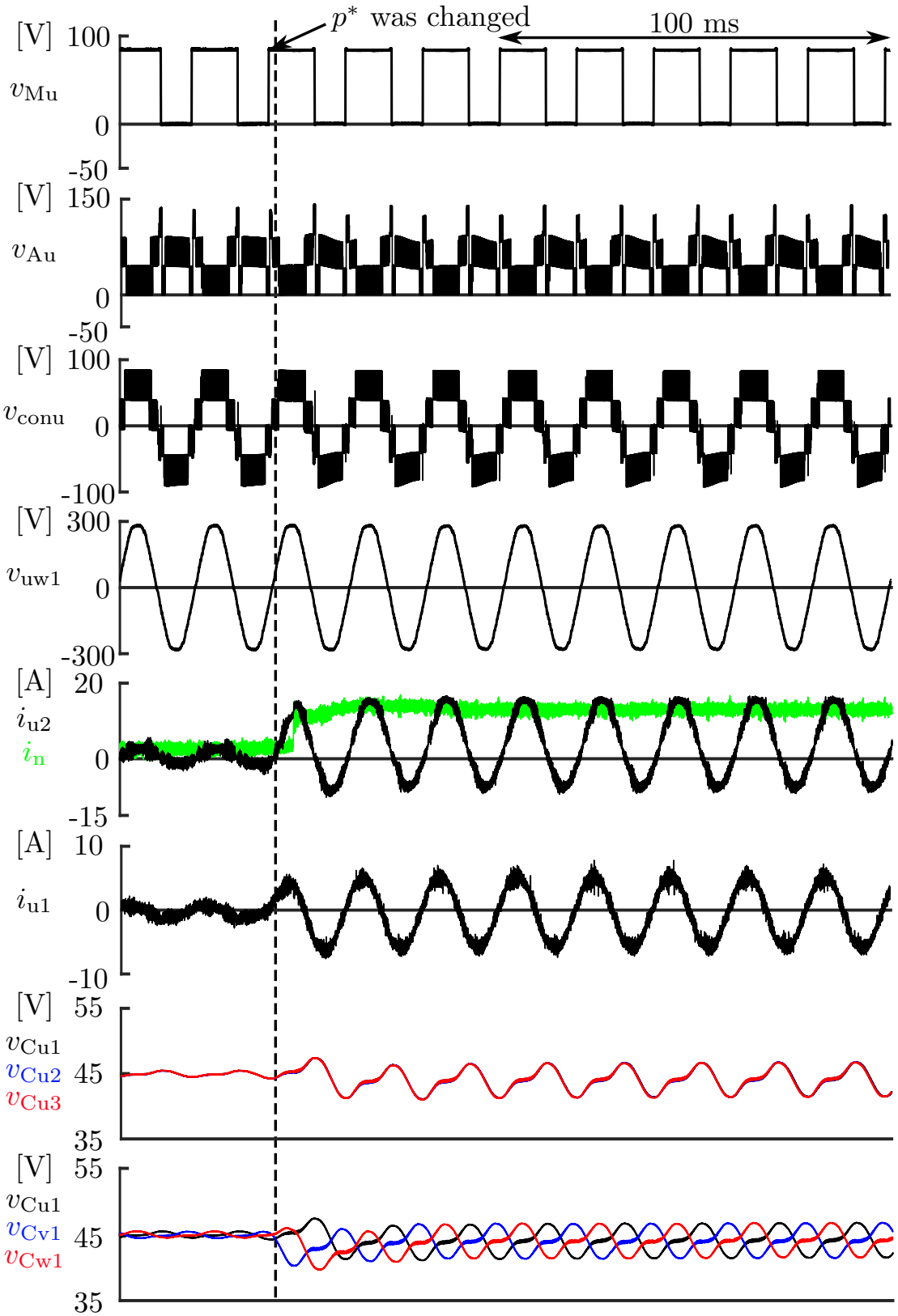


Figure 4.13: Experimental waveforms where p^* was changed from 0.3 kW to 1.5 kW under ramp change.

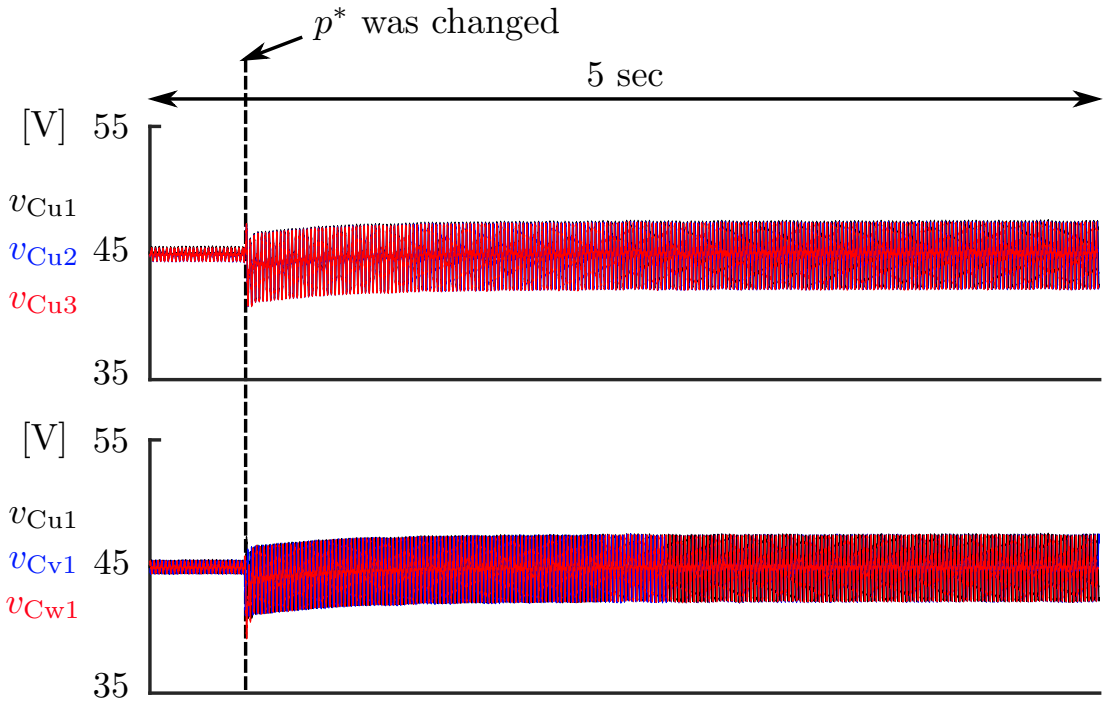


Figure 4.14: Experimental DC-capacitor voltage waveforms where p^* was changed from0.3 kW to 1.5 kW under ramp change in 5 seconds period.

4.2.4 Active Power Control Transient-state Performance

Fig. 4.13 shows the experimental waveforms under a transient state where p^* was increased from 0.3 kW to 1.5 kW under a ramp change while E remained at 85 V. Fig. 4.14 shows the experimental DC-capacitor voltage waveforms with a longer duration of measurement under the same experimental conditions as Fig. 4.13. The voltage and current waveforms correspond to those shown in Fig. 3.1.

The amplitude of the fundamental frequency component and the DC component in the inductor current i_{u2} increases immediately after p^* was increased from 0.3 kW to 1.5 kW under a ramp change. The DC component in the neutral current i_n also increased immediately after the change in p^*. There is a voltage unbalance among v_{Cu1}, v_{Cv1}, and v_{Cw1} following after the change in p^* as shown in Fig. 4.13. With the help of the DC-capacitor voltage control, the voltage balancing could be achieved soon after the change and their DC components are regulated to 45 V without any steady-state error, which is more precisely shown in Fig. 4.14 with a longer period of 5 seconds. No overvoltage or overcurrent appears during the entire transient state.

Fig. 4.15 shows the active power control transient-state waveforms where the DC input

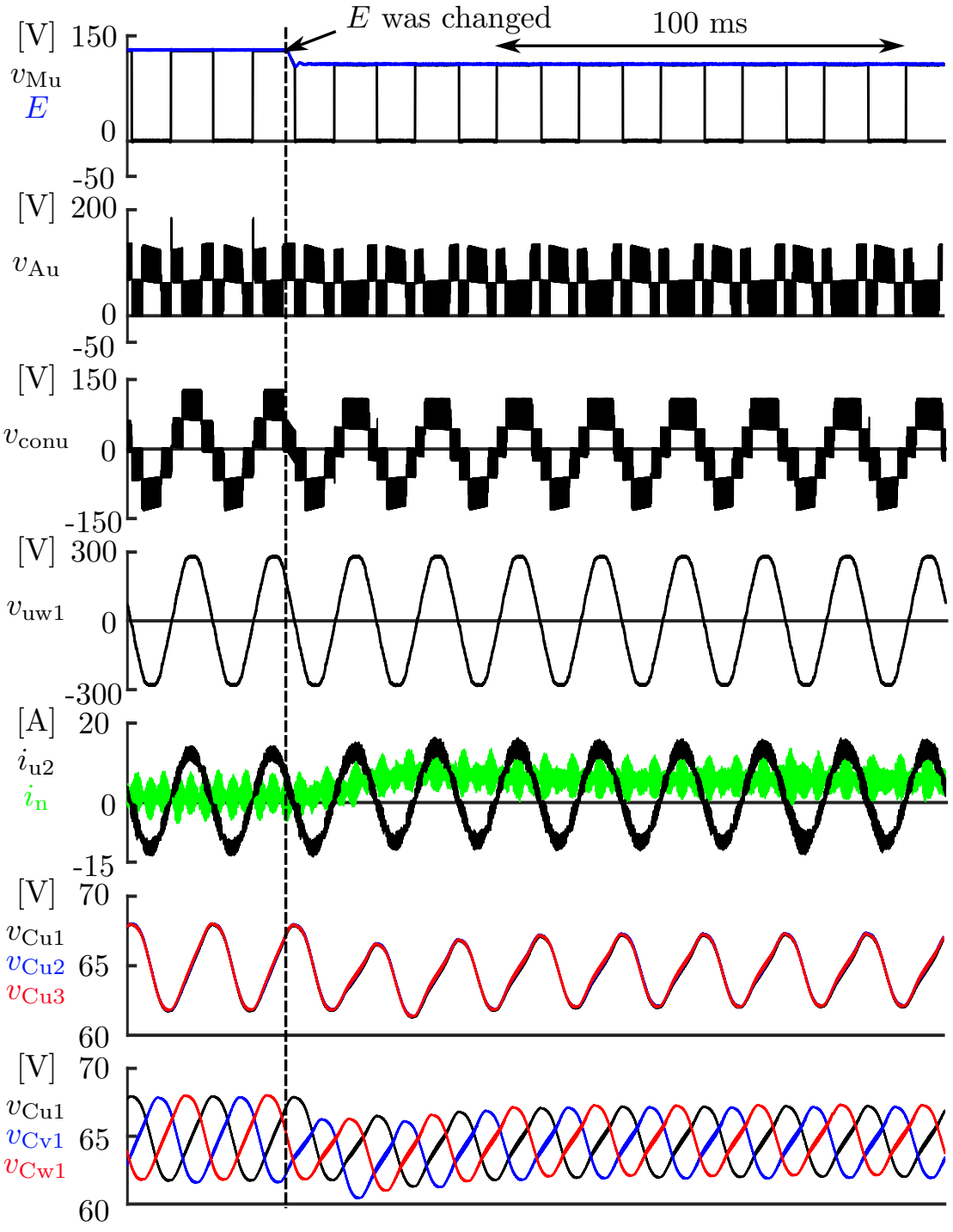


Figure 4.15: Experimental waveforms where E was changed from 130 V to 110 V under ramp change.

voltage was changed from 130 V to 110 V under a ramp change. The capacitor voltage reference was set to 65 V and the active power was 1.5 kW. This sudden voltage change simulates the actual PV array voltage where the DC input voltage of the maximum power point changes because of changes in irradiance and temperature. It also caused the changes in α and I_{dc} and the unbalance of the DC-capacitor voltages. However, the system returned to stable operation soon after the change because of the robust inverter control. This result shows that the proposed inverter could deal with the sudden changes of the DC input voltage, which means that it could easily handle the much slower voltage changes of a PV array.

4.2.5 Reactive Power Control Steady-state Performance

Fig. 4.16 shows the steady-state waveforms where 1.5 kVar reactive power was injected into the grid. The reactive power control is required under grid fault conditions to maintain grid voltage. The waveforms show that i_{u1} lags v_{uw1} by 60° so that the lagging reactive power is provided from the inverter to the grid. Further, the average value of the neutral current i_{n} is zero because no active power is controlled. Experimental waveforms show that the proposed inverter can achieve stable operation under reactive power control.

4.2.6 THD Performance of Downscaled Model

The THD value of the downscaled model is calculated. The data of i_{u1}, which is the grid side u-phase current, are used. The THD values are calculated using MATLAB, and up to the 40^{th}-order harmonic. The THD values of the 85 V and 135 V steady-state cases are 3.132 % and 2.716 %, respectively, which satisfies the requirement of IEEE std 519-2014 [86]. The spectrum of i_{u1} in the 85 V steady-state case is shown in Fig. 4.17. In Fig. 4.17, the spectrum is shown up to the 7^{th}-order harmonic because the magnitudes of higher order harmonics are too small. Besides, the authors believe that the DC component shown in the spectrum was caused by the measurement equipment error.

4.3 Loss and Efficiency Analysis

The loss and efficiency analysis of the proposed inverter with three chopper cells per phase are carried out and they are compared with those of the conventional three-level

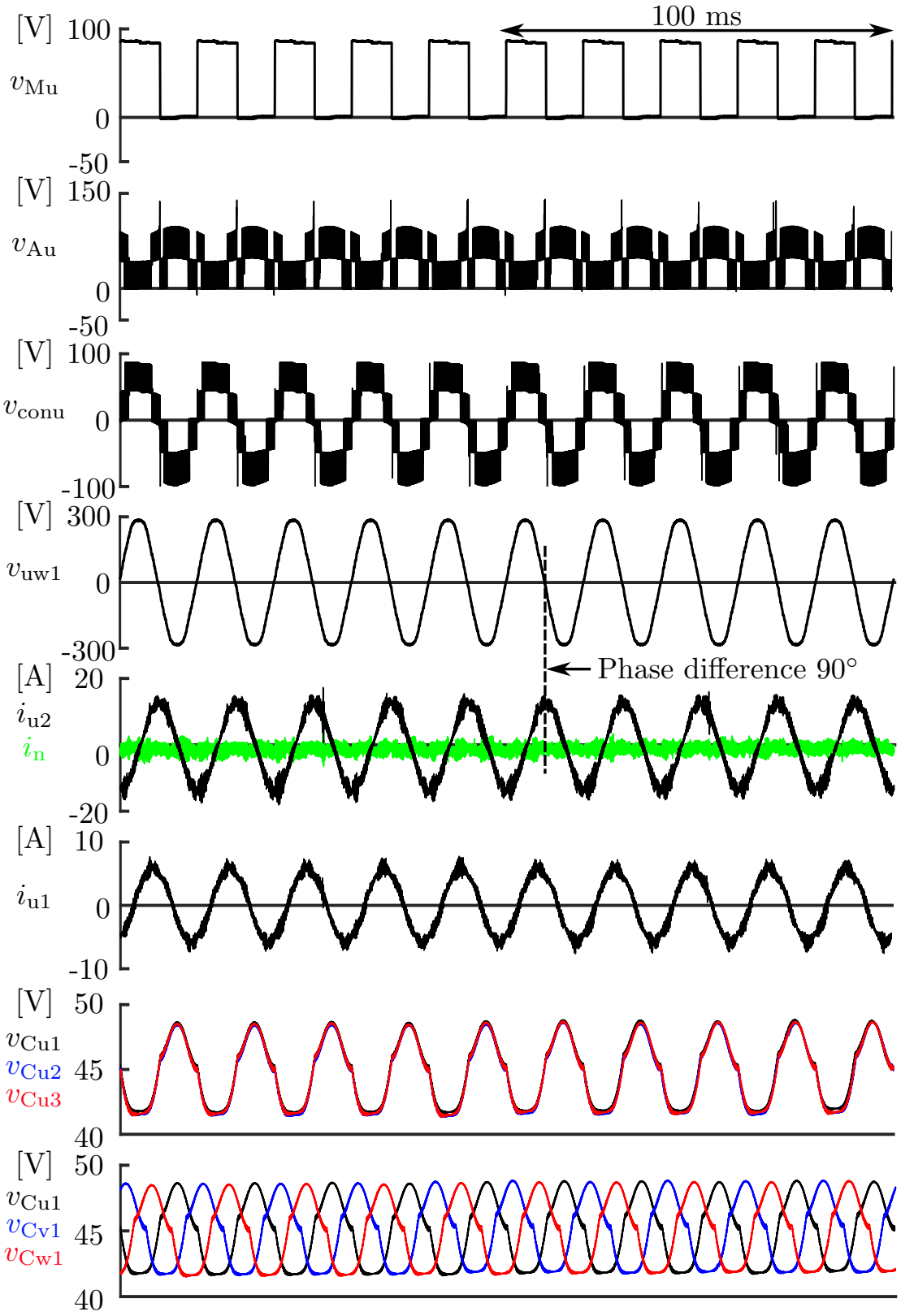


Figure 4.16: Experimental waveforms where 1.5 kVar reactive power was injected to grid.

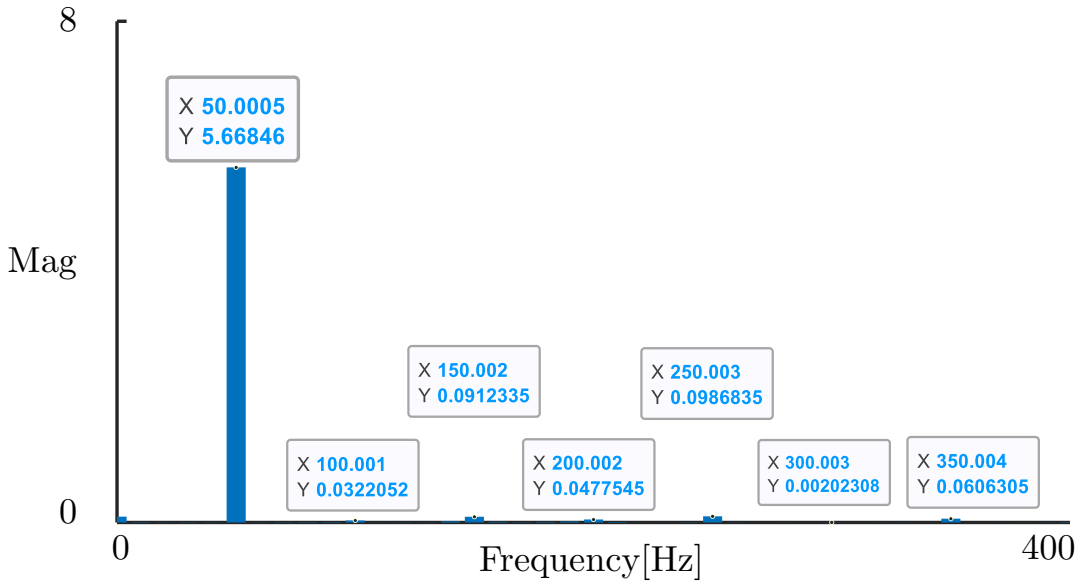


Figure 4.17: Spectrum of i_{u1}.

Table 4.2: Circuit parameters used for loss calculation.

DC input voltage	E	960 V
Secondary line-to-line voltage	$\sqrt{3}V_{\mathrm{ac}}$	1150 V
DC-capacitor voltage	V_C	420 V
Carrier frequency	f_{SA}	2000 Hz

inverter (i.e., T-type inverter), which has been implemented in many cases (e.g., in [31]). It should be noted that the loss in the transformer is not taken into consideration. The switching loss and the conduction loss of the auxiliary converter are considered, while only the conduction loss is considered for the main converter because the switching loss of the main converter with an operating frequency of 50 Hz is negligible. In this section, the analysis and the comparisons are based on active power control cases and the power factor is set to unity. It is assumed that the 3.3-kV IGBT modules 1MBI1000UG-330 from Fuji Electric are used in the main converters and the 1.2-kV IGBT modules CM1000DX-24T from Mitsubishi Electric are used in the auxiliary converters. The parameters used for calculation are obtained from the official data sheets available from the manufacturer homepage.

The loss calculation method of the proposed inverter is based on those shown in [87], [88]; hence, the details will not be shown in this section. Table 4.2 shows the circuit parameters used for loss calculation, and Fig. 4.18 shows the loss breakdown of the proposed inverter. The carrier frequency of each cell was set to $f_{\mathrm{SA}} = 2000$ Hz, which is different

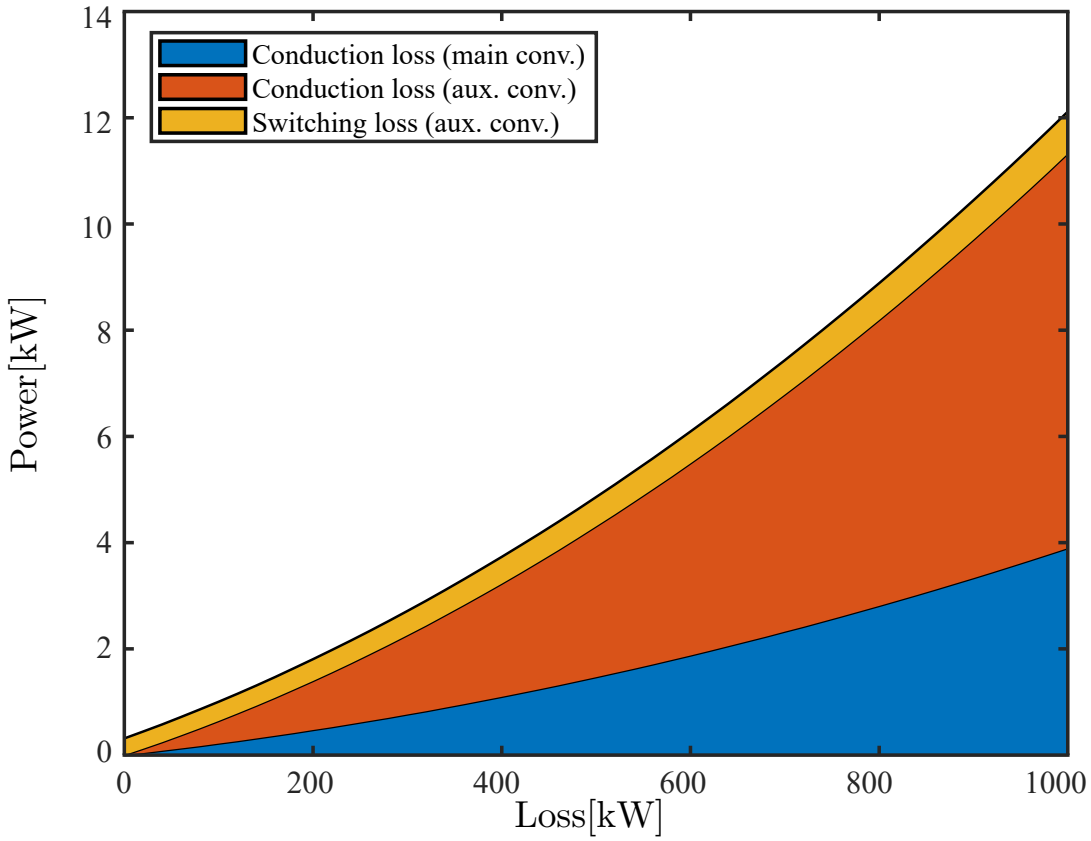


Figure 4.18: Loss breakdown of proposed inverter.

Table 4.3: Parameters of proposed inverter used for comparison with same MPPT range.

DC input voltage	960 V	1100 V	1300 V
DC-capacitor voltage	420 V	450 V	480 V
Secondary line-to-line voltage	1150 V		
MPPT range	960−1300 V		
Carrier freq. (aux.conv.)	2000 Hz		

from the frequency in the experimental verification, and the reason will be explained later. It is obvious from Fig. 4.18 that the switching loss of the proposed inverter is much lower than the conduction loss owing to low V_C and low f_{SA}. The conduction loss of the auxiliary converter is dominant because three power devices are conducting in one operating mode.

The following compares the inverter efficiencies of the proposed inverter and the three-level T-type inverter, where the loss calculation of the three-level T-type inverter is shown in [89]. To conduct a fair comparison, the same 3.3-kV IGBT modules 1MBI1000UG-330 are used for the IGBTs for unidirectional arms, which are T1 and T4 in Fig. 1.5b, and the same 1.2-kV IGBT modules CM1000DX-24T are used for the IGBTs for bidirectional

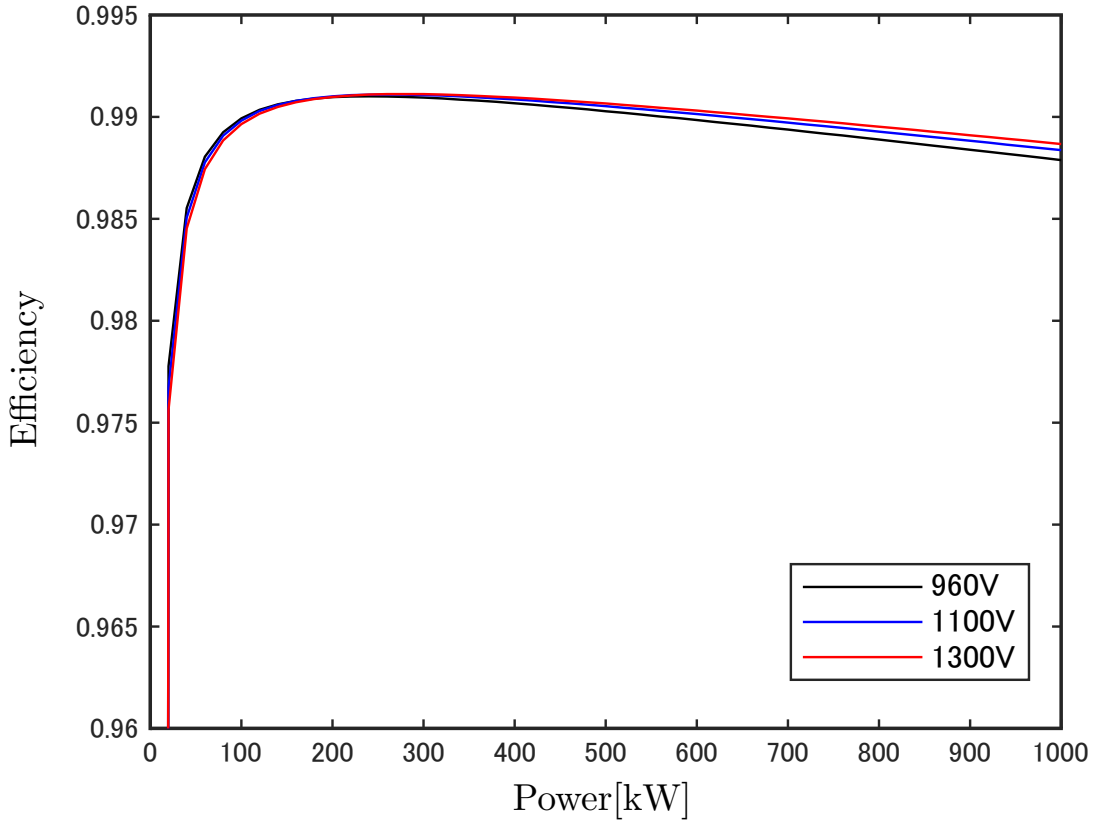


Figure 4.19: Efficiency of proposed inverter when $\sqrt{3}V_{\mathrm{ac}} = 1150\,\mathrm{V}$ with MPPT range of $960-1300\,\mathrm{V}$.

Table 4.4: Parameters of 3-level T-type inverter circuit used for comparison with same MPPT range.

DC input voltage	960 V	1100 V	1300 V
Secondary line-to-line voltage	570 V		
MPPT range	960−1300 V		
Carrier freq.	6 kHz		

Table 4.5: Parameters of proposed inverter used for comparison with same AC voltage.

DC input voltage	480 V	700 V	960 V	1100 V	1300 V
DC-capacitor voltage	220 V	250 V	350 V	380 V	450 V
Secondary line-to-line voltage	570 V				
MPPT range	480−1300 V				
Carrier freq. (aux.conv.)	2 kHz				

switch, which are T2 and T3 in Fig. 1.5b. The carrier frequency of the three-level inverter was set to 6 kHz according to [23] and [25]. The carrier frequency of each cell in Fig. 3.1 was set to 2 kHz so that the equivalent carrier frequency becomes 6 kHz. The following two conditions are set for the comparisons. The first condition is that the two inverters share the same MPPT range of 960 V to 1300 V. In this case, the RMS value of the AC secondary line-to-line voltage of the transformer can be set to 1150 V in the proposed inverter, which is much higher than 570 V in the conventional three-level inverter. Table 4.3 and Table 4.4 summarize the circuit parameters used for comparison under the same MPPT range. It should be noted that the DC-capacitor voltage is changed according to the DC input voltage in the proposed inverter because each chopper cell should produce a maximum voltage of $(E + \sqrt{2}V_{\mathrm{ac}} \sin \alpha)/3$ as shown in (3.10), where 3 is the chopper cell count per phase. Fig. 4.19 shows the efficiency of the proposed inverter under different DC input voltages and Fig. 4.20 shows that of the conventional three-level inverter. It is shown that the proposed inverter can achieve higher efficiency compared with the conventional 3-level inverter, where the maximum efficiency is 99.1 %. The reason of high efficiency originates from lower AC current owing to increased AC voltage.

The second condition is that the AC secondary line-to-line voltages of both inverters are set to the common value of 570 V. In this case, the MPPT range of the proposed inverter is from 480 V to 1300 V, according to (3.6), which is much wider than that of the 3-level inverter, which is from 960 V to 1300 V. Table 4.5 shows the parameters of the proposed inverter used for comparison, and Fig. 4.21 shows the efficiency of the proposed inverter under different DC input voltages. The efficiency of the proposed inverter is decreased compared with that of Fig. 4.19 because of the increased AC current, which is a result of the reduced AC voltage. However, compared with Fig. 4.20, the efficiency is still as high as 98.0 % in the middle power range where the PV inverter most frequently works. In addition, the authors also calculated the efficiency of the conventional three-level T-type inverter coupled with a boost converter. With the help of the boost converter, the T-type

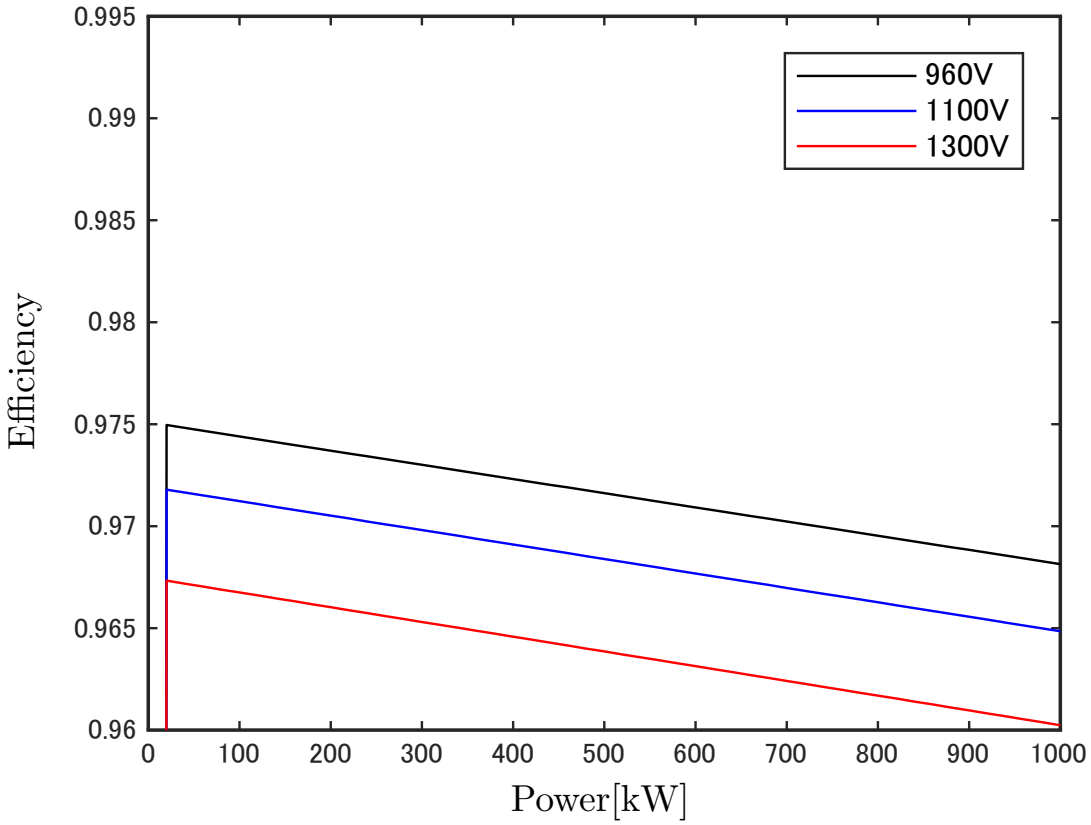


Figure 4.20: Efficiency of 3-level T-type inverter circuit when $\sqrt{3}V_{\mathrm{ac}} = 570\,\mathrm{V}$ with MPPT of $960-1300\,\mathrm{V}$.

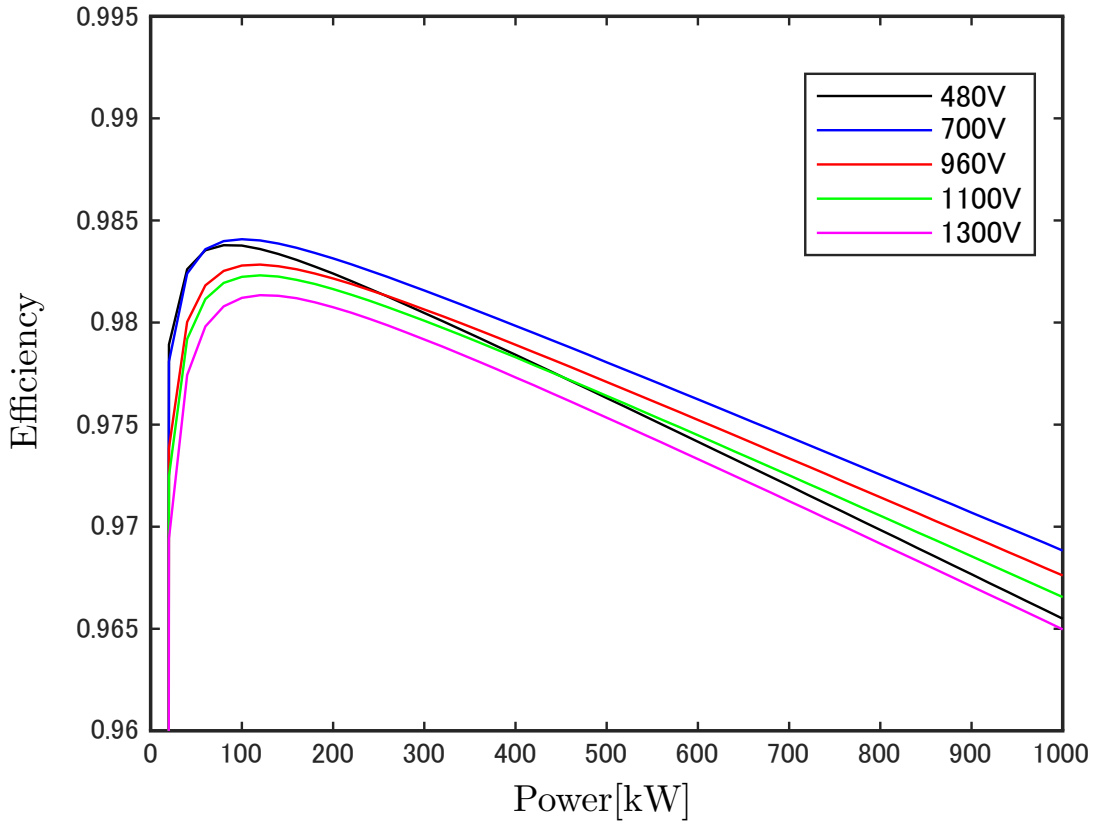


Figure 4.21: Efficiency of proposed inverter when $\sqrt{3}V_{\mathrm{ac}} = 570\,\mathrm{V}$ with MPPT range of $480-1300\,\mathrm{V}$.

inverter could output a line-to-line voltage of $\sqrt{3}V_{\mathrm{ac}} = 1150\,\mathrm{V}$ with the same DC input voltages shown in Fig. 4.20. However, the efficiency becomes lower than what is shown in Fig. 4.20 because of the additional loss introduced by the boost converter.

Furthermore, the proposed inverter could decrease the inductance under the same current ripple. In the proposed inverter, the voltage step change on the inductor during the inverter switching process is V_C. Meanwhile, this value is $E/2$ in the 3-level inverter. When the DC input voltage is 1300 V, the current ripple ratio, which is proportional to the voltage step, is

$$V_C : E/2 = 480 : 1300/2 = 1 : 1.354. \tag{4.6}$$

Equation (4.6) shows that the proposed inverter could reduce the inductance to 74 % that of the 3-level inverter under the same ripple current, which will result in mass, volume, and loss reduction of the inductor.

In addition, the efficiency of the downscaled model in different DC input voltage steady-state operating cases is calculated. The other parameters are the same values shown in Table 4.1. The power was measured by using Newtons4th Ltd PPA5530 power analyzer and the efficiency is calculated based on the obtained experimental data. Fig. 4.22 shows the calculated efficiency. Because the component selection is not optimized in this downscaled model and the loss of the transformer is also included, the efficiency is much lower than the theoretical value shown above. Another reason for the low efficiency is that the switching frequency of each chopper cell of the auxiliary converter is 7.2 kHz in the experiment, while it is 2 kHz in the theoretical analysis to make a fair comparison with the three-level T-type inverter. The increased switching loss also decreases the efficiency.

4.4 Conclusion

This Chapter provides a new individual current control method, which is more suitable to the proposed inverter circuit. Without changing the operation principles of the proposed inverter described in Chapter 3, the performance of the proposed inverter is stable in both low DC input voltage and high DC output voltage cases, which is not achieved with the d-q-0 control method. Different experimental verifications have been carried out to verify the validity of the control method. Further, the loss analysis and the efficiency comparison

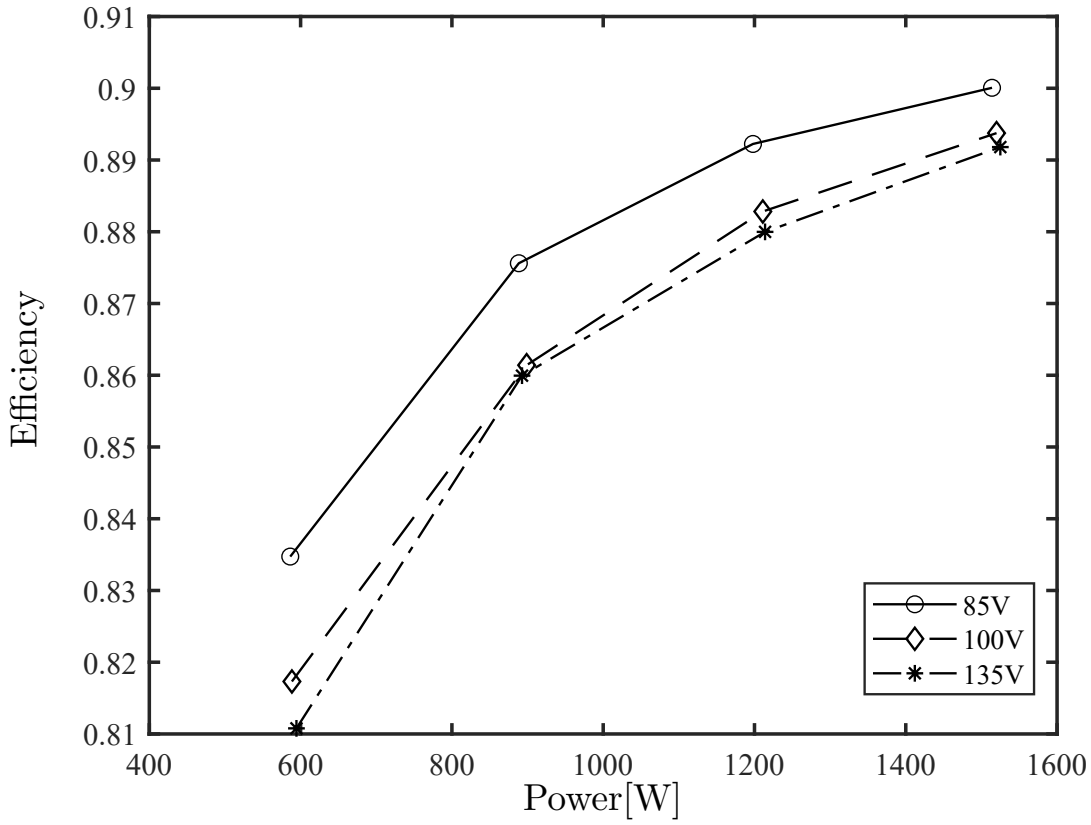
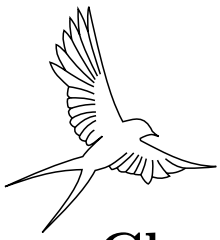


Figure 4.22: Efficiency of downscaled model in different DC input voltage steady-state operating cases.

with that of the conventional three-level T-type inverter are conducted, which shows the high efficiency and the wide MPPT range of the proposed inverter. Even though the cost of the proposed inverter will be higher than the three-level T-type inverter, this is a reasonable trade-off between the efficiency and cost. In addition, the initial charging is achieved without additional circuit.



Chapter 5

LVRT Capability Analysis of Proposed PV Inverter

In Chapter 4, the individual current control is applied to the proposed inverter so that the performance of it is stable both in low DC input voltage case and high DC input voltage. However, the LVRT performance has not been tested and there is no past research focusing on the analysis of the LVRT capability of the proposed inverter under grid faults with experimental verification. This Chapter provides a mathematical-based theoretical analysis of the LVRT capability of the proposed inverter under the grid faults. The theoretical analysis focuses on the LVRT behaviors of the proposed inverter, which includes the capacitor voltage fluctuation, the reason for the overmodulation and the current spikes, and the limit of the LVRT capability/safety operation zone under the SLG fault, considering that the SLG fault is most common which accounts for 75 % to 80 % of the grid faults, according to [90]–[93]. The circuit configuration and the fault position are shown as Fig. 5.1. The SLG fault is assumed to occur at u-phase and the 3P fault is assumed to occur at all three phases. The experimental verification of the LVRT capability of the proposed inverter under the SLG and 3P faults is conducted to prove the reliability of the theoretical analysis. The experimental verification is carried out using the same downscaled model and the fault condition is performed using NF DP045RT, which is a programmable AC power source. It is noteworthy that the fault considered in this chapter is the instantaneous sag defined by IEEE and the duration is set to 5 cycles (100 ms) according to [94].

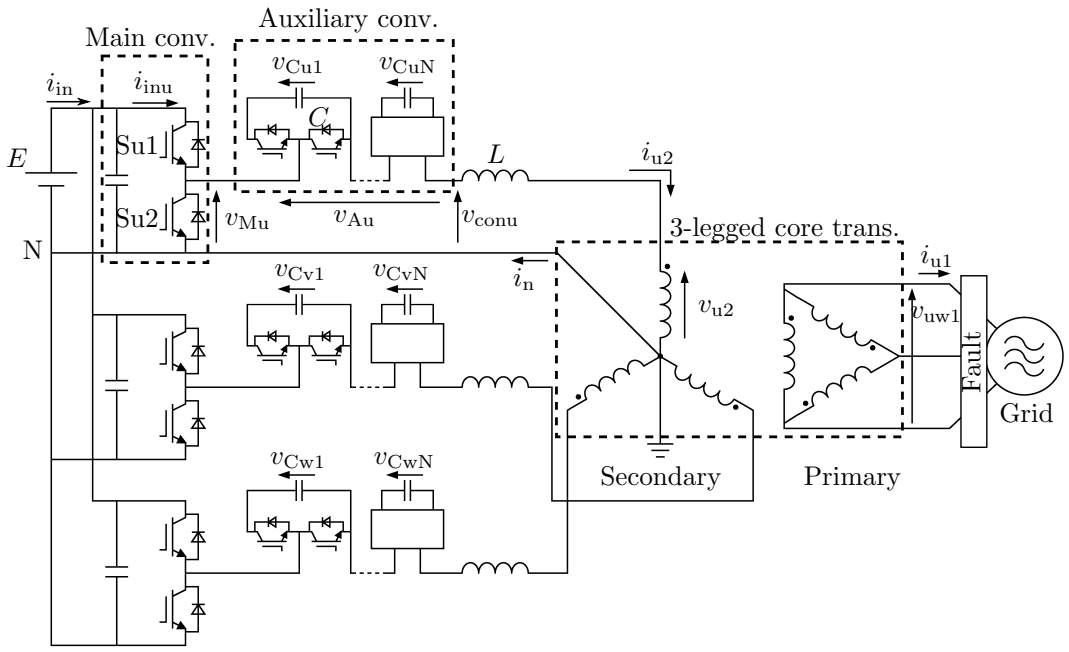


Figure 5.1: Circuit configuration of proposed three-phase PV inverter under grid faults.

5.1 Theoretical Analysis of Capacitor Voltage Fluctuation During SLG Fault

This section only focuses on the theoretical analysis of capacitor voltage fluctuation under the SLG fault because the behaviors under the 3P fault could be analyzed similarly. In this section, the following two assumptions are made; the first assumption is that the leakage inductance and windings resistance of the transformer are zero. If this assumption holds true, the secondary voltage of the transformer is determined only by the grid voltage. The second assumption is that the inductor current of each phase is equal to its reference value without any error, where the generation method of the reference value is provided in Chapter 3.

When the SLG fault happens, the second-order harmonic component will appear in V_{d} and V_{ac} because of unbalanced voltages. This will also affect the values of α and I_{dc} according to (3.31) and (3.32). Consequently, the imbalanced power between the DC and AC sides will cause the DC-capacitor voltage fluctuation in each phase. Because the SLG fault is an asymmetry fault, the DC-capacitor voltage fluctuation of each phase will have different characteristics. In order to protect the proposed inverter circuit from capacitor

overvoltage/undervoltage and operational failure, it is necessary to know the DC-capacitor voltage fluctuation characteristic and the maximum/minimum capacitor voltage. In the followings, firstly, important equations and variables required for the fault analysis are derived. With the derived equations and variables, the DC-capacitor voltages of each phase during the SLG fault will be derived where only their DC components are considered. Furthermore, the AC component of each DC-capacitor voltage will be considered to obtain the maximum/minimum capacitor voltage during the SLG fault.

5.1.1 Derivation of Line-to-neutral Voltage and Inductor Current

In the following, the SLG fault is assumed to occur at the u-phase grid in Fig. 5.1. According to (3.2), (3.3) and (3.4), the primary-side (grid) and the secondary-side voltages of the transformer during the SLG fault are described as

$$\begin{aligned} v_{\mathrm{u1F}} &= \frac{\sqrt{2}m}{\sqrt{3}} V_{\mathrm{grid}} \cos\left(\omega t + \frac{\pi}{6}\right) \\ v_{\mathrm{v1F}} &= \frac{\sqrt{2}}{\sqrt{3}} V_{\mathrm{grid}} \cos\left(\omega t - \frac{\pi}{2}\right) \\ v_{\mathrm{w1F}} &= \frac{\sqrt{2}}{\sqrt{3}} V_{\mathrm{grid}} \cos\left(\omega t - \frac{7\pi}{6}\right), \end{aligned} \tag{5.1}$$

$$\begin{aligned} v_{\mathrm{u2F}} &= \frac{\sqrt{2}m}{2\sqrt{3}a \sin\left(\frac{\pi}{6} - \phi\right)} V_{\mathrm{grid}} \cos\left(\omega t - \phi\right) \\ v_{\mathrm{v2F}} &= \frac{\sqrt{2}m}{2\sqrt{3}a \sin\left(\frac{\pi}{6} - \phi\right)} V_{\mathrm{grid}} \cos\left(\omega t - \frac{2\pi}{3} + \phi\right) \\ v_{\mathrm{w2F}} &= \frac{\sqrt{2}}{\sqrt{3}a} V_{\mathrm{grid}} \cos\left(\omega t - \frac{4\pi}{3}\right), \end{aligned} \tag{5.2}$$

where v_{u1F}, v_{v1F}, and v_{w1F} are the grid line-to-neutral voltages and v_{u2F}, v_{v2F}, and v_{w2F} are the transformer secondary line-to-neutral voltages during the SLG fault, and $\omega = 2\pi f_{\mathrm{SM}}$. m is the voltage sag coefficient and $m \in [0, 1]$. It is notable that a voltage sag of 80 % means that a voltage sag results in 80 % of the voltage remaining [94]. ϕ is the phase jump angle and the following relationship holds true because of the laws of sine:

$$m = \frac{\sin\left(\frac{\pi}{6} - \phi\right)}{\sin\left(\frac{\pi}{6} + \phi\right)}. \tag{5.3}$$

According to (5.2), the transformer secondary voltages of u-phase and v-phase are shifted by the same angle in opposite directions. In contrast, there is no change in that of w-phase.

The voltage sag imposes the second-order harmonic component on the d-axis voltage and decreases its DC component [72], [73], [95]. For the theoretical analysis, only the DC component is considered because the second-order component has little impact on power transfer. In addition, it is assumed that the PLL output is not affected by the voltage sag and it produces the phase information under balanced voltage even during the unbalanced voltage sag [96]. With these assumptions, the d-axis voltage during the SLG fault, which is obtained from Park transformation with the voltages in (5.2), is shown as

$$V_{\mathrm{dF}} = \frac{V_{\mathrm{grid}}}{\sqrt{3}a}(\sqrt{3} - \frac{m}{\sin{(\frac{\pi}{6} - \phi)}}\sin\phi). \tag{5.4}$$

According to (3.3), (3.31), and (3.32), the turn-on (turn-off) angle of the main converter and the DC component of the inductor current during the SLG fault, α_{F} and I_{dcF}, are obtained as

$$\alpha_{\mathrm{F}} = \begin{cases} -\frac{\pi}{2} + \frac{1}{2}\sqrt{\pi^2 - 8 + 4\pi\frac{\sqrt{2}V_{\mathrm{dF}}}{\sqrt{3}E}} & \\ & \text{(ZCS achievable)} \\ 0 & \text{(ZCS not achievable),} \end{cases} \tag{5.5}$$

$$I_{\mathrm{dcF}} = \frac{2\pi I_{\mathrm{ac}} V_{\mathrm{dF}}}{\sqrt{3}E(\pi + 2\alpha_{\mathrm{F}})} - \frac{2\sqrt{2}\cos\alpha_{\mathrm{F}} I_{\mathrm{ac}}}{\pi + 2\alpha_{\mathrm{F}}}. \tag{5.6}$$

In (5.6), I_{ac} is assumed to be the same value as the normal operation and this assumption is valid when the current control works properly. Consequently, the inductor currents during the SLG fault, i_{u2F}, i_{v2F}, and i_{w2F}, are expressed as

$$\begin{aligned} i_{\mathrm{u2F}} &= \sqrt{2}I_{\mathrm{ac}}\cos\omega t + I_{\mathrm{dcF}}, \\ i_{\mathrm{v2F}} &= \sqrt{2}I_{\mathrm{ac}}\cos{(\omega t - \frac{2\pi}{3})} + I_{\mathrm{dcF}}, \\ i_{\mathrm{w2F}} &= \sqrt{2}I_{\mathrm{ac}}\cos{(\omega t - \frac{4\pi}{3})} + I_{\mathrm{dcF}}. \end{aligned} \tag{5.7}$$

5.1.2 Fluctuation of DC-capacitor Voltage

During the SLG fault, the DC-capacitor voltages will fluctuate because of the imbalanced power between the DC and AC sides and this imbalanced power behaves as a power disturbance for the DC-capacitor voltage controller. As explained in Chapter 4, the DC-current reference of u-phase DC-capacitor voltage control, i^*_{udc0}, is determined by the feedback control of $(v_{\mathrm{Cu}})_{\mathrm{dc}}$ and its reference V^*_C, where $(v_{\mathrm{Cu}})_{\mathrm{dc}}$ is the DC component of the average of the capacitor voltages in u-phase, v_{CuAvg}, obtained by an MAF. It should be noted that the relationship $i^*_{\mathrm{udc0}} = 0$ holds ideally under the normal operating condition if the converter loss is negligible. Assuming that i^*_{udc0} equals the actual current, i_{udc0}, the power flowing in the u-phase auxiliary converter originating from $(v_{\mathrm{Au}})_{\mathrm{dc}}$ and i_{udc0} is given by $\Delta p_{\mathrm{Cu}} = (v_{\mathrm{Au}})_{\mathrm{dc}} i_{\mathrm{udc0}}$, where $(v_{\mathrm{Au}})_{\mathrm{dc}}$ is the DC component included in v_{Au} expressed with (3.13). In addition to this power, an additional power $P_{dis\mathrm{u}}$ caused by the fault could flow in the auxiliary converter during the fault. The other two phases could be analyzed in the same way. Hence, the following relationship regarding power holds in the auxiliary converter of each phase during the fault:

$$\begin{aligned}\Delta p_{\mathrm{C}\lambda} + P_{dis\lambda} &= \sum_{j=1}^{N} v_{\mathrm{C}\lambda\mathrm{j}} C \frac{\mathrm{d}v_{\mathrm{C}\lambda\mathrm{j}}}{\mathrm{d}t} \approx C V^*_C \sum_{j=1}^{N} \frac{\mathrm{d}v_{\mathrm{C}\lambda\mathrm{j}}}{\mathrm{d}t} \\ &= N C V^*_C \frac{\mathrm{d}v_{\mathrm{C}\lambda\mathrm{Avg}}}{\mathrm{d}t}, \qquad (\lambda = \mathrm{u}, \mathrm{v}, \mathrm{w}) \end{aligned} \tag{5.8}$$

where $v_{\mathrm{C}\lambda\mathrm{Avg}}$ is the average of the capacitor voltages in each phase. Fig. 5.2 shows the block diagram of DC-capacitor voltage control of each phase considering the power disturbance during the fault. In Fig. 5.2, the delay originating from the MAF is neglected and the relationship $v_{\mathrm{C}\lambda\mathrm{Avg}} = (v_{\mathrm{C}\lambda})_{\mathrm{dc}}$ is assumed to hold for simplifying the analysis, where $(v_{\mathrm{C}\lambda})_{\mathrm{dc}}$ is the DC component of $v_{\mathrm{C}\lambda\mathrm{Avg}}$. Further, a sampling delay originating from the digital control is not considered in Fig. 5.2 and this assumption is reasonable because the response time of the DC-capacitor voltage, the order of which is a few tens of milliseconds or more, is much longer than the sampling period, the order of which is 0.1 milliseconds or less. In addition, the AC component included in the capacitor voltage is excluded in Fig. 5.2.

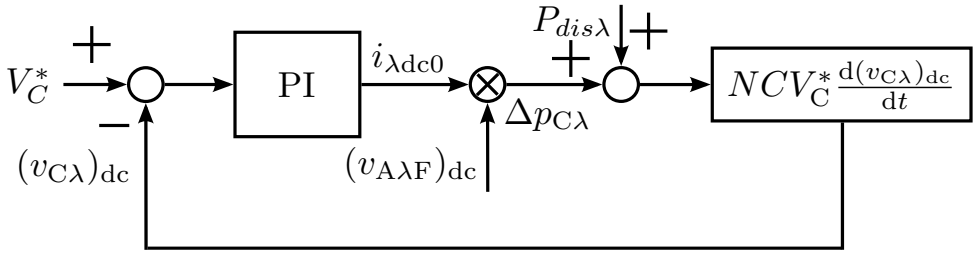


Figure 5.2: Block diagram of DC-capacitor voltage control of each phase considering power disturbance during the fault.

According to Fig. 5.2, the following differential equation is obtained:

$$(K_{\mathrm{vP}}(V_C^* - (v_{\mathrm{C}\lambda})_{\mathrm{dc}}) + \int K_{\mathrm{vI}}(V_C^* - (v_{\mathrm{C}\lambda})_{\mathrm{dc}})\,\mathrm{d}t)(v_{\mathrm{A}\lambda})_{\mathrm{dc}} + P_{dis\lambda} = 3CV_C^* \frac{\mathrm{d}(v_{\mathrm{C}\lambda})_{\mathrm{dc}}}{\mathrm{d}t}. (\lambda = \mathrm{u, v, w}) \tag{5.9}$$

In (5.9), the relationship $N = 3$ is used. It is assumed that $(v_{\mathrm{AuF}})_{\mathrm{dc}} \approx (v_{\mathrm{Au}})_{\mathrm{dc}}$ during the first cycle during the SLG fault. K_{vP} and K_{vI} are the proportional and integral coefficients of the DC-capacitor voltage control, respectively. $P_{dis\lambda}$ is the power disturbance of each phase and can be calculated as

$$P_{dis\lambda} = \frac{1}{T}(\int_0^T v_{\mathrm{M}\lambda} i_{\lambda 2\mathrm{F}}\,\mathrm{d}t - \int_0^T v_{\lambda 2\mathrm{F}} i_{\lambda 2\mathrm{F}}\,\mathrm{d}t). (\lambda = \mathrm{u, v, w}) \tag{5.10}$$

The first term on the right-hand side in (5.10) corresponds to the average DC input power and the second term corresponds to the average AC output power. By solving (5.9), the theoretical average DC-capacitor voltage of each phase in t domain is obtained as the following equation where $t = 0$ corresponds to the time when the fault happens.

$$X = \frac{\sqrt{K_{\mathrm{vP}}^2 (v_{\mathrm{A}\lambda})_{\mathrm{dc}}^2 - 12CV_C^* K_{\mathrm{vI}}(v_{\mathrm{A}\lambda})_{\mathrm{dc}}}}{6CV_C^*}, \tag{5.11}$$

$$Y = \frac{K_{\mathrm{vP}}(v_{\mathrm{A}\lambda})_{\mathrm{dc}}}{6CV_C^*}, \tag{5.12}$$

$$(v_{\mathrm{C}\lambda})_{\mathrm{dc}} = V_C^* - \frac{P_{dis\lambda}}{\sqrt{K_{\mathrm{vP}}^2 (v_{\mathrm{A}\lambda})_{\mathrm{dc}}^2 - 12CV_C^* K_{\mathrm{vI}}(v_{\mathrm{A}\lambda})_{\mathrm{dc}}}} * (e^{t(-X-Y)} - e^{t(X-Y)}). \quad (\lambda = \mathrm{u, v, w}) \tag{5.13}$$

By calculating $P_{dis\lambda}$, it is found out that the DC-capacitor voltages of u-phase and

v-phase will increase and that of w-phase will decrease at the beginning of the SLG fault because the relationships $P_{dis\mathrm{u}} > 0$, $P_{dis\mathrm{v}} > 0$ and $P_{dis\mathrm{w}} < 0$ are always true when the SLG fault happens at the primary side of u-phase. Because of the PI regulator, the DC-capacitor voltages will be regulated to the reference value V_C^* with the passage of time.

5.1.3 Derivation of Capacitor Voltage Including AC Component

Since the capacitors are charged and discharged every cycle, it is also necessary to take the charging/discharging process (AC component) into consideration to obtain the maximum (u-phase and v-phase)/minimum (w-phase) capacitor voltage. However, the complicated operating principles under the SLG fault will cause the equations unsolvable. In order to simplify the analysis process, an assumption that the SLG fault does not affect the AC component of capacitor voltages was introduced. In other words, the AC component during the fault is assumed to be equal to the one during the normal condition. The AC component of the u-phase capacitor voltages is denoted as $(v_{\mathrm{Cu}})_{\mathrm{ac}}$ and the following equation is obtained according to Figs. 5.1 and 3.2:

$$v_{\mathrm{Au}} i_{\mathrm{u2}} = 3C(V_C^* + (v_{\mathrm{Cu}})_{\mathrm{ac}}) \frac{\mathrm{d}(v_{\mathrm{Cu}})_{\mathrm{ac}}}{\mathrm{d}t} \approx 3CV_C^* \frac{\mathrm{d}(v_{\mathrm{Cu}})_{\mathrm{ac}}}{\mathrm{d}t}. \tag{5.14}$$

The relationship $N = 3$ is used in (5.14). Equation (5.14) can be solved by substituting (3.9) and (3.17) into it and $(v_{\mathrm{Cu}})_{\mathrm{ac}}$ is derived as:

$$(v_{\mathrm{Cu}})_{\mathrm{ac}} = \begin{cases} \frac{(EI_{\mathrm{dc}} - V_{\mathrm{ac}} I_{\mathrm{ac}})\theta}{3\omega CV_C^*} + \frac{\sqrt{2}(EI_{\mathrm{ac}} - V_{\mathrm{ac}} I_{\mathrm{dc}}) \sin\theta}{3\omega CV_C^*} \\ \qquad - \frac{V_{\mathrm{ac}} I_{\mathrm{ac}} \sin 2\theta}{6\omega CV_C^*} \\ \qquad (-\frac{\pi}{2} - \alpha \le \theta \le \frac{\pi}{2} + \alpha) \\ -\frac{V_{\mathrm{ac}} I_{\mathrm{ac}} \theta}{3\omega CV_C^*} - \frac{\sqrt{2} V_{\mathrm{ac}} I_{\mathrm{dc}} \sin\theta}{3\omega CV_C^*} - \frac{V_{\mathrm{ac}} I_{\mathrm{ac}} \sin 2\theta}{6\omega CV_C^*} \\ \quad + \frac{EI_{\mathrm{dc}}}{3\omega CV_C^*}(\frac{\pi}{2} + \alpha) + \frac{\sqrt{2} EI_{\mathrm{ac}}}{3\omega CV_C^*} \sin(\frac{\pi}{2} + \alpha). \\ \qquad (\frac{\pi}{2} + \alpha < \theta < \frac{3\pi}{2} - \alpha) \end{cases} \tag{5.15}$$

θ is the phase angle of v_{u2} shown in (3.2) and the voltage of the u-phase capacitor during the SLG fault is the sum of $(v_{\mathrm{Cu}})_{\mathrm{dc}}$, obtained from (5.13), and $(v_{\mathrm{Cu}})_{\mathrm{ac}}$. The voltages of the v-phase and w-phase capacitors could be obtained in the same way. The comparison of the theoretical value and the experimental data will be carried out in Section 5.3.

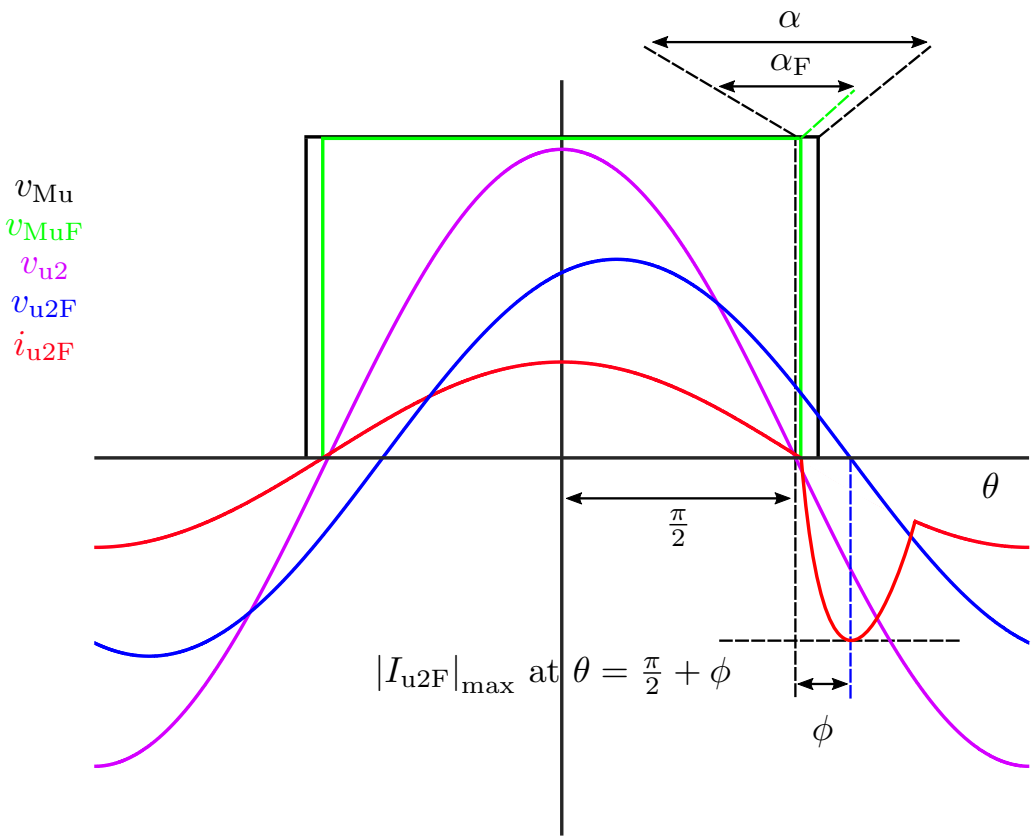


Figure 5.3: Theoretical waveforms of u-phase current and voltages.

5.2 Theoretical Analysis of Overmodulation and Current Spike During SLG Fault

5.2.1 Reasons for Overmodulation and Current Spike

As explained in Section 5.1, a phase jump angle ϕ will appear in v_{u2F} and v_{v2F}, according to (5.2). However, the PLL output is not affected by the voltage sag and it produces the phase information under balanced voltage even during the unbalanced voltage sag, which makes that the main converter will still operate based on the phase information without the SLG fault. Therefore, the output voltage of the main converter of u-phase and v-phase during the SLG fault, v_{MuF} and v_{MvF}, will not be in phase with v_{u2F} and v_{v2F}, respectively.

The theoretical waveforms of voltages and current of u-phase during the SLG fault are shown in Fig. 5.3. According to (5.2), the amplitude of v_{u2F} will decrease and the phase will shift to right by ϕ compared with v_{u2}. In addition, the turn on/off angle

of the main converter in this case, α_{F}, will be smaller than or equal to α in (3.31), according to (5.5), which results in a smaller duty cycle v_{MuF} shown in Fig. 5.3. If $\alpha_{\mathrm{F}} \geq \phi$ holds true in this case, the inverter will still operate safely even though there is a phase difference. Unfortunately, with the decrease of the voltage sag coefficient (voltage sag becomes serious), $\alpha_{\mathrm{F}} < \phi$ will hold true eventually. In this case, the auxiliary converter will be forced to output a negative voltage according to (3.1), which is impossible for a chopper-cell cascaded converter. Therefore, overmodulation will happen and the negative voltage, $-v_{\mathrm{u2F}}$, will be imposed on the inductor resulting in a negative current spike, where $\theta \in [\pi/2 + \alpha_{\mathrm{F}}, \pi/2 + \phi]$ in Fig. 5.3. The relationship between the variation of i_{u2F}, Δi_{u2F}, and v_{u2F} is shown as:

$$\omega(L+l)\frac{\mathrm{d}\Delta i_{\mathrm{u2F}}}{\mathrm{d}\theta} = -v_{\mathrm{u2F}}.\ (\pi/2 + \alpha_{\mathrm{F}} \leq \theta \leq \pi/2 + \phi) \tag{5.16}$$

L is the inductor value and l is the leakage inductance of the transformer. Since the value of v_{u2F} is decreasing in this region, the gradient of Δi_{u2} will increase and equal zero at $\theta = \pi/2 + \phi$, which also means i_{u2F} reaches its maximum absolute value, $|i_{\mathrm{u2F}}|_{\mathrm{Max}}$. The theoretical waveform of i_{u2F} is shown in Fig. 5.3.

Similarly, theoretical waveforms of voltages and current of v-phase during the SLG fault are shown in Fig. 5.4. It is noteworthy that Fig. 5.3 and Fig. 5.4 do not share the same x-axis. When it comes to the case of v-phase, the values of α_{F}, and the amplitudes of the voltage and the current will not change. However, the waveform of v_{v2F} will shift to left by ϕ in this case, which is obvious from (5.2). This will also cause overmodulation of the v-phase auxiliary converter, where $\theta \in [-\pi/2 - \phi, -\pi/2 - \alpha_{\mathrm{F}}]$ in Fig. 5.4. However, since the value of v_{v2F} is increasing in this case, the gradient of the negative current spike of i_{v2F} will keep decreasing until the main converter output becomes positive, where $\theta = -\pi/2 - \alpha_{\mathrm{F}}$. Similarly, the relationship is obtained:

$$\omega(L+l)\frac{\mathrm{d}\Delta i_{\mathrm{v2F}}}{\mathrm{d}\theta} = -v_{\mathrm{v2F}},\ \ (-\pi/2 - \phi \leq \theta \leq -\pi/2 - \alpha_{\mathrm{F}}) \tag{5.17}$$

and i_{v2F} reaches its maximum absolute value, $|i_{\mathrm{v2F}}|_{\mathrm{Max}}$, at $\theta = -\pi/2 - \alpha_{\mathrm{F}}$.

The overmodulation can also happen to w-phase, but that is caused by the DC-voltage fluctuation. As explained in Section 5.1, if the DC-capacitor voltage of w-phase drops too much during the SLG fault, the auxiliary converter may not be able to output the required

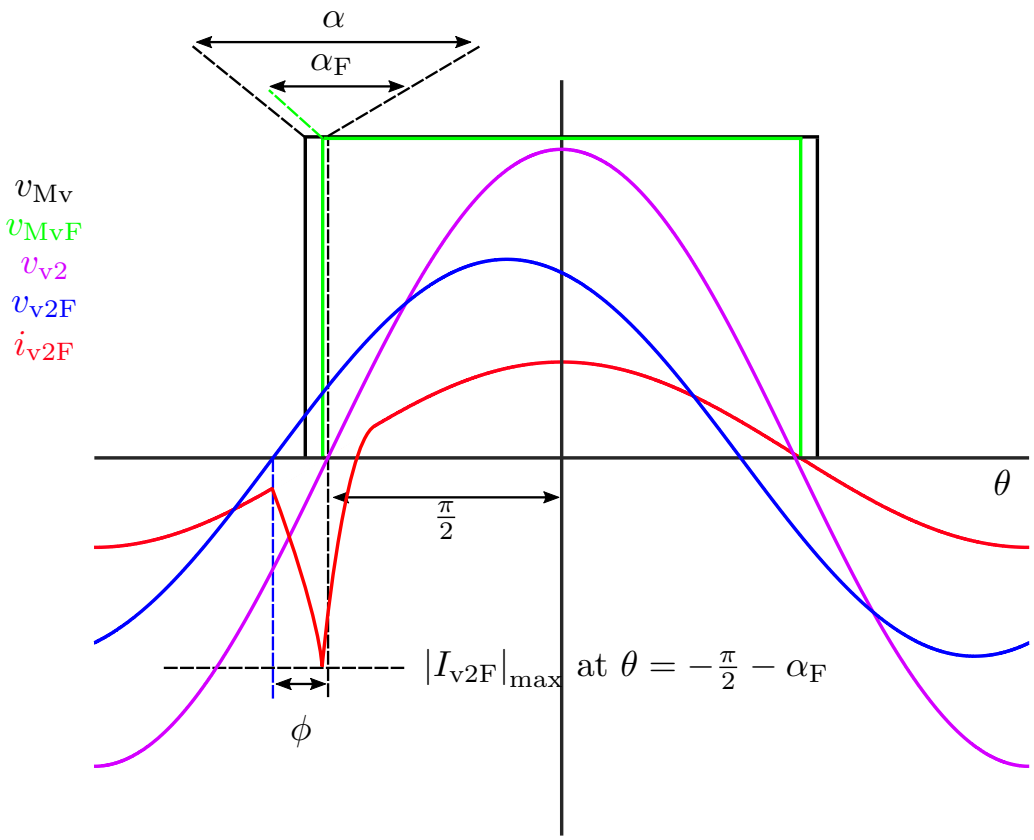


Figure 5.4: Theoretical waveforms of v-phase current and voltages.

voltage resulting in overmodulation. However, this could be prevented by increasing the reference value of the DC-capacitor voltage. In contrast, the overmodulation of u-phase and v-phase will definitely happen when the voltage sag becomes more and more serious.

5.2.2 Overmodulation Borderline

As explained above, the overmodulation of u-phase and v-phase is unpreventable when serious voltage sag happens during the SLG fault. Therefore, it is necessary to figure out the borderline where the overmodulation will happen.

According to the explanation above, the borderline of the overmodulation of u-phase and v-phase is:

$$\phi = \alpha_{\mathrm{F}}. \tag{5.18}$$

Equation (5.18) can be solved by substituting (5.2), (5.3), (5.4) and (5.5) into it and using reasonable approximations of $\sin\phi \cong \phi$ and $\cos\phi \cong 1 - \frac{\phi^2}{2}$. The solving process is too

complicated and too long. Therefore, the detail of the solving process is left out in this Chapter. The result of the substituting and simplifying is a quartic equation shown as:

$$
\begin{aligned}
&a_4x^4 + a_3x^3 + a_2x^2 + a_1x + a_0 = 0,\\
&a_4 = -216 + 108\pi y,\\
&a_3 = (144\pi - 18\sqrt{3}\pi^2)y - 432,\\
&a_2 = -9\pi^2y^2 + (108\pi - 24\sqrt{3}\pi^2)y - 360 + 18\pi^2,\\
&a_1 = -6\pi^2y^2 + (96\pi - 6\sqrt{3}\pi^2)y + 36\pi^2 - 288,\\
&a_0 = -\pi^2y^2 + 24\pi y + 18\pi^2 - 144,\\
&x = \frac{1+m}{1-m},\\
&y = \frac{\sqrt{2}V_{\text{grid}}}{\sqrt{3}aE}.
\end{aligned}
\tag{5.19}
$$

Considering the overmodulation will definitely happen when the voltage sag coefficient m is small enough, there is at least one real solution for (5.19). Obviously, the variable x in (5.19) is large than or equal to one and the overmodulation will not disappear with the decrease of m. Therefore, the largest real solution of x is the solution for the borderline problem and the solution is shown as:

$$
\begin{aligned}
&x = -\frac{a_3}{4a_4} + \frac{\sqrt{b_1}}{2} + \frac{\sqrt{b_4}}{2},\\
&b_1 = \frac{b_3}{4\sqrt{b_4}} + \frac{a_3^2}{2a_4^2} - \frac{2^{\frac{1}{3}}b_5}{3b_8^{\frac{1}{3}}a_4} - \frac{b_8^{\frac{1}{3}}}{3*2^{\frac{1}{3}}a_4} - \frac{4a_2}{3a_4},\\
&b_3 = -\frac{a_3^3}{a_4^3} + \frac{4a_2a_3}{a_4^2} - \frac{8a_1}{a_4},\\
&b_4 = \frac{a_3^2}{4a_4^2} + \frac{2^{\frac{1}{3}}b_5}{3b_8^{\frac{1}{3}}a_4} + \frac{b_8^{\frac{1}{3}}}{3*2^{\frac{1}{3}}a_4} - \frac{2a_2}{3a_4},\\
&b_5 = a_2^2 - 3a_1a_3 + 12a_0a_4,\\
&b_6 = 2a_2^3 - 9a_1a_2a_3 + 27a_0a_3^2 + 27a_1^2a_4 - 72a_0a_2a_4,\\
&b_7 = -4b_5^3 + b_6^2,\\
&b_8 = b_6 + \sqrt{b_7}.
\end{aligned}
\tag{5.20}
$$

In every operation case, x can be obtained by providing, V_{grid}, a, and E. Consequently, the borderline voltage sag coefficient m could be obtained. Therefore, the borderline voltage

sag where the overmodulation of u-phase and v-phase can be calculated, theoretically. The theoretical result will be examined using the experimental data in Section 5.3. In addition, if α is already zero in (3.31) in normal operation, the overmodulation of u-phase and v-phase will happen no matter how slight the voltage sag is.

5.2.3 Peak Value of Current Spike

With (5.19) and (5.20), the borderline where the overmodulation of u-phase and v-phase will happen could be obtained. However, the overmodulation does not mean operational failure of the proposed inverter circuit during the SLG fault because the inductor can also compensate for the voltage that the auxiliary converter cannot output. Therefore, whether an operational failure will happen is determined by the peak values of the u-phase and v-phase current spikes shown in Figs. 5.3 and 5.4. If either of the peak values triggers the overcurrent protection, which means that it reaches the overcurrent limit, the operational failure will happen. With the results obtained above, Δi_{u2F} and Δi_{v2F} in equations (5.16) and (5.17) can be solved. Therefore, the peak values of the current spike of u-phase and v-phase are the sum of their variation and their value when the overmodulation happens, respectively, which are obtained as:

$$|i_{\mathrm{u2F}}|_{\mathrm{Max}} = \frac{\sqrt{2}m(1-\cos(\alpha_{\mathrm{F}}-\phi))}{2\sqrt{3}a\omega(L+l)\sin(\frac{\pi}{6}-\phi)}V_{\mathrm{grid}}, \tag{5.21}$$

$$\begin{aligned}|i_{\mathrm{v2F}}|_{\mathrm{Max}} = &\frac{\sqrt{2}m(1-\cos(\alpha_{\mathrm{F}}-\phi))}{2\sqrt{3}a\omega(L+l)\sin(\frac{\pi}{6}-\phi)}V_{\mathrm{grid}} \\ &-\sqrt{2}I_{\mathrm{ac}}\cos(-\frac{\pi}{2}-\phi)-I_{\mathrm{dcF}}.\end{aligned} \tag{5.22}$$

It is notable that the absolute values are used for peak values and the value of i_{u2F} when the overmodulation happens is zero. Therefore, $|i_{\mathrm{v2F}}|_{\mathrm{Max}}$ is larger than $|i_{\mathrm{u2F}}|_{\mathrm{Max}}$ in most cases, and the overcurrrent of v-phase is more likely to happen during the SLG fault. The comparison between the experimental data and theoretical values will be conducted in Section 5.3. In addition, the experiment system data are used to calculate the peak values in different SLG fault cases in Section 5.3 for the evaluation of the LVRT capability of the proposed inverter.

Table 5.1: Circuit Parameters Used for Experiments.

Active power reference	p^*	1.5 kW
Reactive power reference	q^*	0
DC input voltage	E	85 V or 135 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	3
DC-capacitor voltage	V_{C}	45 V or 60 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	7.2 kHz
Fault duration	t_{F}	100 ms

5.3 Experiment

5.3.1 Experimental Conditions

The same downscaled system was used for experiments and the circuit parameters are summarized in Table 5.1. The DC input voltage corresponding to the PV array voltage, E, was produced using NF DP030RS. The SLG fault (u-phase) and the 3P fault were performed on the primary side of the transformer shown as Fig. 5.1 using NF DP045RT, which is a programmable AC power source. According to IEEE Std 1159-2019 [94], the fault duration, t_{F}, was set to 100 ms. The reference value of the active power was 1.5 kW and the reference value of reactive power was zero. The reference value of the DC-capacitor voltage was set to 45 V when the DC input voltage was 85 V and was set to 60 V when the DC input voltage was 135 V considering (3.11). The deadtime was set to 4.0 µs for the main and the auxiliary converters. The voltage ratio of the transformer was set to $a = 2$.

The control system is composed of a digital signal processor unit utilizing Texas Instruments TMS320C6678 and a field programmable gate array unit utilizing Altera Cyclone IV. The voltage and current waveforms were measured using Textronix DPO4104B-L with a frequency band of 1 GHz, Textronix MDO4104C with a frequency band of 1 GHz, and Hioki Memory Hicoder 8861-50.

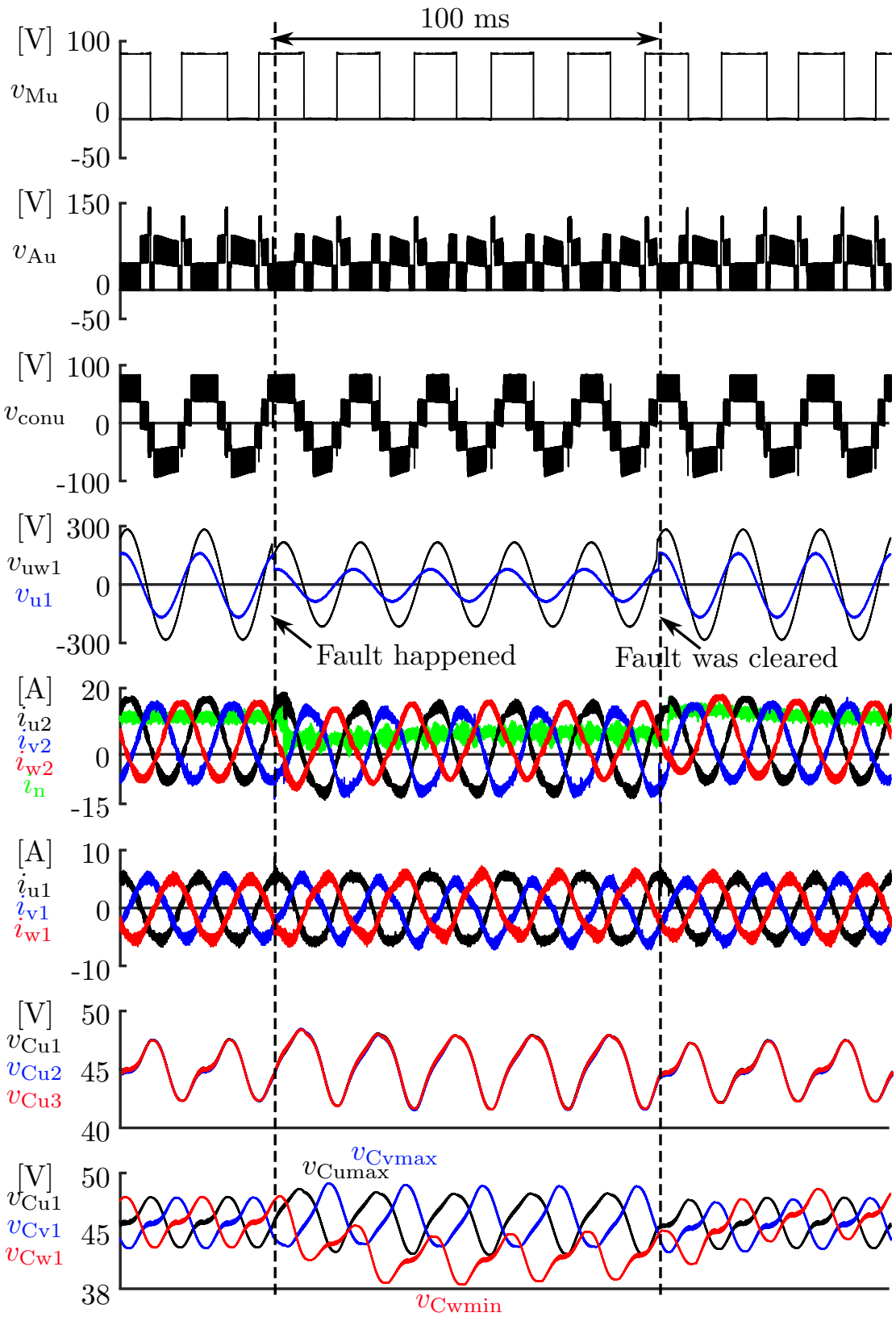


Figure 5.5: Experimental waveforms during SLG faults where $E = 85\,\mathrm{V}$ and v_{u1} dropped by 50 %.

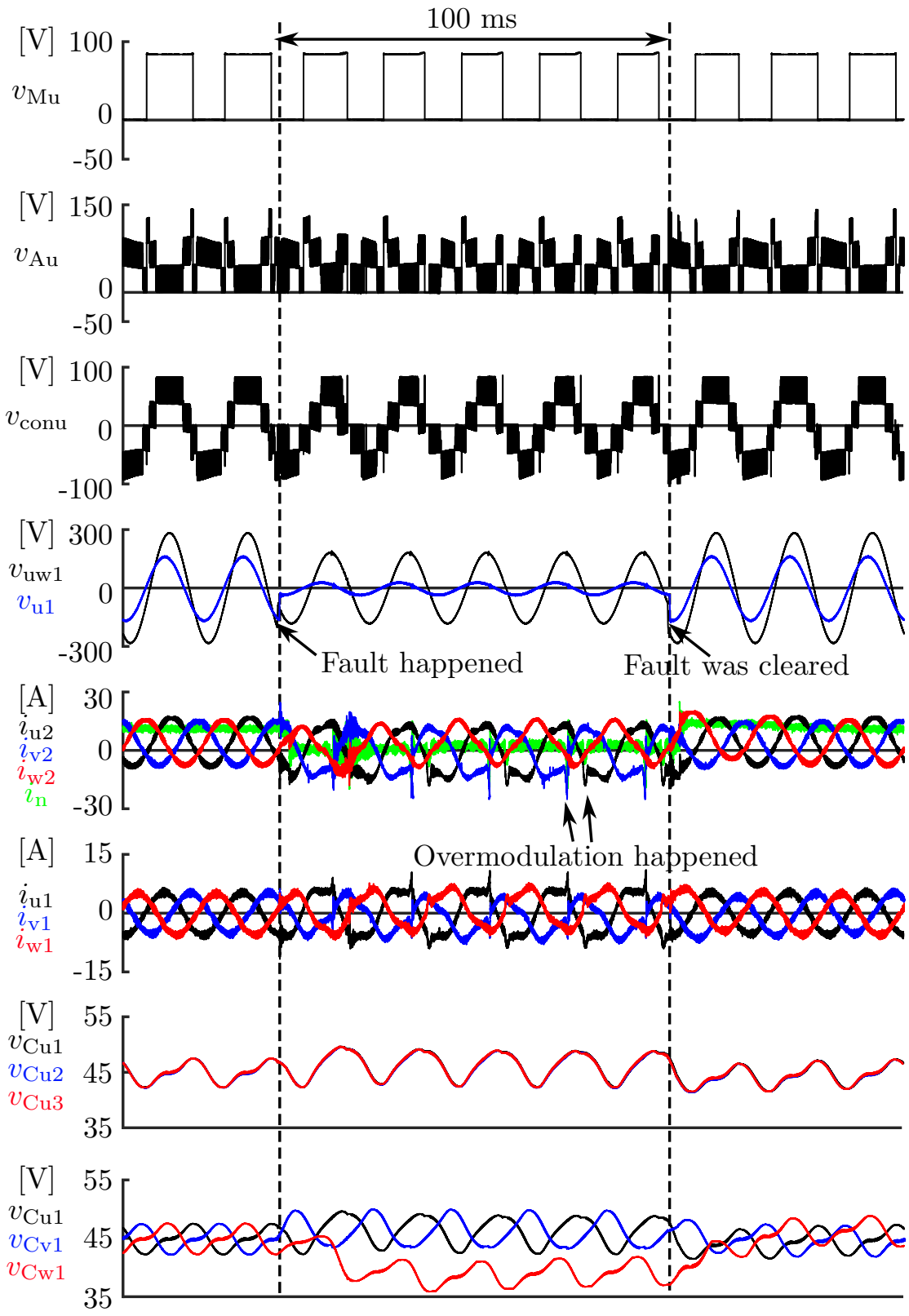


Figure 5.6: Experimental waveforms during SLG faults where $E = 85\,\mathrm{V}$ and v_{u1} dropped by 80 %.

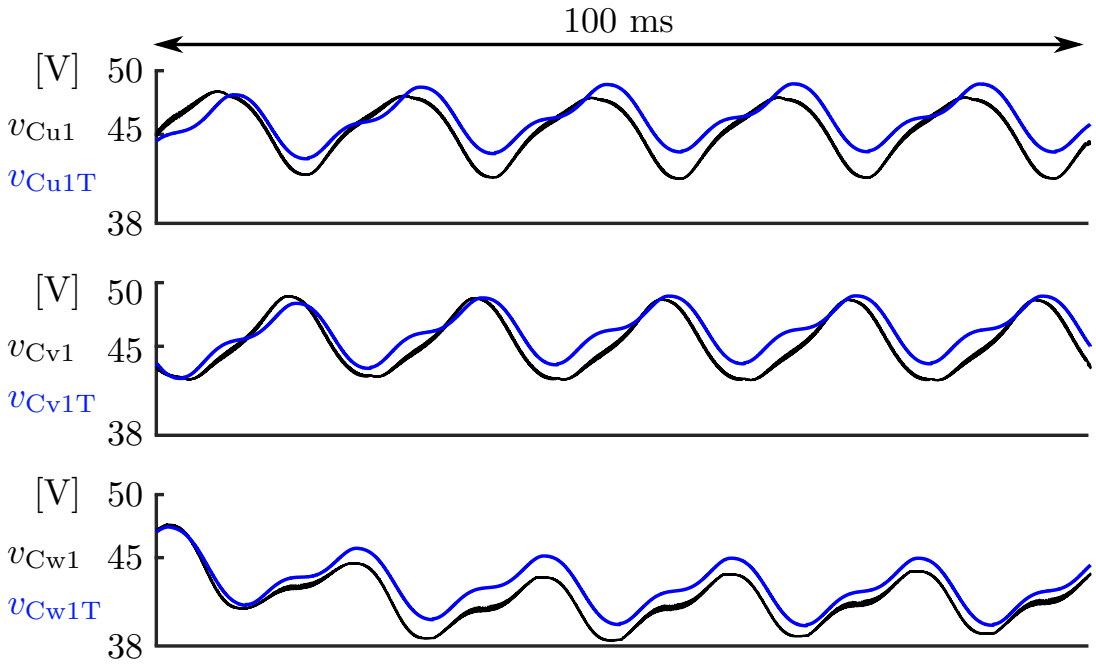


Figure 5.7: Comparison of experimental capacitor voltages and theoretical capacitor voltages during SLG fault.

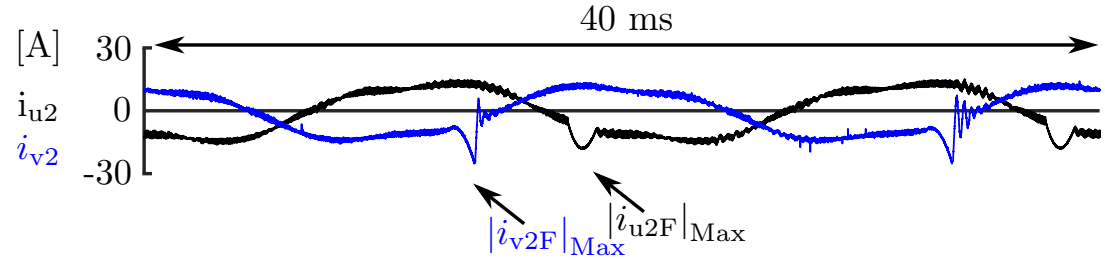


Figure 5.8: Zoomed in waveforms of current spikes in u-phase and v-phase of Fig. 5.6.

5.3.2 LVRT Capability Performance During SLG Fault

Figs. 5.5 and 5.6 show the experimental waveforms of the proposed inverter circuit during the SLG fault (u-phase) where $E = 85\,\mathrm{V}$. During the SLG fault, the amplitude of v_{u1} dropped by 50 % in Fig. 5.5. A voltage sag and a phase jump occurred in v_{uw1} because of the Y-Δ connection. The value of the neutral line current i_n decreased during the fault because I_{dcF} is smaller than I_{dc}, which can be obtained from (3.32) and (5.6). The theoretical value of i_n during the SLG fault is obtained as three times of I_{dcF}, which is 5.74 A. The DC components for DC-capacitor voltage control, i_{udc0}, i_{vdc0}, and i_{wdc0} are not considered, and this theoretical value is the same as the average experimental value of i_n during the SLG fault, which is 5.74 A. The 50-Hz component of each phase current

during the fault is the same as the one during the normal condition, while some low-order frequency components originate from the imbalanced voltages, which are not considered in the theoretical analysis. Consequently, these low-order frequency components also appeared in i_{u1}, i_{v1}, and i_{w1}, which are the grid currents.

The DC-capacitor voltage data of Fig. 5.5 is used for verifying the validity of the theoretical analysis in Section 5.1. The DC-capacitor voltages of u-phase and v-phase increase following the fault occurrence while that of w-phase decreases, which agrees well with the conclusion obtained in Section 5.1. The comparison of the experimental capacitor voltages and theoretical capacitor voltages during the SLG fault is shown in Fig. 5.7. v_{Cu1}, v_{Cv1}, and v_{Cw1} are the experimental capacitor voltage waveforms, which are the same waveforms shown in Fig. 5.5 between the dotted lines, and v_{Cu1T}, v_{Cv1T}, and v_{Cw1T} are the theoretical capacitor voltage waveforms during the SLG fault. The errors are caused by the following reasons. Firstly, the effect of MAF is not considered in theory, whereas it is used in experiments. Secondly, the difference between the initial capacitor voltage in each phase when the fault happens will affect the value of the initial DC voltage where (5.13) assumes that the initial DC component of each phase is V_C^*. The theoretical maximum/minimum values of the capacitor voltages (including AC component) are obtained from (5.13) and (5.15) as

$$\begin{cases} v_{\mathrm{CumaxT}} = 49.0\,\mathrm{V} \\ v_{\mathrm{CvmaxT}} = 49.0\,\mathrm{V} \\ v_{\mathrm{CwminT}} = 39.6\,\mathrm{V}. \end{cases} \tag{5.23}$$

According to the experimental data, the maximum/minimum values of the capacitor voltages are shown as

$$\begin{cases} v_{\mathrm{Cumax}} = 48.4\,\mathrm{V} \\ v_{\mathrm{Cvmax}} = 49.0\,\mathrm{V} \\ v_{\mathrm{Cwmin}} = 38.4\,\mathrm{V}. \end{cases} \tag{5.24}$$

The accuracy is higher than 97 % and this proves the reliability of the theoretical analysis developed in Section 5.1. The DC-capacitor voltages will be regulated back to 45 V if the

duration of the SLG fault was longer.

According to the theoretical analysis, the overmodulation will happen when m is smaller than 0.54. That's why some very small current pikes can be observed in the negative half cycles of $i_{\mathrm{v}2}$ in Fig. 5.5. However, it is too small so it can be neglected.

Fig. 5.6 shows the waveforms where the amplitude of $v_{\mathrm{u}1}$ dropped by 80 %. The DC-capacitor voltage variations are larger because of larger power unbalance, which agrees well with the theory in Section 5.1. In addition, obvious overmodulation happened in this case. There were current spikes in u-phase and v-phase currents, whereas w-phase current was still stable because the overmodulation did not happen to w-phase. Fig. 5.8, which is the zoomed in waveforms of the current spikes, shows that the shapes of the spikes are very similar to those of the theoretical waveforms shown in Figs. 5.3 and 5.4 in Section 5.2 except that the theoretical analysis in Section 5.2 does not consider the effect of unbalanced magnetic field and the current oscillation after the spikes disappear.

Fig. 5.9 shows the experimental waveforms of the proposed inverter circuit during the SLG fault (u-phase) where $E = 135\,\mathrm{V}$ and $v_{\mathrm{u}1}$ with a voltage sag of 50 %. The waveforms are basically the same as those shown in Fig. 5.5 except that the DC component included in the neutral current i_{n} is negative due to the increased E. The theoretical value and the average experimental value of i_{n} during the SLG fault are $-4.69\,\mathrm{A}$ and $-4.02\,\mathrm{A}$, respectively. The overmodulation is more obvious in Fig. 5.9 than in Fig. 5.5.

Fig. 5.10 shows the experimental waveforms of the proposed inverter circuit during the SLG fault (u-phase) where $E = 135\,\mathrm{V}$ and $v_{\mathrm{u}1}$ with a voltage sag of 30 %. The overmodulation happened and the peak values are even larger than those of Fig. 5.9.

The experimental data of $|i_{\mathrm{u}2\mathrm{F}}|_{\mathrm{Max}}$ and $|i_{\mathrm{v}2\mathrm{F}}|_{\mathrm{Max}}$ obtained from the zoomed in waveforms Fig. 5.11 are:

$$\begin{cases} |i_{\mathrm{u}2\mathrm{F}}|_{\mathrm{Max}} = 14.70\,\mathrm{A} \\ |i_{\mathrm{v}2\mathrm{F}}|_{\mathrm{Max}} = 22.60\,\mathrm{A}. \end{cases} \tag{5.25}$$

The peak values calculated from the theoretical calculation are:

$$\begin{cases} |i_{\mathrm{u}2\mathrm{F}}|_{\mathrm{MaxT}} = 16.62\,\mathrm{A} \\ |i_{\mathrm{v}2\mathrm{F}}|_{\mathrm{MaxT}} = 22.27\,\mathrm{A}. \end{cases} \tag{5.26}$$

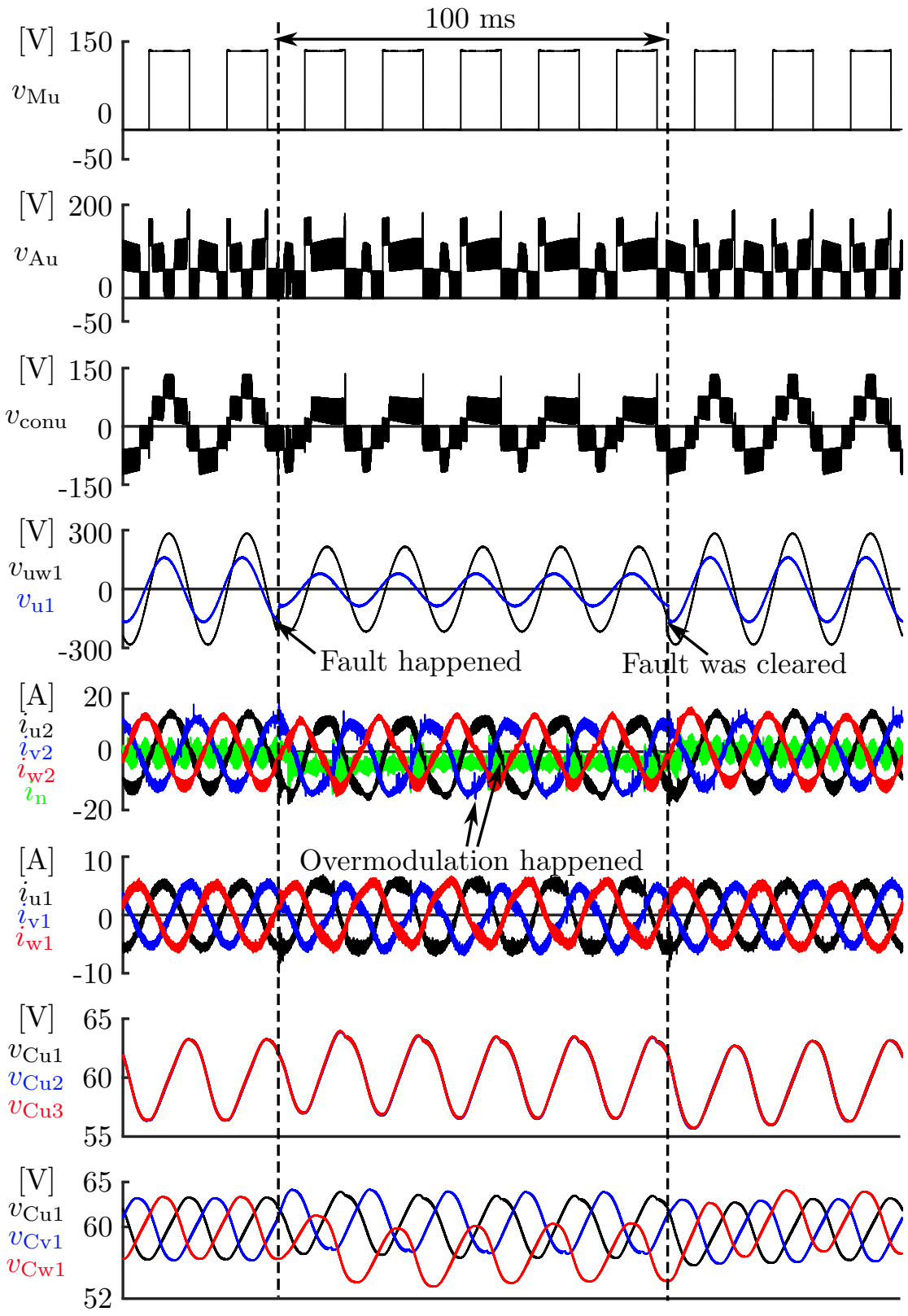


Figure 5.9: Experimental waveforms during SLG faults where $E = 135\,\mathrm{V}$ and v_{u1} dropped by 50 %.

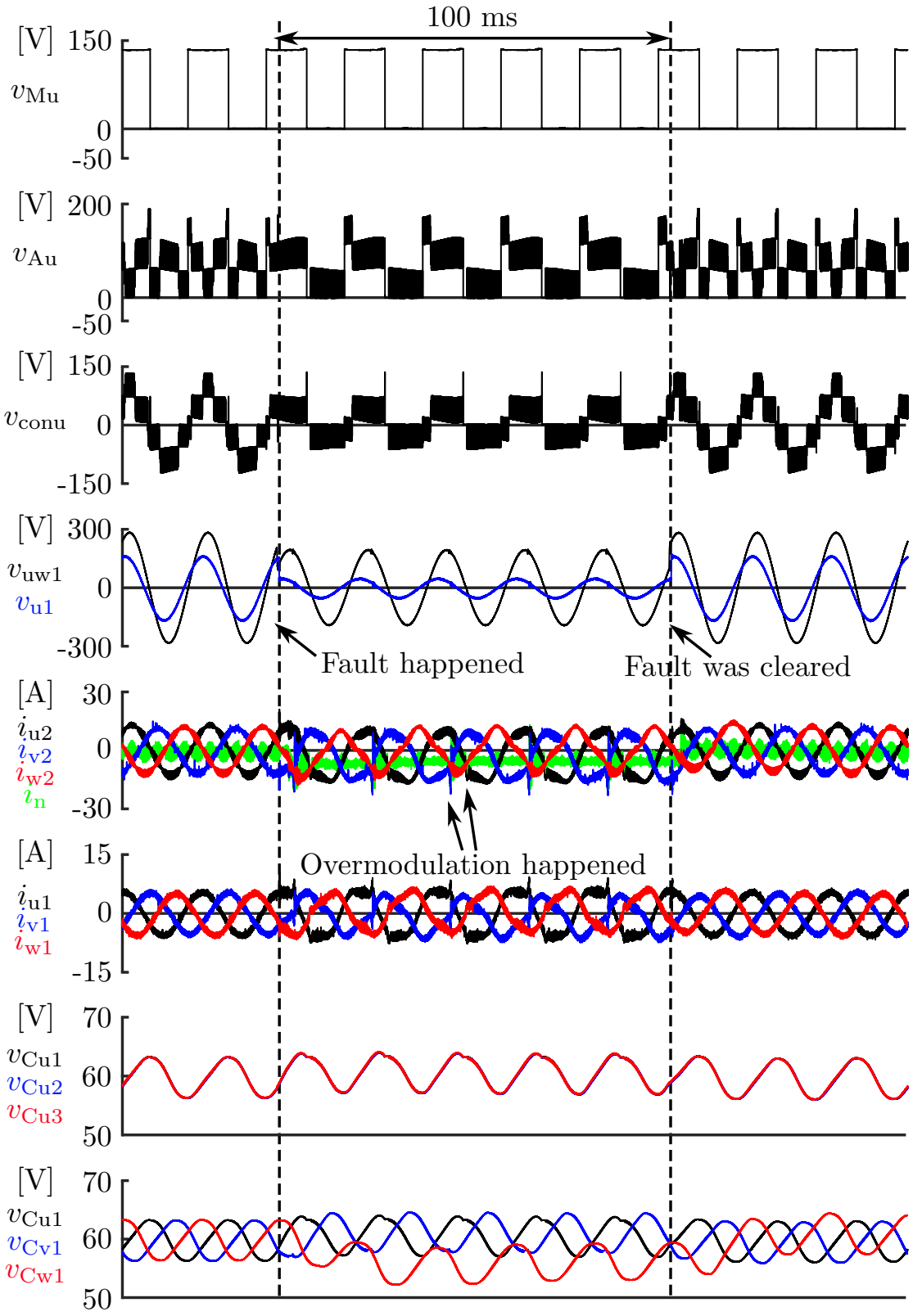


Figure 5.10: Experimental waveforms during SLG faults where $E = 135\,\mathrm{V}$ and v_{u1} dropped by 70 %.

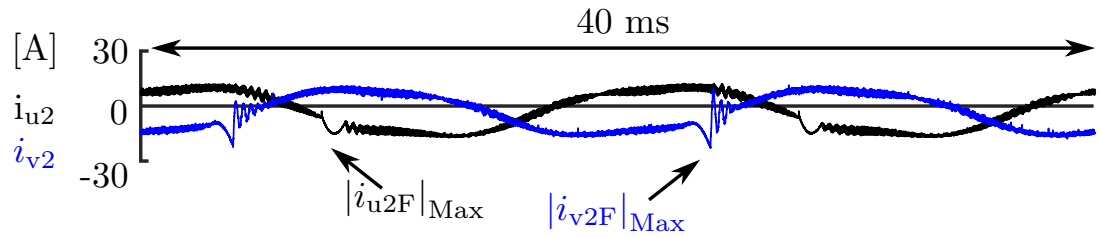


Figure 5.11: Zoomed in waveforms of current spikes in u-phase and v-phase of Fig. 5.10.

The accuracy of the theoretical analysis is very high. Further, if v_{u1} drops by 80 % in this case, the peak value of v-phase current spike will trigger the overcurrent protection, which means an operational failure, and this will also be revealed in Fig. 5.14 later.

5.3.3 LVRT Capability Performance During 3P Fault

Fig. 5.12 shows the experimental waveforms of the proposed inverter circuit during the 3P fault where $E = 85\,\mathrm{V}$. The line-to-neutral voltage of the primary side of the transformer (grid) dropped by 70 % during the 3P fault. The operating principles during the 3P fault are similar to the ones of the 135-V normal condition, where $\alpha = 0$ and $\frac{V_{ac}}{E} < \frac{\sqrt{2}}{\pi}$. Therefore, i_n is negative during the 3P fault according to (3.32). The capacitor voltage fluctuation of each phase when the fault occurred and the fault was cleared is similar because of the symmetrical fault. Specifically, the capacitor voltages of all phases increased when the fault occurred and they decreased when the fault was cleared. The theoretical analysis of the capacitor voltage fluctuation during the 3P fault could be done with a similar method as the SLG fault and hence it is left out in this article. The currents and the capacitor voltages kept balanced during the 3P fault.

Fig. 5.13 shows the experimental waveforms of the proposed inverter circuit during the 3P fault where $E = 135\,\mathrm{V}$ and the line-to-neutral voltage of the grid dropped by 70 %. The voltage and current waveforms are similar to those shown in Fig. 5.12 even though the DC input voltage was increased. The performance of the proposed inverter during the 3P fault is more stable than that during the SLG fault.

5.3.4 Evaluation of LVRT Capability of Proposed Inverter

Judging from the experimental results, it is more important to evaluate the LVRT capability of the proposed inverter under the SLG fault. Therefore, the peak values of the current

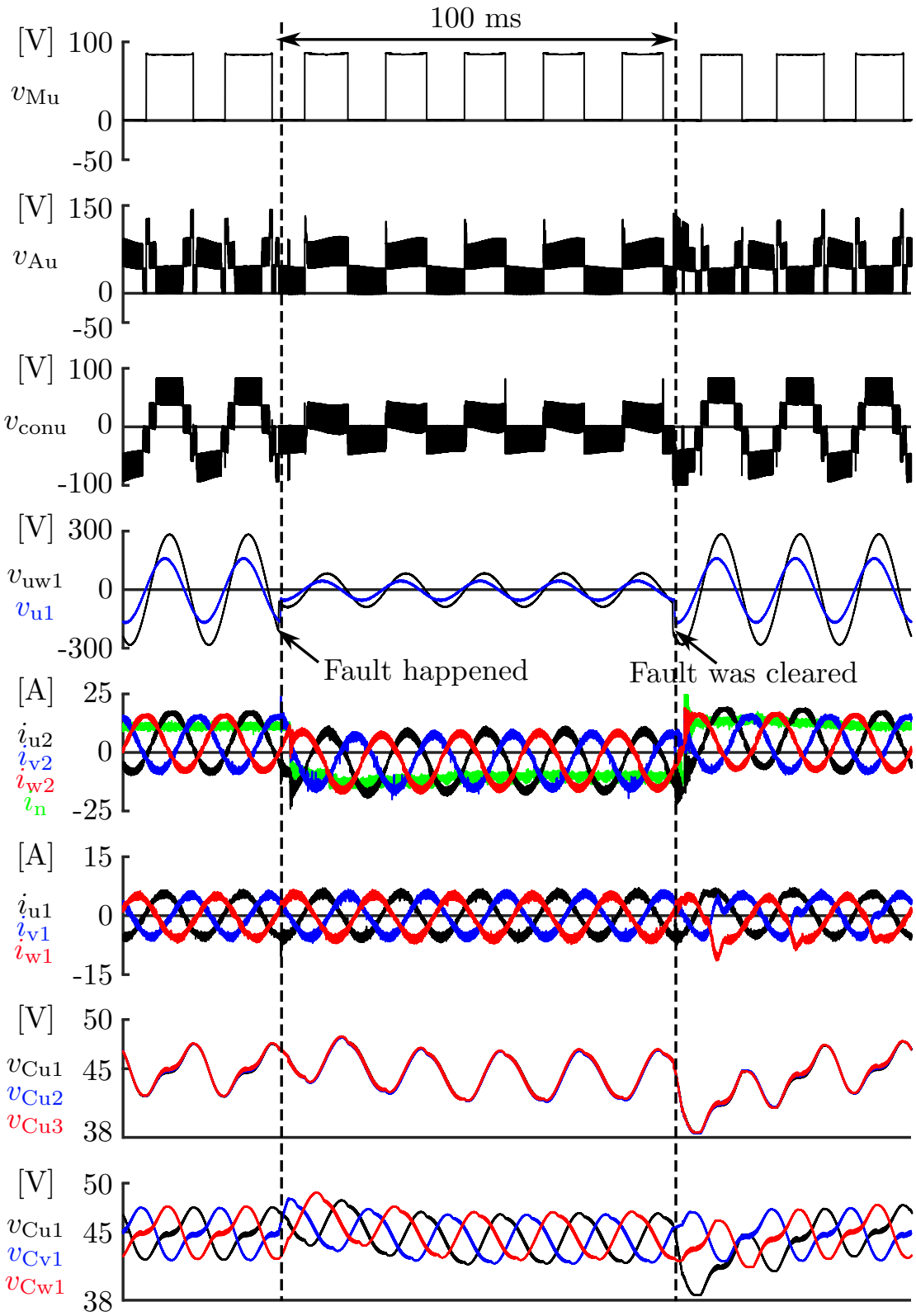


Figure 5.12: Experimental waveforms during 3P fault where $E = 85\,\mathrm{V}$ and primary side line-to-neutral voltage dropped by 70 %.

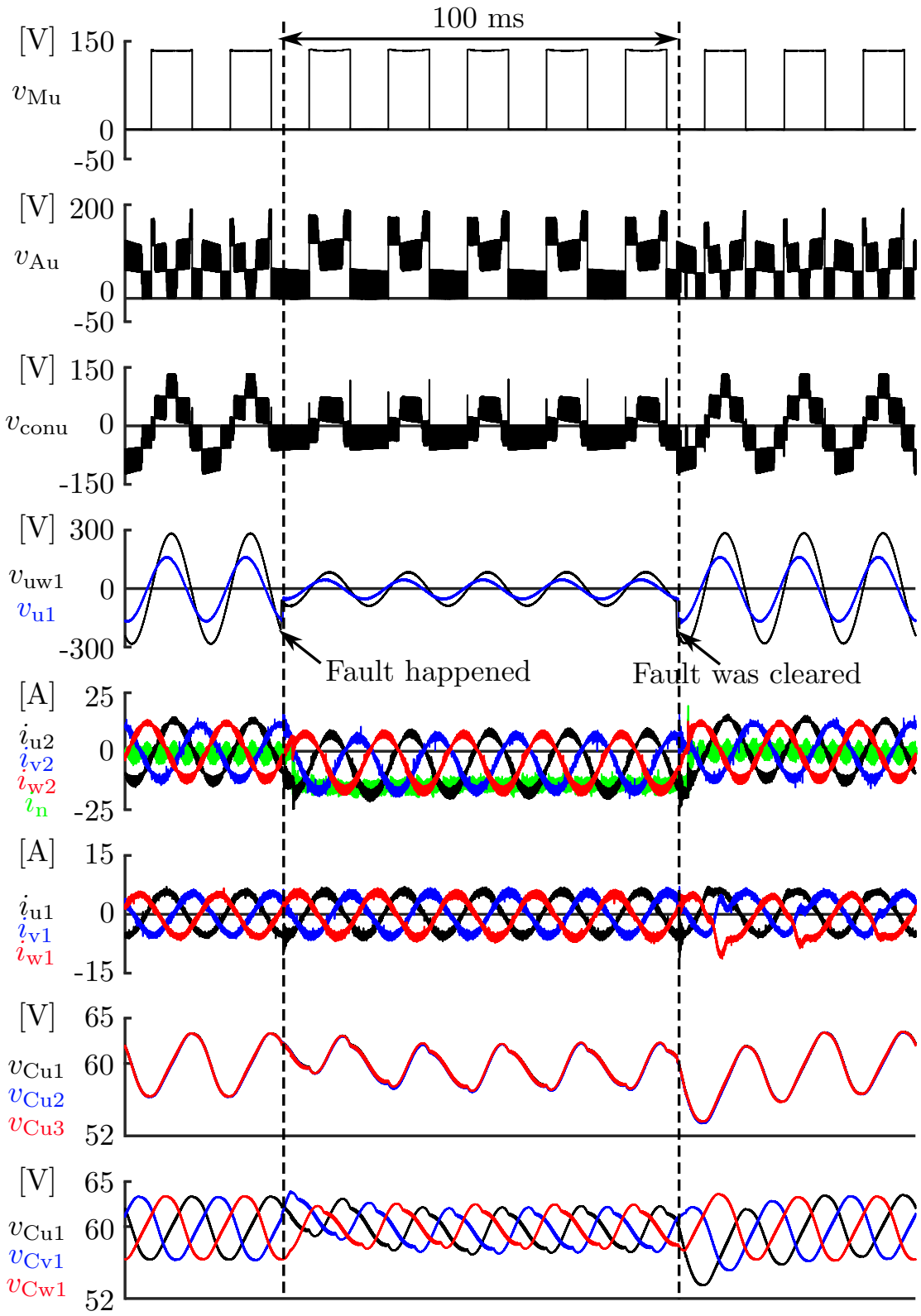


Figure 5.13: Experimental waveforms during 3P fault where $E = 135\,\mathrm{V}$ and primary side line-to-neutral voltage dropped by 70 %.

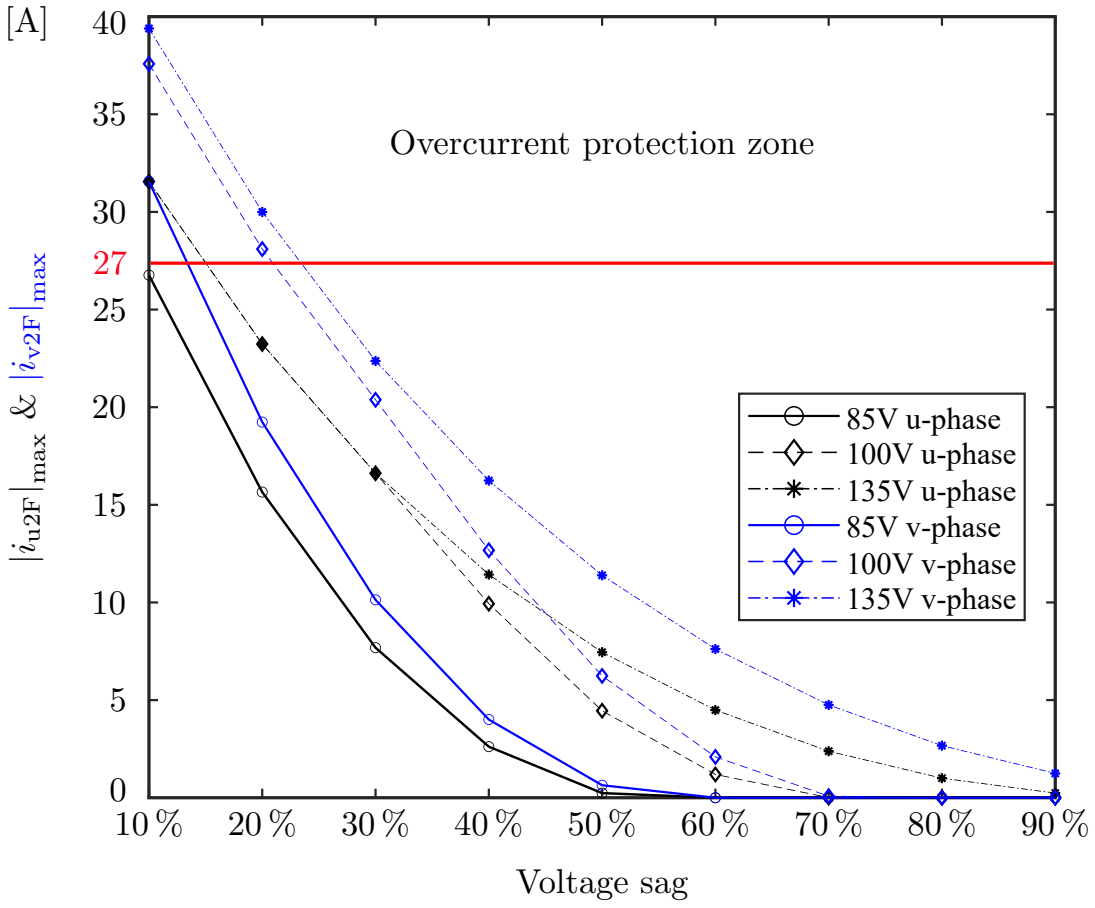


Figure 5.14: LVRT capability of the 1.5-kW downscaled system under the SLG fault.

spikes in different operation cases are calculated using the parameters of the downscaled experiment system, which are shown in Fig. 5.14.

For the downscaled system, the overcurrent limit was set to 175 % of the nominal current in $E = 85\,\mathrm{V}$ case, which is 27 A. Fig. 5.14 also shows that a voltage sag of 20 % in $E = 135\,\mathrm{V}$ case will cause v-phase overcurrent, which is mentioned above. It is obvious that $|i_{v2F}|_{MaxT}$ is always larger than $|i_{u2F}|_{MaxT}$ in the same overmodulation case. It can be concluded that the LVRT capability of the proposed inverter circuit under the SLG fault will get worse with the increase of the DC-input voltage. However, it is still able to deal with most voltage sag operation cases.

5.4 Conclusion

This Chapter has provided a detailed LVRT capability analysis of the three-phase PV inverter. The theoretical analysis of the proposed inverter during the grid faults based on mathematical calculation and figures, including the capacitor voltage fluctuation, the

reason for overmodulation and its borderline, and the peak value of current spikes during the overmodulation, has been developed. Experimental verification using the same downscaled system verified the reliability of the theoretical analysis.

Chapter 6

Evaluation of Chopper-cell Number and Performance Comparison of Proposed PV Inverter

Besides the topics addressed in the previous Chapters, there is one more very important topic need to be discussed, which is whether we could decrease the total cost of the proposed PV inverter without sacrificing its performance.

Generally speaking, the selection of the cascaded cell (submodule) number of the MMCCs is crucial. When the MMCCs are applied to high-voltage applications such as HVDC systems, the required cell number is mainly determined by the required voltage levels, and the number of cells can reach several hundreds, which eventually increases the cost and volume of the converter [32], [75]. A significant amount of research has been carried out to reduce the cost and volume of the MMCCs using new circuit topologies [76], the latest power devices [77], and the capacitor voltage oscillation reduction method [78]. On the other hand, the results in the previous Chapters show that there is no need increasing the cell number to increase the voltage level or to improve the inverter performance by reducing the voltage/current harmonics for a smaller size of passive filter components. In addition, the increased cell number may result in increased converter loss and cost. It is obvious that the minimum cell number per phase for enjoying the benefit of the

MMCC technologies is two. Hence, a detailed evaluation of the chopper-cell number is carried out by conducting performance comparison between the inverter using two cells per phase (two-cell inverter) and the one using three cells per phase (three-cell inverter) in this Chapter.

It is noteworthy that change of chopper-cell number does not change the range of MPPT. For a fair comparison, the same equivalent switching frequency is assumed in both inverters, which means that the carrier frequency of each cell in the auxiliary converter of the two-cell inverter is 1.5 times that of the three-cell one. Since the circuit configuration, the operation principles, and the control method do not change, the detail of them are left out in this Chapter. In addition, the DC-capacitor voltage of the two-cell inverter should be higher than that of the three-cell one considering (3.11).

6.1 Loss and Efficiency Comparison

The loss and efficiency analyses of the proposed three-cell inverter were carried out in Section 4.3 for comparisons with those of the conventional three-level inverter (i.e., T-type NPC inverter). The carrier frequency of the main converter in the three-cell inverter was set to 50 Hz, and that of each chopper cell was set to 2 kHz so that the equivalent carrier frequency became 6 kHz to match the normal carrier frequency of the conventional three-level inverter for fair comparisons.

Following the works shown in Section 4.3, the loss breakdown of the two-cell inverter will be calculated, and the efficiency comparisons between the two-cell inverter and the three-cell inverter will be conducted in this section. In order to conduct fair comparisons, the loss in the transformer is not considered, which is similar to the previous work. The switching and conduction loss of the auxiliary converter is taken into consideration. In contrast, only the conduction loss is considered for the main converter because ZCS is achieved in most cases, and the switching loss of the main converter with a carrier frequency of 50 Hz is negligible. It is noteworthy that the calculation in this section is based on active power control cases and the power factor is set to unity. To keep the consistency with the previous work, it is still assumed that the 3.3-kV IGBT modules 1MBI1000UG-330 from Fuji Electric are used in the main converters and the 1.2-kV IGBT modules CM1000DX-24T from Mitsubishi Electric are used in the auxiliary converters because

Table 6.1: Circuit parameters used for loss calculation.

DC input voltage	E	960 V
Secondary line-to-line voltage	$\sqrt{3}V_{\mathrm{ac}}$	1150 V
Two-cell inverter DC-capacitor voltage	V_{C}	650 V
Three-cell inverter DC-capacitor voltage	V_{C}	420 V
Two-cell inverter carrier freq. (aux.conv.)	f_{SA}	3 kHz
Three-cell inverter carrier freq. (aux.conv.)	f_{SA}	2 kHz
Carrier freq. (main conv.)	f_{SM}	50 Hz

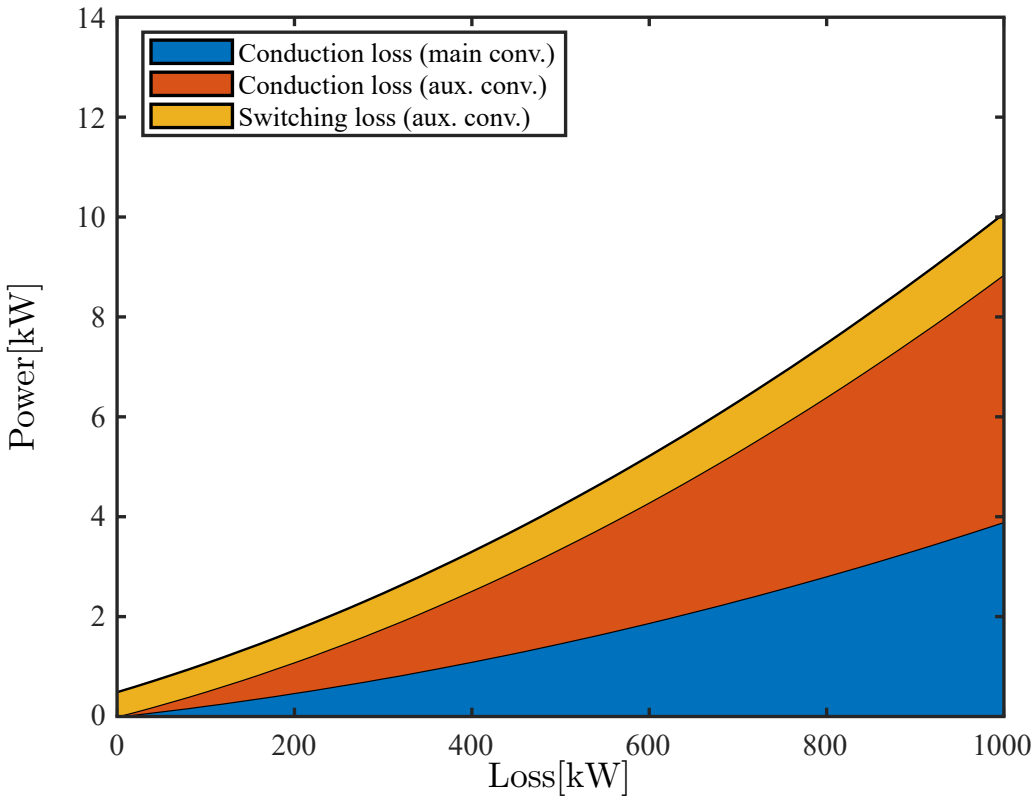
Table 6.2: Parameters of proposed inverter used for comparison with same MPPT range.

DC input voltage	960 V	1100 V	1300 V
Two-cell inverter DC-capacitor voltage	650 V	680 V	730 V
Three-cell inverter DC-capacitor voltage	420 V	450 V	480 V
Secondary line-to-line voltage	1150 V		
MPPT range	960−1300 V		
Two-cell inverter carrier freq. (aux.conv.)	3 kHz		
Three-cell inverter carrier freq. (aux.conv.)	2 kHz		
Carrier freq. (main conv.)	50 Hz		

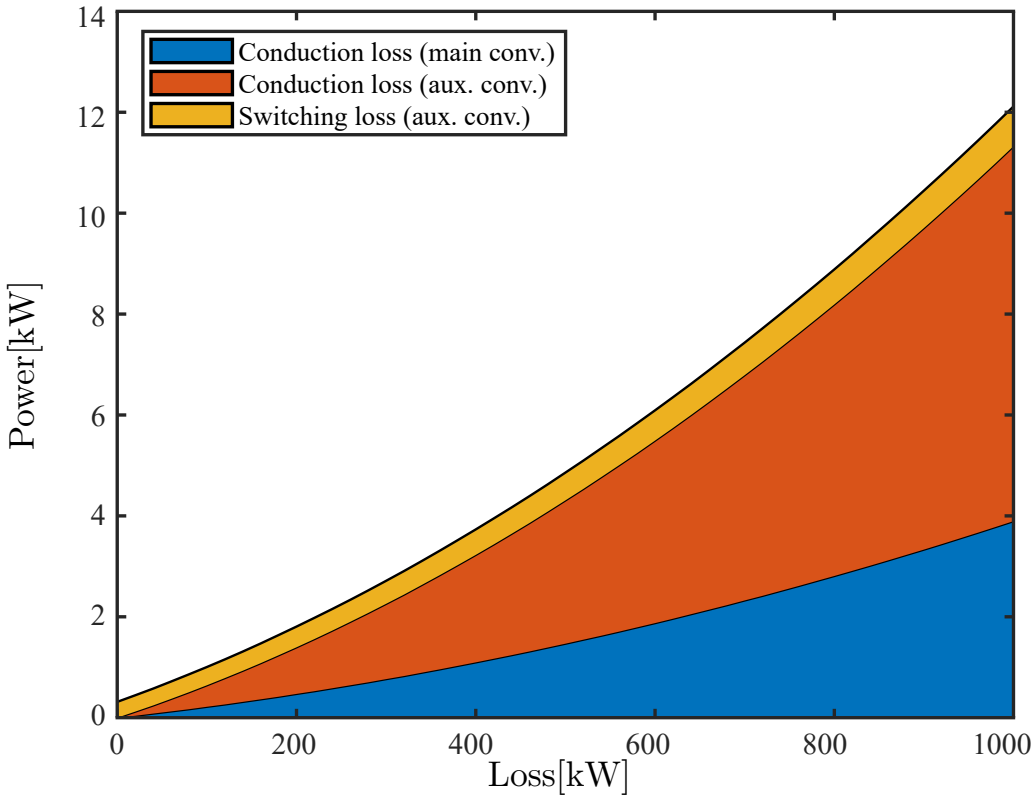
the maximum DC-capacitor voltage is 730 V for the two-cell inverter and 480 V for the three-cell inverter. The parameters used for calculation are obtained from the official data sheets available on the manufacturer's homepage.

Table 6.1 shows the circuit parameters used for loss calculation. The carrier frequency of each cell in the auxiliary converter in the two-cell inverter was set to $f_{\mathrm{SA}} = 3\,\mathrm{kHz}$ to achieve the same equivalent switching frequency of 6 kHz as that of the three-cell inverter calculated in Section 4.3. The DC-capacitor voltages of the two inverters are different because of different cell numbers and they are determined according to (3.11). The same loss calculation method is used, and the results are shown in Fig. 6.1. From the comparison, it is obvious that the main converter conduction loss of the two-cell inverter is the same as that of the three-cell inverter. However, the conduction loss of the auxiliary converter of the two-cell inverter is almost 2/3 of that of the three-cell inverter at the output power of 1000 kW because the number of power devices used in the auxiliary converter of the two-cell inverter is 2/3 that of the three-cell inverter. Even though the switching loss of the auxiliary converter of the two-cell inverter is larger than that of the three-cell inverter because of the increased DC-capacitor voltage, the total loss decreases as the output power increases compared with that of the three-cell inverter.

The following compares the efficiency of the two-cell and three-cell inverters with the same DC-input and AC-output voltages and the same MPPT range. The circuit param-

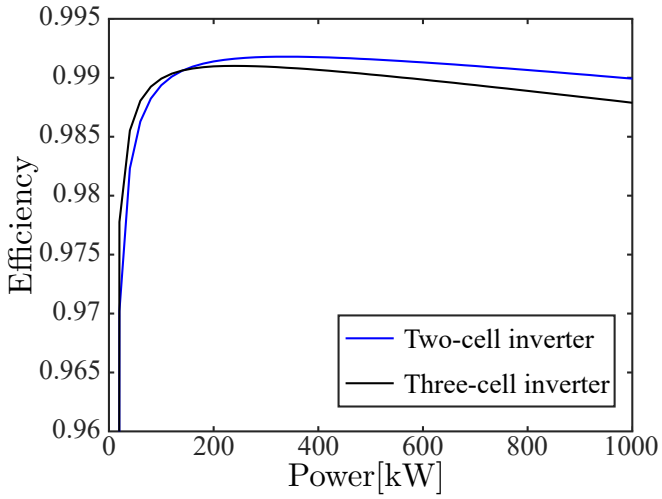


(a)

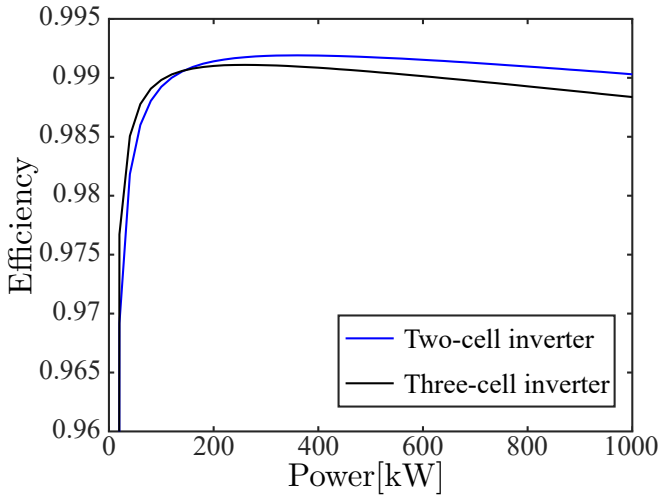


(b)

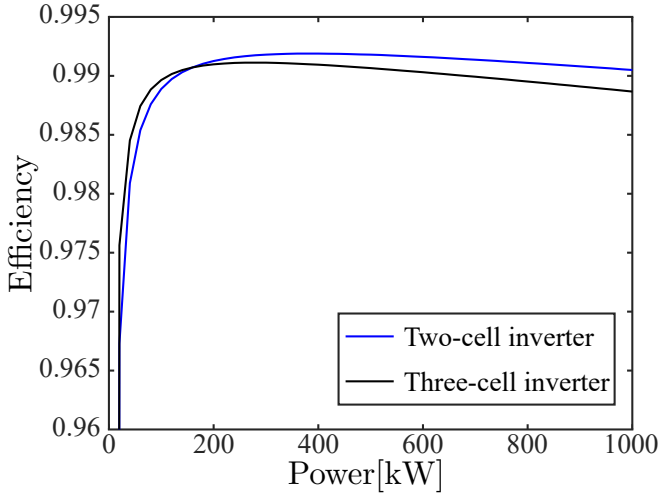
Figure 6.1: Loss breakdown of proposed inverter: a) two-cell inverter circuit, b) three-cell inverter circuit.



(a)



(b)



(c)

Figure 6.2: Efficiency comparisons of proposed inverter when $\sqrt{3}V_{\text{ac}} = 1150\,\text{V}$ with MPPT range of $960 - 1300\,\text{V}$: a) $E = 960\,\text{V}$, b) $E = 1100\,\text{V}$, 3) $E = 1300\,\text{V}$.

Table 6.3: Two-cell inverter circuit parameters used for experiments.

Active power reference	p^*	1.5 kW
DC input voltage	E	85 V or 135 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	2
DC-capacitor voltage	V_{C}	65 V or 75 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	10.8 kHz
Fault duration	t_{F}	100 ms

Table 6.4: Three-cell inverter circuit parameters used for experiments.

Active power reference	p^*	1.5 kW
DC input voltage	E	85 V or 135 V
Nominal grid voltage	V_{grid}	200 V
Voltage ratio of Tr.	a	$200/100 = 2$
Secondary voltage of Tr.	V_{ac}	58 V
Inductor	L	0.21 mH
Leakage inductance of Tr.	l	0.27 mH
Chopper-cell count/phase	N	3
DC-capacitor voltage	V_{C}	45 V or 60 V
Cell capacitor	C	4.4 mF
Carrier freq. (main conv.)	f_{SM}	50 Hz
Carrier freq. (aux. conv.)	f_{SA}	7.2 kHz
Fault duration	t_{F}	100 ms

eters used for efficiency calculation are shown in Table 6.2 and the result of comparisons is shown in Fig. 6.2. According to Fig. 6.2, the two-cell inverter circuit has a higher efficiency in all of the three cases when the output power is higher than 200 kW, and the maximum efficiency is 99.2 %. In contrast, the efficiency of the three-cell inverter is higher when the output power is lower than 200 kW because the switching loss of the auxiliary converter is dominant in this region. Because the proposed inverter circuit is designed for applications in megawatt power level PV systems, the two-cell inverter circuit is better than the three-cell inverter circuit in terms of loss and efficiency.

6.2 Experiment

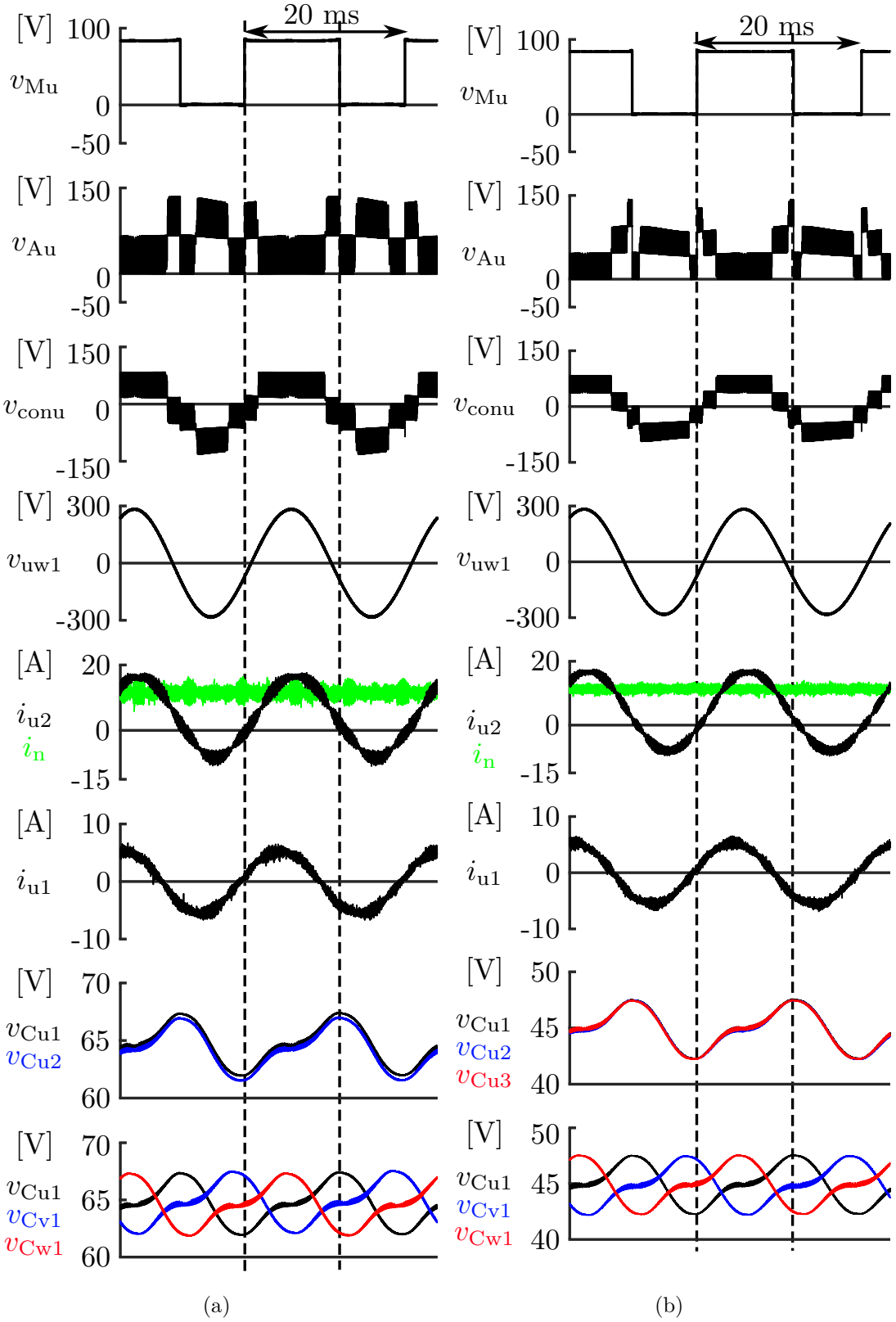
6.2.1 Experimental conditions

The experimental verifications during the steady state, the SLG fault, and the 3P fault were carried out using the same 1.5-kW downscaled system used in previous Chapters. The circuit parameters of the two-cell inverter and the three-cell inverter are summarized in Tables 6.3 and 6.4, respectively. The DC input voltage corresponding to the PV array voltage, E, was produced using the DC power source NF DP030RS. The grid voltage, which is the primary side voltage of the transformer was produced using the programmable AC power source NF DP045RT. The SLG fault (u-phase) and the 3P fault were performed on the primary side of the transformer shown in Fig. 5.1 using the sequence function of NF DP045RT. According to IEEE Std 1159-2019 [94], the fault duration, t_{F}, was set to 100 ms. The reference value of the active power was 1.5 kW. The reference value of the DC-capacitor voltage in the two-cell inverter was set to 65 V when the DC input voltage was 85 V and was set to 75 V when the DC input voltage was 135 V considering (3.11) except for Fig. 6.9a, the reason of which will be explained later. Similarly, the reference value of the DC-capacitor voltage in the three-cell inverter was set to 45 V when the DC input voltage was 85 V and it was set to 60 V when the DC input voltage was 135 V, respectively. The deadtime was set to 4.0 µs for the main and the auxiliary converters. The voltage ratio of the transformer was set to $a = 2$ so that the secondary line-to-neutral (phase) RMS voltage was $V_{\mathrm{ac}} = V_{\mathrm{grid}}/(\sqrt{3}a) = 58\,\mathrm{V}$.

The control system is composed of a digital signal processor unit utilizing Texas Instruments TMS320C6678 and a field programmable gate array unit utilizing Altera Cyclone IV. The voltage and current waveforms were measured using Textronix DPO4104B-L with a frequency band of 1 GHz, Textronix MDO4104C with a frequency band of 1 GHz, and Hioki Memory Hicoder 8861-50. The following mainly focuses on the behavior comparisons of the two-cell inverter and the three-cell inverter under the steady state and the fault condition.

6.2.2 Steady-state performance comparisons

Fig. 6.3 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter under a steady-state when $p^* = 1.5\,\mathrm{kW}$ and $E = 85\,\mathrm{V}$. It corresponds



(a) (b)

Figure 6.3: Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 85\,\mathrm{V}$: a) two-cell inverter circuit, b) three-cell inverter circuit.

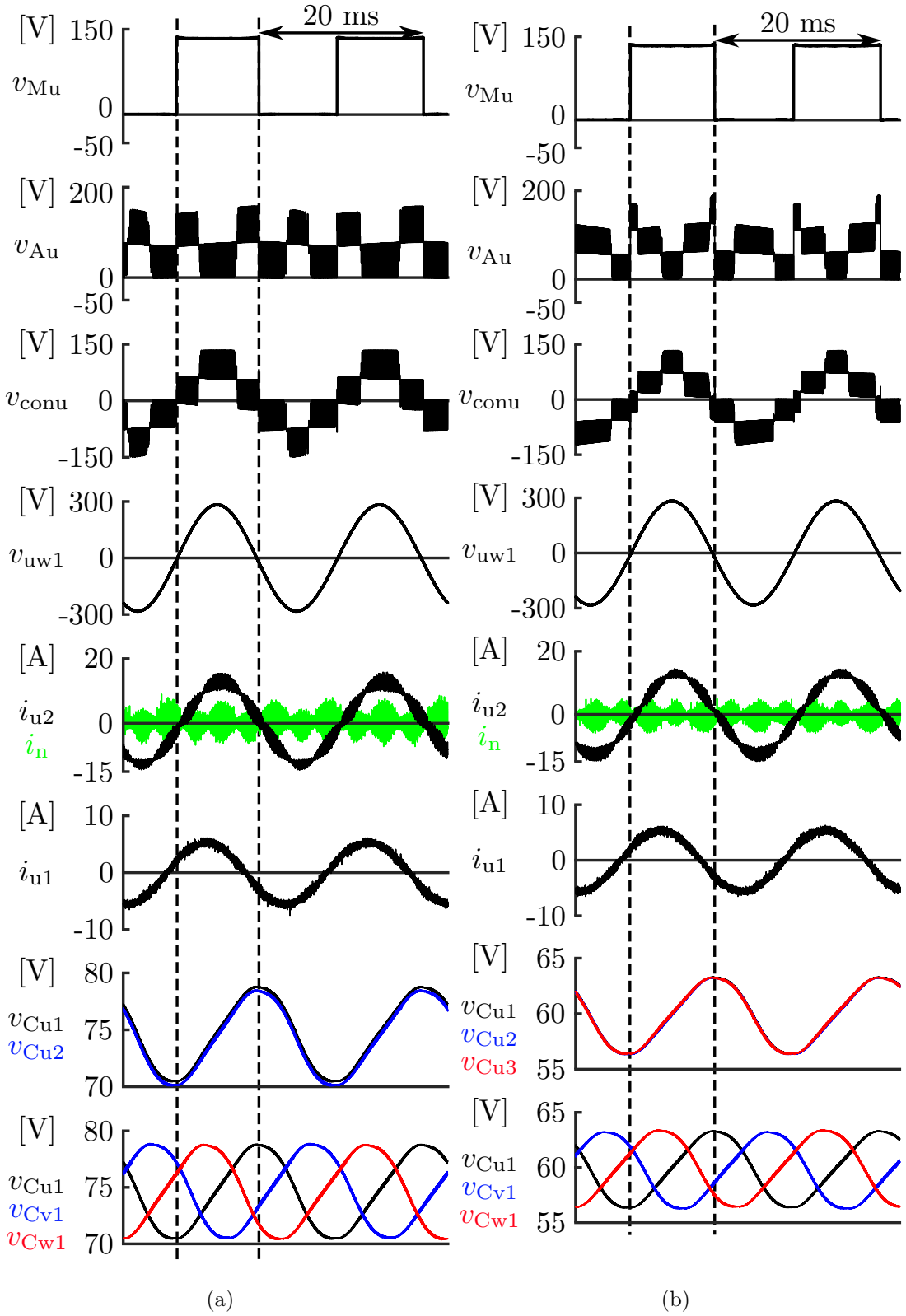
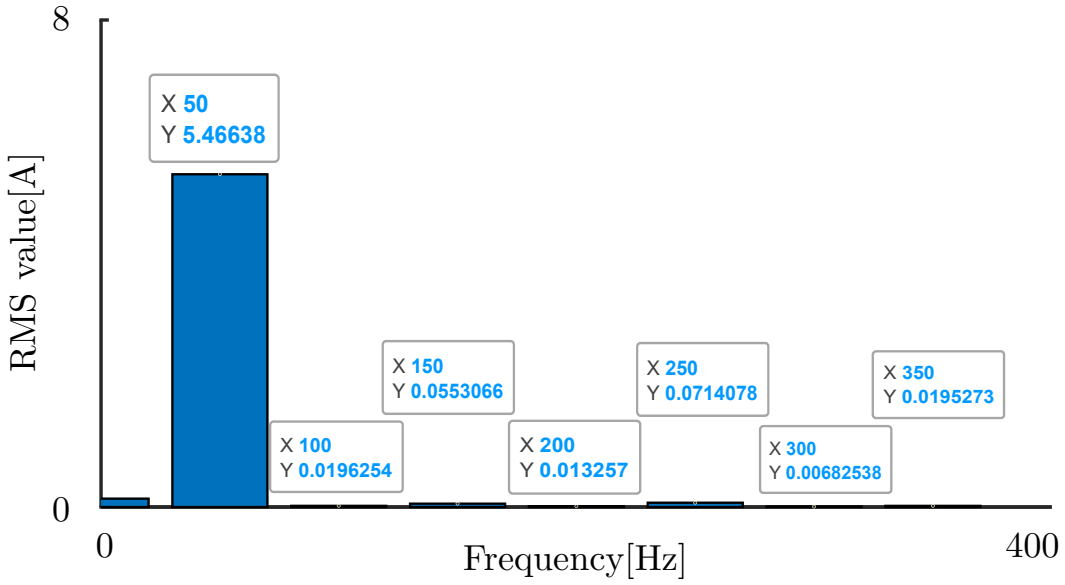


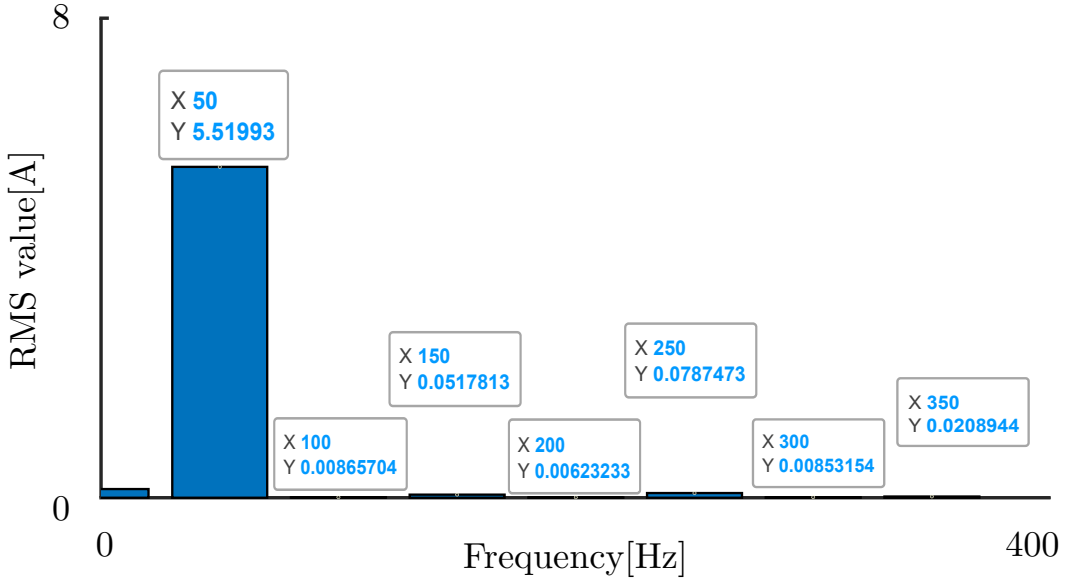
Figure 6.4: Experimental waveforms under steady state where $p^* = 1.5\,\mathrm{kW}$ and $E = 135\,\mathrm{V}$: a) two-cell inverter circuit, b) three-cell inverter circuit.

to the low DC input voltage region where the ZCS can be achieved. Basically, the two-cell inverter and the three-cell inverter have similar experimental waveforms except for several differences. The auxiliary converter output voltage, v_{Au}, of the two-cell inverter has a three-level output waveform, whereas that of the three-cell inverter has a four-level output waveform. There are a few more harmonic components in i_{u1}, i_{u2}, and i_{n} of the two-cell inverter than those of the three-cell inverter. The reason for this phenomenon is that the active filter function of the auxiliary converter is weakened by reducing the cell number. In addition, the increased DC-capacitor voltage also increases the harmonic components in the two-cell inverter circuit. The DC-capacitor voltages are regulated to the reference value of 65 V and 45 V without any steady-state error in both inverter circuits, respectively. However, only two cells capacitor voltages need to be balanced per phase in the two-cell inverter, whereas there are three of them that need to be balanced per phase in the three-cell inverter. Fig. 6.4 shows the waveforms comparison of another experiment under a steady-state when $p^* = 1.5\,\mathrm{kW}$ and $E = 135\,\mathrm{V}$. It corresponds to the high DC input voltage region where ZCS cannot be achieved in this region. The waveforms comparison shows similar results as that of Fig. 6.3. In this case, the DC component included in the neutral current i_{n} is negative due to the increased E.

Further, the comparison of the THD values of the two-cell inverter and the three-cell inverter is carried out. The data of the u-phase grid current, i_{u1}, are used for calculation. The THD values are calculated using MATLAB, and up to the 40^{th}-order harmonic. The THD values of the 85 V steady-state cases of the two-cell inverter and the three-cell inverter are 2.735 % and 2.608 %, respectively. Meanwhile, the THD values of the 135 V steady-state cases of the two-cell inverter and the three-cell inverter are 1.956 % and 1.928 %, respectively. All of the THD values obtained above satisfy the requirement of IEEE std 519-2014 [86]. In addition, the comparison of the spectrum of i_{u1} of the two-cell inverter and the three-cell inverter in the 135 V steady-state case is shown in Fig. 6.5, where X stands for the frequency and Y stands for the RMS value. In Fig. 6.5, both spectrums are shown up to the 7^{th}-order harmonic because the RMS values of higher order harmonics are too small. It should be noted that the DC components shown in the spectrums were caused by the measurement equipment error. The THD performance of the two-cell inverter in Fig. 6.5a shows that the two-cell inverter exhibits similar performance to that of the three-cell inverter, which is shown in Fig. 6.5b. In addition, the high frequency harmonic

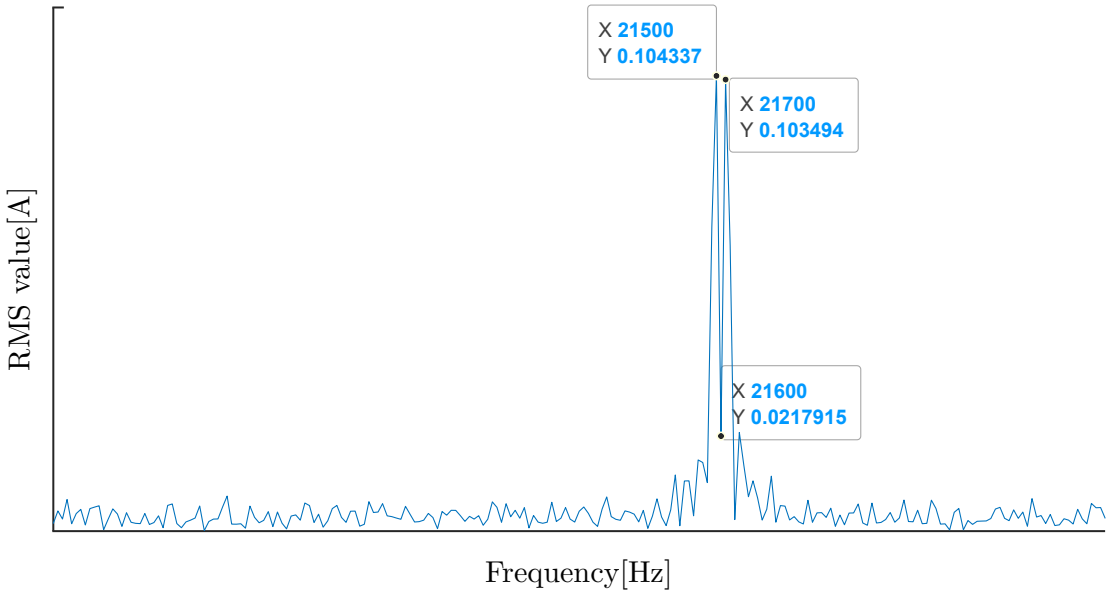


(a)

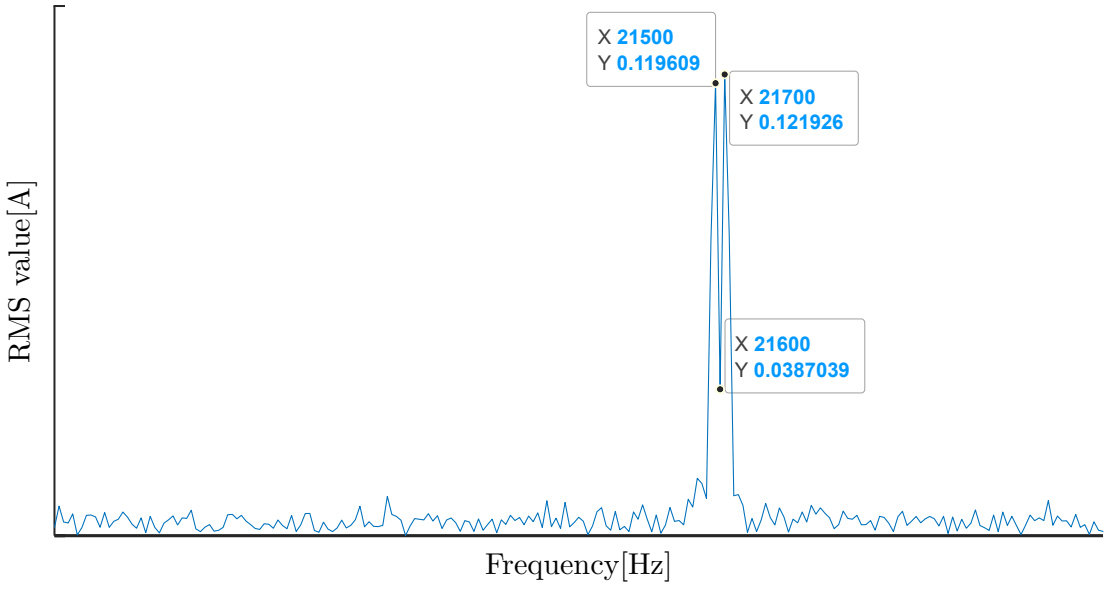


(b)

Figure 6.5: Spectrum of i_{u1}: a) two-cell inverter circuit, b) three-cell inverter circuit.



(a)



(b)

Figure 6.6: 21.6 kHz components of i_{u1}: a) two-cell inverter circuit, b) three-cell inverter circuit.

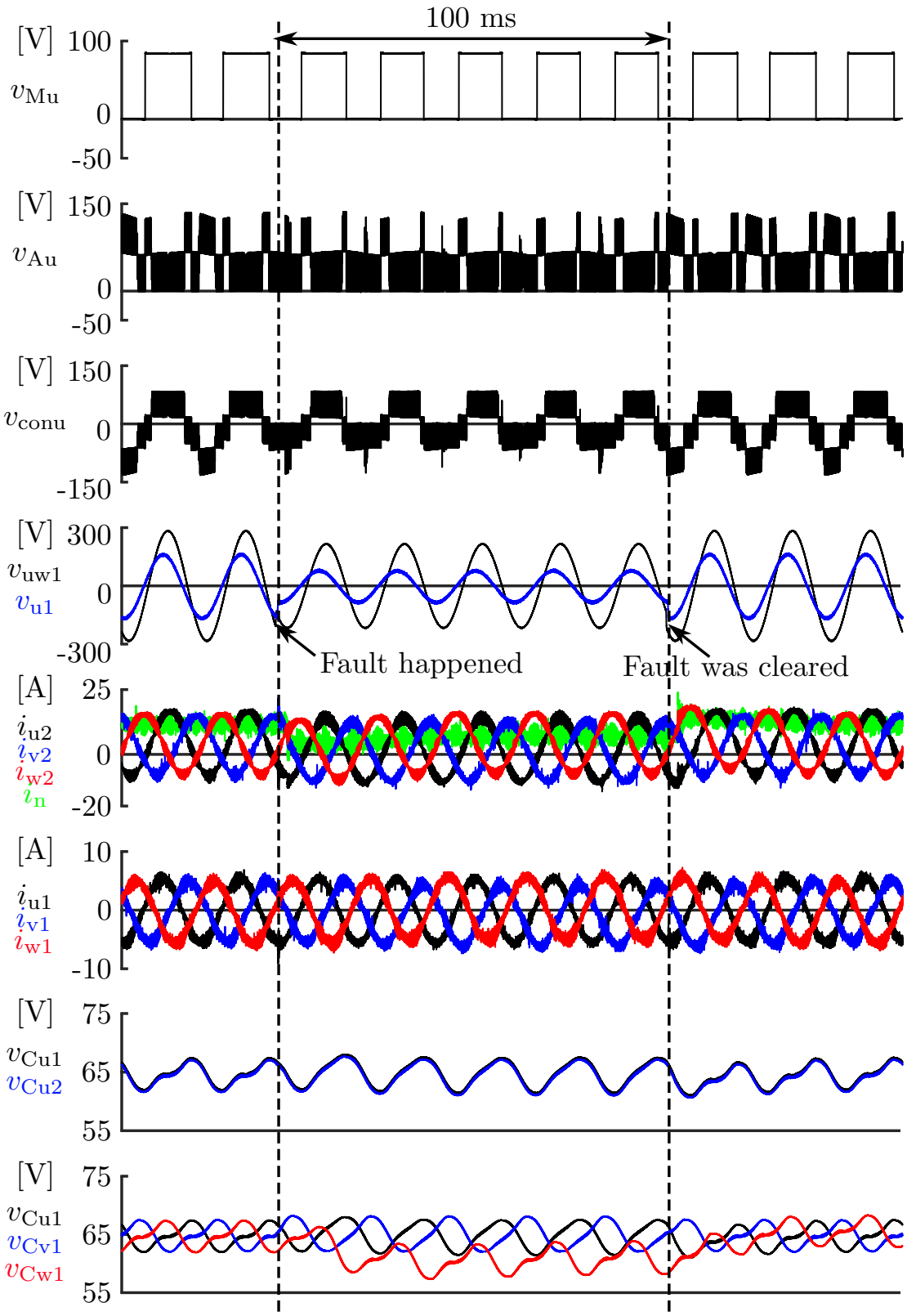
components corresponding to the equivalent switching frequency contained in i_{u1} of the two-cell inverter and the three-cell inverter are also compared in Fig. 6.6. The results show that high frequency harmonic component does not change much by decreasing the chopper-cell number from three to two.

6.2.3 LVRT capability performance comparisons during SLG fault

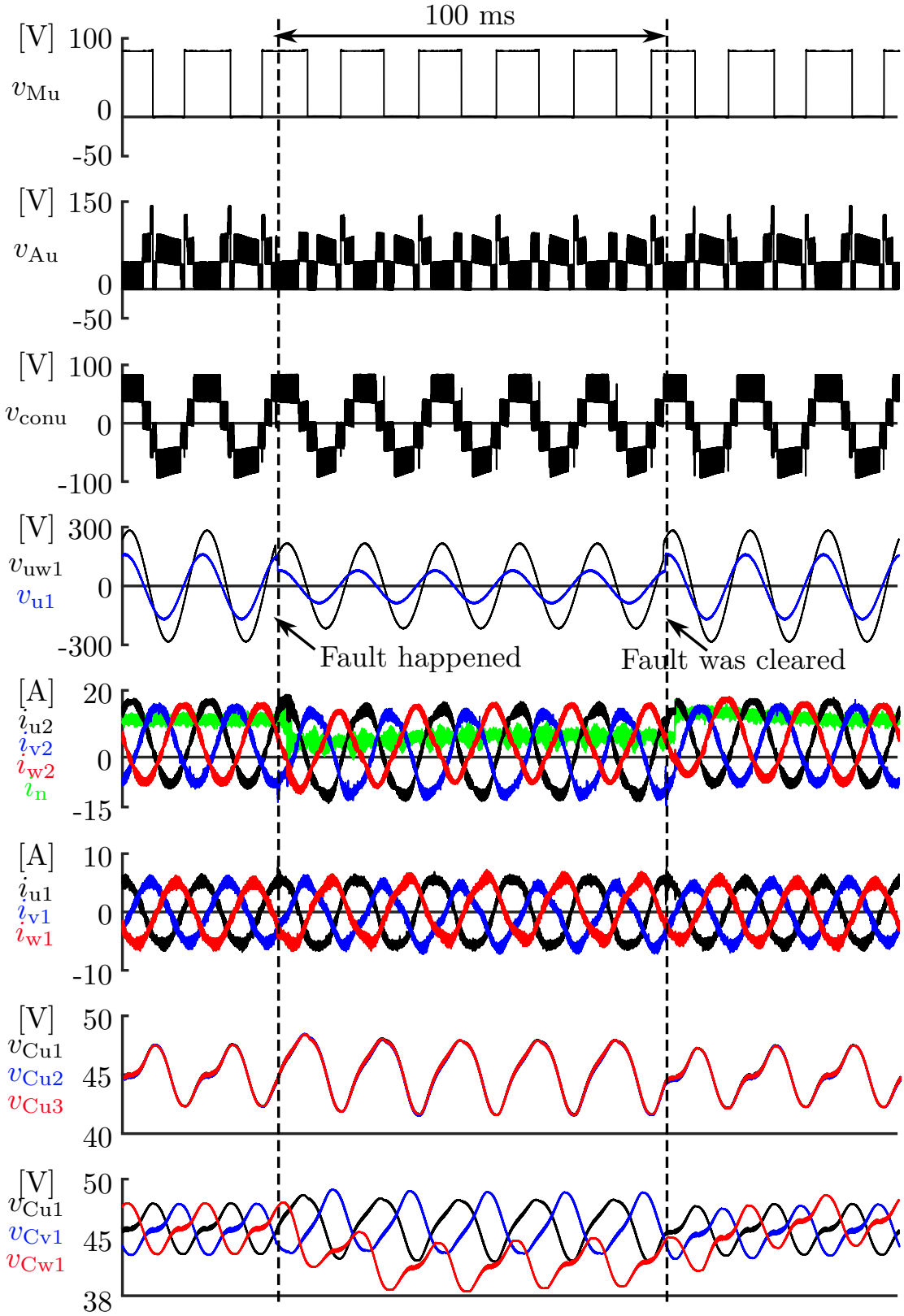
Fig. 6.7 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter during an SLG fault (u-phase) where $E = 85\,\mathrm{V}$. During the SLG fault, the amplitude of v_{u1} dropped by 50 %, and a voltage dip and a phase jump occurred in v_{uw1} because of the Y-Δ connection of the transformer. Both inverters behaved similarly during the SLG fault. The value of the neutral line current i_n of both inverters decreased during the fault because several coefficients in (3.32) changed during the SLG fault. In addition, the currents of the two-cell inverter contained less low-order harmonic currents during the SLG fault than those of the three-cell inverter. The reason is that reduction of the cell number makes the capacitor voltage balancing control easier during the SLG fault, which increases the robustness and the LVRT capability of the proposed inverter. The DC-capacitor voltage unbalances occurred during the SLG fault and the DC-capacitor voltages of u-phase and v-phase increased slightly and that of w-phase decreased in both inverter circuits. However, the voltage variance of the two-cell inverter circuit is larger than that of the three-cell inverter circuit because the power unbalance caused by the SLG fault was imposed on only two cells. After the fault was cleared, the DC-capacitor voltages of both inverters were regulated to the reference values, respectively. Fig. 6.8 shows the waveforms comparison of another experiment during the SLG fault when $p^* = 1.5\,\mathrm{kW}$ and $E = 135\,\mathrm{V}$. Similarly, the amplitude of v_{u1} dropped by 50 %, and a voltage dip and a phase jump occurred in v_{uw1}. Both inverters have similar performances as shown in Fig. 6.7.

6.2.4 LVRT capability performance comparisons during 3P fault

Fig. 6.9 shows the experimental waveforms comparison of the two-cell inverter and the three-cell inverter during a 3P fault where $E = 85\,\mathrm{V}$. The line-to-neutral voltage of the primary side of the transformer (grid) dropped by 60 % during the 3P fault. The operation principles during the 3P fault are similar to the ones of the 135-V normal condition, where

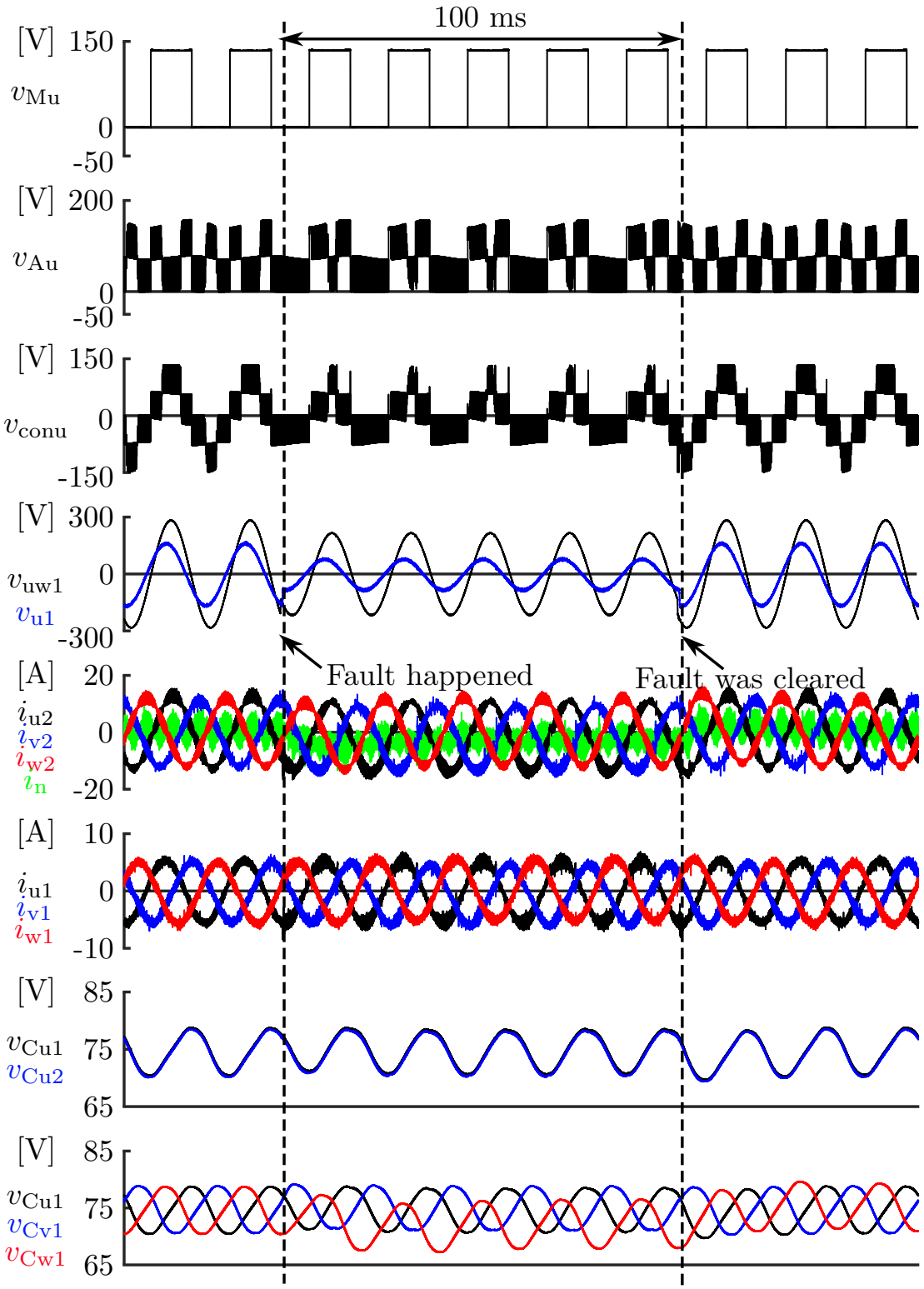

100 ms
[V] 100
v_{Mu}
0
-50
[V] 150
v_{Au}
0
-50
[V] 150
v_{conu}
0
-150
[V] 300
v_{uw1}
v_{u1}
0
-300
Fault happened
Fault was cleared
[A] 25
i_{u2}
i_{v2}
i_{w2}
i_n
0
-20
[A] 10
i_{u1}
i_{v1}
i_{w1}
0
-10
[V] 75
v_{Cu1}
v_{Cu2}
65
55
[V] 75
v_{Cu1}
v_{Cv1}
v_{Cw1}
65
55

(a)

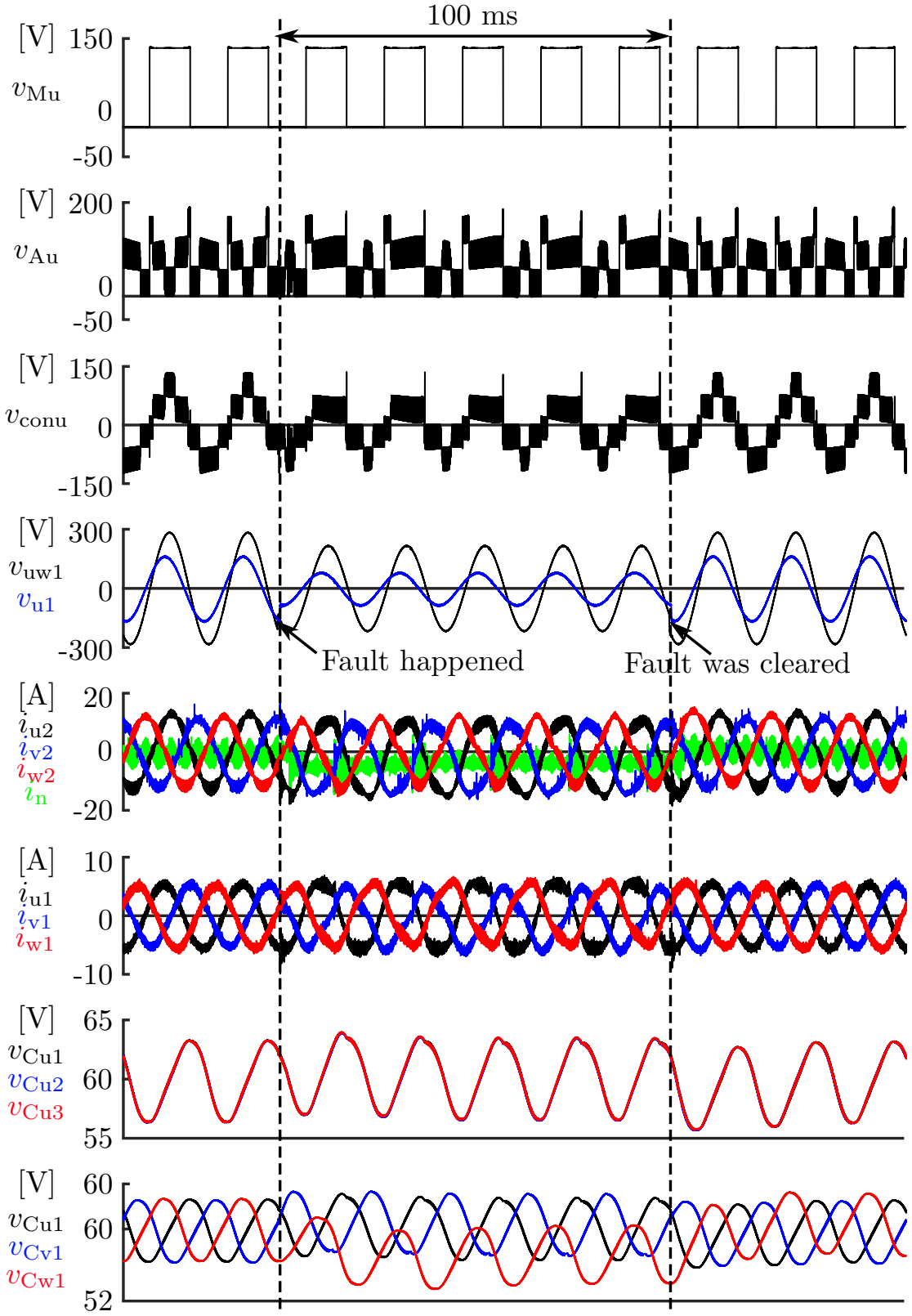


(b)

Figure 6.7: Experimental waveforms during SLG fault where $E = 85\,\mathrm{V}$ and v_{u1} dropped by 50 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

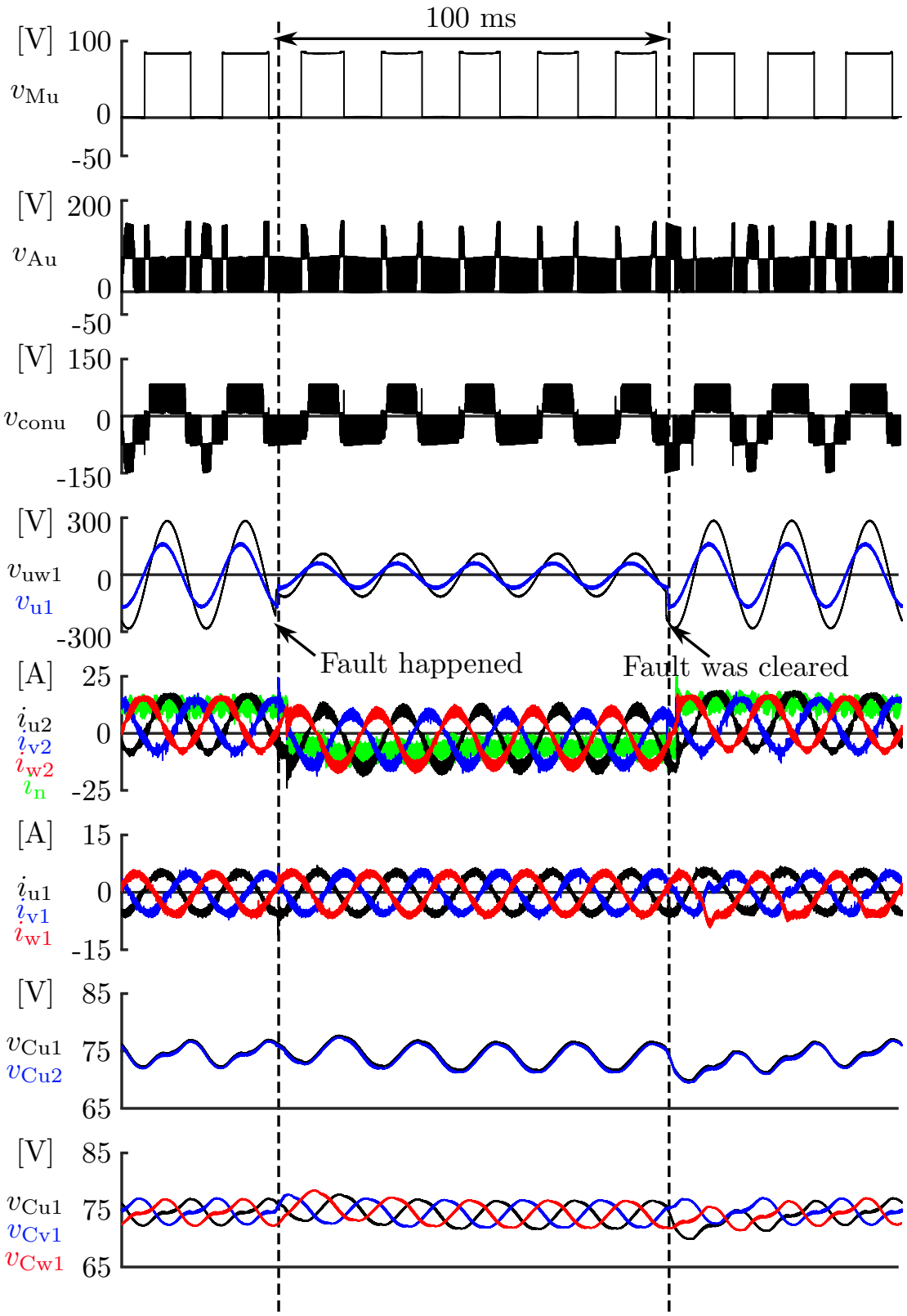

100 ms
[V] 150
v_{Mu}
0
-50
[V] 200
v_{Au}
0
-50
[V] 150
v_{conu}
0
-150
[V] 300
v_{uw1}
v_{u1}
0
-300
Fault happened
Fault was cleared
[A] 20
i_{u2}
i_{v2}
i_{w2}
i_n
0
-20
[A] 10
i_{u1}
i_{v1}
i_{w1}
0
-10
[V] 85
v_{Cu1}
v_{Cu2}
75
65
[V] 85
v_{Cu1}
v_{Cv1}
v_{Cw1}
75
65

(a)

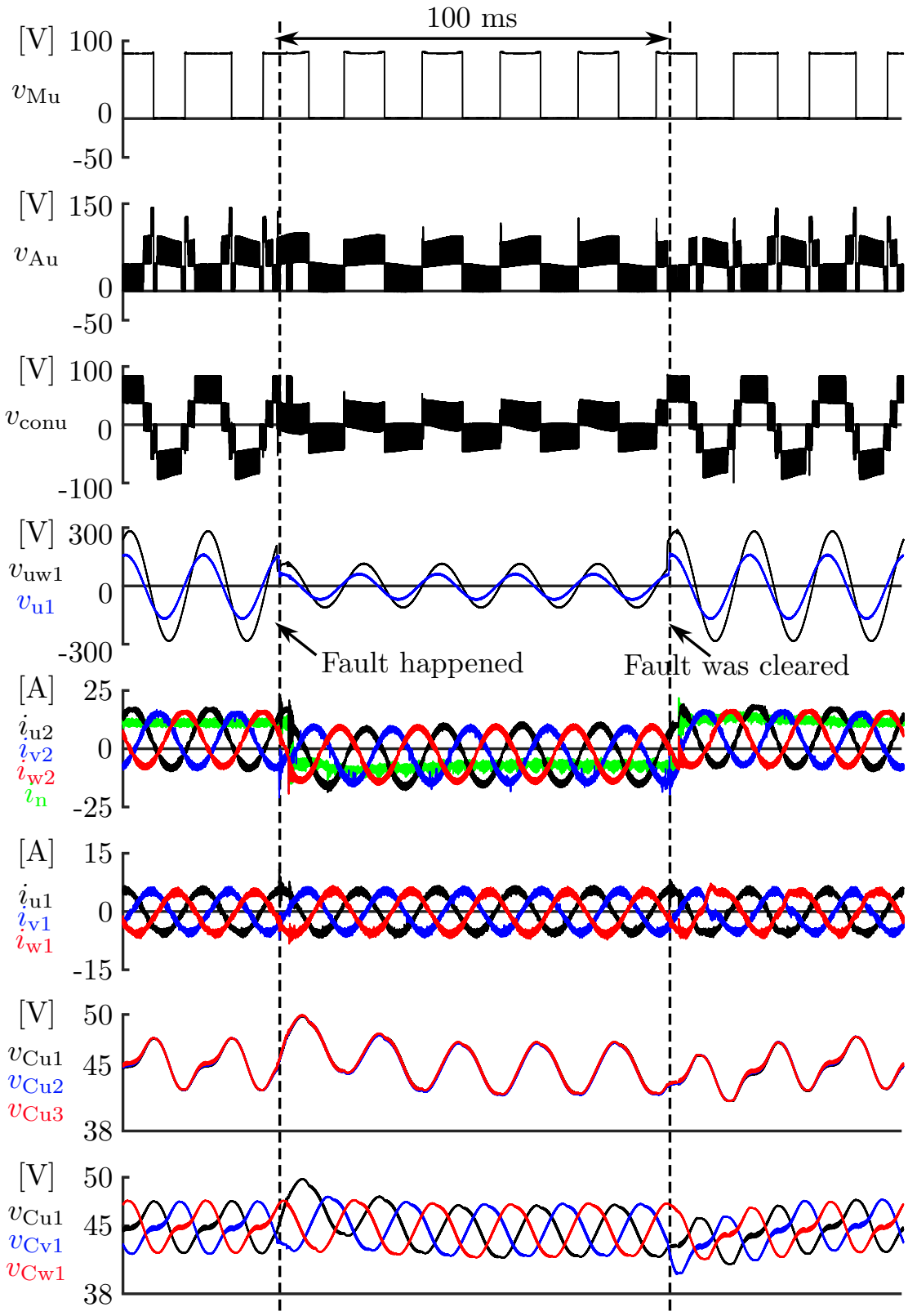


(b)

Figure 6.8: Experimental waveforms during SLG fault where $E = 135\,\mathrm{V}$ and v_{u1} dropped by 50 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

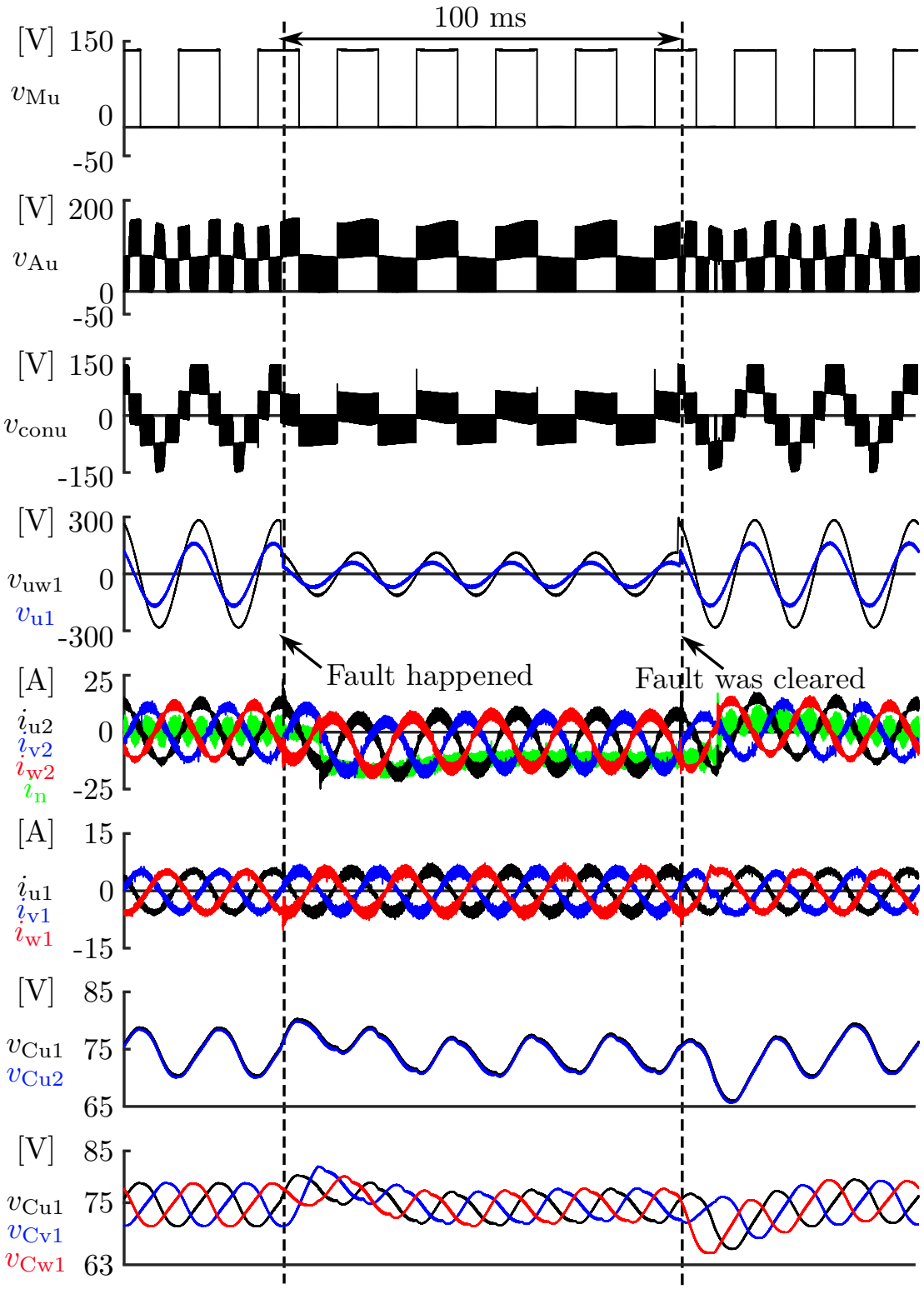

100 ms
[V] 100
v_{Mu}
0
-50
[V] 200
v_{Au}
0
-50
[V] 150
v_{conu}
0
-150
[V] 300
v_{uw1}
v_{u1}
0
-300
Fault happened
Fault was cleared
[A] 25
i_{u2}
i_{v2}
i_{w2}
i_n
0
-25
[A] 15
i_{u1}
i_{v1}
i_{w1}
0
-15
[V] 85
v_{Cu1}
v_{Cu2}
75
65
[V] 85
v_{Cu1}
v_{Cv1}
v_{Cw1}
75
65

(a)

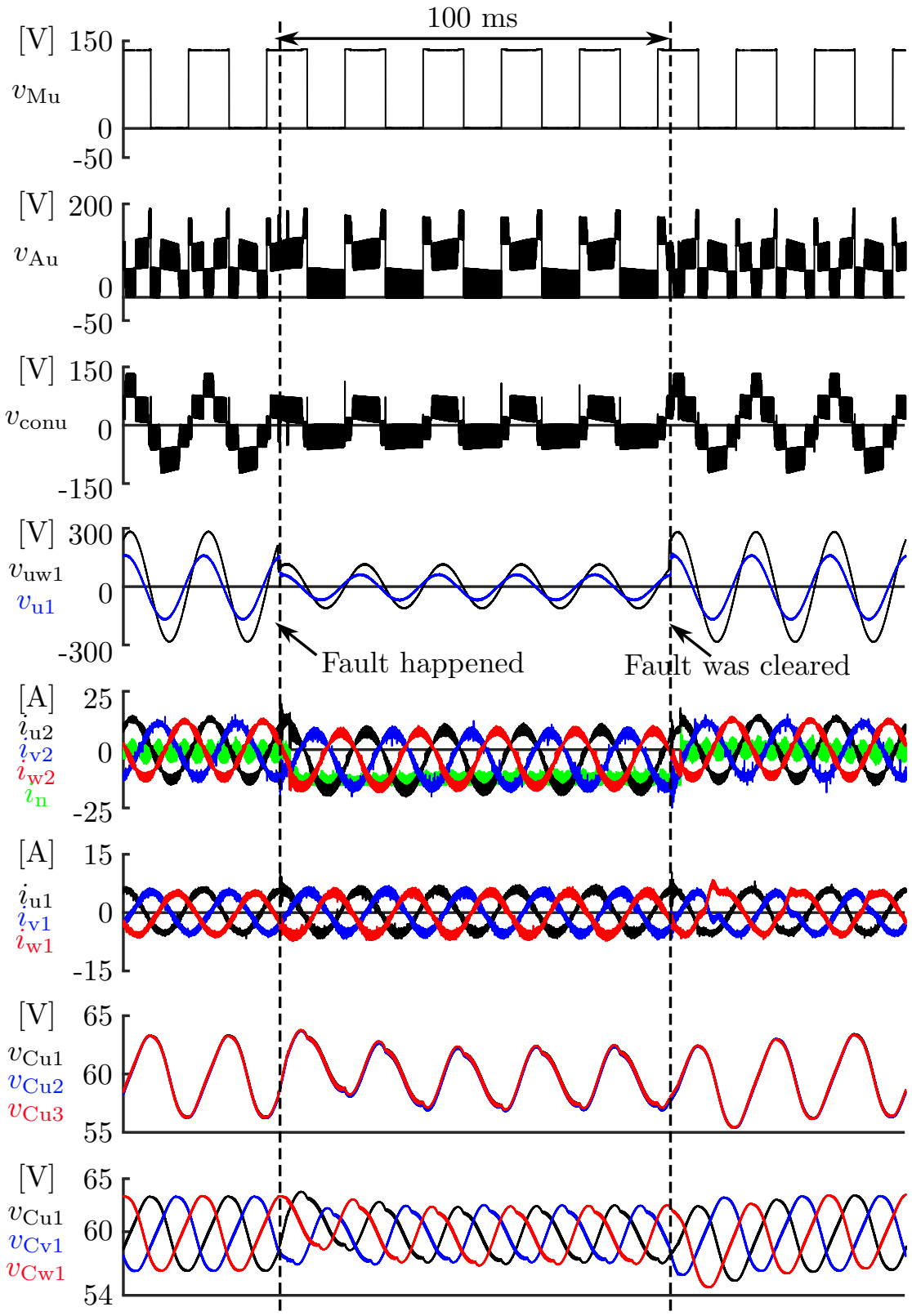


(b)

Figure 6.9: Experimental waveforms during 3P fault where $E = 85\,\mathrm{V}$ and primary side line-to-neutral voltage dropped by 60 %: a) two-cell inverter circuit, b) three-cell inverter circuit.


100 ms
[V] 150
v_{Mu}
0
-50
[V] 200
v_{Au}
0
-50
[V] 150
v_{conu}
0
-150
[V] 300
v_{uw1}
0
v_{u1}
-300
Fault happened
Fault was cleared
[A] 25
i_{u2}
i_{v2}
i_{w2}
i_n
0
-25
[A] 15
i_{u1}
i_{v1}
i_{w1}
0
-15
[V] 85
v_{Cu1}
v_{Cu2}
75
65
[V] 85
v_{Cu1}
v_{Cv1}
v_{Cw1}
75
63

(a)



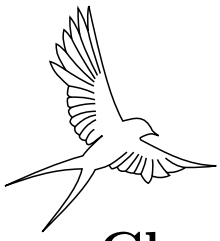
(b)

Figure 6.10: Experimental waveforms during 3P fault where $E = 135\,\mathrm{V}$ and primary side line-to-neutral voltage dropped by 60 %: a) two-cell inverter circuit, b) three-cell inverter circuit.

$\alpha = 0$ and $\frac{V_{ac}}{E} < \frac{\sqrt{2}}{\pi}$. Therefore, i_n is negative during the 3P fault according to (3.32). The DC-capacitor voltage fluctuation of each phase when the fault occurred and was cleared is similar because of the symmetrical fault. Specifically, the capacitor voltages of all phases increased when the fault occurred and they decreased when the fault was cleared. However, the DC-capacitor voltage drop of the two-cell inverter when the fault was cleared broke the operational requirement (3.11) when the DC-capacitor voltage was set to 65 V. Therefore, it was set to 75 V in the experiment. The currents and the capacitor voltages were kept balanced during the 3P fault in both inverter circuits. Fig. 6.10 shows the waveforms comparison of another experiment during the 3P fault when $p^* = 1.5\,\text{kW}$ and $E = 135\,\text{V}$. Similarly, the line-to-neutral voltage of the primary side of the transformer (grid) dropped by 60 % during the 3P fault and both inverters have similar performance as shown in Fig. 6.9. The larger voltage drop in v_{cw1} in Fig. 6.10a compared to that in Fig. 6.9a was caused by the different moments when the faults were cleared.

6.3 Conclusion

This Chapter has evaluated and compared the performance of the proposed two-cell and three-cell inverters in terms of loss, efficiency, THD performance, and experimental performance during steady and fault states to evaluate the chopper-cell number in the auxiliary converter. The comparisons have revealed that the two-cell inverter has lower total loss and higher efficiency in megawatt power-level applications. In addition, the power devices with the same voltage/current ratings can be applied to the two inverters. It has been shown that the THD performances of the two inverters are similar under the same equivalent switching frequency. The experimental verifications under the SLG and 3P faults have exhibited that the two-cell inverter shows superior performance than the three-cell inverter in terms of current and DC-capacitor voltage fluctuation.



Chapter 7

Conclusion

This dissertation presents a detailed study of a novel three-phase inverter for utility-scale PV systems where multiple cascaded bidirectional chopper cells and a three-phase line-frequency transformer with a three-limb core are used. The major contributions of this dissertation are:

- **A single-stage three-phase PV inverter with high AC output voltage and wide MPPT range** - As explained in Chapter 1, the narrow MPPT range of conventional two/three-level conventional PV inverters is hard to satisfy the requirement of the fast developing PV electricity generation. However, the proposed PV inverter has a much wider MPPT range. Meanwhile, the high AC output voltage decreases the total loss.

- **New individual current control method** - The conventional d-q-0 control method shown in Chapter 3 is not suitable to the proposed inverter circuit. The new individual current control method introduced in Chapter 4 has a better performance than the conventional one. With the new control method, the stable operation of the proposed inverter circuit is achieved.

- **Theoretical analysis focusing on the LVRT behaviors of the proposed inverter** - The theoretical analysis includes the capacitor voltage fluctuation, the reason for the overmodulation and the current spikes, and the limit of the LVRT capability/safety operation zone under the SLG fault. The theoretical analysis is based on mathematical calculation and figures and experimental verification using the same downscaled system verified the reliability of the theoretical analysis.

- **Evaluation of chopper-cell number** - The performance of the proposed PV inverter with two chopper cells and three chopper cells is compared in terms of loss, efficiency, THD performance, and experimental performance during steady and fault states. The comparisons are based on theoretical calculation and experimental verification and it is revealed that the two-cell inverter has lower total loss and higher efficiency in megawatt power-level applications. The conclusion is that the two-cell inverter is better than the three-cell inverter in terms of loss, efficiency, THD performance, and experimental performance during steady and fault states.

7.1 Future Research

Even though an abundance of information is included in this dissertation, there are still more could be discussed about the proposed PV inverter:

- **Enhancement of control method** - Since the AC components are controlled directly in the proposed new individual control method, the PI control is replaced with a proportional control. However, the proportional resonant control may have a better performance in the proposed inverter circuit. It is worthy to test whether the proportional resonant control has a better performance.

- **Improvement of LVRT performance** - As shown in Fig. 5.14, there is limit to the LVRT capability of the proposed inverter, which means operational failures will happen under some serious grid faults. Therefore, new operational principles or new control methods are needed to handle the grid fault situations.

- **Widening the MPPT range** - It is proved that the MPPT range can be even wider with the introduction of the third-order harmonic components. However, this requires the modification of the circuit configuration and the control methods.

List of Publications

Journal Publications

1. L. Qiao, Y. Shimizu and M. Hagiwara, "Current Control of Three-Phase Inverter Using Multiple Bidirectional Choppers Intended for 1.5-kV PV Systems," in IEEE Transactions on Industry Applications, vol. 59, no. 1, pp. 910-924, Jan.-Feb. 2023, doi: 10.1109/TIA.2022.3204736.

2. L. Qiao and M. Hagiwara, "Evaluation and Performance of Three-Phase Inverter Using Multiple Bidirectional Choppers Intended for 1.5-kVdc PV Systems," in IEEE Access, vol. 11, pp. 32636-32647, 2023, doi: 10.1109/ACCESS.2023.3263526.

Conference Publications

1. L. Qiao, Y. Shimizu and M. Hagiwara, "Experimental Verification of Three-phase PV Inverter Using Multiple Bidirectional Choppers for Utility-scale PV Systems," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 259-266, doi: 10.1109/ECCE47101.2021.9595228

2. L. Qiao and M. Hagiwara, "Performance of Three-phase Inverter Using Multiple Bidirectional Choppers for 1.5-kV PV Systems Capable of Wide MPPT Range," 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 338-344, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807031.

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