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Interface Engineering in Amorphous Oxide Semiconductor TFTs for Display and Memory Applications

Amorphous oxide semiconductor thin-film transistor (AOS TFT) plays an important role as the backplane to drive flat panel displays utilizing its high mobility, low off current, transparency, and capability for large-area fabrication. As the demand for superior display quality and the interest in the applications of memory continue to grow, the performance requirements of AOS have become increasingly stringent. In the display field, the quest of higher resolution and dynamic range has led to the adoption of high-mobility AOSs, but the bias-instability of these materials has impeded the performance. When AOS transistors are employed in memory devices, the complexity of the architecture and the reduced scale to nanometer dimensions highlights interface issues that are overlooked in flat panel display driving TFTs. The advancement of AOS TFT critically depends on carefully addressing the interface issues of transistor devices, specifically on how to solve or leverage the interactions between different layers and AOS for superior performance.

In this thesis, the several interfaces of AOS TFT devices are investigated, including the oxide semiconductor back channel, the interface between the channel and dielectric, and the contact interface. The impact of impurities adsorbed on the TFT back channel on bias-stress stability is discussed, and the use of self-aligned passivation is proposed to address the complexities of passivation processes and enhance device stability. Exploiting the characteristic of the interface between channel and dielectric, where there are high concentration defects serving as electron trapping and de-trapping, a charge trapping random-access memory device suitable for high-order in-memory computing is developed. For the contact interface of memory devices with complex architectures, the employment of Pd to create a good hydrogen transfer pathway is explored to mitigate the issue of high contact resistance at buried contact interfaces. These investigations into interfaces are significant for the development of high-performance displays and high-density, multi-functional memory devices.