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題目(和文)	ディスプレイおよびメモリ応用のための非晶質酸化物半導体TFTの界面エンジニアリング
Title(English)	Interface Engineering in Amorphous Oxide Semiconductor TFTs for Display and Memory Applications
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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

Amorphous oxide semiconductor thin-film transistor (AOS TFT) plays an important role as the backplane to drive flat panel displays utilizing its high mobility, low off current, transparency, and capability for large-area fabrication. As the demand for superior display quality and the interest in the applications of memory continue to grow, the performance requirements of AOS have become increasingly stringent. In the display field, the quest of higher resolution and dynamic range has led to the adoption of high-mobility AOSs, but the bias-instability of these materials has impeded the performance. When AOS transistors are employed in memory devices, the complexity of the architecture and the reduced scale to nanometer dimensions highlights interface issues that are overlooked in flat panel display driving TFTs. The advancement of AOS TFT critically depends on carefully addressing the interface issues of transistor devices, specifically on how to solve or leverage the interactions between different layers and AOS for superior performance.

In this thesis, the several interfaces of AOS TFT devices are investigated, including the oxide semiconductor back channel, the interface between the channel and dielectric, and the contact interface. These investigations into interfaces are significant for the development of high-performance displays and high-density, multi-functional memory devices.

The TFTs with amorphous indium-tin-zinc oxide (a-ITZO) semiconductors have attracted much attention for their high field effect mobility. However, the significant impurity sensitivity of AOS semiconductor seriously affects the stability of electrical characteristic. The absorbed charged oxygen, moisture, and residual organic component from fabrication process at the surface of channel induce a serious shift of threshold voltage under bias gate voltage stress. In chapter 2, a novel self-aligned passivation process by employing developer-etchable amorphous gallium oxide (a-GaO_x) to obtain highly stable a-ITZO transistors and also simplify the conventional passivation process without additional etching steps was introduced. The contact issue caused by the passivation layer is eliminated owing to the etching process, and the ITZO channel area still remains passivated by a-GaO_x. Benefited from the a-GaO_x layer, the threshold voltage (V_T) shift under 1-hour NBS of a-ITZO transistors are significantly decreased to 0.09 V, and the devices exhibit good PBS stability of V_T shift of 0.34 V in 1 h. The passivated transistors also obtain the high field effect mobility over 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and the very low subthreshold slope under 90 mV/dec.

With the growing computational demands of neural networks, the traditional CPU plus memory configuration of the Von Neumann architecture is increasingly found to be inefficient in handling parallel computations such as polynomial operations. Consequently, in-memory computing architectures have recently garnered significant attention due to their ability to efficiently manage parallel computations. The floating-gate transistor offers the capability to perform in-memory ternary multiplication (TM) operations. However, the complex fabrication process of the floating-gate structure and the high voltages required for programming remain areas that need further improvement. On other hand, the interface between the dielectric and oxide semiconductor channel in AOS TFTs inherently possesses defects that can trap and de-trap electrons during device operation, thus altering the electrical characteristics of the device. In chapter 3, a TaO_x-based a-IGZO TFT memory, named charge trapping random-access memory (CT-RAM) was introduced, which can execute ternary computations by utilizing the change in transconductance (g_m) curves due to charge trapping at the interface. Unlike conventional TFTs that only allow two input parameters (drain voltage, V_D and gate voltage, V_G), employing TaO_x as the dielectric layer, CT-RAM enables the alteration of the conductivity properties (i.e. g_m) of TFT through V_G, serving as a third modifiable input parameter. This method is helpful for the realization of polynomial regression computation engines with reduced hardware overhead.

As the focus on AOS in memory applications deepens, there is a push for higher packing densities and more efficient read-write efficiencies, leading to increasingly complex AOS transistor structures with dimensions scaled down to the nanometer size. This trend is accompanied by more pronounced contact issues. However, conventional methods to addressing contact resistance in TFTs used for flat-panel displays are not applicable to buried interfaces. Development of novel method to resolve this issue is a current challenge for the

future development of complex structured AOS memory devices. In chapter 4, a strategy utilizing Palladium (Pd) as an electrode material to construct a hydrogen transfer pathway was introduced. During hydrogen annealing treatment, Pd's extremely high hydrogen diffusion rate, moderate hydrogen solubility and high reactivity of H^0 are utilized to efficiently transport hydrogen to the interface. This is based on the principle that when the charge transition level of $E(H^+/H^-)$ falls below the conduction band minimum of a high mobility oxide semiconductor, it generates carrier electrons, facilitating the formation of a high charge density interface layer. Detection through hard X-ray photoelectron spectroscopy shows that the high reactivity of H^0 within Pd reduces metal oxides at the interface, forming a metallic interface layer. By comparing processing times and temperatures, it was found that 150°C is the optimal temperature for annealing in a 5% H_2 atmosphere for 10 min, which did not affect the channel length. The contact resistance of the treated a-IGZO bottom contact TFT was reduced by more than two orders of magnitude, and the mobility was enhanced from 3.2 to ~20 $cm^2 V^{-1} s^{-1}$. Furthermore, the treated a-IGZO TFT also demonstrated excellent bias-stability, further proving the reliability of using Pd as a hydrogen transfer pathway in the process.