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Article / Book Information

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Doctoral Program

論 文 要 旨

THESIS SUMMARY

系・コース： Department of, Graduate major in	Information and Communications Engineering 系 コース	申請学位（専攻分野）： Academic Degree Requested	博士 Doctor of (Philosophy)
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要旨（英文 800 語程度）

Thesis Summary (approx.800 English Words)

This dissertation, titled "Routing Strategies for Critical Routing Layers in Modern Advanced Chips," consists of six chapters.

Chapter 1 is "Introduction." This research highlights the growing importance of 3D integration technology in modern semiconductor devices. Specifically, the study discusses the use of bonding techniques to directly connect wafers, a crucial advancement in the development of products such as CMOS image sensors and NAND flash memory. These technologies enable higher device performance and compact designs but introduce new challenges, particularly in routing design. The presence of bonding pads, arranged in arrays, obstructs conventional automated routing methods, necessitating innovative solutions. This research introduces novel routing strategies to address these issues, ensuring efficient routing and improved design feasibility in 3D IC implementations. Additionally, the introduction provides an overview of the motivation behind this study, discussing the limitations of existing routing methodologies and the necessity for new approaches that can accommodate the constraints and complexities inherent in 3D IC routing.

Chapter 2 is "Channel Routing." It provides an overview of related research and conventional channel structures. Traditional two-layer standard-cell routing methods position net terminals along the periphery of the routing channel. However, in critical routing layers of 3D ICs, terminals may be located within the channel itself, and either horizontal or vertical routing resources may be severely constrained. Existing automatic routing algorithms struggle to adapt to these new conditions, leading to inefficiencies in routing completion and quality. This chapter emphasizes the necessity of developing a General Channel Single-Trunk Routing Method, which ensures efficient routing by assigning each net a single trunk in a uniform direction. By optimizing trunk assignments, the method enhances routing feasibility while considering the structural constraints of 3D IC routing layers. Furthermore, the chapter discusses prior research in channel routing and how the new method proposed in this dissertation builds upon and extends existing techniques to meet the unique demands of 3D ICs.

Chapter 3 is "Routing Framework of GCRP." It formulates the general channel routing problem as a trunk assignment problem, where each net's trunk is assigned to a specific routing track. This dissertation introduces the Greedy Routing Framework with Guarantee (GRFG), which incrementally assigns trunks while ensuring that no overlaps occur. GRFG guarantees the completion of trunk assignments as long as the number of available tracks meets or exceeds the maximum congestion level within the routing channel. By implementing GRFG, routing completion is assured while allowing for priority-based trunk assignments, resulting in diverse and optimized routing solutions. Furthermore, the chapter discusses the advantages of a structured framework in enabling scalable and effective routing in highly constrained environments. The discussion also includes an analysis of potential limitations and extensions of GRFG, providing insight into future developments in routing methodologies.

Chapter 4 is "Length Minimization Algorithm of GCRP." It focuses on reducing vertical wire length in general channels to optimize routing efficiency. The study proposes the Symmetric Difference General Channel Routing Algorithm (SDG), which strategically assigns a net's trunk to a track where the symmetric difference in the number of terminals above and below the track is minimized. This heuristic approach effectively reduces total vertical routing length, thereby lowering wire resistance and improving signal integrity. SDG builds upon the principles of GRFG by prioritizing nets based on their symmetric difference of terminal counts, leading to optimized routing solutions. Additionally, the chapter evaluates the impact of SDG on routing feasibility and its ability to balance track usage effectively in scenarios with varying congestion levels. The chapter further presents simulation results comparing SDG with traditional routing techniques, highlighting its advantages in terms of wire length reduction and overall efficiency.

Chapter 5 is "Local Congestion Alleviation Algorithm of GCRP." It addresses the critical issue of local congestion, which can significantly hinder routing completion. To mitigate this challenge, the study introduces the Under, Enclose, Over Routing Algorithm (UEO), a heuristic routing method designed to

reduce local vertical congestion in general channels. UEO establishes a range of preferred tracks where congestion-prone trunks should be assigned while prioritizing nets to avoid heavily congested regions whenever possible. Although UEO may slightly increase the total vertical wire length compared to SDG, it significantly alleviates local congestion, thereby improving the overall feasibility of routing solutions. This chapter also analyzes the trade-offs between minimizing congestion and optimizing routing efficiency, providing a comprehensive assessment of UEO's effectiveness in addressing congestion-related constraints in 3D IC routing. The impact of UEO on routing scalability and its ability to improve manufacturability in real-world semiconductor fabrication processes are also discussed.

Chapter 6 is "Conclusion." The dissertation concludes by summarizing the key contributions of the proposed single-trunk routing algorithms for general channels. The study demonstrates that these methodologies significantly enhance routing efficiency in 3D IC implementations by systematically addressing congestion and minimizing wire length. Furthermore, the dissertation outlines future research directions, emphasizing the need to incorporate real-world design constraints such as process variation, power distribution, and thermal management. These considerations will be essential in refining and extending the applicability of the proposed routing strategies to next-generation semiconductor technologies.

This dissertation presents and validates novel routing strategies for critical routing layers in 3D IC implementations. The proposed methods offer substantial contributions to engineering and industrial applications, demonstrating significant value as a doctoral dissertation in engineering.