論文 / 著書情報
Article / Book Information

題目(和文)	将来の三次元積層型電界効果トランジスタに向けた低基板温度及び低粒子フラックススパッタリングによるMoS2膜質向上
Title(English)	Improvement of MoS2 Film Quality using Low-Particle-Flux Sputtering at Low-Substrate Temperature for Future 3D-Stacked Field-Effect Transistors
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種別(和文)	論文要旨
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（博士課程）
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論 文 要 旨

THESIS SUMMARY

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要旨（英文 800 語程度）
Thesis Summary（approx.800 English Words ）

This thesis extensively investigates the improvement of molybdenum disulfide (MoS_2) film quality at low temperatures for future three-dimensional stacked field-effect transistors. MoS_2 films are known to exhibit high electron mobility even in an atomic layer thickness, making them a promising alternative to silicon channels in next-generation 3Dstacked FETs. Conventional methods for forming MoS_2 films include exfoliation and chemical vapor deposition (CVD) conducted at high temperatures of 800^{o}C or more. While these methods are effective for obtaining high-quality films, they are limited by their inability to effectively reduce defect densities and their incompatibility with the strict thermal budget requirements for stacked transistors. To overcome these challenges, the author adopted sputtering, a deposition method that can produce large-area, uniform films at significantly lower temperatures below 500^{o}C. However, sputtered MoS_2 films exhibit problems such as small grain sizes and high sulfur defect densities, limiting their potential for practical applications. To address these issues, sulfur-vapor annealing (S-annealing) at 700^{o}C has been proposed in previous studies to compensate for sulfur vacancies and improve film quality. This study seeks to deepen the understanding of the effects of S-annealing on MoS_2 films by sputtering, identify strategies to improve film quality even before S-annealing, and explore the feasibility of producing high-quality films at even lower temperatures. The author set three critical target parameters for MoS_2 film quality. First, the film formation temperature was set to 700^{o}C or less for front-end-of-line (FEOL) processes and 400^{o}C or less for back-end-of-line (BEOL) processes to meet industrial requirements. Second, the crystal size was set to 7.9 nm or more for the channel dimensions of future semiconductor devices. Third, the target mobility is set at 185 cm^2/Vs with a corresponding sulfur defect density (Vs) below 0.14%. These parameters serve as a guideline for balancing material performance with manufacturing feasibility. The crystal growth mechanism during sputtering is analyzed, which examined how the surface migration length of sputtered particles contributes to the grain size increase. Three key factors that enlarge this surface migration length of particles were identified: increasing the substrate temperature ($T_{\text{sub.}}$), increasing the flux temperature (T_{flux}), and reducing the particle flux to the substrate. Additionally, simulations of the behavior of sputtered particles traveling from the target to the substrate revealed that high RF power, a short target-to-substrate distance, and low Ar pressure are practical approaches to increase the sulfur flux to the substrate, thereby reducing the sulfur defect density. These suggest that process parameters must be carefully tuned to optimize the deposition conditions for high-quality films. First, it was observed that enlarging $T_{sub.}$ enhances the surface migration of sputtered particles, leading to larger grains. However, excessively high $T_{sub.}$ caused an increase in sulfur defect density, likely due to sulfur evaporation under prolonged exposure to elevated temperatures. S-annealing effectively compensated for these deficiencies, restoring film quality and reducing defect densities. The optimal substrate temperature was identified as 300°C, where films showed the lowest sulfur defect density after annealing. This temperature represents an ideal trade-off between enabling sufficient surface migration and avoiding excessive sulfur loss during deposition. Next, to further improve crystal size, the author investigated the effects of RF power modulation, which controls both T_{flux} and particle flux. Intermediate RF power provided the best balance, producing films with sufficient Tflux and low particle flux, which promoted more significant grain formation. Additionally, a grid was introduced into the sputtering system to reduce particle flux further while maintaining adequate flux energy. This approach significantly improved the crystal size with a lower deposition rate, and the nucleation density decreases with a low particle flux. Finally, the performance of the sputtering method was benchmarked against other deposition techniques. It was demonstrated that sputtering achieves superior results in terms of crystallite size with low-temperature deposition. Crystal size reached a maximum size of 26 nm and an average size of 9.1 nm, exceeding the target of 7.9 nm. Films deposited at 300°C met the thermal budget requirements for FEOL and BEOL processes while showing significant improvements in grain size. However, the standard deviation was 7.9 nm, suggesting the need for selective removal of the microcrystalline regions of the second layer and deposition with even lower particle flux. Furthermore, the sulfur defect density remained at 1.65%, which calculated the mobility of ~26.5 cm^2/Vs, indicating that further optimization is required to achieve the target mobility. Additional studies on sulfur flux supply during sputtering are recommended to bridge this gap and further enhance material performance. In conclusion, this thesis comprehensively analyzes the factors influencing the quality of sputtered MoS_2 films. The results demonstrate that optimizing particle temperature on the substrate surface and reducing particle flux during sputtering significantly enhances crystal size, while additional sulfur supply can effectively mitigate sulfur defects. These findings contribute to developing high-quality MoS_2 films suitable for next-generation logic semiconductors and offer valuable insights for industrial applications. This work establishes a foundation for further exploration of sputtering techniques and their potential integration into advanced semiconductor manufacturing processes.