論文 / 著書情報
Article / Book Information

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Journal/Book name	European Solid-State Circuits Conference (ESSCIRC), , , pp. 440–443
発行日 / Issue date	2009, 9
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A low-phase-noise injection-locked differential ring-VCO with half-integral subharmonic locking in 0.18 μm CMOS

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***Abstract*—Design and implementation of a CMOS differential ring-VCO that locks at half-integral $(1.5, 2.5, 3.5, \cdots)$ as well as integral $(1, 2, 3, \cdots)$ multiples of the injected reference frequency $f_{\rm ref}$ are presented. The advantage of half-integral subharmonic locking is that, for a given VCO output frequency step, the output phase noise can be lowered than when using integral subharmonic locking because of the higher $(2\times)$ reference frequency. For example, the 1-MHz-offset phase noise at a VCO output frequency of 1.5 GHz was -136 dBc/Hz when locked to an integral subharmonic of $f_{\rm ref} = 0.5$ GHz, whereas it was as low as -139 dBc/Hz when locked to a half-integral subharmonic of $f_{\rm ref} = 1.0$ GHz. The ring-VCO was fabricated with a 0.18 μm CMOS process. An explanation is given as to why it locks to half-integral subharmonics and how such an oscillator could be designed. Half-integral or, more generally, nonintegral subharmonic locking could make an effective means to reduce the phase noise of high-resolution injection-locked VCOs.**

I. Introduction

While digital circuit blocks have been shrinking with the continuous advancement of CMOS technologies, it is difficult to scale down RF/analog circuit blocks due to the presence of large circuit elements, especially passive components. The lack of scalability of RF/analog circuit blocks has been becoming a serious problem since they consume growing percentage of expensive Si real estate. One of the burning questions of the day is how to make RF/analog blocks scalable.

Ring oscillator-based voltage-controlled oscillators (VCOs) are attractive in terms of frequency tuning range. Furthermore, they have the particularly desirable property that inductors can be dispensed with altogether, which makes ring-VCOs highly scalable. Unfortunately, their phase-noise performance is far inferior to that of LC-VCOs' with comparable power consumption. It has been quantitatively shown [1], [2] that it is very difficult to lower the phase noise of a ring-VCO to an acceptable level on its own without undue power consumption. Nevertheless, low-phase-noise ring-VCO is still a possibility if some noise-suppression mechanism could be added. One such option would be injection locking. Assuming that $L_{\rm out}(\omega)$, $L_{\rm ref}(\omega)$, and $L_{\rm vco}(\omega)$ are phase noise power functions of an injection-locked VCO, a reference signal, and a free-running VCO, respectively, $L_{\rm out}(\omega)$ can be expressed as

$$L_{\rm out}(\omega) = L_{\rm ref}(\omega) \cdot H_{\rm LPF}(\omega) + L_{\rm vco}(\omega) \cdot H_{\rm HPF}(\omega), \quad (1)$$

where $H_{\rm LPF}(\omega)$ and $H_{\rm HPF}(\omega)$ are low-pass and high-pass transfer functions, respectively. Both $H_{\rm HPF}(\omega)$ and $H_{\rm LPF}(\omega)$ have the same cutoff frequency, known as the loop bandwidth. It is proportional to the power and the frequency of the injected signal [3]. Eq. (1) says that the noise in the injected signal mainly affects the output noise at low offset frequencies (relative to the carrier frequency) and that the VCO noise becomes dominant as the offset approaches the cutoff frequency. If the injected signal has low phase noise and large enough power, the VCO output could have improved phase noise characteristics within the loop bandwidth. Moreover, injection-locked VCOs tend to have smaller footprints, less restrictions on the design of loop bandwidth, and less internal noise sources than conventional phase-locked loops (PLLs) [3].

In this paper, we propose a method of reducing the phase noise of subharmonically injection-locked ring-VCOs without coarsening the output frequency step.

II. Injection locking and locking frequency selection rule

The injection-locking mode to be used in VCOs will be fundamental or subharmonic locking, in which the frequency $f_{\rm ref}$ of the injected reference signal is, respectively, equal to or lower than the VCO output frequency $f_{\rm o}$. In the ordinary integral subharmonic locking, the subharmonic ratio $r = f_{\rm ref}/f_{\rm o}$ is given by $1/n$, where $n = 2, 3, 4, \cdots$. Then, if a VCO is to be able to generate frequencies with a fine step, $f_{\rm ref}$ has to be low. If, however, $f_{\rm ref}$ and r are halved simultaneously, the phase noise originating from the VCO cannot be rejected as efficiently because the loop bandwidth (i.e. the cutoff frequency of $H_{\rm HPF}(\omega)$) also halves. High-offset output phase noise (still within the loop bandwidth) is expected to increase by 6 dB by halving $f_{\rm ref}$ [3]–[5]. This is a major obstacle to realizing a high-resolution VCO by lowering $f_{\rm ref}$. Conversely, if $f_{\rm ref}$ could somehow be doubled without adverse effects, the phase noise could be reduced. To realize scalable low-phase-noise high-resolution ring-VCOs, we propose to exploit half-integral subharmonic locking, in which the subharmonic ratio is given by $r = 1/1.5, 1/2, 1/2.5, 1/3, \cdots$. This is the simplest case of nonintegral subharmonic locking [6]. If, for instance, injections are given both at the rising and falling edges of a 50-%-duty-cycle reference signal as shown in Fig. 1, phase error $\Delta\phi$ would not accumulate as much as in the case where only one injection is given every $1/f_{\rm ref}$. Note that the operation of our ring-VCO is somewhat different than Fig. 1.

In an injection-locked oscillator, the possibility of locking to *some* nonintegral subharmonics can be understood by considering a feedback system with nonlinearity [6]. This model is an extension of that for integral subharmonic locking [7].

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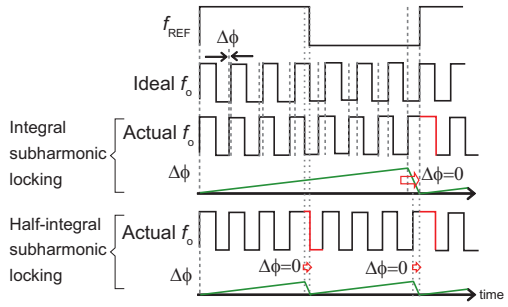

Fig. 1. The changes of phase error $\Delta\phi$ when phase corrections are made once or twice per $1/f_{\rm ref}$.

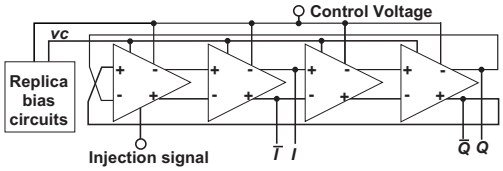

Fig. 2. Four-stage injection-locked differential ring-VCO.

However, no explanation has been given as to *which* subharmonics might actually be selected for locking. The selection rule for locking frequency would follow from symmetry consideration [8]. To put it loosely, if an oscillator locks to a subharmonic $f_{\rm ref} = rf_{\rm o}$, whether integral or nonintegral, the oscillator's electrical response should be invariant under a temporal translation of the injected signal by $1/(rf_{\rm o})$. In theory, by designing an oscillator so that it possesses necessary symmetry properties, it can be made to lock to desired subharmonics.

In the following section, we describe the design of an injection-locked CMOS differential ring-VCO capable of half-integral subharmonic locking due to topological symmetry.

III. Design of the Injection-Locked Ring-VCO

The proposed ring-VCO is shown in Fig. 2. It is based on a four-stage differential ring oscillator. The reference signal is injected into the leftmost delay cell as rail-to-rail pulses. As far as the topology is concerned, the circuit in Fig. 2 might appear to be a normal differential ring oscillator capable of (only) integral subharmonic locking.

Let us consider for simplicity the case of fundamental locking, namely $f_{\rm o} = f_{\rm ref}$. In that case, the amount of phase shift induced by an injected pulse should be a periodic function of the delay of the arrival of the pulse relative to, say, a rising edge of free-running oscillations. The period would be $1/f_{\rm o}$. Recall now that the ring-VCO in Fig. 2 is a differential circuit and has a certain symmetry. Suppose in addition that the reference pulses force the voltage difference between the upper and lower nodes in the leftmost delay cell to go to zero. A wavefront traveling in the Möbius loop (Fig. 2) is forced to make phase corrections by the injected pulses only once as it travels around the loop. But there is one other wavefront, traveling at the opposite end of the loop, that undergoes nominally the same phase corrections. Then, in the time domain, the amount of phase shift induced by a pulse should actually oscillate with the period of $1/(2f_{\rm o})$ as a function of the temporal translation of the reference signal, as shown in Fig. 3. This allows the oscillator to lock to $f_{\rm ref} = f_{\rm o}/1.5$, for example (Fig. 3). Thus, our differential ring-VCO can lock to half-integral subharmonics. In effect, the situation is similar to that shown in Fig. 1, and results in phase noise reduction. Note that perfect symmetry is not a requirement; otherwise, the locking range would be infinitesimal. As will be shown in the next section, the proposed ring-VCO shows fairly wide locking ranges. The adoption of a ring-VCO rather than a high-Q resonator-based VCO is actually an important design decision also in this regard, for (locking range) $\simeq$ (loop bandwidth) $\propto Q^{-1}$ [7].

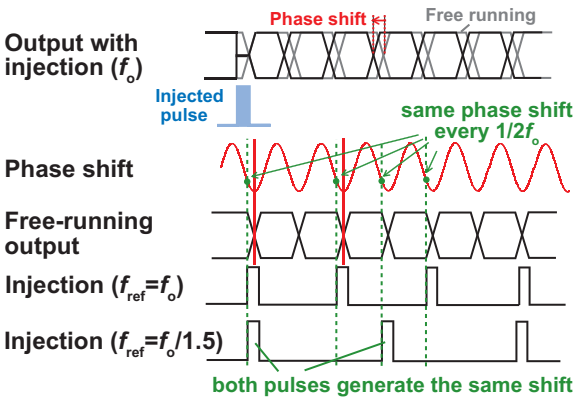

Fig. 3. The mechanism of half-integral subharmonic locking in the proposed differential ring-VCO. The amount of phase shift induced by an injected pulse is invariant under a temporal translation of the pulse by $1/(2f_{\rm o})$ (corresponding to $r = 2$) because of the designed symmetry of the circuit.

A schematic of the proposed delay cell with a voltage-controlled differential load is shown in Fig. 4. The load comprises a pMOS latch, which produces delay or phase-rotation required for satisfying the oscillation condition. In the commonly-used delay cells with a pMOS resistive load, the range of the control voltage that has a reasonable sensitivity is limited to 0 V to the pMOS threshold voltage. In the proposed delay cell, the nMOS transistors $\rm M_{n4}$ and $\rm M_{n5}$ are added in order to make the sensitive range rail-to-rail (0 V to 1.8 V), thereby offering superior controllability. Incidentally, this design also makes the delay cell suitable for the use in PLLs. Those nMOS transistors are considerably smaller than other transistors constituting the load. As the control voltage rises, $\rm M_{n4}$ and $\rm M_{n5}$ lower the output voltages $V_{\rm out}$ and $V_{\rm outb}$ and enhance the latching action. To widen the frequency-tuning range, a simple replica bias circuit is adopted. It reduces the tail current as the oscillation frequency becomes lower. The ring-VCO has a frequency-tuning range of 1.0 GHz to 2.2 GHz when free-running.

Narrow pulses are injected into a delay cell (Fig. 2) by switching $\rm M_{ni1}$ and $\rm M_{ni2}$ in Fig. 4. This topology is known as the direct injection-locking scheme [9]. The amplitude of the reference pulses is rail-to-rail. This is to ensure that the differential voltage goes to almost zero when a pulse is

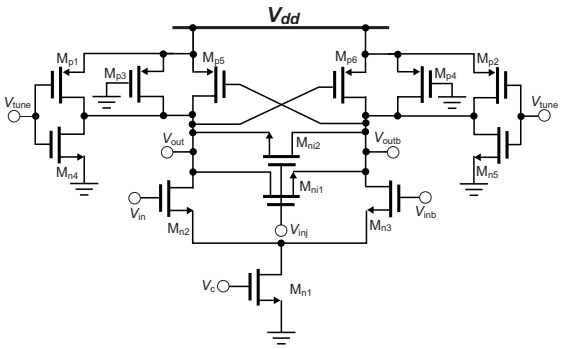

Fig. 4. Proposed differential delay cell.

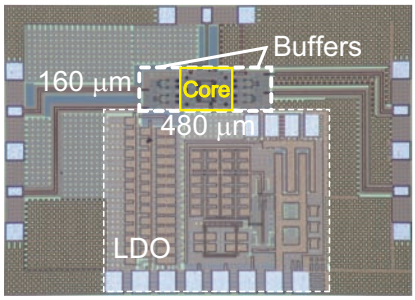

Fig. 5. A micrograph of the VCO with output buffers, powered by a low-dropout voltage regulator (LDO). The latter converts 3.3 V to 1.8 V.

applied and also to make the switches exhibit nonlinearity. Otherwise, the symmetry and nonlinearity required for half-integral subharmonic locking could be lost.

IV. Measurement Results

Fig. 5 shows a chip micrograph. The area of the ring-VCO is $480 \times 160\,\mu\text{m}^2$ including output buffers. 250-ps-wide reference input pulses were generated by Anritsu MP1761B pulse pattern generator. The output signal was analyzed by Agilent Technologies E5052A signal source analyzer. Fig. 6 shows VCO responses with and without a reference input of $f_{\text{ref}} = 80\,\text{MHz}$. As the control voltage was swept, the VCO successfully locked to half-integral subharmonics.

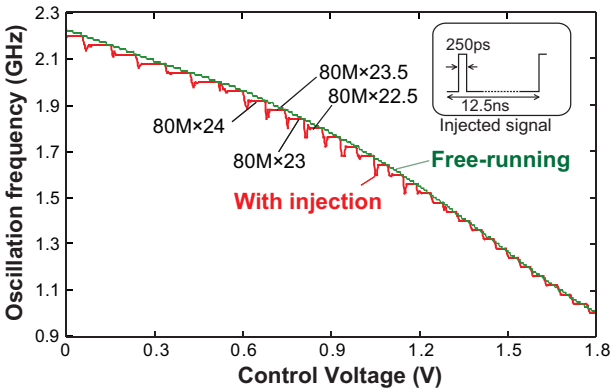

Fig. 6. Measured oscillation frequency f_{o} versus the control voltage V_{tune} with and without an 80 MHz pulsed input.

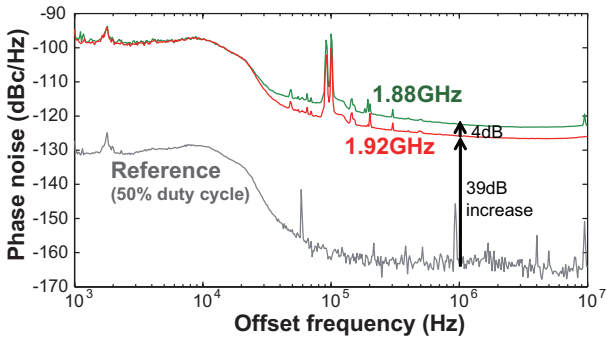

Fig. 7. Measured phase noise of a reference signal at $f_{\text{ref}} = 80\,\text{MHz}$ with a 50 % duty cycle, an 1.92 GHz ($= 24 f_{\text{ref}}$) output ($V_{\text{tune}} = 697\,\text{mV}$), and an 1.88 GHz ($= 23.5 f_{\text{ref}}$) output ($V_{\text{tune}} = 755\,\text{mV}$).

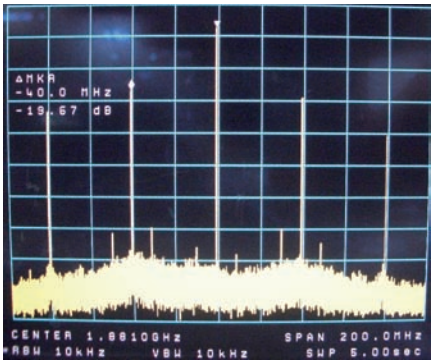

Fig. 8. Measured output frequency spectrum of the ring-VCO at $f_{\text{o}} = 1.88\,\text{GHz}$ with $f_{\text{ref}} = 80\,\text{MHz}$ when phase noise was minimized.

Fig. 7 shows the phase-noise characteristics of VCO outputs at 1.88 GHz and 1.92 GHz in the lowest-phase-noise condition when locked to $f_{\text{ref}} = 80\,\text{MHz}$ and also an 80 MHz input signal with a 50 % duty cycle. The reason for showing the result for 50 % duty cycle is that the signal source analyzer failed to correctly analyze the actual input pulses (2 % duty cycle at $f_{\text{ref}} = 80\,\text{MHz}$). The free-running signal at $f_{\text{o}} = 1.92\,\text{GHz}$ had a phase noise of $-91\,\text{dBc/Hz}$ at 1 MHz offset. Compared to the 50-%-duty-cycle input signal, the output phase noise at 1.92 GHz and 1.88 GHz were higher by about 39 dB and 43 dB, respectively. Since $f_{\text{o}} = 24 f_{\text{ref}}$ at 1.92 GHz, the output phase noise is expected to increase by about $20 \log 24 = 28\,\text{dB}$. The remaining approximately 10 dB increase could be due to the difference in duty cycle of the input signals. The output phase noise at 1.88 GHz ($r = 1/23.5$) was 4 dB higher than that at 1.92 GHz ($r = 1/24$). This is presumably due to less perfect symmetry present in the half-integer condition. When the VCO was operating under the optimal bias condition, the output phase noise at 1.88 GHz was up to 31 dB as low as the free-running case, and the 1-MHz-offset phase noise was $-122\,\text{dBc/Hz}$. The corresponding frequency spectrum is shown in Fig. 8.

Fig. 9 shows the output phase-noise characteristics at $f_{\text{o}} = 1.5\,\text{GHz}$ when the input frequencies were $f_{\text{ref}} = f_{\text{o}}/3 = 0.5\,\text{GHz}$ and $f_{\text{o}}/1.5 = 1.0\,\text{GHz}$. At low offset frequencies, the noise in the reference signal multiplied by $r^{-1} = f_{\text{o}}/f_{\text{ref}}$

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF CLOCK MULTIPLIERS.

Reference	Technology	f_o [GHz]	f_o/f_{ref}	Phase noise [dBc/Hz]	Offset [MHz]	Area [mm^2]	Power [mW]	Method
This work	0.18 μm	1.92	24	**−126**	1	0.031*	55**	Injection locking
		1.88	23.5	**−122**	1			
[5]	90 nm	2.0	23	−120	0.2	0.008	13	Phase alignment†
[10]	0.18 μm	2.0	10	−108	1	0.0001	0.2	Injection locking
[11]	0.13 μm	2.0	8	−125	0.6	0.07	23	PLL
[12]	0.13 μm	1.6	32	−118	1	0.06**	5.1***	MDLL‡
[13]	90 nm	0.8	8	−124	2	0.048	15	PLL + MDLL
[14]	0.35 μm	0.9	9	−127	0.33	1.2	130	MDLL

* Core only. ** Includes current in the LDO. *** Core only. **** Multi-chip solution with externals. † Based on injection locking. ‡ Multiplying DLL.

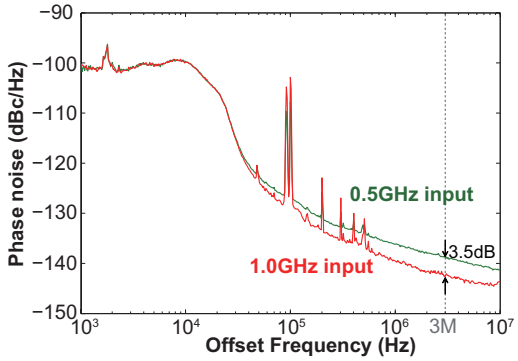

Fig. 9. Measured output phase noise characteristics at $f_o = 1.5$ GHz when $f_{ref} = 0.5$ GHz and $f_{ref} = 1.0$ GHz.

dominates the output phase noise [4]. The difference in phase noise in the 0.5 GHz and 1.0 GHz reference signals is canceled at the output by the prefactor r^{-1}. As regards the noise originating from the VCO, according to a linear model [3]–[5], the cutoff frequency of $H_{HPF}(\omega)$ goes up with f_{ref}. High-offset phase noise within the loop bandwidth is expected to decrease by about 6 dB by doubling f_{ref} if only integral subharmonic locking is taking place before and after the change in f_{ref}. If half-integral subharmonic locking occurs after doubling f_{ref}, some degradation is expected, as was shown in Fig. 7. The general tendency seen in Fig. 9 is consistent with the theoretical prediction. The 1.0 GHz input successfully gave 3.5 dB lower phase noise at 3 MHz offset than the 0.5 GHz input.

Table I shows a performance summary and comparison with other CMOS ring oscillator-based clock multipliers. The proposed circuit has good phase-noise performance.

V. CONCLUSION

We proposed a method of reducing the phase noise of injection-locked VCOs without affecting the output frequency step by utilizing half-integral subharmonic locking. For a VCO output frequency of f_o, the phase noise of the output signal locked to a half-integral subharmonic $f_{ref} = f_o/(n + 1/2)$ $(n = 1, 2, \cdots)$ is expected to be lower than that locked to an integral subharmonic $f'_{ref} = f_o/(2n+1)$ because $f_{ref} = 2f'_{ref}$. A differential ring-VCO can be designed to lock to half-integral subharmonics by giving it necessary symmetry properties. We experimentally verified half-integral subharmonic locking and the phase noise reduction in a differential ring-VCO fabricated with a 0.18 μm CMOS process. The use of half-integral or, more generally, nonintegral subharmonic injection locking could make a powerful means of realizing low-phase-noise high-resolution ring-VCOs.

ACKNOWLEDGMENTS

This work was partially supported by STARC, KAKENHI, MIC.SCOPE, NEDO, and VDEC in collaboration with Cadence Design Systems, Inc., Agilent Technologies Japan, Ltd., and Mentor Graphics, Inc.

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