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Design of CMOS inverter-based output buffers adapting the Cherry-Hooper broadbanding technique

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***Abstract*—A methodology for designing CMOS inverter-based output buffers considering speed, gain, jitter, and drivability requirements is presented. In this methodology, the band-broadening technique of the classic Cherry-Hooper amplifier is adapted for CMOS inverters. A buffer designed in this manner offers higher speed than a commonly used simple chain of inverters with exponentially increasing gate widths. The buffer is implemented by making minor modifications to a 4-stage CMOS inverter chain. The proposed design is suitable for output buffers for high-speed CMOS logic circuits.**

I. Introduction

The output data of a digital integrated circuit is sent off a chip through output buffers. Output buffers are required to drive large capacitive loads or low-resistance loads, typically $50\,\Omega$. Since measurement results are invariably affected by the performance of output buffers, they often have to outperform logic gates used in internal function blocks in terms of speed. Their failure to operate properly could mean a failed chip regardless of whether the internal function blocks are operating correctly.

It is often a serious challenge to design output buffers that can meet speed, gain, low jitter, and drivability requirements. The design of a buffer consisting of a chain of CMOS inverters with exponentially increasing gate widths is well known and well established [1]–[3]. This so-called "exponential horn [1]" is meant to drive a large capacitive load with minimal propagation delay. However, the total bandwidth of a cascade of two or more amplifier stages is narrower than that of a constituent stage [4], [5]. An exponential horn, having a very high gain, therefore has a rather limited bandwidth and is not ideal for high-speed buffering. The high gain also gives rise to increased jitter.

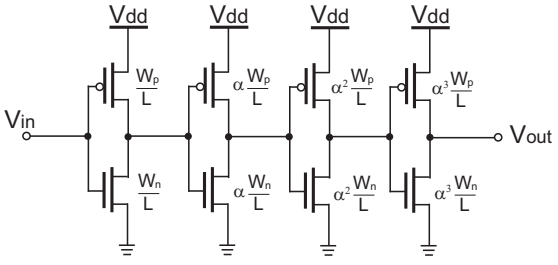

Fig. 1. Chain of inverters with exponentially increasing size. So-called exponential horn.

In this paper, we propose a methodology for designing CMOS inverter-based high-speed output buffers that drive a $50\,\Omega$ load. The high speed is achieved by adapting the band broadening technique of the classic Cherry-Hooper amplifier [4], [6] for CMOS inverters. The buffer is implemented by making minor modifications to a 4-stage exponential horn.

The use of CMOS inverters as buffers is known to be suboptimal in various respects including speed [1], and the proposed design shares many of the drawbacks with the ordinary CMOS design. The proposed design is not intended to replace any existing ultrahigh-speed designs such as those based on differential amplifiers [1]. Our aim is to provide a reasonably straightforward design methodology for output buffers for high-speed CMOS logic circuits.

The rest of this paper is organized as follows. In Section II, the Cherry-Hooper band broadening technique is explained. Section III suggests a simple procedure for determining circuit parameters for the buffer. Section IV compares the performance of the proposed CMOS inverter-based buffer with the conventional one by simulation. Finally, Section V concludes this paper.

In the simulation results presented in this paper, model parameters for a $0.18\,\mu$m Si CMOS process are used. All gate lengths are $0.18\,\mu$m. The standard power supply voltage is $V_{\rm dd} = 1.8\,$V.

II. Cherry-Hooper broadbanding technique for CMOS inverters

An NMOS implementation of the Cherry-Hooper amplifier [4], [6] with a resistive load is shown in Fig. 2(a). The feedback resistor $R_{\rm f}$ raises the pole frequencies and enables high-speed operation. Let us look at the input impedance $Z_{\rm x}$ of the second stage. It is given by

$$Z_{\rm x} = \frac{R_{\rm f} + (r_{\rm o2} \parallel R_{\rm L})}{1 + g_{\rm m2}(r_{\rm o2} \parallel R_{\rm L})} \simeq g_{\rm m2}^{-1}, \tag{1}$$

where $r_{\rm o2}$ and $g_{\rm m2}$ are the differential on resistance and the transconductance of M2, respectively. The assumption behind the approximation in (1) is $R_{\rm f} \ll (r_{\rm o2} \parallel R_{\rm L})$. Since our goal is to design high-speed buffers and a relatively small $R_{\rm f}$ will be required for accomplishing that, the assumption should be valid. The small input resistance of (1) reduces the Miller effect [7] at the first stage. The effective input capacitance

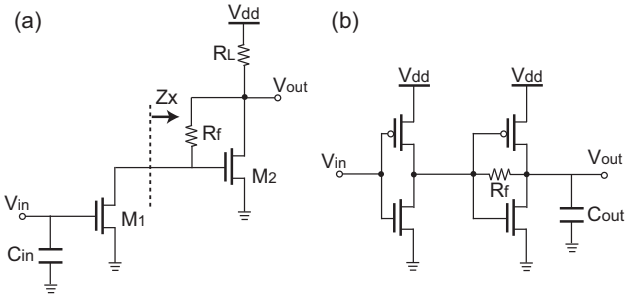

Fig. 2. (a) An NMOS version of the Cherry-Hooper amplifier. (b) Proposed CMOS version of the Cherry-Hooper amplifier.

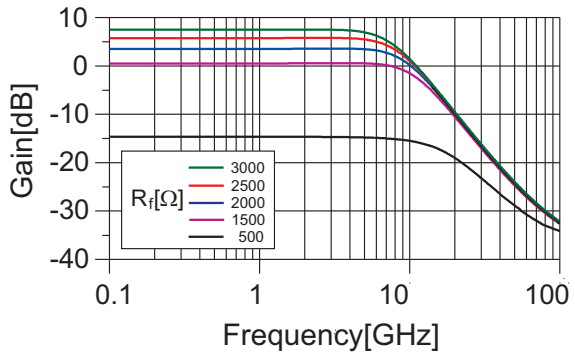

Fig. 3. The dependence of the voltage gain $|G_{21}|$ of a CMOS Cherry-Hooper stage (Fig. 2(b)) on $R_{\rm f}$.

$C_{\rm in}$ including the Miller capacitance is

$$C_{\rm in} = C_{\rm gs1} + C_{\rm gd1}(1 + g_{\rm m1}Z_{\rm x}), \tag{2}$$

and the input pole is higher than that in an ordinary cascade of common-source stages. The small $Z_{\rm x}$ also makes the pole frequency associated with the middle node high. Likewise, the presence of $R_{\rm f}$ decreases the output impedance of the second stage and increases the output pole frequency. The dc voltage gain A_0 of the Cherry-Hooper amplifier (Fig. 2(a)) is given by

$$A_0 = \frac{V_{\rm out}}{V_{\rm in}} \simeq g_{\rm m1}R_{\rm f} - \frac{g_{\rm m1}}{g_{\rm m2}}. \tag{3}$$

As is implied by (1)–(3), the cutoff frequency of the Cherry-Hooper amplifier does not depend significantly on $R_{\rm f}$.

A similar band-broadening can be attained by introducing a feedback resistor to the second stage of a cascade of two CMOS inverters, as shown in Fig. 2(b). We will hereafter refer to this CMOS inverter-based broadband amplifier as the CMOS Cherry-Hooper amplifier. The dependence of its voltage gain $|G_{21}|$ [5] on $R_{\rm f}$ is shown in Fig. 3.

Fig. 4 shows a schematic of the proposed on-chip output buffer. It consists of two CMOS Cherry-Hooper stages. It can be seen as a four-stage exponential horn (Fig. 1) with feedback resistors. In the next section we suggest a procedure for determining the parameter values.

III. A DESIGN PROCEDURE

A reasonable set of values of $W_{\rm p}/W_{\rm n}$, α, $R_{\rm f1}$, and $R_{\rm f2}$ can be determined through the following procedure.

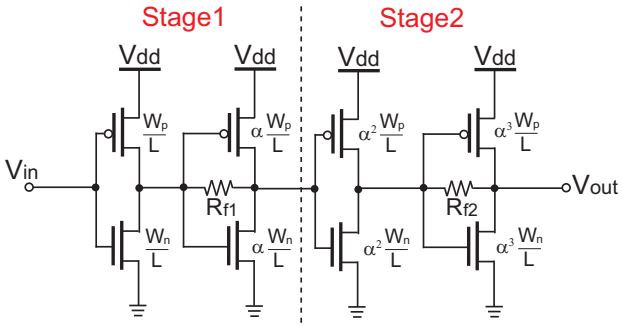

Fig. 4. Schematic of the proposed CMOS inverter-based output buffer.

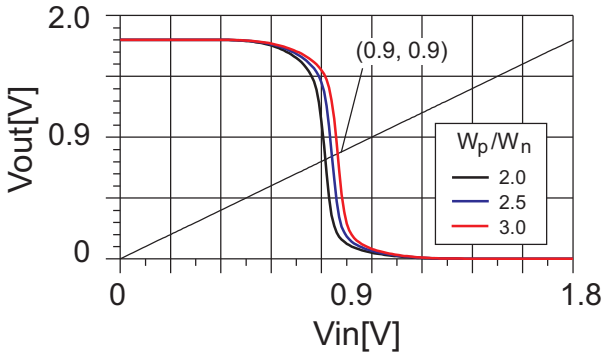

Fig. 5. DC voltage transfer curves of CMOS inverter with different values of $W_{\rm p}/W_{\rm n}$.

A. Choose $W_{\rm p}/W_{\rm n}$ ratio

First, determine the ratio of the PMOS gate width to the NMOS gate width. Fig. 5 shows the voltage transfer curves of the CMOS inverter with different values of $W_{\rm p}/W_{\rm n}$. In order to reduce jitter, a $W_{\rm p}/W_{\rm n}$ value that brings the inverter switching threshold close to $V_{\rm dd}/2 = 0.9\,{\rm V}$ should be chosen. However, a very large value leads to a large input capacitance and hinders high-speed operation. Shortest propagation delay is expected to result from $1.5 < W_{\rm p}/W_{\rm n} < 2$ [3]. In this paper, $W_{\rm p}/W_{\rm n} = 3$ was chosen in favor of jitter reduction.

B. Determine gate widths and scaling factor α

The rightmost inverter in Fig. 4 has to be able to drive a $50\,\Omega$ load and produce a certain voltage swing $V_{\rm p-p}$. The peak current flowing through the load can be written as $i_{\rm d} = V_{\rm p-p}/50$. If, for instance, the desired logic swing is $V_{\rm p-p} = 500\,{\rm mV}$, $i_{\rm d} = 10\,{\rm mA}$ is required. An appropriate NMOS gate width $\alpha^3 W_{\rm n}$ (Fig. 6) can then be found from transient simulation. The PMOS gate width $\alpha^3 W_{\rm p}$ can subsequently be determined using the $W_{\rm p}/W_{\rm n}$ ratio chosen in Section III-A.

When simulating the rightmost inverter for the purpose of determining the NMOS width, the effect of the feedback resistor $R_{\rm f2}$ should be relatively small. However, $R_{\rm f2}$ could be included if desired. In that case, an initial estimate of $R_{\rm f2}$ has to be made at this stage. On the one hand, since we are trying to build a high-speed buffer, the final value of $R_{\rm f2}$ would not be orders of magnitude larger than $50\,\Omega$. On the other hand,

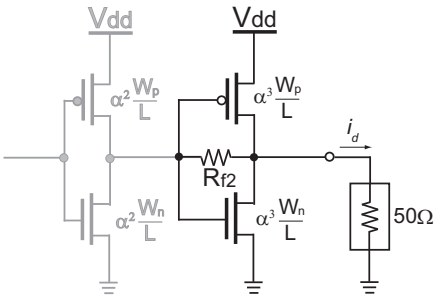

Fig. 6. The rightmost inverter that drives a 50 Ω load.

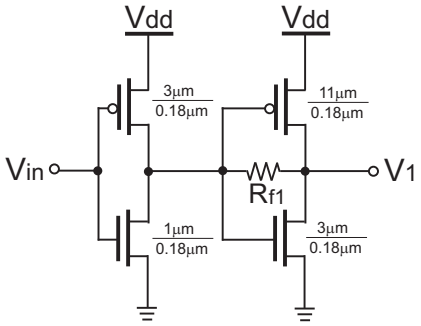

Fig. 7. Schematic of the first CMOS Cherry-Hooper stage.

since a gain that gives the desired output swing is required, the value of R_{f2} is likely to be larger than 50 Ω. In this paper, we used $R_{f2} = 100\,\Omega$ as an initial estimate. In any case, the initial choice of R_{f2} has only a minor impact on i_d and $\alpha^3 W_n$.

The NMOS width W_n of the leftmost inverter is determined from the drivability of the logic gate preceding the inverter. For example, W_n might be twice as large as the NMOS width (e.g. 0.5 μm) of the minimum-sized standard inverter cell.

Once the widths of the leftmost and rightmost inverters are determined, one can calculate the scaling factor α.

C. Determine feedback resistances R_{f1} and R_{f2}

Let us first look at R_{f1}. Fig. 7 shows a schematic of the first CMOS Cherry-Hooper stage. All parameters other than the feedback resistance R_{f1} have already been given. the bode plots of the voltage gain G_{21} [5] are shown in Fig. 8. The hybrid parameter G_{21} is used here rather than the scattering parameter S_{21} because the input impedance of the following CMOS Cherry-Hooper stage is high. The first CMOS Cherry-Hooper stage should provide a moderate voltage gain for signal swing recovery. On the other hand, excessive gain would cause jitter and limit the bandwidth. In this example, we chose an R_{f1} value that gave a dc gain of 6 dB.

We are finally in a position to revisit R_{f2}, which we temporarily set to 100 Ω earlier. First, put in all the parameter values determined so far and perform transient simulations. Check the output signal swing and adjust the value of R_{f2} so that the desired signal swing of $V_{p-p} = 500$ mV is achieved. Finally, one could check the cutoff frequency and group delay characteristics through S-parameter simulation. The use of S_{21}

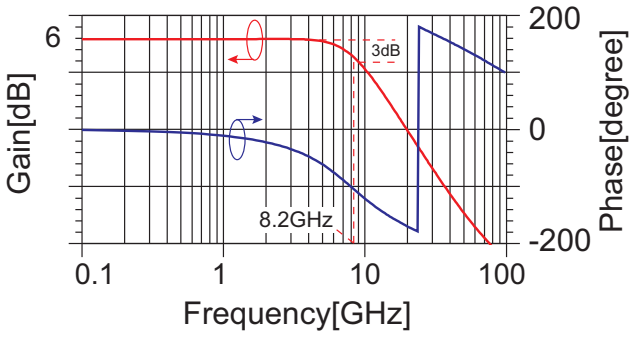

Fig. 8. Bode plots G_{21}.

TABLE I
VALUES OF α, R_{f1}, AND R_{f2} DETERMINED FROM THE VALUES OF THE INPUT PARAMETERS L, W_p, W_n BY FOLLOWING THE PROCEDURE DESCRIBED IN SECTION III.

L	W_n	W_p	α	R_{f1}	R_{f2}
0.18 μm	1 μm	3 μm	3.68	2.4 kΩ	110 Ω

is suggested here because the load impedance is supposed to be 50 Ω.

The values of parameters W_p, α, R_{f1}, and R_{f2} thus determined are given in Table I.

IV. COMPARISON WITH CONVENTIONAL BUFFER

In this section, we compare the performance of the proposed buffer (Fig. 4) with that without the feedback resistors (Fig. 1) for a few scenarios. Table II summarizes the parameter values.

A. $W_n = 1\,\mu$m, $V_{dd} = 1.8$ V

Eye diagrams for $W_n = 1\,\mu$m at 7 Gb/s are shown in Fig. 9(a) and Fig. 9(b). Both buffers are functioning but the proposed buffer exhibits less jitter. This is because the proposed buffer has a much lower gain and broader bandwidth as shown in Fig. 10. The group delay characteristics shown in Fig. 11 are also consistent with the time domain results. Fig. 9(c) and Fig. 9(d) are eye diagrams at 8 Gb/s.

B. $W_n = 2\,\mu$m, $V_{dd} = 1.8$ V

Fig. 12 shows eye diagrams at 8 Gb/s for a wider input gate width of $W_n = 2\,\mu$m. Again, the proposed buffer shows superior performance even if the gate width is changed.

C. $W_n = 1\,\mu$m, $V_{dd} = 1.2$ V

In this scenario, the input NMOS width is $W_n = 1\,\mu$m as in the first scenario, but the power supply voltage is lowered

TABLE II
VALUES OF PARAMETERS IN EACH SCENARIO.

Scenario	A	B	C
V_{dd} [V]	1.8	1.8	1.2
W_n [μm]	1	2	1
α	3.7	1.9	5
R_{f1} [kΩ]	2.4	1.3	6.8
R_{f2} [Ω]	110	80	100

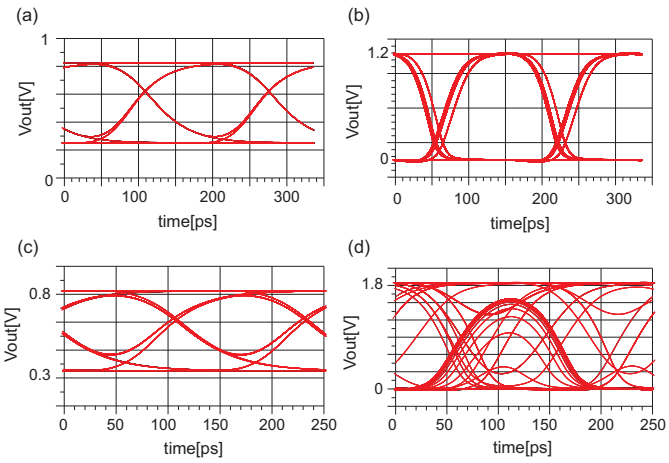

Fig. 9. Eye diagrams at 7 Gb/s [(a) and (b)] and 8 Gb/s [(c) and (d)]. $W_{\rm n} = 1\,\mu$m and $V_{\rm dd} = 1.8$ V. (a) and (c) are results from the proposed buffer. (b) and (d) are results from the conventional buffer.

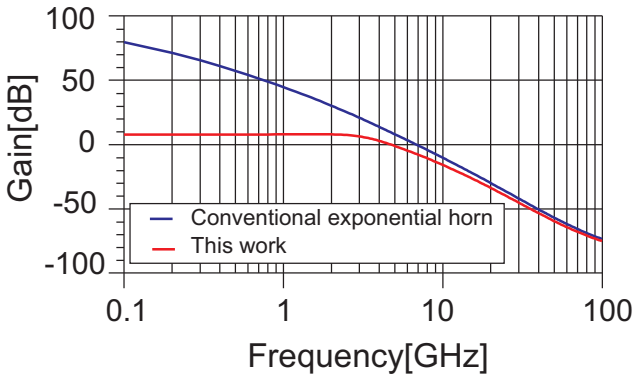

Fig. 10. Magnitudes of $|S_{21}|$ of the buffers.

to $V_{\rm dd} = 1.2$ V. Given the current trend of supply voltage reduction and the demand for low power, it is important that good output buffers can be designed for low-voltage operation too. The eye diagrams at 1.5 Gb/s, shown in Fig. 13, suggests that the proposed buffer is also promising for low voltage use.

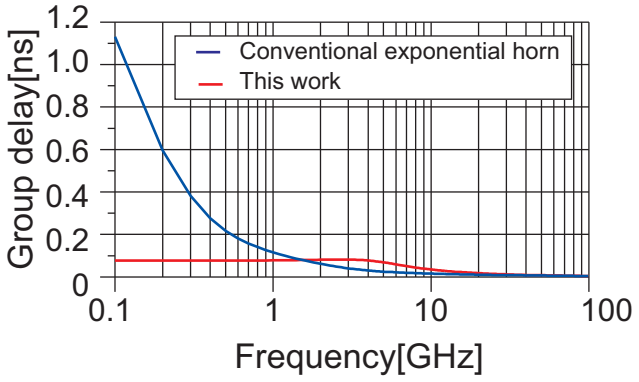

Fig. 11. S_{21} group delay characteristics. The proposed buffer shows a wide distortion-free region.

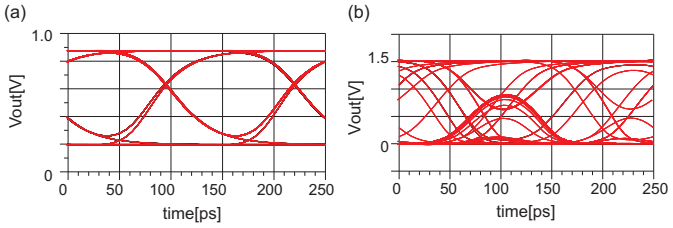

Fig. 12. Eye diagrams at 8 G/s when $W_{\rm n} = 2\,\mu$m and $V_{\rm dd} = 1.8$ V. (a) Proposed buffer. (b) Conventional buffer.

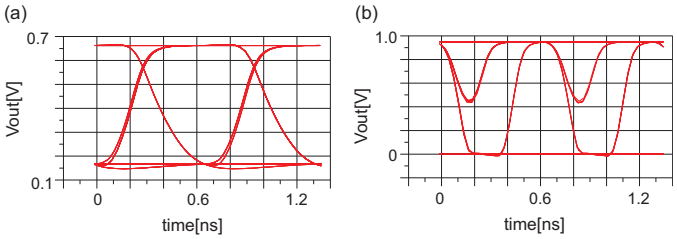

Fig. 13. Eye diagrams at 1.5 Gb/s when $W_{\rm n} = 1\,\mu$m and $V_{\rm dd} = 1.2$ V. (a) Proposed buffer. (b) Conventional buffer.

V. Conclusion

In this paper, we proposed a methodology for designing CMOS inverter-based high-speed output buffers considering speed, gain, low jitter, and drivability requirements. The speed is achieved by adopting the Cherry-Hooper broadbanding technique. The proposed buffer consists of two CMOS Cherry-Hooper stages. We also proposed a simple procedure for determining key circuit parameters. The validity of the procedure was confirmed in different scenarios by simulation. The proposed buffer is expected to offer higher speed than a commonly used chain of inverters with exponentially increasing size.

Acknowledgment

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