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A 20 Gb/s 1:4 DEMUX with Near-Rail-to-Rail Logic Swing in 90 nm CMOS process

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***Abstract* — A 9.5 mW 20 Gb/s 40×70 μm^2 inductorless 1:4 DEMUX in 90 nm CMOS process is presented. In order to reduce power and area, the DEMUX uses a multi-phase clock architecture that requires a smaller number of latches operating at a slower clock rate than in the conventional tree architecture. To provide low-voltage scalability, the latches operate with a near-tail-to-rail logic swing. It is realized without significant speed penalty by adopting current-sourceless CML-type latches with unconventional settings. It offers a larger noise margin and elimination of logic level converters too. The well-balanced scalable design could possibly broaden the applications of high-speed SerDes in the coming ultralow-voltage many-core era.**

***Index Terms* — DEMUX, CMOS, multi-phase clock architecture, near-rail-to-rail logic swing**

I. Introduction

Applications of high-performance demultiplexers (DEMUXes) [1]–[6] have so far been limited chiefly to those that accept a design trade-off in favor of speed, such as fiber-optic communication systems. In typical optical wavelength-division multiplexing (WDM) systems, for example, per-wavelength speed of 10 Gb/s or faster is required. The conventional wisdom in gaining or maintaining speed of CML-type circuits, used in [1]–[6], has been to reduce the signal amplitude. A dilemma here is that the noise immunity might have to be traded off. Another problem is that current-mode logic (CML)-type circuits do not go well with the trend of lowering the supply voltage. As regards other factors than the speed, since as many DEMUXes as the wavelength multiplicity are needed in WDM systems, the power and area are also important considerations. We present a 1:4 DEMUX with near-rail-to-rail architecture that could offer a possible solution to the challenges in signal integrity and low-voltage scalability as well as in balancing the speed, power, and area.

II. Architecture

Fig. 1 shows the architecture of the 1:4 DEMUX along with a timing chart. This multi-phase clock architecture was chosen in favor of power and area reductions. The half-rate clock $\mathrm{CLK_{in}}$ is halved in frequency by the divider consisting of 2 latches. Its outputs are quadrature-phase-shifted and are fed into the two 1:2 DEMUXes. In the upper 1:2 DEMUX, a pair of master-slave latches (MSLs) samples every other bit in the input bitstream $\mathrm{D_{in}}$ by using rising and falling edges of the quarter-rate clock signal $\mathrm{CLK_2}$. The latch $\mathrm{L_{d1}}$ aligns the outputs from the pair of MSLs. The lower 1:2 DEMUX operates likewise. The two 1:2 DEMUXes sample the input bitstream alternately as dictated by the phase-shifted clock signals $\mathrm{CLK_1}$ and $\mathrm{CLK_2}$ and perform the 1:4 DEMUX function. The latches $\mathrm{L_{d0}}$ and $\mathrm{L_{d2}}$ align the outputs from the lower 1:2 DEMUX with those from the upper one. The 1:4 DEMUX uses 12 latches altogether, as opposed to 15 in the conventional tree architecture [3], [4], which uses three 1:2 DEMUXes operating at a half rate. The quarter-rate operation of the 1:2 DEMUXes in our design leads to low power dissipation. This design is similar to the 12-latch 1:4 DEMUX proposed in [6]. It thus allows more than 20 % power and area reductions in comparison with the 15-latch DEMUX. The selector circuit in Fig. 1 is for performing measurement with a small number of pads. It is a simple combinational logic circuit consisting of transmission gates and NOR gates.

III. Circuit Design

Fig. 2 shows circuit schematics of three different CML-type latches. The CML has conventionally been the architecture of choice for high-speed digital circuits. However, in 90 nm CMOS, the power supply voltage is limited to about 1.2 V and the threshold voltage is about 0.3 V. Each transistor, therefore, cannot enjoy sufficiently high voltage across its drain and source required for high-speed operation. Switching noise degrades the output eye opening as shown in Fig. 2(a). The current-sourceless CML structure was recently proposed for low-voltage operation [4], [7]. The tail transistor is eliminated to give increased voltage headroom. The size of the upper transistors is determined so that the gain of the differential amplifier is as low as 1 dB to 2 dB for high speed latching. The simulated eye diagram (Fig. 2(b)) shows a wider opening than that of the conventional CML (Fig. 2(a)). The signal swing is limited

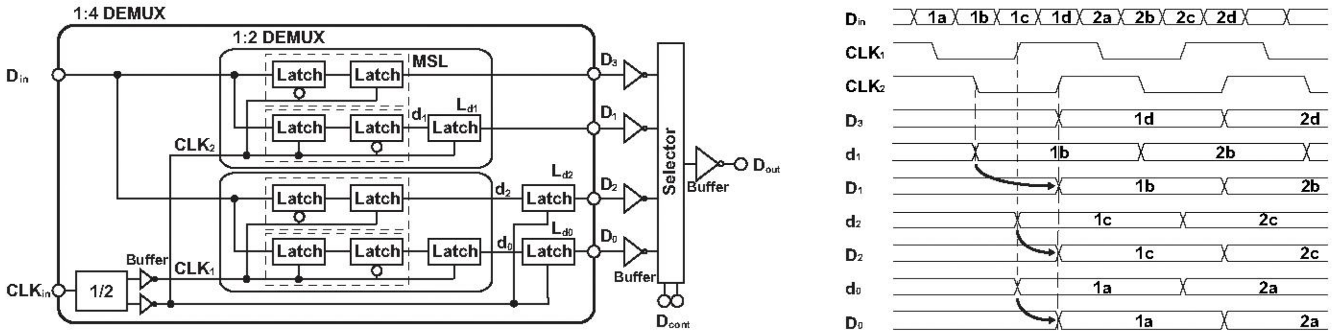

Fig. 1. 1:4 DEMUX with multi-phase clock architecture and timing chart. Circuit core is enclosed in large rounded rectangle.

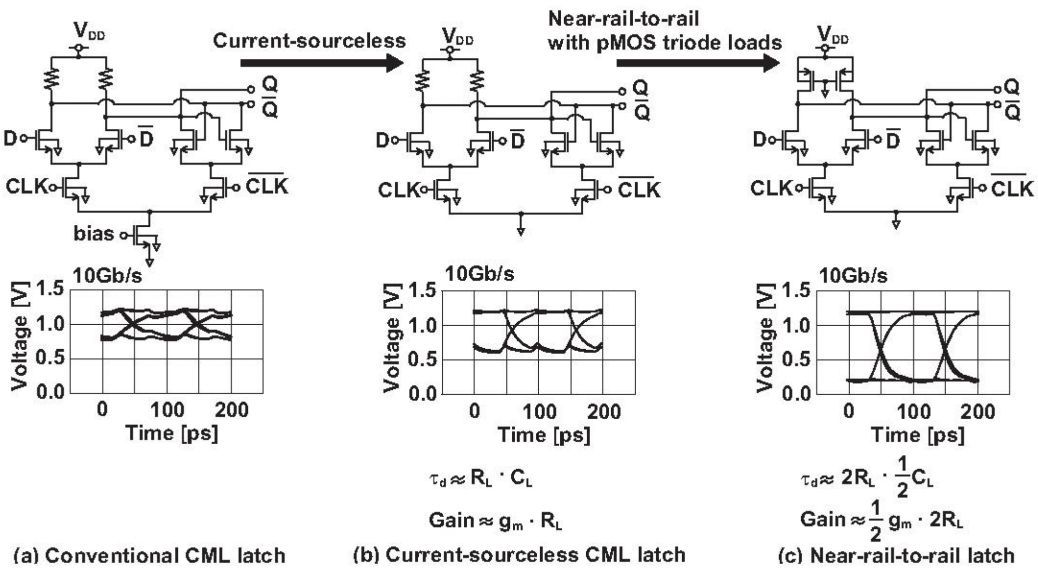

Fig. 2. Circuit schematics of latches with CML-type topology and simulated eye diagrams.

to up to 0.6 V, yet the clock has to have a rail-to-rail voltage swing.

In our design, in order to give a larger noise margin and better scalability in light of the ever-lowering supply voltage, near-rail-to-rail architecture is introduced making use of the current-sourceless CML-type topology [4]. To achieve the transition from the 0.6 V swing [4] to a near-1.2 V swing, the resistance R_L of the loads has to be roughly doubled, but the speed might drop as a consequence. However, since the gain goes up with R_L, the transistors can actually be made smaller to keep the gain low. Then, the parasitic capacitance C_L associated with the transistors, including those being driven at the next stage, also becomes smaller, and therefore the cut-off frequency remains high. The signal amplitude thus becomes nearly rail-to-rail without imposing significant speed penalty. It is not quite rail-to-rail because of the small voltage drop across the transistors. In order to make the voltage drop small, the clocked transistors should be enlarged somewhat. Circuit blocks built with the near-rail-to-rail architecture can be freely intermixed with CMOS digital blocks without logic level conversion. In Fig. 1, the divider, the 1:2 DEMUXes, and the latches L_{d0} and L_{d2} are near-rail-to-rail, and the rest are built of CMOS logic gates and transmission gates.

Fig. 3(a) schematically shows the layout of the current-sourceless CML latch in Fig. 2(b). The polysilicon load resistors cover a significant area. To reduce the area, PMOS loads operating in the triode (or linear) region are adopted as was done in [1], as shown in Figs. 2(c) and 3(b). This is a technique used in the pseudo-NMOS logic [8]. The area of the latch is estimated to become about a third of the current-sourceless CML architecture's, as illustrated in Fig. 3. The use of the PMOS triode loads instead of polysilicon resistors has no adverse effect on the signal integrity when the signal amplitude is near-rail-to-rail. A micrograph of the test chip is shown in Fig. 4. The circuit core area is $40 \times 70\,\mu m^2$.

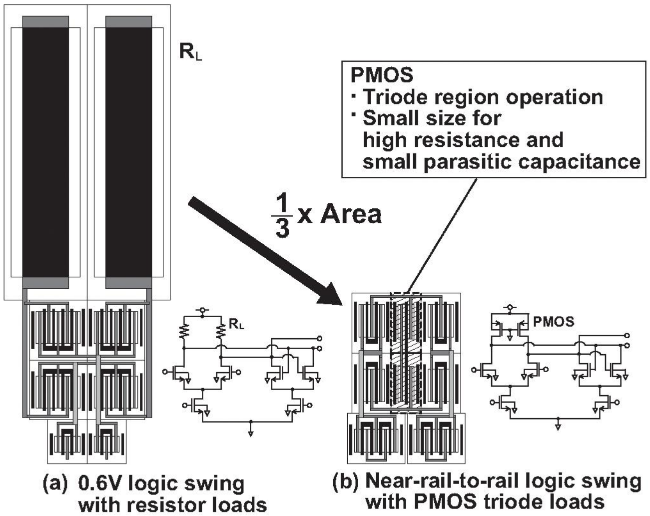

Fig. 3. Area reduction with the use of PMOS loads.

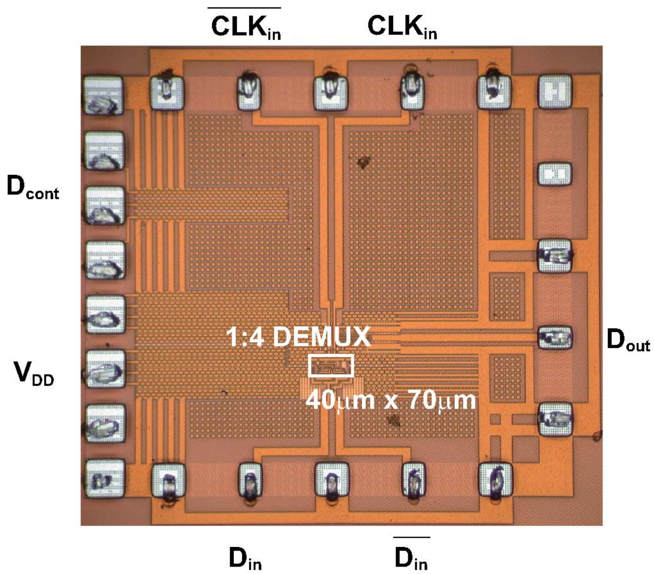

Fig. 4. Micrograph of 1:4 DEMUX.

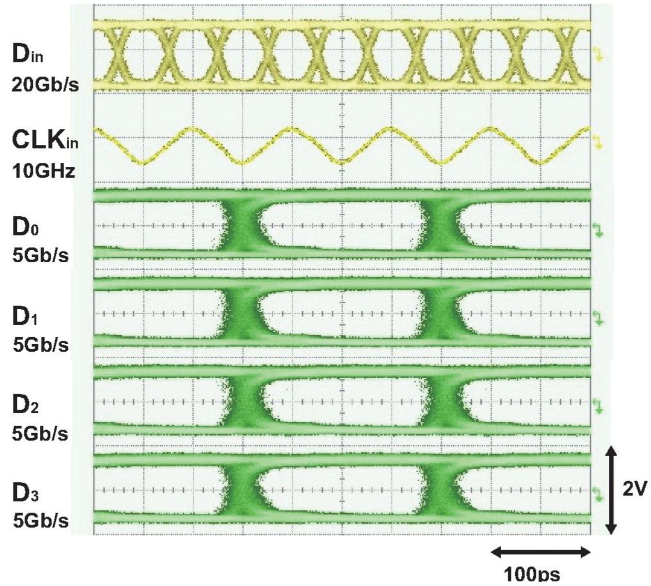

Fig. 5. Measured eye diagrams of 1:4 DEMUX.

IV. Measurement Results

Fig. 5 shows measured output eye diagrams. The input was 20 Gb/s non-return-to-zero (NRZ) $2^{31}-1$ pseudo-random binary sequence (PRBS). A half-rate sinusoidal clock signal of 10 GHz was also supplied. Each of the four output data streams was observed using a sampling oscilloscope and an error detector by selecting a channel. Wide eye openings were observed at an error rate of less than 10^{-12}. The output jitter was 20 ps (p-p). The input data phase margin was 100 degrees for the input data mentioned. The power dissipation was 9.5 mW with the supply voltage of 1.2 V. Measurement was made also with lower supply voltages of down to 0.9 V. When the supply voltage was 0.9 V, the operation speed was 13 Gb/s and the power dissipation was 3.3 mW.

Comparisons are made in Fig. 6 of area and speed of CMOS DEMUXes [1]–[5]. Further details of the DEMUXes are given in Table I. All the earlier DEMUXes used CML-type architecture with a small logic swing. The power dissipation values of our circuit, listed in Table I, are those of the circuit core (Fig. 1). This is because a DEMUX usually is connected to digital circuits on the same chip. But [2]–[5] only showed power dissipation values including output buffers, and those values are listed in Table I. While this prevents a strict comparison of power dissipation, we believe that the multi-phase clock architecture contributed to the low power. With respect to the area, ours is well over an order of magnitude smaller than the next smallest 1:4 DEMUX [3] and is still smaller than the 1:2 DEMUX [5]. Our inductorless DEMUX offers a good balance of speed, power, and area.

V. Conclusions

In conclusion, a 9.5 mW 20 Gb/s near-rail-to-rail 1:4 DEMUX occupying the area of $40\times70\ \mu m^2$ is demonstrated in 90nm CMOS process. When the supply voltage is lowered from 1.2 V to 0.9 V, it operates at 13 Gb/s and 3.3 mW. The near-rail-to-rail architecture offers larger noise margin, better scalability with supply-voltage reduction than the existing CML-type architecture, and elimination of logic level converters for interfacing with CMOS digital blocks. The

TABLE I
SUMMARY OF HIGH-SPEED CMOS DEMUXES.

	[1]	[2]	[3]	[4]	[5]	This work	
DEMUX	1:8	1:2	1:4	1:4	1:2	1:4	
Circiut topology	feedback MOS CML	capacitive-splitting CML	coupled-latch CML	current-sourceless CML	CML	near-rail-to-rail	
Load	PMOS triode	R + L	R	R + L	R	PMOS triode	
Data rate	10 Gb/s	20 Gb/s	19 Gb/s	40 Gb/s	40 Gb/s	20 Gb/s	13 Gb/s
Power consumption	48 mW	105 mW*	210 mW*	62mW*	108 mW*	9.5 mW	3.3 mW
Supply voltage	2.0 V	2.0 V	1.2 V	1.2 V	1.5 V	1.2 V	0.9 V
Voltage swing	0.2 V	1.0 V	0.25 V	0.5 V	0.6 V	1.0 V	0.8 V
Core circiut area	300 x 420 μm^2	650 x 770 μm^2	280 x 410 μm^2	1400 x 1800 μm^2	60 x 70 μm^2	40 x 70 μm^2	
Technology	0.18 μm	0.18 μm	0.13 μm	90 nm	0.12 μm	90 nm	

*Includes output buffer

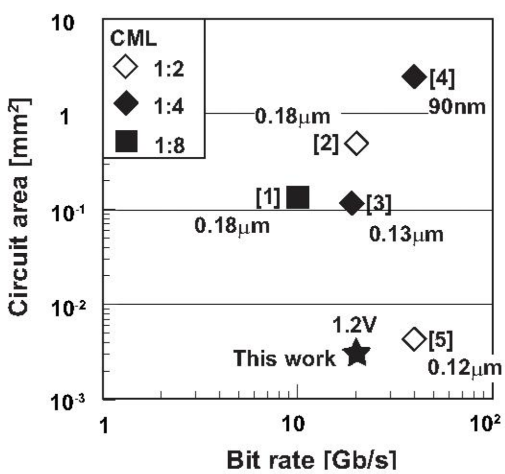

Fig. 6. Comparison of areas of high-speed CMOS DEMUXes.

small footprint, the low power, and the manifold advantages brought by the near-rail-to-rail operation could possibly broaden the applications of high-speed serializer/deserializer (SerDes) to, for example, communication between subsystems constituting a complex system in a package (SiP) or system on a chip (SoC) in the coming ultralow-voltage many-core era.

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