<table>
<thead>
<tr>
<th>項目</th>
<th>内容</th>
</tr>
</thead>
<tbody>
<tr>
<td>タイトル</td>
<td>Design of Wideband Linear Voltage-to-Current Converters</td>
</tr>
<tr>
<td>著者</td>
<td>Retdian Nicodimus, Shigetaka Takagi</td>
</tr>
<tr>
<td>発行日</td>
<td>2010, 2</td>
</tr>
<tr>
<td>URL</td>
<td><a href="http://search.ieice.org/">http://search.ieice.org/</a></td>
</tr>
<tr>
<td>権利情報</td>
<td>本著作物の著作権は電子情報通信学会に帰属します。</td>
</tr>
<tr>
<td></td>
<td>Copyright (c) 2010 Institute of Electronics, Information and Communication Engineers.</td>
</tr>
</tbody>
</table>
This paper proposes a feedback loop design method which removes the trade off between loop gain and bandwidth. The principle of voltage-to-current conversion using passive resistor and the conventional feedback configuration will be explained in Sect. 2. The proposed circuit and its design strategy will be discussed in Sect. 3. Finally, simulation results of the proposed voltage-to-current converter will be shown in Sect. 4.

2. Principle of Linear V-I Converter

An easy method of voltage-to-current conversion is use of a single transistor. However, this method does not offer good linearity which might be a critical requirement in some applications. Many ideas have been proposed in order to obtain better linearity, however, many of them still use active devices as the main part of the voltage-to-current converter. Considering again that breakdown voltage as well as power-supply voltage is getting lower while the signal voltage which is determined by standard is not getting lower at all, use of a passive device (resistor) as a voltage-to-current converter might be the only solution in a standard CMOS process.

The principle of a voltage-to-current conversion using a resistor is shown a nullator and norator model in Fig. 1. Here either one of the resistor terminals is virtually connected to ground by nullator and the current flows through the resistor will be given by

$$I_{IN} = \frac{V_{IN}}{R}.$$  (1)

It is clear that the input voltage is converted into current by a resistor. This implies a voltage-to-current conversion with high linearity. However, in practical implementations, nullator and norator are implemented using active devices. As a result, there will be a non-zero impedance $Z_{IN}$, which represents the input impedance of the circuit and is con-

![Fig. 1 Nullator-norator model of ideal V-I converter.](image)

Manuscript received June 18, 2009.
Manuscript revised August 31, 2009.

†The author is with the Global Edge Institute, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.

††The author is with the Department of Communications and Integrated Systems, Graduate School of Science and Engineering, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.

a) E-mail: nico@ec.ss.titech.ac.jp

DOI: 10.1587/transfun.E93.A.382

Copyright © 2010 The Institute of Electronics, Information and Communication Engineers
Input current $I_{IN}$ is not only determined by $R$, but also another element, $Z_{IN}$. Here, $Z_{IN}$ has non-linearities since the impedance is a property of active devices. Those non-linearities will appear as the non-linearities in the voltage-to-current conversion. For an arbitrary value of $R$, the larger $Z_{IN}$ is, the worse the linearity will be. A simple example of conventional voltage-to-current converter implementation is shown in Fig. 3. The input impedance seen from node $a$, $Z_a$, is approximately

$$Z_a \approx \frac{1}{g_m},$$

where $g_m$ is the transconductance of a MOS transistor.

In order to reduce the non-linearities, the voltage-to-current converter circuit should be designed to have an input impedance as small as possible. One of the conventional ways to reduce the impedance of an arbitrary node is by applying a feedback loop to the node as shown in Fig. 4. Here $Z_a$ is the impedance seen from node $a$ without any feedback. When a feedback is applied, assuming that the DC-gain of the operational amplifier is $A$, then the impedance at node $a$ will be reduced to

$$Z'_a = \frac{Z_a}{1 + A}.$$ 

If the operational amplifier has a 1st-order frequency characteristic, such that

$$A(s) = \frac{A_0}{1 + s/\omega}$$

where $A_0$ and $\omega$ are the DC-gain and the cutoff angular frequency of the operational amplifier respectively, then

$$Z'_a(s) = \frac{Z_a(\omega + s)}{(1 + A_0)\omega + s}.$$ 

Here the frequency response of $Z'_a(s)$ has a pole at $(1 + A_0)\omega$ and a zero at $\omega$ as shown in Fig. 5. Another gain stage can be added to further reduce the impedance as shown in Fig. 6. In this case the impedance of node $a$ is given by

$$Z'_a = \frac{Z_a}{1 + A_1 A_2}.$$ 

Again, assume that both amplifiers $A_1$ and $A_2$ have a 1st-order frequency characteristic, the total gain of a two-stage operational amplifier (by $A_1$ and $A_2$), $G_C(s)$ is given by

$$G_C(s) = \frac{A_{01}}{1 + s/\omega_1} \cdot \frac{A_{02}}{1 + s/\omega_2}$$

where $A_{01}, A_{02}, \omega_1$ and $\omega_2$ are the DC-gains and the cutoff angular frequencies of the first and second amplifiers respectively. Assume that the frequency characteristics of $A_1(s)$ and $A_2(s)$ are given by the curves in Fig. 7. The loop gain $G_C(s)$ should have enough phase margin to guarantee the stability of the loop. In order to obtain a minimum phase margin of 45 degrees, the second pole of $G_C(s)$ should be at least equal to its unity gain frequency. From Fig. 7, since $\omega_1$ will be the dominant pole while $\omega_2$ will be the second pole, the condition can be derived by solving $|G_C(j\omega)| = 1$ for $\omega = \omega_2$, which gives
\[
\omega_1 = \sqrt{\frac{2}{A_{01}^2 A_{02}^2 - 2}} \times \omega_2. \tag{9}
\]
Assume that \(A_{01} A_{02} \gg 2\), then
\[
\omega_1 \approx \frac{\sqrt{2}}{A_{01} A_{02}} \times \omega_2. \tag{10}
\]
Since the gain-bandwidth product of \(G_C(s)\), \(GB_C\) is given by
\[
GB_C = A_{01} A_{02} \omega_1, \tag{11}
\]
substituting Eq. (10) into (11) gives
\[
GB_C \approx \sqrt{2} \omega_2 = \frac{\sqrt{2}}{A_{02}} GB_2, \tag{12}
\]
where \(GB_2 = A_{02} \omega_2\) is the gain-bandwidth product of the second stage. If \(GB_2\) is the affordable maximum gain-bandwidth product (\(GB_{\text{max}}\)), then the gain-bandwidth product of the two-stage operational amplifier by cascading \(A_2\) will be smaller than \(GB_{\text{max}}\) by a factor of \(\sqrt{2}/A_{02}\) (see Fig. 8). Furthermore, in practical cases, the second pole is set to \(2 \omega_0\) (\(\omega_0\): unity gain frequency) or higher frequencies to avoid peaking in the frequency response. As a result,
\[
GB_C \leq \frac{GB_2}{2 A_{02}} \tag{14}
\]

\[
\omega_1 = \sqrt{\frac{2}{A_{01}^2 A_{02}^2 - 2}} \times \omega_2. \tag{9}
\]

3. Proposed Circuit

The proposed method of lowering an impedance without having a penalty on the bandwidth is shown in Fig. 9. In the proposed configuration, each stages have a direct feedback loop (nested-feedback loop). Here, the impedance seen from node \(a\) will be found as
\[
Z'_a = \frac{Z_a}{1 + A_2 + A_1 A_2}. \tag{15}
\]
Again, assuming that each operational amplifiers have a first order frequency response, the impedance seen from node \(a\) will be
\[
Z'_a(s) = \frac{Z_a}{1 + \frac{A_2(1 + s/\omega_1)}{1 + s/\omega_2}(1 + s/\omega_2)} \tag{18}
\]
If \(\omega_2 = (1 + A_0) \omega_1\), which is approximately the unity gain frequency of \(A_1\), then \(Z'_a(s)\) can be rewritten as
\[
Z'_a(s) = \frac{Z_a}{1 + \frac{(1 + A_0) A_{02}}{(1 + s/\omega_1)}}. \tag{19}
\]
From Eq. (19), the open loop gain \(G_p(s)\) is given by
\[
G_p(s) = \frac{(1 + A_0) A_{02}}{1 + s/\omega_1} \tag{20}
\]
which is a first order frequency response with a DC-gain of \((1 + A_0) A_{02}\) and a cutoff frequency at \(\omega_1\). The equivalent gain bandwidth product \(GB_P\) is
\[
GB_P = (1 + A_0) A_{02} \times \omega_1. \tag{21}
\]
Assuming that \(A_0 \gg 1\), the gain bandwidth product is approximately
\[
GB_P \approx A_{01} A_{02} \omega_1. \tag{22}
\]
Remember that since \( \omega_2 = (1 + A_1) \omega_1 \), then
\[
GB_p \approx A_{02} \omega_2 = GB_2. \tag{23}
\]
Compared to Eq. (14), Eq. (23) shows that there is no penalty in the bandwidth of the proposed configuration (Fig. 10).

The proposed configuration can be expanded into a general form as shown in Fig. 11. Assuming that each stages have a first order frequency characteristic, the general form of Eq. (15) can be expressed as
\[
Z'_a = \frac{Z_a}{1 + \sum_{i=1}^{n} \prod_{j=i}^{n} A_j}, \tag{24}
\]
where \( A_j \) and \( \omega_j \) are the DC gain and the cutoff angular frequency of the \( j \)-th amplifier respectively. Repeating the procedure of poles cancellation as shown in Eqs. (18) and (19), the poles for each stages are given by equations in Table 1. Here the pole of \( n \)-th stage amplifier \( \omega_n \) will be given by
\[
\omega_n = \left(1 + \sum_{i=1}^{n-1} \prod_{j=i}^{n-1} A_j \right) \omega_1 \tag{25}
\]
\[
= \omega_1 + \left(\sum_{i=1}^{n-1} \prod_{j=i}^{n-1} A_j \right) \omega_1 \tag{26}
\]
ros in the right hand side of the s-plane, the proposed configuration has a straightforward and easier compensation scheme. The loop gain of the proposed configuration, $G_P(s)$, can be found from Eq. (24) as

$$G_P(s) = \frac{N(s)}{D(s)} = \sum_{i=1}^{n} \prod_{j=i}^{n} \frac{A_j}{1 + s/\omega_j}. \quad (34)$$

This means that as long as $A_j > 0 (j = 1 \sim n)$ and the poles of each gain stages are in the left hand side of s-plane, the zeros of $G_P(s)$ will also lay on the left hand side of s-plane. As a result, all pole-zero cancellations in the proposed nested feedback configuration are stable (pole-zero cancellation of right hand side zero is unstable). A feedback loop incorporating pole-zero cancellations will be stable if and only if there is no unstable pole-zero cancellations in $G_P(s)$ and $1 + \frac{P(s)}{1 + GP(s)}$ is stable [9]. The second condition means the real part of every roots of polynomial $P(s) = N(s) + D(s)$ must be negative. From Eq. (34), $P(s)$ is given by

$$P(s) = \sum_{i=1}^{n-1} \left( \prod_{j=1}^{i} (1 + s/\omega_j) \right) \left( \prod_{k=i+1}^{n} A_k \right) \quad (35)$$

In an $n$-stage configuration with equal gain for each stages ($G_{mi}R_{Oi} = G_mR_O = \text{constant}$), the $n$-th stage will have the smallest capacitance while the largest one is the capacitance of the 1-st stage which is given by

$$C_1 = (G_mR_O)^n C_n. \quad (40)$$

For a 3-stage amplifier with a gain of 10 for each stages, $C_1$ will be as large as 1000 times of $C_n$. It is clear that this design strategy is not a practical one since the capacitances will consume a large chip area.
Table 2  Parameters of each stages.

<table>
<thead>
<tr>
<th></th>
<th>$A_1$</th>
<th>$A_2$</th>
<th>$A_3$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>39</td>
<td>32</td>
<td>25</td>
<td>dB</td>
</tr>
<tr>
<td>$f_{-3dB}$</td>
<td>0.01</td>
<td>0.69</td>
<td>21.7</td>
<td>MHz</td>
</tr>
<tr>
<td>Tail current</td>
<td>2</td>
<td>10</td>
<td>1800</td>
<td>μA</td>
</tr>
<tr>
<td>Differential pair</td>
<td>2/1.5</td>
<td>4/0.5</td>
<td>280/0.18</td>
<td>μm/μm</td>
</tr>
</tbody>
</table>

($V_{DD} = 1.8V, C_1 = 2pF, C_2 = 0.3pF$)

Equation (39) shows that the ratio between capacitances of $n$-th stage and $(n-1)$-th stage depends on the transconductance of $(n-1)$-th stage $G_{m(n-1)}$ and the output resistance of $n$-th stage $R_{On}$. It is clear that a reasonable way to reduce the gain-bandwidth product of $(n-1)$-th stage is by reducing its transconductance. In a simple single-ended amplifier with a differential pair, this can be done by simply reducing the bias current and the size of the input MOS transistors.

Figure 15 shows the proposed voltage-to-current converter which is realized using a 3-stage nested feedback amplifier, a common gate circuit and a resistor. Source follower circuits are added to the input of final stage to provide a proper bias for the differential pair of the stage. Here the values of tail currents, differential pair MOSFETs’ sizes and capacitances $C_1, C_2$ are set to meet the condition in Eq. (29).

Table 2 shows the simulated parameters for each gain stages which is designed with 0.18 μm CMOS process parameters. The total DC gain and gain-bandwidth product are approximately 96 dB and 700 MHz respectively. It is possible to improve the DC gain further, however the equations to find the circuit parameters will be different because there is a high possibility that the MOSFETs will fall into weak inversion region (referring to Table 2, the current flows in each MOSFETs will be smaller than 1 μA).

4. Simulation Results

The proposed circuit in Fig. 15 is simulated using Spectre with 0.18 μm CMOS process parameters. The other parameters are shown in Table 3. The DC characteristics of the proposed circuit is shown in Fig. 16. The characteristics of a conventional voltage-to-current converter using a common gate circuit (Fig. 3) are also shown for comparison. The transistors sizes of common gate stages in Figs. 3 and 15 have been set such that both the conventional and proposed circuits have equal total bias currents of 10.4 mA. The linearity of the proposed circuit can be confirmed from transconductance which is obtained from the derivation of output current. The proposed circuit has a constant transconductance which is equal to $1/R$, while the conventional one has a curved characteristic with fluctuation of more than 6%. The good linearity performance of the proposed circuit is due to the low input impedance by the proposed nested feedback configuration. The frequency characteristic of input impedance $Z_{in}$ is shown in Fig. 17. While the conventional circuit has an input impedance of approximately 5.4Ω, the input impedance of the proposed circuit is approximately 130μΩ at frequencies up to 10kHz. Considering that the total DC gain is 96 dB, the theoretical input impedance of the proposed circuit is 86μΩ. The difference between simulation and theoretical values are mainly caused by an attenuation at common gate stage and parasitic resistances, which are not considered in the analysis.

From Fig. 18, the bandwidth (~3 dB frequency) of the proposed circuit is found to be 350 MHz. The output current of conventional common gate circuit decreases slightly at frequency of a few MHz. This is caused by the parasitic elements in MOS transistor of the common gate circuit. In contrary, the proposed circuit compensates the effect of parasitics and extends the bandwidth. This property is not discussed in this paper but will be included in future publications.

The linearity of the voltage-to-current converter is evaluated using Total Harmonic Distortion (THD). First, the input voltage amplitude is varied from 0.5 V to 2.5 V while
than 500 kHz. On the other hand, the proposed circuit keeps the THD lower than 1% for frequencies up to 10 MHz. The THD of the proposed circuit is getting lower as the frequency decreases. Finally, the performance comparison is summarized in Table 4.

5. Conclusions

A voltage-to-current converter with a nested feedback configuration is proposed. The proposed configuration enables a design of a high loop-gain configuration without reducing the bandwidth. The proposed configuration allows the implementation of a wideband voltage-to-current converter with high linearity. Simulation results using 0.18 μm CMOS process parameters show a highly linear voltage-to-current conversion characteristic. The simulated bandwidth of the proposed circuit is 350 MHz. A THD as low as 0.1m% is achieved using a 3-stage configuration of the proposed topology. The THD improvement of the proposed circuit is more than 60 dB compared to the one of a common gate circuit under a same total current consumption of 10.4 mA.

Acknowledgment

This work is supported by MEXT’s program “Promotion of Environmental Improvement for Independence of Young Researchers” under the Special Coordination Funds for Promoting Science and Technology and by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References


Retdian Nicodimus was born in Malang, Indonesia, on March 3, 1976. He received the Bachelor of Engineering, Master of Engineering and Doctor of Engineering degrees from Tokyo Institute of Technology, in 2000, 2002 and 2005 respectively. He works as an assistant professor at the Department of Communications and Integrated Systems, Graduate School of Science and Engineering, Tokyo Institute of Technology since 2005 and joins The Global Edge Institute of the same university from the fiscal year 2009. His main interest lies in the field of analog integrated circuits. Nicodimus is a member of the Institute of Electrical and Electronics Engineers.

Shigetaka Takagi was born in Tokyo. He received the B.E., M.E., and Doctor of Engineering degrees from Tokyo Institute of Technology, in 1981, 1983, and 1986, respectively. Then he became a Research Associate of Tokyo Institute of Technology where he is now a Professor in the Department of Communications and Integrated Systems. In the fiscal year 1998 he was a visiting Associate Professor of Osaka University. His main interest lies in the field of analog integrated circuits. He received the Best Paper Awards in 1996 and 2001 from the Institute of Electronics, Information, and Communication Engineers. He is the author of “Analog MOS Electronic Circuits” and “Linear Circuit Theory,” and a co-author of “Introduction to Digital Integrated Circuits” (in Japanese). Dr. Takagi is a member of the Institute of Electrical Engineers of Japan and the Institute of Electrical and Electronics Engineers.