論文 / 著書情報
Article / Book Information

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Citation	ECS Transactions, Vol. 11, No. 6, pp. 467-472
発行日 / Pub. date	2007, 6
DOI	http://dx.doi.org/10.1149/1.2778403
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ECS Transactions, 11 (6) 467-472 (2007)
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Advantages of Nano-grating Substrates in CMOS -FET Characteristics

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The drivability enhancement of CMOSFET of both n-type and p-type was achieved by using nano-grating silicon substrate without any complex fabrication process. The transconductances of both nMOSFET and pMOSFET on nano-grating substrates were increased thanks to the increase in effective channel width, leading to the area advantage of about 64% normalized by that of a conventional substrate. The channels were formed on horizontal (100) and vertical (110) surfaces of the nano-grating. Due to the existence of the current flowing in <110> direction on (110) surface, the effective carrier mobility in nano-grating nMOSFET was lower, while that in nano-grating pMOSFET was larger than the conventional one. So the difference of drivability enhancement between nMOSFET and pMOSFET became slighter, from which the area balance of CMOS circuit fabricated on the nano-grating substrates were improved.

Introduction

CMOS downsizing has been accelerated very aggressively in these years. Even though MOSFETs are downscaled, total performance of the integrated circuits is not guaranteed to be improved because of the short channel effects (SCE). So the new technologies such as mobility enhancement by strained silicon channel, three-dimensional structure are introduced to surpass SCE and improve the performance of the transistors (1-6). And utilizing the advantage of carrier mobility dependence on surface orientation, high performance CMOS devices fabricated on hybrid substrates with different crystal orientations, nFETs on silicon of (100) surface orientation and pFETs on (110) surface orientation were reported (7). However, these technologies need a special substrate or complex process, resulting in some problem about integration with conventional process and the problem of cost. The MOSFETs fabricated on the nano-grating substrate were reported to enhance current drivability (8-9).

In this paper, the advantages of the nano-grating silicon substrates for CMOS-FET characteristics are reported.

Process Flow and Device Fabrication

The process started with a conventional p-type (100) Si wafer. Firstly, boron atoms and arsenic atoms were implanted to the channel region of nMOSFETs and pMOSFETs, repectively. The lines and spaces with the pitch of 140 nm were patterned using EB direct lithography technology. To reduce the damage to the channel area, dry etching was used to etch the surface of the wafer to form nano-grating steps with the height of 35 nm. For the height was so much smaller than the values required in site-flatness required by ITRS (10) that it was unnecessary to care about surface roughness or deviation caused by nano-gratings during the fabrication of devices. The wafer with nano-gratings was chemically cleaned, followed by the conventional MOSFET fabrication process. The channels of transistors on the nano-grating substrates were aligned to the direction of the nano-gratings. The gate insulator of SiON film with the thickness of 2nm was grown by thermal oxidation, followed with nitridation in the NO atmosphere at 800℃. The poly Si gate electrode was formed by chemical vapour deposition at 600℃and followed by patterning, ion implantation of gate,

source and drain regions. The activation annealing was performed at 1000℃ in N_2 ambient. The standard contact metallization steps completed the device fabrication. Figure 1 shows the structure of CMOS devices on the nano-grating silicon substrate and the corss-sectional SEM picture of the nano-grating. The current in the devices on the nano-grating substrate flows along three kinds of surfaces of silicon, i.e., on the top, bottom and sidewall of each grating, which results in an effectively-enhanced channel width. In this experiment, both the nano-grating substrate and the conventional one were employed to compare the performance of devices on them. And we will call the device fabricated on the nano-grating substrate as the nano-grating device, while the one on the conventional substrate as the conventional one, and define the plain size of the device as the plain occupation area on the substrate.

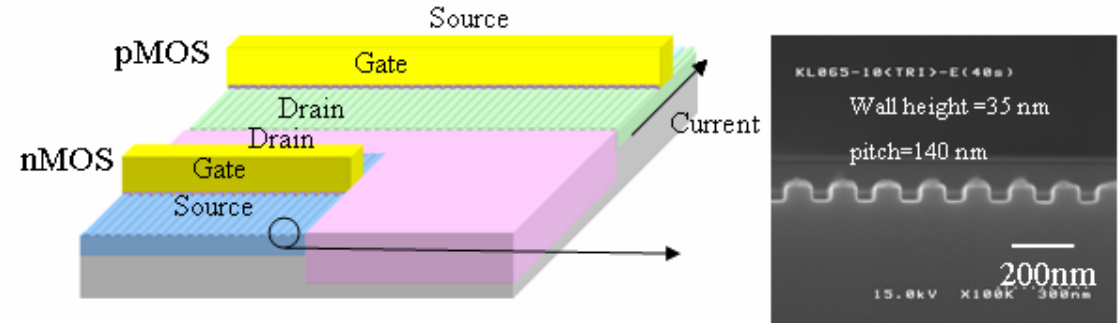


Figure1. The structure of CMOS devices fabricated on a nano-grating substrate

Device Performance

Drain current–voltage characteristics

The drain current-voltage characteristics for the nano-grating device and the conventional one in both n-type and p-type were measured. Figure 2 shows the I_d-V_{ds} characteristics of nMOSFET and pMOSFET with conventional and nano-grating channels in the same plain channel width of 5 μm and channel length of 0.25 μm.

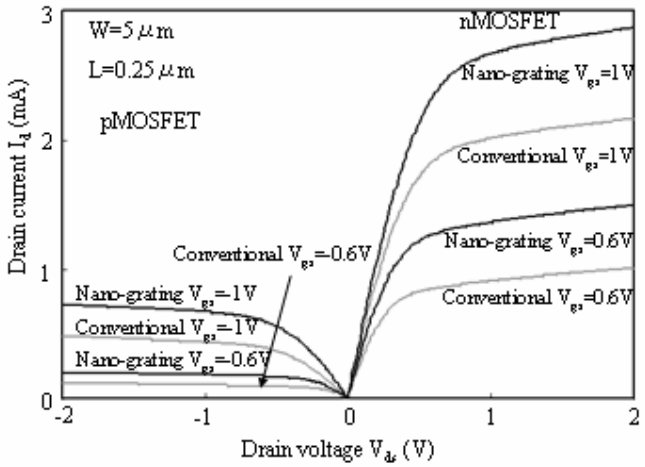


Figure2. Drain current-voltage characteristics of the nano-grating devices and the conventional ones with the same plane area

An increase of I_d current in both n-type and p-type nano-grating device was confirmed, so the nano-grating channel structure can be considered to be effective. The I_d increase, however, may be

caused by changes in threshold voltage, mobility, and gate-oxide thickness as well as channel width. The threshold voltage of nano-grating device was measured to be smaller than that of conventional one, which was considered to be due to the lower doping concentration in the nano-grating substrate when doped with the same dose as the conventional substrate (9).

Drain current-gate overdrive voltage characteristics

To take the changed threshold voltage into consideration, Fig. 3 shows the drain current-gate overdrive voltage characteristics of both the nano-grating MOSFET and the conventional one of the same plain area with the channel width of 5 μm and the channel length of 0.25 μm at the drain bias of 0.05V and 2V for n-MOSFET and -0.05V and -2V for p-MOSFET, respectively.. From Fig. 3, it can be observed that the drain current I_d had been enhanced by using the nano-grating substrate. But the enhancement of drain current I_d in nano-grating nMOSFET is smaller, while in nano-grating pMOSFET, it is larger than the enhancement estimated from the effective channel width increase which is considered to be 35% from the result of capacitance measurement, so it can be assured that there are some changes in carrier mobility, which will be discussed in detail later.

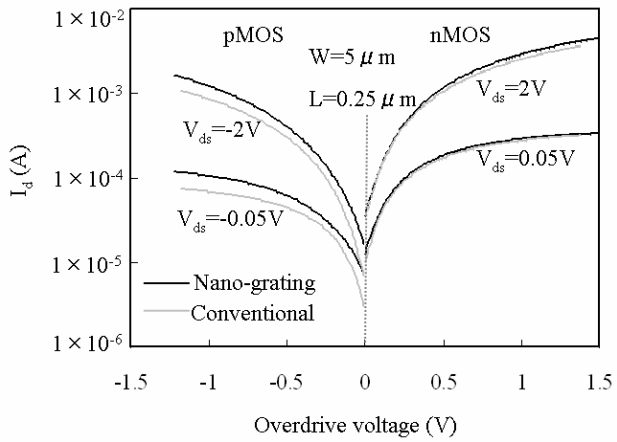


Figure3. Drain current-gate overdrive voltage characteristics of the nano-grating MOSFETs and the conventional ones with the same plane area

Transconductance characteristics

Figure 4 shows the transconductance as the function of gate voltage for the nano-grating and conventional n-MOSFETs and p-MOSFETs in the saturation region when drain voltage V_{ds}=2V or -2V, respectively. It is obvious that in both n- and p-type, the transconductance of the nano-grating device is larger than that of the conventional one with the same plain area size.

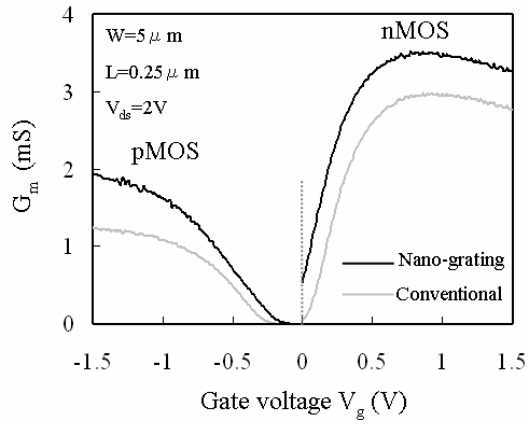
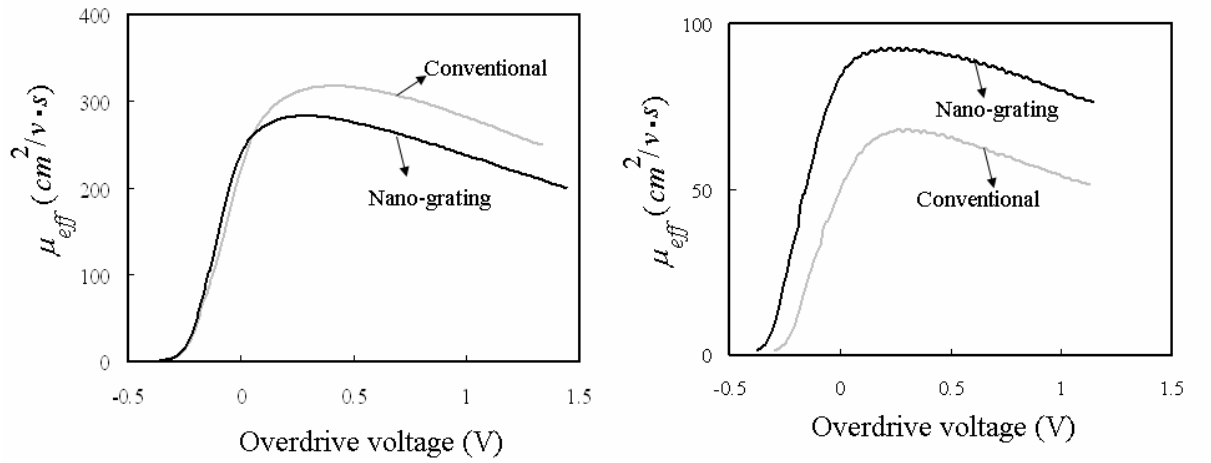


Figure4. Transconductance characteristics of the nano-grating MOSFETs and the conventional ones with the same plane size

Discussions

Effective channel mobility

Figure 5.a shows the effective electron mobility characteristics of the nano-grating and conventional n-MOSFETs versus the gate overdrive voltage. It can be clearly seen that in lower voltage region, the electron mobility in nano-grating device is larger than that in the conventional one, which is considered to be induced by the lower impurity concentration in nano-grating device. In higher voltage region, the mobility is smaller than that in conventional one. Figure 5(b) shows the effective hole mobility characteristics of the nano-grating and conventional p-MOSFETs. It is obvious that the hole mobility in the nano-grating device is larger than that in the conventional one over all the voltage region.



(a) nMOS (b) pMOS

Fig. 5 The effective mobility characteristics of the nano-grating and conventional devices

These characteristics were analyzed as follows: The current flow direction in both the nano-grating and the conventional device is <110>, and in the nano-grating device the channel region is formed on horizontal (100) and vertical (110) surfaces. So the nano-grating MOSFET can be equivalent to one conventional transistor T_1 on (100) with channel width W_1 in parallel with T_2 on (110) with channel width W_2 as shown in Fig. 6.

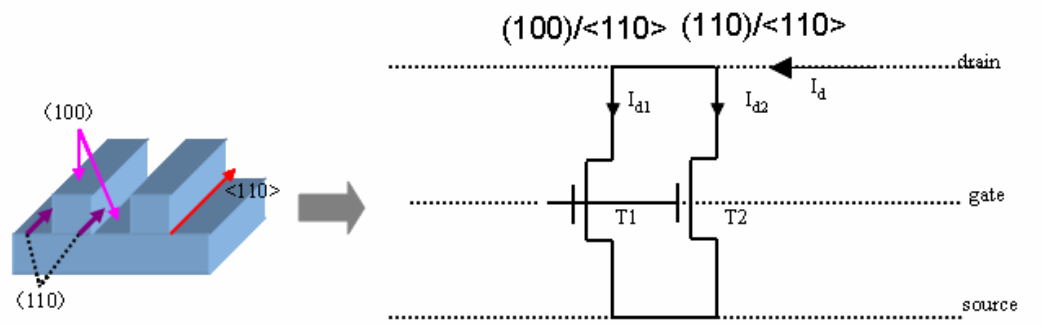


Fig. 6 The equivalent circuit of a nano-grating device

The drain current I_d of nano-grating device is the sum of currents flowing in the two transistors. So the effective carrier mobility can be deduced as

$$\mu_{eff} = \frac{W_1}{W}\mu_{eff1} + \frac{W_2}{W}\mu_{eff2}, (W = W_1 + W_2)$$

For the <110> current direction on (110) surface gives smaller electron mobility and larger hole mobility than those of <110> on (100), the average effective mobility in nano-grating nMOSFET is degraded (11), while in pMOSFET is improved, presenting a trade off between optimization of the two carrier types.

CMOS area characteristics

The basic element of CMOS circuit – an inverter was employed to investigate the area advantage of the nano-grating substrate. To achieve the minimum delay time, the current drivability of n- and p-type MOSFET must keep in the same, which is usually realized by adjusting the channel width. As shown in Table 1, for the drivability enhancement, a 0.25μm CMOS inverter circuit fabricated on the nano-grating substrate needs only 64% area of the conventional one to realize the same performance. To keep the current flowing through the pMOSFET as same as nMOSFET, the area of pMOSFET is larger than nMOSFET, and the ratio is 2.68 on (100) surface in this research, but if the nano-grating substrate is used, the ratio will decrease to 1.89, so better area balance can be achieved.

The results show that using the nano-grating substrates can enhance the drivability of device, resulting in great area advantage. And for the existence of <110> current direction on (110) surface, the mobility difference between nMOSFET and pMOSFET becomes slighter, resulting in better area balance.

Table 1 The characteristic comparison between CMOS inverters fabricated on the nano-grating and the conventional substrates

	Nano-grating		**Conventional**	
	n	p	n	p
Gm (mS/μm)	0.72	0.38	0.59	0.22
Relative transistor area	0.82	1.55	1	2.68
p/n MOSFET area ratio	1.89		2.68	
Relative CMOS inverter area	0.64		1	

Conclusion

By using nano-grating Si substrates, the CMOS-FETs with higher current drivability and area advantage compared to those on the conventional planar silicon CMOS were realized, while the fabrication process was almost the same as the conventional CMOS process except for the formation of the nano-gratings. For the existence of the <110> channel direction on (110) surface orientation, the pMOS performance such as current drivability and transconductance was enhanced more than the nMOS, enabling one to integrate higher performance pFETs without degradation of the nFETs and leading to much balanced CMOS with higher drivability.

Acknowledgments

The authors would like to thank H. Shido, M.Fukuda, and Y.Mishima with Fujitsu Laboratories Ltd. for their support.

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