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High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs

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***Abstract*—A high-efficiency CMOS rectifier circuit for UHF RFIDs was developed. The rectifier has a cross-coupled bridge configuration and is driven by a differential RF input. A differential-drive active gate bias mechanism simultaneously enables both low ON-resistance and small reverse leakage of diode-connected MOS transistors, resulting in large power conversion efficiency (PCE), especially under small RF input power conditions. A test circuit of the proposed differential-drive rectifier was fabricated with 0.18 μm CMOS technology, and the measured performance was compared with those of other types of rectifiers. Dependence of the PCE on the input RF signal frequency, output loading conditions and transistor sizing was also evaluated. At the single-stage configuration, 67.5% of PCE was achieved under conditions of 953 MHz, −12.5 dBm RF input and 10 KΩ output load. This is twice as large as that of the state-of-the-art rectifier circuit. The peak PCE increases with a decrease in operation frequency and with an increase in output load resistance. In addition, experimental results show the existence of an optimum transistor size in accordance with the output loading conditions. The multi-stage configuration for larger output DC voltage is also presented.**

***Index Terms*—Differential, power conversion efficiency (PCE), radio frequency identification (RFID), rectifier, ultra-high frequency (UHF).**

I. Introduction

THE applications of radio-frequency identification (RFID) technologies are rapidly expanding in the fields of supply chain management, access control, logistics, etc. [1]–[3]. A major type of RFID is a passive tag having no battery. Since it must be powered by the radio frequency (RF) signal radiated from a reader, the communication range is limited by the RF power transmission. RFIDs can also be categorized in terms of RF frequency. HF (13.56 MHz) RFIDs use near-field magnetic coupling for power/data transfer, resulting in a limitation of communication distance of less than 1 m. RFIDs using UHF [4], [5] or higher frequency [6], [7] bands utilize far-field electromagnetic wave transmission and have a longer communication distance. However, free-space receivable power using an appropriate antenna is proportional to λ^2 and electromagnetic waves are easily absorbed by materials at higher frequencies. Because of these factors, the communication range can be maximized by utilizing the UHF band (860–960 MHz). Recently, UHF RFID having a communication distance of 7 m has been reported [5].

The theoretical practicable operating power of an RFID tag $P_{\rm tag}$ is calculated from the Friis transmission equation:

$$P_{\rm tag} = {\rm EIRP}_{\rm reader} \cdot G_{\rm tag} \cdot \eta_{\rm rectifier} \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \qquad (1)$$

where ${\rm EIRP}_{\rm reader}$ is the effective isotropic radiation power of a reader, $G_{\rm tag}$ is the tag antenna gain, $\eta_{\rm rectifier}$ is the RF-to-DC power conversion efficiency (PCE) of the rectifier, and d is the communication distance. Note that perfect impedance matching between the tag antenna and the rectifier is assumed. From this equation, it can be concluded that in order to achieve a longer communication range of UHF RFIDs, improvement in the PCE of a rectifier circuit is a unique and effective approach because an ${\rm EIRP}_{\rm reader}$ is limited by regional regulations (4 W EIRP is the maximum transmitted power permitted in the U.S. and Japan), $G_{\rm tag}$ is roughly determined by the allowable antenna area (1.64 for the $\lambda/2$ dipole antenna), and $P_{\rm tag}$ is also roughly determined by the baseband signal processing functions implemented in the tag (generally, it varies from 10 to 100 μW in accordance with the tag functions).

The PCE of the rectifier circuit is affected by circuit topology, diode-device parameters, input RF signal frequency and amplitude, and output loading conditions. Since the input RF signal of RFIDs in long-range operations is quite small, small turn-on voltage is the most important factor for the diode device. The Schottky diode has been utilized with a multi-stage configuration despite of the additional processing cost because of its small turn-on voltage of 200–300 mV [4], [5].

The PCE for a rectifier using a diode-connected MOSFET is generally worse than that of the Schottky diode due to its large threshold voltage (Vth), but when Vth cancellation techniques are utilized, the PCE can be increased dramatically. Therefore, several techniques have been proposed to increase the PCE [7]–[11]. However, these techniques are all based on a "static" Vth cancellation technique which compensates Vth constantly, regardless of the instant RF voltage applied to the diodes. Although this is effective to reduce ON-resistance and achieve small diode loss in the forward-bias condition, reverse leakage loss increases when the gate bias voltage becomes too large.

In this paper we propose an "active" Vth cancellation scheme in which Vth can be minimized in a forward bias condition and be increased in a reverse bias condition automatically by a cross-

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coupled differential circuit configuration [12]. A test chip was designed and fabricated using 0.18 μm CMOS technology with RF options. The test chip was measured under various input and output conditions. Measured performances were compared with the previously proposed Vth cancellation rectifiers.

The paper is organized as follows. Section II defines the Power Conversion Efficiency (PCE) and then presents a qualitative analysis of the conventional rectifier circuit. Section III presents a detailed description of the proposed rectifier circuit, Section IV describes and discusses measurement results, and finally, the conclusion is presented in Section V.

II. Power Conversion Efficiency (PCE) Analysis and Conventional Rectifier Circuits

PCE of the rectifier is defined by the output power $P_{\rm OUT}$ divided by the input power $P_{\rm IN}$. The input power can be written as the sum of the output power and the loss of the rectifier $P_{\rm LOSS}$. Therefore, PCE can be written as follows:

$$\begin{aligned} {\rm PCE} &\equiv \frac{P_{\rm OUT}}{P_{\rm IN}} = \frac{P_{\rm OUT}}{P_{\rm OUT}+P_{\rm LOSS}} \\ &= \frac{P_{\rm OUT}}{P_{\rm OUT}+N\cdot P_{\rm DIODE}} \end{aligned} \tag{2}$$

where N is the number of diode stages and $P_{\rm DIODE}$ is the power loss of each diode [13], [14]. Diode loss originates from the resistive loss when current flows through the diode and can be written as follows:

$$P_{\rm DIODE} \equiv P_{\rm FWD} + P_{\rm REV} \tag{3}$$

where $P_{\rm FWD}$ and $P_{\rm REV}$ are forward diode loss and reverse diode loss, which can be determined by the turn-on voltage and the reverse leakage current of the diode, respectively. Since reverse leakage current in a conventional diode implementation is negligible, diode loss is roughly determined by the forward diode loss. Therefore, in order to realize large PCE, small turn-on voltage of the diode for reducing forward diode loss is essential.

For this purpose, a Schottky diode is utilized in rectifiers [4], [5]. It has a relatively small turn-on voltage of around 200–300 mV. The rectifier circuit using the Schottky diode achieves a large PCE, but it is not compatible with the conventional CMOS technology and requires costly fabrication processing. Instead, a diode-connected MOS transistor is widely used. Fig. 1(a) shows a conventional rectifier circuit using diode-connected MOS transistors. A unit doubler circuit composed of two-stage diodes is shown for the purpose of simplicity. Simple diode-connected n-channel MOS transistors are connected in series and an intermediate node is connected to the RF input terminal through coupling capacitor $C_{\rm C}$. The effective turn-on voltage of the diode-connected MOS transistor is almost equal to the threshold voltage of the MOS transistor, which is smaller than a pn-junction diode, but generally larger than a Schottky diode. Therefore, a rectifier utilizing this simple diode-connected MOS configuration cannot achieve a large PCE.

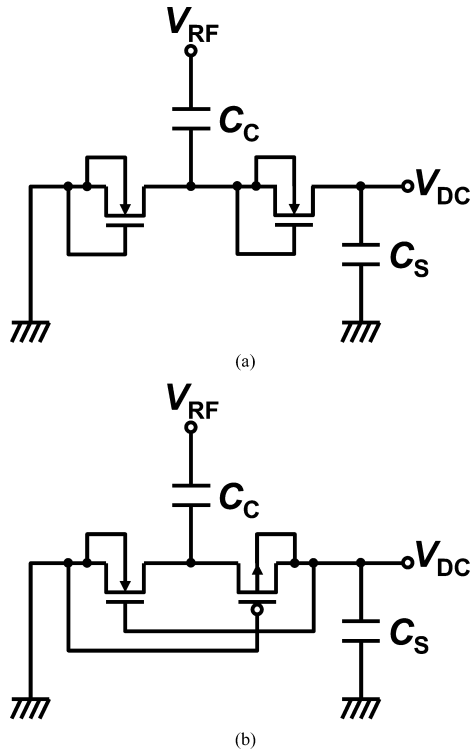

Fig. 1. Conventional rectifier circuits. (a) Simple diode connected configuration. (b) Self-Vth-Cancellation (SVC) scheme as an example of static gate biasing.

In order to reduce the effective turn-on voltage for achieving larger PCE, several Vth cancellation schemes have been proposed [8]–[11]. One uses a switched-capacitor technique to generate DC gate bias voltage from an external power supply [8] and others generate DC gate bias voltage from the output voltage of the rectifiers themselves [9]–[11]. Among them, Fig. 1(b) shows the Self-Vth-Cancellation (SVC) rectifier [10], [11], which achieves the highest PCE at low input power conditions. Gate electrodes of the nMOS transistor and the pMOS transistor are connected to the output terminal and ground terminal, respectively. Gate-source voltages of the nMOS and pMOS transistors are "statically" biased using the output DC voltage, thus reducing the effective Vth of the MOS transistors. When the DC bias voltage is not so large and the effective threshold voltage of MOS transistors is not so small, we can ignore the reverse leakage current, and therefore energy loss in the rectifier circuit is caused only by resistive loss in the forward bias condition as described above. Therefore, PCE is roughly determined by the effective ON-resistance of the diode-connected MOS transistor and the minimization of the effective threshold voltage of MOS transistors results in a large PCE. However, when the effective threshold voltage of the MOS transistor is too small due to the excessive DC bias voltage, for instance, when it becomes negative, the MOS transistor is always ON and increased reverse leakage current cannot be ignored. If the reverse leakage current is not negligible, it directly results in energy loss since charges flowing in a reverse direction are simply wasted. Therefore, reverse diode loss $P_{\rm REV}$ rapidly increases. In addition, the forward current

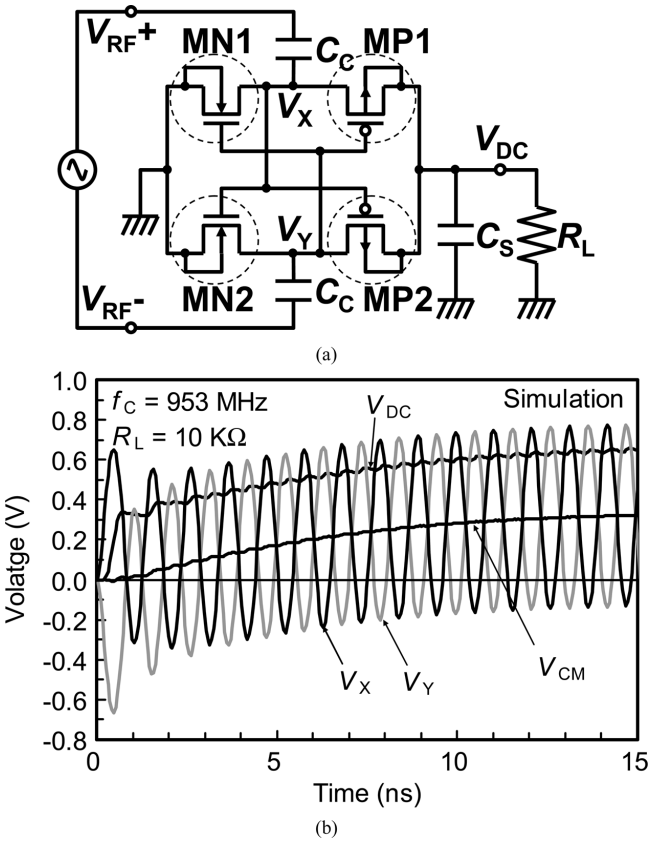

Fig. 2. Differential-drive CMOS rectifier circuit proposed in this study. (a) Circuit schematic. (b) Voltage waveforms of internal nodes.

must be further increased to compensate the reverse leakage current, thus further increasing energy loss. As a result, it is concluded that we cannot achieve a small ON-resistance and a small reverse-leakage current at the same time by "static" Vth cancellation schemes.

III. Proposed Differential-Drive CMOS Rectifier Circuit

Fig. 2(a) shows the unit stage of the newly developed differential-drive CMOS rectifier circuit. The circuit has a cross-coupled differential CMOS configuration with a bridge structure. This kind of circuit topology is known as a low-frequency rectifier circuit and is sometimes applied to the rectifier in RFIDs without actual test-chip measurement and/or detailed performance analysis [15]. We analyzed it thoroughly under various operating conditions and found that it is also very effective as a high-frequency rectifier for RFIDs. Voltage waveforms of internal RF nodes $V_{\rm X}$ and $V_{\rm Y}$ obtained by simulation are shown in Fig. 2(b). Common-mode voltage $V_{\rm CM}$, which is almost the same as the DC components of $V_{\rm X}$ and $V_{\rm Y}$ and is about half of the output DC voltage $V_{\rm DC}$ under the steady-state condition, is generated by a rectification operation and acts as a kind of static gate bias voltage compensating Vth, as in the previous static Vth cancellation schemes. In addition, in this differential scheme, the gate of transistors is actively biased by a differential-mode signal. When $V_{\rm X}$ is negative, which corresponds to the forward bias condition for the nMOS MN1 diode, the gate voltage of MN1, which is $V_{\rm Y}$, is positively biased and effectively decreases the turn-on voltage of MN1, resulting in a small ON-resistance. On the other hand, when $V_{\rm x}$ becomes positive, which corresponds to the reverse bias condition, the gate voltage rapidly decreases, which effectively reduces the reverse leakage current.

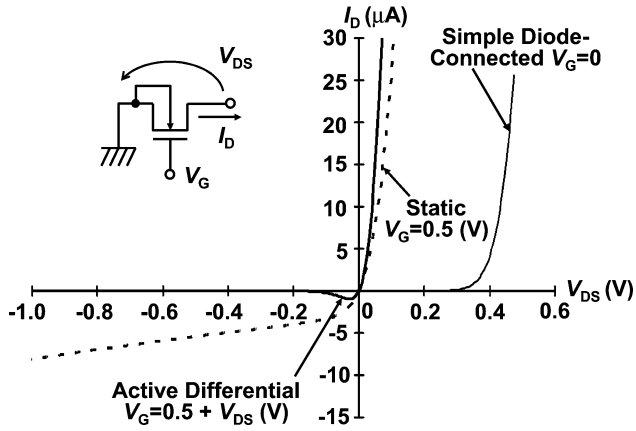

Fig. 3. I-V characteristics of diode-connected n-channel MOS transistors.

Fig. 3 shows measured *I–V* characteristics of a diode-connected nMOS transistor. Gate length and width of the MOS transistor are 0.18 μm and 3.6 μm, respectively. In the figure, the static Vth cancellation and the active differential Vth cancellation schemes are compared. DC bias voltage for both schemes is set at 0.5 V as an example. In the static Vth cancellation case, static gate bias voltage reduces ON-resistance in contrast with the zero-bias condition (simple diode-connected), but also increases the reverse leakage current, which leads to diode loss and degradation of the PCE. On the other hand, in the active differential Vth cancellation scheme, reverse leakage current can be immediately suppressed by a negative gate bias. As a result, both smaller ON-resistance and smaller reverse leakage current are simultaneously obtained.

The operation mechanism of the rectifier circuit is described in the following. When some amount of input power is applied, the rectifier starts its operation and reaches steady state in a short time. The output DC voltage $V_{\rm DC}$ as well as the DC voltages of $V_{\rm X}$ and $V_{\rm Y}$ is determined by a balance among the three components, namely, forward-transferred charges, reverse-transferred charges and charges flowing to an output load. At the beginning of the operation, since forward-transferred charges are larger than the sum of the others, the output DC voltage $V_{\rm DC}$ and the DC voltages of $V_{\rm X}$ and $V_{\rm Y}$ increase towards their steady-state values as shown in Fig. 2(b). When the circuit is in steady state, the following equations hold:

$$\begin{cases} Q_{F\_\rm MN1} - Q_{R\_\rm MN1} = Q_{F\_\rm MP1} - Q_{R\_\rm MP1} \equiv Q_1 \\ Q_{F\_\rm MN2} - Q_{R\_\rm MN2} = Q_{F\_\rm MP2} - Q_{R\_\rm MP2} \equiv Q_2 \\ Q_1 + Q_2 = \frac{V_{\rm DC}}{R_L} T \end{cases} \quad (4)$$

where $Q_{\rm F\_MN1}$, $Q_{\rm F\_MP1}$, $Q_{\rm F\_MN2}$, and $Q_{\rm F\_MP2}$ stand for the amount of charges transferred in the forward direction through nMOS MN1, pMOS MP1, nMOS MN2 and pMOS MP2 during the unit period T, respectively, and $Q_{\rm R\_MN1}$, $Q_{\rm R\_MP1}$, $Q_{\rm R\_MN2}$, and $Q_{\rm R\_MP2}$ stand for the amount of charges transferred in the reverse direction through nMOS MN1, pMOS MP1, nMOS MN2 and pMOS MP2 during

the unit period T, respectively. Then, Q_1 and Q_2 are the net charges transferred in the forward direction during the unit period T through the upper path composed of MN1 and MP1 and the lower path composed of MN2 and MP2, respectively. The first and second equations mean that net charges transferred in the forward direction through the nMOS must be the same as those transferred through the pMOS connected in-series. The third equation means that total net charges transferred in the forward direction are equal to the charges flowing to the output load. DC voltages of $V_{\rm X}$, $V_{\rm Y}$, and $V_{\rm DC}$ converge in order for these equations to hold. Note that if the characteristics of nMOS and pMOS are ideally symmetrical, DC voltages of $V_{\rm X}$ and $V_{\rm Y}$ become just half of the output DC voltage $V_{\rm DC}$ in the steady state. Furthermore, if the upper path and lower path are ideally matched, Q_1 equals Q_2. DC voltages of $V_{\rm X}$ and $V_{\rm Y}$ are the same and are also equal to the common-mode voltage $V_{\rm CM}$.

Similar to other rectifier circuits using a diode-connected MOS transistor, the differential-drive CMOS rectifier cannot start to operate when the voltage amplitude of the RF signal applied to a MOS transistor is smaller than the threshold voltage of the MOS transistor since the static bias voltage for the MOS transistor in the differential-drive CMOS rectifier is generated with the operation of the rectifier itself. On the other hand, the receivable power at the tag far from the reader is very weak. For instance, under the conditions where the frequency is 953 MHz, $\mathrm{EIRP}_{\rm reader}$ is 4 W, and $G_{\rm tag}$ is 1.64, the receivable power of the tag is resultantly as small as 114 μW (-9.4 dBm), assuming that the distance is 6 m. When using an antenna having an impedance of 73 Ω (the case for a free-space dipole antenna), terminal voltage is only 91 $\mathrm{mV_{RMS}}$, which is smaller than the threshold voltages of MOS transistors and is quite insufficient to drive diode-connected MOS transistors efficiently. Therefore, an impedance matching circuit is generally required between an antenna and a rectifier. By applying an appropriate impedance matching circuit, voltage amplitude larger than the threshold voltage of an MOS transistor can be obtained if the input impedance of the rectifier is high enough, which actually means that the rectifier is highly efficient. Assuming that an equivalent parallel resistance of the input impedance of the rectifier is 10 kΩ, for instance, input voltage amplitude of 1 $V_{\rm RMS}$ can be obtained under an input power of 100 μW by an ideal impedance matching circuit. Once the differential-drive CMOS rectifier starts to operate with large input voltage amplitude, generated output DC voltage effectively compensates the threshold voltage of MOS transistor, resulting in the remarkable increase in PCE. Although the loss of the impedance matching circuit itself must be considered for the overall system optimization, we ignore it in this study since it is beyond the scope of this paper. We analyze the rectifier circuits under the condition that the perfect impedance matching is obtained in order to evaluate the intrinsic performance of the rectifiers.

The proposed rectifier has a differential input configuration. It can be directly connected to antennas, such as a dipole antenna, having a balanced output. Note that it can also be directly connected to single-ended unbalanced antennas without any problem. This is because RFID tag chips in which the rectifier is integrated are self-completed without any output interconnection. Furthermore, they are coupled very weakly to the earth, absolute ground, since they are very small in size as compared with the distance to the ground in usual operating conditions. Therefore, the internal ground level of the tag can arbitrarily vary and there is no need for it to be fixed. In other words, from the standpoint of the RFID tag chip isolated from the earth, there is no difference between balanced input and unbalanced input which are defined with regard to the earth.

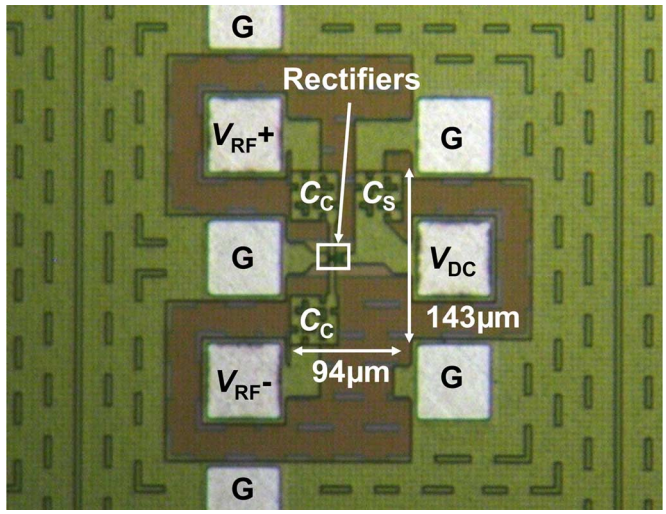

Fig. 4. Photomicrograph of fabricated differential-drive CMOS rectifier.

IV. Results and Discussion

A. Chip Design and Measurement Setup

A test chip was designed and fabricated with a 0.18 μm CMOS process having RF options. Channel width/length of nMOS and pMOS transistors were 3.6 μm/0.18 μm and 18 μm/0.18 μm, respectively, if not otherwise specified. Measured Vths for nMOS and pMOS were 0.437 V and -0.450 V, respectively. Both coupling capacitor $C_{\rm C}$ and smoothing capacitor $C_{\rm S}$ were designed to be 1.13 pF. In order to evaluate the intrinsic performance of the rectifier circuit, we did not implement an ESD protection circuit or a limiter in the test chip, although they are generally required in practical applications to protect MOS devices from high voltage.

The start-up waveforms shown in Fig. 2(b) as an example were obtained by simulation using the design parameters specified above. Although the transient response of the rectifier strongly depends on the circuit parameters and operating conditions, the output DC voltage $V_{\rm DC}$ reaches its steady state at 15 ns from the beginning in this case. This transient behavior is sufficiently fast for practical use since in conventional RFID systems, the RF signal from the reader is powered-up in several to several hundreds of micro-seconds.

A photomicrograph of the chip is shown in Fig. 4. Since shielded low-loss probing pads and MIM capacitors were used, substrate loss could be avoided.

Measurements were carried out using VNA (Agilent PNA-X) with a GSGSG differential RF probe. Since a rectifier is a large-signal nonlinear circuit, conventional mixed-mode S-parameter measurements for linear differential circuits using

a single-ended stimulus cannot be applied. In addition, since the internal ground level of the differential-drive CMOS rectifier must be fixed for a wired measurement of an output DC voltage, direct measurement by applying a single-ended signal to the differential input terminal is not possible. Of course, although nonlinear differential circuits can be evaluated for a limited frequency band by using a balun with a single-ended S-parameter measurement, it requires accurate characterization of the balun itself and common-mode signal components generated by imperfection of the circuit may degrade measurement accuracy. Thus, in this study, the True-Mode Stimulus Application (TMSA) feature of the VNA was utilized to apply a true differential stimulus signal to the test chip. Input power $P_{\rm IN}$ to the rectifier was calculated from mixed-mode S-parameters measured with TMSA by using the equation

$$P_{\rm IN} = P_S \cdot (1 - |S_{\rm dd11}|^2 - |S_{\rm cd11}|^2) \tag{5}$$

where $P_{\rm S}$ is a source power and $S_{\rm dd11}$ and $S_{\rm cd11}$ are differential-to-differential and differential-to-common mode reflection coefficients, respectively. No de-embedding procedure was conducted since substrate loss is negligible and can be ignored. A resistor $R_{\rm L}$ was connected to the DC output terminal as an output load to emulate the DC power dissipation of baseband circuits in RFIDs. Output DC voltage $V_{\rm DC}$ was measured by an oscilloscope.

B. Measured Performance

Fig. 5 shows measured PCE as a function of input RF power $P_{\rm IN}$ in dBm. The measurement was carried out at 953 MHz and an $R_{\rm L}$ of 10 KΩ. The newly developed differential-drive CMOS rectifier achieved 67.5% of the peak PCE at −12.5 dBm of RF input, which is the highest PCE ever reported, and specifically, more than two times larger than the previous Self-Vth-Cancellation (SVC) scheme [10], [11]. This allows the possible operation of a tag dissipating 38 μW at an 8.5-m range under UHF RFID regulations (4 W EIRP). At this point, measured input impedance of the rectifier was 355-j1797 Ω, which corresponds to an equivalent parallel resistance and capacitance of 9.4 KΩ and 90 fF, respectively. Note that this equivalent parallel input capacitance includes parasitic capacitance of the input pads of about 30 fF. With regard to the impedance matching with an antenna, a matching circuit should be designed so as to match this impedance in order to achieve the largest total efficiency.

PCE automatically decreases as the input power increases over −10 dBm. This is a self-output power regulation function, with which the SVC scheme is also equipped, and is effective in practical rectifier operations in RFIDs. This characteristic appears since a common-mode voltage $V_{\rm CM}$, which works as a static gate bias voltage for MOS transistors in the differential-drive CMOS rectifier, becomes too large and reverse leakage current of the MOS transistors increases under the large RF input power conditions.

Fig. 6 shows the measured output DC voltage $V_{\rm DC}$ as a function of the input RF power $P_{\rm IN}$. Although PCE has peaking characteristics as described previously, $V_{\rm DC}$ monotonically increases with the increase in $P_{\rm IN}$. Therefore, there is no problem

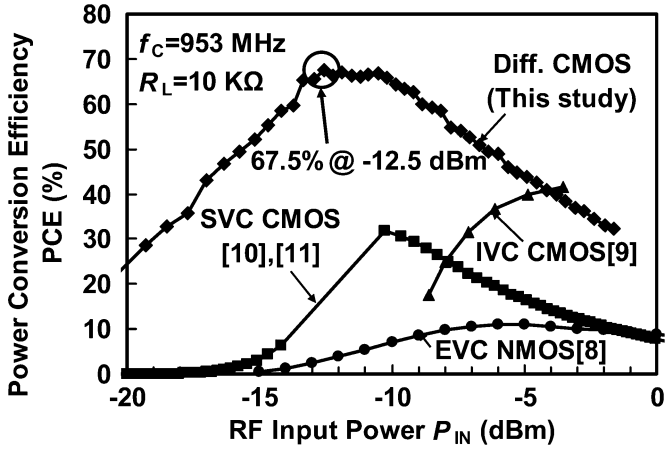

Fig. 5. Measured PCE as a function of $P_{\rm IN}$.

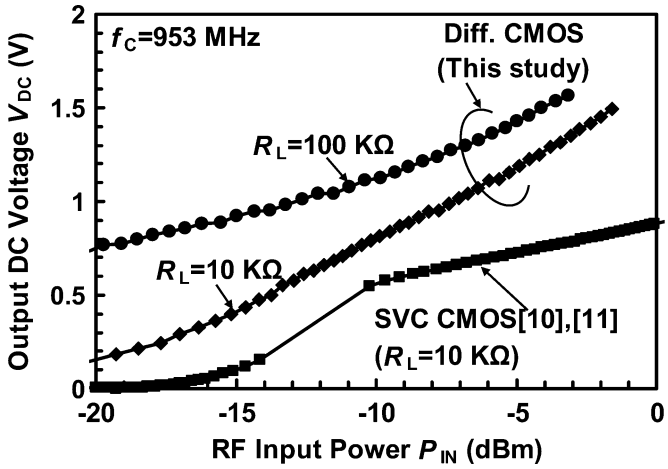

Fig. 6. Measured $V_{\rm DC}$ as a function of $P_{\rm IN}$.

in the operation stability of the RFID tags. It can be clearly seen that the differential-drive CMOS rectifier can generate larger output DC voltage than the SVC rectifier.

C. PCE Dependence on Frequency and Output Loading Condition

Fig. 7 shows PCE dependence on operation frequency. When the operation frequency increases, the PCE simply decreases. This is because energy loss caused by the parasitic resistance increases with the increase in the high-frequency current flowing in the circuit due to the increase in the input reactance. However, thanks to the high-efficiency nature of the developed rectifier, a PCE larger than 50% can be maintained at a frequency as high as 2 GHz.

When the output load resistance $R_{\rm L}$ increases, the PCE curve shifts to a smaller input power region, as shown in Fig. 8. With larger $R_{\rm L}$, the peak PCE can be obtained at a smaller input power. The value of the peak PCE increases slightly with the increase in $R_{\rm L}$. When $R_{\rm L}$ is 100 KΩ, for instance, a peak PCE of 82.6% was achieved at an input power of −24.5 dBm (3.57 μW). This result indicates that a communication range of 34 m can be realized when the power dissipation of a tag

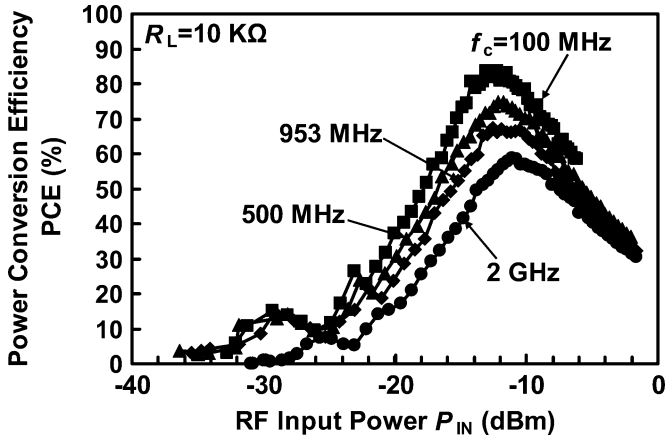

Fig. 7. Measured frequency dependence of PCE.

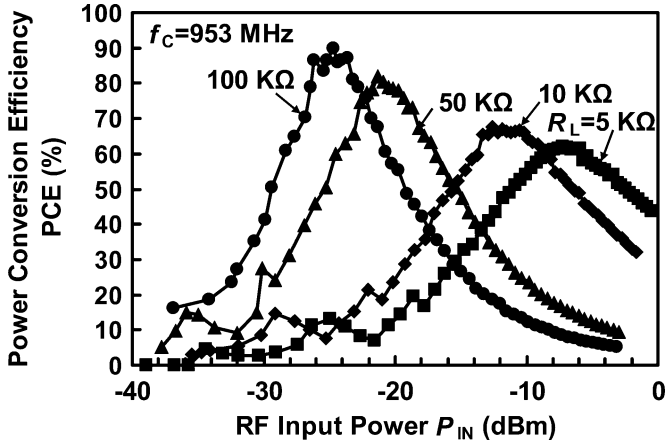

Fig. 8. Measured R_{L} dependence of PCE. PCEs are plotted as a function of P_{IN}.

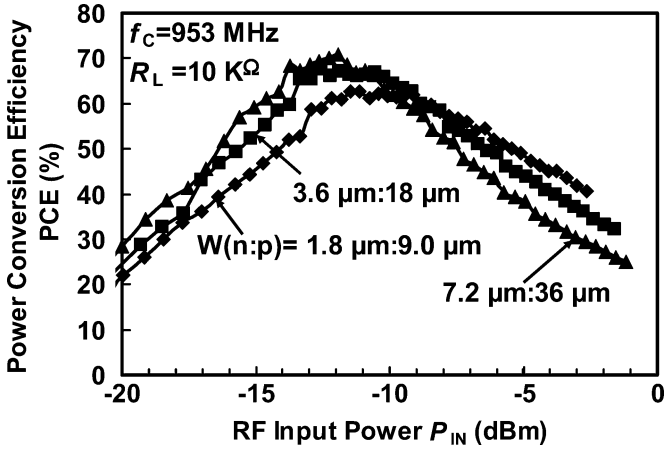

Fig. 9. Measured PCEs depending on transistor sizing.

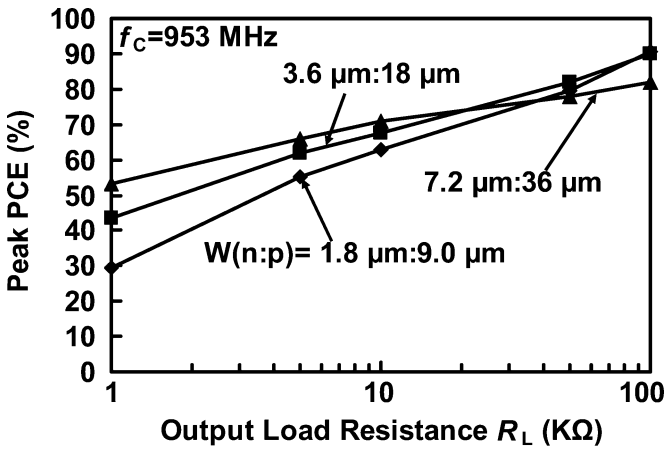

Fig. 10. Peak PCEs as a function of R_{L}.

is reduced down to 3 μW and perfect impedance matching between a tag antenna and the rectifier can be realized.

D. PCE Dependence on Transistor Sizing

Fig. 9 shows PCE dependence on transistor sizes of the rectifier. In addition to the typical case, where gate widths of n-channel and p-channel MOS transistors are designed to be 3.6 μm and 18 μm, respectively, a narrower version, where they are 1.8 μm and 9 μm, and a wider version, where they are 7.2 μm and 36 μm, were designed and measured. The gate length of MOS transistors was fixed at 0.18 μm and the width ratio between n-channel and p-channel MOS transistors was also fixed at 5, which is the best for balanced operation of the rectifier under the typical estimated conditions. Although there is not a distinct difference in transistor sizing, the wider version exhibits a slightly larger peak PCE under the condition of $R_{\mathrm{L}} = 10$ KΩ. This is because under this output loading condition, small ON-resistance of the diodes achieved by the wider transistors is more effective for achieving large PCE than the small reverse leakage current obtained by the narrower transistors.

Fig. 10 shows peak PCEs as a function of output load resistance. The narrower, typical, and wider versions are compared. When the output load resistance is small, the wider version has the largest peak PCE, while the narrower version is the best for large output loading resistance. It can be concluded that an optimal transistor size exists according to the output loading conditions and careful design is necessary.

E. Multi-Stage Configuration

In Fig. 11, PCEs of a single-stage rectifier circuit are replotted as a function of output DC voltage. Although there are some variations according to the output loading conditions, peak PCEs are obtained at an output DC voltage ranging from 0.5 V to 0.8 V. This output DC voltage is insufficient for CMOS digital baseband circuits in RFIDs, where 3–5xVth is generally required for V_{DD} power supply voltage. In order to obtain larger output DC voltage, the multi-stage configuration shown in Fig. 12 is effective. Unit stages are serially stacked along the DC path and connected in parallel to the input RF terminals. By this multi-stage configuration, we can design a rectifier circuit which can provide appropriate DC output voltage at the optimal operating point where the maximum PCE can be obtained.

It should be noted that, ideally speaking, when constructing a multi-stage configuration, we can eliminate an inter-stage smoothing capacitor C_{S} in the case of the differential-drive CMOS rectifier as shown in the figure. The forward current of MP11 injected into the inter-stage node between the first

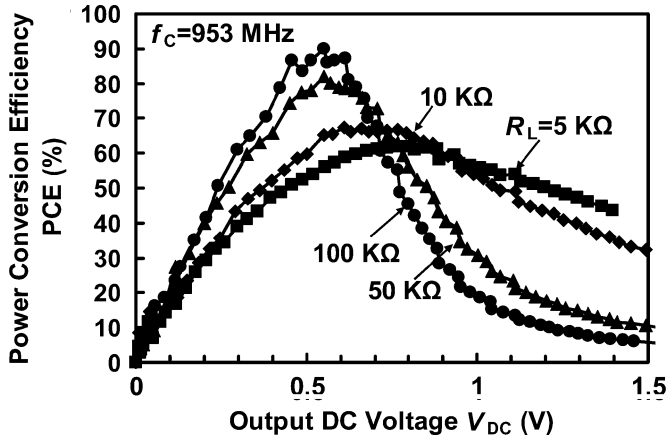

Fig. 11. Measured PCEs as a function of $V_{\rm DC}$.

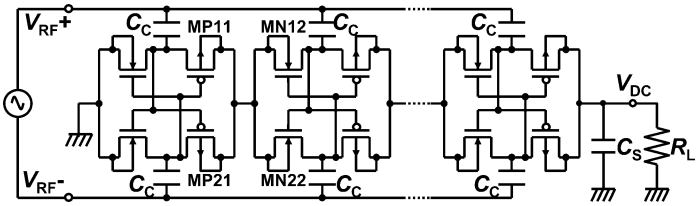

Fig. 12. Multi-stage configuration.

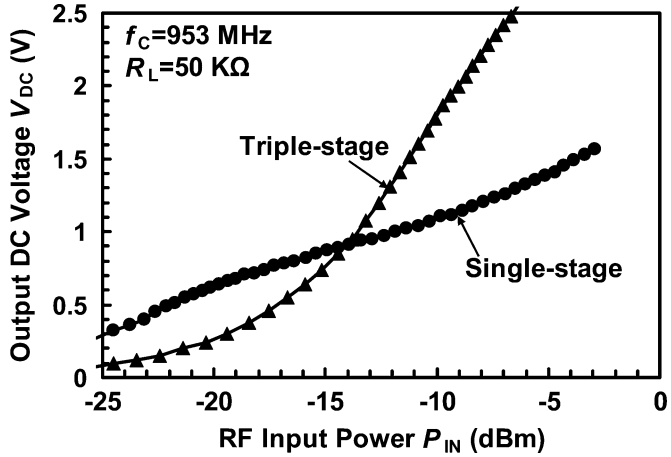

Fig. 13. Measured $V_{\rm DC}$ as a function of $P_{\rm IN}$. Single-stage and three-stage configurations are compared.

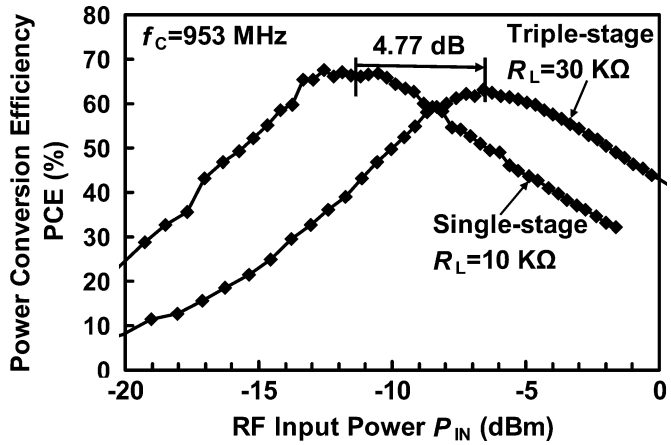

Fig. 14. Measured PCEs as a function $P_{\rm IN}$. A single-stage rectifier has a 10 K Ω output load, while a three-stage rectifier drives a 30 K Ω output load.

and second stages, for instance, is simultaneously sunk by forward-biased MN22. In the same way, the forward current of MP21 is simultaneously sunk by MN12. If nMOS and pMOS are well matched, a voltage ripple can be minimized even for a small smoothing capacitor. This is one of the interesting features of the differential-drive CMOS rectifier.

As an example of the multi-stage differential-drive CMOS rectifier, a three-stage rectifier was designed and its performance was compared with that of the single stage rectifier. Note that in the actual three-stage rectifier we designed, explicit inter-stage smoothing capacitors having a capacitance of 100 fF were added to compensate for the imperfectness of the matching between nMOS and pMOS transistors.

Fig. 13 shows output DC voltages as a function of RF input power. Output loading resistance was set at 50 KΩ. The three-stage rectifier outputs smaller DC voltage than the single-stage rectifier at an RF input power less than −14 dBm. This is because in the multi-stage configurations, PCE becomes smaller than the single-stage under small RF input power conditions. In the multi-stage configuration, unit stages are connected in parallel to the RF input as described before and this reduces the input impedance of the rectifier. Therefore, the RF signal voltage amplitude of the multi-stage rectifier becomes smaller than that of the single-stage rectifier under the same RF input power condition and this leads to the decrease in PCE since sufficient RF signal voltage amplitude larger than the threshold voltage of MOS transistors is essential for achieving higher PCE. At an RF input power larger than −14 dBm, on the other hand, the three-stage rectifier outputs larger DC voltage than the single-stage rectifier since stacked rectifier stages work effectively under the sufficiently large RF signal amplitude. When RF input power was −10 dBm, for instance, sufficient DC voltage of 1.8 V was obtained. At this operating condition, PCE was maintained at 65%.

In the three-stage configuration, each stage of the three-stage rectifier works just the same as a single-stage rectifier when a three-times-larger output loading resistance is utilized. Therefore, a three-times-larger output DC voltage can be obtained with the same PCE at the three-times-larger RF input power condition as compared with the single-stage rectifier. This was confirmed by the measurement results shown in Fig. 14. PCE characteristics of the three-stage rectifier driving 30 KΩ output loading resistance are almost the same as those estimated by simply shifting PCE characteristics of the single-stage rectifier driving 10 KΩ by 4.77 dB.

V. Conclusion

We developed a high-efficiency CMOS rectifier circuit for UHF RFIDs with an active Vth cancellation scheme. The rectifier can automatically minimize the effective Vth of diode-connected MOS transistors in a forward bias condition and automatically increase it in a reverse bias condition by a cross-coupled differential circuit configuration. The circuit has a large PCE, especially under small RF input power conditions. For example, a rectifier circuit achieved a PCE as large as 67.5% at

953 MHz, −12.5 dBm of RF input and 10 KΩ of output loading, two times larger than those of previously reported rectifiers. The multi-stage configuration was also evaluated as being effective to achieve large output DC voltage without degrading PCE.

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