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Functional gate metal-oxide-semiconductor field-effect transistors using tunnel injection/ejection of trap charges enabling self-adjustable threshold voltage for ultralow power operation

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Metal-oxide-semiconductor field-effect transistors (MOSFETs) with a functional gate, which enables self-adjustment of threshold voltage (V_{th}), were proposed for ultralow power operation and fabricated with conventional complementary metal-oxide-semiconductor (CMOS) technology. In the on-current state of fabricated nMOSFETs, electron ejection from the charge trap layer by direct tunneling makes V_{th} low and increases on-current further. In the off-current state, electron injection into the charge trap layer makes V_{th} high and suppresses subthreshold leakage current. Although the characteristic time of electron transfer of the functional gate from on-current state to off-current state is fairly long, the logic mode operating principle has been verified with the experimental device. Reduction of tunnel oxide thickness (T_{ox}) will reduce the time, which will lead to the practical use of the proposed device for CMOS logic application. © *2011 American Institute of Physics*. [doi:10.1063/1.3549178]

Extensive effort has been devoted to scaling metal-oxide-semiconductor field-effect transistors (MOSFETs) for low power consumption large-scale integrated circuits (LSIs).[1] The introduction of high-k gate dielectrics has also been intensively studied for power reduction.[2,3] However, the fundamental difficulty in decreasing threshold voltage (V_{th}) and/or *S*-factors in scaling MOSFETs limits the further reduction of power supply voltage. *S* denotes subthreshold swing. As power (*P*) is proportional to $V_{DD}{}^2$ (V_{DD} is the power supply voltage), a lowering of V_{th} by 0.1 V with keeping the gate overdrive voltage same corresponds to a 20% reduction of power consumption in advanced complementary metal-oxide-semiconductor (CMOS) LSIs. However, a lowering in V_{th} generally accompanies an increase in the off-current. To avoid this increase, it is necessary to achieve a small *S*-factor or to adjust V_{th} to a high value in the off-current state and to a low value in the on-current state. To date, tunnel field-effect transistors (FETs),[4] ferroelectric-gate FETs,[5,6] and suspended-gate MOSFETs[7,8] have been proposed and have attracted significant interest to achieve *S*-factors lower than 60 mV/sec. However, there are still issues with these potential devices for process cost and compatibility with already existing CMOS fabrication technology. In this study, we propose a MOSFET with a functional gate that enables V_{th} self-adjustment for low power operation. We fabricated a prototype device with conventional CMOS fabrication technology and showed the fundamental device characteristics necessary for low power logic operation.

A schematic diagram is shown in Fig. 1. The structure of the proposed MOSFET resembled that of the conventional floating gate memory. Only the difference was that a thin tunnel gate SiO_2 existed between the floating gate and top gate electrode for the proposed functional gate. Electrons transferred between the floating gate and the top gate electrode in the proposed device. The thicknesses of the tunnel gate oxide (T_{ox}) and lower gate oxide were 1.2 and 10 nm, respectively. The poly-Si floating gate was formed for the charge trap layer. The thickness of the floating gate was 70 nm. The device fabrication process was similar to that of the floating gate memory previously reported[9–11] with a slight modification. Silicon-on-insulator wafer wafer was used and electron beam lithography was utilized to define the floating gate and channel. The thickness of the Si channel was 60 nm. The channel width and length were 1.0 and 18 μm, respec-

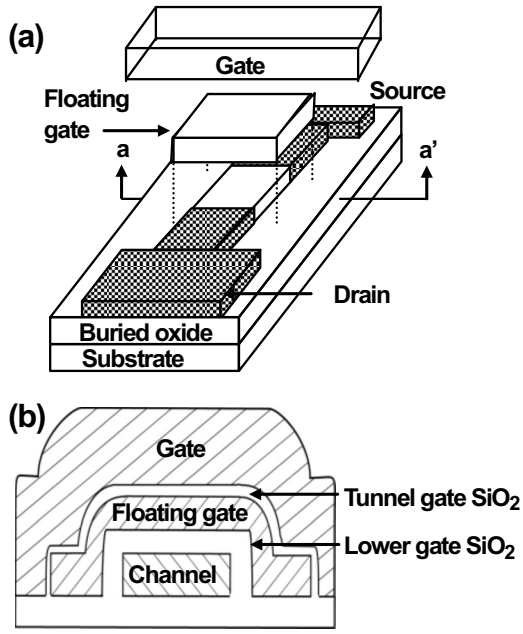

FIG. 1. (a) Schematics of fabricated functional gate MOSFET. The shaded regions are heavily As^+ implanted. (b) Cross-sectional view along a-a′ line in (a). Thicknesses of the tunnel gate oxide, lower gate oxide, and Si channel were 1.2, 10, and 60 nm, respectively.

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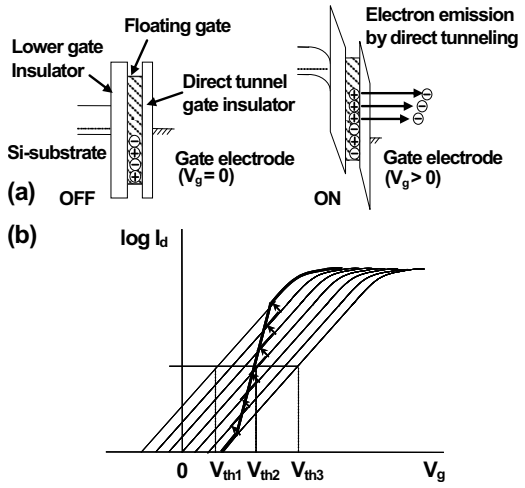

FIG. 2. (a) Band diagram of functional gate structure for the proposed MOSFET in the off-current and on-current states. (b) Operating principle of self-adjustment of threshold voltage for ultralow power operation of the proposed functional gate MOSFET.

tively. After defining the channel area and forming the lower gate oxide, an amorphous Si film was deposited for the floating gate. Then, the resist line was formed parallel to the channel, and dry etching was carried out to define the width of the floating gate. The width of the floating gate was 1.6 μm, which was slightly larger than that of the channel. While the tunnel gate oxide was formed, the amorphous Si of the floating gate changed to poly-Si. After that, a poly-Si film was deposited for the top gate electrode. The resist line was formed perpendicularly across the channel, and the dry etching was stopped upon reaching the lower gate oxide. The length of the floating gate and the top gate electrode were the same (1.0 μm) using this self-aligned etching process.

The band diagram of the functional gate structure and operation principle of the proposed nMOSFET are shown in Figs. 2(a) and 2(b), respectively. Since the gate voltage (V_g) was sufficiently low in the off-current state, no electron transfer occurred from the floating gate to the top gate electrode [Fig. 2(a)], keeping V_{th} high [V_{th3} in Fig. 2(b)]. On the other hand, V_g was large enough in the on-current state, and electrons transferred from the floating gate to the top gate electrode [Fig. 2(a)]. This led to additional lowering of the surface potential of the channel, making V_{th} low [V_{th1} in Fig. 2(b)] and increasing the on-current further. In this way, the proposed MOSFET could increase the on-current without increasing the off-current, leading to ultralow power operation.

Figure 3 shows the dependence of drain current (I_d)-V_g characteristics on bias V_g application. In Fig. 3(a), V_{th} was measured after the positive bias V_g (which varied from 1 to 10 V with a voltage step of 1 V) was applied to the gate electrode for 60 s. While V_{th} shift did not occur until the positive bias voltage was 7 V, V_{th} shifted to the negative side above 8 V, which was the opposite direction to that of conventional floating gate memory, showing that the trapped electrons were indeed ejected from the floating gate. Owing to the relatively large T_{ox}, V_g over 8 V was necessary to eject electrons from the floating gate by direct tunneling for 60 s of V_g application time. When V_{th} was defined as V_g at an I_d of 10^{-7} A, the value of V_{th} shift was -0.15, -0.53, and -1.06 V for a V_g application of 8, 9, and 10 V, respectively. Here, V_{th} was returned to around the initial V_{th} value by the

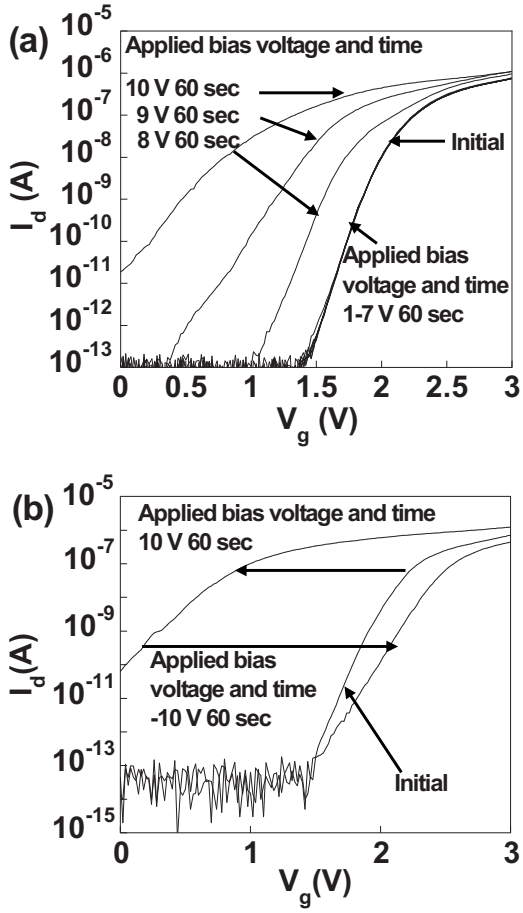

FIG. 3. Bias voltage dependence of I_d-V_g characteristics. V_d=0.1 V. (a) After 60 s of application of positive bias V_g (1–10 V with 1 V steps) was applied, I_d-V_g curve was obtained. (b) I_d-V_g characteristics after positive bias V_g application (10 V, 60 s) and subsequent negative bias V_g application (-10 V, 60 s).

procedure described later before each V_g application and the V_{th} shift were measured from the returned value. For these V_g applications, effective voltage of 0.9–1.1 V is estimated to be applied to the tunnel gate oxide. Therefore, self-adjustment of V_{th}, which increased the on-current, was realized keeping the off-current low. By the application of negative V_g, V_{th} returned to close to the initial V_{th} value [Fig. 3(b)]. After the positive V_g application of 10 V for 60 s, the subsequent negative V_g application of -10 V for 60 s made V_{th} shift to the positive side, showing the electron injection into the floating gate. The direction of the V_{th} shift was also opposite to that of conventional floating gate memory.

Figure 4 shows I_d-drain voltage (V_d) characteristics after the positive and negative bias voltage applications. Typical I_d-V_d characteristics such as clear saturation were obtained after both the positive and negative V_g applications. Consistent with the results in Fig. 3, the on-current is indeed larger after the positive V_g application of 10 V for 60 s than after the subsequent negative V_g application of -10 V for 60 s.

Figure 5 shows the dependence of I_d-V_g characteristics on time after the application of positive V_g. After the V_g application, it was seen that V_{th} slowly returned to the initial V_{th} value; electron injection into the floating gate occurred slowly. The characteristic time was found to be over an hour. Although it took a long time to become off-current state, the off-current became sufficiently low. Strictly speaking, to use the proposed device for logic applications, quick recovery

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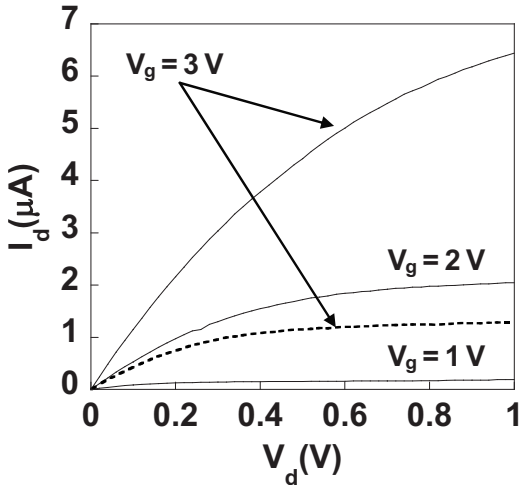

FIG. 4. I_d-V_d characteristics as a parameter of V_g after the positive bias V_g application (10 V, 60 s) (solid line) and subsequent negative bias V_g application (−10 V, 60 s) (broken line).

to the off-current state is necessary when V_g returns to 0 V from a high voltage. The way to make the time as short as 0.1 ns is to reduce T_{ox} to 0.5 nm. According to an extrapolation from the experimental data of electron tunneling injection/ejection,[12] the time becomes as short as 0.1 ns when T_{ox} is reduced to 0.5 nm. Though it looks very difficult to realize such a thin T_{ox}, it will be possible utilizing techniques such an atomic layer deposition (ALD).[3,13–16] Indeed, a thin (physical thickness of 0.5 nm) Si nitride was successfully deposited on a Si substrate by ALD as a barrier layer of ZrO_2 gate dielectrics.[15,16] For a thin tunnel oxide with T_{ox} =0.5 nm, tunnel current density is simulated to be about 10^5 A/cm^2 at a gate voltage of 0.5 V for an n$^+$-gate/p-Si nMOSFET.[17] Using the tunnel current density, the injected/ejected charge amount ΔQ to/from the floating gate is 10^{-5} C/cm^2 during a switching time of 0.1 nm. Then, the threshold voltage shift ΔV_{th} accompanied with the charge injection/ejection is calculated to be 1.4 V from $\Delta V_{th} = \Delta Q / C$. Here, the capacitance C between the upper gate and

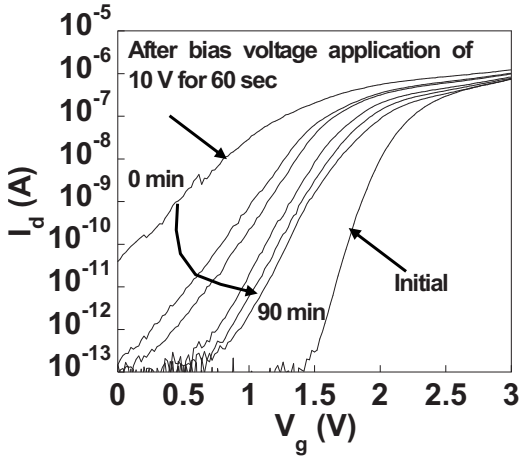

FIG. 5. Time dependence of I_d-V_g characteristics after the positive bias V_g application (10 V, 60 s). I_d-V_g curves were measured at 0, 5, 10, 30, 60, and 90 min after the V_g application. V_d=0.1 V.

the floating gate is 6.9×10^{-6} F/cm^2 since the upper gate oxide is the tunnel gate oxide (T_{ox}=0.5 nm) for the device in this study. Therefore, sufficient ΔV_{th} is considered to be obtained at T_{ox}=0.5 nm for the ultralow power logic application. It should be noted that, as far as for the ultralow power logic applications to such as watches, health care devices, or passive radio frequency integrated circuit tags, the relatively long characteristic time may be allowable and T_{ox} can be much larger than 0.5 nm.

Finally, it should be noted that for reliability enhancement, making the floating gates plural may be effective. Separating the trap charge layers into plural ones could effectively avoid the V_{th} shift caused by the production of a leakage pass as can be seen in the case of floating dot memory.[18–20]

In summary, the operating principle of functional gate MOSFETs, which enables V_{th} self-adjustment for ultralow power operation, has been proposed. A prototype device was fabricated, and fundamental device characteristics necessary for the self-adjustment of V_{th} have been demonstrated. Reduction of T_{ox} will make the characteristic time of electron transfer short and will open the way to CMOS logic applications.

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